RENESAS

RL78/G10

RENESAS MCU

True Low Power Platform (as low as 46 µA/MHz), 2.0 to 5.5V Operation,
1 to 4 Kbyte Flash for General Purpose Applications

<R> **1. OUTLINE**

1.1 Features

Ultra-Low Power Technology
- 2.0 to 5.5 V operation from a single supply
- Stop (RAM retained): 0.56 µA
- Operating: 46 µA /MHz

RL78-S1 Core
- Instruction execution: 78 % of instructions can be executed in 1 to 2 clock cycles
- CISC architecture (Harvard) with 3-stage pipeline
- Multiply: 8 x 8 to 16-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 2 clock cycle
- 1-wire on-chip debug function

Main Flash Memory
- Density: 1 to 4 Kbyte
- Flash memory rewritable voltage: 4.5 to 5.5 V

RAM
- 128 to 512 Byte size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 20 MHz with +/-2 % accuracy over voltage (2.0 to 5.5 V) and temperature (-20 to +85°C)
- Pre-configured settings: 20 MHz, 10 MHz, 5 MHz, 2.5 MHz, and 1.25 MHz

Reset and Supply Management
- Selectable power-on reset (SPOR) generator with 4 setting options

Multiple Communication Interfaces
- 1 x I^{2}C master
- 1 x I^{2}C multi-master (only for 16-pin product)
- 1 x UART (7-, 8-bit)
- Up to 2 x CSI/SPI (7-, 8-bit)

Extended-Function Timers
- Multi-function 16-bit timers: Up to 4 channels
- Interval timer: 12-bit, 1 channel (only for 16-pin product)
- 15 kHz watchdog timer : 1 channel

Rich Analog
- ADC: Up to 7 channels, 10-bit resolution, 3.4 µs conversion time
- Supports 2.4 V
- Internal reference voltage (0.815 V (typ.))
- Comparator: 1 channel (only for 16-pin product)

Safety Features
- Detects execution of illegal instruction
- Detects watchdog timer program loop

General Purpose I/O
- High-current (up to 20 mA per pin)
- Open-drain, internal pull-up support

External Interrupt
- External interrupt input: Up to 4
- Key interrupt input: 6

Operating Ambient Temperature
- Standard: -40 to +85°C

Package Type and Pin Count
- SSOP: 10 and 16 pin

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○ ROM, RAM capacities

Flash ROM	RAM	10 pins	16 pins
4 KB	512 B	R5F10Y17ASP [Note 2]	R5F10Y47ASP [Note 2]
2 KB	256 B	R5F10Y16ASP	R5F10Y46ASP [Note 2]
1 KB	128 B	R5F10Y14ASP	R5F10Y44ASP [Note 2]

Notes 1. 16-pin products only

2. Under development

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

<R> **1.2 List of Part Numbers**
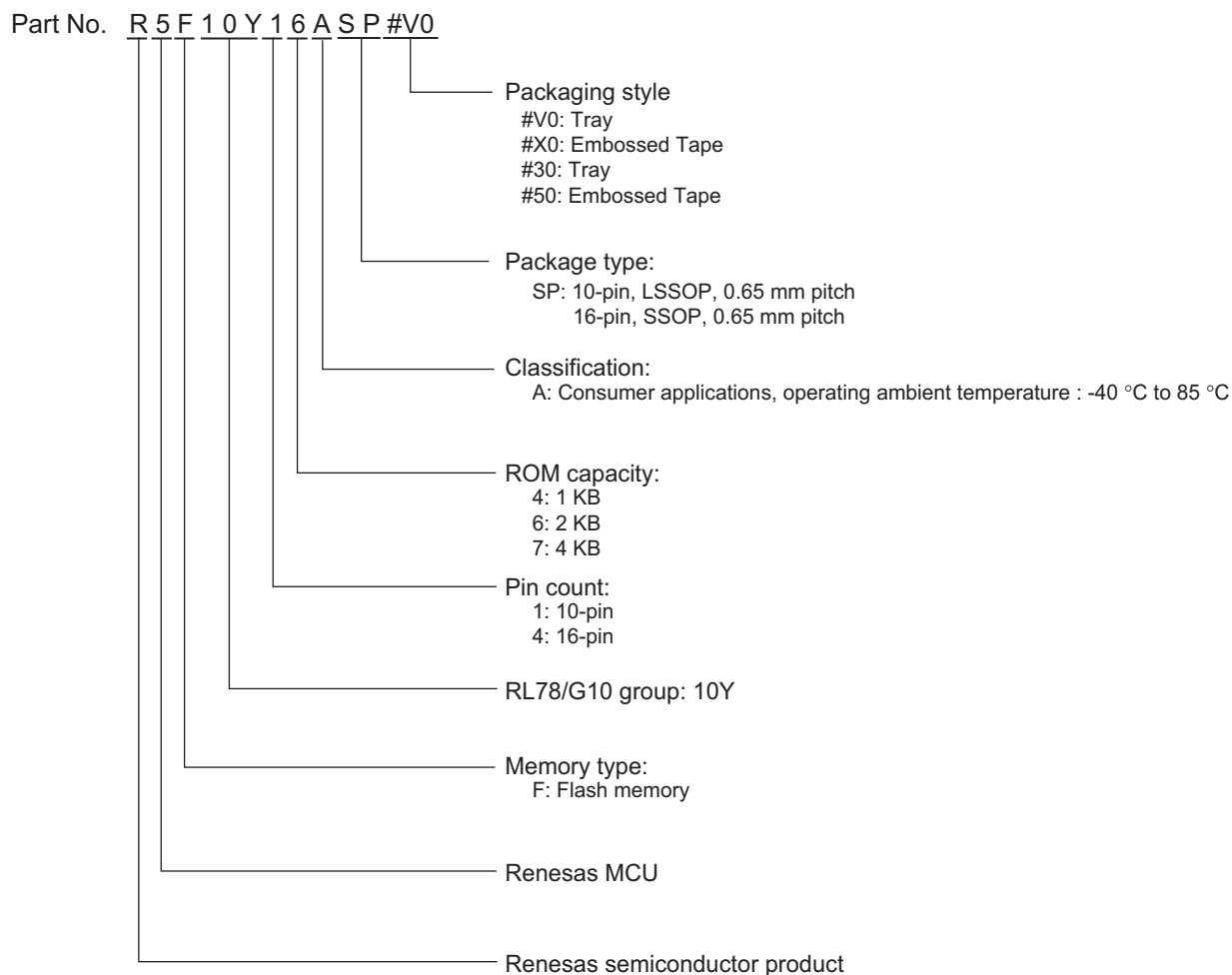
Figure 1-1. Part Number, Memory Size, and Package of RL78/G10

Part No.   R 5 F 1 0 Y 1 6 A S P #V0

- Packaging style
  - #V0: Tray
  - #X0: Embossed Tape
  - #30: Tray
  - #50: Embossed Tape

- Package type:
  - SP: 10-pin, LSSOP, 0.65 mm pitch
  - 16-pin, SSOP, 0.65 mm pitch

- Classification:
  - A: Consumer applications, operating ambient temperature : -40 °C to 85 °C

- ROM capacity:
  - 4: 1 KB
  - 6: 2 KB
  - 7: 4 KB

- Pin count:
  - 1: 10-pin
  - 4: 16-pin

- RL78/G10 group: 10Y

- Memory type:
  - F: Flash memory

- Renesas MCU

- Renesas semiconductor product

Table 1-1. List of Ordering Part Numbers

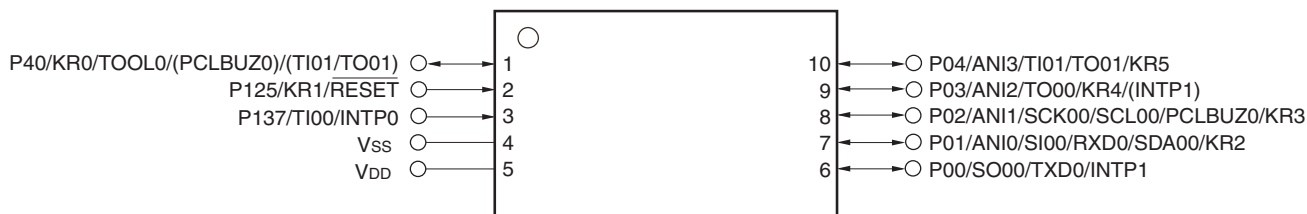| Pin count	Package	Part Number
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65 mm pitch)	R5F10Y17ASP#30 [Note], R5F10Y17ASP#50 [Note]
		R5F10Y16ASP#V0, R5F10Y16ASP#X0
		R5F10Y14ASP#V0, R5F10Y14ASP#X0
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65 mm pitch)	R5F10Y47ASP#30 [Note], R5F10Y47ASP#50 [Note]
		R5F10Y46ASP#30 [Note], R5F10Y46ASP#50 [Note]
		R5F10Y44ASP#30 [Note], R5F10Y44ASP#50 [Note]

Note   Under development

Caution   **The part number represents the number at the time of publication.**
Be sure to review the latest part number through the target product page in the Renesas Electronics Corp.website.

1.3 Pin Configuration (Top View)

1.3.1 10-pin products

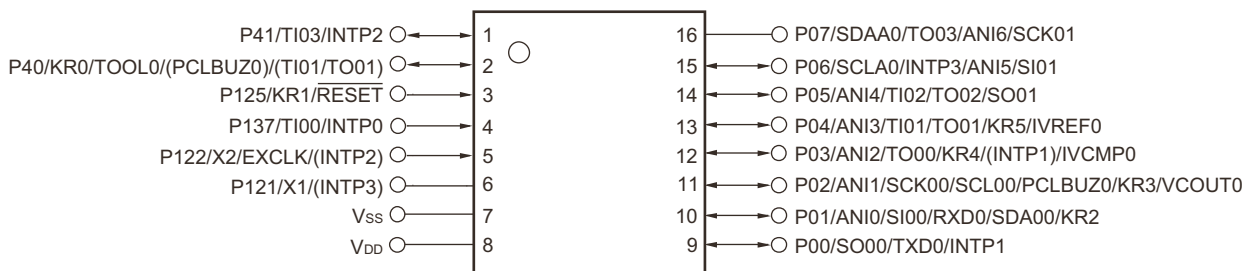- 10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65 mm pitch)

P40/KR0/TOOL0/(PCLBUZ0)/(TI01/TO01) — 1
P125/KR1/RESET — 2
P137/TI00/INTP0 — 3
Vss — 4
VDD — 5

10 — P04/ANI3/TI01/TO01/KR5
9 — P03/ANI2/TO00/KR4/(INTP1)
8 — P02/ANI1/SCK00/SCL00/PCLBUZ0/KR3
7 — P01/ANI0/SI00/RXD0/SDA00/KR2
6 — P00/SO00/TXD0/INTP1

Remarks 1. For pin identification, see **1.4 Pin Identification**.

<R>   2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-6 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G10 User's Manual.**

1.3.2 16-pin products

- **16-pin plastic SSOP (4.4 × 5.0 mm, 0.65 mm pitch)**

P41/TI03/INTP2 — 1
P40/KR0/TOOL0/(PCLBUZ0)/(TI01/TO01) — 2
P125/KR1/RESET — 3
P137/TI00/INTP0 — 4
P122/X2/EXCLK/(INTP2) — 5
P121/X1/(INTP3) — 6
Vss — 7
VDD — 8

16 — P07/SDAA0/TO03/ANI6/SCK01
15 — P06/SCLA0/INTP3/ANI5/SI01
14 — P05/ANI4/TI02/TO02/SO01
13 — P04/ANI3/TI01/TO01/KR5/IVREF0
12 — P03/ANI2/TO00/KR4/(INTP1)/IVCMP0
11 — P02/ANI1/SCK00/SCL00/PCLBUZ0/KR3/VCOUT0
10 — P01/ANI0/SI00/RXD0/SDA00/KR2
9 — P00/SO00/TXD0/INTP1

Remarks 1. For pin identification, see **1.4 Pin Identification**.

<R>   2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). See **Figure 4-6 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G10 User's Manual**.

1.4 Pin Identification

ANI0 to ANI6	: Analog Input
INTP0 to INTP3	: External Interrupt Input
KR0 to KR5	: Key Return
P00 to P07	: Port 0
P40, P41	: Port 4
P121, P122, P125	: Port 12
P137	: Port 13
PCLBUZ0	: Programmable Clock Output/ Buzzer Output
EXCLK	: External Clock Input
X1, X2	: Crystal Oscillator
IVCMP0	: Comparator Input
VCOUT0	: Comparator Output
IVREF0	: Comparator Reference Input
$\overline{\text{RESET}}$	: Reset
RxD0	: Receive Data
SCK00, SCK01	: Serial Clock Input/Output
SCL00, SCLA0	: Serial Clock Output
SDA00, SDAA0	: Serial Data Input/Output
SI00, SI01	: Serial Data Input
SO00, SO01	: Serial Data Output
TI00 to TI03	: Timer Input
TO00 to TO03	: Timer Output
TOOL0	: Data Input/Output for Tool
TxD0	: Transmit Data
V_{DD}	: Power Supply
V_{SS}	: Ground

1.5 Block Diagram

1.5.1 10-pin products
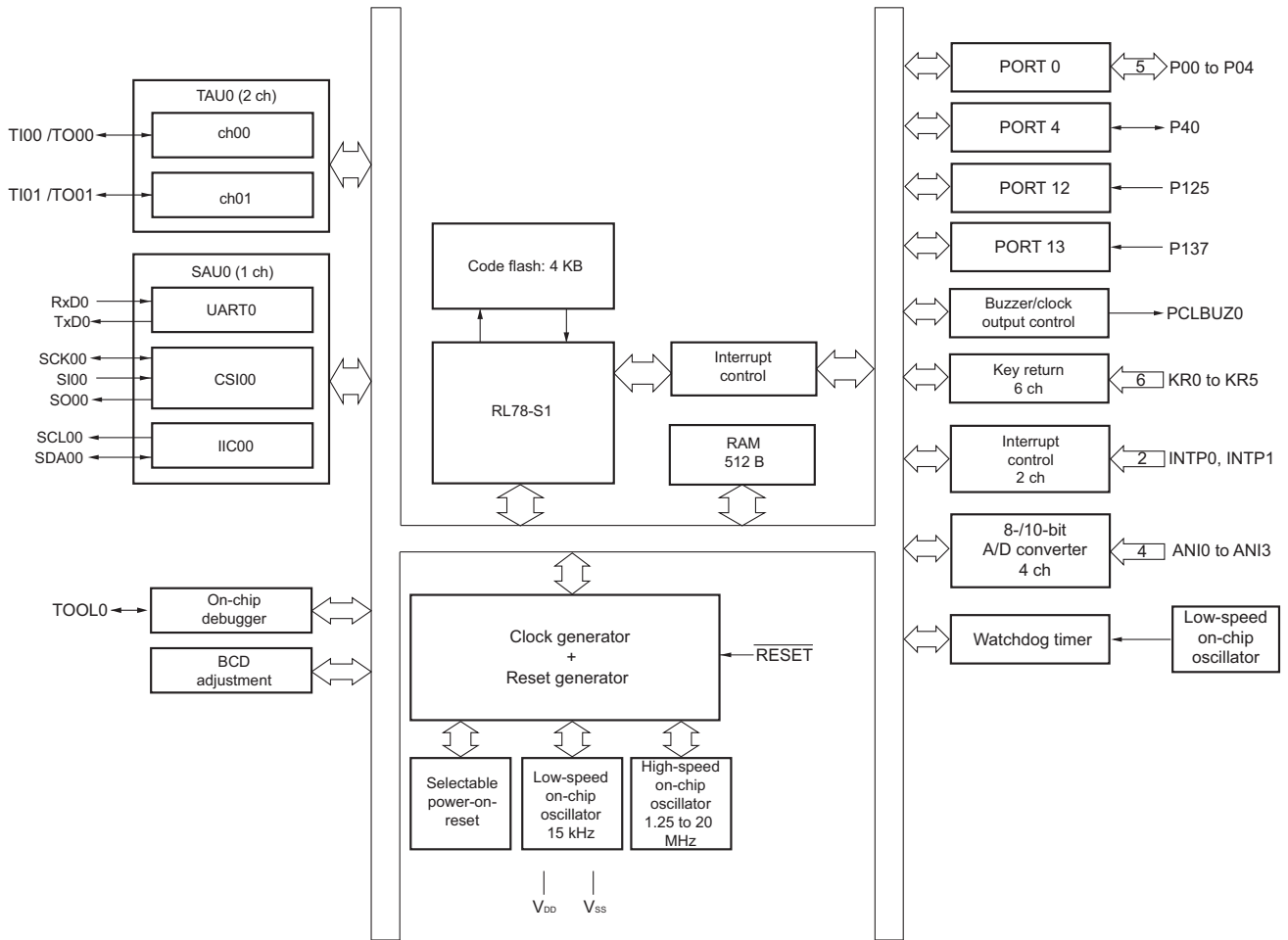
1.5.2 16-pin products
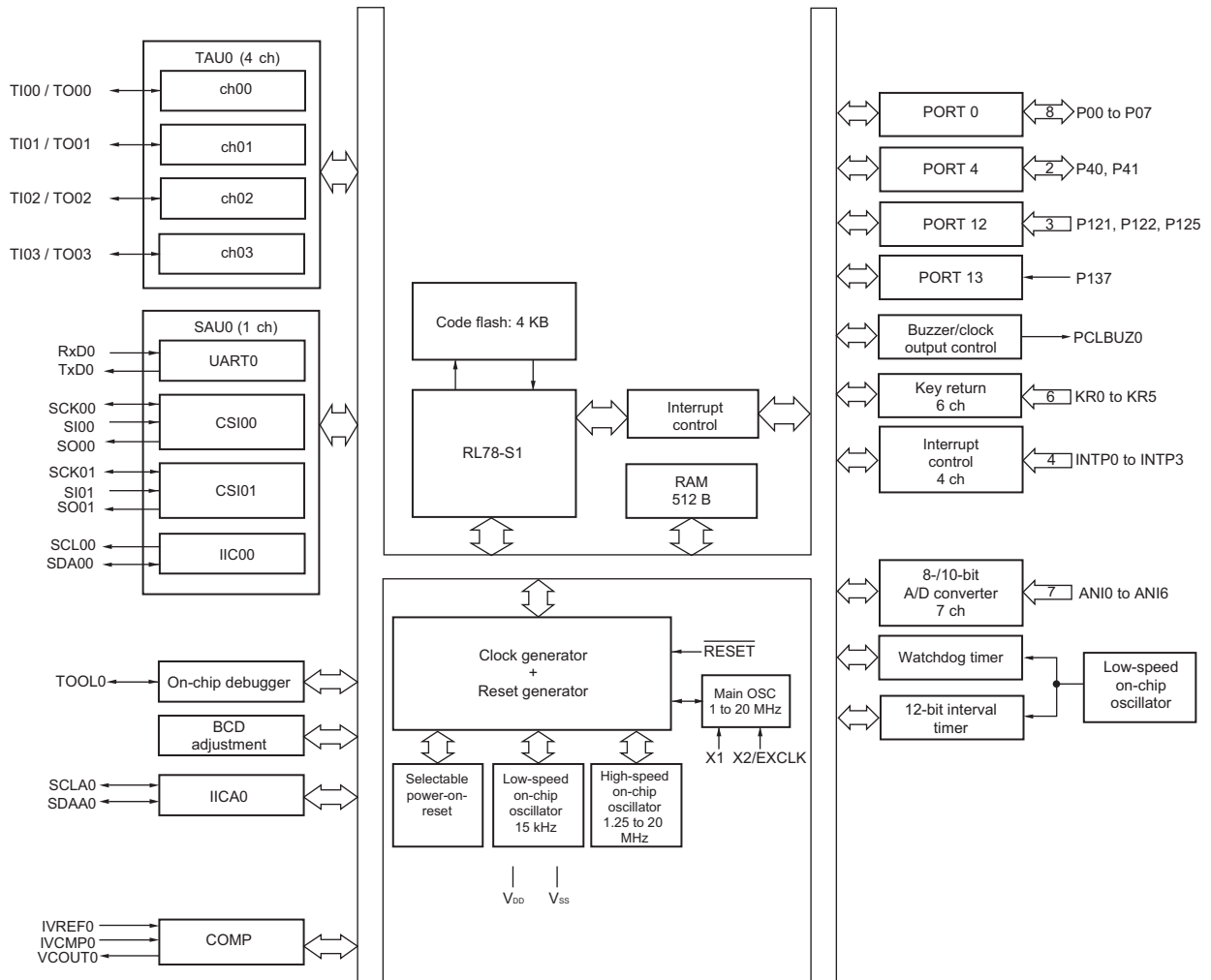
1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

<R>

Item		10-pin			16-pin		
		R5F10Y14ASP	R5F10Y16ASP	R5F10Y17ASP	R5F10Y44ASP	R5F10Y46ASP	R5F10Y47ASP
Code flash memory		1 KB	2 KB	4 KB	1 KB	2 KB	4 KB
RAM		128 B	256 B	512 B	128 B	256 B	512 B
Main system clock	High-speed system clock	—			X1, X2 (crystal/ceramic) oscillation, external main system clock input (EXCLK): 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V 1 to 5 MHz: V_{DD} = 2.0 to 5.5 V [Note 3]		
	High-speed on-chip oscillator clock	• 1.25 to 20 MHz (V_{DD} = 2.7 to 5.5 V) • 1.25 to 5 MHz (V_{DD} = 2.0 to 5.5 V [Note 3])					
Low-speed on-chip oscillator clock		15 kHz (TYP)					
General-purpose register		8-bit register × 8					
Minimum instruction execution time		0.05 μs (20 MHz operation)					
Instruction set		• Data transfer (8 bits) • Adder and subtractor/logical operation (8 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.					
I/O port	Total	8			14		
	CMOS I/O	6 (N-ch open-drain output (V_{DD} tolerance): 2)			10 (N-ch open-drain output (V_{DD} tolerance): 4)		
	CMOS input	2			4		
Timer	16-bit timer	2 channels			4 channels		
	Watchdog timer	1 channel					
	12-bit interval timer	—			1 channel		
	Timer output	2 channels (PWM output: 1)			4 channels (PWM outputs: 3 [Note 1])		
Clock output/buzzer output		1					
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f_{MAIN} = 20 MHz operation)					
Comparator		—			1		
8-/10-bit resolution A/D converter		4 channels			7 channels		
Serial interface		[10-pin products] CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel [16-pin products] CSI: 2 channels/simplified I²C: 1 channel/UART: 1 channel					
	I²C bus	—			1 channel		
Vectored interrupt sources	Internal	8			14		
	External	3			5		
Key interrupt		6					
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by selectable power-on-reset • Internal reset by illegal instruction execution [Note 2] • Internal reset by data retention lower limit voltage					
Selectable power-on-reset circuit		• Detection voltage Rising edge (V_{SPOR}): 2.25 V/2.68 V/3.02 V/4.45 V (max.) Falling edge (V_{SPDR}): 2.20 V/2.62 V/2.96 V/4.37 V (max.)					

<R>

Item	10-pin			16-pin		
	R5F10Y14ASP	R5F10Y16ASP	R5F10Y17ASP	R5F10Y44ASP	R5F10Y46ASP	R5F10Y47ASP
On-chip debug function	Provided					
Power supply voltage	V_{DD} = 2.0 to 5.5 V Note 3					
Operating ambient temperature	T_A = - 40 to + 85 °C					

Notes 1. The number of outputs varies, depending on the setting of channels in use and the number of the master
(see **6.9.4 Operation as multiple PWM output function in the RL78/G10 User's Manual**).

2. The illegal instruction is generated when instruction code FFH is executed. Reset by the illegal instruction
execution not issued by emulation with the on-chip debug emulator.

3. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage (V_{SPOR}) of the
selectable power-on-reset (SPOR) circuit should also be considered.

2. ELECTRICAL SPECIFICATIONS

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product. Refer to 2.1 Port Functions and 2.2.1 Functions for each product in the RL78/G10 User's Manual.

3. Use this product within the voltage range from 2.25 to 5.5 V because the detection voltage (V_{SPOR}) of the selectable power-on-reset (SPOR) circuit should also be considered.

<R> **2.1 Absolute Maximum Ratings**

(T_A = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			−0.5 to +6.5	V
Input Voltage	V_{I1}			−0.3 to V_{DD} + 0.3 [Note]	V
Output Voltage	V_{O1}			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin		−40	mA
		Total of all pins	P40, P41	−70	mA
			P00 to P07	−100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins	P40, P41	70	mA
			P00 to P07	100	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note   Must be 6.5 V or lower.

Caution   **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
          2. The reference voltage is V_{SS}.

<R> **2.2 Oscillator Characteristics**

2.2.1 X1 oscillator characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1		20	MHz
		2.0 V ≤ V_{DD} < 2.7 V	1		5	MHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution   **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark   When using the X1 oscillator, refer to **5.4 System Clock Oscillator in the RL78/G10 User's Manual.**

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation clock frequency [Notes 1, 2]	f_{IH}		1.25		20	MHz
High-speed on-chip oscillator oscillation clock frequency accuracy		T_A = -20 to +85°C	-2.0		+2.0	%
		T_A = -40 to -20°C	-3.0		+3.0	%
Low-speed on-chip oscillator oscillation clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator oscillation clock frequency accuracy			-15		+15	%

Notes 1.   High-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (000C2H).
2.   This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

<R> **2.3.1 Pin characteristics**

(T_A = −40 to +85°C, 2.0 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)   **(1/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for 10-pin products: P00 to P04, P40 16-pin products: P00 to P07, P40, P41				−10.0 Note 2	mA
		Total of 10-pin products: P40 16-pin products: P40, P41 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V			−20.0	mA
			2.7 V $\leq$ V_{DD} < 4.0 V			−4.0	mA
			2.0 V $\leq$ V_{DD} < 2.7 V			−3.0	mA
		Total of 10-pin products: P00 to P04 16-pin products: P00 to P07 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V			−60.0	mA
			2.7 V $\leq$ V_{DD} < 4.0 V			−12.0	mA
			2.0 V $\leq$ V_{DD} < 2.7 V			−9.0	mA
		Total of all pins (When duty $\leq$ 70% Note 3)				−80.0	mA
Output current, low Note 4	I_{OL1}	Per pin for 10-pin products: P00 to P04, P40 16-pin products: P00 to P07, P40, P41				20.0 Note 2	mA
		Total of 10-pin products: P40 16-pin products: P40, P41 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V			40.0	mA
			2.7 V $\leq$ V_{DD} < 4.0 V			6.0	mA
			2.0 V $\leq$ V_{DD} < 2.7 V			1.2	mA
		Total of 10-pin products: P00 to P04 16-pin products: P00 to P07 (When duty $\leq$ 70% Note 3)	4.0 V $\leq$ V_{DD} $\leq$ 5.5 V			80.0	mA
			2.7 V $\leq$ V_{DD} < 4.0 V			12.0	mA
			2.0 V $\leq$ V_{DD} < 2.7 V			2.4	mA
		Total of all pins (When duty $\leq$ 70% Note 3)				120.0	mA

Notes 1.   Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2.   Do not exceed the total current value.

3.   This is the output current value under conditions where the duty factor $\leq$ 70%.

The output current value when the duty factor > 70% can be calculated with the following expression (when changing the duty factor to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OH} = - 10.0 mA
  Total output current of pins = (- 10.0 × 0.7)/(80 × 0.01) $\cong$ - 8.7 mA
- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OL} = 10.0 mA
  Total output current of pins = (10.0 × 0.7)/(80 × 0.01) $\cong$ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4.   Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

Caution   P00, P01, P06, and P07 do not output high level in N-ch open-drain mode.

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

<R> **(T$_A$ = –40 to +85°C, 2.0 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)**   **(2/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$			0.8 V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$			0		0.2 V$_{DD}$	V
Output voltage, high Note 1	V$_{OH1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	I$_{OH}$ = -10 mA	V$_{DD}$ - 1.5			V
			I$_{OH}$ = -3.0 mA	V$_{DD}$ - 0.7			V
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	I$_{OH}$ = -2.0 mA	V$_{DD}$ - 0.6			V
		2.0 V ≤ V$_{DD}$ ≤ 5.5 V	I$_{OH}$ = -1.5 mA	V$_{DD}$ - 0.5			V
Output voltage, low Note 2	V$_{OL1}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V	I$_{OL}$ = 20 mA			1.3	V
			I$_{OL}$ = 8.5 mA			0.7	V
		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	I$_{OL}$ = 3.0 mA			0.6	V
			I$_{OL}$ = 1.5 mA			0.4	V
		2.0 V ≤ V$_{DD}$ ≤ 5.5 V	I$_{OL}$ = 0.6 mA			0.4	V
Input leakage current, high	I$_{LIH1}$	P00 to P07, P40, P41, P125, P137 V$_I$ = V$_{DD}$				1	µA
	I$_{LIH2}$	P121, P122 (X1, X2, EXCLK) V$_I$ = V$_{DD}$	In input port or external clock input			1	
			In resonator connection			10	
Input leakage current, low	I$_{LIL1}$	P00 to P07, P40, P41, P125, P137 V$_I$ = V$_{SS}$				-1	µA
	I$_{LIL2}$	P121, P122 (X1, X2, EXCLK) V$_I$ = V$_{SS}$	In input port or external clock input			-1	
			In resonator connection			-10	
On-chip pull-up resistance	R$_U$	V$_I$ = V$_{SS}$		10	20	100	kΩ

Notes 1. The value under the condition which satisfies the high-level output current (I$_{OH1}$).
　　　2. The value under the condition which satisfies the low-level output current (I$_{OL1}$).

Caution **The maximum value of V$_{IH}$ of P00, P01, P06, and P07 is V$_{DD}$ even in N-ch open-drain mode. P00, P01, P06, and P07 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

2.3.2 Supply current characteristics

(1) Flash ROM: 1 and 2 KB of 10-pin products

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I_{DD1}	Operating mode	Basic operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		0.91		mA
			Normal operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		1.57	2.04	
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		0.85	1.15	
	I_{DD2}[Note 2]	HALT mode		f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		350	820	µA
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		290	600	
	I_{DD3}[Note 3]	STOP mode		V_{DD} = 3.0 V			0.56	2.00	µA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. Not including the current flowing into the watchdog timer.

Remarks 1. f_{IH}: High-speed on-chip oscillator clock frequency

2. Temperature condition of the typical value is T_A = 25°C

<R> **(2) Flash ROM: 4 KB of 10-pin products, and 16-pin products**

(T_A = –40 to +85°C, 2.0 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I_{DD1}	Operating mode	Basic operation	f_{IH} = 20 MHz [Note 4]	V_{DD} = 3.0 V, 5.0 V		0.92		mA
			Normal operation	f_{IH} = 20 MHz [Note 4]	V_{DD} = 3.0 V, 5.0 V		1.59	2.14	
				f_{IH} = 5 MHz [Note 4]	V_{DD} = 3.0 V, 5.0 V		0.87	1.20	
				f_{MX} = 20 MHz [Notes 5, 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		1.43	1.93	
					Resonator connection		1.54	2.13	
				f_{MX} = 5 MHz [Notes 5, 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		0.67	1.02	
					Resonator connection		0.72	1.12	
	I_{DD2}[Note 2]	HALT mode		f_{IH} = 20 MHz [Note 4]	V_{DD} = 3.0 V, 5.0 V		360	900	µA
				f_{IH} = 5 MHz [Note 4]	V_{DD} = 3.0 V, 5.0 V		310	660	
				f_{MX} = 20 MHz [Notes 5, 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		200	700	
					Resonator connection		300	900	
				f_{MX} = 5 MHz [Notes 5, 6] V_{DD} = 3.0 V, 5.0 V	Square wave input		100	440	
					Resonator connection		150	540	
	I_{DD3}[Note 3]	STOP mode	V_{DD} = 3.0 V				0.61	2.25	µA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator (16-pin products only), I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. Not including the current flowing into the 12-bit interval timer and watchdog timer.

4. When the high-speed system clock is stopped.

5. When the high-speed on-chip oscillator is stopped.

6. 16-pin products only

Remarks 1. f_{IH}: High-speed on-chip oscillator clock frequency

2. f_{MX}: High-speed system clock frequency (X1 clock oscillator frequency or external main system clock frequency)

3. Temperature condition of the typical value is T_A = 25°C

<R> **(3) Peripheral Functions (Common to all products)**

(T_A = –40 to +85°C, 2.0 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} [Note 1]				0.30		μA
12-bit interval timer operating current	I_{TMKA} [Notes 1, 2, 3]				0.01		μA
Watchdog timer operating current	I_{WDT} [Notes 1, 4]				0.01		μA
A/D converter operating current	I_{ADC} [Notes 1, 5]	When conversion at maximum speed	V_{DD} = 5.0 V		1.30	1.90	mA
			V_{DD} = 3.0 V		0.50		mA
Comparator operating current	I_{CMP} [Notes 1, 6]	In high-speed mode	V_{DD} = 5.0 V		6.50		μA
		In low-speed mode	V_{DD} = 5.0 V		1.70		μA
Internal reference voltage operating current	I_{VREG} [Note 1]				10		μA

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{TMKA}, when the 12-bit interval timer is in operation.

4. Current flowing only to the watchdog timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{WDT} when the watchdog timer is in operation.

5. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the comparator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator is in operation.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. Temperature condition of the typical value is T_A = 25°C

2.4 AC Characteristics

(T$_A$ = –40 to +85°C, 2.0 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

<R>

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	When high-speed on-chip oscillator clock (f$_{IH}$) is selected	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.05		0.8	µs
			2.0 V ≤ V$_{DD}$ < 2.7 V	0.2		0.8	µs
		When high-speed system clock (f$_{MX}$) is selected	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.05		1.0	µs
			2.0 V ≤ V$_{DD}$ < 2.7 V	0.2		1.0	µs
External system clock frequency	T$_{EX}$		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	1.0		20	MHz
			2.0 V ≤ V$_{DD}$ < 2.7 V	1.0		5	MHz
External system clock input high-level width, low-level width	T$_{EXH}$, T$_{EXL}$		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	24			ns
			2.0 V ≤ V$_{DD}$ < 2.7 V	95			ns
TI00 to TI03 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$	Noise filter is not used		1/f$_{MCK}$ + 10			ns
TO00 to TO03 output frequency	f$_{TO}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V				10	MHz
		2.7 V ≤ V$_{DD}$ < 4.0 V				5	MHz
		2.0 V ≤ V$_{DD}$ < 2.7 V				2.5	MHz
PCLBUZ0 output frequency	f$_{PCL}$	4.0 V ≤ V$_{DD}$ ≤ 5.5 V				10	MHz
		2.7 V ≤ V$_{DD}$ < 4.0 V				5	MHz
		2.0 V ≤ V$_{DD}$ < 2.7 V				2.5	MHz
$\overline{RESET}$ low-level width	t$_{RSL}$			10			µs

**Remark**   f$_{MCK}$: Timer array unit operation clock frequency

(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n1 bit of timer mode register 0nH (TMR0nH). n: Channel number (n = 0 to 3))

<R> **Minimum Instruction Execution Time during Main System Clock Operation**

TCY vs VDD

Cycle time TCY [μs]

Supply voltage VDD [V]

— When the high-speed on-chip oscillator clock is selected

—·—· When the high-speed system clock is selected

AC Timing Test Points

V_{IH}/V_{OH} Test points V_{IH}/V_{OH}
V_{IL}/V_{OL} V_{IL}/V_{OL}

<R> **External System Clock Timing**

$1/f_{EX}$

t_{EXL} t_{EXH}

EXCLK

<R> **TI/TO Timing**

TI00 to TI03

TO00 to TO03
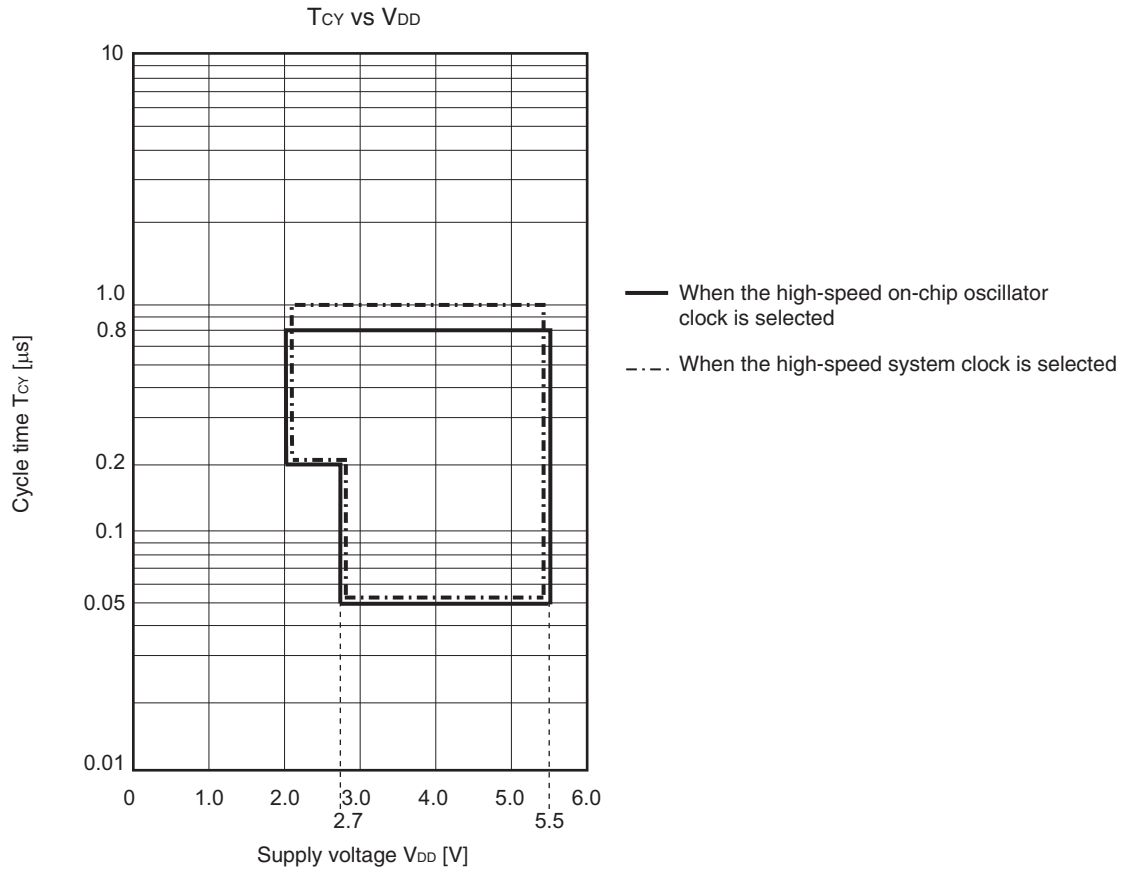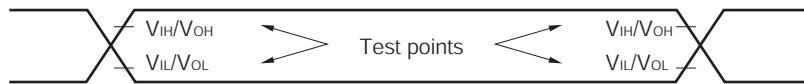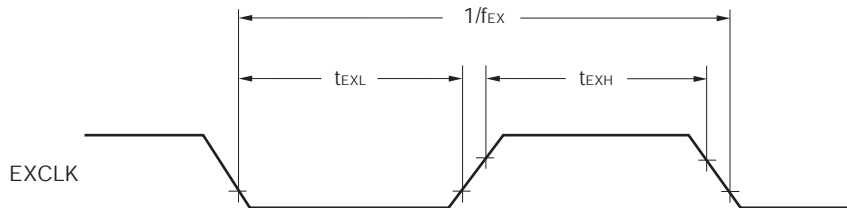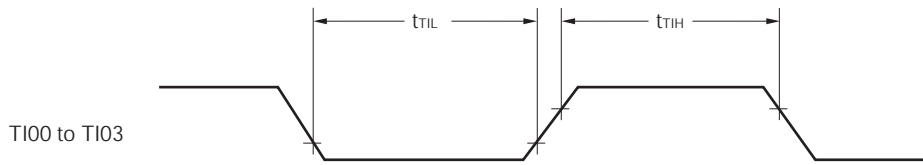
$\overline{\text{RESET}}$ Input Timing

$\overline{\text{RESET}}$
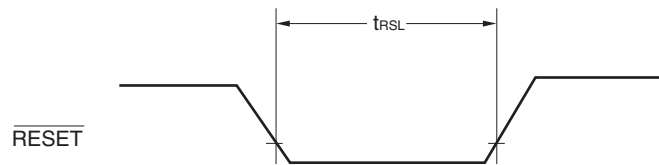
2.5 Serial Interface Characteristics

AC Timing Test Points
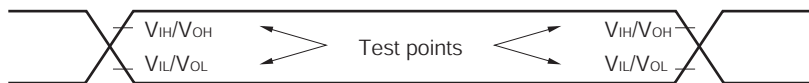
2.5.1 Serial array unit

(1) UART mode

(T_A = –40 to +85°C, 2.0 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 20 MHz			3.3	Mbps

UART mode connection diagram
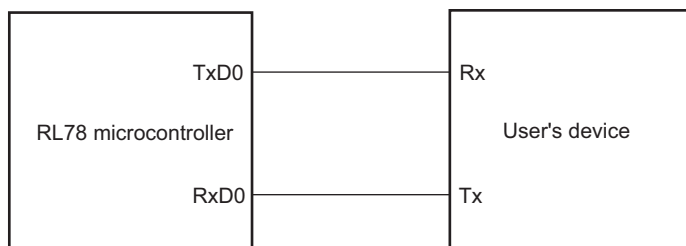
UART mode bit width (reference)
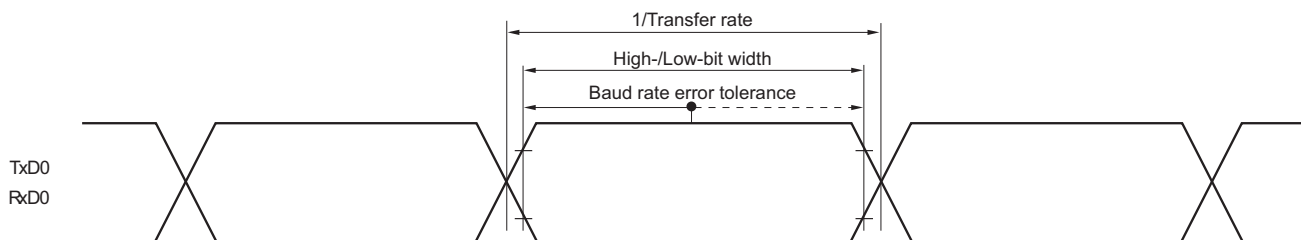
Remark f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0, 1))

(2) CSI mode (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 18			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 50			ns
SIp setup time (to SCKp↑) [Note 1]	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		47			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		110			ns
SIp hold time (from SCKp↑) [Note 1]	t_{KSI1}			19			ns
Delay time from SCKp↓ to SOp output [Note 2]	t_{KSO1}	C = 30 pF [Note 3]				25	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to SCKp↓" and SIp hold time becomes "from SCKp↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from SCKp↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

(3) CSI mode (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 16 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2			ns
SIp setup time (to SCKp↑) [Note 1]	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30			ns
SIp hold time (from SCKp↑) [Note 1]	t_{KSI2}	2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output [Note 2]	t_{KSO2}	C = 30 pF [Note 3]	2.7 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 50	ns
			2.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 110	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to SCKp↓" and the SIp hold time becomes "from SCKp↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from SCKp↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. C is the load capacitance of the SOp output lines.

Remarks 1. p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0, 1))

CSI mode connection diagram
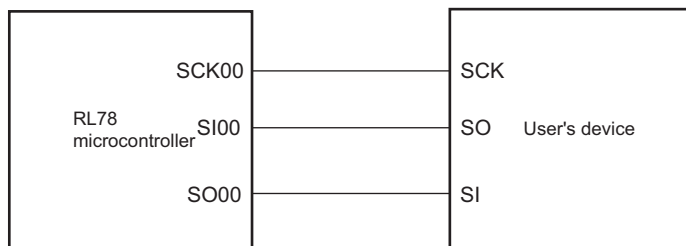
CSI mode serial transfer timing
(When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1.)
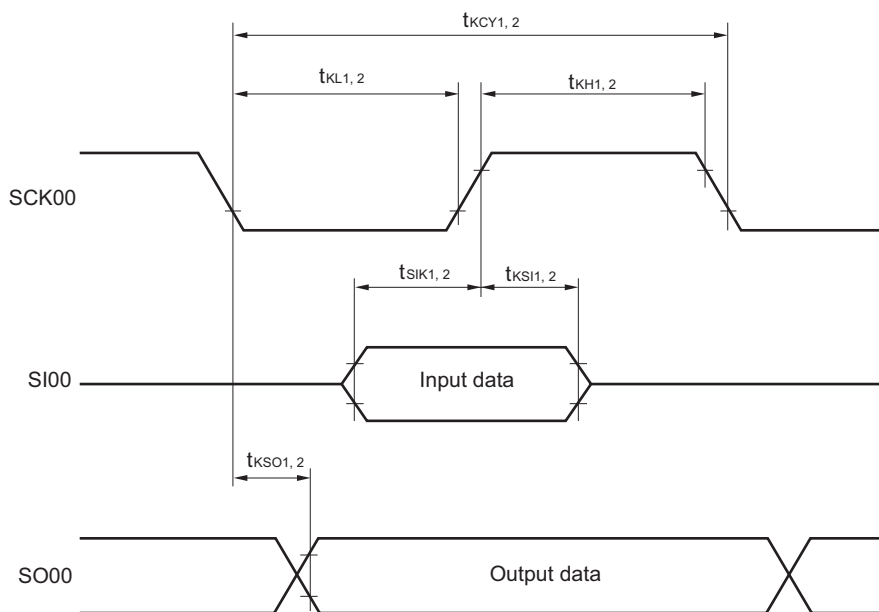
Remark   p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

(4) Simplified I²C mode

(T$_A$ = –40 to +85°C, 2.0 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f$_{SCL}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ		400 [Note 1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		ns
Hold time when SCLr = "H"	t$_{HIGH}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		ns
Data setup time (reception)	t$_{SU: DAT}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ	1/f$_{MCK}$ + 145 [Note 2]		ns
Data hold time (transmission)	t$_{HD: DAT}$	C$_b$ = 100 pF, R$_b$ = 3 kΩ	0	355	ns

Notes **1.**   The value must also be equal to or less than f$_{MCK}$/4.
      2.   Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the N-ch open drain output (V$_{DD}$ tolerance) mode for the SDAr pin by using the port output mode register 0 (POM0).

Simplified I²C mode connection diagram
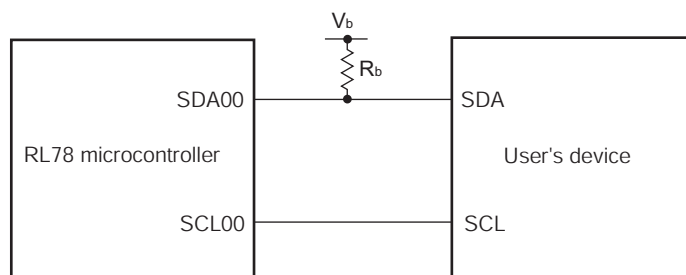
Simplified I²C mode serial transfer timing
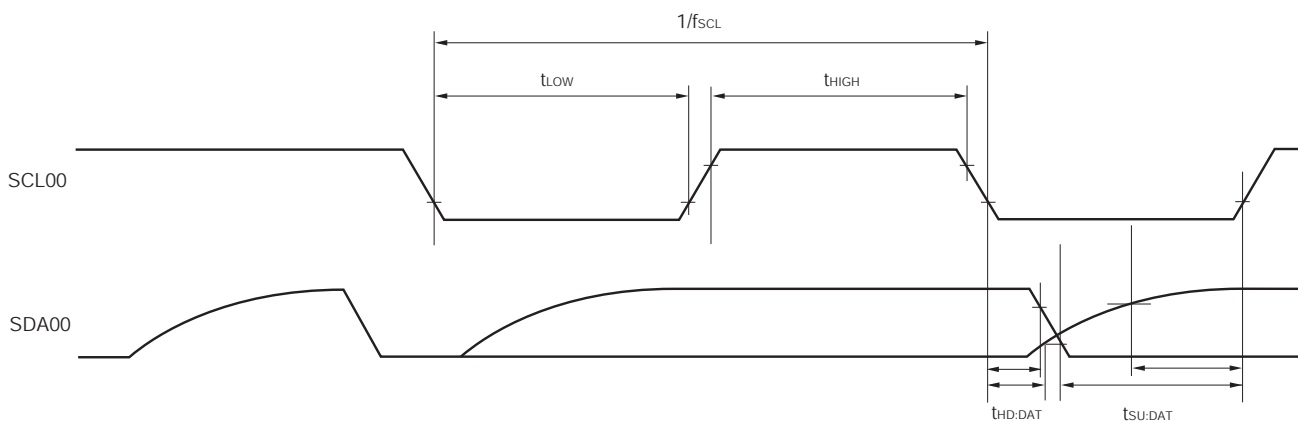
Remarks **1.**   R$_b$ [Ω]: Communication line (SDAr) pull-up resistance,
            C$_b$ [F]: Communication line (SCLr, SDAr) load capacitance
      2.   r: IIC number (r = 00)
      3.   f$_{MCK}$: Serial array unit operation clock frequency
            (Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial
            mode register 0nH (SMR0nH). n: Channel number (n = 0))

<R> **2.5.2 Serial interface IICA**

(T$_A$ = −40 to +85°C, 2.0 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ ≥ 3.5 MHz			0	400	kHz
		Standard mode: f$_{CLK}$ ≥ 1 MHz	0	100			kHz
Setup time of restart condition	t$_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	t$_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t$_{LOW}$		4.7		1.3		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$		4.0		0.6		μs
Data setup time (reception)	t$_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	t$_{SU:STO}$		4.0		0.6		μs
Bus-free time	t$_{BUF}$		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.
　　　　　2. The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$
　　　　　　(acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up
　　　　　resistor) at that time in each mode are as follows.

　　　　　Standard mode:　C$_b$ = 400 pF, R$_b$ = 2.7 kΩ
　　　　　Fast mode:　　　　C$_b$ = 200 pF, R$_b$ = 1.7 kΩ

IICA serial transfer timing
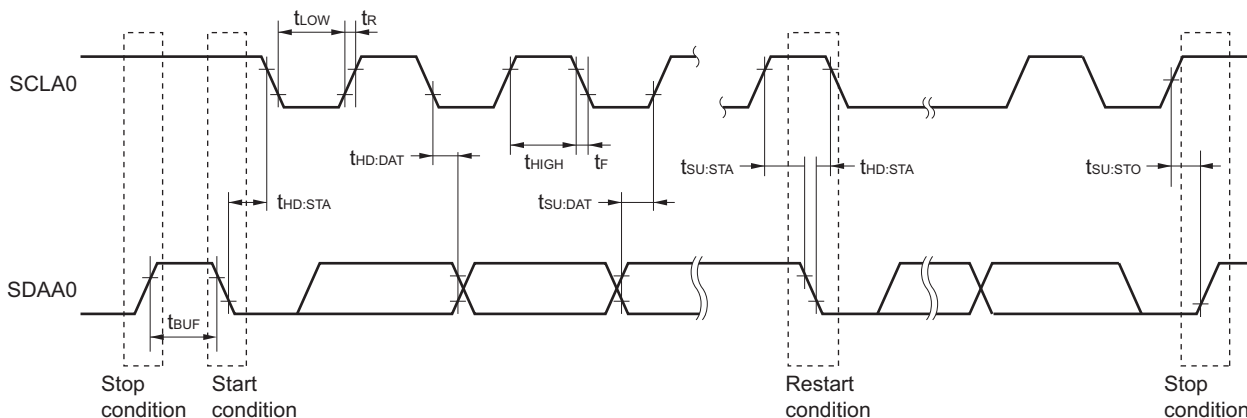
2.6 Analog Characteristics

<R> **2.6.1 A/D converter characteristics**

(Target pin: ANI0 to ANI6, internal reference voltage)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Notes 1, 2, 3]	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1	LSB
			V_{DD} = 3 V		±2.3	±4.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI6	2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		18.4	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V [Note 5]	4.6		18.4	μs
		10-bit resolution Target pin: internal reference voltage [Note 6]	2.4 V ≤ V_{DD} ≤ 5.5 V	4.6		18.4	μs
Zero-scale error[Notes 1, 2, 3, 4]	E_{ZS}	10-bit resolution	V_{DD} = 5 V			±0.19	%FSR
			V_{DD} = 3 V			±0.39	%FSR
Full-scale error[Notes 1, 2, 3, 4]	E_{FS}	10-bit resolution	V_{DD} = 5 V			±0.29	%FSR
			V_{DD} = 3 V			±0.42	%FSR
Integral linearity error[Notes 1, 2, 3]	ILE	10-bit resolution	V_{DD} = 5 V			±1.8	LSB
			V_{DD} = 3 V			±1.7	LSB
Differential linearity error [Notes 1, 2, 3]	DLE	10-bit resolution	V_{DD} = 5 V			±1.4	LSB
			V_{DD} = 3 V			±1.5	LSB
Analog input voltage	V_{AIN}	Target pin: ANI0 to ANI6		0		V_{DD}	V
		Target pin: internal reference voltage [Note 6]			V_{REG} [Note 7]		V

Notes 1. TYP. Value is the average value at T_A = 25°C. MAX. value is the average value ±3σ at normal distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

4. This value is indicated as a ratio (%FSR) to the full-scale value.

5. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when conversion is done in the operating voltage range of 2.4 V ≤ V_{DD} < 2.7 V.

6. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when the internal reference voltage is selected as the target for conversion.

7. Refer to **2.6.3 Internal reference voltage characteristics**.

Cautions 1. Arrange wiring and insert the capacitor so that no noise appears on the power supply/ground line.

2. Do not allow any pulses that rapidly change such as digital signals to be input/output to/from the pins adjacent to the conversion pin during A/D conversion.

3. Note that the internal reference voltage cannot be used as the reference voltage of the comparator when the internal reference voltage is selected as the target for A/D conversion.

<R> **2.6.2 Comparator characteristics**

(T_A = –40 to +85°C, 2.0 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	I_{VREF}	IVREF0 pin input (when C0VFR bit = 0)		0		V_{DD} - 1.4	V
		Internal reference voltage (when C0VRF bit = 1) [Note 1]			V_{REG} [Note 2]		V
	I_{VCMP}	IVCMP0 pin input		-0.3		V_{DD} + 0.3	V
Output delay	t_d	V_{DD} = 3.0 V, input slew rate > 50 mV/µs	High-speed mode			0.5	µs
			Low-speed mode		2.0		µs
Operation stabilization wait time	t_{CMP}			100			µs

Notes **1.** When the internal reference voltage is selected as the reference voltage of the comparator, the internal reference voltage cannot be used as the target for A/D conversion.

   2. Refer to **2.6.3 Internal reference voltage characteristics**.

<R> **2.6.3 Internal reference voltage characteristics**

(T_A = –40 to +85°C, 2.0 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal reference voltage	V_{REG}		0.74	0.815	0.89	V
Operation stabilization wait time	t_{AMP}	When A/D converter is used (ADS register = 07H)	5			µs

Note The internal reference voltage cannot be simultaneously used by the A/D converter and the comparator; only one of them must be selected.

2.6.4 SPOR Circuit characteristics

(T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Power supply voltage level	V_{SPOR0}	Power supply rise time	4.08	4.28	4.45	V
			Power supply fall time	4.00	4.20	4.37	V
		V_{SPOR1}	Power supply rise time	2.76	2.90	3.02	V
			Power supply fall time	2.70	2.84	2.96	V
		V_{SPOR2}	Power supply rise time	2.44	2.57	2.68	V
			Power supply fall time	2.40	2.52	2.62	V
		V_{SPOR3}	Power supply rise time	2.05	2.16	2.25	V
			Power supply fall time	2.00	2.11	2.20	V
Minimum pulse width [Note]		T_{LSPW}		300			µs

Note   Time required for the reset operation by the SPOR when V_{DD} becomes under V_{SPOR}.

<R> **Caution   Set the detection voltage (V_{SPOR}) in the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H). The operating voltage range is as follows:**
When the CPU operating frequency is from 1 MHz to 20 MHz: V_{DD} = 2.7 to 5.5 V
When the CPU operating frequency is from 1 MHz to 5 MHz: V_{DD} = 2.0 to 5.5 V

2.6.5 Power supply voltage rising slope characteristics

(T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

2.6.6 Data retention power supply voltage characteristics

(T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.9		5.5	V

Caution   Data in the RESF register is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}). Note that data in the RESF register might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}).

<R>
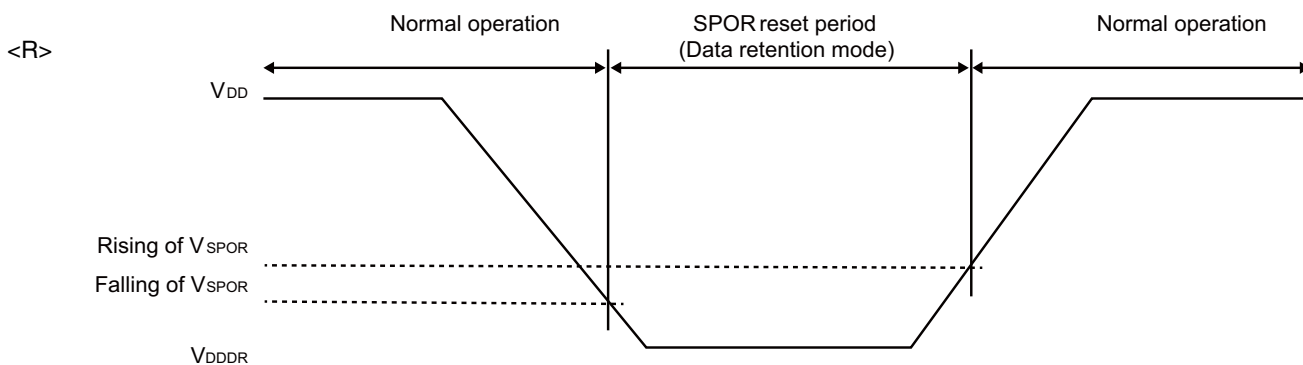
2.7 Flash Memory Programming Characteristics

(T_A = 0 to + 40°C, 4.5 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Code flash memory rewritable times [Notes 1, 2, 3]	C_{erwr}	Retained for 20 years.	T_A = +85°C	1000			Times

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

   2. When using flash memory programmer.

   3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.8 Dedicated Flash Memory Programmer Communication (UART)

(T_A = 0 to + 40°C, 4.5 V $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate				115,200		bps

Remark   The transfer rate during flash memory programming is fixed to 115,200 bps.

2.9 Timing of Entry to Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	SPOR reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	SPOR reset must be released before the external reset is released.	10			µs
Time to hold the TOOL0 pin at the low level after the external reset is released	t_{HD}	SPOR reset must be released before the external reset is released.	1			ms
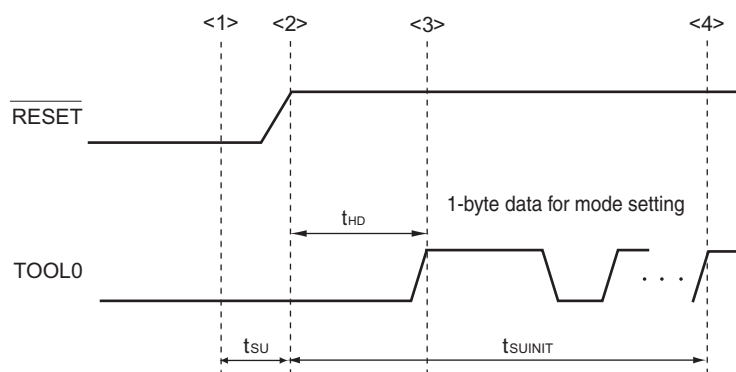
<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (SPOR reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of entry to the flash memory programming mode by UART reception is completed.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released

3. PACKAGE DRAWINGS

3.1 10-pin products

<R>   R5F10Y17ASP, R5F10Y16ASP, R5F10Y14ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05

detail of lead end
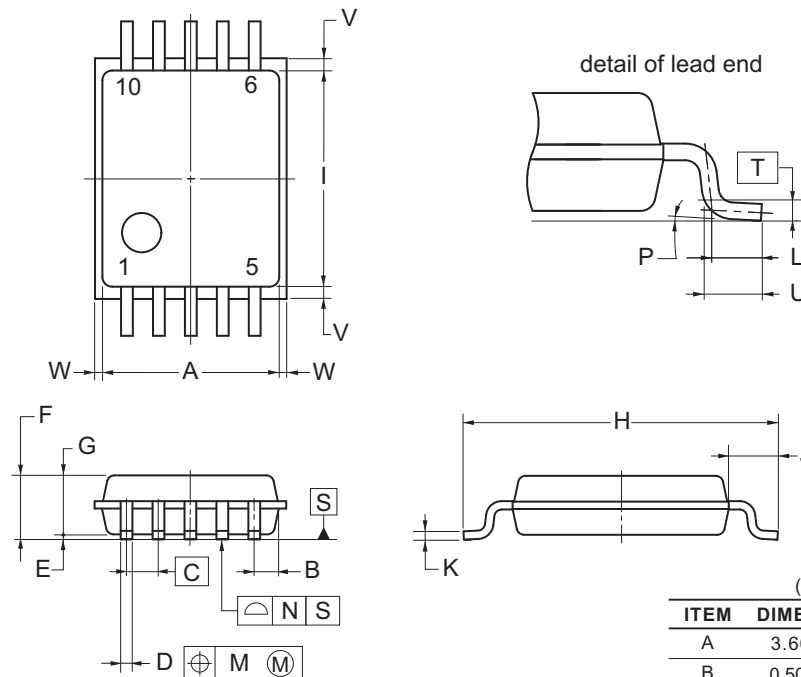
NOTE
Each lead centerline is located within 0.13 mm
of its true position (T.P.) at maximum material
condition.

(UNIT:mm)

ITEM	DIMENSIONS
A	3.60±0.10
B	0.50
C	0.65 (T.P.)
D	0.24±0.08
E	0.10±0.05
F	1.45 MAX.
G	1.20±0.10
H	6.40±0.20
I	4.40±0.10
J	1.00±0.20
K	$0.17{+0.08 \atop -0.07}$
L	0.50
M	0.13
N	0.10
P	$3°{+5° \atop -3°}$
T	0.25 (T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

3.2 16-pin products

R5F10Y47ASP, R5F10Y46ASP, R5F10Y44ASP

<R>

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-B	P16MA-65-FAB	0.08

detail of lead end

INDEX MARK

Terminal cross section

Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.85	5.00	5.15
D_1	5.05	5.20	5.35
E	4.20	4.40	4.60
A_2	——	1.50	——
A_1	0.075	0.125	0.175
A	——	——	1.725
b_p	0.17	0.24	0.32
b_1	——	0.22	——
c	0.14	0.17	0.20
c_1	——	0.15	——
θ	0°	——	8°
H_E	6.20	6.40	6.60
e	——	0.65	——
x	——	——	0.13
y	——	——	0.10
Z_D	——	0.225	——
L	0.35	0.50	0.65
L_1	——	1.00	——

RENESAS

Rev.	Date	Description	
		Page	**Summary**
1.00	Apr 15, 2013	-	First Edition issued
2.00	Jan 10, 2014	1, 2	Modification of descriptions in 1.1 Features
		3	Modification of description in 1.2 List of Part Numbers
		4	Modification of remark 2 in 1.3.1 10-pin products and 1.3.2 16-pin products
		8, 9	Addition of description of R5F10Y17ASP in 1.6 Outline of Functions
		11	Modification of description in 2.1 Absolute Maximum Ratings
		12	Modification of description in 2.2 Oscillator Characteristics
		13, 14	Modification of description, notes 1 to 4, and caution in 2.3.1 Pin characteristics
		16	Addition of description, notes 1 to 6, and remarks 1 and 2 in (2) Flash ROM: 4 KB of 10-pin products, and 16-pin products
		17	Addition of description, notes 1 to 6, and remarks 1 to 3 in (3) Peripheral Functions (Common to all products)
		18	Modification of description in 2.4 AC Characteristics
		19	Addition of figure of Minimum Instruction Execution Time during Main System Clock Operation
		19	Addition of figure of External System Clock Timing
		20	Modification of TI/TO Timing
		25	Addition of description in 2.5.2 Serial interface IICA
		26	Modification of description and notes 1 to 6 in 2.6.1 A/D converter characteristics
		27	Addition of description, notes 1 and 2 in 2.6.2 Comparator characteristics
		27	Addition of description and note in 2.6.3 Internal reference voltage characteristics
		28	Additioni of caution in 2.6.4 SPOR Circuit characteristics
		28	Addition of figure in 2.6.6 Data retention power supply voltage characteristics
		31	Addition of R5F10Y17ASP in 3.1 10-pin products
		32	Modification of package drawing in 3.2 16-pin products

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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STM8TL53G4U6 PIC16F877-04/P-B R5F10Y17ASP#30 CY8C3MFIDOCK-125 403708R MB95F354EPF-G-SNE2 MB95F564KPFT-G-

SNE2 MB95F564KWQN-G-SNE1 MB95F636KP-G-SH-SNE2 MB95F636KPMC-G-SNE2 MB95F694KPMC-G-SNE2 MB95F778JPMC1-

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