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April 1st, 2010
Renesas Electronics Corporation

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User's Manual

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R8C/2H Group, R8C/2J Group

Hardware Manual

RENESAS MCU

R8C FAMILY / R8C/2x SERIES

Renesas Electronics
www.renesas.com

Rev.1.00 2008.03

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/2H Group, R8C/2J Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Technology Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/2H Group, R8C/2J Group Datasheet	REJ03B0217
Hardware manual	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/2H Group, R8C/2J Group Hardware Manual	This hardware manual
Software manual	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Technology Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names

Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.

Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

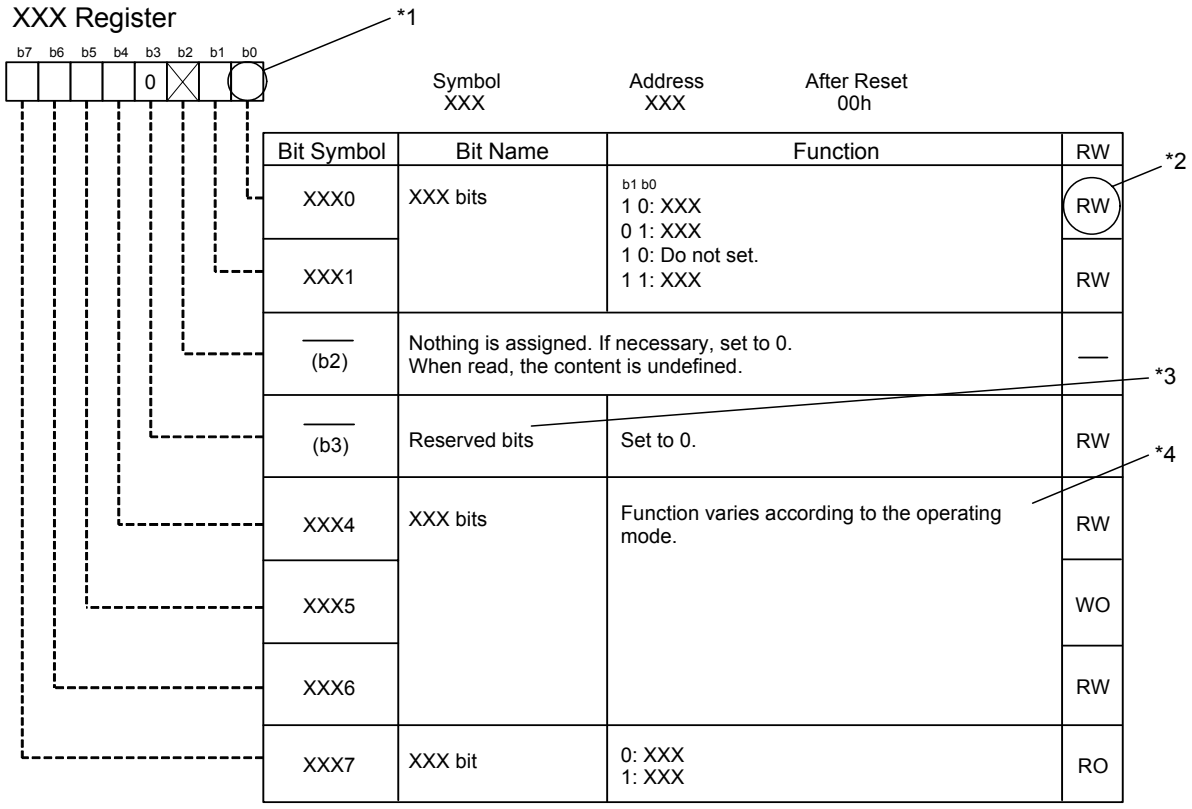
(2) Notation of Numbers

The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.

Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.



*1

Blank: Set to 0 or 1 according to the application.
0: Set to 0.
1: Set to 1.
X: Nothing is assigned.

*2

RW: Read and write.
RO: Read only.
WO: Write only.
–: Nothing is assigned.

*3

- Reserved bit
  Reserved bit. Set to specified value.

*4

- Nothing is assigned
  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value
  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.
  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input / Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver / Transmitter
VCO	Voltage Controlled Oscillator

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Address	Register	Symbol	Page
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	91
0005h	Processor Mode Register 1	PM1	91
0006h	System Clock Control Register 0	CM0	96, 97
0007h	System Clock Control Register 1	CM1	98, 99
0008h			
0009h			
000Ah	Protect Register	PRCR	117
000Bh			
000Ch	System Clock Select Register(2)	OCD	100
000Dh	Watchdog Timer Reset Register	WDTR	149
000Eh	Watchdog Timer Start Register	WDTS	149
000Fh	Watchdog Timer Control Register	WDC	150
0010h	Address Match Interrupt Register 0	RMAD0	137
0011h			
0012h			
0013h	Address Match Interrupt Enable Register	AIER	137
0014h	Address Match Interrupt Register 1	RMAD1	137
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	151
001Dh			
001Eh			
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	101
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	101
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	101
0023h			
0024h			
0025h			
0026h			
0027h			
0028h	Clock Prescaler Reset Flag(2)	CPSRF	102
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	102
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	102
002Ch			
002Dh			
002Eh	BGR Trimming Auxiliary Register A	BGRTRMA	55
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0034h			
0035h			
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0037h	Voltage Monitor 2 Circuit Control Register	VW2C	45, 58
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	43
0039h			
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003Ch	Comparator Mode Register	ALCMR	59
003Dh	Voltage Monitor Circuit Edge Select Register	VCAC	46, 60
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003Fh	BGR Trimming Register	BGRTRM	61

Address	Register	Symbol	Page
0040h			
0041h	Comparator 1 Interrupt Control Register	VCMP1IC	123
0042h	Comparator 2 Interrupt Control Register	VCMP2IC	123
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register(2)	TREIC	123
004Bh	UART2 Transmit Interrupt Control Register(2)	S2TIC	123
004Ch	UART2 Receive Interrupt Control Register(2)	S2RIC	123
004Dh	Key Input Interrupt Control Register	KUPIC	123
004Eh			
004Fh			
0050h	Compare 1 Interrupt Control Register	CMP1IC	123
0051h	UART0 Transmit Interrupt Control Register	S0TIC	123
0052h	UART0 Receive Interrupt Control Register	S0RIC	123
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	123
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	123
0059h	INT1 Interrupt Control Register	INT1IC	124
005Ah			
005Bh	Timer RF Interrupt Control Register	TRFIC	123
005Ch	Compare 0 Interrupt Control Register	CMP0IC	123
005Dh	INT0 Interrupt Control Register	INT0IC	124
005Eh			
005Fh	Capture Interrupt Control Register	CAPIC	123
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
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0073h			
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0077h			
0078h			
0079h			
007Ah			
007Bh			
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007Dh			
007Eh			
007Fh			

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. This register is not implemented in the R8C/2J Group.

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0080h			
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0097h			
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009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
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00A8h			
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00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
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00BBh			
00BCh			
00BDh			
00BEh			
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Address	Register	Symbol	Page
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00F9h	External Input Enable Register	INTEN	131
00FAh	INT Input Filter Select Register	INTF	132
00FBh	Key Input Enable Register	KIEN	135
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00FDh	Pull-Up Control Register 1	PUR1	82
00FEh			
00FFh			

NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

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0100h	Timer RA Control Register	TRACR	159
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0103h	Timer RA Prescaler Register	TRAPRE	160
0104h	Timer RA Register	TRA	160
0105h			
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0107h	LIN Status Register	LINST	245
0108h	Timer RB Control Register	TRBCR	175
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012Ch			
012Dh			
012Eh			
012Fh			

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0130h			
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0142h			
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0144h			
0145h			
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0147h			
0148h			
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0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			

Address	Register	Symbol	Page
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	266
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	265
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	262
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. This register is not implemented in the R8C/2J Group.

Address	Register	Symbol	Page
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			

Address	Register	Symbol	Page
0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			
0240h			
0241h			
0242h			
0243h			
0244h			
0245h			
0246h			
0247h			
0248h			
0249h			
024Ah			
024Bh			
024Ch			
024Dh			
024Eh			
024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			

NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
0260h			
0261h			
0262h			
0263h			
0264h			
0265h			
0266h			
0267h			
0268h			
0269h			
026Ah			
026Bh			
026Ch			
026Dh			
026Eh			
026Fh			
0270h			
0271h			
0272h			
0273h			
0274h			
0275h			
0276h			
0277h			
0278h			
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h	Timer RF Register	TRF	215
0291h			
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h			
0299h	Timer RF Control Register 2(2)	TRFCR2	216
029Ah	Timer RF Control Register 0	TRFCR0	216
029Bh	Timer RF Control Register 1	TRFCR1	217
029Ch	Capture and Compare 0 Register	TRFM0	215
029Dh			
029Eh	Compare 1 Register	TRFM1	215
029Fh			

Address	Register	Symbol	Page
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			
02C0h			
02C1h			
02C2h			
02C3h			
02C4h			
02C5h			
02C6h			
02C7h			
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. This register is not implemented in the R8C/2J Group.

Address	Register	Symbol	Page
02E0h			
02E1h			
02E2h			
02E3h			
02E4h			
02E5h			
02E6h			
02E7h			
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh	Pin Select Register 4	PINSR4	46, 61, 80
02FCh			
02FDh			
02FEh			
02FFh	Timer RF Output Control Register	TRFOUT	217

FFFFh	Option Function Select Register	OFS	33, 144, 152, 260

NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

1. Overview

1.1 Features

The R8C/2H Group and R8C/2J Group of single-chip MCUs incorporate the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

1.1.1 Applications

Electric power meters, electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Table 1.1 outlines the Specifications for R8C/2H Group and Table 1.2 outlines the Specifications for R8C/2J Group.

Table 1.1 Specifications for R8C/2H Group

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 125 ns (System clock = 8 MHz, VCC = 2.7 to 5.5 V) 250 ns (System clock = 4 MHz, VCC = 2.2 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.3 Product List for R8C/2H Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3
Comparator		• 2 circuits (shared with voltage monitor 1 and voltage monitor 2) • External reference voltage input is available
I/O Ports		• Output-only: 1 • CMOS I/O ports: 15, selectable pull-up resistor
Clock	Clock generation circuits	• 2 circuits: On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), XCIN clock oscillation circuit (32 kHz) • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• External: 3 sources, Internal: 17 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits × 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode
	Timer RF	16 bits × 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode
Serial Interface	UART0, UART2	Clock synchronous serial I/O/UART × 2
LIN Module		Hardware LIN: 1 (timer RA, UART0)
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		System clock = 8 MHz (VCC = 2.7 to 5.5 V) System clock = 4 MHz (VCC = 2.2 to 5.5 V)
Current consumption		5 mA (VCC = 5 V, system clock = 8 MHz) 23 μA (VCC = 3 V, wait mode (low-speed on-chip oscillator on)) 0.7 μA (VCC = 3 V, stop mode, BGR trimming circuit disabled)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version)(1)
Package		20-pin LSSOP Package code: PLSP0020JB-A (previous code: 20P2F-A)

NOTE:
1. Specify the D version if D version functions are to be used.

Table 1.2 Specifications for R8C/2J Group

Item	Function	Specification
CPU	Central processing unit	R8C/Tiny series core • Number of fundamental instructions: 89 • Minimum instruction execution time: 125 ns (System clock = 8 MHz, VCC = 2.7 to 5.5 V) 250 ns (System clock = 4 MHz, VCC = 2.2 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM	Refer to **Table 1.4 Product List for R8C/2J Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3
Comparator		• 2 circuits (shared with voltage monitor 1 and voltage monitor 2) • External reference voltage input is available
I/O Ports		CMOS I/O ports: 12, selectable pull-up resistor
Clock	Clock generation circuits	• 1 circuits: On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• External: 3 sources, Internal: 14 sources, Software: 4 sources • Priority levels: 7 levels
Watchdog Timer		15 bits × 1 (with prescaler), reset start selectable
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RE	Not implemented
	Timer RF	16 bits × 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode
Serial Interface	UART0	Clock synchronous serial I/O/UART × 1
LIN Module		Hardware LIN: 1 (timer RA, UART0)
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		System clock = 8 MHz (VCC = 2.7 to 5.5 V) System clock = 4 MHz (VCC = 2.2 to 5.5 V)
Current consumption		5 mA (VCC = 5 V, system clock = 8 MHz) 23 μA (VCC = 3 V, wait mode (low-speed on-chip oscillator on)) 0.7 μA (VCC = 3 V, stop mode, BGR trimming circuit disabled)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version)(1)
Package		20-pin LSSOP Package code: PLSP0020JB-A (previous code: 20P2F-A)

NOTE:
1. Specify the D version if D version functions are to be used.

1.2 Product List

Table 1.3 lists Product List for R8C/2H Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2H Group. Table 1.4 lists Product List for R8C/2J Group, Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2J Group.

Table 1.3 Product List for R8C/2H Group **Current of Mar. 2008**

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212H1SNSP	4 Kbytes	256 bytes	PLSP0020JB-A	N version
R5F212H2SNSP	8 Kbytes	384 bytes	PLSP0020JB-A	
R5F212H1SDSP	4 Kbytes	256 bytes	PLSP0020JB-A	D version
R5F212H2SDSP	8 Kbytes	384 bytes	PLSP0020JB-A	

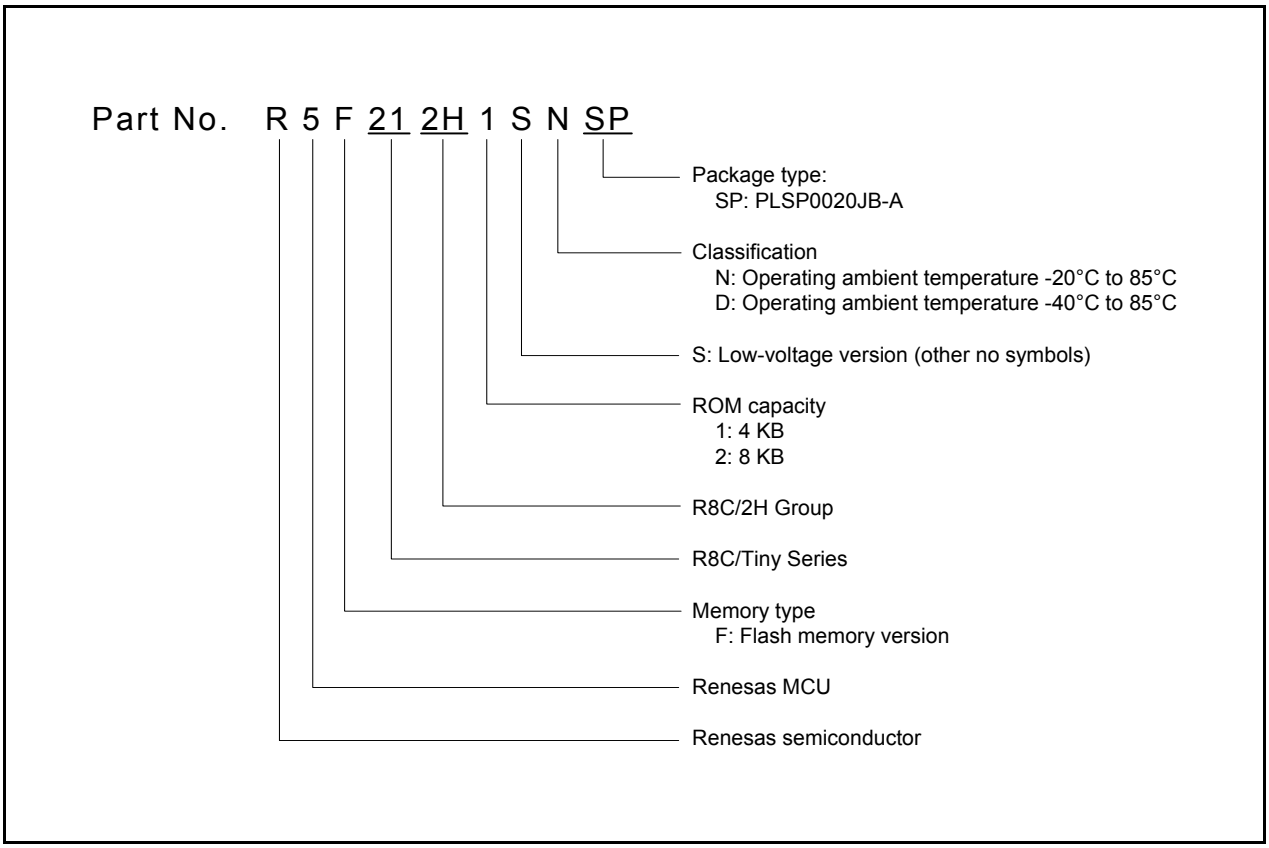


Figure 1.1 Part Number, Memory Size, and Package of R8C/2H Group

Table 1.4 Product List for R8C/2J Group **Current of Mar. 2008**

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212J0SNSP	2 Kbytes	256 bytes	PLSP0020JB-A	N version
R5F212J1SNSP	4 Kbytes	384 bytes	PLSP0020JB-A	
R5F212J0SDSP	2 Kbytes	256 bytes	PLSP0020JB-A	D version
R5F212J1SDSP	4 Kbytes	384 bytes	PLSP0020JB-A	

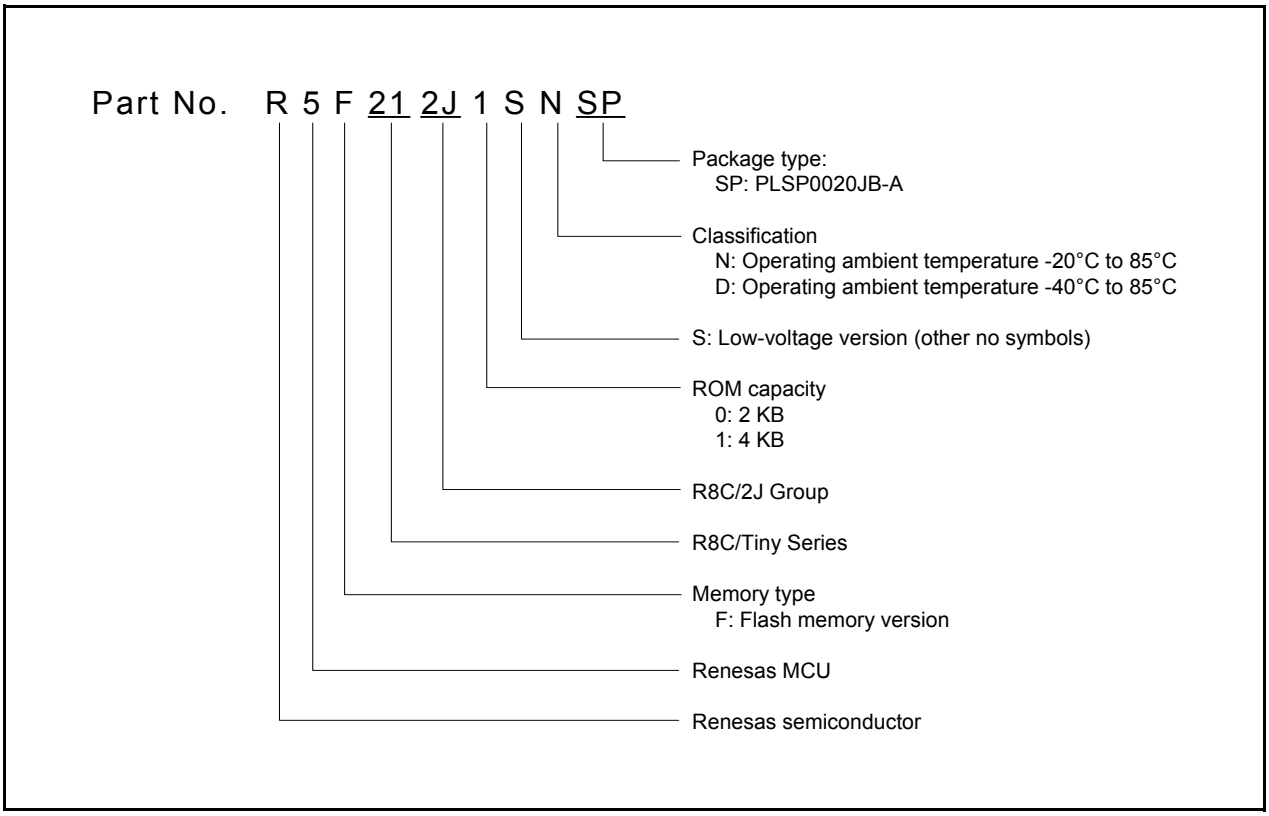


Figure 1.2 Part Number, Memory Size, and Package of R8C/2J Group

1.3 Block Diagram

Figure 1.3 shows a Block Diagram of R8C/2H Group and Figure 1.4 shows a Block Diagram of R8C/2J Group.

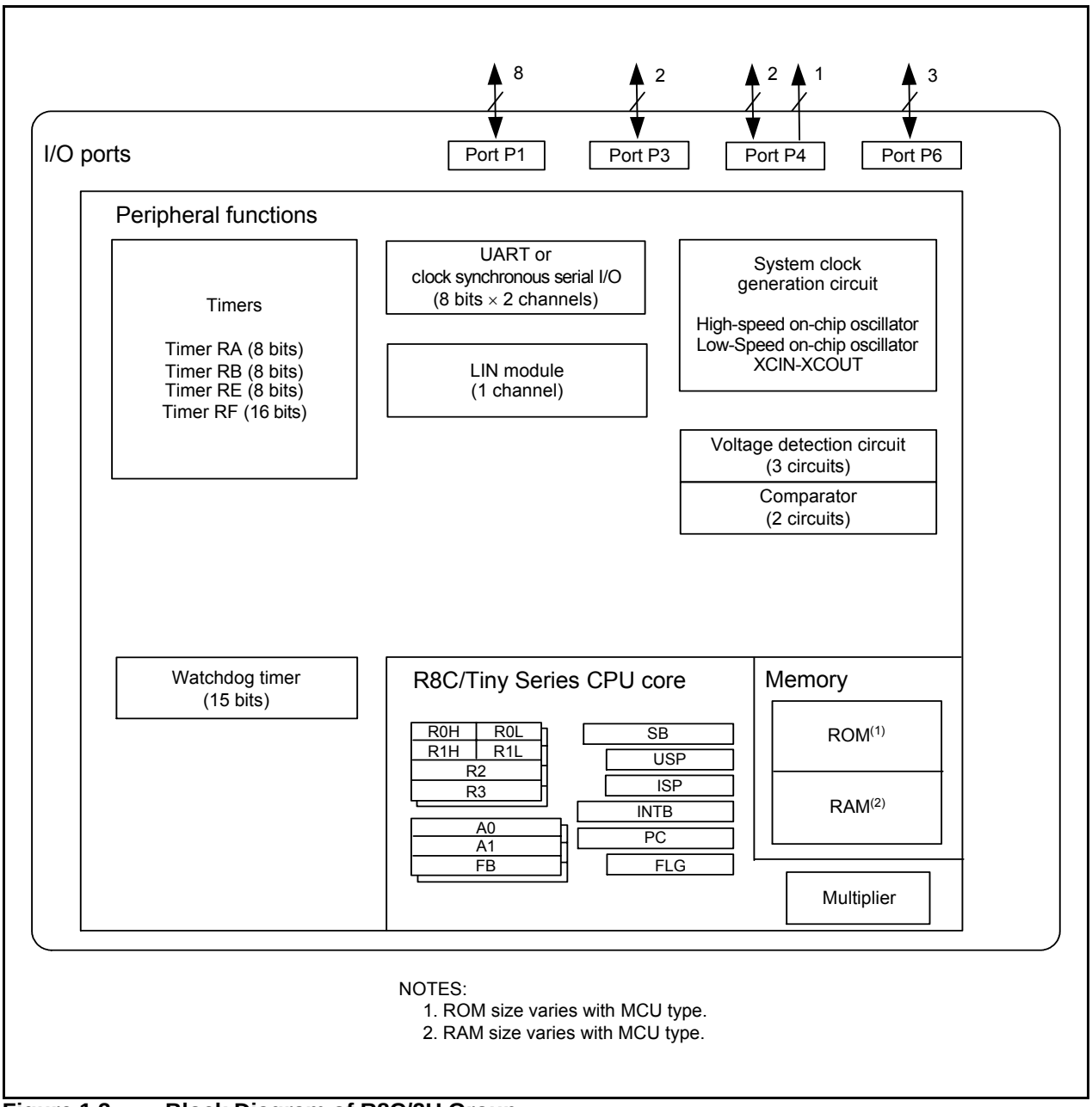


Figure 1.3 Block Diagram of R8C/2H Group

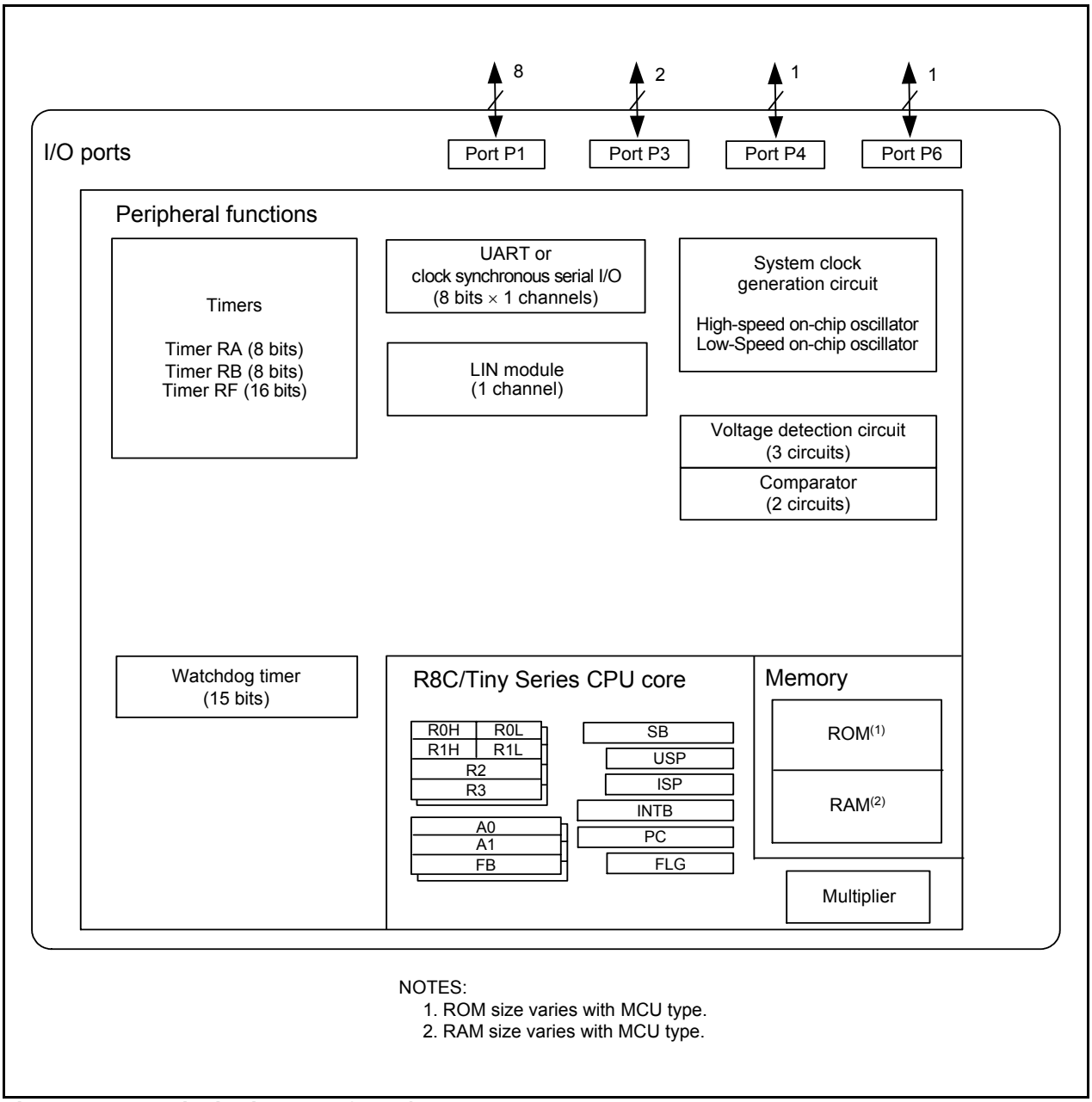
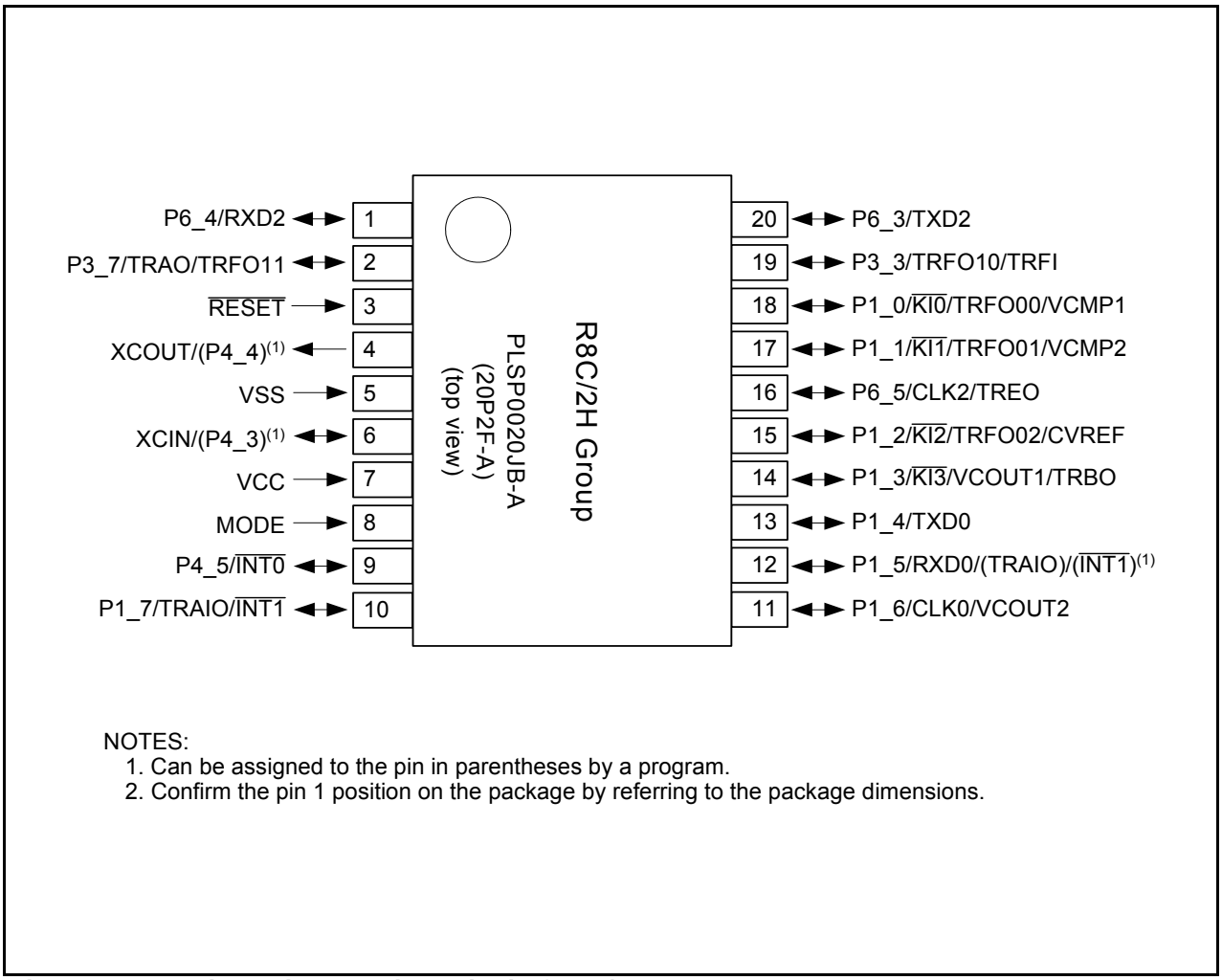


Figure 1.4 Block Diagram of R8C/2J Group

1.4 Pin Assignment

Figure 1.5 shows Pin Assignment (Top View) of R8C/2H Group. Table 1.5 outlines the Pin Name Information by Pin Number of R8C/2H Group.
Figure 1.6 shows Pin Assignment (Top View) of R8C/2J Group. Table 1.6 outlines the Pin Name Information by Pin Number of R8C/2J Group.



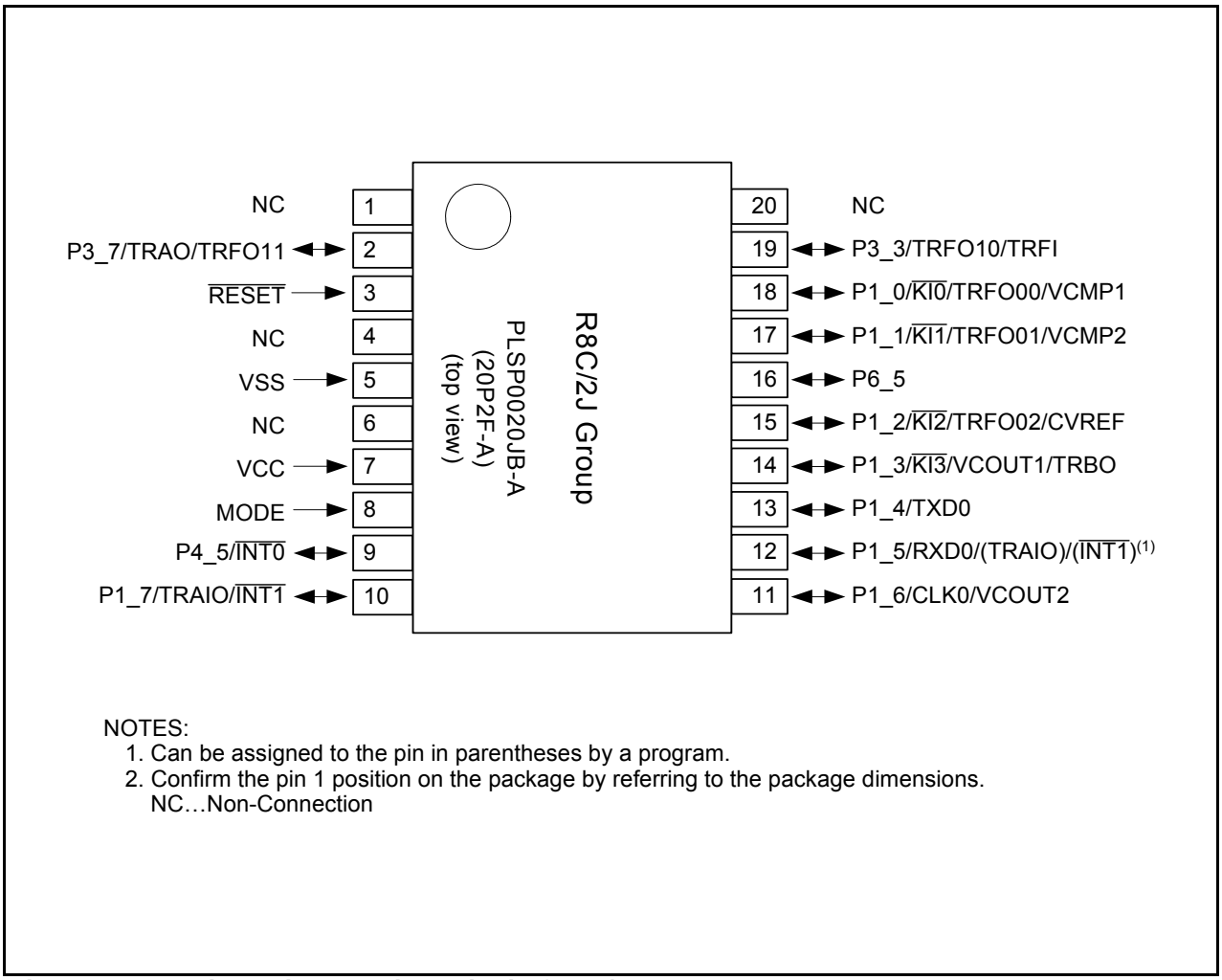
NOTES:
1. Can be assigned to the pin in parentheses by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.5 Pin Assignment (Top View) of R8C/2H Group

Table 1.5 Pin Name Information by Pin Number of R8C/2H Group

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
			Interrupt	Timer	Serial Interface	Comparator
1		P6_4			RXD2	
2		P3_7		TRAO/TRFO11		
3	$\overline{\text{RESET}}$					
4	XCOUT	(P4_4)				
5	VSS					
6	XCIN	(P4_3)				
7	VCC					
8	MODE					
9		P4_5	$\overline{\text{INT0}}$			
10		P1_7	$\overline{\text{INT1}}$	TRAIO		
11		P1_6			CLK0	VCOUT2
12		P1_5	($\overline{\text{INT1}}$)(1)	(TRAIO)(1)	RXD0	
13		P1_4			TXD0	
14		P1_3	$\overline{\text{KI3}}$	TRBO		VCOUT1
15		P1_2	$\overline{\text{KI2}}$	TRFO02		CVREF
16		P6_5		TREO	CLK2	
17		P1_1	$\overline{\text{KI1}}$	TRFO01		VCMP2
18		P1_0	$\overline{\text{KI0}}$	TRFO00		VCMP1
19		P3_3		TRFO10/TRFI		
20		P6_3			TXD2	

NOTE:
1. Can be assigned to the pin in parentheses by a program.



NOTES:
1. Can be assigned to the pin in parentheses by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.
NC…Non-Connection

Figure 1.6 Pin Assignment (Top View) of R8C/2J Group

Table 1.6 Pin Name Information by Pin Number of R8C/2J Group

Pin Number	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
			Interrupt	Timer	Serial Interface	Comparator
1	NC(2)					
2		P3_7		TRAO/TRFO11		
3	$\overline{\text{RESET}}$					
4	NC(2)					
5	VSS					
6	NC(2)					
7	VCC					
8	MODE					
9		P4_5	$\overline{\text{INT0}}$			
10		P1_7	$\overline{\text{INT1}}$	TRAIO		
11		P1_6			CLK0	VCOUT2
12		P1_5	($\overline{\text{INT1}}$)(1)	(TRAIO)(1)	RXD0	
13		P1_4			TXD0	
14		P1_3	$\overline{\text{KI3}}$	TRBO		VCOUT1
15		P1_2	$\overline{\text{KI2}}$	TRFO02		CVREF
16		P6_5				
17		P1_1	$\overline{\text{KI1}}$	TRFO01		VCMP2
18		P1_0	$\overline{\text{KI0}}$	TRFO00		VCMP1
19		P3_3		TRFO10/TRFI		
20	NC(2)					

NOTES:
1. Can be assigned to the pin in parentheses by a program.
2. NC(Non-Connection)

1.5 Pin Functions

Table 1.7 lists Pin Functions of R8C/2H Group and Table 1.8 lists Pin Functions of R8C/2J Group.

Table 1.7 Pin Functions of R8C/2H Group

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins.(1) To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$	I	$\overline{\text{INT}}$ interrupt input pins
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RE	TREO	O	Divided clock output pin
Timer RF	TRFI	I	Timer RF input pin
	TRFO00 to TRFO02, TRFO10 to TRFO11	O	Timer RF output pins
Serial interface	CLK0, CLK2	I/O	Clock I/O pin
	RXD0, RXD2	I	Serial data input pin
	TXD0, TXD2	O	Serial data output pin
Comparator	VCMP1, VCMP2	I	Analog input pins to comparator
	CVREF	I	Reference voltage input pin to comparator
	VCOUT1, VCOUT2	O	Comparator output pins
I/O port	P1_0 to P1_7, P3_3, P3_7, P4_3, P4_5, P6_3 to P6_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Output port	P4_4	O	Output-only port

I: Input O: Output I/O: Input and output

NOTE:

1. Refer to the oscillator manufacturer for oscillation characteristics.

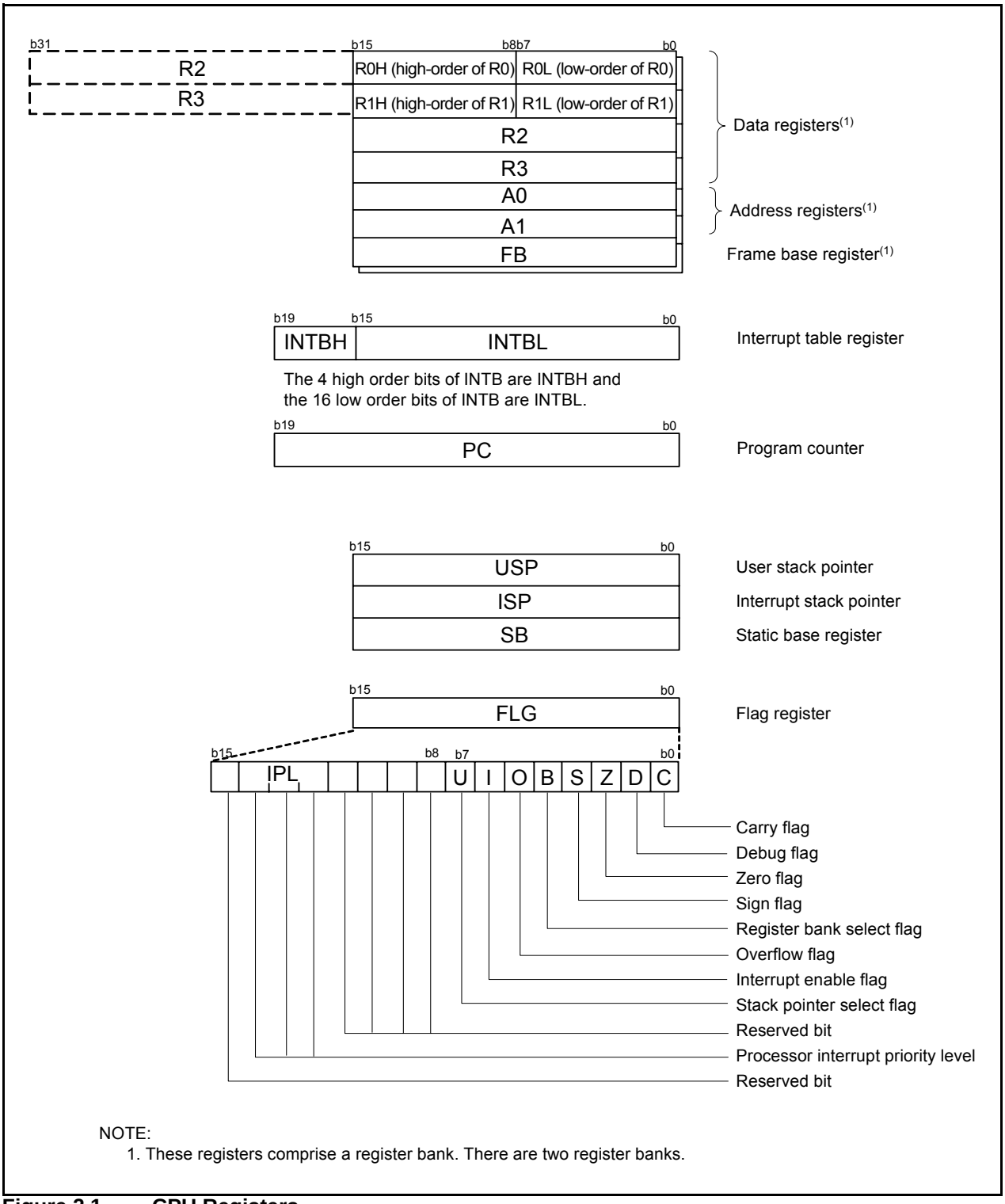
Table 1.8 Pin Functions of R8C/2J Group

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$	I	$\overline{\text{INT}}$ interrupt input pins
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RF	TRFI	I	Timer RF input pin
	TRFO00 to TRFO02, TRFO10 to TRFO11	O	Timer RF output pins
Serial interface	CLK0	I/O	Clock I/O pin
	RXD0	I	Serial data input pin
	TXD0	O	Serial data output pin
Comparator	VCMP1, VCMP2	I	Analog input pins to comparator
	CVREF	I	Reference voltage input pin to comparator
	VCOUT1, VCOUT2	O	Comparator output pins
I/O port	P1_0 to P1_7, P3_3, P3_7, P4_5, P6_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

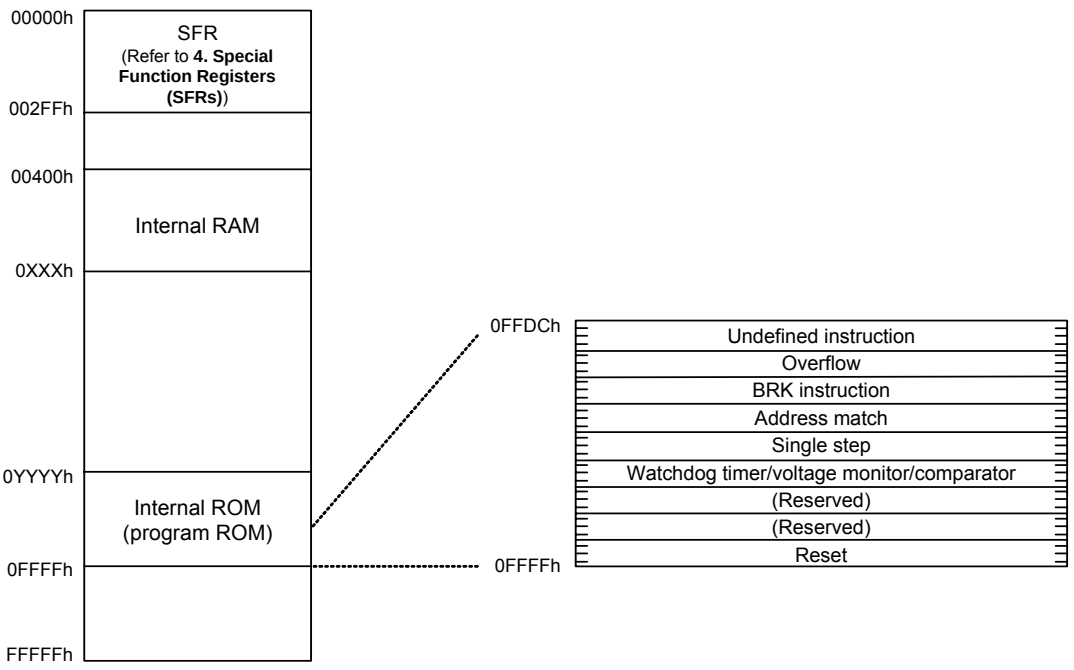
IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

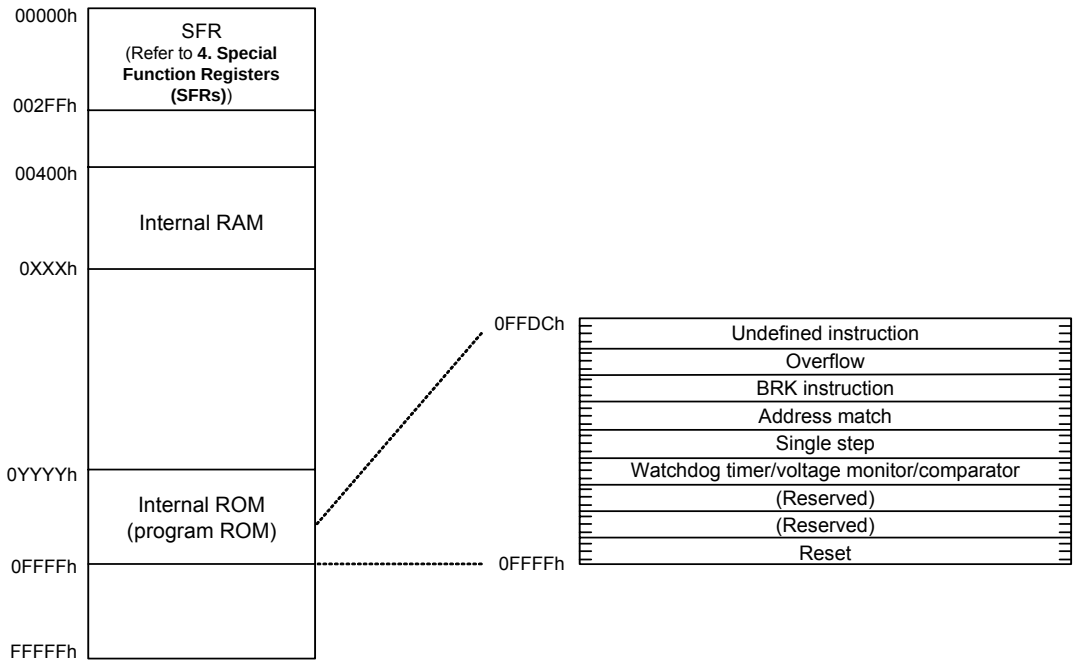
Figure 3.1 is a Memory Map of R8C/2H Group and Figure 3.2 is a Memory Map of R8C/2J Group. The R8C/2H group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 4-Kbyte internal ROM area is allocated addresses 0F000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 256-bytes internal RAM area is allocated addresses 00400h to 004FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F212H1SNSP, R5F212H1SDSP	4 Kbytes	0F000h	256 bytes	004FFh
R5F212H2SNSP, R5F212H2SDSP	8 Kbytes	0E000h	384 bytes	0057Fh

Figure 3.1 Memory Map of R8C/2H Group



NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F212J0SNSP, R5F212J0SDSP	2 Kbytes	0F800h	256 bytes	004FFh
R5F212J1SNSP, R5F212J1SDSP	4 Kbytes	0F000h	384 bytes	0057Fh

Figure 3.2 Memory Map of R8C/2J Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01011000b
0007h	System Clock Control Register 1	CM1	00h
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	System Clock Select Register[3]	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b[2]
001Dh			
001Eh			
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When Shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
0024h			
0025h			
0026h			
0027h			
0028h	Clock Prescaler Reset Flag[3]	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh	BGR Trimming Auxiliary Register A	BGRTRMA	When Shipping
002Fh	BGR Trimming Auxiliary Register B	BGRTRMB	When Shipping

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The CSPROINI bit in the OFS register is set to 0.
3. This register is not implemented in the R8C/2J Group.

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1(2)	VCA1	00001000b
0032h	Voltage Detection Register 2(2)	VCA2	00h(3) 00100000b(4)
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register(5)	VW1C	00001010b
0037h	Voltage Monitor 2 Circuit Control Register(5)	VW2C	00000010b
0038h	Voltage Monitor 0 Circuit Control Register(2)	VW0C	1000X010b(3) 1100X011b(4)
0039h			
003Ah			
003Bh	Voltage Detection Circuit External Input Control Register	VCAB	00h
003Ch	Comparator Mode Register	ALCMR	00h
003Dh	Voltage Monitor Circuit Edge Select Register	VCAC	00h
003Eh	BGR Control Register	BGRCR	00h
003Fh	BGR Trimming Register	BGRTRM	When Shipping
0040h			
0041h	Comparator 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0042h	Comparator 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register(6)	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register(6)	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register(6)	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh			
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah			
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh	Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
6. This register is not implemented in the R8C/2J Group.

Table 4.3 SFR Information (3)(1)

Address	Register	Symbol	After reset
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			
0080h			
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.4 SFR Information (4)(1)

Address	Register	Symbol	After reset
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh			
00BEh			
00BFh			
00C0h			
00C1h			
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h			
00E1h	Port P1 Register	P1	00h
00E2h			
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	00h
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	00h
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	00h
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)[1]

Address	Register	Symbol	After reset
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h	Pin Select Register 2	PINSR2	00h
00F7h			
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh			
00FFh			
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register[2]	TRESEC	XXh
0119h	Timer RE Minute Data Register / Compare Data Register[2]	TREMIN	XXh
011Ah	Timer RE Hour Data Register[2]	TREHR	X0XXXXXXb
011Bh	Timer RE Day of Week Data Register[2]	TREWK	X0000XXXb
011Ch	Timer RE Control Register 1[2]	TRECR1	XXX0X0X0b
011Dh	Timer RE Control Register 2[2]	TRECR2	00XXXXXXb
011Eh	Timer RE Count Source Select Register[2]	TRECSR	00001000b
011Fh	Timer RE Real-Time Clock Precision Adjust Register[2]	TREOPR	00h
0120h			
0121h			
0122h			
0123h			
0124h			
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			
012Ch			
012Dh			
012Eh			
012Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions
2. This register is not implemented in the R8C/2J Group.

Table 4.6 SFR Information (6)[1]

Address	Register	Symbol	After reset
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h	UART2 Transmit/Receive Mode Register[2]	U2MR	00h
0161h	UART2 Bit Rate Register[2]	U2BRG	XXh
0162h	UART2 Transmit Buffer Register[2]	U2TB	XXh
0163h			XXh
0164h	UART2 Transmit/Receive Control Register 0[2]	U2C0	00001000b
0165h	UART2 Transmit/Receive Control Register 1[2]	U2C1	00000010b
0166h	UART2 Receive Buffer Register[2]	U2RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. This register is not implemented in the R8C/2J Group.

Table 4.7 SFR Information (7)[1]

Address	Register	Symbol	After reset
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.8 SFR Information (8)(1)

Address	Register	Symbol	After reset
01B0h			
01B1h			
01B2h			
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h			
01C1h			
01C2h			
01C3h			
01C4h			
01C5h			
01C6h			
01C7h			
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)(1)

Address	Register	Symbol	After reset
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
0220h			
0221h			
0222h			
0223h			
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.10 SFR Information (10)[1]

Address	Register	Symbol	After reset
0230h			
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			
0240h			
0241h			
0242h			
0243h			
0244h			
0245h			
0246h			
0247h			
0248h			
0249h			
024Ah			
024Bh			
024Ch			
024Dh			
024Eh			
024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h			
0261h			
0262h			
0263h			
0264h			
0265h			
0266h			
0267h			
0268h			
0269h			
026Ah			
026Bh			
026Ch			
026Dh			
026Eh			
026Fh			

X: Undefined
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)[1]

Address	Register	Symbol	After reset
0270h			
0271h			
0272h			
0273h			
0274h			
0275h			
0276h			
0277h			
0278h			
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h	Timer RF Register	TRF	00h
0291h			00h
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h			
0299h	Timer RF Control Register 2[4]	TRFCR2	00h
029Ah	Timer RF Control Register 0	TRFCR0	00h
029Bh	Timer RF Control Register 1	TRFCR1	00h
029Ch	Capture and Compare 0 Register	TRFM0	0000h[2]
029Dh			FFFFh[3]
029Eh	Compare 1 Register	TRFM1	FFh
029Fh			FFh
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			

X: Undefined

NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. After input capture mode.
3. After output compare mode.
4. This register is not implemented in the R8C/2J Group.

Table 4.12 SFR Information (12)(1)

Address	Register	Symbol	After reset
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			
02C0h			
02C1h			
02C2h			
02C3h			
02C4h			
02C5h			
02C6h			
02C7h			
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh	Pin Select Register 4	PINSR4	00h
02FCh			
02FDh			
02FEh			
02FFh	Timer RF Output Control Register	TRFOUT	00h
FFFFh	Option Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Resets

The following resets are implemented: hardware reset, power-on reset, voltage monitor 0 reset, voltage monitor 1 reset, voltage monitor 2 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources. Figure 5.1 shows the Block Diagram of Reset Circuit.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	Input voltage of $\overline{\text{RESET}}$ pin is held “L”
Power-on reset	VCC rises
Voltage monitor 0 reset	VCC falls (monitor voltage: Vdet0)
Voltage monitor 1 reset	VCC falls (monitor voltage: Vdet1)
Voltage monitor 2 reset	VCC falls (monitor voltage: Vdet2)
Watchdog timer reset	Underflow of watchdog timer
Software reset	Write 1 to PM03 bit in PM0 register

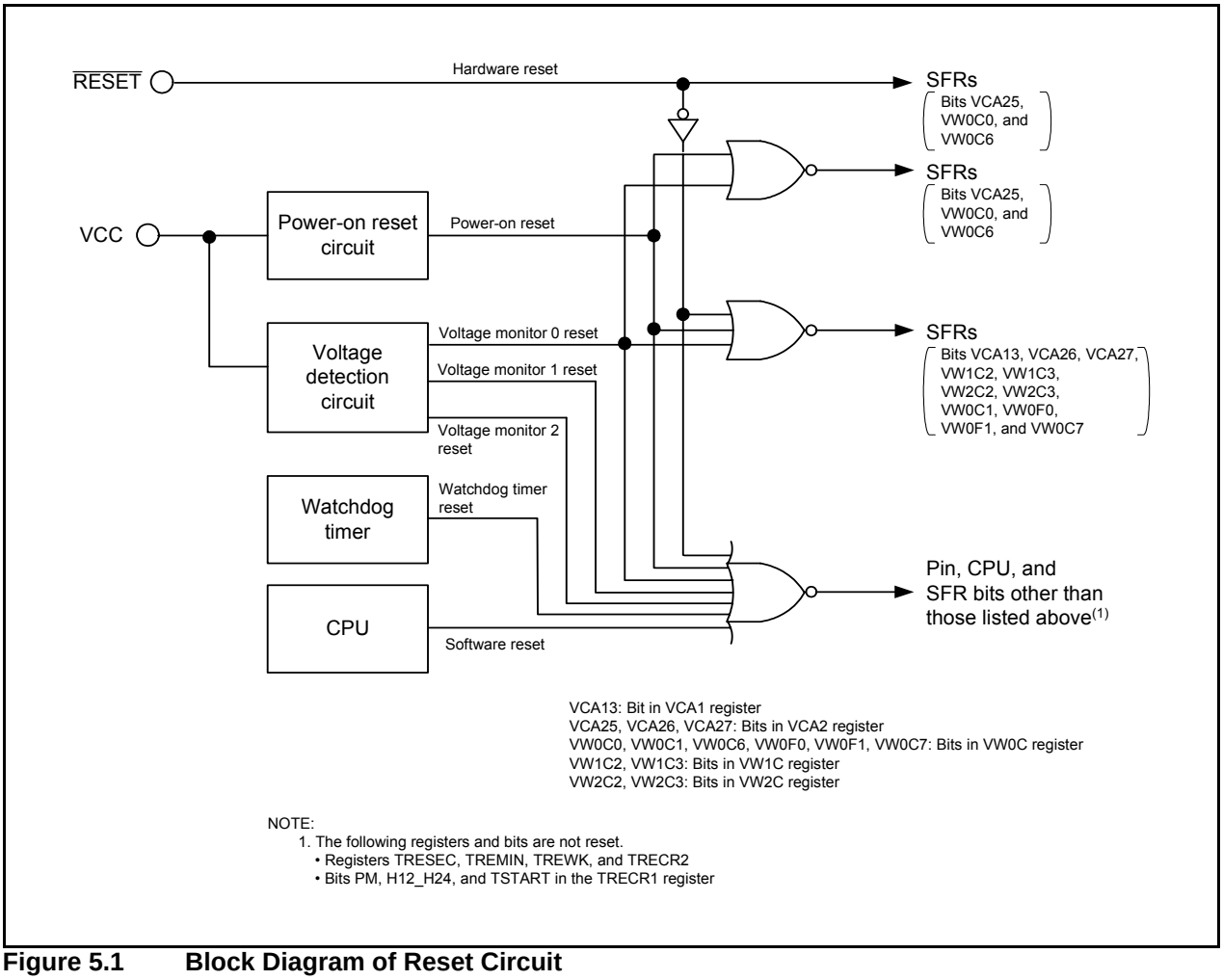


Figure 5.1 Block Diagram of Reset Circuit

Table 5.2 shows the Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”, Figure 5.2 shows the CPU Register Status after Reset, Figure 5.3 shows the Reset Sequence, and Figure 5.4 shows the OFS Register.

Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”

Pin Name	Pin Functions
P1, P3_3, P3_7	Input port
P4_3, P4_5 (1)	Input port
P4_4 (1)	Output port
P6_3 to P6_5 (1)	Input port

NOTE:
1. Ports P4_3, P4_4, P6_3, and P6_4 are not available in the R8C/2J Group.

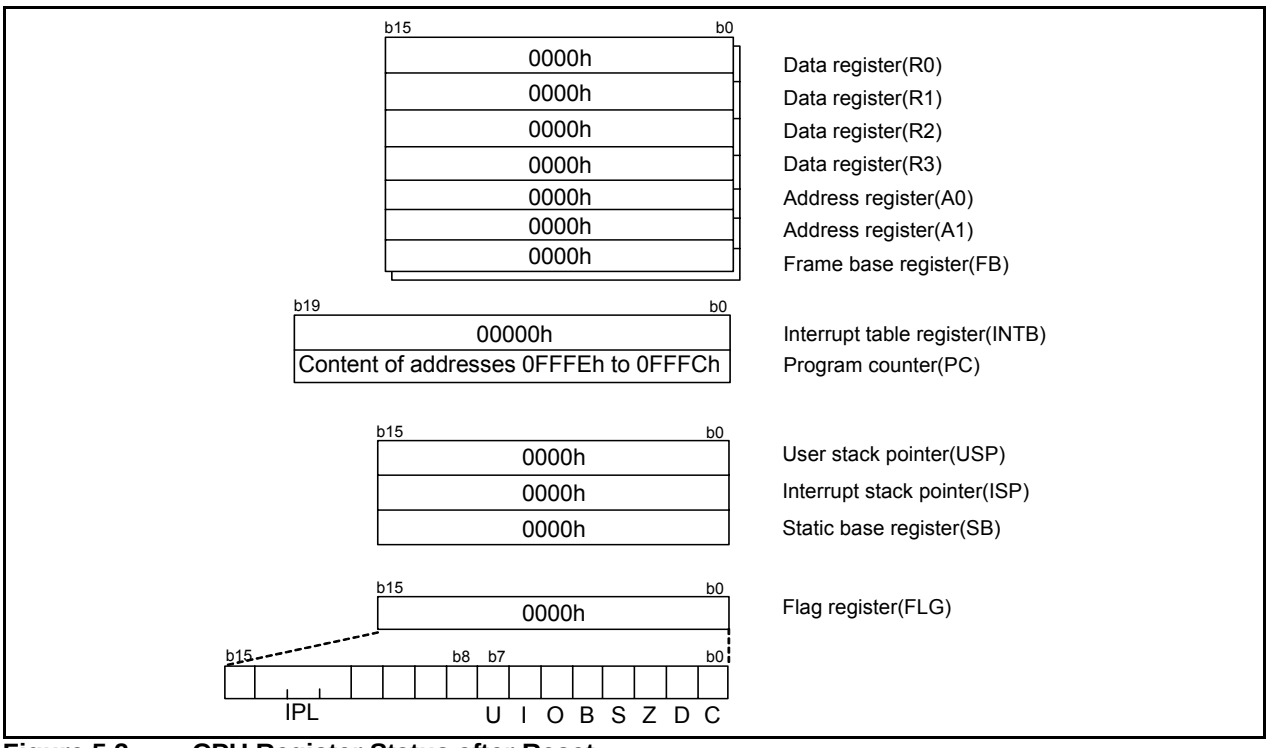
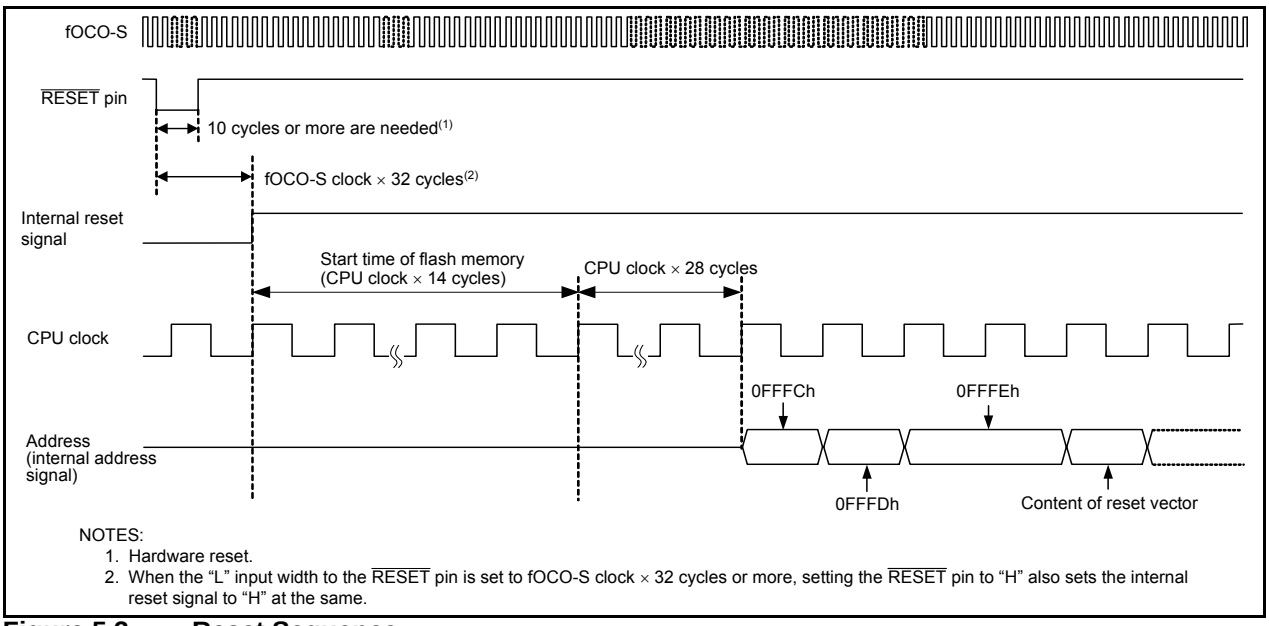


Figure 5.2 CPU Register Status after Reset



NOTES:
1. Hardware reset.
2. When the “L” input width to the $\overline{\text{RESET}}$ pin is set to fOCO-S clock × 32 cycles or more, setting the $\overline{\text{RESET}}$ pin to “H” also sets the internal reset signal to “H” at the same.

Figure 5.3 Reset Sequence

Option Function Select Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
	1		1			1	

Symbol	Address	When Shipping
OFS	0FFFFh	FFh(3)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b4)	Reserved bit	Set to 1.	RW
LVD0ON	Voltage detection 0 circuit start bit(2)	0 : Voltage monitor 0 reset enabled after hardware reset 1 : Voltage monitor 0 reset disabled after hardware reset	RW
— (b6)	Reserved bit	Set to 1.	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. Setting the LVD0ON bit is only valid after a hardware reset. To use the power-on reset, set the LVD0ON bit to 0 (voltage monitor 0 reset enabled after hardware reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Figure 5.4 OFS Register

5.1 Hardware Reset

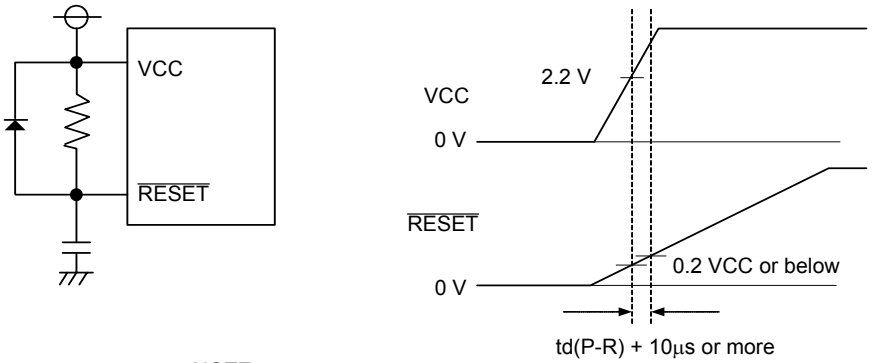
A reset is applied using the $\overline{\text{RESET}}$ pin. When an “L” signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating conditions, pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”**). When the input level applied to the $\overline{\text{RESET}}$ pin changes from “L” to “H”, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the state of the SFRs after reset.
The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled “L” while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.
Figure 5.5 shows an Example of Hardware Reset Circuit and Operation and Figure 5.6 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.1.1 When Power Supply is Stable

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 μs.
(3) Apply “H” to the $\overline{\text{RESET}}$ pin.

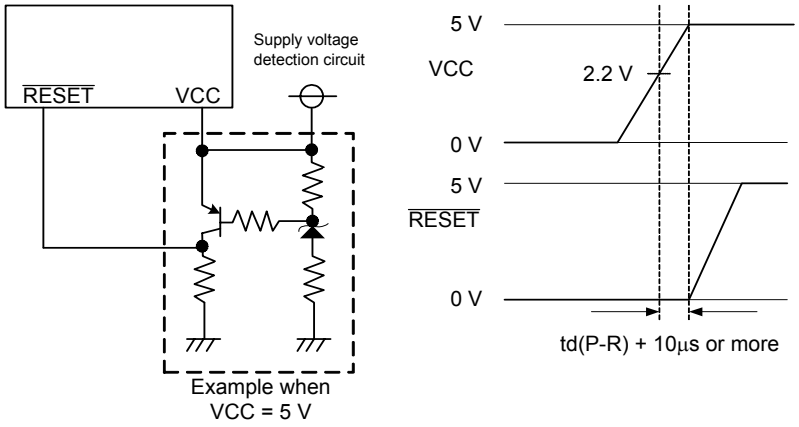
5.1.2 Power On

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **22. Electrical Characteristics**).
(4) Wait for 10 μs.
(5) Apply “H” to the $\overline{\text{RESET}}$ pin.



NOTE:
1. Refer to **22. Electrical Characteristics**.

Figure 5.5 Example of Hardware Reset Circuit and Operation

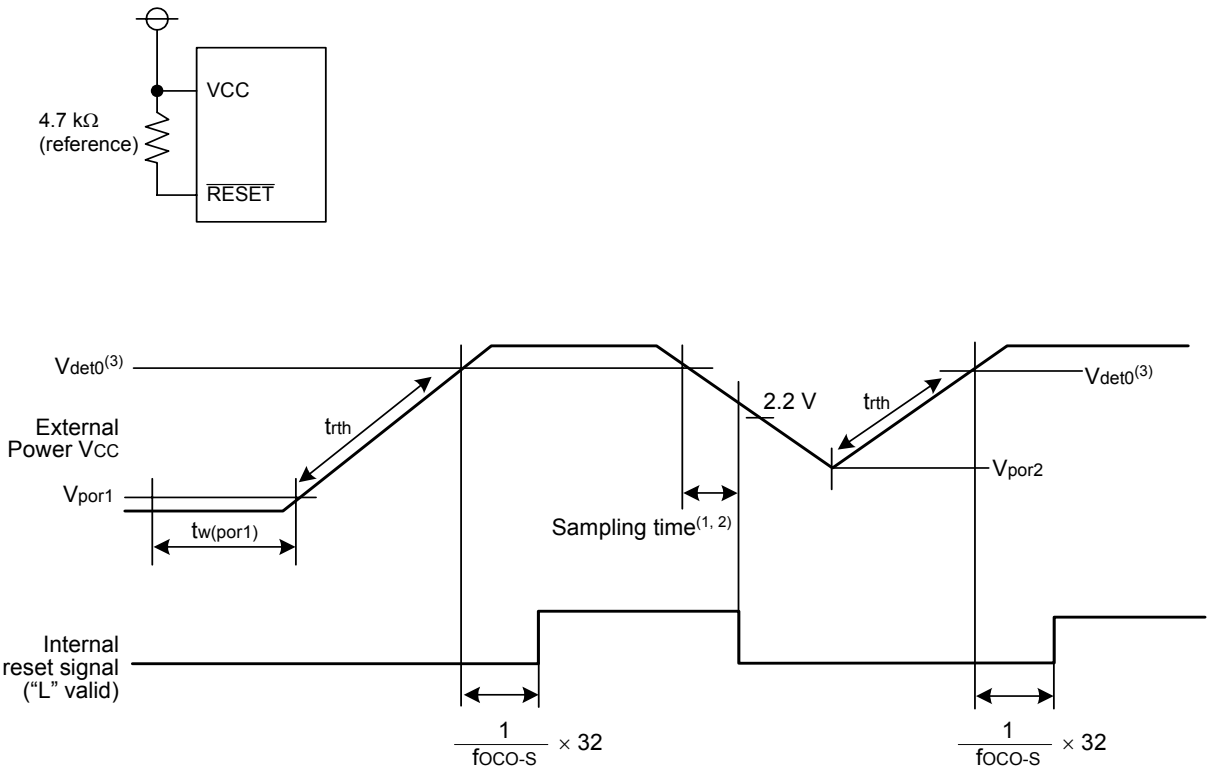


NOTE:
1. Refer to **22. Electrical Characteristics**.

Figure 5.6 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

5.2 Power-On Reset Function

When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises while the rise gradient is trth or more, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFR. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8VCC or more. When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held "H" and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock after reset.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFR after power-on reset.
The voltage monitor 0 reset is enabled after power-on reset.
Figure 5.7 shows an Example of Power-On Reset Circuit and Operation.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
4. Refer to **22. Electrical Characteristics**.
5. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.

Figure 5.7 Example of Power-On Reset Circuit and Operation

5.3 Voltage Monitor 0 Reset

A reset is applied using the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet0.

When the input voltage to the VCC pin reaches the Vdet0 level or below, the pins, CPU, and SFR are reset.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock start counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held “H” and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock after reset.

The LVD0ON bit in the OFS register can be used to enable or disable voltage monitor 0 reset after a hardware reset. Setting the LVD0ON bit is only valid after a hardware reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.

The LVD0ON bit cannot be changed by a program. To set the LVD0ON bit, write 0 (voltage monitor 0 reset enabled after hardware reset) or 1 (voltage monitor 0 reset disabled after hardware reset) to bit 5 of address 0FFFFh using a flash programmer.

Refer to **Figure 5.4 OFS Register** for details of the OFS register.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFR after voltage monitor 0 reset.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet0 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset.

5.4 Voltage Monitor 1 Reset

A reset is applied using the on-chip voltage detection 1 circuit. The voltage detection 1 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet1.

When the input voltage to the VCC pin reaches the Vdet1 level or below, the pins, CPU, and SFR are reset and a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock.

The voltage monitor 1 does not reset some portions of the SFR. Refer to **4. Special Function Registers (SFRs)** for details.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet1 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 1 reset.

5.5 Voltage Monitor 2 Reset

A reset is applied using the on-chip voltage detection 2 circuit. The voltage detection 2 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet2.

When the input voltage to the VCC pin reaches the Vdet2 level or below, the pins, CPU, and SFR are reset and the program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock.

The voltage monitor 2 does not reset some SFRs. Refer to **4. Special Function Registers (SFRs)** for details.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet2 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 2 reset.

5.6 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFR if the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected as the CPU clock.
The watchdog timer reset does not reset some SFRs. Refer to **4. Special Function Registers (SFRs)** for details.
The internal RAM is not reset. When the watchdog timer underflows, the contents of internal RAM are undefined.
Refer to **16. Watchdog Timer** for details of the watchdog timer.

5.7 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFR. The program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock divided by 8 is automatically selected for the CPU clock.
The software reset does not reset some SFRs. Refer to **4. Special Function Registers (SFRs)** for details.
The internal RAM is not reset.

6. Voltage Detection Circuit

The voltage detection circuit monitors the input voltage to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program. Alternately, voltage monitor 0 reset, voltage monitor 1 interrupt, voltage monitor 1 reset, voltage monitor 2 interrupt, and voltage monitor 2 reset can also be used.
Note that voltage monitor 1 and voltage monitor 2 share the voltage detection circuit with comparator 1 and comparator 2. Either voltage monitor 1 and voltage monitor 2 or comparator 1 and comparator 2 can be selected.
Table 6.1 lists the Specifications of Voltage Detection Circuit and Figures 6.1 to 6.4 show the Block Diagrams. Figures 6.5 to 6.10 show the Associated Registers.

Table 6.1 Specifications of Voltage Detection Circuit

Item		Voltage Detection 0	Voltage Detection 1	Voltage Detection 2
VCC Monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by falling	Passing through Vdet1 by rising or falling	Passing through Vdet2 by rising or falling
	Monitor	None	VW1C3 bit in VW1C register	VCA13 bit in VCA1 register
			Whether VCC is higher or lower than Vdet1	Whether VCC is higher or lower than Vdet2
Process When Voltage is Detected	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset at Vdet0 > VCC; restart CPU operation at VCC > Vdet0	Reset at Vdet1 > VCC; restart CPU operation after a specified time	Reset at Vdet2 > VCC; restart CPU operation after a specified time
	Interrupt	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Interrupt request at both or either of Vdet1 > VCC and VCC > Vdet1	Interrupt request at both or either of Vdet2 > VCC and VCC > Vdet2
Digital Filter	Switch enabled/disabled	Available	Available	Available
	Sampling time	(Divide-by-n of fOCO-S) × 4 n: 1, 2, 4, and 8	(Divide-by-n of fOCO-S) × 2 n: 1, 2, 4, and 8	(Divide-by-n of fOCO-S) × 2 n: 1, 2, 4, and 8

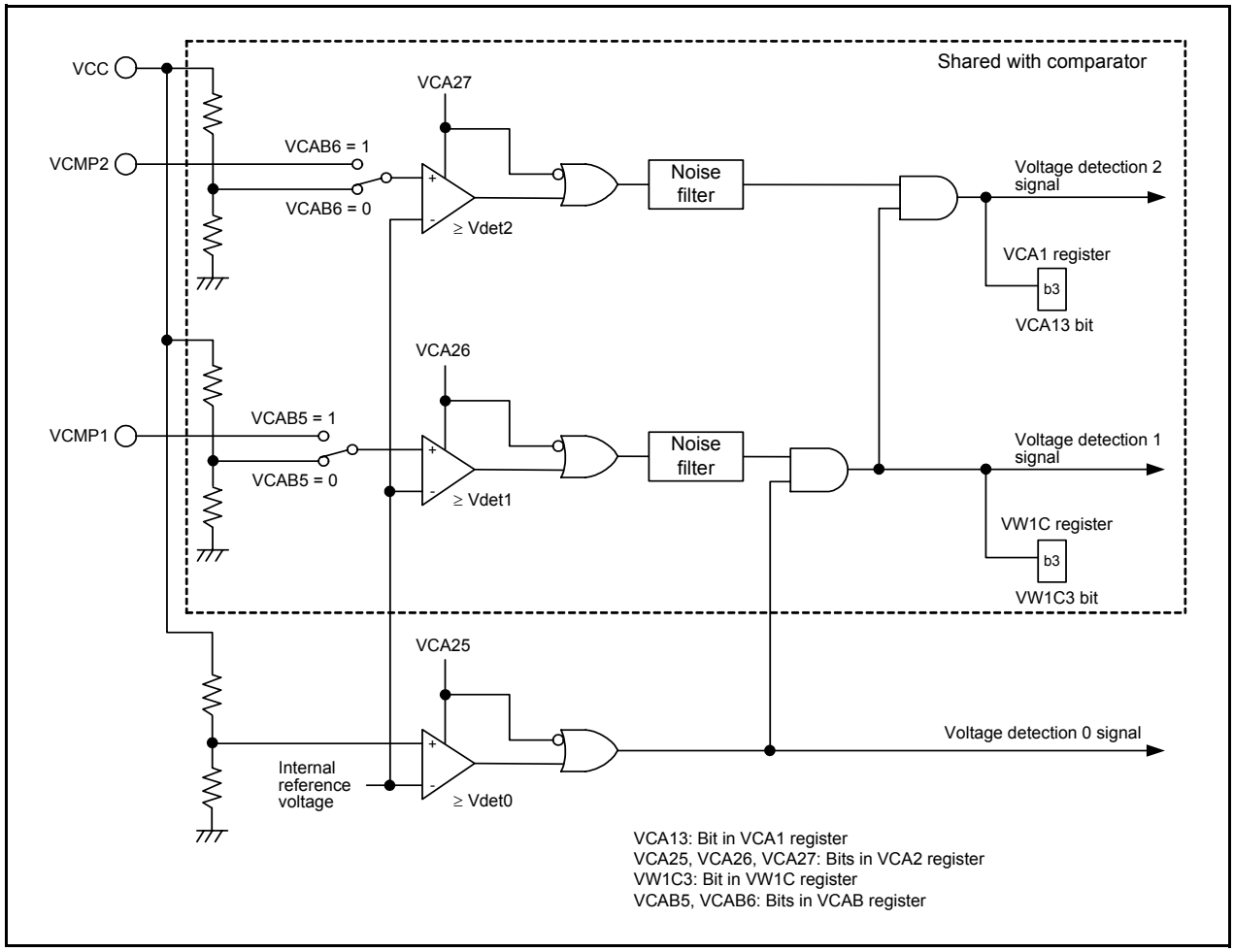


Figure 6.1 Block Diagram of Voltage Detection Circuit

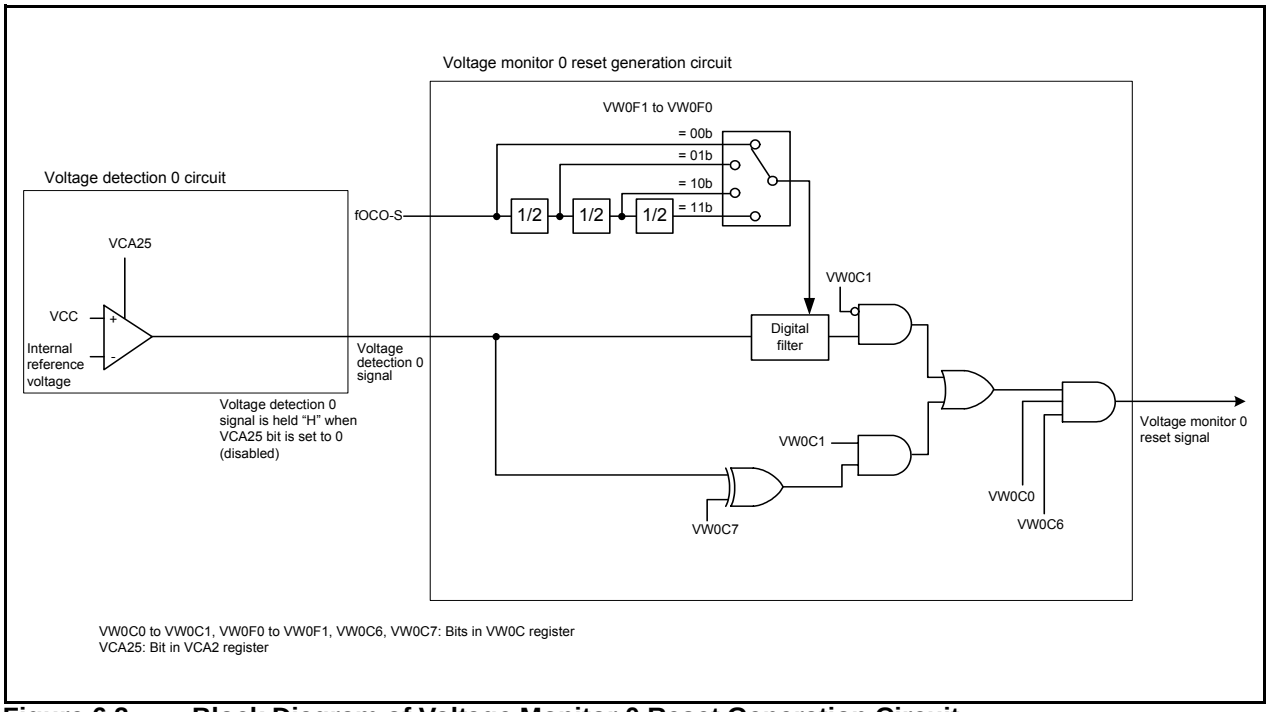


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

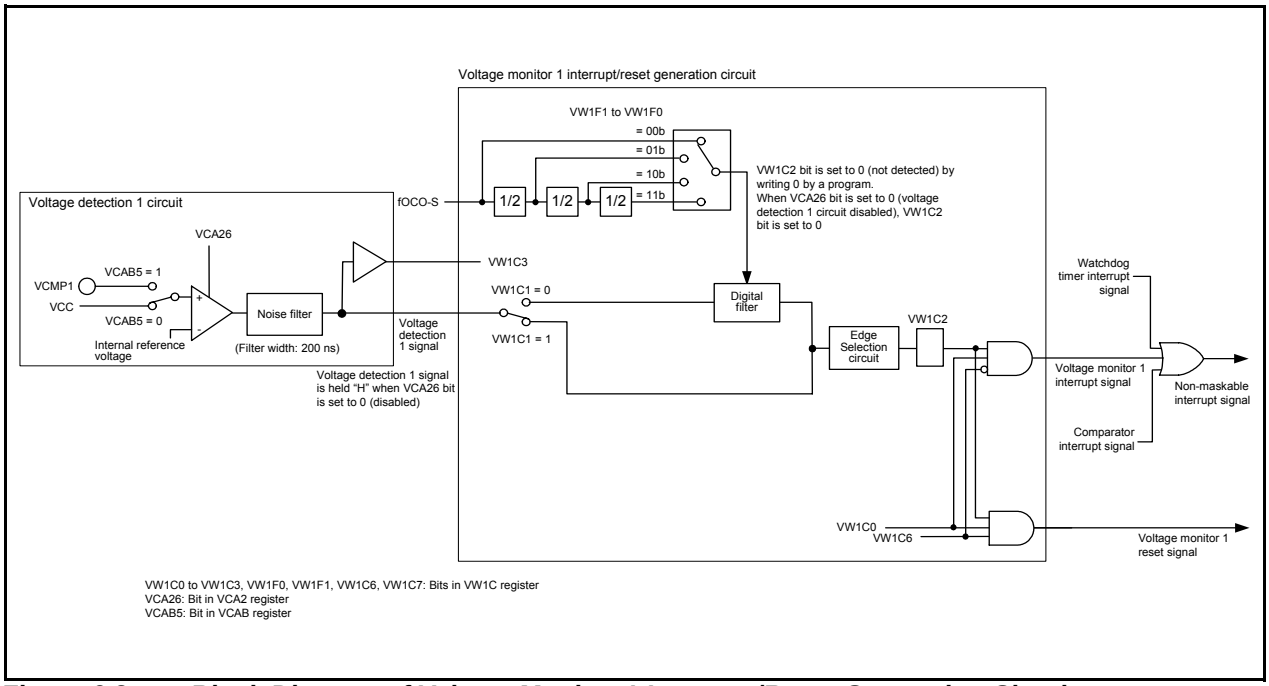


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt/Reset Generation Circuit

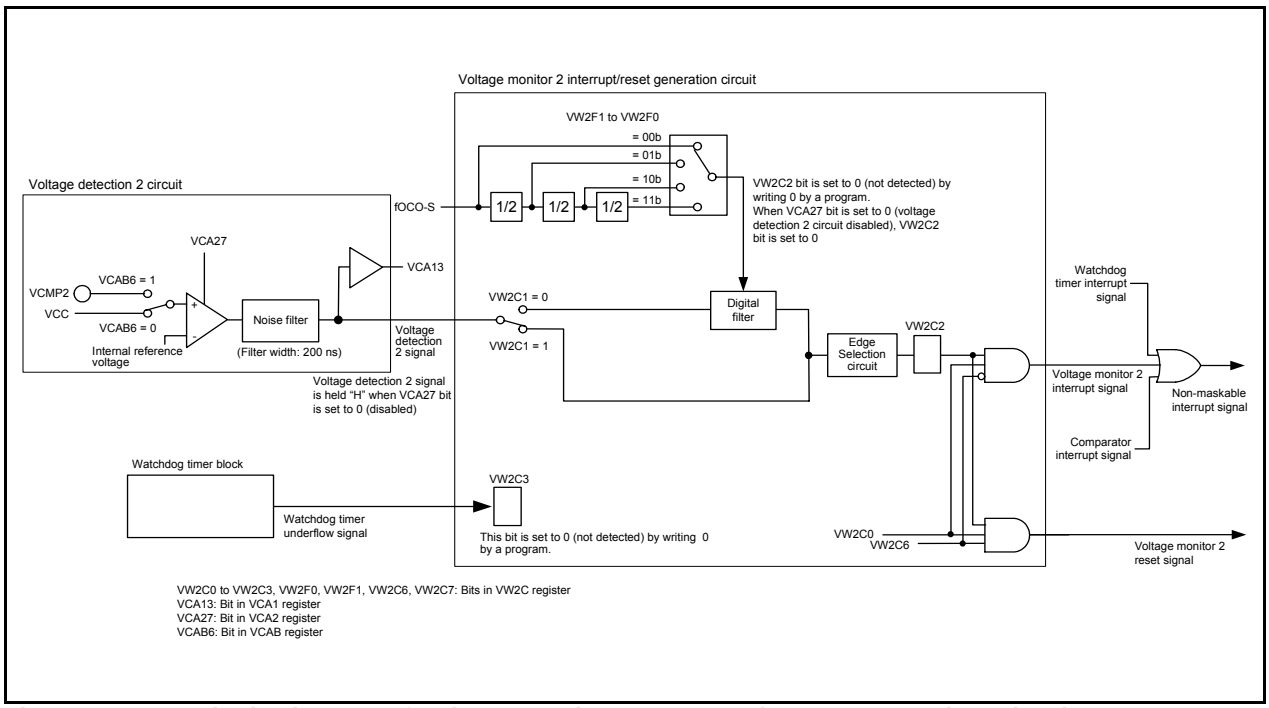
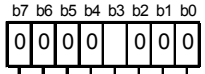


Figure 6.4 Block Diagram of Voltage Monitor 2 Interrupt/Reset Generation Circuit

Voltage Detection Register 1

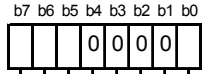


Symbol	Address	After Reset(2)
VCA1	0031h	00001000b

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0.	RW
VCA13	Voltage detection 2 signal monitor flag(1)	0 : VCC < Vdet2 1 : VCC ≥ Vdet2 or voltage detection 2 circuit disabled	RO
— (b7-b4)	Reserved bits	Set to 0.	RW

NOTES:
1. The VCA13 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). The VCA13 bit is set to 1 (VCC ≥ Vdet 2) when the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled).
2. Software reset, watchdog timer reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect this register.

Voltage Detection Register 2(1)



Symbol	Address	After Reset(5)
VCA2	0032h	The LVD0ON bit in the OFS register is set to 1 and hardware reset : 00h Power-on reset, voltage monitor 0 reset or LVD0ON bit in the OFS register is set to 0, and hardware reset : 00100000b

Bit Symbol	Bit Name	Function	RW
VCA20	Internal power low consumption enable bit(6)	0 : Low consumption disabled 1 : Low consumption enabled(7)	RW
— (b4-b1)	Reserved bits	Set to 0.	RW
VCA25	Voltage detection 0 enable bit(2)	0 : Voltage detection 0 circuit disabled 1 : Voltage detection 0 circuit enabled	RW
VCA26	Voltage detection 1 enable bit(3)	0 : Voltage detection 1 circuit disabled 1 : Voltage detection 1 circuit enabled	RW
VCA27	Voltage detection 2 enable bit(4)	0 : Voltage detection 2 circuit disabled 1 : Voltage detection 2 circuit enabled	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting to the VCA2 register.
2. To use the voltage monitor 0 reset, set the VCA25 bit to 1.
   After the VCA25 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
3. To use the voltage monitor 1 interrupt/reset or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1.
   After the VCA26 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
4. To use the voltage monitor 2 interrupt/reset or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect this register.
6. Use the VCA20 bit only when entering to wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 11.12 Handling Procedure of Internal Power Low Consumption Using VCA20 Bit**.
7. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).

Figure 6.5 Registers VCA1 and VCA2

Voltage Monitor 0 Circuit Control Register (1)

b7	b6	b5	b4	b3	b2	b1	b0
					0		

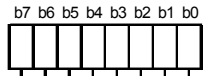
Symbol	Address	After Reset(2)
VW0C	0038h	The LVD0ON bit in the OFS register is set to 1 and hardware reset : 1000X010b Power-on reset, voltage monitor 0 reset or LVD0ON bit in the OFS register is set to 0, and hardware reset : 1100X011b

Bit Symbol	Bit Name	Function	RW
VW0C0	Voltage monitor 0 reset enable bit(3)	0 : Disable 1 : Enable	RW
VW0C1	Voltage monitor 0 digital filter disable mode select bit	0 : Digital filter enabled mode (digital filter circuit enabled) 1 : Digital filter disabled mode (digital filter circuit disabled)	RW
VW0C2	Reserved bit	Set to 0.	RW
— (b3)	Reserved bit	When read, the content is undefined.	RO
VW0F0	Sampling clock select bits	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW0F1			RW
VW0C6	Voltage monitor 0 circuit mode select bit	When the VW0C0 bit is set to 1 (voltage monitor 0 reset enabled), set to 1.	RW
VW0C7	Voltage monitor 0 reset generation condition select bit(4)	When the VW0C1 bit is set to 1 (digital filter disabled mode), set to 1.	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting to the VW0C register.
2. The value remains unchanged after a software reset, watchdog timer reset, voltage monitor 1 reset, and voltage monitor 2 reset.
3. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled). Set the VW0C0 bit to 0 (disable), when the VCA25 bit is set to 0 (voltage detection 0 circuit disabled). To set VW0C0 bit to 1 (enable), follow the procedure shown in **Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset**.
4. The VW0C7 bit is enabled when the VW0C1 bit set to 1 (digital filter disabled mode).

Figure 6.6 VW0C Register

Voltage Monitor 1 Circuit Control Register (1)



Symbol	Address	After Reset(8)
VW1C	0036h	00001010b

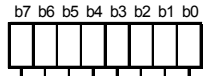
Bit Symbol	Bit Name	Function	RW
VW1C0	Voltage monitor 1 interrupt/reset enable bit(6)	0 : Disable 1 : Enable	RW
VW1C1	Voltage monitor 1 digital filter disable mode select bit(2)	0 : Digital filter enabled mode (digital filter circuit enabled) 1 : Digital filter disabled mode (digital filter circuit disabled)	RW
VW1C2	Voltage change detection flag(3, 4, 8)	0 : Not detected 1 : Vdet1 crossing detected	RW
VW1C3	Voltage detection 1 signal monitor flag(3, 8)	0 : VCC < Vdet1 1 : VCC ≥ Vdet1 or voltage detection 1 circuit disabled	RO
VW1F0	Sampling clock select bits	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW1F1			RW
VW1C6	Voltage monitor 1 circuit mode select bit(5)	0 : Voltage monitor 1 interrupt mode 1 : Voltage monitor 1 reset mode	RW
VW1C7	Voltage monitor 1 interrupt/reset generation condition select bit(7, 9)	0 : When VCC reaches Vdet1 or above 1 : When VCC reaches Vdet1 or below	RW

NOTES:

1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting to the VW1C register. When the VW1C register is rewritten, the VW1C2 bit may be set to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.
2. To use the voltage monitor 1 interrupt to exit stop mode and to return again, write 0 to the VW1C1 bit before writing 1.
3. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, it is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW1C6 bit is enabled when the VW1C0 bit is set to 1 (voltage monitor 1 interrupt/reset enabled).
6. The VW1C0 bit is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disable) when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled). To set VW1C0 bit to 1 (enable), follow the procedure shown in **Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt and Reset**.
7. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). Set the VW1C7 bit after setting the VCAC1 bit to 0.
8. Bits VW1C2 and VW1C3 remain unchanged after a software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset.
9. When the VW1C6 bit is set to 1 (voltage monitor 1 reset mode), set the VW1C7 bit to 1 (when VCC reaches Vdet1 or below). (Do not set to 0.)

Figure 6.7 VW1C Register

Voltage Monitor 2 Circuit Control Register (1)



Symbol	Address	After Reset(8)
VW2C	0037h	00000010b

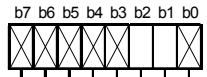
Bit Symbol	Bit Name	Function	RW
VW2C0	Voltage monitor 2 interrupt/reset enable bit(6)	0 : Disable 1 : Enable	RW
VW2C1	Voltage monitor 2 digital filter disable mode select bit(2)	0 : Digital filter enabled mode (digital filter circuit enabled) 1 : Digital filter disabled mode (digital filter circuit disabled)	RW
VW2C2	Voltage change detection flag(3, 4, 8)	0 : Not detected 1 : Vdet2 crossing detected	RW
VW2C3	WDT detection flag(4, 8)	0 : Not detected 1 : Detected	RW
VW2F0	Sampling clock select bits	b5 b4 0 0 : fOCO-S divided by 1 0 1 : fOCO-S divided by 2 1 0 : fOCO-S divided by 4 1 1 : fOCO-S divided by 8	RW
VW2F1			RW
VW2C6	Voltage monitor 2 circuit mode select bit(5)	0 : Voltage monitor 2 interrupt mode 1 : Voltage monitor 2 reset mode	RW
VW2C7	Voltage monitor 2 interrupt/reset generation condition select bit(7, 9)	0 : When VCC reaches Vdet2 or above 1 : When VCC reaches Vdet2 or below	RW

NOTES:

1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting to the VW2C register. When the VW2C register is rewritten, the VW2C2 bit may be set to 1. Set the VW2C2 bit to 0 after rewriting the VW2C register.
2. To use the voltage monitor 2 interrupt to exit stop mode and to return again, write 0 to the VW2C1 bit before writing 1.
3. The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, it is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW2C6 bit is enabled when the VW2C0 bit is set to 1 (voltage monitor 2 interrupt/reset enabled).
6. The VW2C0 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disable) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled). To set VW2C0 bit to 1 (enable), follow the procedure shown in **Table 6.4 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt and Reset**.
7. The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). Set the VW2C7 bit after setting the VCAC2 bit to 0.
8. Bits VW2C2 and VW2C3 remain unchanged after a software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset.
9. When the VW2C6 bit is set to 1 (voltage monitor 2 reset mode), set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below). (Do not set to 0.)

Figure 6.8 VW2C Register

Voltage Monitor Circuit Edge Select Register



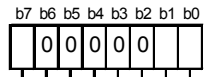
Symbol	Address	After Reset
VCAC	003Dh	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
VCAC1	Voltage monitor 1 circuit edge select bit(1)	0 : One edge 1 : Both edges	RW
VCAC2	Voltage monitor 2 circuit edge select bit(2)	0 : One edge 1 : Both edges	RW
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. The VW1C7 bit in the VW1C register is enabled when the VCAC1 bit is set to 0 (one edge). Set the VW1C7 bit after setting the VCAC1 bit to 0.
2. The VW2C7 bit in the VW2C register is enabled when the VCAC2 bit is set to 0 (one edge). Set the VW2C7 bit after setting the VCAC2 bit to 0.

Figure 6.9 VCAC Register

Pin Select Register 4 (R8C/2H Group)

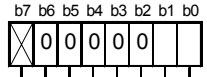


Symbol	Address	After Reset
PINSR4	02FBh	00h

Bit Symbol	Bit Name	Function	RW
TRFOSEL	TRFO11 pin select bit(1)	0 : Disabled 1 : Enabled	RW
COMPSEL	Voltage monitor/comparator select bit	0 : Voltage monitor 1, voltage monitor 2 1 : Comparator 1, comparator 2	RW
— (b6-b2)	Reserved bits	Set to 0.	RW
TREOSEL2	TREO pin select 2 bit(2)	0 : Disabled 1 : Enabled	RW

NOTES:
1. Set the TRFOSEL bit to 1 (enabled) before using timer RF.
2. Set the TREOSEL2 bit to 1 (enabled) before using timer RE.

Pin Select Register 4 (R8C/2J Group)



Symbol	Address	After Reset
PINSR4	02FBh	00h

Bit Symbol	Bit Name	Function	RW
TRFOSEL	TRFO11 pin select bit(1)	0 : Disabled 1 : Enabled	RW
COMPSEL	Voltage monitor/comparator select bit	0 : Voltage monitor 1, voltage monitor 2 1 : Comparator 1, comparator 2	RW
— (b6-b2)	Reserved bits	Set to 0.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Set the TRFOSEL bit to 1 (enabled) before using timer RF.

Figure 6.10 PINSR4 Register

6.1 VCC Input Voltage

6.1.1 Monitoring Vdet0

Vdet0 cannot be monitored.

6.1.2 Monitoring Vdet1

Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled). After td(E-A) has elapsed (refer to **22. Electrical Characteristics**), Vdet1 can be monitored by the VW1C3 bit in the VW1C register.

6.1.3 Monitoring Vdet2

Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled). After td(E-A) has elapsed (refer to **22. Electrical Characteristics**), Vdet2 can be monitored by the VCA13 bit in the VCA1 register.

6.2 Voltage Monitor 0 Reset

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor 0 Reset and Figure 6.11 shows an Example of Voltage Monitor 0 Reset Operation. To use the voltage monitor 0 reset to exit stop mode, set the VW0C1 bit in the VW0C register to 1 (digital filter disabled).

Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset

Step	When Using Digital Filter	When Not Using Digital Filter
1	Set the VCA25 bit in the VCA2 register to 1 (voltage detection 0 circuit enabled)	
2	Wait for td(E-A)	
3	Select the sampling clock of the digital filter by the VW0F0 to VW0F1 bits in the VW0C register	Set the VW0C7 bit in the VW0C register to 1
4(1)	Set the VW0C1 bit in the VW0C register to 0 (digital filter enabled)	Set the VW0C1 bit in the VW0C register to 1 (digital filter disabled)
5(1)	Set the VW0C6 bit in the VW0C register to 1 (voltage monitor 0 reset mode)	
6	Set the VW0C2 bit in the VW0C register to 0	
7	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	–
8	Wait for 4 cycles of the sampling clock of the digital filter	– (No wait time required)
9	Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled)	

NOTE:
1. When the VW0C0 bit is set to 0, steps 3, 4, and 5 can be executed simultaneously (with 1 instruction).

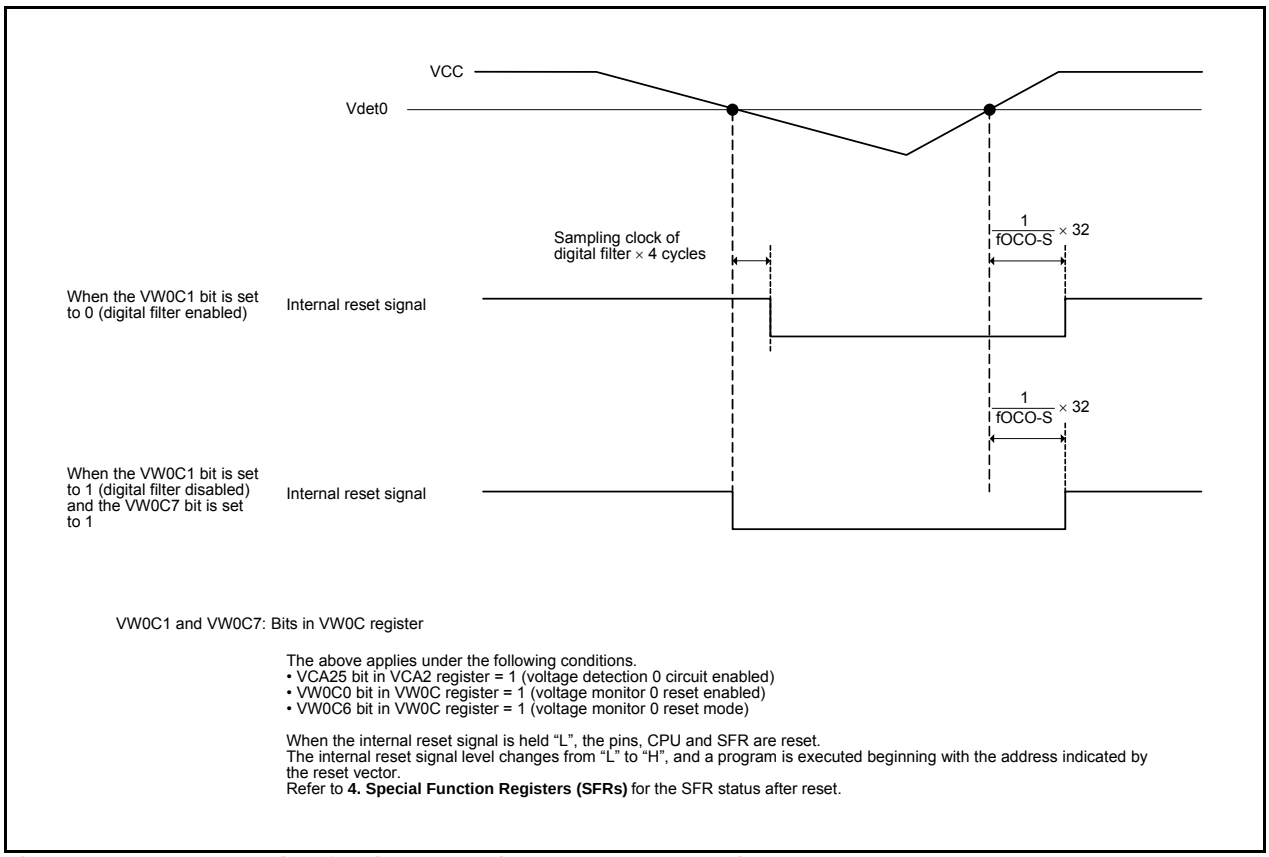


Figure 6.11 Example of Voltage Monitor 0 Reset Operation

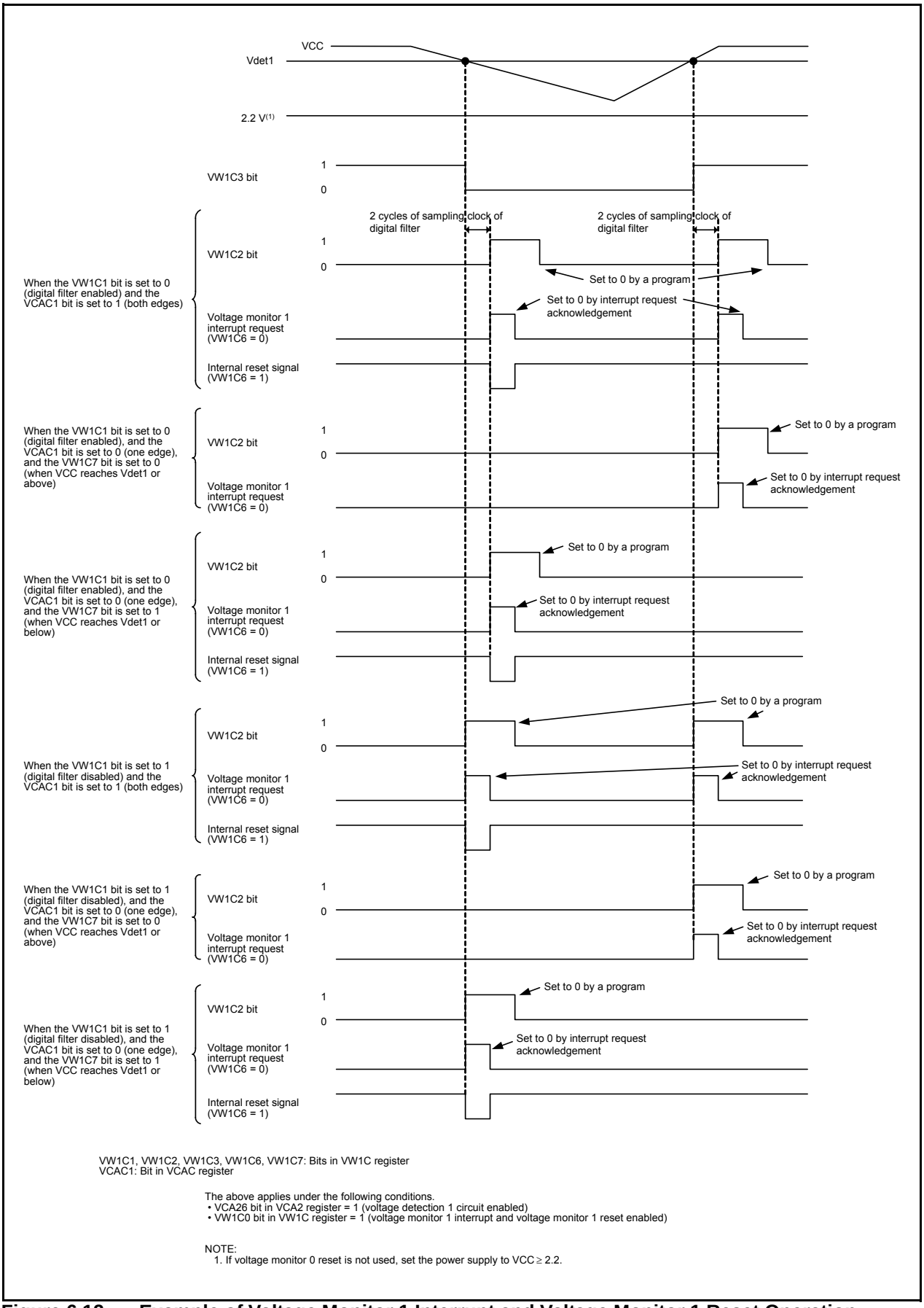
6.3 Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt and Reset. Figure 6.12 shows an Example of Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset Operation. To use the voltage monitor 1 interrupt or voltage monitor 1 reset to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt and Reset

Step	When Using Digital Filter		When Not Using Digital Filter	
	Voltage Monitor 1 Interrupt	Voltage Monitor 1 Reset	Voltage Monitor 1 Interrupt	Voltage Monitor 1 Reset
1	Set the COMPSEL bit in the PINSR4 register to 0 (voltage monitor 1, voltage monitor 2)			
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled)			
3	Wait for td(E-A)			
4	Select the sampling clock of the digital filter by the VW1F0 to VW1F1 bits in the VW1C register		Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled)	
5(2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled)		–	
6	Select the timing of the interrupt and reset request by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register(1)		Select the timing of the interrupt and reset request by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register(1)	
7	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt mode)	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset mode)	Set the VW1C6 bit in the VW1C register to 0 (voltage monitor 1 interrupt mode)	Set the VW1C6 bit in the VW1C register to 1 (voltage monitor 1 reset mode)
8	Set the VW1C2 bit in the VW1C register to 0 (Vdet1 crossing is not detected)			
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)		–	
10	Wait for 2 cycles of the sampling clock of the digital filter		– (No wait time required)	
11	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt/reset enabled)			

NOTES:
1. Set the VW1C7 bit to 1 (when VCC reaches Vdet1 or below) for the voltage monitor 1 reset.
2. When the VW1C0 bit is set to 0, steps 4 and 5 can be executed simultaneously (with 1 instruction).



VW1C1, VW1C2, VW1C3, VW1C6, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register

The above applies under the following conditions.
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage monitor 1 interrupt and voltage monitor 1 reset enabled)

NOTE:
1. If voltage monitor 0 reset is not used, set the power supply to VCC ≥ 2.2.

Figure 6.12 Example of Voltage Monitor 1 Interrupt and Voltage Monitor 1 Reset Operation

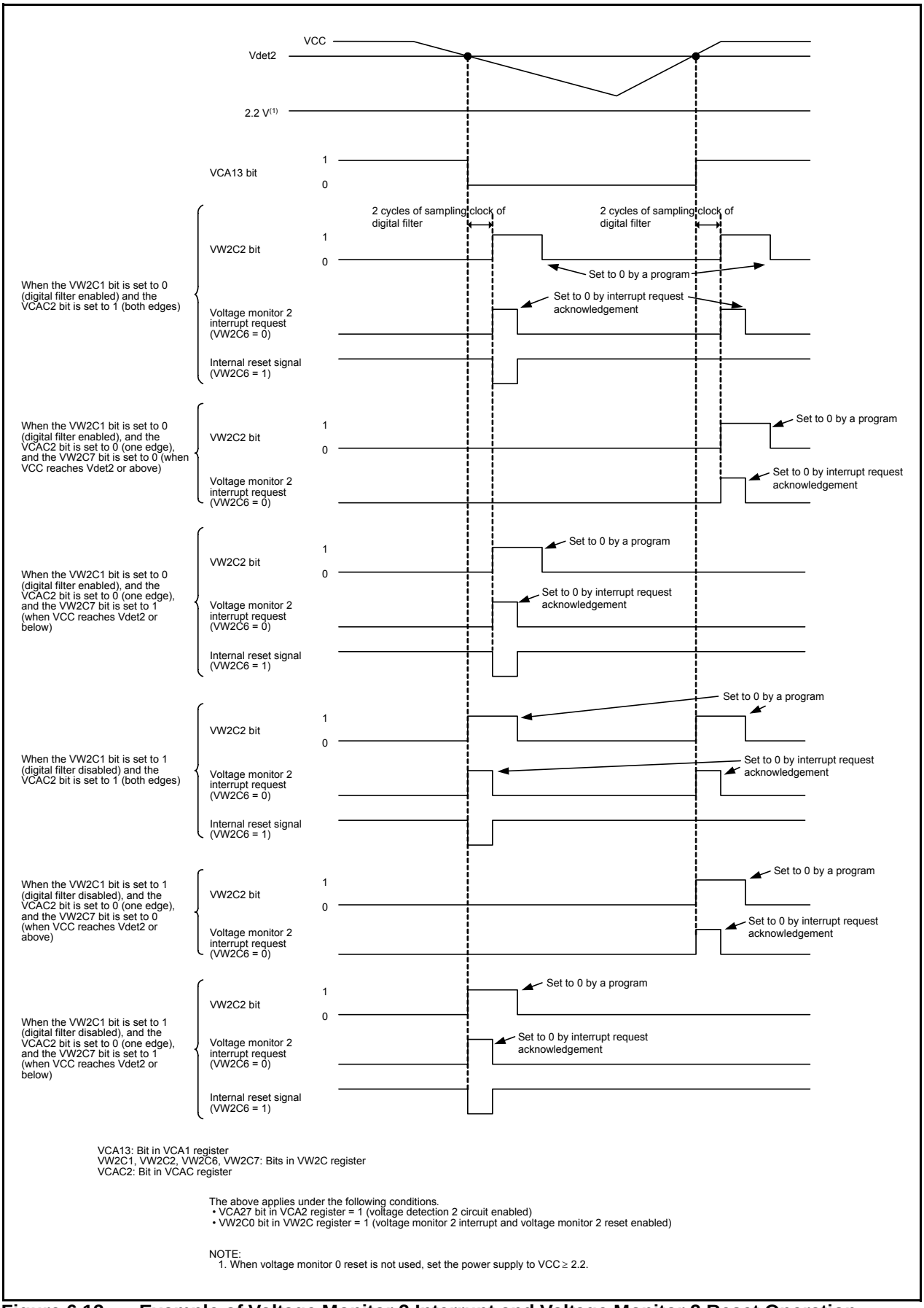
6.4 Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset

Table 6.4 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt and Reset. Figure 6.13 shows an Example of Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset Operation. To use the voltage monitor 2 interrupt or voltage monitor 2 reset to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Table 6.4 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt and Reset

Step	When Using Digital Filter		When Not Using Digital Filter	
	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset	Voltage Monitor 2 Interrupt	Voltage Monitor 2 Reset
1	Set the COMPSEL bit in the PINSR4 register to 0 (voltage monitor 1, voltage monitor 2)			
2	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled)			
3	Wait for td(E-A)			
4	Select the sampling clock of the digital filter by the VW2F0 to VW2F1 bits in the VW2C register		Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled)	
5(2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled)		–	
6	Select the timing of the interrupt and reset request by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register(1)		Select the timing of the interrupt and reset request by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register(1)	
7	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode)	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode)	Set the VW2C6 bit in the VW2C register to 0 (voltage monitor 2 interrupt mode)	Set the VW2C6 bit in the VW2C register to 1 (voltage monitor 2 reset mode)
8	Set the VW2C2 bit in the VW2C register to 0 (Vdet2 crossing is not detected)			
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)		–	
10	Wait for 2 cycles of the sampling clock of the digital filter		– (No wait time required)	
11	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt/reset enabled)			

NOTES:
1. Set the VW2C7 bit to 1 (when VCC reaches Vdet2 or below) for the voltage monitor 2 reset.
2. When the VW2C0 bit is set to 0, steps 4 and 5 can be executed simultaneously (with 1 instruction).



VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C6, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register

The above applies under the following conditions.
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (voltage monitor 2 interrupt and voltage monitor 2 reset enabled)

NOTE:
1. When voltage monitor 0 reset is not used, set the power supply to VCC ≥ 2.2.

Figure 6.13 Example of Voltage Monitor 2 Interrupt and Voltage Monitor 2 Reset Operation

7. Comparator

The comparators compare a reference input voltage and an analog input voltage. Comparator 1 and comparator 2 are independent of each other. Note that comparator 1 and comparator 2 share the voltage detection circuit with voltage monitor 1 and voltage monitor 2. Either comparator 1 and comparator 2 or voltage monitor 1 and voltage monitor 2 can be selected to use the voltage detection circuit.

7.1 Overview

The comparison result of the reference input voltage and analog input voltage can be read by software. The result also can be output from the VCOUTi (i = 1 or 2) pin. An internal reference voltage or input voltage to the CVREF pin can be selected as the reference input voltage. The comparator 1 interrupt and comparator 2 interrupt also can be used.

Table 7.1 lists the Specifications of Comparator, Figure 7.1 shows the Block Diagram of Comparator, and Table 7.2 lists the Pin Configuration of Comparator.

Table 7.1 Specifications of Comparator

Item		Comparator 1	Comparator 2
Analog input voltage		Input voltage to VCMP1 pin	Input voltage to VCMP2 pin
Reference input voltage		Internal reference voltage or input voltage to CVREF pin	
Comparison target		Whether passing thorough reference input voltage by rising or falling	
Comparison result monitor		VW1C3 bit in VW1C register	VCA13 bit in VCA1 register
		Whether higher or lower than reference input voltage	
Interrupt		Comparator 1 interrupt (non-makable or maskable selectable)	Comparator 2 interrupt (non-makable or maskable selectable)
		Interrupt request at both or either of reference input voltage > input voltage to VCMP1 pin and input voltage to VCMP1 pin > reference input voltage	Interrupt request at both or either of reference input voltage > input voltage to VCMP2 pin and input voltage to VCMP2 pin > reference input voltage
Digital Filter	Switch enabled/disabled	Available	
	Sampling time	(fOCO-S divided by n) × 2 n: 1, 2, 4, 8	
Comparison result output		Output from VCOUT1 pin (Whether the comparison result output is inverted or not can be selected)	Output from VCOUT2 pin (Whether the comparison result output is inverted or not can be selected)

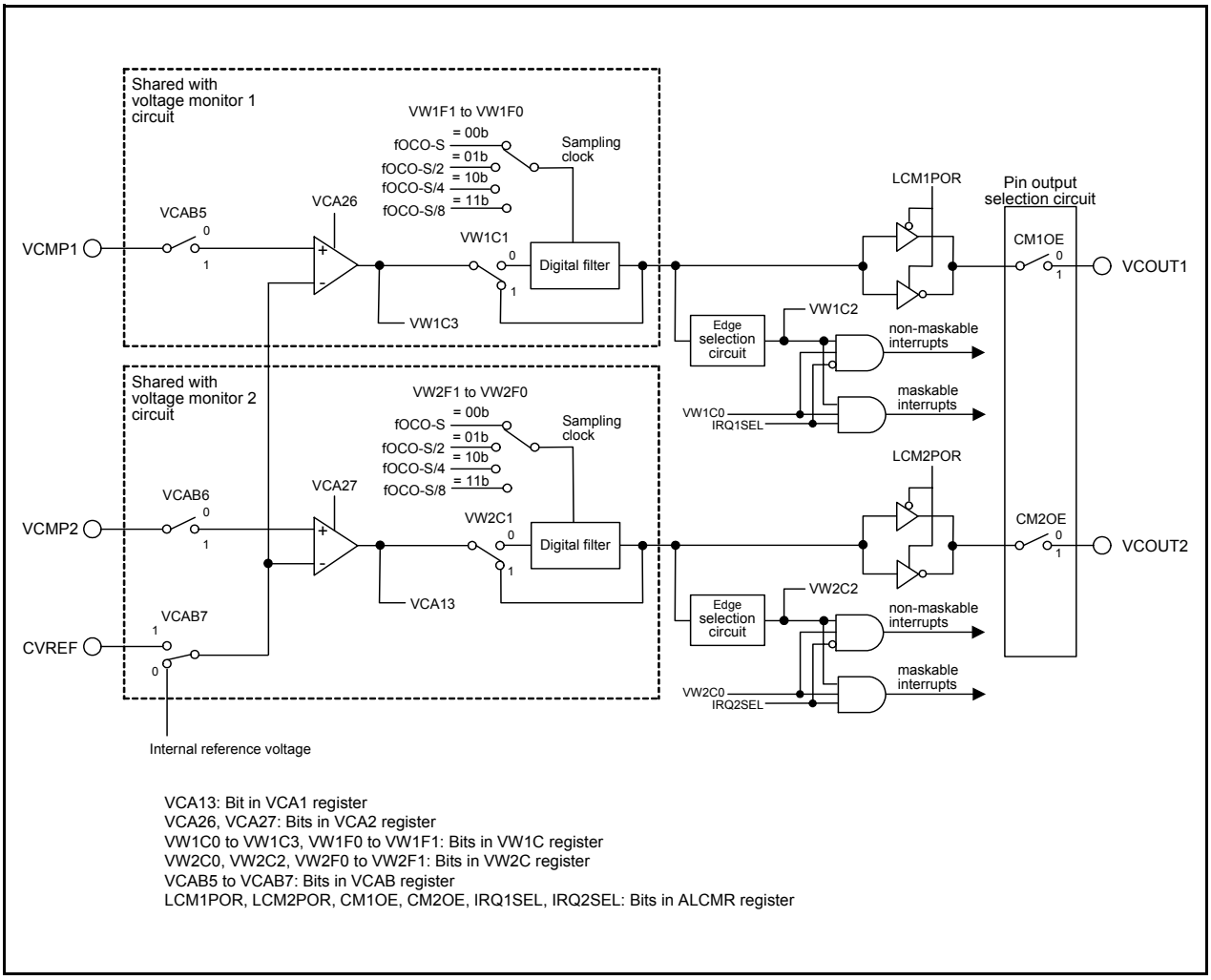


Figure 7.1 Block Diagram of Comparator

Table 7.2 Pin Configuration of Comparator

Pin Name	I/O	Function
VCMP1	Input	Comparator 1 analog pin
VCOUT1	Output	Comparator 1 comparison result output pin
VCMP2	Input	Comparator 2 analog pin
VCOUT2	Output	Comparator 2 comparison result output pin
CVREF	Input	Comparator reference voltage pin

7.2 Register Description

Figures 7.2 to 7.11 show the registers associated with the comparator when comparator 1 or comparator 2 is selected.

BGR Trimming Auxiliary Register A

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
BGRTRMA	002Eh	When Shipping

Function	RW
Stores data for internal reference voltage (Vref) correction when VCC = 3.6 to 5.5 V. (The value is the same as that of the BGRTRM register after a reset). Optimal correction to match the voltage conditions can be achieved by transferring this value to the BGRTRM register.	RO

BGR Trimming Auxiliary Register B

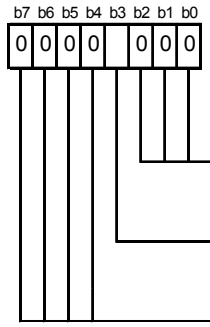
b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
BGRTRMB	002Fh	When Shipping

Function	RW
Stores data for internal reference voltage (Vref) correction when VCC = 2.2 to 3.6 V. Optimal correction to match the voltage conditions can be achieved by transferring this value to the BGRTRM register.	RO

Figure 7.2 Registers BGRTRMA and BGRTRMB

Voltage Detection Register 1

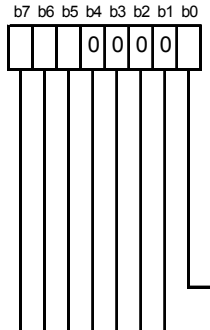


Symbol	Address	After Reset(2)
VCA1	0031h	00001000b

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0.	RW
VCA13	Comparator 2 signal monitor flag(1)	0: VCMP2 < reference voltage 1: VCMP2 ≥ reference voltage or comparator 2 circuit disabled	RO
— (b7-b4)	Reserved bits	Set to 0.	RW

NOTES:
1. The VCA13 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (comparator 2 circuit enabled). The VCA13 bit is set to 1 (VCMP2 ≥ reference voltage) when the VCA27 bit in the VCA2 register is set to 0 (comparator 2 circuit disabled).
2. Software reset and watchdog timer reset do not affect this register.

Voltage Detection Register 2(1)



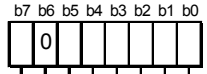
Symbol	Address	After Reset(2)
VCA2	0032h	The LVD0ON bit in the OFS register is set to 1 and hardware reset : 00h Power-on reset, voltage monitor 0 reset or the LVD0ON bit in the OFS register is set to 0, and hardware reset : 00100000b

Bit Symbol	Bit Name	Function	RW
VCA20	Internal power low consumption enable bit(3)	0: Low consumption disabled 1: Low consumption enabled(7)	RW
— (b4-b1)	Reserved bits	Set to 0.	RW
VCA25	Voltage detection 0 enable bit(4)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	RW
VCA26	Comparator 1 enable bit(5)	0: Comparator 1 circuit disabled 1: Comparator 1 circuit enabled	RW
VCA27	Comparator 2 enable bit(6)	0: Comparator 2 circuit disabled 1: Comparator 2 circuit enabled	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.
2. Software reset and watchdog timer reset do not affect this register.
3. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 11.12 Handling Procedure of Internal Power Low Consumption Using VCA20 Bit**.
4. To use the voltage monitor 0 reset, set the VCA25 bit to 1.
   After the VCA25 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
5. To use the comparator 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1.
   After the VCA26 bit is set to 1 from 0, the comparator 1 circuit waits for td(E-A) to elapse before starting operation.
6. To use the comparator 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is set to 1 from 0, the comparator 2 circuit waits for td(E-A) to elapse before starting operation.
7. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).

Figure 7.3 Registers VCA1 and VCA2

Voltage Monitor 1 Circuit Control Register (1)



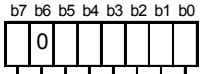
Symbol	Address	After Reset(2)
VW1C	0036h	00001010b

Bit Symbol	Bit Name	Function	RW
VW1C0	Comparator 1 interrupt enable bit(3)	0: Disable 1: Enable	RW
VW1C1	Comparator 1 digital filter disable mode select bit(4)	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	RW
VW1C2	Comparator 1 interrupt flag(2, 5, 6)	[Source for setting this bit to 0] 0: Write 0 [Source for setting this bit to 0] 1: When interrupt request is generated	RW
VW1C3	Comparator 1 signal monitor flag(2, 5)	0: VCMP1 < reference voltage 1: VCMP1 ≥ reference voltage or comparator 1 circuit disabled	RO
VW1F0	Sampling clock select bits	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	RW
VW1F1			RW
VW1C6	Reserved bit	Set to 0.	RW
VW1C7	Comparator 1 interrupt generation condition select bit(7)	0: When VCMP1 reaches reference voltage or above 1: When VCMP1 reaches reference voltage or below	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW1C register. When the VW1C register is rewritten, the VW1C2 bit may be set to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.
2. Bits VW1C2 and VW1C3 remain unchanged after a software reset or watchdog timer reset.
3. The VW1C0 is enabled when the VCA26 bit in the VCA2 register is set to 1 (comparator 1 circuit enabled). When the VCA26 bit is set to 0 (comparator 1 circuit disabled), set the VW1C0 bit to 0 (disable). To set the VW1C0 bit to 1 (enable), follow the procedure shown in **Table 7.3 Procedure for Setting Bits Associated with Comparator 1 Interrupt.**
4. To use the comparator 1 interrupt to exit stop mode and to return again, write 1 to the VW1C1 bit after writing 0.
5. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1 (comparator 1 circuit enabled).
6. Set this bit to 0 by a program. When 0 is written by a program, it is set to 0 (and remains unchanged even if 1 is written to it).
7. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). Set the VW1C7 bit after setting the VCAC1 bit to 0.

Figure 7.4 VW1C Register

Voltage Monitor 2 Circuit Control Register (1)



Symbol	Address	After Reset(2)
VW2C	0037h	00000010b

Bit Symbol	Bit Name	Function	RW
VW2C0	Comparator 2 interrupt enable bit(3)	0: Disable 1: Enable	RW
VW2C1	Comparator 2 digital filter disable mode select bit(4)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	RW
VW2C2	Comparator 2 interrupt flag(2, 5, 6)	[Source for setting this bit to 0] 0: Write 0 [Source for setting this bit to 0] 1: When interrupt request is generated	RW
VW2C3	WDT detection flag(2, 6)	0: Not detected 1: Detected	RW
VW2F0	Sampling clock select bits	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	RW
VW2F1			RW
VW2C6	Reserved bit	Set to 0.	RW
VW2C7	Comparator 2 interrupt generation condition select bit(7)	0: When VCMP2 reaches reference voltage or above 1: When VCMP2 reaches reference voltage or below	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register. When the VW2C register is rewritten, the VW2C2 bit may be set to 1. Set the VW2C2 bit to 0 after rewriting the VW2C register.
2. Bits VW2C2 and VW2C3 remain unchanged after a software reset or watchdog timer reset.
3. The VW2C0 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (comparator 2 circuit enabled). Set the VW2C0 bit to 0 (disable) when the VCA27 bit is set to 0 (comparator 2 circuit disabled). To set the VW2C0 bit to 1 (enable), follow the procedure shown in **Table 7.4 Procedure for Setting Bits Associated with Comparator 2 Interrupt**.
4. To use the comparator 2 interrupt to exit stop mode and to return again, write 1 to the VW2C1 bit after writing 0.
5. The VW2C2 is enabled when the VCA27 bit in the VCA2 register is set to 1 (comparator 2 circuit enabled).
6. Set this bit to 0 by a program. When 0 is written by a program, it is set to 0 (and remains unchanged even if 1 is written to it).
7. The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). Set the VW2C7 bit after setting the VCAC2 bit to 0.

Figure 7.5 VW2C Register

Voltage Detection Circuit External Input Control Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
			0	0	0	0	0

Symbol	Address	After Reset
VCAB	003Bh	00h

Bit Symbol	Bit Name	Function	RW
— (b4-b0)	Reserved bits	Set to 0.	RW
VCAB5	VCMP1 comparison voltage external input select bit	0: Supply voltage (VCC) 1: VCMP1 pin input voltage	RW
VCAB6	VCMP2 comparison voltage external input select bit	0: Supply voltage (VCC) 1: VCMP2 pin input voltage	RW
VCAB7	Comparator circuit reference voltage select bit	0: Internal reference voltage 1: CVREF pin input voltage	RW

NOTE:
1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCAB register.

Figure 7.6 VCAB Register

Comparator Mode Register

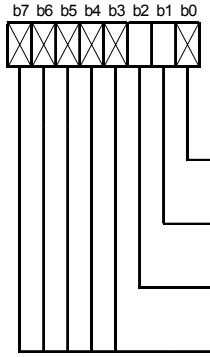
b7	b6	b5	b4	b3	b2	b1	b0
X	X						

Symbol	Address	After Reset
ALCMR	003Ch	00h

Bit Symbol	Bit Name	Function	RW
LCM1POR	VCOUT1 output polarity select bit	0: Non-inverted comparator 1 comparison result is output to VCOUT1 1: Inverted comparator 1 comparison result is output to VCOUT1	RW
LCM2POR	VCOUT2 output polarity select bit	0: Non-inverted comparator 2 comparison result is output to VCOUT2 1: Inverted comparator 2 comparison result is output to VCOUT2	RW
CM1OE	VCOUT1 output enable bit	0: Output disabled 1: Output enabled	RW
CM2OE	VCOUT2 output enable bit	0: Output disabled 1: Output enabled	RW
IRQ1SEL	Comparator 1 interrupt type select bit	0: Non-maskable interrupt 1: Maskable interrupt	RW
IRQ2SEL	Comparator 2 interrupt type select bit	0: Non-maskable interrupt 1: Maskable interrupt	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 7.7 ALCMR Register

Voltage Monitor Circuit Edge Select Register



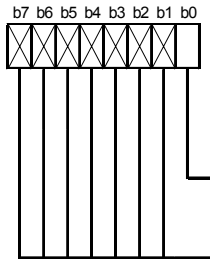
Symbol	Address	After Reset
VCAC	003Dh	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
VCAC1	Comparator 1 circuit edge select bit(1)	0: One edge 1: Both edges	RW
VCAC2	Comparator 2 circuit edge select bit(2)	0: One edge 1: Both edges	RW
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. The VW1C7 bit in the VW1C register is enabled when the VCAC1 bit is set to 0 (one edge). Set the VW1C7 bit after setting the VCAC1 bit to 0.
2. The VW2C7 bit in the VW2C register is enabled when the VCAC2 bit is set to 0 (one edge). Set the VW2C7 bit after setting the VCAC2 bit to 0.

Figure 7.8 VCAC Register

BGR Control Register(1)



Symbol	Address	After Reset
BGRCR	003Eh	00h

Bit Symbol	Bit Name	Function	RW
BGRCR0	Internal reference voltage (Vref) adjustment circuit (BGR trimming circuit) enable bit(2)	0: Enabled 1: Disabled	RW
— (b7-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the BGRCR register.
2. When the BGRCR0 bit is set to 1 (disabled), the accuracy/precision of the following is not guaranteed:
   • Internal reference voltage for comparator 1 and comparator 2
   • Detection voltage for voltage detection circuit 0 to voltage detection circuit 2
   • Oscillation frequency of the high-speed on-chip oscillator
   Use these functions while the BGRCR0 bit is set to 0 (enabled).
   To set the BGRCR0 bit to 1 (disabled), first disable voltage detection circuits 0 to 2 and disable comparators 1 and 2 with the internal reference voltage selected. Also stop the high-speed on-chip oscillator. Then set the BGRCR0 bit to 1 (disabled).

Figure 7.9 BGRCR Register

BGR Trimming Register(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
BGRTRM	003Fh	When Shipping

Function	RW
Bits 0 to 7 can be used to adjust the level of the internal reference voltage (Vref). Write either of the following values into the BGRTRM register. • Value stored in the BGRTRMA register • Value stored in the BGRTRMB register • 15h Do not write values other than the above into the BGRTRM register. Follow the procedure shown in Figure 7.16 for writing data to the BGRTRM register.	RW

NOTE:
1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the BGRTRM register.

Figure 7.10 BGRTRM Register

Pin Select Register 4 (R8C/2H Group)

b7 b6 b5 b4 b3 b2 b1 b0: 0 0 0 0 0 0

Symbol	Address	After Reset
PINSR4	02FBh	00h

Bit Symbol	Bit Name	Function	RW
TRFOSEL	TRFO11 pin select bit(1)	0 : Disabled 1 : Enabled	RW
COMPSEL	Voltage monitor/comparator select bit	0 : Voltage monitor 1, voltage monitor 2 1 : Comparator 1, comparator 2	RW
— (b6-b2)	Reserved bits	Set to 0.	RW
TREOSEL2	TREO pin select 2 bit(2)	0 : Disabled 1 : Enabled	RW

NOTES:
1. Set the TRFOSEL bit to 1 (enabled) before using timer RF.
2. Set the TREOSEL2 bit to 1 (enabled) before using timer RE.

Pin Select Register 4 (R8C/2J Group)

b7 b6 b5 b4 b3 b2 b1 b0: X 0 0 0 0 0

Symbol	Address	After Reset
PINSR4	02FBh	00h

Bit Symbol	Bit Name	Function	RW
TRFOSEL	TRFO11 pin select bit(1)	0 : Disabled 1 : Enabled	RW
COMPSEL	Voltage monitor/comparator select bit	0 : Voltage monitor 1, voltage monitor 2 1 : Comparator 1, comparator 2	RW
— (b6-b2)	Reserved bits	Set to 0.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Set the TRFOSEL bit to 1 (enabled) before using timer RF.

Figure 7.11 PINSR4 Register

7.3 Monitoring Comparison Results

7.3.1 Monitoring Comparator 1

After the following settings are made, the comparison result of comparator 1 can be monitored by the VW1C3 bit in the VW1C register after td(E-A) has elapsed (refer to **22. Electrical Characteristics**).

(1) Set the COMPSEL bit in the PINSR4 register is set to 1 (comparator 1, comparator 2).
(2) Set the VCAB5 bit in the VCAB register to 1 (VCMP1 pin input voltage).
(3) Set the VCA26 bit in the VCA2 register to 1 (comparator 1 circuit enabled).

7.3.2 Monitoring Comparator 2

After the following settings are made, the comparison result of comparator 2 can be monitored by the VCA13 bit in the VCA1 register after td(E-A) has elapsed (refer to **22. Electrical Characteristics**).

(1) Set the COMPSEL bit in the PINSR4 register to 1 (comparator 1, comparator 2).
(2) Set the VCAB6 bit in the VCAB register to 1 (VCMP2 pin input voltage).
(3) Set the VCA27 bit in the VCA2 register to 1 (comparator 2 circuit enabled).

7.4 Functional Description

Comparator 1 and comparator 2 operate independently.
The comparison result of the reference input voltage and analog input voltage can be read by software. The result can also be output from the VCOUTi (i = 1 or 2) pin. An internal reference voltage or input voltage to the CVREF pin can be selected as the reference input voltage. The comparator 1 interrupt or the comparator 2 interrupt also can be used by selecting non-maskable or maskable for each interrupt.

7.4.1 Comparator 1

Table 7.3 lists the Procedure for Setting Bits Associated with Comparator 1 Interrupt, Figure 7.12 shows an Operating Example of Comparator 1 (When Digital Filter Enabled), and Figure 7.13 shows an Operating Example of Comparator 1 (When Digital Filter Disabled).

Table 7.3 Procedure for Setting Bits Associated with Comparator 1 Interrupt

Step	When Using Digital Filter	When Not Using Digital Filter
1	Set the COMPSEL bit in the PINSR4 register to 1 (comparator 1, comparator 2)	
2	Set the VCAB5 bit in the VCAB register to 1 (VCMP1 pin input voltage)	
3	Set the VCA26 bit in the VCA2 register to 1 (comparator 1 circuit enabled)	
4	Wait for td(E-A)	
5	Select the interrupt type by the IRQ1SEL bit in the ALCMR register	
6	Select the sampling clock by bits VW1F0 and VW1F1 in the VW1C register	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled)
7(1)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled)	–
8	Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register	
9	Set the VW1C2 bit in the VW1C register to 0	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	–
11	Wait for 2 cycles of the sampling clock of the digital filter.	– (No wait time required)
12	Set the VW1C0 bit in the VW1C register to 1 (comparator 1 interrupt enabled)	

NOTE:
1. When the VW1C0 bit is set to 0, steps 6 and 7 can be executed at the same time (with one instruction)

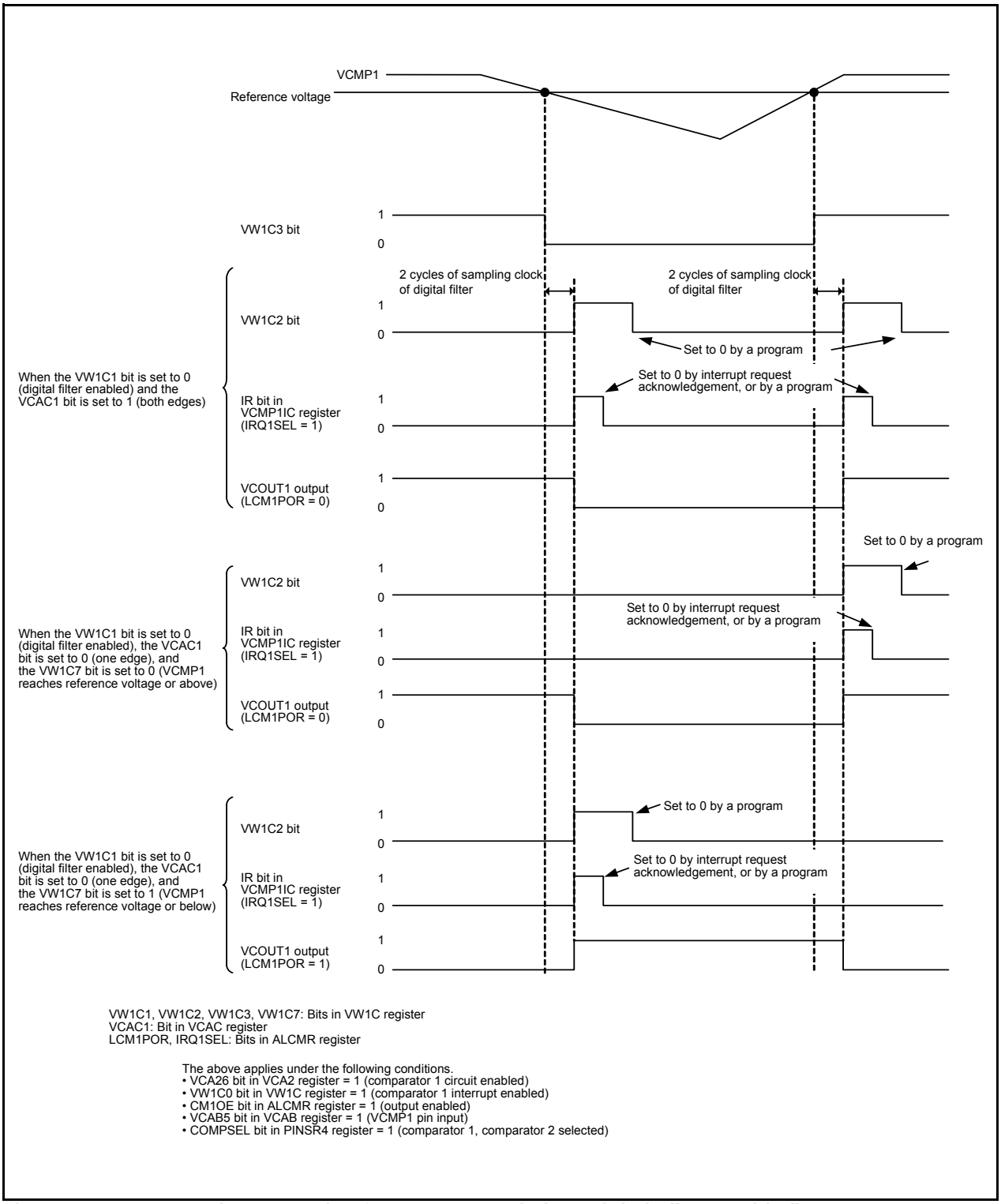


Figure 7.12 Operating Example of Comparator 1 (When Digital Filter Enabled)

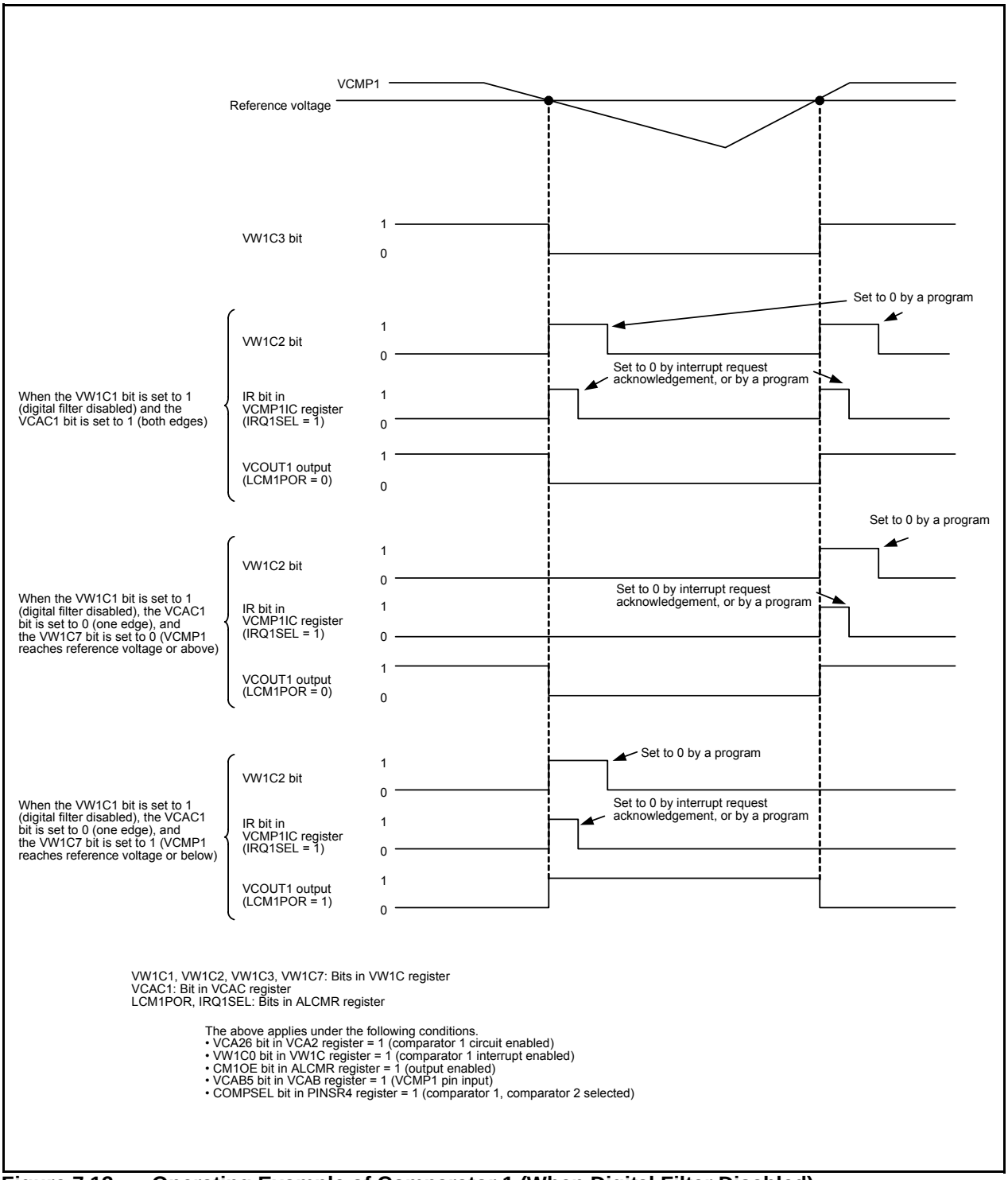


Figure 7.13 Operating Example of Comparator 1 (When Digital Filter Disabled)

7.4.2 Comparator 2

Table 7.4 lists the Procedure for Setting Bits Associated with Comparator 2 Interrupt, Figure 7.14 shows an Operating Example of Comparator 2 (When Digital Filter Enabled), and Figure 7.15 shows an Operating Example of Comparator 2 (When Digital Filter Disabled).

Table 7.4 Procedure for Setting Bits Associated with Comparator 2 Interrupt

Step	When Using Digital Filter	When Not Using Digital Filter
1	Set the COMPSEL bit in the PINSR4 register to 1 (comparator 1, comparator 2)	
2	Set the VCAB6 bit in the VCAB register to 1 (VCMP2 pin input voltage)	
3	Set the VCA27 bit in the VCA2 register to 1 (comparator 2 circuit enabled)	
4	Wait for td(E-A)	
5	Select the interrupt type by the IRQ2SEL bit in the ALCMR register	
6	Select the sampling clock by bits VW2F0 and VW2F1 in the VW2C register	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled)
7(1)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled)	–
8	Select the interrupt request timing by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register	
9	Set the VW2C2 bit in the VW2C register to 0	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	–
11	Wait for 2 cycles of the sampling clock of the digital filter.	– (No wait time required)
12	Set the VW2C0 bit in the VW2C register to 1 (comparator 2 interrupt enabled)	

NOTE:
1. When the VW2C0 bit is set to 0, steps 6 and 7 can be executed at the same time (with one instruction).

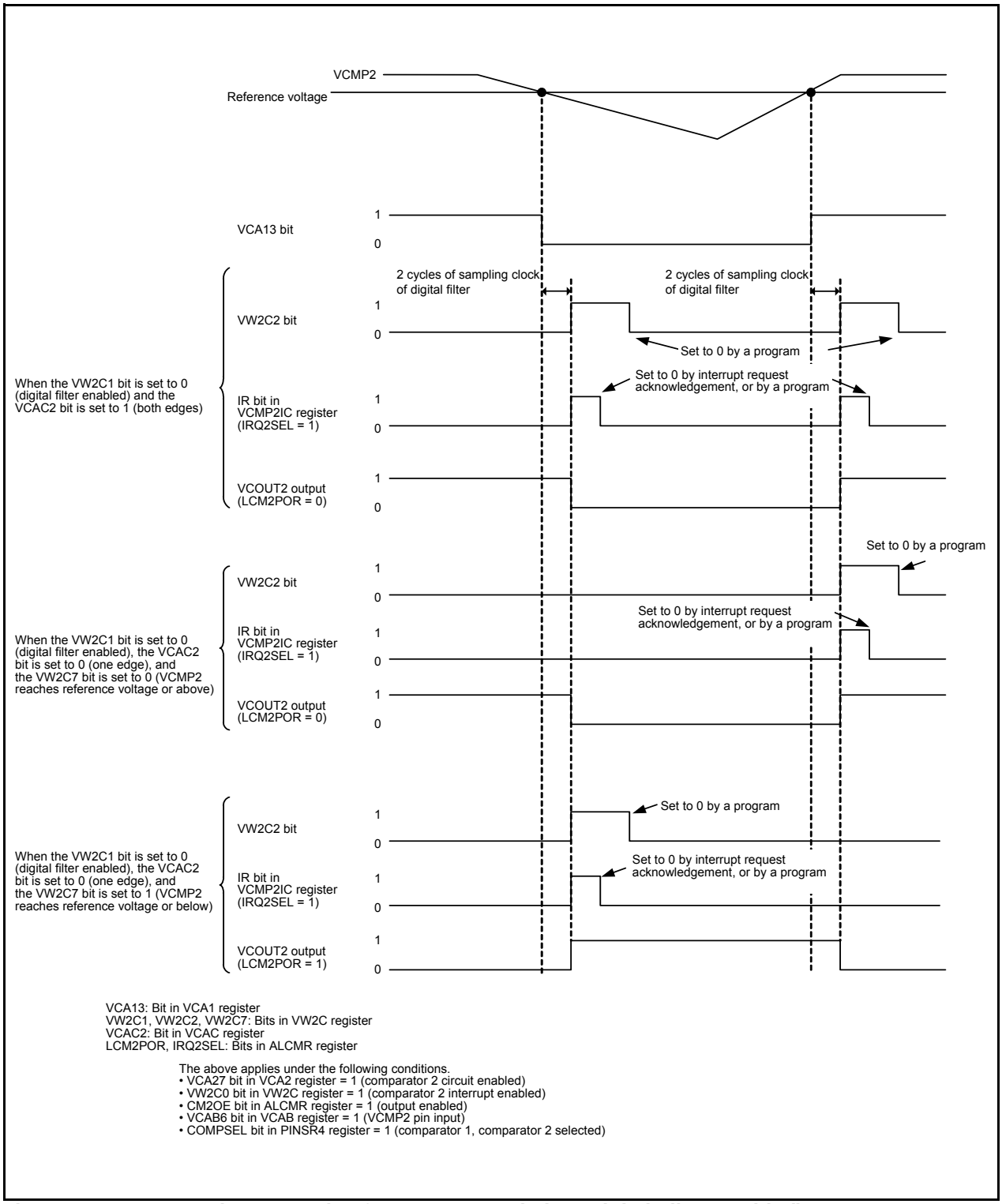


Figure 7.14 Operating Example of Comparator 2 (When Digital Filter Enabled)

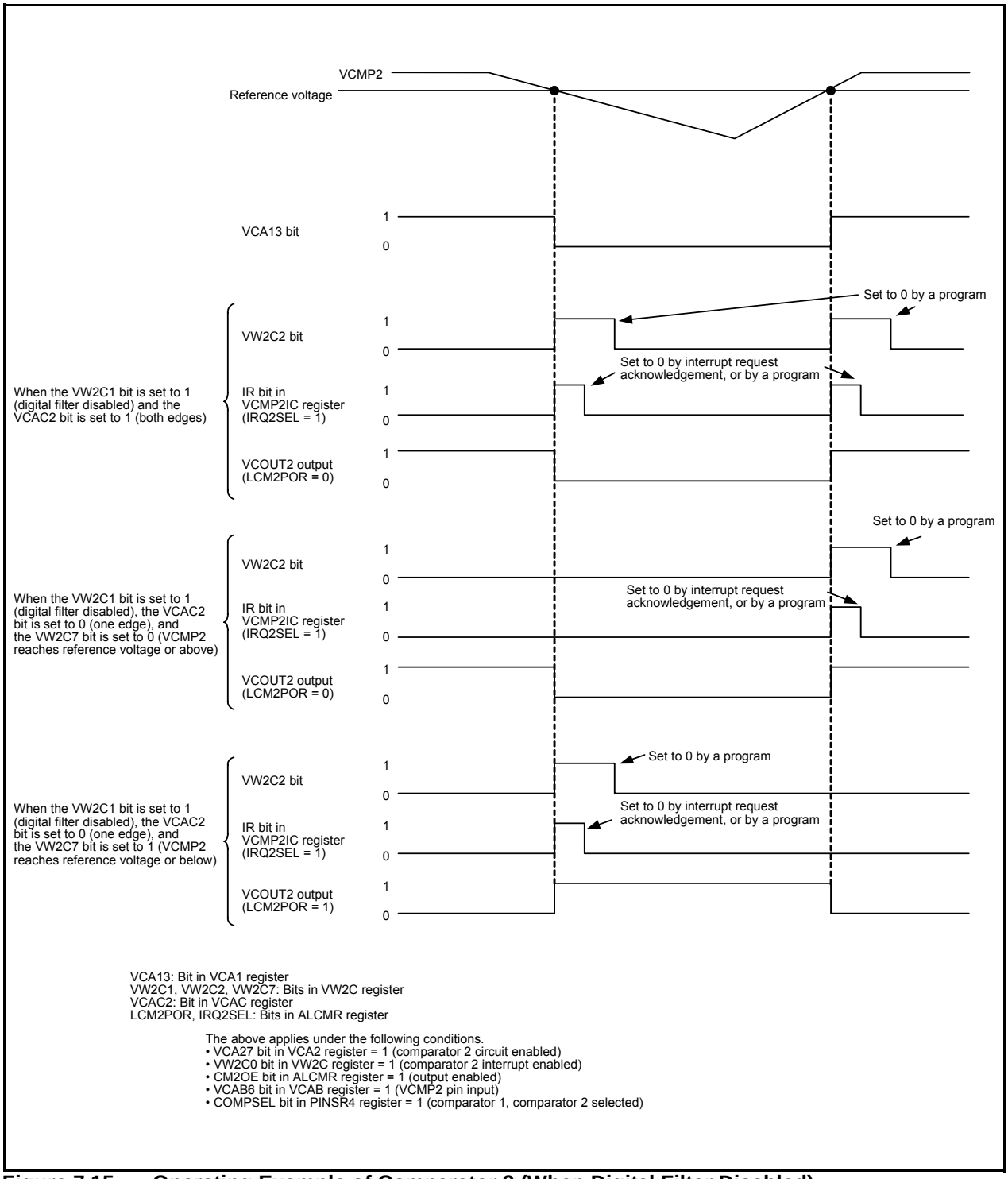


Figure 7.15 Operating Example of Comparator 2 (When Digital Filter Disabled)

7.5 Comparator 1 and Comparator 2 Interrupts

Two interrupt requests are generated, one each for comparator 1 and comparator 2. Non-maskable or maskable can be selected for each interrupt type. Refer to **13. Interrupts** for interrupts.

7.5.1 Non-Maskable Interrupts

When IRQiSEL (i = 1 or 2) bit in the ALCMR register is set to 0, the comparator i interrupt functions as a non-maskable interrupt. When the selected interrupt request timing occurs, the VWiC2 bit in the VWiC register is set to 1. At this time, a non-maskable interrupt request for comparator i is generated.

7.5.2 Maskable Interrupts

When the IRQiSEL (i = 1 or 2) bit in the ALCMR register is set to 1, the comparator i interrupt functions as a maskable interrupt. The comparator i interrupt uses the single VCMPiIC register (bits IR and ILVL0 to ILVL2) and a single vector. When the selected interrupt request timing occurs, the VWiC2 bit in the VWiC register is set to 1. At this time, the IR bit in the VCMPiIC register is set to 1 (interrupt requested).
Refer to **13.1.6 Interrupt Control** for the VCMPiIC register and **13.1.5.2 Relocatable Vector Tables** for interrupt vectors.

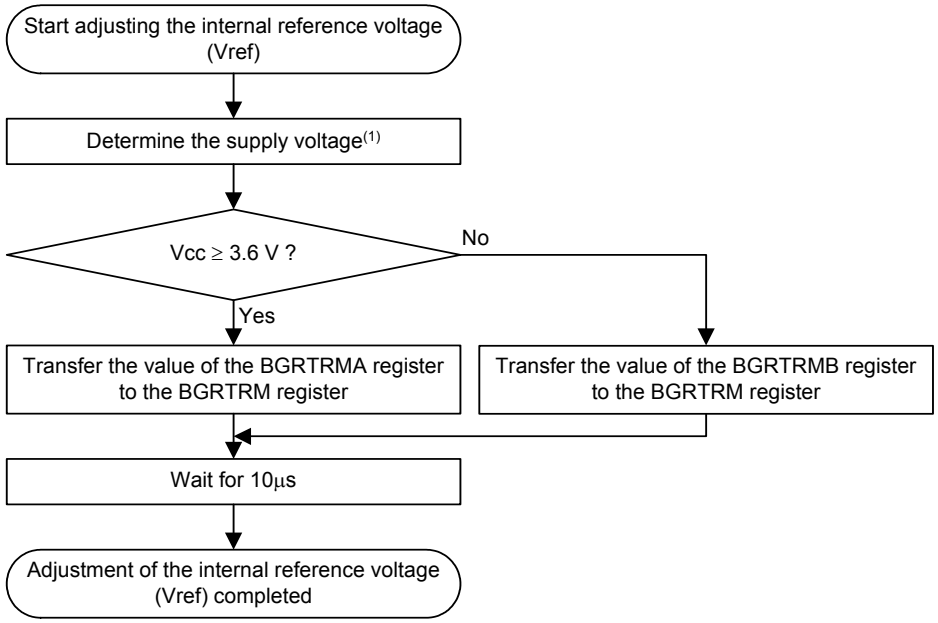
7.6 Adjusting Internal Reference Voltage (Vref)

The level of the internal reference voltage (Vref) can be adjusted with the value of the BGRTRM register. The values for correcting the Vref are stored in registers BGRTRMA and BGRTRMB before shipping the MCU. The value of the BGRTRMA register is the same as that of the BGRTRM register after reset.

To use separate correction values to match the supply voltage ranges, transfer them from registers BGRTRMA and BGRTRMB to the BGRTRM register. Figure 7.16 shows the Procedure for Adjusting Internal Reference Voltage (Vref).

When the BGRCR0 bit in the BGRCR register to 1 (disabled), the internal reference voltage (Vref) adjustment circuit (BGR trimming circuit) is disabled and the value of the BGRTRM register is also disabled.

When the BGR trimming circuit is disabled, the accuracy of the internal reference voltage (Vref) is not guaranteed. Disable voltage detection circuits 0 to 2 and disable comparators 1 and 2 with the internal reference voltage selected. The high-speed on-chip oscillator should also be stopped as necessary because the precision of its oscillation frequency is not also guaranteed.



NOTE:
1. The supple voltage can be determined by reading the monitor flag (VCA13 bit in VCA1 register) for voltage detection 2. Figure 7.17 shows an Example of Adjusting Internal Reference Voltage (Vref) (Voltage Detection 2 Used for Determining Supply Voltage).

Figure 7.16 Procedure for Adjusting Internal Reference Voltage (Vref)

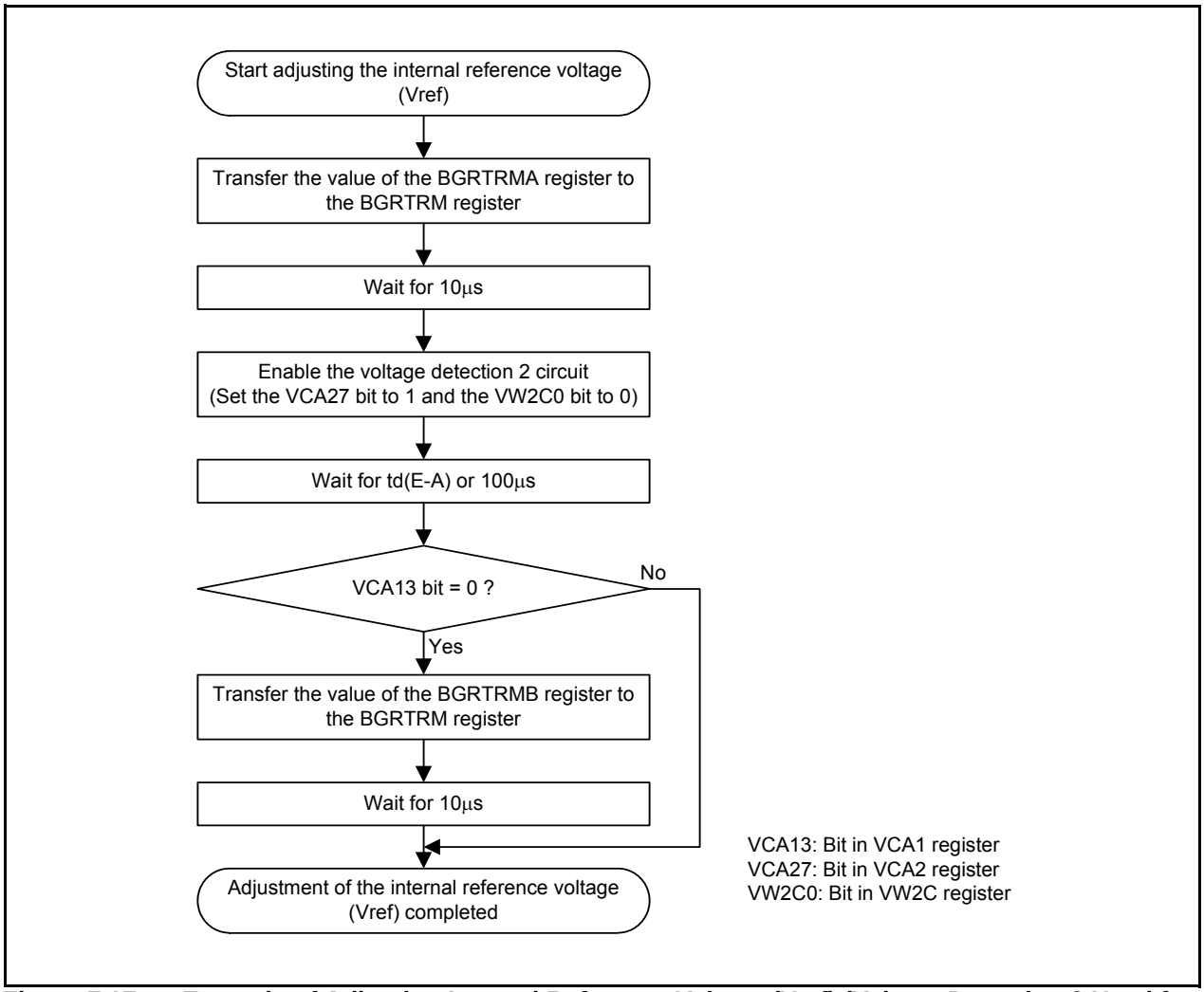


Figure 7.17 Example of Adjusting Internal Reference Voltage (Vref) (Voltage Detection 2 Used for Determining Supply Voltage)

8. I/O Ports

There are 15 input/output (I/O) ports P1, P3_3, P3_7, P4_3, P4_5, and P6_3 to P6_5 in the R8C/2H Group.
When the XCIN clock oscillation circuit is not used, P4_3 can be used as an I/O port and P4_4 can be used as an output port.
Table 8.1 lists an Overview of I/O Ports for R8C/2H Group.

Table 8.1 Overview of I/O Ports for R8C/2H Group

Ports	I/O	Type of Output	I/O Setting	Internal Pull-Up Resister
P1	I/O	CMOS3 State	Set per bit	Set every 4 bits(1)
P3_3, P3_7	I/O	CMOS3 State	Set per bit	Set every bit(1)
P4_3	I/O	CMOS3 State	Set per bit	Set every bit(2)
P4_4	Output	CMOS3 State	Set per bit(3)	None
P4_5	I/O	CMOS3 State	Set per bit	Set every bit(2)
P6_3	I/O	CMOS3 State	Set per bit	Set every bit(2)
P6_4, P6_5	I/O	CMOS3 State	Set per bit	Set every 2 bits(2)

NOTES:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by PUR0 register.
2. In input mode, whether an internal pull-up resistor is connected or not can be selected by PUR1 register.
3. Do not use port P4_4 as an input port (input mode).

There are 12 input/output (I/O) ports P1, P3_3, P3_7, P4_5, and P6_5 in the R8C/2J Group.
Table 8.2 lists an Overview of I/O Ports for R8C/2H Group.

Table 8.2 Overview of I/O Ports for R8C/2J Group

Ports	I/O	Type of Output	I/O Setting	Internal Pull-Up Resister
P1	I/O	CMOS3 State	Set per bit	Set every 4 bits(1)
P3_3, P3_7	I/O	CMOS3 State	Set per bit	Set every bit(1)
P4_5	I/O	CMOS3 State	Set per bit	Set every bit(2)
P6_5	I/O	CMOS3 State	Set per bit	Set every bit(2)

NOTES:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by PUR0 register.
2. In input mode, whether an internal pull-up resistor is connected or not can be selected by PUR1 register.

8.1 Functions of I/O Ports

The PDi_j (j = 0 to 7) bit in the PDi (i = 1, 3, 4, 6) register controls I/O of the following: Ports P1, P3_3, P3_7, P4_3, P4_5, P6_3 to P6_5 in the R8C/2H Group and ports P1, P3_3, P3_7, P4_5, and P6_5 in the R8C/2J Group. The Pi register consists of a port latch to hold output data and a circuit to read pin states.
Figures 8.1 to 8.3 show the Configurations of I/O Ports. Table 8.3 lists the Functions of I/O Ports. Also, Figure 8.5 shows the PDi (i = 1, 3, 4, or 6) Register (R8C/2H Group). Figure 8.6 shows the Pi (i = 1, 3, 4, or 6) Register (R8C/2H Group), Figure 8.7 shows the PDi (i = 1, 3, 4, or 6) Register (R8C/2J Group), Figure 8.8 shows the Pi (i = 1, 3, 4, or 6) Register (R8C/2J Group), Figure 8.9 shows Registers PINSR2 and PINSR4, Figure 8.10 shows the PMR Register, Figure 8.11 shows Registers PUR0 and PUR1.

Table 8.3 Functions of I/O Ports

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register(1)	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Reading	Read pin input level	Read the port latch
Writing	Write to the port latch	Write to the port latch. The value written to the port latch is output from the pin.

i = 1, 3, 4, 6, j = 0 to 7
NOTE:
1. In the R8C/2H Group, nothing is assigned to bits PD4_0 to PD4_2, PD4_6, PD4_7, PD6_1, PD6_2, and PD6_7. Bits PD3_0 to PD3_2, PD3_4 to PD3_6, PD6_0, and PD6_6 are reserved.
In the R8C/2J Group, nothing is assigned to bits PD4_0 to PD4_2, PD4_6, PD4_7, PD6_1, PD6_2, and PD6_7. Bits PD3_0 to PD3_2, PD3_4 to PD3_6, PD4_3, PD4_4, PD6_0, PD6_3, PD6_4, and PD6_6 are reserved.

8.2 Effect on Peripheral Functions

I/O ports function as I/O ports for peripheral functions (refer to **Table 1.5 Pin Name Information by Pin Number of R8C/2H Group** and **Table 1.6 Pin Name Information by Pin Number of R8C/2J Group**).
Table 8.4 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 1, 3, 4, 6, j = 0 to 7). Refer to the description of each function for information on how to set peripheral functions.

Table 8.4 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 1, 3, 4, 6, j = 0 to 7)

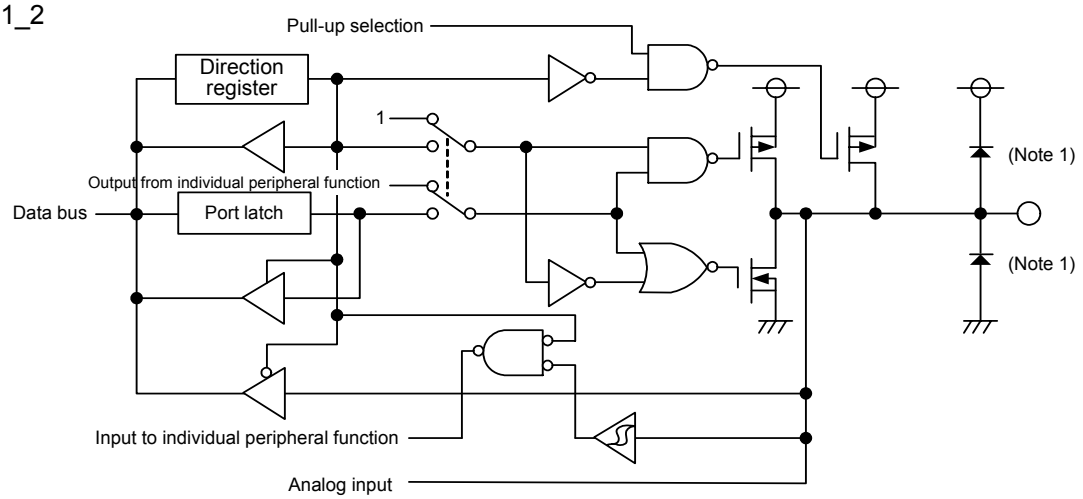
I/O of Peripheral Functions	PDi_j Bit Settings for Shared Pin Functions(1)
Input	Set this bit to 0 (input mode).
Output	This bit can be set to either 0 or 1 (output regardless of the port setting)

NOTE:
1. In the R8C/2H Group, nothing is assigned to bits PD4_0 to PD4_2, PD4_6, PD4_7, PD6_1, PD6_2, and PD6_7. Bits PD3_0 to PD3_2, PD3_4 to PD3_6, PD6_0, and PD6_6 are reserved.
In the R8C/2J Group, nothing is assigned to bits PD4_0 to PD4_2, PD4_6, PD4_7, PD6_1, PD6_2, and PD6_7. Bits PD3_0 to PD3_2, PD3_4 to PD3_6, PD4_3, PD4_4, PD6_0, PD6_3, PD6_4, and PD6_6 are reserved.

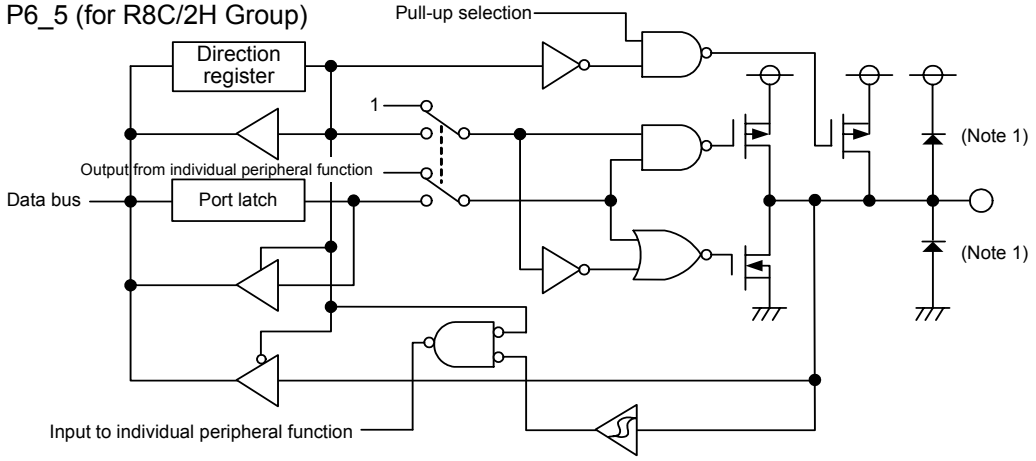
8.3 Pins Other than Programmable I/O Ports

Figure 8.4 shows the Configuration of I/O Pins.

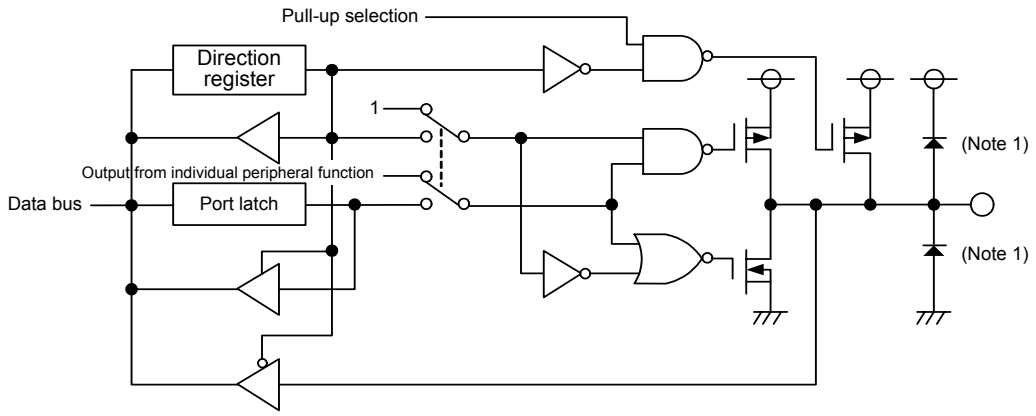
P1_0 to P1_2



P1_3, P1_6,
P3_3, and P6_5 (for R8C/2H Group)



P1_4, P3_7, and P6_3 (for the R8C/2H Group only)



NOTE:
1. ⊣◀ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

Figure 8.1 Configuration of I/O Ports (1)

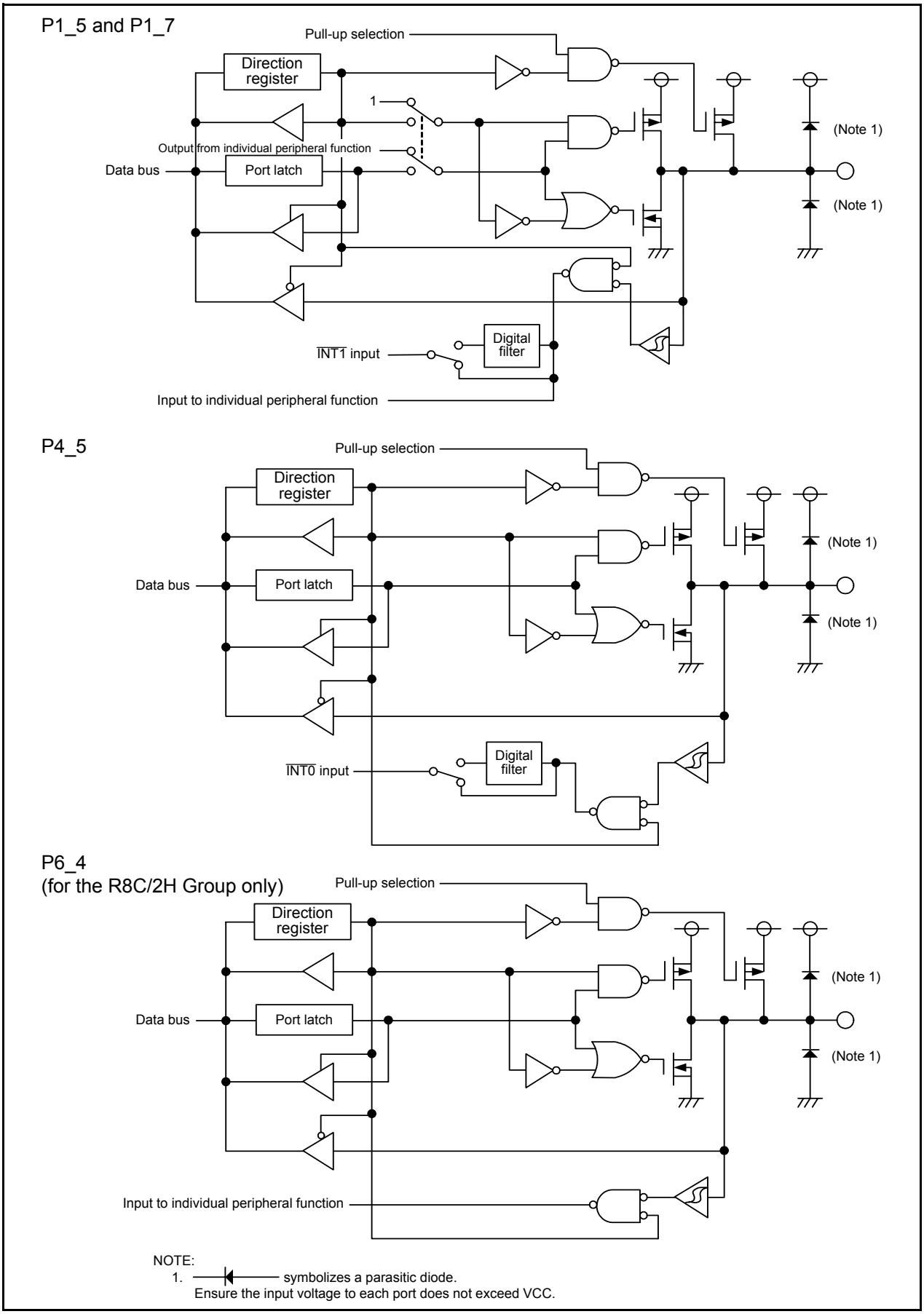


Figure 8.2 Configuration of I/O Ports (2)

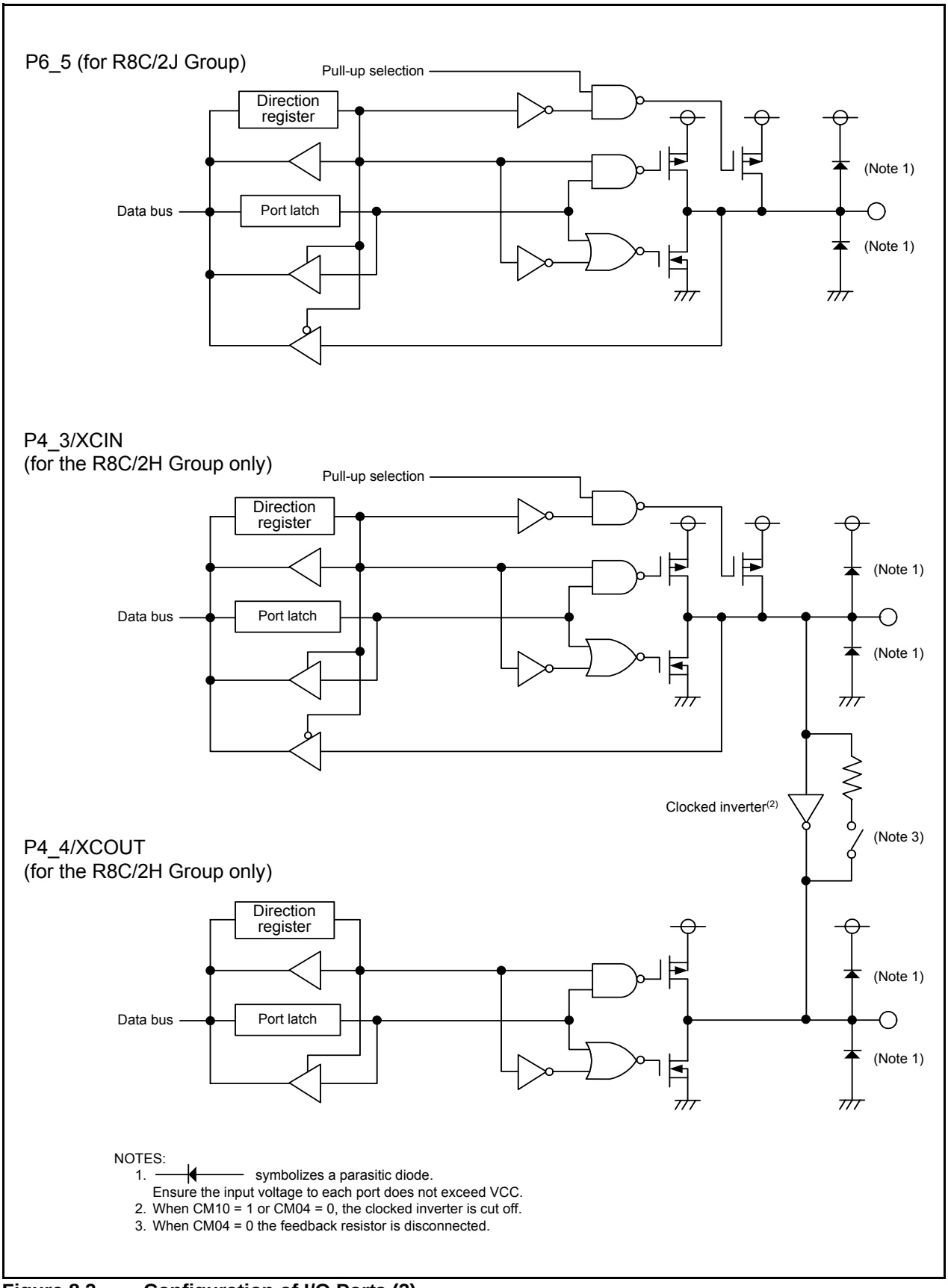


Figure 8.3 Configuration of I/O Ports (3)

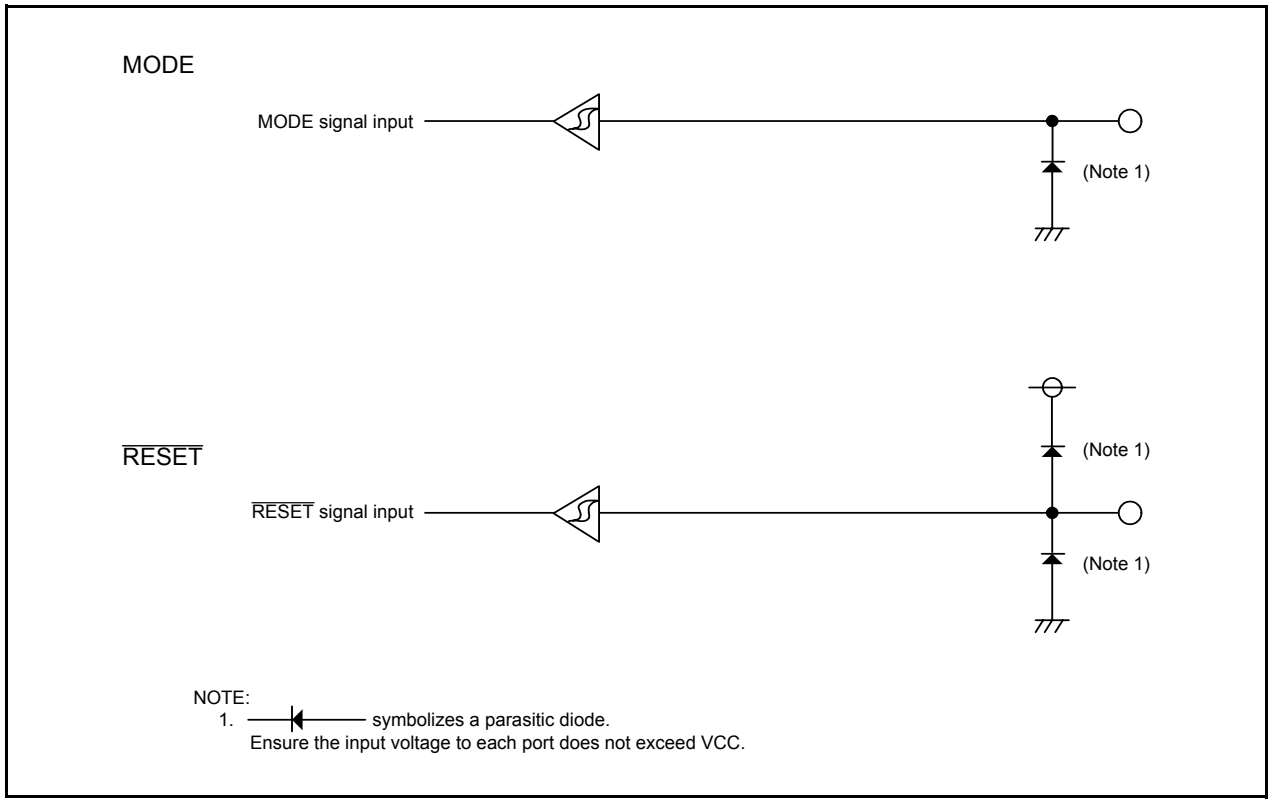
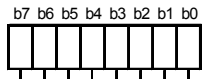


Figure 8.4 Configuration of I/O Pins

Port Pi Direction Register (i = 1, 3, 4, or 6)[1, 2, 3] (R8C/2H Group)



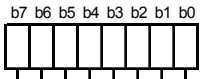
Symbol	Address	After Reset
PD1	00E3h	00h
PD3	00E7h	00h
PD4	00EAh	00h
PD6	00EEh	00h

Bit Symbol	Bit Name	Function	RW
PDi_0	Port Pi_0 direction bit	0 : Input mode (functions as an input port) 1 : Output mode (functions as an output port)	RW
PDi_1	Port Pi_1 direction bit		RW
PDi_2	Port Pi_2 direction bit		RW
PDi_3	Port Pi_3 direction bit		RW
PDi_4	Port Pi_4 direction bit		RW
PDi_5	Port Pi_5 direction bit		RW
PDi_6	Port Pi_6 direction bit		RW
PDi_7	Port Pi_7 direction bit		RW

NOTES:
1. Bits PD3_0 to PD3_2 and PD3_4 to PD3_6 in the PD3 register are reserved. Set to 0.
2. Bits PD4_0 to PD4_2, PD4_6, and PD4_7 in the PD4 register are unavailable on this MCU.
   If it is necessary to set bits PD4_0 to PD4_2, PD4_6, and PD4_7, set to 0 (input mode). When read, the content is 0.
   To use port P4_4 as an output port, set the PD4_4 bit to 1 (output mode). Do not use port P4_4 as an input port.
3. Bits PD6_1, PD6_2, and PD6_7 in the PD6 register are unavailable on this MCU.
   If it is necessary to set bits PD6_1, PD6_2, and PD6_7, set to 0 (input mode). When read, the content is 0.
   Bits PD6_0 and PD6_6 are reserved. Set to 0.

Figure 8.5 PDi (i = 1, 3, 4, or 6) Register (R8C/2H Group)

Port Pi Register (i = 1, 3, 4, or 6)[1, 2, 3] (R8C/2H Group)



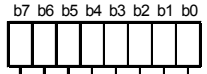
Symbol	Address	After Reset
P1	00E1h	00h
P3	00E5h	00h
P4	00E8h	00h
P6	00ECh	00h

Bit Symbol	Bit Name	Function	RW
Pi_0	Port Pi_0 bit	The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register. 0 : "L" level 1 : "H" level	RW
Pi_1	Port Pi_1 bit		RW
Pi_2	Port Pi_2 bit		RW
Pi_3	Port Pi_3 bit		RW
Pi_4	Port Pi_4 bit		RW
Pi_5	Port Pi_5 bit		RW
Pi_6	Port Pi_6 bit		RW
Pi_7	Port Pi_7 bit		RW

NOTES:
1. Bits P3_0 to P3_2 and P3_4 to P3_6 in the P3 register are reserved. Set to 0.
2. Bits P4_0 to P4_2, P4_6, and P4_7 in the P4 register are unavailable on this MCU.
   If it is necessary to set bits P4_0 to P4_2, P4_6, and P4_7, set to 0 ("L" level). When read, the content is 0.
3. Bits P6_1, P6_2, and P6_7 in the P6 register are unavailable on this MCU.
   If it is necessary to set bits P6_1, P6_2, and P6_7, set to 0 ("L" level). When read, the content is 0.
   Bits P6_0 and P6_6 are reserved. Set to 0.

Figure 8.6 Pi (i = 1, 3, 4, or 6) Register (R8C/2H Group)

Port Pi Direction Register (i = 1, 3, 4, or 6)(1, 2, 3) (R8C/2J Group)



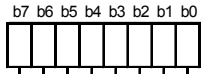
Symbol	Address	After Reset
PD1	00E3h	00h
PD3	00E7h	00h
PD4	00EAh	00h
PD6	00EEh	00h

Bit Symbol	Bit Name	Function	RW
PDi_0	Port Pi_0 direction bit	0 : Input mode (functions as an input port) 1 : Output mode (functions as an output port)	RW
PDi_1	Port Pi_1 direction bit		RW
PDi_2	Port Pi_2 direction bit		RW
PDi_3	Port Pi_3 direction bit		RW
PDi_4	Port Pi_4 direction bit		RW
PDi_5	Port Pi_5 direction bit		RW
PDi_6	Port Pi_6 direction bit		RW
PDi_7	Port Pi_7 direction bit		RW

NOTES:
1. Bits PD3_0 to PD3_2 and PD3_4 to PD3_6 in the PD3 register are reserved. Set to 0.
2. Bits PD4_0 to PD4_2, PD4_6, and PD4_7 in the PD4 register are unavailable on this MCU.
   If it is necessary to set bits PD4_0 to PD4_2, PD4_6, and PD4_7, set to 0 (input mode). When read, the content is 0.
   Bits PD4_3 and PD4_4 are reserved. Set to 0.
3. Bits PD6_1, PD6_2, and PD6_7 in the PD6 register are unavailable on this MCU.
   If it is necessary to set bits PD6_1, PD6_2, and PD6_7, set to 0 (input mode). When read, the content is 0.
   Bits PD6_0, PD6_3, PD6_4, and PD6_6 are reserved. Set to 0.

Figure 8.7 PDi (i = 1, 3, 4, or 6) Register (R8C/2J Group)

Port Pi Register (i = 1, 3, 4, or 6)(1, 2, 3) (R8C/2J Group)



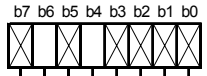
Symbol	Address	After Reset
P1	00E1h	00h
P3	00E5h	00h
P4	00E8h	00h
P6	00ECh	00h

Bit Symbol	Bit Name	Function	RW
Pi_0	Port Pi_0 bit	The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register. 0 : "L" level 1 : "H" level	RW
Pi_1	Port Pi_1 bit		RW
Pi_2	Port Pi_2 bit		RW
Pi_3	Port Pi_3 bit		RW
Pi_4	Port Pi_4 bit		RW
Pi_5	Port Pi_5 bit		RW
Pi_6	Port Pi_6 bit		RW
Pi_7	Port Pi_7 bit		RW

NOTES:
1. Bits P3_0 to P3_2 and P3_4 to P3_6 in the P3 register are reserved. Set to 0.
2. Bits P4_0 to P4_2, P4_6, and P4_7 in the P4 register are unavailable on this MCU.
   If it is necessary to set bits P4_0 to P4_2, P4_6, and P4_7, set to 0 ("L" level). When read, the content is 0.
   Bits P4_3 and P4_4 are reserved. Set to 0.
3. Bits P6_1, P6_2, and P6_7 in the P6 register are unavailable on this MCU.
   If it is necessary to set bits P6_1, P6_2, and P6_7, set to 0 ("L" level). When read, the content is 0.
   Bits P6_0, P6_3, P6_4, and P6_6 are reserved. Set to 0.

Figure 8.8 Pi (i = 1, 3, 4, or 6) Register (R8C/2J Group)

Pin Select Register 2

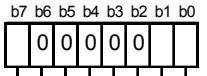


Symbol	Address	After Reset
PINSR2	00F6h	00h

Bit Symbol	Bit Name	Function	RW
— (b3-b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TRAOSEL	TRAO pin select bit(1)	0 : Disabled 1 : Enabled	RW
— (b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TRBOSEL	TRBO pin select bit(2)	0 : Disabled 1 : Enabled	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Set the TRAOSEL bit to 1 (enabled) before using timer RA.
2. Set the TRBOSEL bit to 1 (enabled) before using timer RB.

Pin Select Register 4 (R8C/2H Group)

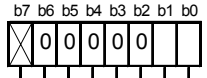


Symbol	Address	After Reset
PINSR4	02FBh	00h

Bit Symbol	Bit Name	Function	RW
TRFOSEL	TRFO11 pin select bit(1)	0 : Disabled 1 : Enabled	RW
COMPSEL	Voltage monitor/comparator select bit	0 : Voltage monitor 1, voltage monitor 2 1 : Comparator 1, comparator 2	RW
— (b6-b2)	Reserved bits	Set to 0.	RW
TREOSEL2	TREO pin select 2 bit(2)	0 : Disabled 1 : Enabled	RW

NOTES:
1. Set the TRFOSEL bit to 1 (enabled) before using timer RF.
2. Set the TREOSEL2 bit to 1 (enabled) before using timer RE.

Pin Select Register 4 (R8C/2J Group)



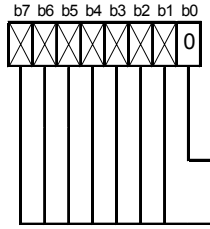
Symbol	Address	After Reset
PINSR4	02FBh	00h

Bit Symbol	Bit Name	Function	RW
TRFOSEL	TRFO11 pin select bit(1)	0 : Disabled 1 : Enabled	RW
COMPSEL	Voltage monitor/comparator select bit	0 : Voltage monitor 1, voltage monitor 2 1 : Comparator 1, comparator 2	RW
— (b6-b2)	Reserved bits	Set to 0.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Set the TRFOSEL bit to 1 (enabled) before using timer RF.

Figure 8.9 Registers PINSR2 and PINSR4

Port Mode Register



Symbol	Address	After Reset
PMR	00F8h	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	Set to 0.	RW
— (b7-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 8.10 PMR Register

Pull-Up Control Register 0

b7	b6	b5	b4	b3	b2	b1	b0
						0	

Symbol	Address	After Reset
PUR0	00FCh	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b1)	Reserved bit	Set to 0.	RW
PU02	P1_0 to P1_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU03	P1_4 to P1_7 pull-up(1)		RW
— (b5-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
PU06	P3_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU07	P3_7 pull-up(1)		RW

NOTE:
1. When this bit is set to 1 (pulled up), the pin w hose direction bit is set to 0 (input mode) is pulled up.

Pull-Up Control Register 1 (R8C/2H Group)

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
PUR1	00FDh	00h

Bit Symbol	Bit Name	Function	RW
PU10	P4_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU11	P4_5 pull-up(1)		RW
— (b3-b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
PU14	P6_3 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
PU15	P6_4, P6_5 pull-up(1)		RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When this bit is set to 1 (pulled up), the pin w hose direction bit is set to 0 (input mode) is pulled up.

Pull-Up Control Register 1 (R8C/2J Group)

b7	b6	b5	b4	b3	b2	b1	b0
			0				0

Symbol	Address	After Reset
PUR1	00FDh	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	Set to 0.	RW
PU11	P4_5 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
— (b3-b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b4)	Reserved bit	Set to 0.	RW
PU15	P6_5 pull-up(1)	0 : Not pulled up 1 : Pulled up	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When this bit is set to 1 (pulled up), the pin w hose direction bit is set to 0 (input mode) is pulled up.

Figure 8.11 Registers PUR0 and PUR1

8.4 Port Setting

Table 8.5 to Table 8.22 list the port setting.

Table 8.5 Port P1_0/$\overline{\text{KI0}}$/TRFO00/VCMP1

Register	PD1	TRFOUT	KIEN	VCAB	Function
Bit	PD1_0	TRFOUT0	KI0EN	VCAB5	
Setting value	0	0	0	0	Input port(1)
	1	0	0	0	Output port
	X	1	0	0	TRFO00 output
	0	0	1	0	$\overline{\text{KI0}}$ input(1, 2)
	0	0	0	1	VCMP1 input(1)

X: 0 or 1
NOTES:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Set bit 2 (reserved bit) in the PINSR4 register to 0.

Table 8.6 Port P1_1/$\overline{\text{KI1}}$/TRFO01/VCMP2

Register	PD1	TRFOUT	KIEN	VCAB	Function
Bit	PD1_1	TRFOUT1	KI1EN	VCAB6	
Setting value	0	0	0	0	Input port(1)
	1	0	0	0	Output port
	X	1	0	0	TRFO01 output
	0	0	1	0	$\overline{\text{KI1}}$ input(1, 2)
	0	0	0	1	VCMP2 input(1)

X: 0 or 1
NOTES:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Set bit 3 (reserved bit) in the PINSR4 register to 0.

Table 8.7 Port P1_2/$\overline{\text{KI2}}$/TRFO02/CVREF

Register	PD1	TRFOUT	KIEN	VCAB	Function
Bit	PD1_2	TRFOUT2	KI2EN	VCAB7	
Setting value	0	0	0	0	Input port(1)
	1	0	0	0	Output port
	X	1	0	0	TRFO02 output
	0	0	1	0	$\overline{\text{KI2}}$ input(1)
	0	0	0	1	CVREF input(1)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 8.8 Port P1_3/$\overline{KI3}$/VCOUT1/TRBO

Register	PD1	Timer RB Setting	KIEN	ALCMR	Function
Bit	PD1_3	–	KI3EN	CM1OE	
Setting value	0	Other than TRBO usage conditions	0	0	Input port(1)
	1	Other than TRBO usage conditions	0	0	Output port
	0	Other than TRBO usage conditions	1	0	$\overline{KI3}$ input(1)
	X	Refer to **Table 8.9 TRBO Pin Setting**	0	0	TRBO output
	X	Other than TRBO usage conditions	0	1	VCOUT1 output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 8.9 TRBO Pin Setting

Register	PINSR2	TRBIOC	TRBMR		Function
Bit	TRBOSEL	TOCNT(1)	TMOD1	TMOD0	
Setting value	1	0	0	1	Programmable waveform generation mode
	1	0	1	0	Programmable one-shot generation mode
	1	0	1	1	Programmable wait one-shot generation mode
	1	1	0	1	P1_3 output port
	Other than above				Other than TRBO usage conditions

NOTE:
1. Set the TOCNT bit in the TRBIOC register to 0 in modes except for programmable waveform generation mode.

Table 8.10 Port P1_4/TXD0

Register	PD1	U0MR			Function
Bit	PD1_4	SMD2	SMD1	SMD0	
Setting value	0	0	0	0	Input port(1)
	1	0	0	0	Output port
	X	0	0	1	TXD0 output(2)
		1		0	
				1	
			1	0	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. N-channel open-drain output by setting the NCH bit in the U0C0 register to 1.

Table 8.11 Port P1_5/RXD0/(TRAIO)/($\overline{\text{INT1}}$)

Register	PD1	TRAIOC		TRAMR			INTEN	Function
Bit	PD1_5	TIOSEL	TOPCR(3)	TMOD2	TMOD1	TMOD0	INT1EN	
Setting value	0	0	X	X	X	X	0	Input port(1)
		1	1	0	0	1		
			0			0		
	1	0	X	X	X	X	0	Output port
		1	0	0	0	0		
	0	0	X	X	X	X	0	RXD0 input(1)
		1	0	Other than 001b				
	0	1	0	0	0	0	1	$\overline{\text{INT1}}$ input(1, 2)
			1			1		
	0	1	0	Other than 000b, 001b			X	TRAIO input(1)
	0	1	0	Other than 000b, 001b			1	TRAIO input/$\overline{\text{INT1}}$ input(1, 2)
	X	1	0	0	0	1	X	TRAIO output

X: 0 or 1

NOTES:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Set bit 0 (reserved bit) in the PMR register to 0.
3. Set the TOPCR bit in the TRAIOC register to 0 in modes except for pulse output mode.

Table 8.12 Port P1_6/CLK0/VCOUT2

Register	PD1	ALCMR	U0MR				Function
Bit	PD1_6	CM2OE	CKDIR	SMD2	SMD1	SMD0	
Setting value	0	0	0	Other than 001b			Input port(1)
			1	X	X	X	
	1	0	X	Other than 001b			Output port
	X	0	0	0	0	1	CLK0 output
	0	0	1	X	X	X	CLK0 input(1)
	X	1	X	X	X	X	VCOUT2 output

X: 0 or 1

NOTE:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 8.13 Port P1_7/TRAIO/$\overline{\text{INT1}}$

Register	PD1	TRAIOC		TRAMR			INTEN	Function
Bit	PD1_7	TIOSEL	TOPCR(3)	TMOD2	TMOD1	TMOD0	INT1EN	
Setting value	0	1	X	X	X	X	0	Input port(1)
		0	1	0	0	1		
			0			0		
	1	1	X	X	X	X	0	Output port
		0	0	0	0	0		
	0	0	0	0	0	0	1	$\overline{\text{INT1}}$ input(1, 2)
			1			1		
	0	0	0	Other than 000b, 001b			X	TRAIO input(1)
	0	0	0	Other than 000b, 001b			1	TRAIO input/$\overline{\text{INT1}}$ input(1, 2)
	X	0	0	0	0	1	X	TRAIO output

X: 0 or 1

NOTES:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Set bit 0 (reserved bit) in the PMR register to 0.
3. Set the TOPCR bit in the TRAIOC register to 0 in modes except for pulse output mode.

Table 8.14 Port P3_3/TRFO10/TRFI

Register	PD3	TRFOUT	Function
Bit	PD3_3	TRFOUT3	
Setting value	0	0	Input port(1)
	1	0	Output port
	X	1	TRFO10 output
	0	0	TRFI input(1)

X: 0 or 1
NOTE:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.

Table 8.15 Port P3_7/TRAO/TRFO11

Register	PD3	PINSR2	TRAIOC	PINSR4	TRFOUT	Function
Bit	PD3_7	TRAOSEL	TOENA	TRFOSEL	TRFOUT4	
Setting value	0	X	0	X	0	Input port(1)
	1	X	0	X	0	Output port
	X	1	1	X	0	TRAO output
	X	X	0	1	1	TRFO11 output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.

Table 8.16 Port P4_3/(XCIN) (for R8C/2H Group only)

Register	PD4	CM0	CM1		Circuit specifications		Function
Bit	PD4_3	CM04	CM10	CM12	Oscillation buffer	Feedback resistor	
Setting value	0	0	X	X	OFF	OFF	Input port(1, 2)
	1	0	X	X	OFF	OFF	Output port(2)
	X	1	0	0	ON	ON	XCIN clock oscillation (on-chip feedback resistor enabled)
	X	1	0	1	ON	OFF	XCIN clock oscillation (on-chip feedback resistor disabled)
	X	1	1	0	OFF	ON	XCIN clock oscillation stop
				1	OFF	OFF	
	X	1	0	0	ON	ON	External XCIN clock input
				1	ON	OFF	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU10 bit in the PUR1 register to 1.
2. Refer to **8.6.1 Port P4_3, P4_4 (for R8C/2H Group only).**

Table 8.17 Port P4_4/(XCOUT) (for R8C/2H Group only)

Register	PD4	CM0	CM1		Circuit specifications		Function
Bit	PD4_4	CM04	CM10	CM12	Oscillation buffer	Feedback resistor	
Setting value	1	0	X	X	OFF	OFF	Output port(1)
	X	1	0	0	ON	ON	XCIN clock oscillation (on-chip feedback resistor enabled)
	X	1	0	1	ON	OFF	XCIN clock oscillation (on-chip feedback resistor disabled)
	X	1	1	0	OFF	ON	XCIN clock oscillation stop
				1	OFF	OFF	
	X	1	0	0	ON	ON	External XCOUT clock output (inverted output of XCIN clock)
				1	ON	OFF	

X: 0 or 1
NOTE:
1. Refer to **8.6.1 Port P4_3, P4_4 (for R8C/2H Group only).**

Table 8.18 Port P4_5/$\overline{\text{INT0}}$

Register	PD4	INTEN	Function
Bit	PD4_5	INT0EN	
Setting value	0	0	Input port(1)
	1	0	Output port
	0	1	$\overline{\text{INT0}}$ input

NOTE:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.

Table 8.19 Port P6_3/TXD2 (for R8C/2H Group only)

Register	PD6	U2MR			Function
Bit	PD6_3	SMD2	SMD1	SMD0	
Setting value	0	0	0	0	Input port(1)
	1	0	0	0	Output port
	X	0	0	1	TXD2 output(2)
		1		0	
				1	
			1	0	

X: 0 or 1
NOTES:
1. Pulled up by setting the PU14 bit in the PUR1 register to 1.
2. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

Table 8.20 Port P6_4/RXD2 (for R8C/2H Group only)

Register	PD6	Function
Bit	PD6_4	
Setting value	0	Input port(1)
	1	Output port
	0	RXD2 input(1)

NOTE:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.

Table 8.21 Port P6_5/CLK2/TREO (for R8C/2H Group)

Register	PD6	PINSR4	TRECR1	U2MR				Function
Bit	PD6_5	TREOSEL2	TOENA	CKDIR	SMD2	SMD1	SMD0	
Setting value	0	0	X	0	Other than 001b			Input port(1)
				1	X	X	X	
	1	0	X	X	Other than 001b			Output port
	X	0	X	0	0	0	1	CLK2 output
	0	0	X	1	X	X	X	CLK2 input(1)
	X	1	1	X	X	X	X	TREO output

X: 0 or 1
NOTE:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.

Table 8.22 Port P6_5 (for R8C/2J Group)

Register	PD6	Function
Bit	PD6_5	
Setting value	0	Input port(1)
	1	Output port

NOTE:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.

8.5 Unassigned Pin Handling

Table 8.23 lists Unassigned Pin Handling.

Table 8.23 Unassigned Pin Handling

Pin Name	Connection
Ports P1, P3_3, P3_7, P4_3 to P4_5, P6_3 to P6_5 (4)	• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up).(2) • After setting to output mode, leave these pins open.(1, 2)
$\overline{\text{RESET}}$ (3)	Connect to VCC via a pull-up resistor(2)

NOTES:
1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When the power-on reset function is in use.
4. Ports P4_3, P4_4, P6_3, and P6_4 are not available in the R8C/2J Group. Leave NC pins open.

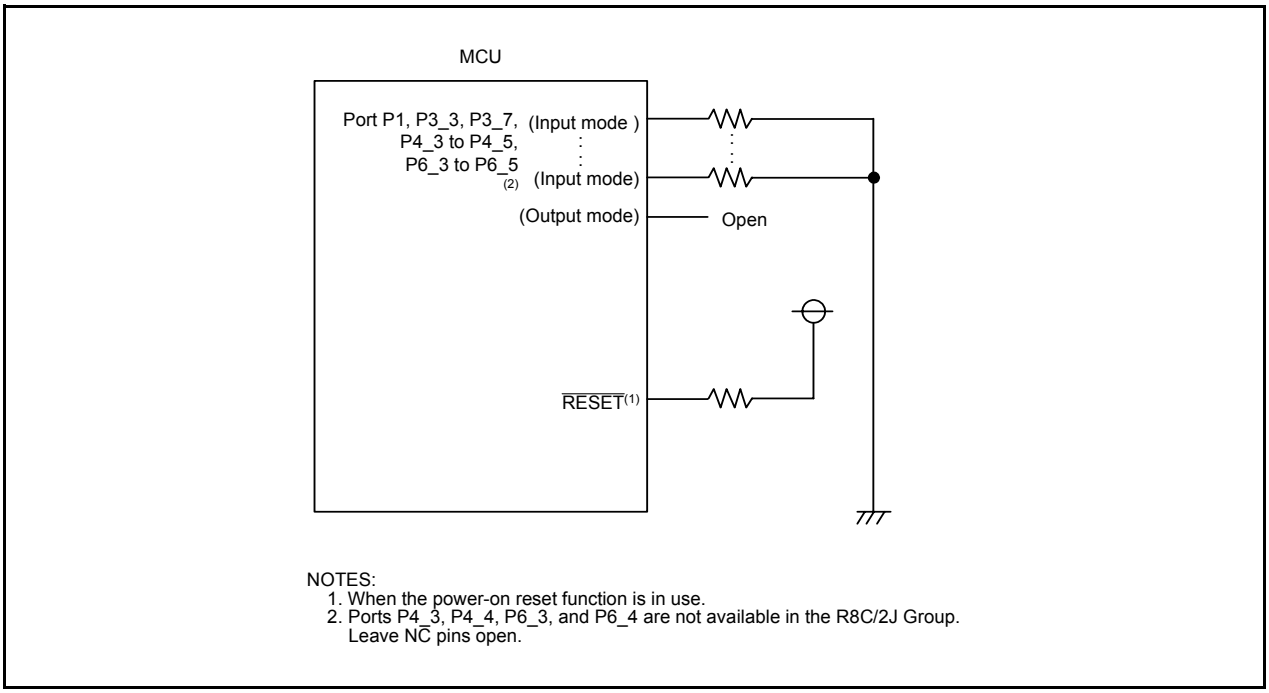


Figure 8.12 Unassigned Pin Handling

8.6 Notes on I/O Ports

8.6.1 Port P4_3, P4_4 (for R8C/2H Group only)

Ports P4_3 and P4_4 are also used as the XCIN function and the XCOUT function, respectively. During a reset period and after a reset release, these ports are set to the XCIN and XCOUT functions. Pins P4_3 and P4_4 can be switched to the port functions by setting the CM04 bit in the CM0 register to 0 (ports P4_3 and P4_4) by a program.

To use ports P4_3 and P4_4 as ports, note the following:

- Port P4_3

After a reset until the CM04 bit is set to 0 (ports P4_3 and P4_4) by a program, a typical 10 MΩ impedance is connected between the P4_3 pin and the MCU power supply or GND. If the XCIN is set to intermediate-level input or left floating, a shoot-through current flows into the oscillation driver.

- Port P4_4

Use port P4_4 as an output port by setting the PD4_4 bit in the PD4 register to 1 (output mode). After a reset until the CM04 bit is set to 0 (ports P4_3 and P4_4) by a program, the P4_4 pin may output an intermediate potential of about 2.0 V.

9. Processor Mode

9.1 Processor Modes

Single-chip mode can be selected as the processor mode.
Table 9.1 lists Features of Processor Mode. Figure 9.1 shows the PM0 Register and Figure 9.2 shows the PM1 Register.

Table 9.1 Features of Processor Mode

Processor Mode	Accessible Areas	Pins Assignable as I/O Port Pins
Single-chip mode	SFR, internal RAM, internal ROM	All pins are I/O ports or peripheral function I/O pins

Processor Mode Register 0(1)

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	0	0	0

Symbol: PM0 | Address: 0004h | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0.	RW
PM03	Software reset bit	The MCU is reset when this bit is set to 1. When read, the content is 0.	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Set the PRC1 bit in the PRCR register to 1 (write enable) before rewriting the PM0 register.

Figure 9.1 PM0 Register

Processor Mode Register 1(1)

b7	b6	b5	b4	b3	b2	b1	b0
0	X	X	X	X	X	0	0

Symbol: PM1 | Address: 0005h | After Reset: 00h

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Reserved bits	Set to 0.	RW
PM12	WDT interrupt/reset switch bit	0 : Watchdog timer interrupt 1 : Watchdog timer reset(2)	RW
— (b6-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b7)	Reserved bit	Set to 0.	RW

NOTES:
1. Set the PRC1 bit in the PRCR register to 1 (write enable) before rewriting the PM1 register.
2. The PM12 bit is set to 1 by a program (It remains unchanged even if 0 is written to it).
When the CSPRO bit in the CSPR register is set to 1 (count source protect mode enabled), the PM12 bit is automatically set to 1.

Figure 9.2 PM1 Register

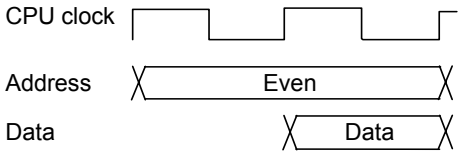
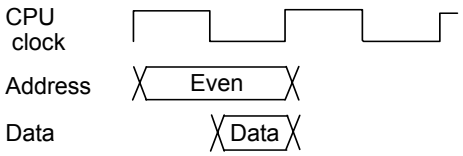
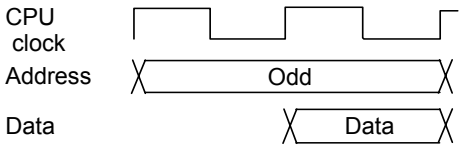
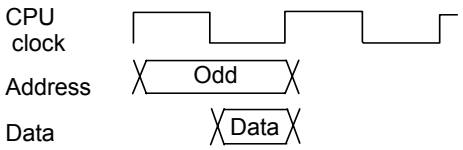
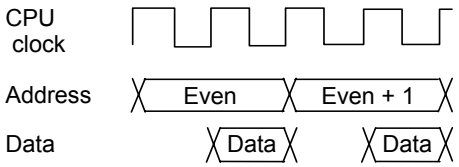
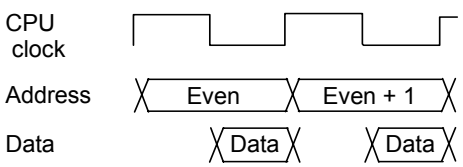
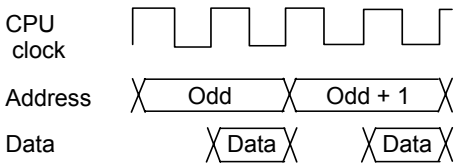
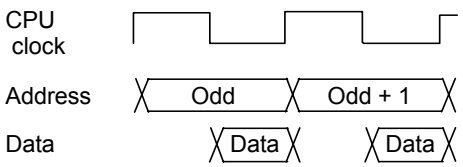
10. Bus

The bus cycles differ when accessing ROM/RAM, and when accessing SFR.
Table 10.1 lists Bus Cycles by Access Space.
ROM/RAM and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.
Table 10.2 lists Access Units and Bus Operations.

Table 10.1 Bus Cycles by Access Space

Access Area	Bus Cycle
SFR	2 cycles of CPU clock
ROM/RAM	1 cycle of CPU clock

Table 10.2 Access Units and Bus Operations

Area	SFR	ROM, RAM
Even address Byte access		
Odd address Byte access		
Even address Word access		
Odd address Word access		

11. Clock Generation Circuit

The clock generation circuit in the R8C/2H Group has:
- XCIN clock oscillation circuit
- Low-speed on-chip oscillator
- High-speed on-chip oscillator

The clock generation circuit in the R8C/2J Group has:
- Low-speed on-chip oscillator
- High-speed on-chip oscillator

Table 11.1 lists Specifications of Clock Generation Circuit for R8C/2H Group. Table 11.2 lists Specifications of Clock Generation Circuit for R8C/2J Group. Figure 11.1 shows a Clock Generation Circuit for R8C/2H Group. Figure 11.2 shows a Clock Generation Circuit for R8C/2J Group. Figures 11.3 to 11.11 show clock associated registers. Figure 11.12 shows a Handling Procedure of Internal Power Low Consumption Using VCA20 Bit.

> The XCIN clock oscillation circuit is not implemented in the R8C/2J Group.
> The description about the XCIN clock oscillation circuit in this chapter applies to the R8C/2H Group only.

Table 11.1 Specifications of Clock Generation Circuit for R8C/2H Group

Item	XCIN Clock Oscillation Circuit	On-Chip Oscillator	
		High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source
Clock frequency	32.768 kHz	Approx. 8 MHz	Approx. 125 kHz
Connectable oscillator	• Crystal oscillator	–	–
Oscillator connect pins	XCIN, XCOUT(1)	–(1)	–(1)
Oscillation stop, restart function	Usable	Usable	Usable
Oscillator status after reset	Oscillate	Stop	Oscillate
Others	• Externally generated clock can be input(2) • On-chip feedback resistor RfXCIN (connected/ not connected, selectable)	–	–

NOTES:
1. These pins can be used as P4_3 or P4_4 when using the on-chip oscillator clock as the CPU clock while the XCIN clock oscillation circuit is not used.
2. Set the CM04 bit in the CM0 register to 1 (XCIN-XCOUT pin) when an external clock is input.

Table 11.2 Specifications of Clock Generation Circuit for R8C/2J Group

Item	On-Chip Oscillator	
	High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source
Clock frequency	Approx. 8 MHz	Approx. 125 kHz
Oscillation stop, restart function	Usable	None
Oscillator status after reset	Stop	Oscillate

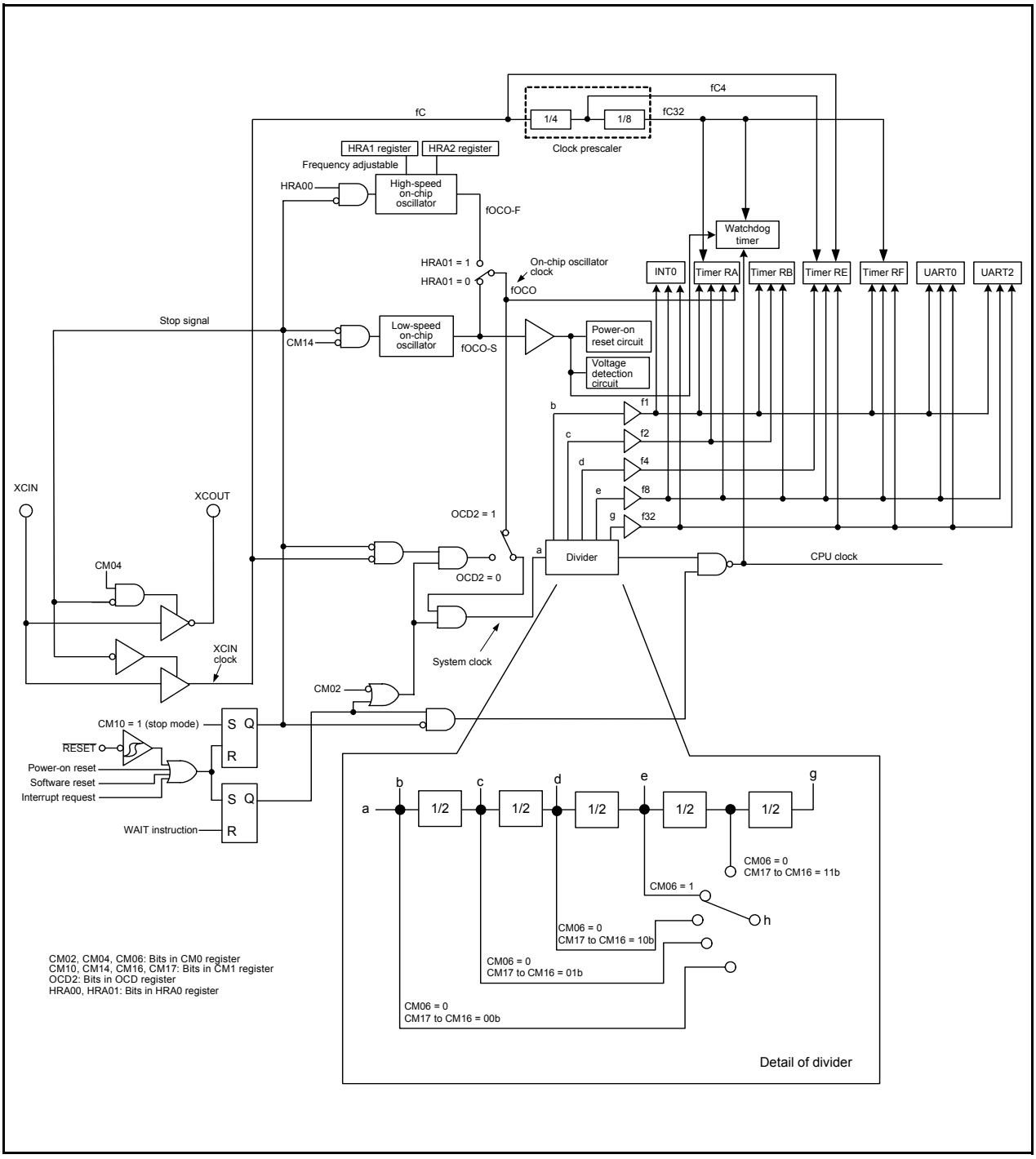


Figure 11.1 Clock Generation Circuit for R8C/2H Group

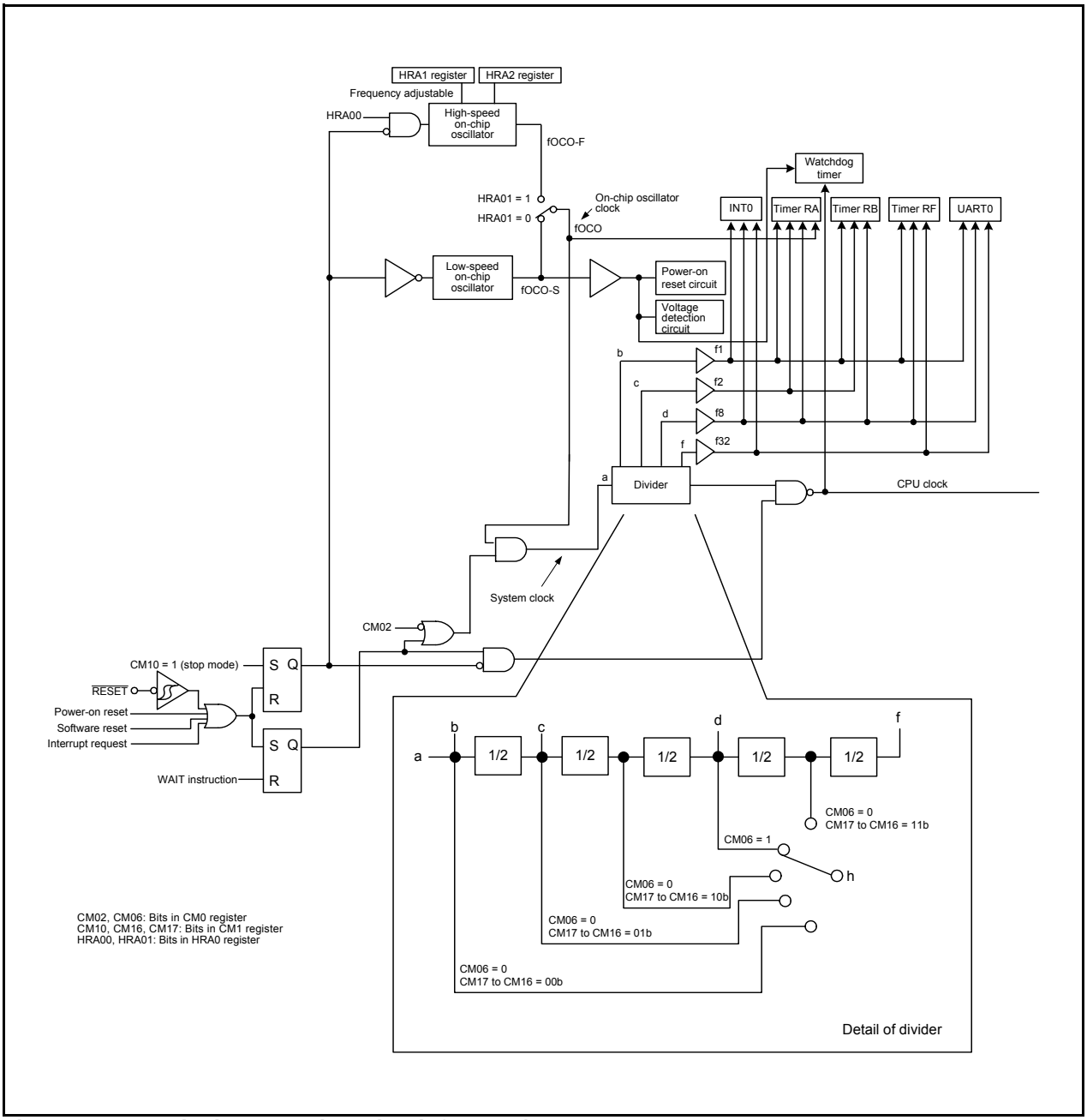


Figure 11.2 Clock Generation Circuit for R8C/2J Group

System Clock Control Register 0[1] (R8C/2H Group)

Symbol	Address	After Reset
CM0	0006h	01011000b

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b1)	Reserved bit	Set to 0.	RW
CM02	WAIT peripheral function clock stop bit	0 : Peripheral function clock does not stop in wait mode 1 : Peripheral function clock stops in wait mode	RW
CM03	XCIN-XCOUT drive capacity select bit[2]	0 : LOW 1 : HIGH	RW
CM04	Port, XCIN-XCOUT switch bit[3, 4]	0 : Ports P4_3, P4_4 1 : XCIN-XCOUT pin	RW
— (b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
CM06	System clock division select bit 0[5]	0 : CM16, CM17 enabled 1 : Divide-by-8 mode	RW
— (b7)	Reserved bit	Set to 0.	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the CM0 register.
2. When entering stop mode, the CM03 bit is set to 1 (HIGH). Rewrite the CM03 bit while the XCIN clock oscillation stabilizes.
3. P4_3 and P4_4 can be used as ports when the CM04 bit is set to 0 (ports P4_3 and P4_4).
   To use the XCIN clock, set the CM04 bit to 1 (XCIN-XCOUT pin). Also, set port P4_3 as input ports without pull-up.
4. If the CM10 bit in the CM1 register is set to 1 (stop mode), when the CM04 bit is set to 1 (XCIN-XCOUT pin), the XCIN(P4_3) pin is set to the high-impedance state and the XCOUT (P4_4) pin is set to “H”. When the CM04 bit is set to 0 (I/O ports P4_3 and P4_4), pins XCIN (P4_3) and XOUT (P4_4) retain the I/O status (status just before stop mode is entered).
5. When entering stop mode, the CM06 bit is set to 1 (divide-by-8 mode).

Figure 11.3 CM0 Register (R8C/2H Group)

System Clock Control Register 0[1] (R8C/2J Group)

b7	b6	b5	b4	b3	b2	b1	b0
0		X	0	1		0	X

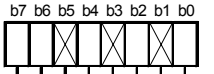
Symbol	Address	After Reset
CM0	0006h	01011000b

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b1)	Reserved bit	Set to 0.	RW
CM02	WAIT peripheral function clock stop bit	0 : Peripheral function clock does not stop in wait mode 1 : Peripheral function clock stops in wait mode	RW
— (b3)	Reserved bit	Set to 1.	RW
— (b4)	Reserved bit	Set to 0.[3]	RW
— (b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
CM06	System clock division select bit 0[2]	0 : CM16, CM17 enabled 1 : Divide-by-8 mode	RW
— (b7)	Reserved bit	Set to 0.	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the CM0 register.
2. When entering stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
3. The b4 bit is set to 1 after reset. Set this bit to 0 at the beginning of the program.

Figure 11.4 CM0 Register (R8C/2J Group)

System Clock Control Register 1[1] (R8C/2H Group)



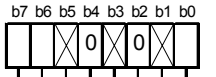
Symbol	Address	After Reset
CM1	0007h	00h

Bit Symbol	Bit Name	Function	RW
CM10	All clock stop control bit[2, 3, 4]	0 : Clock operates 1 : Stops all clocks (stop mode)	RW
— (b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
CM12	XCIN-XCOUT on-chip feedback resistor select bit	0 : On-chip feedback resistor enabled 1 : On-chip feedback resistor disabled	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
CM14	Low-speed on-chip oscillation stop bit[4, 5, 6, 7]	0 : Low-speed on-chip oscillator on 1 : Low-speed on-chip oscillator off	RW
— (b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
CM16	System clock division select bits 1[8]	b7 b6 0 0 : No division mode 0 1 : Divide-by-2 mode 1 0 : Divide-by-4 mode 1 1 : Divide-by-16 mode	RW
CM17			RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the CM1 register.
2. If the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
3. If the CM10 bit is set to 1 (stop mode), when the CM04 bit in the CM0 register is set to 1 (XCIN-XCOUT pin), the XCIN(P4_3) pin is set to the high-impedance state and the XCOUT (P4_4) pin is set to "H". When the CM04 bit is set to 0 (I/O ports P4_3 and P4_4), pins XCIN (P4_3) and XOUT (P4_4) retain the I/O status (status just before stop mode is entered).
4. When count source protection mode for the watch dog timer is enabled (refer to **16.2 Count Source Protection Mode Enabled**), the value remains unchanged even if bits CM10 and CM14 are set.
5. When the OCD2 bit in the OCD register is set to 0 (XCIN clock selected), the CM14 bit is set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
6. When using the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when using the digital filter), set the CM14 bit to 0 (low-speed on-chip oscillator on).
7. In count source protect mode enabled, the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
8. When the CM06 bit in the CM0 register is set to 0 (bits CM16, CM17 enabled), bits CM16 to CM17 are enabled.

Figure 11.5 CM1 Register (R8C/2H Group)

System Clock Control Register 1[1] (R8C/2J Group)



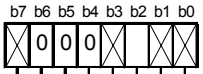
Symbol	Address	After Reset
CM1	0007h	00h

Bit Symbol	Bit Name	Function	RW
CM10	All clock stop control bit[2]	0 : Clock operates 1 : Stops all clocks (stop mode)	RW
— (b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b2)	Reserved bit	Set to 0.	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b4)	Reserved bit	Set to 0.	RW
— (b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
CM16	System clock division select bits 1[3]	b7 b6 0 0 : No division mode 0 1 : Divide-by-2 mode 1 0 : Divide-by-4 mode 1 1 : Divide-by-16 mode	RW
CM17			RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the CM1 register.
2. When count source protection mode for the watch dog timer is enabled (refer to **16.3 Count Source Protection Mode Enabled**), the value remains unchanged even if the CM10 bit is set.
3. When the CM06 bit in the CM0 register is set to 0 (bits CM16, CM17 enabled), bits CM16 to CM17 are enabled.

Figure 11.6 CM1 Register (R8C/2J Group)

System Clock Select Register[1] (for R8C/2H Group only)



Symbol	Address	After Reset
OCD	000Ch	00000100b

Bit Symbol	Bit Name	Function	RW
— (b1-b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
OCD2	System clock select bit	0 : Selects XCIN clock 1 : Selects on-chip oscillator clock[2]	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b6-b4)	Reserved bits	Set to 0.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting to the OCD register.
2. The CM14 in the CM1 register bit is set to 0 (low-speed on-chip oscillator on) if the OCD2 bit is set to 1 (on-chip oscillator clock selected).

Figure 11.7 OCD Register (for R8C/2H Group only)

High-Speed On-Chip Oscillator Control Register 0(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
HRA0	0020h	00h

Bit Symbol	Bit Name	Function	RW
HRA00	High-speed on-chip oscillator enable bit	0 : High-speed on-chip oscillator off 1 : High-speed on-chip oscillator on	RW
HRA01	High-speed on-chip oscillator select bit(2)	0 : Selects low-speed on-chip oscillator(3) 1 : Selects high-speed on-chip oscillator	RW
— (b7-b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the HRA0 register.
2. Change the HRA01 bit under the following conditions.
   • HRA00 = 1 (high-speed on-chip oscillation on)
   • The CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
3. When setting the HRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the HRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the HRA00 bit to 0 after setting the HRA01 bit to 0.

High-Speed On-Chip Oscillator Control Register 1(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
HRA1	0021h	When Shipping

Function	RW
The frequency of the high-speed on-chip oscillator is adjusted with bits 0 to 7.(2) High-speed on-chip oscillator frequency = 8 MHz (HRA1 register = value when shipping; fOCO-fast mode 0) Setting the HRA1 register to a lower value results in a higher frequency. Setting the HRA1 register to a higher value results in a lower frequency.	RW

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the HRA1 register.
2. When changing the values of the HRA1 register, adjust these bits not to exceed the maximum value of the system clock.

High-Speed On-Chip Oscillator Control Register 2(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
HRA2	0022h	00h

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	Set to 0.	RW
HRA21	High-speed on-chip oscillator mode select bit(3)	0: fOCO-fast mode 0 (8 MHz when the HRA1 register is set to the value when shipping) 1: fOCO-fast mode 2(2)	RW
— (b4-b2)	Reserved bits	Set to 0.	RW
— (b7-b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Set the PRC0 bit in the PRCR register to 1 (write enable) before rewriting the HRA2 register.
2. Switching fOCO-fast mode 0 to fOCO-fast mode 2 multiplies the frequency by 0.5.
3. Set this bit not to exceed the maximum value of the system clock.

Figure 11.8 Registers HRA0, HRA1, and HRA2

Clock Prescaler Reset Flag (for R8C/2H Group only)

b7	b6	b5	b4	b3	b2	b1	b0
	0	0	0	0	0	0	0

Symbol	Address	After Reset
CPSRF	0028h	00h

Bit Symbol	Bit Name	Function	RW
— (b6-b0)	Reserved bits	Set to 0.	RW
CPSR	Clock prescaler reset flag(1)	Setting this bit to 1 initializes the clock prescaler. (When read, the content is 0)	RW

NOTE:
1. Only write 1 to this bit when selecting the XCIN clock as the CPU clock, .

Figure 11.9 CPSRF Register (for R8C/2H Group only)

High-Speed On-Chip Oscillator Control Register 4

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
FRA4	0029h	When Shipping

Function	RW
Stores data for frequency correction when VCC = 2.7 to 5.5 V. (The value is the same as that of the HRA1 register after a reset.) Optimal frequency correction to match the voltage conditions can be achieved by transferring this value to the HRA1 register.	RO

High-Speed On-Chip Oscillator Control Register 6

b7	b6	b5	b4	b3	b2	b1	b0

Symbol	Address	After Reset
FRA6	002Bh	When Shipping

Function	RW
Stores data for frequency correction when VCC = 2.2 to 5.5 V. Optimal frequency correction to match the voltage conditions can be achieved by transferring this value to the HRA1 register.	RO

Figure 11.10 Registers FRA4 and FRA6

Voltage Detection Register 2(1)

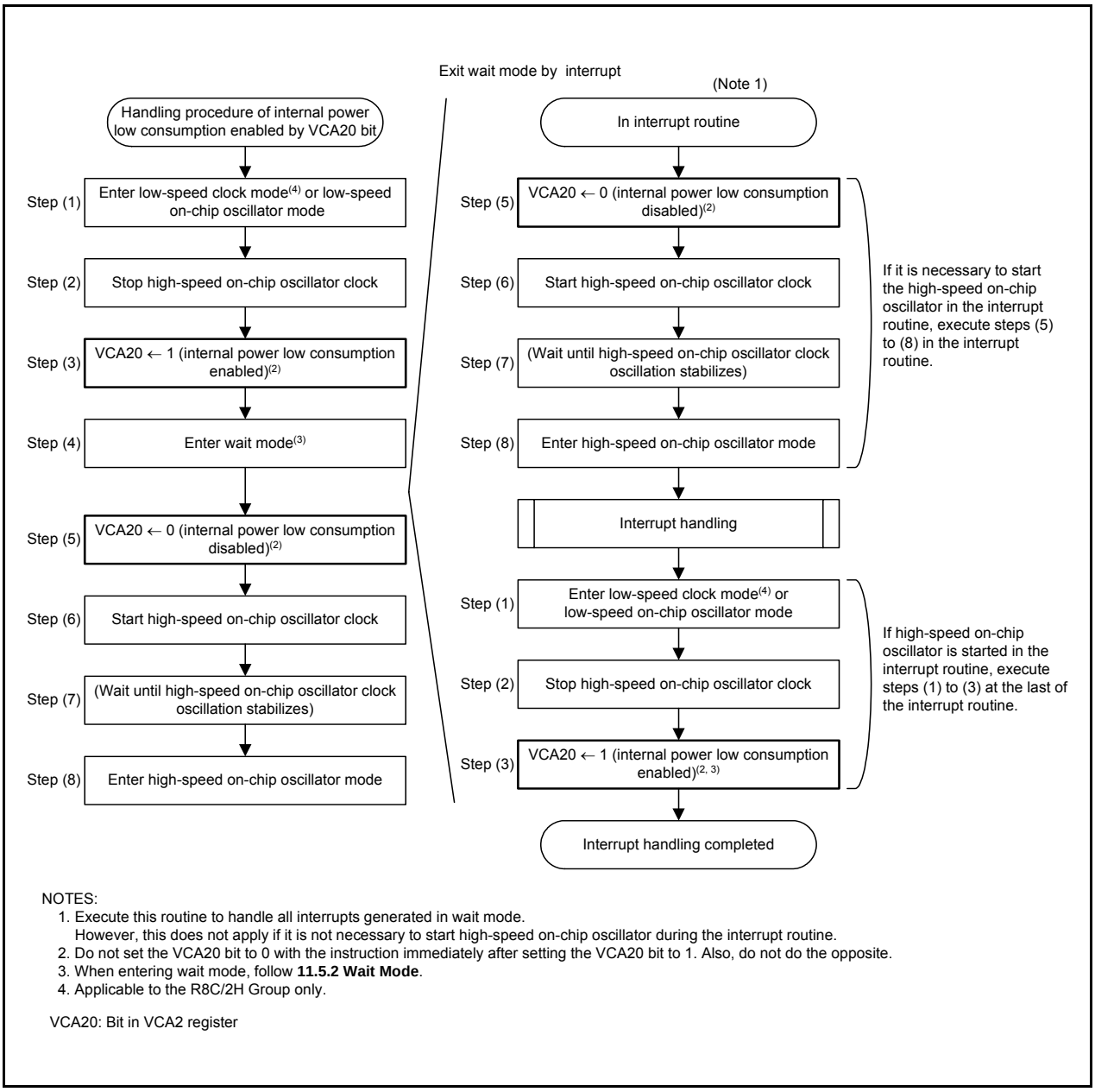
b7	b6	b5	b4	b3	b2	b1	b0
			0	0	0	0	

Symbol	Address	After Reset(5)
VCA2	0032h	The LVD0ON bit in the OFS register is set to 1 and hardware reset : 00h Power-on reset, voltage monitor 0 reset or LVD0ON bit in the OFS register is set to 0, and hardware reset : 00100000b

Bit Symbol	Bit Name	Function	RW
VCA20	Internal power low consumption enable bit(6)	0 : Low consumption disabled 1 : Low consumption enabled(7)	RW
— (b4-b1)	Reserved bits	Set to 0.	RW
VCA25	Voltage detection 0 enable bit(2)	0 : Voltage detection 0 circuit disabled 1 : Voltage detection 0 circuit enabled	RW
VCA26	Voltage detection 1 enable bit(3)	0 : Voltage detection 1 circuit disabled 1 : Voltage detection 1 circuit enabled	RW
VCA27	Voltage detection 2 enable bit(4)	0 : Voltage detection 2 circuit disabled 1 : Voltage detection 2 circuit enabled	RW

NOTES:
1. Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting to the VCA2 register.
2. To use the voltage monitor 0 reset, set the VCA25 bit to 1.
   After the VCA25 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
3. To use the voltage monitor 1 interrupt/reset or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1.
   After the VCA26 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
4. To use the voltage monitor 2 interrupt/reset or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1.
   After the VCA27 bit is set to 1 from 0, the voltage detection circuit waits for td(E-A) to elapse before starting operation.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, and voltage monitor 2 reset do not affect this register.
6. Use the VCA20 bit only when entering to wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 11.12 Handling Procedure of Internal Power Low Consumption Using VCA20 Bit**.
7. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).

Figure 11.11 VCA2 Register



NOTES:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When entering wait mode, follow **11.5.2 Wait Mode**.
4. Applicable to the R8C/2H Group only.

VCA20: Bit in VCA2 register

Figure 11.12 Handling Procedure of Internal Power Low Consumption Using VCA20 Bit

The clocks generated by the clock generation circuits are described below.

11.1 On-Chip Oscillator Clocks

These clocks are supplied by the on-chip oscillators (high-speed on-chip oscillator and a low-speed on-chip oscillator). The on-chip oscillator clock is selected by the HRA01 bit in the HRA0 register.

11.1.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, and fOCO-S.
After reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 8 is selected as the CPU clock.
The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

11.1.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, and fOCO-F.

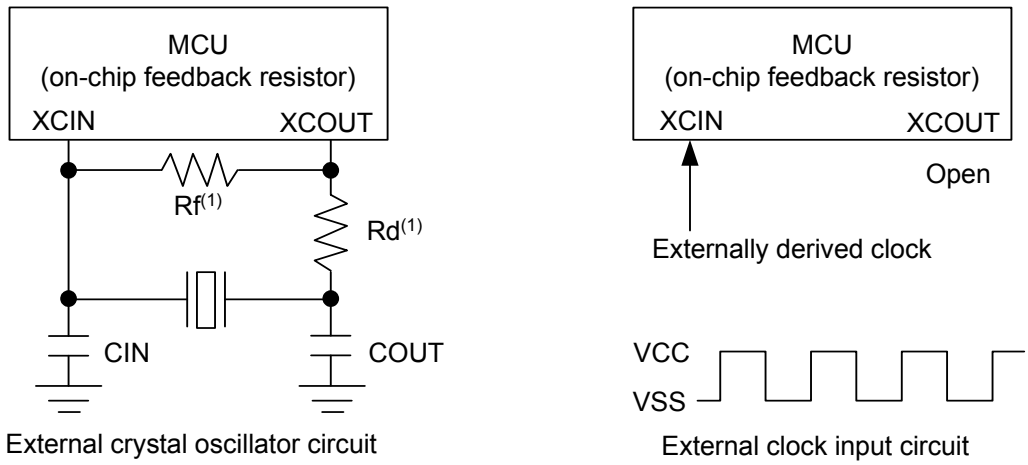
After reset, the on-chip oscillator clock generated by the high-speed on-chip oscillator stops. Oscillation is started by setting the HRA00 bit in the HRA0 register to 1 (high-speed on-chip oscillator on). The frequency can be adjusted by registers HRA1 and HRA2.
Furthermore, frequency correction data corresponding to the supply voltage ranges listed below is stored in registers FRA4 and FRA6. To use separate correction values to match these voltage ranges, transfer them from register FRA4 or FRA6 to the HRA1 register.

- FRA4 register: Stores data for frequency correction corresponding to VCC = 2.7 V to 5.5 V.
  (The value is the same as that of the HRA1 register after a reset.)
- FRA6 register: Stores data for frequency correction corresponding to VCC = 2.2 V to 5.5 V.

Since there are differences in the amount of frequency adjustment among the bits in the HRA1 register, make adjustments by changing the settings of individual bits. Adjust the HRA1 register so that the frequency of the high-speed on-chip oscillator clock does not exceed the maximum value of the system clock.

11.2 XCIN Clock (for R8C/2H Group only)

This clock is supplied by the XCIN clock oscillation circuit. This clock is used as the clock source for the CPU clock, peripheral function clock. The XCIN clock oscillation circuit is configured by connecting a resonator between the XCIN and XCOUT pins. The XCIN clock oscillation circuit includes an on-chip a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed in the chip. The XCIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XCIN pin.
Figure 11.13 shows Examples of XCIN Clock Connection Circuits.
During and after reset, the XCIN clock oscillates.
The XCIN clock starts oscillating when the CM04 bit in the CM0 register is set to 1 (XCIN-XCOUT pin).
To use the XCIN clock for the CPU clock source, set the OCD2 bit in the OCD register to 0 (selects XCIN clock) after the XCIN clock is oscillating stably.
This MCU has an on-chip feedback resistor and on-chip resistor disable/enable switching is possible by the CM12 bit in the CM1 register.
In stop mode, all clocks including the XCIN clock stop. Refer to **11.4 Power Control** for details.



NOTE:
1. Insert a damping resistor and feedback resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the manufacturer of the oscillator. When the oscillation drive capacity is set to low, check that oscillation is stable. Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XCIN and XCOUT following the instructions.

Figure 11.13 Examples of XCIN Clock Connection Circuits

11.3 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions. Refer to **Figure 11.1 Clock Generation Circuit for R8C/2H Group** and **Figure 11.2 Clock Generation Circuit for R8C/2J Group**.

11.3.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. Either the XCIN clock (for R8C/2H Group only) or the on-chip oscillator clock can be selected.

11.3.2 CPU Clock

The CPU clock is an operating clock for the CPU and watchdog timer.
The system clock can be divided by 1 (no division), 2, 4, 8, or 16 to produce the CPU clock. Use the CM06 bit in the CM0 register and bits CM16 to CM17 in the CM1 register to select the value of the division.
Use the XCIN clock while the XCIN clock oscillation stabilizes (for the R8C/2H Group only).
After reset, the low-speed on-chip oscillator clock divided by 8 provides the CPU clock.
When entering stop mode from high-speed clock mode, the CM06 bit is set to 1 (divide-by-8 mode).

11.3.3 Peripheral Function Clock (f1, f2, f4, f8, and f32)

The peripheral function clock is the operating clock for the peripheral functions.
The clock fi (i = 1, 2, 4, 8, and 32) is generated by the system clock divided by i. The clock fi is used for timers RA, RB, RE, and RF, and the serial interface.
When the WAIT instruction is executed after setting the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode), the clock fi stop.

11.3.4 fOCO

fOCO is an operating clock for the peripheral functions.
fOCO runs at the same frequency as the on-chip oscillator clock and can be used as the source for timer RA.
When the WAIT instruction is executed, the clocks fOCO does not stop.

11.3.5 fOCO-F

fOCO-F is generated by the high-speed on-chip oscillator and supplied by setting the HRA00 bit to 1.
When the WAIT instruction is executed, the clock fOCO-F does not stop.

11.3.6 fOCO-S

fOCO-S is an operating clock for the watchdog timer and voltage detection circuit. fOCO-S is supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on) and uses the clock generated by the low-speed on-chip oscillator. When the WAIT instruction is executed or in count source protect mode of the watchdog timer, fOCO-S does not stop.

11.3.7 fC4 and fC32 (for R8C/2H Group only)

The clock fC4 is used for timer RE and the clock fC32 is used for timer RA, timer RF, and watchdog timer.
Use fC4 and fC32 while the XCIN clock oscillation stabilizes.

11.4 Power Control

There are three power control modes. All modes other than wait mode and stop mode are referred to as standard operating mode.

11.4.1 Standard Operating Mode

Standard operating mode is further separated into three modes.
Table 11.3 lists the Settings and Modes of Clock Associated Bits for R8C/2H Group and Table 11.4 lists the Settings and Modes of Clock Associated Bits for R8C/2J Group.
In standard operating mode, the CPU clock and the peripheral function clock are supplied to operate the CPU and the peripheral function clocks. Power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. When unnecessary oscillator circuits stop, power consumption is further reduced.
Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. If the new clock source is the XCIN clock, allow sufficient wait time in a program until oscillation is stabilized before exiting (for the R8C/2H Group only).

Table 11.3 Settings and Modes of Clock Associated Bits for R8C/2H Group

Modes		OCD Register	CM1 Register		CM0 Register		HRA0 Register	
		OCD2	CM17, CM16	CM14	CM06	CM04	HRA01	HRA00
High-speed on-chip oscillator mode	No division	1	00b	–	0	–	1	1
	Divide-by-2	1	01b	–	0	–	1	1
	Divide-by-4	1	10b	–	0	–	1	1
	Divide-by-8	1	–	–	1	–	1	1
	Divide-by-16	1	11b	–	0	–	1	1
Low-speed on-chip oscillator mode	No division	1	00b	0	0	–	0	–
	Divide-by-2	1	01b	0	0	–	0	–
	Divide-by-4	1	10b	0	0	–	0	–
	Divide-by-8	1	–	0	1	–	0	–
	Divide-by-16	1	11b	0	0	–	0	–
Low-speed clock mode	No division	0	00b	–	0	1	–	–
	Divide-by-2	0	01b	–	0	1	–	–
	Divide-by-4	0	10b	–	0	1	–	–
	Divide-by-8	0	–	–	1	1	–	–
	Divide-by-16	0	11b	–	0	1	–	–

–: Can be 0 or 1, no change in outcome

Table 11.4 Settings and Modes of Clock Associated Bits for R8C/2J Group

Modes		CM1 Register	CM0 Register	HRA0 Register	
		CM17, CM16	CM06	HRA01	HRA00
High-speed on-chip oscillator mode	No division	00b	0	1	1
	Divide-by-2	01b	0	1	1
	Divide-by-4	10b	0	1	1
	Divide-by-8	–	1	1	1
	Divide-by-16	11b	0	1	1
Low-speed on-chip oscillator mode	No division	00b	0	0	–
	Divide-by-2	01b	0	0	–
	Divide-by-4	10b	0	0	–
	Divide-by-8	–	1	0	–
	Divide-by-16	11b	0	0	–

–: Can be 0 or 1, no change in outcome

11.4.1.1 High-Speed On-Chip Oscillator Mode

The high-speed on-chip oscillator is used as the on-chip oscillator clock when the HRA00 bit in the HRA0 register is set to 1 (high-speed on-chip oscillator on) and the HRA01 bit in the HRA0 register is set to 1. The on-chip oscillator divided by 1 (no division), 2, 4, 8, or 16 provides the CPU clock. Set the CM06 bit to 1 (divide-by-8 mode) when transiting to high-speed clock mode.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used as the watchdog timer and voltage detection circuit (for R8C/2H Group only).

11.4.1.2 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on) or the HRA01 bit in the HRA0 register is set to 0, the low-speed on-chip oscillator provides the on-chip oscillator clock.
The on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 provides the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used as the watchdog timer and voltage detection circuit (for R8C/2H Group only).
In this mode, stopping the high-speed on-chip oscillator, and setting the FMR47 bit in the FMR4 register to 1 (flash memory low consumption current read mode enabled) enables low consumption operation.
To enter wait mode from low-speed on-chip oscillator mode, setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled) enables lower consumption current in wait mode.
Refer to **21. Reducing Power Consumption** for how to reduce the power consumption.

11.4.1.3 Low-Speed Clock Mode (for R8C/2H Group only)

The XCIN clock divided by 1 (no division), 2, 4, 8, or 16 provides the CPU clock. Set the CM06 bit to 1 (divide by-8 mode) when transiting to high-speed on-chip oscillator mode, low-speed on-chip oscillator mode. If the CM14 bit is set to 0 (low-speed on-chip oscillator on) or the HRA00 bit in the HRA0 register is set to 1 (high speed on-chip oscillator on), fOCO can be used as timer RA.
When the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used as the watchdog timer and voltage detection circuit.
In this mode, stopping the high-speed on-chip oscillator, and setting the FMR47 bit in the FMR4 register to 1 (flash memory low consumption current read mode enabled) enables low consumption operation.
To enter wait mode from low-speed clock mode, setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled) enables lower consumption current in wait mode.
Refer to **21. Reducing Power Consumption** for how to reduce the power consumption.

11.4.2 Wait Mode

Since the CPU clock stops in wait mode, the CPU, which operates using the CPU clock, and the watchdog timer, when count source protection mode is disabled, stop. The XCIN clock (for R8C/2H Group only) and on-chip oscillator clock do not stop and the peripheral functions using these clocks continue operating.

11.4.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the f1, f2, f4, f8, and f32 clocks stop in wait mode. This reduces power consumption.

11.4.2.2 Entering Wait Mode

The MCU enters wait mode when the WAIT instruction is executed.

11.4.2.3 Pin Status in Wait Mode

The I/O port is the status before wait mode was entered is maintained.

11.4.2.4 Exiting Wait Mode

The MCU exits wait mode by a reset or a peripheral function interrupt.
The peripheral function interrupts are affected by the CM02 bit. When the CM02 bit is set to 0 (peripheral function clock does not stop in wait mode), all peripheral function interrupts can be used to exit wait mode. When the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the peripheral functions using the peripheral function clock stop operating and the peripheral functions operated by external signals or on-chip oscillator clock can be used to exit wait mode.
Table 11.5 lists Interrupts to Exit Wait Mode and Usage Conditions.

Table 11.5 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 = 0	CM02 = 1
Serial interface interrupt	Usable when operating with internal or external clock	Usable when operating with external clock
Key input interrupt	Usable	Usable
Timer RA interrupt	Usable in all modes	Can be used if there is no filter in event counter mode. Usable by selecting fOCO or fC32(1) as count source.
Timer RB interrupt	Usable in all modes	(Do not use)
Timer RE interrupt(1)	Usable in all modes	Usable when operating in real time clock mode
Timer RF interrupt	Usable in all modes	(Do not use)
$\overline{INT0}$, $\overline{INT1}$ interrupt	Usable	Can be used if there is no filter
Voltage monitor 1 interrupt	Usable	Usable
Voltage monitor 2 interrupt	Usable	Usable

NOTE:
1. Applicable to the R8C/2H Group only.

Figure 11.14 shows the Time from Wait Mode to Interrupt Routine Execution.
When using a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting wait mode.

When exiting by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register, as described in Figure 11.14.
The CPU clock, when exiting wait mode by a peripheral function interrupt, is the same clock as the CPU clock when the WAIT instruction is executed.

FMR0 Register FMSTP Bit	Time until Flash Memory is Activated (T1)	Time until CPU Clock is Supplied (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	Period of system clock × 12 cycles + 30 μs (max.)	Period of CPU clock × 6 cycles	Period of CPU clock × 20 cycles	Following total time is the time from wait mode until an interrupt routine is executed.
1 (flash memory stops)	Period of system clock × 12 cycles	Same as above	Same as above	

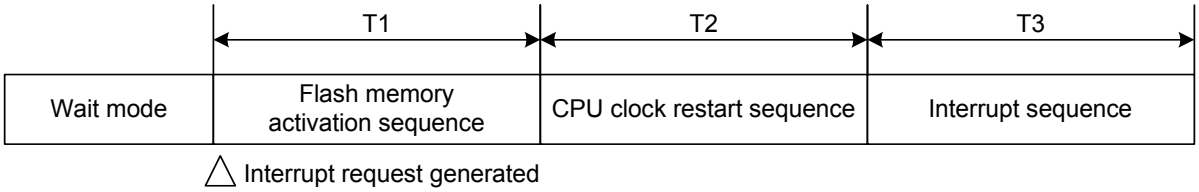


Figure 11.14 Time from Wait Mode to Interrupt Routine Execution

11.4.3 Stop Mode

Since the oscillator circuits stop in stop mode, the CPU clock and peripheral function clock stop and the CPU and peripheral functions that use these clocks stop operating. The least power required to operate the MCU is in stop mode. If the voltage applied to the VCC pin is VRAM or more, the contents of internal RAM is maintained.
The peripheral functions clocked by external signals continue operating.
Table 11.6 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 11.6 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	–
$\overline{\text{INT0}}$, $\overline{\text{INT1}}$ interrupt	Can be used if there is no filter
Timer RA interrupt	When there is no filter and external pulse is counted in event counter mode
Serial interface interrupt	When external clock is selected
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (VW1C1 bit in VW1C register is set to 1)
Voltage monitor 2 interrupt	Usable in digital filter disabled mode (VW2C1 bit in VW2C register is set to 1)

11.4.3.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode), the CM03 bit in the CM0 register is set to 1 (XCIN clock oscillator circuit drive capacity high) (for the R8C/2H Group only).

11.4.3.2 Pin Status in Stop Mode

The status before wait mode was entered is maintained.
In the R8C/2H Group, when the CM04 bit in the CM0 register is set to 1 (XCIN-XOUT pin), the XCIN (P4_3) pin is set to the high-impedance state and the XCOUT (P4_4) pin is set to “H”. When the CM04 bit is set to 0 (I/O ports P4_3 and P4_4), pins XCIN (P4_3) and XOUT (P4_4) retain the I/O status (status just before stop mode is entered).

11.4.3.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
Figure 11.15 shows the Time from Stop Mode to Interrupt Routine Execution.
When using a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operates the peripheral function to be used for exiting stop mode.

When exiting by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply is started.
If the clock used immediately before stop mode is a system clock and stop mode is exited by a peripheral function interrupt, the CPU clock becomes the previous system clock divided by 8.

FMR0 Register FMSTP Bit	Time until Flash Memory is Activated (T2)	Time until CPU Clock is Supplied (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	Period of system clock × 12 cycles + 30 µs (max.)	Period of CPU clock × 6 cycles	Period of CPU clock × 20 cycles	Following total time of T0 to T4 is the time from stop mode until an interrupt handling is executed.
1 (flash memory stops)	Period of system clock × 12 cycles	Same as above	Same as above	

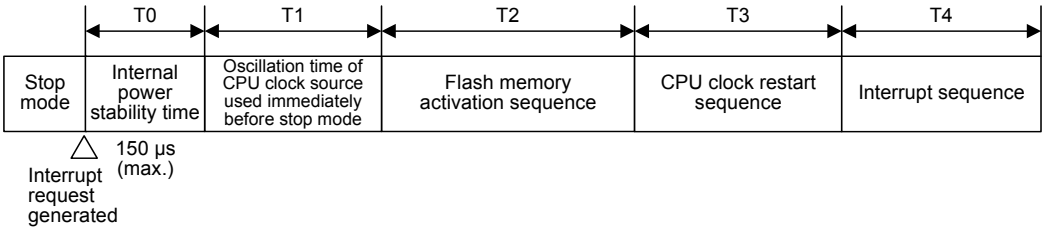


Figure 11.15 Time from Stop Mode to Interrupt Routine Execution

Figure 11.16 shows the State Transitions in Power Control Mode for R8C/2H Group and Figure 11.17 shows the State Transitions in Power Control Mode for R8C/2J Group.

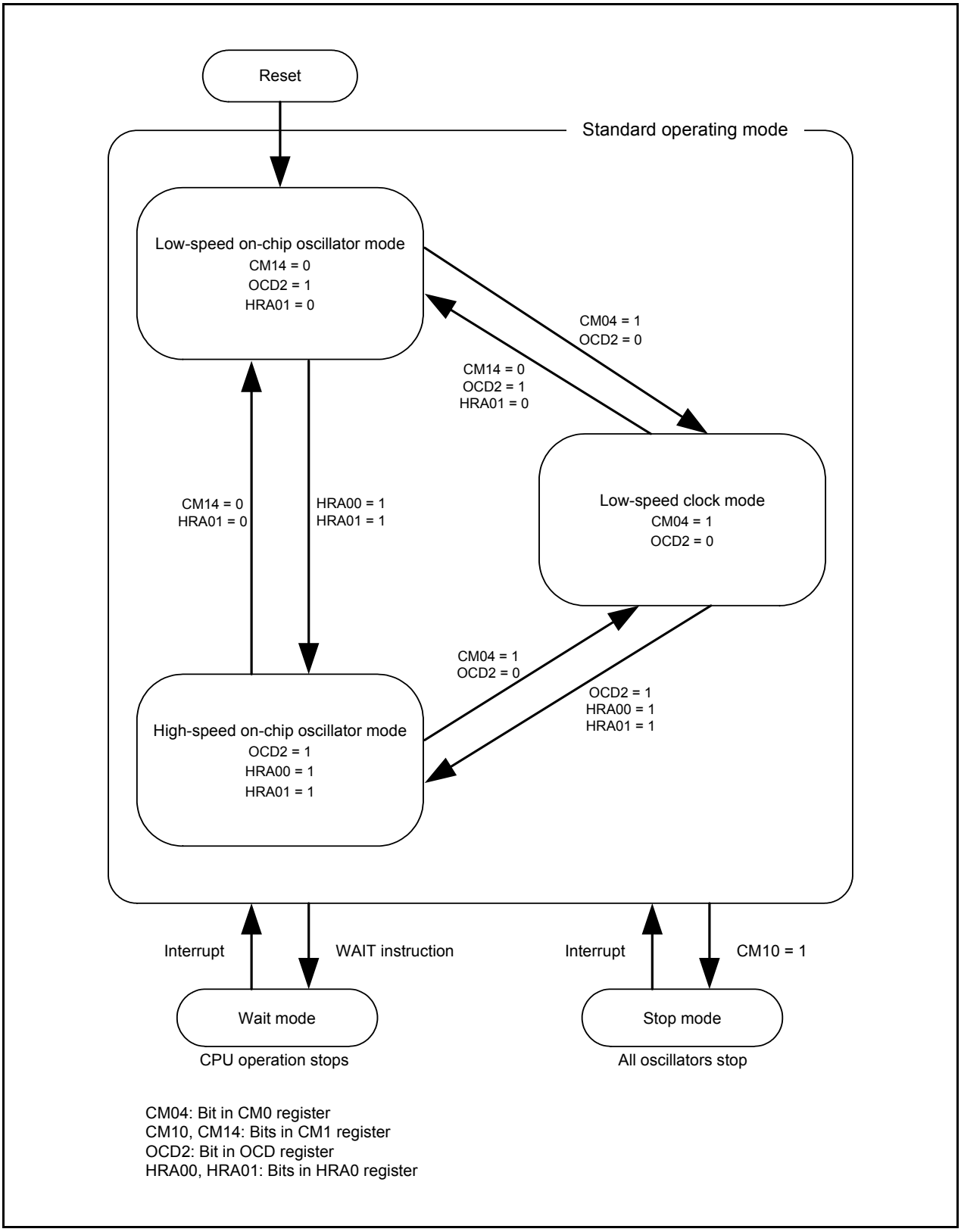


Figure 11.16 State Transitions in Power Control Mode for R8C/2H Group

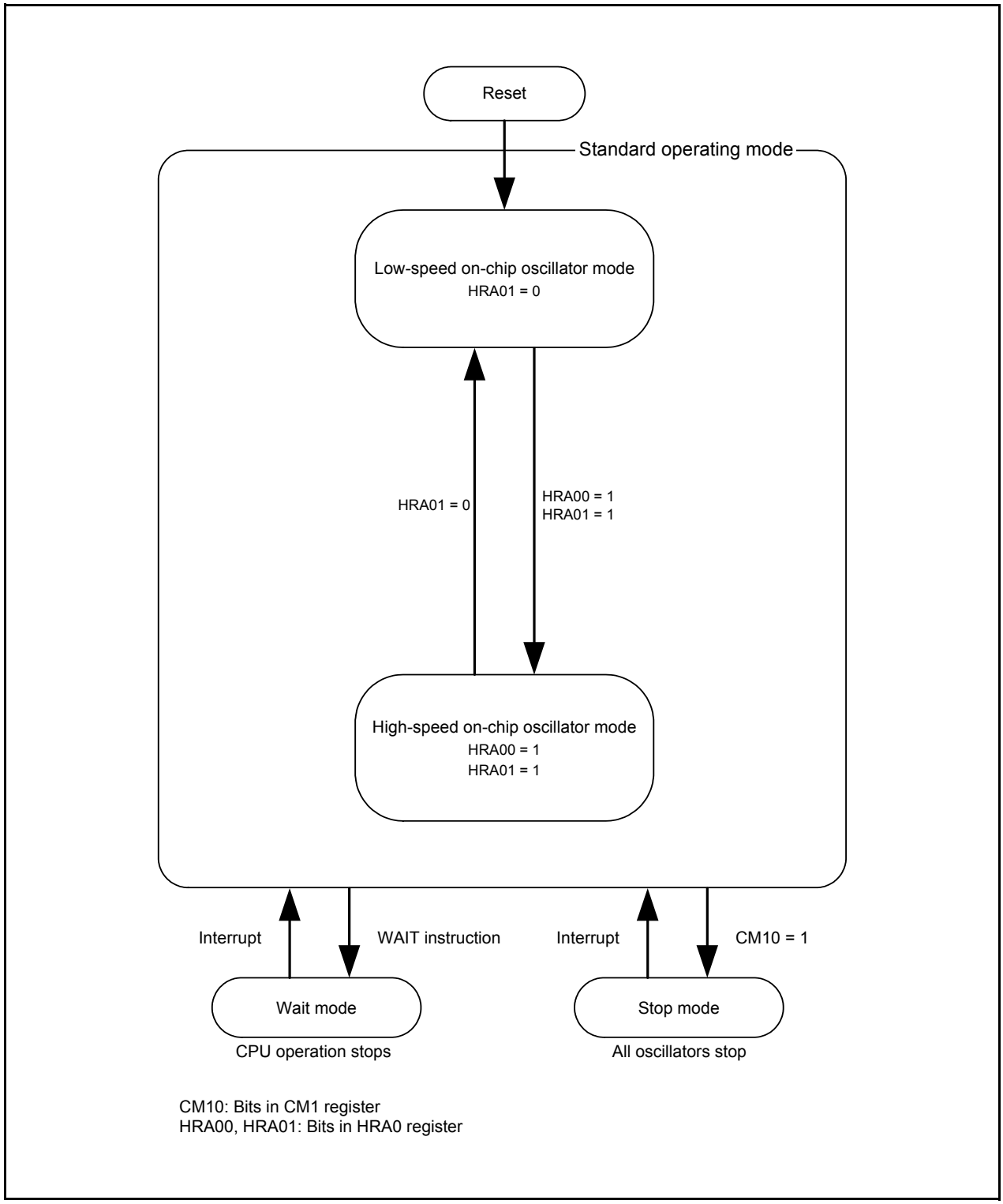


Figure 11.17 State Transitions in Power Control Mode for R8C/2J Group

11.5 Notes on Clock Generation Circuit

11.5.1 Stop Mode

When entering stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least 4 NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter stop mode

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        BSET    0,PRCR          ; Protect disabled
        FSET    I               ; Enable interrupt
        BSET    0,CM1           ; Stop mode
        JMP.B   LABEL_001
LABEL_001 :
        NOP
        NOP
        NOP
        NOP
```

11.5.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the WAIT instruction and the program stops. Insert at least 4 NOP instructions after the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        FSET    I               ; Enable interrupt
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

11.5.3 Oscillation Circuit Constants

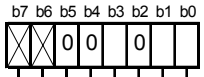
Ask the manufacturer of the oscillator to specify the best oscillation circuit constants for your system.

12. Protection

The protection function protects important registers from being easily overwritten when a program runs out of control. Figure 12.1 shows the PRCR Register. The registers protected by the PRCR register are listed below.

- Registers protected by PRC0 bit: Registers CM0, CM1, OCD (for the R8C/2H Group only), HRA0, HRA1, and HRA2
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC3 bit: Registers VCA2, VW0C, VW1C, VW2C, VCAB, BGRCR, and BGRTRM

Protect Register



Symbol	Address	After Reset
PRCR	000Ah	00h

Bit Symbol	Bit Name	Function	RW
PRC0	Protect bit 0	Writing to registers CM0, CM1, OCD (for the R8C/2H Group only), HRA0, HRA1, and HRA2 is enabled. 0 : Disables writing 1 : Enables writing	RW
PRC1	Protect bit 1	Writing to registers PM0 and PM1 is enabled. 0 : Disables writing 1 : Enables writing	RW
— (b2)	Reserved bit	Set to 0.	RW
PRC3	Protect bit 3	Writing to registers VCA2, VW0C, VW1C, VW2C, VCAB, BGRCR, and BGRTRM is enabled. 0 : Disables writing 1 : Enables writing	RW
— (b5-b4)	Reserved bits	Set to 0.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. This PRC2 bit is set to 0 after writing 1 to this bit and executing a write to any address. Since the other bits are not set to 0, set them to 0 by a program.

Figure 12.1 PRCR Register

13. Interrupts

13.1 Interrupt Overview

13.1.1 Types of Interrupts

Figure 13.1 shows the Types of Interrupts.

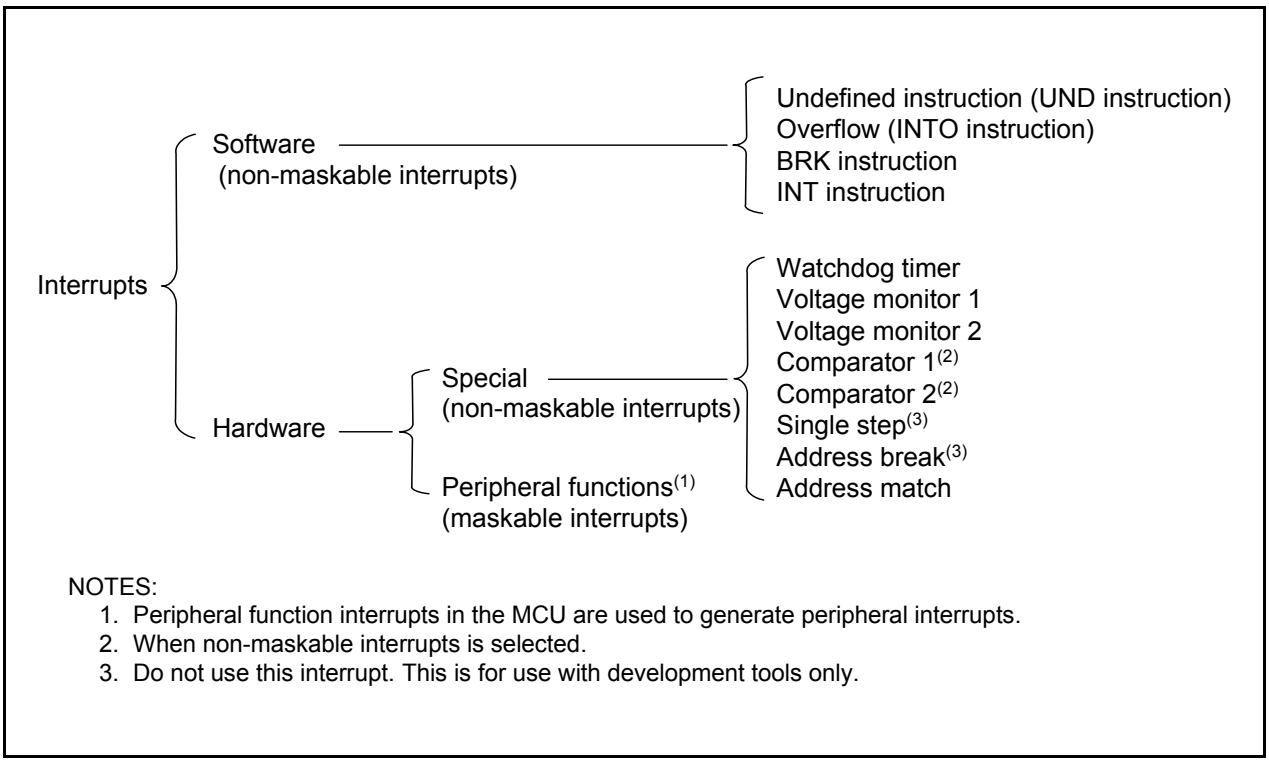


Figure 13.1 Types of Interrupts

- Maskable Interrupts: The interrupt enable flag (I flag) enables or disables these interrupts. The interrupt priority order can be changed based on the interrupt priority level.
- Non-Maskable Interrupts: The interrupt enable flag (I flag) does not enable or disable these interrupts. The interrupt priority order cannot be changed based on interrupt priority level.

13.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

13.1.2.1 Undefined Instruction Interrupt

The undefined instruction interrupt is generated when the UND instruction is executed.

13.1.2.2 Overflow Interrupt

The overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are: ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

13.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

13.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. The INT instruction can select software interrupt numbers 0 to 63. Software interrupt numbers 3 to 31 are assigned to the peripheral function interrupt. Therefore, the MCU executes the same interrupt routine when the INT instruction is executed as when a peripheral function interrupt is generated. For software interrupt numbers 0 to 31, the U flag is saved to the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

13.1.3 Special Interrupts

Special interrupts are non-maskable. However, the comparator 1 and comparator 2 can select maskable interrupts, too.

13.1.3.1 Watchdog Timer Interrupt

The watchdog timer interrupt is generated by the watchdog timer. For details of the watchdog timer, refer to **16. Watchdog Timer**.

13.1.3.2 Voltage Monitor 1 Interrupt

The voltage monitor 1 interrupt is generated by the voltage monitor 1 circuit. For details of the voltage monitor 1 circuit, refer to **6. Voltage Detection Circuit**.

13.1.3.3 Voltage Monitor 2 Interrupt

The voltage monitor 2 interrupt is generated by the voltage monitor 2 circuit. For details of the voltage monitor 2, refer to **6. Voltage Detection Circuit**.

13.1.3.4 Comparator 1 Interrupt

The comparator 1 interrupt is generated by the comparator 1. The non-maskable interrupt or maskable interrupt can be selected. For details of the comparator 1 interrupt, refer to **7. Comparator**.

13.1.3.5 Comparator 2 Interrupt

The comparator 2 interrupt is generated by the comparator 2. The non-maskable interrupt or maskable interrupt can be selected. For details of the comparator 2 interrupt, refer to **7. Comparator**.

13.1.3.6 Single-Step Interrupt, and Address Break Interrupt

Do not use these interrupts. They are for use by development tools only.

13.1.3.7 Address Match Interrupt

The address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 when the AIER0 or AIER1 bit in the AIER register is set to 1 (address match interrupt enable). For details of the address match interrupt, refer to **13.4 Address Match Interrupt**.

13.1.4 Peripheral Function Interrupt

The peripheral function interrupt is generated by the internal peripheral function of the MCU and is a maskable interrupt. Refer to **Table 13.2 Relocatable Vector Tables** for sources of the peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

13.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 13.2 shows an Interrupt Vector.

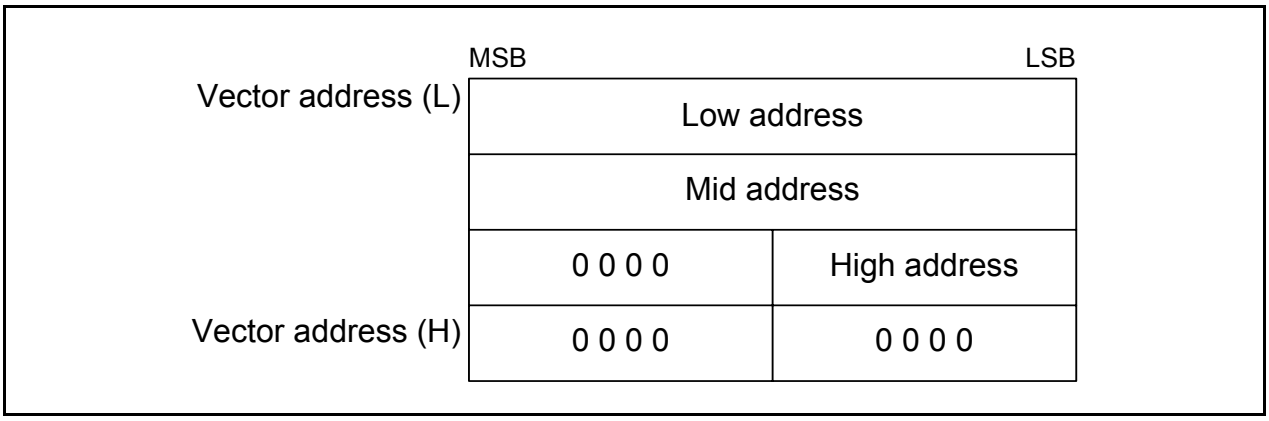


Figure 13.2 Interrupt Vector

13.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 13.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **20.3 Functions to Prevent Rewriting of Flash Memory**.

Table 13.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt on UND instruction	R8C/Tiny Series Software Manual
Overflow	0FFE0h to 0FFE3h	Interrupt on INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE7h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		13.4 Address Match Interrupt
Single step(1)	0FFECh to 0FFEFh		
Watchdog timer, Voltage monitor 1, Voltage monitor 2, Comparator 1, Comparator 2	0FFF0h to 0FFF3h		16. Watchdog Timer 6. Voltage Detection Circuit 7. Comparator
Address break(1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

NOTE:
1. Do not use these interrupts. They are for use by development tools only.

13.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Table 13.2 lists the Relocatable Vector Tables.

Table 13.2 Relocatable Vector Tables

Interrupt Source	Vector Addresses(1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction(2)	+0 to +3(0000h to 0003h)	0	–	R8C/Tiny Series Software Manual
Comparator 1	+4 to +7(0004h to 0007h)	1	VCMP1IC	7. Comparator
Comparator 2	+8 to +11(0008h to 000Bh)	2	VCMP2IC	
(Reserved)		3 to 9	–	–
Timer RE(3)	+40 to +43(0028h to 002Bh)	10	TREIC	17.3 Timer RE (for R8C/2H Group only)
UART2 transmit(3)	+44 to +47(002Ch to 002Fh)	11	S2TIC	18. Serial Interface
UART2 receive(3)	+48 to +51(0030h to 0033h)	12	S2RIC	
Key input	+52 to +55(0034h to 0037h)	13	KUPIC	13.3 Key Input Interrupt
(Reserved)		14	–	–
(Reserved)		15	–	–
Compare 1	+64 to +67(0040h to 0043h)	16	CMP1IC	17.4 Timer RF
UART0 transmit	+68 to +71(0044h to 0047h)	17	S0TIC	18. Serial Interface
UART0 receive	+72 to +75(0048h to 004Bh)	18	S0RIC	
(Reserved)		19	–	–
(Reserved)		20	–	–
(Reserved)		21	–	–
Timer RA	+88 to +91(0058h to 005Bh)	22	TRAIC	17.1 Timer RA
(Reserved)		23	–	–
Timer RB	+96 to +99(0060h to 0063h)	24	TRBIC	17.2 Timer RB
$\overline{\text{INT1}}$	+100 to +103(0064h to 0067h)	25	INT1IC	13.2 $\overline{\text{INT}}$ Interrupt
(Reserved)		26	–	
Timer RF	+108 to +111(006Ch to 006Fh)	27	TRFIC	17.4 Timer RF
Compare 0	+112 to +115(0070h to 0073h)	28	CMP0IC	
$\overline{\text{INT0}}$	+116 to +119(0074h to 0077h)	29	INT0IC	13.2 $\overline{\text{INT}}$ Interrupt
(Reserved)		30	–	–
Capture	+124 to +127(007Ch to 007Fh)	31	CAPIC	17.4 Timer RF
Software interrupt(2)	+128 to +131(0080h to 0083h) to +252 to +255(00FCh to 00FFh)	32 to 63	–	R8C/Tiny Series Software Manual

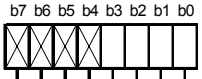
NOTES:
1. These addresses are relative to those in the INTB register.
2. The I flag does not disable these interrupts.
3. Applicable to the R8C/2H Group only.

13.1.6 Interrupt Control

The following describes enabling and disabling the maskable interrupts and setting the priority for acknowledgement. The explanation does not apply to nonmaskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in each interrupt control register to enable or disable maskable interrupts. Whether an interrupt is requested is indicated by the IR bit in each interrupt control register.
Figure 13.3 shows the Interrupt Control Register and Figure 13.4 shows the INTiIC Register (i = 0 or 1).

Interrupt Control Register(2)

Symbol	Address	After Reset
VCMP1IC	0041h	XXXXX000b
VCMP2IC	0042h	XXXXX000b
TREIC (for R8C/2H Group only)	004Ah	XXXXX000b
S2TIC (for R8C/2H Group only)	004Bh	XXXXX000b
S2RIC (for R8C/2H Group only)	004Ch	XXXXX000b
KUPIC	004Dh	XXXXX000b
CMP1IC	0050h	XXXXX000b
S0TIC	0051h	XXXXX000b
S0RIC	0052h	XXXXX000b
TRAIC	0056h	XXXXX000b
TRBIC	0058h	XXXXX000b
TRFIC	005Bh	XXXXX000b
CMP0IC	005Ch	XXXXX000b
CAPIC	005Fh	XXXXX000b

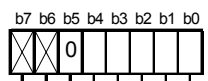


Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0 : Level 0 (interrupt disable) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0 : Requests no interrupt 1 : Requests interrupt	RW(1)
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

NOTES:
1. Only 0 can be written to the IR bit. Do not write 1.
2. Rewrite the interrupt control register when the interrupt request which is applicable for its register is not generated. Refer to **13.5.5 Changing Interrupt Control Register Contents**.

Figure 13.3 Interrupt Control Register

INTi Interrupt Control Register (i=0 or 1)(2)



Symbol	Address	After Reset
INT1IC	0059h	XX00X000b
INT0IC	005Dh	XX00X000b

Bit Symbol	Bit Name	Function	RW
ILVL0	Interrupt priority level select bits	b2 b1 b0 0 0 0 : Level 0 (interrupt disable) 0 0 1 : Level 1 0 1 0 : Level 2 0 1 1 : Level 3 1 0 0 : Level 4 1 0 1 : Level 5 1 1 0 : Level 6 1 1 1 : Level 7	RW
ILVL1			RW
ILVL2			RW
IR	Interrupt request bit	0 : Requests no interrupt 1 : Requests interrupt	RW(1)
POL	Polarity switch bit(4)	0 : Selects falling edge 1 : Selects rising edge(3)	RW
— (b5)	Reserved bit	Set to 0.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

NOTES:
1. Only 0 can be written to the IR bit. (Do not write 1.)
2. Rewrite the interrupt control register when the interrupt request which is applicable for the register is not generated. Refer to **13.5.5 Changing Interrupt Control Register Contents**.
3. If the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (selects falling edge).
4. The IR bit may be set to 1 (requests interrupt) when the POL bit is rewritten. Refer to **13.5.4 Changing Interrupt Sources**.

Figure 13.4 INTiIC Register (i = 0 or 1)

13.1.6.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

13.1.6.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. Then, when the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (= interrupt not requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.

13.1.6.3 ILVL2 to ILVL0 Bits and IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 13.3 lists the Settings of Interrupt Priority Levels and Table 13.4 lists the Interrupt Priority Levels Enabled by IPL.

The following are conditions under which an interrupt is acknowledged:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 13.3 Settings of Interrupt Priority Levels

ILVL2 to ILVL0 Bits	Interrupt Priority Level	Priority Order
000b	Level 0 (interrupt disabled)	–
001b	Level 1	Low
010b	Level 2	↓
011b	Level 3	
100b	Level 4	
101b	Level 5	
110b	Level 6	
111b	Level 7	High

Table 13.4 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Levels
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts are disabled

13.1.6.4 Interrupt Sequence

An interrupt sequence is performed between an interrupt request acknowledgement and interrupt routine execution.

When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instructions, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.

Figure 13.5 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU gets interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (interrupt not requested).

(2) The FLG register is saved to a temporary register(1) in the CPU immediately before entering the interrupt sequence.

(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (interrupts disabled).
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.

(4) The CPU's internal temporary register(1) is saved to the stack.

(5) The PC is saved to the stack.

(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.

(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.

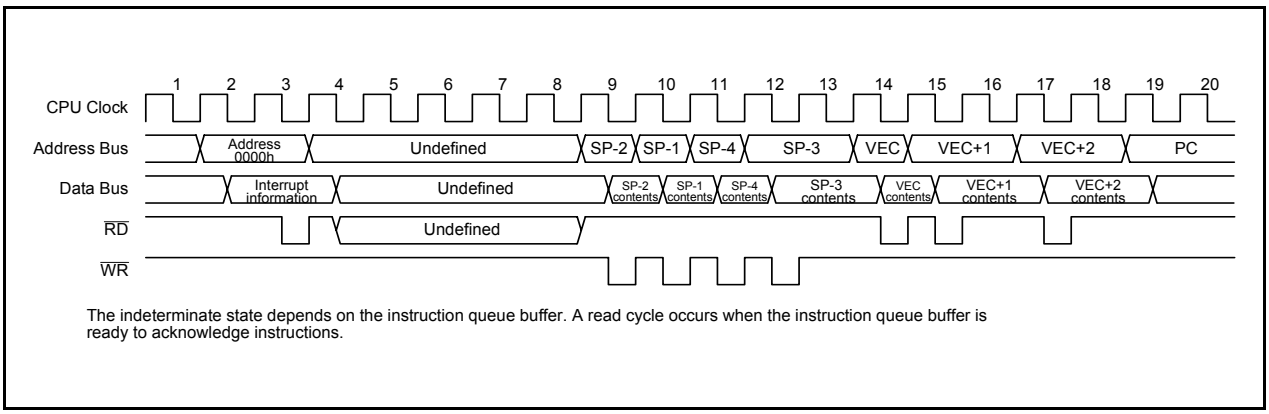


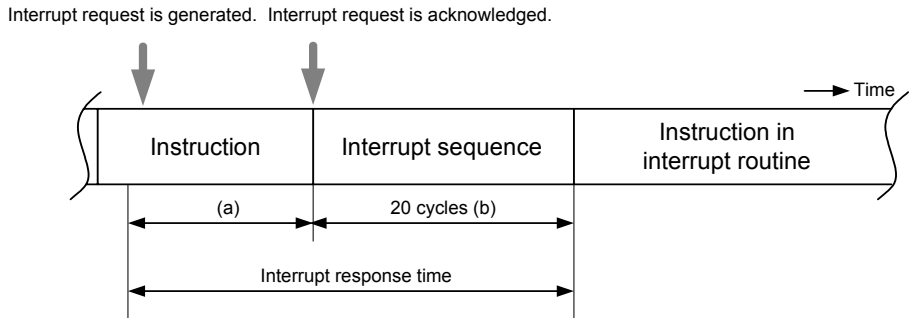
Figure 13.5 Time Required for Executing Interrupt Sequence

NOTE:

1. This register cannot be used by user.

13.1.6.5 Interrupt Response Time

Figure 13.6 shows the Interrupt Response Time. The interrupt response time is the period between an interrupt request generation and the execution of the first instruction in the interrupt routine. The interrupt response time includes the period between interrupt request generation and the completion of execution of the instruction (refer to (a) in **Figure 13.6**) and the period required to perform the interrupt sequence (20 cycles, refer to (b) in **Figure 13.6**).



(a) Period between interrupt request generation and the completion of execution of an instruction. The length of time varies depending on the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait and when the register is set as the divisor)
(b) 21 cycles for address match and single-step interrupts.

Figure 13.6 Interrupt Response Time

13.1.6.6 IPL Change when Interrupt Request is Acknowledged

When an interrupt request of a maskable interrupt is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt or special interrupt request is acknowledged, the level listed in Table 13.5 is set in the IPL.
Table 13.5 lists the IPL Value When Software or Special Interrupt Is Acknowledged.

Table 13.5 IPL Value When Software or Special Interrupt Is Acknowledged

Interrupt Source	Value Set in IPL
Watchdog timer, voltage monitor 1, voltage monitor 2, comparator 1(1), comparator 2(1), address break	7
Software, address match, single-step	Not changed

NOTE:
1. When non-maskable interrupts is selected.

13.1.6.7 Saving a Register

In the interrupt sequence, the FLG register and PC are saved to the stack.
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved to the stack, the 16 low-order bits in the PC are saved.
Figure 13.7 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers are saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used(1) with a single instruction.

NOTE:
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

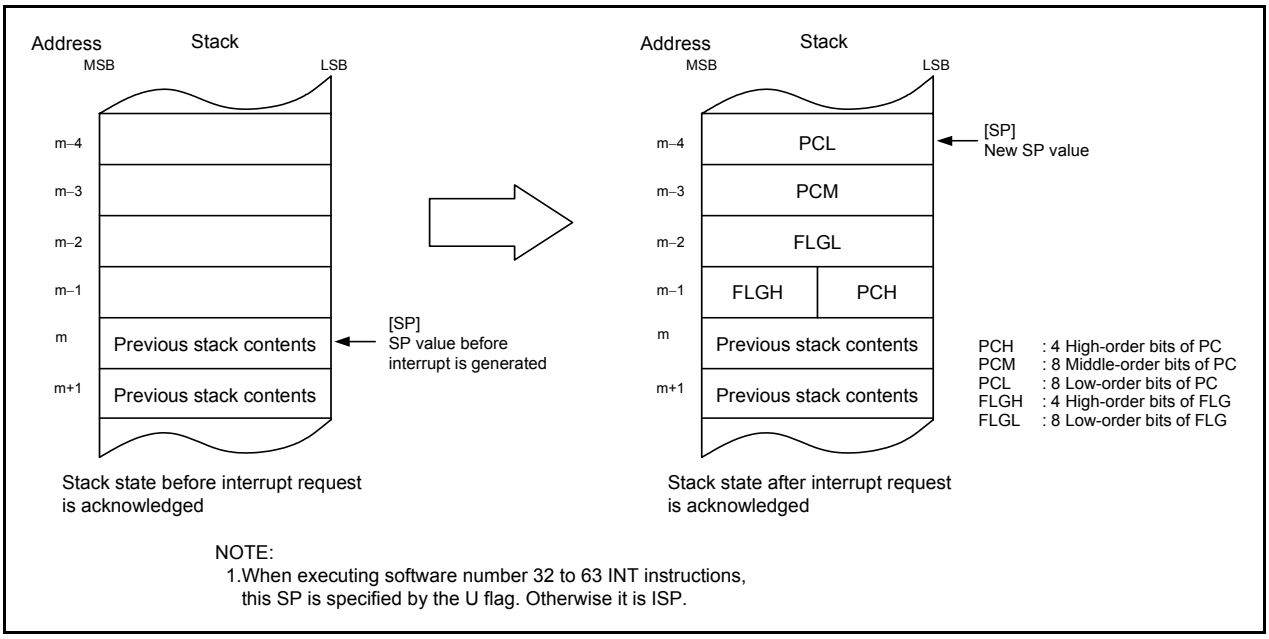


Figure 13.7 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.
Figure 13.8 shows the Register Saving Operation.

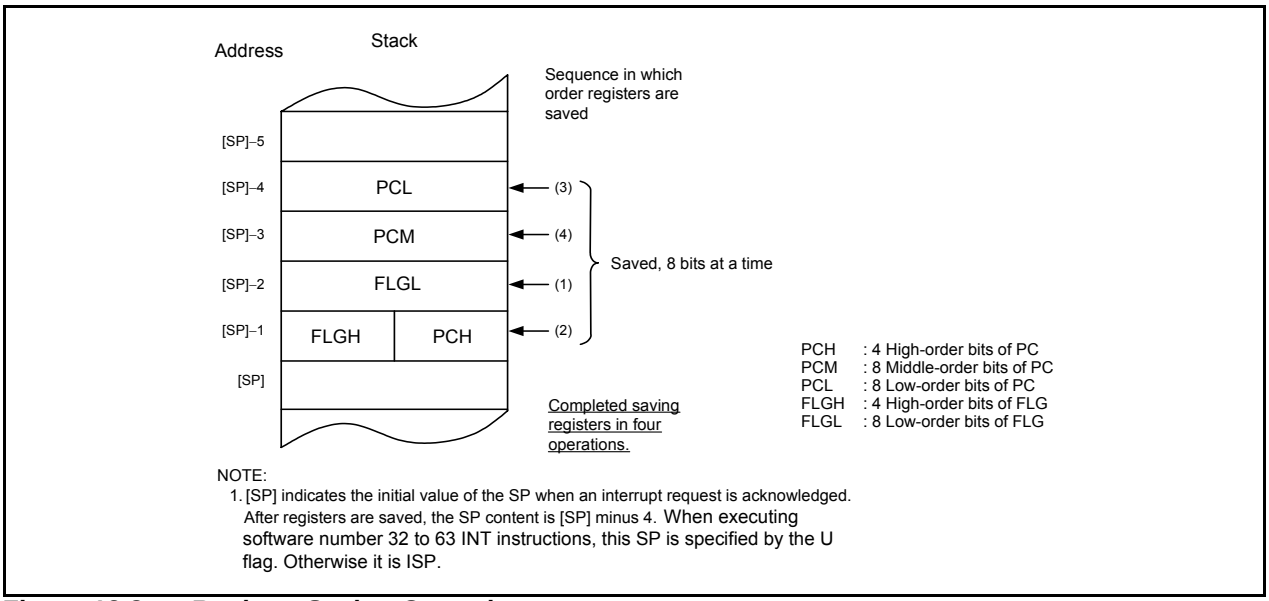


Figure 13.8 Register Saving Operation

13.1.6.8 Returning from an Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved to the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.
Restore registers saved by a program in an interrupt routine using the POPM instruction or others before executing the REIT instruction.

13.1.6.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.
Set bits ILVL2 to ILVL0 to select the desired priority level for maskable interrupts (peripheral functions). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, and the higher priority interrupts acknowledged.
The priority levels of special interrupts, such as reset (reset has the highest priority) and watchdog timer, are set by hardware.
Figure 13.9 shows the Priority Levels of Hardware Interrupts.
The interrupt priority does not affect software interrupts. The MCU jumps to the interrupt routine when the instruction is executed.

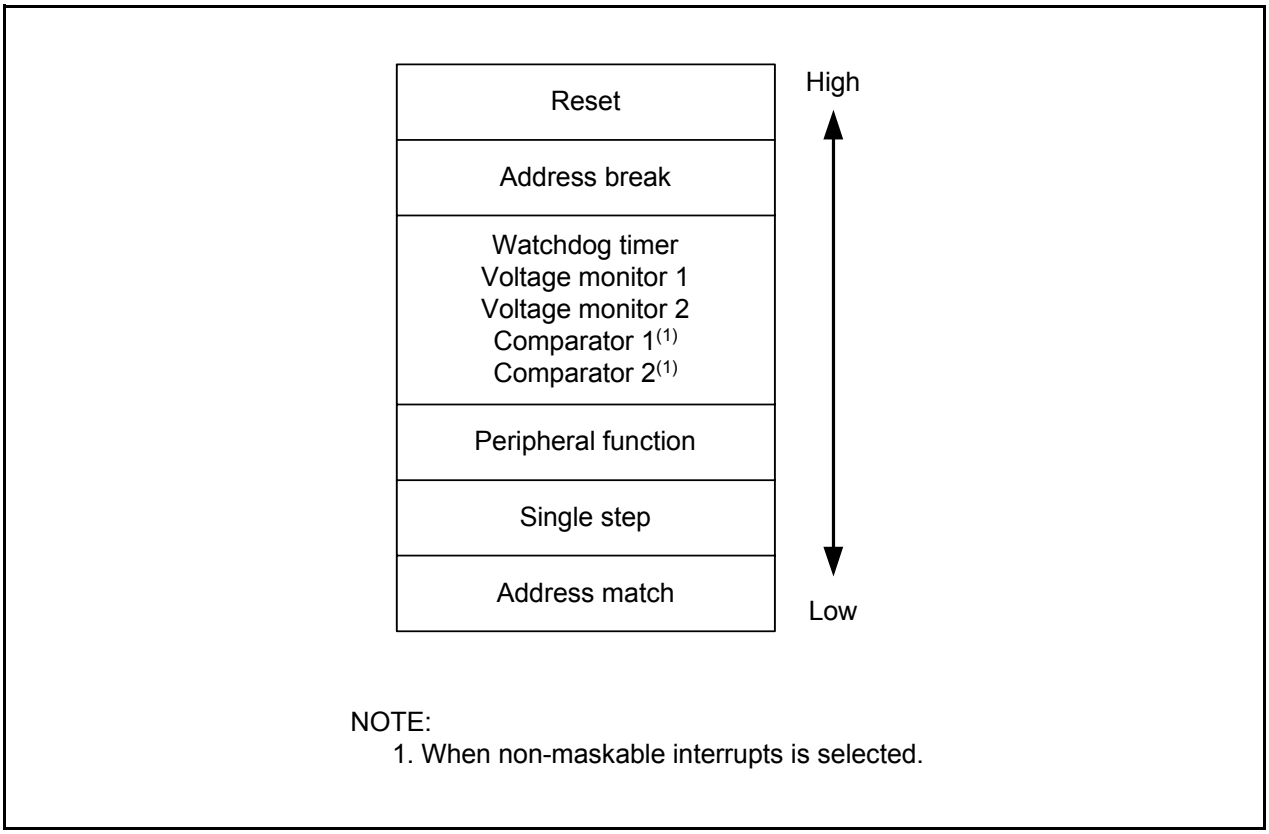


Figure 13.9 Priority Levels of Hardware Interrupts

13.1.6.10 Interrupt Priority Judgement Circuit

The interrupt priority judgement circuit selects the highest priority interrupt, as shown in Figure 13.10.

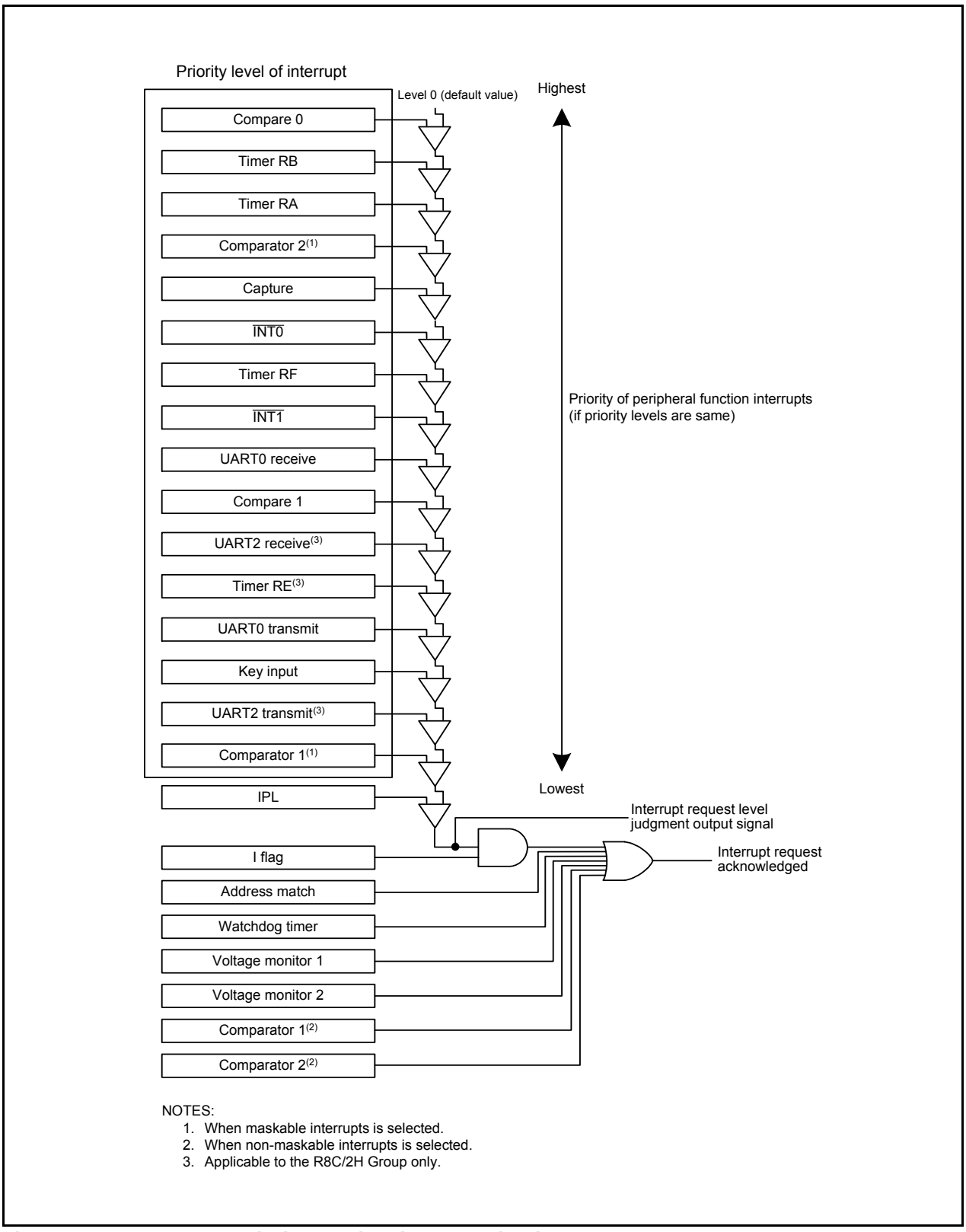


Figure 13.10 Interrupt Priority Level Judgement Circuit

13.2 $\overline{\text{INT}}$ Interrupt

13.2.1 $\overline{\text{INTi}}$ Interrupt (i = 0 or 1)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. Table 13.6 lists the Pin Configuration of $\overline{\text{INT}}$ Interrupt. When using the $\overline{\text{INTi}}$ interrupt, the INTiEN bit in the INTEN register is set to 1 (enable). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register.
Inputs can be passed through a digital filter with three different sampling clocks.
Figure 13.11 shows the INTEN Register. Figure 13.12 shows the INTF Register.

Table 13.6 Pin Configuration of $\overline{\text{INT}}$ Interrupt

Pin name	Input/Output	Function
$\overline{\text{INT0}}$ (P4_5)	Input	$\overline{\text{INT0}}$ interrupt input, Timer RB external trigger input
$\overline{\text{INT1}}$ (P1_5 or P1_7)(1)	Input	$\overline{\text{INT1}}$ interrupt input

NOTE:
1. The $\overline{\text{INT1}}$ pin is selected by the TIOSEL bit in the TRAIOC register. Refer to **8. I/O Ports** for details.

External Input Enable Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

Symbol: INTEN — Address: 00F9h — After Reset: 00h

Bit Symbol	Bit Name	Function	RW
INT0EN	$\overline{\text{INT0}}$ input enable bit	0 : Disable 1 : Enable	RW
INT0PL	$\overline{\text{INT0}}$ input polarity select bit(1, 2)	0 : One edge 1 : Both edges	RW
INT1EN	$\overline{\text{INT1}}$ input enable bit	0 : Disable 1 : Enable	RW
INT1PL	$\overline{\text{INT1}}$ input polarity select bit(1, 2)	0 : One edge 1 : Both edges	RW
— (b7-b4)	Reserved bits	Set to 0.	RW

NOTES:
1. When setting the INTiPL bit (i = 0, 1) to 1 (both edges), set the POL bit in the INTiIC register to 0 (selects falling edge).
2. The IR bit in the INTiIC register may be set to 1 (requests interrupt) when the INTiPL bit is rewritten. Refer to **13.5.4 Changing Interrupt Sources**.

Figure 13.11 INTEN Register

$\overline{\text{INT}}$ Input Filter Select Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0				

Symbol	Address	After Reset
INTF	00FAh	00h

Bit Symbol	Bit Name	Function	RW
INT0F0	$\overline{\text{INT0}}$ input filter select bits	b1 b0 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT0F1			RW
INT1F0	$\overline{\text{INT1}}$ input filter select bits	b3 b2 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
INT1F1			RW
— (b7-b4)	Reserved bits	Set to 0.	RW

Figure 13.12 INTF Register

13.2.2 $\overline{\text{INTi}}$ Input Filter (i = 0 or 1)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected by bits INTiF1 to INTiF0 in the INTF register. The IR bit in the INTiIC register is set to 1 (interrupt requested) when the $\overline{\text{INTi}}$ level is sampled for every sampling clock and the sampled input level matches three times.

Figure 13.13 shows the Configuration of $\overline{\text{INTi}}$ Input Filter. Figure 13.14 shows an Operating Example of $\overline{\text{INTi}}$ Input Filter.

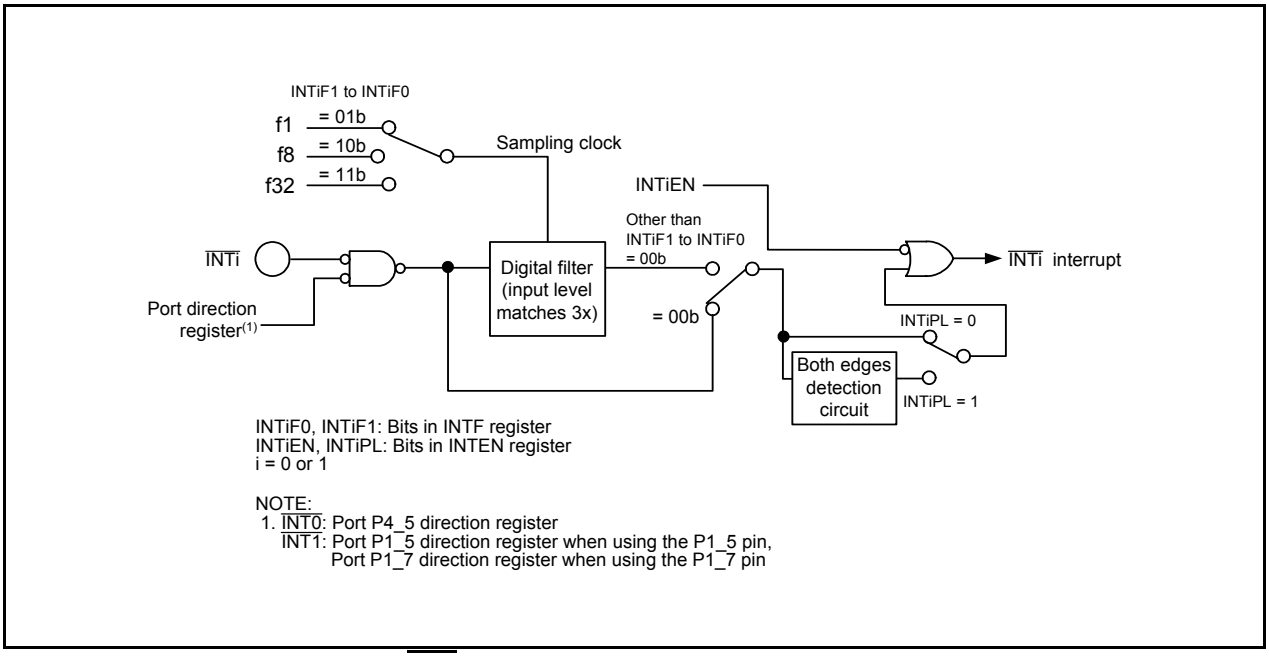


Figure 13.13 Configuration of $\overline{\text{INTi}}$ Input Filter

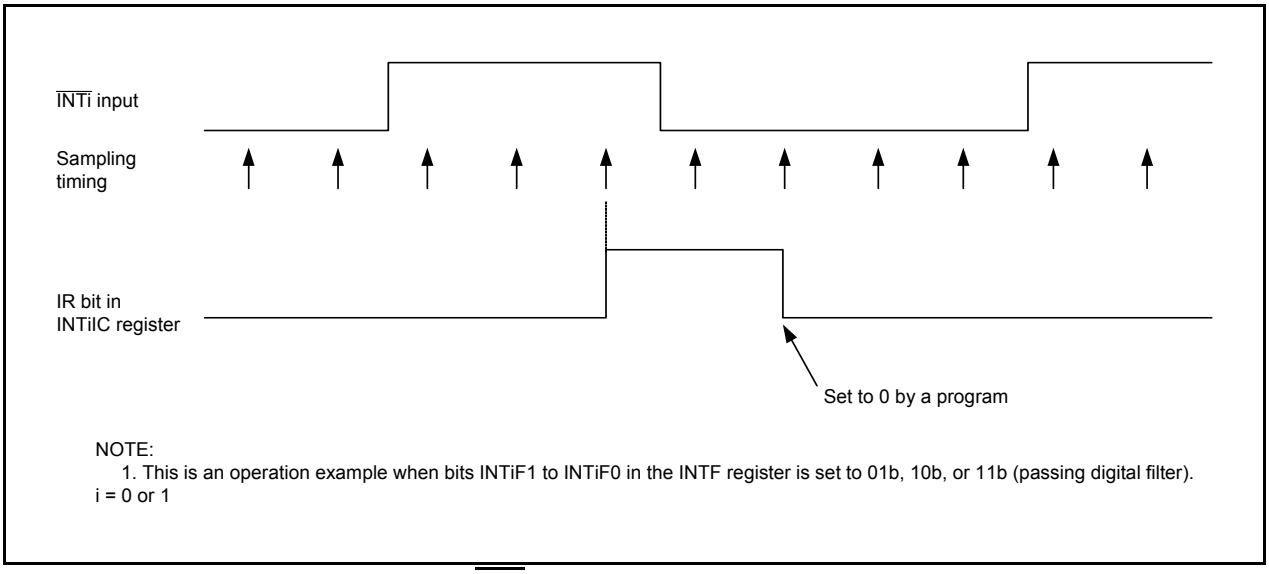


Figure 13.14 Operating Example of $\overline{\text{INTi}}$ Input Filter

13.3 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of the $\overline{K10}$ to $\overline{K13}$ pins. Table 13.7 lists the Pin Configuration of Key Input Interrupt. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN (i = 0 to 3) bit in the KIEN register can select whether the pins are used as $\overline{KIi}$ input. The KIiPL bit in the KIEN register can select the input polarity.

When inputting "L" to the $\overline{KIi}$ pin which sets the KIiPL bit to 0 (falling edge), the input of the other pins $\overline{K10}$ to $\overline{K13}$ is not detected as interrupts. Also, when inputting "H" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), the input of the other pins $\overline{K10}$ to $\overline{K13}$ is not detected as interrupts.

Figure 13.15 shows a Block Diagram of Key Input Interrupt. Figure 13.16 shows the KIEN Register.

Table 13.7 Pin Configuration of Key Input Interrupt

Pin name	Input/Output	Function
$\overline{KI0}$ (P1_0)	Input	$\overline{KI0}$ input
$\overline{KI1}$ (P1_1)	Input	$\overline{KI1}$ input
$\overline{KI2}$ (P1_2)	Input	$\overline{KI2}$ input
$\overline{KI3}$ (P1_3)	Input	$\overline{KI3}$ input

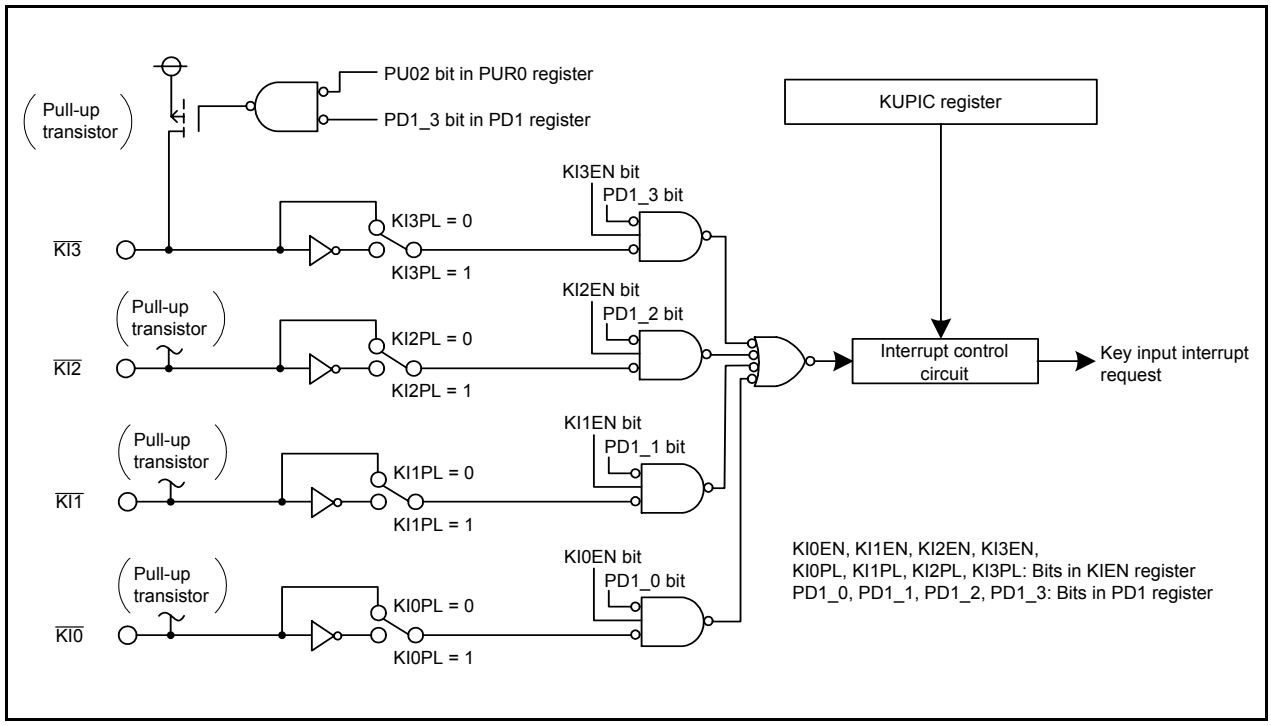


Figure 13.15 Block Diagram of Key Input Interrupt

Key Input Enable Register(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
KIEN	00FBh	00h

Bit Symbol	Bit Name	Function	RW
KI0EN	KI0 input enable bit	0 : Disable 1 : Enable	RW
KI0PL	KI0 input polarity select bit	0 : Falling edge 1 : Rising edge	RW
KI1EN	KI1 input enable bit	0 : Disable 1 : Enable	RW
KI1PL	KI1 input polarity select bit	0 : Falling edge 1 : Rising edge	RW
KI2EN	KI2 input enable bit	0 : Disable 1 : Enable	RW
KI2PL	KI2 input polarity select bit	0 : Falling edge 1 : Rising edge	RW
KI3EN	KI3 input enable bit	0 : Disable 1 : Enable	RW
KI3PL	KI3 input polarity select bit	0 : Falling edge 1 : Rising edge	RW

NOTE:
1. The IR bit in the KUPIC register may be set to 1 (requests interrupt) when the KIEN register is rewritten. Refer to **13.5.4 Changing Interrupt Sources**.

Figure 13.16 KIEN Register

13.4 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi register (i = 0 or 1). This interrupt is used as a break function by the debugger. When using the on-chip debugger, do not set an address match interrupt (registers of AIER, RMAD0, and RMAD1 and fixed vector tables) in a user system.

Set the starting address of any instruction in the RMADi register. Bits AIER0 and AIER1 in the AIER0 register can be used to select enable or disable of the interrupt. The I flag and IPL do not affect the address match interrupt.
The value of the PC (refer to **13.1.6.7 Saving a Register** for the value of the PC) which is saved to the stack when an address match interrupt is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, return by one of the following means:

- Change the content of the stack and use the REIT instruction.
- Use an instruction such as POP to restore the stack as it was before the interrupt request was acknowledged. Then use a jump instruction.

Table 13.8 lists the Values of PC Saved to Stack when Address Match Interrupt is Acknowledged. Table 13.9 lists the Correspondence Between Address Match Interrupt Sources and Associated Registers.
Figure 13.17 shows Registers AIER and RMAD0 to RMAD1.

Table 13.8 Values of PC Saved to Stack when Address Match Interrupt is Acknowledged

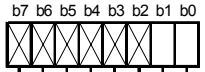
Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved(1)
• Instruction with 2-byte operation code(2) • Instruction with 1-byte operation code(2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
Instructions other than the above	Address indicated by RMADi register + 1

NOTES:
1. Refer to the **13.1.6.7 Saving a Register** for the PC value saved.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual (REJ09B0001)**. **Chapter 4. Instruction Code/Number of Cycles** contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 13.9 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER0	RMAD0
Address match interrupt 1	AIER1	RMAD1

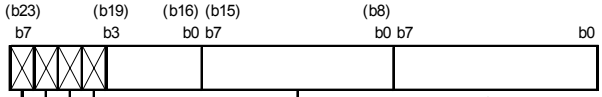
Address Match Interrupt Enable Register



Symbol	Address	After Reset
AIER	0013h	00h

Bit Symbol	Bit Name	Function	RW
AIER0	Address match interrupt 0 enable bit	0 : Disable 1 : Enable	RW
AIER1	Address match interrupt 1 enable bit	0 : Disable 1 : Enable	RW
— (b7-b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Address Match Interrupt Register i (i = 0 or 1)



Symbol	Address	After Reset
RMAD0	0012h-0010h	000000h
RMAD1	0016h-0014h	000000h

Function	Setting Range	RW
Address setting register for address match interrupt	00000h to FFFFFh	RW
— (b7-b4): Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 13.17 Registers AIER and RMAD0 to RMAD1

13.5 Notes on Interrupts

13.5.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the acknowledged interrupt IR bit is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

13.5.2 SP Setting

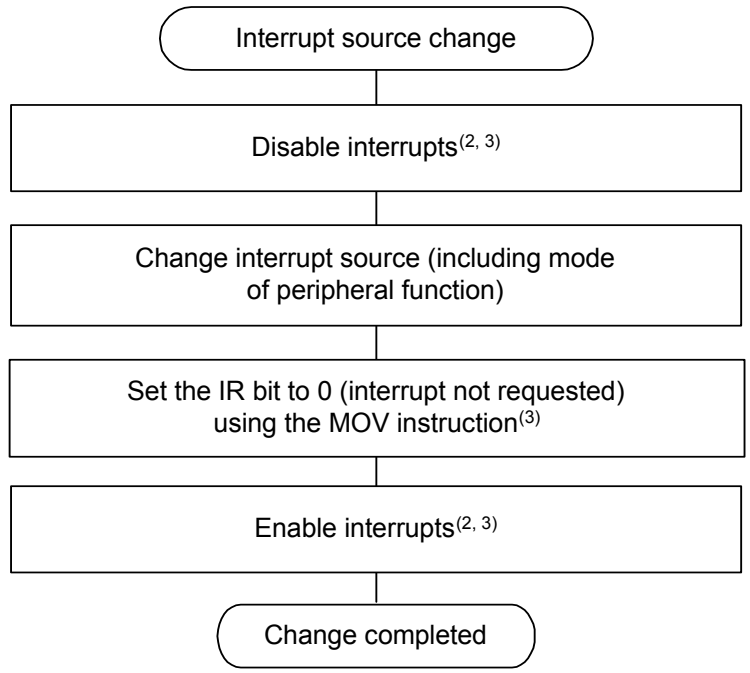
Set any value in the SP before an interrupt is acknowledged. The SP is set to 0000h after reset. Therefore, if an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

13.5.3 External Interrupt and Key Input Interrupt

Either "L" level or an "H" level of width shown in the Electrical Characteristics is necessary for the signal input to pins $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 22.17** (VCC = 5V), **Table 22.23** (VCC = 3V), **Table 22.29** (VCC = 2.2V), **Table 22.45** (VCC = 5V), **Table 22.50** (VCC = 3V), and **Table 22.55** (VCC = 2.2V) **External Interrupt $\overline{\text{INTi}}$ (i = 0 or 1) Input**.

13.5.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. When using an interrupt, set the IR bit to 0 (no interrupt requested) after changing the interrupt source. In addition, changes of interrupt sources include all factors that change the interrupt sources assigned to individual software interrupt numbers, polarities, and timing. Therefore, if a mode change of a peripheral function involves interrupt sources, edge polarities, and timing, set the IR bit to 0 (no interrupt requested) after the change. Refer to the individual peripheral function for its related interrupts.
Figure 13.18 shows an Example of Procedure for Changing Interrupt Sources.



IR bit: The interrupt control register bit of an interrupt whose source is changed.

NOTES:
1. Execute the above settings individually. Do not execute two or more settings at once (by one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled. If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 of the interrupt whose source is changed.
3. Refer to **13.5.5 Changing Interrupt Control Register Contents** for the instructions to be used and usage notes.

Figure 13.18 Example of Procedure for Changing Interrupt Sources

13.5.5 Changing Interrupt Control Register Contents

(a) The contents of an interrupt control register can only be changed while no interrupt requests corresponding to that register are generated. If interrupt requests may be generated, disable interrupts before changing the interrupt control register contents.

(b) When changing the contents of an interrupt control register after disabling interrupts, be careful to choose appropriate instructions.
Changing any bit other than IR bit
If an interrupt request corresponding to a register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt request may be ignored. If this causes a problem, use the following instructions to change the register: AND, OR, BCLR, BSET
Changing IR bit
If the IR bit is set to 0 (interrupt not requested), it may not be set to 0 depending on the instruction used. Therefore, use the MOV instruction to set the IR bit to 0.

(c) When disabling interrupts using the I flag, set the I flag as shown in the sample programs below. Refer to (b) regarding changing the contents of interrupt control registers by the sample programs.

Sample programs 1 to 3 are for preventing the I flag from being set to 1 (interrupts enabled) before the interrupt control register is changed for reasons of the internal bus or the instruction queue buffer.

Example 1: Use NOP instructions to prevent I flag from being set to 1 before interrupt control register is changed

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use dummy read to delay FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use POPC instruction to change I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

14. ID Code Areas

14.1 Overview

The ID code areas are used to implement a function that prevents the flash memory from being rewritten in standard serial I/O mode. This function prevents the flash memory from read, rewritten, or erased.
The ID code areas are assigned to 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh of the respective vector highest-order addresses of the fixed vector table. Figure 14.1 shows the ID Code Areas.

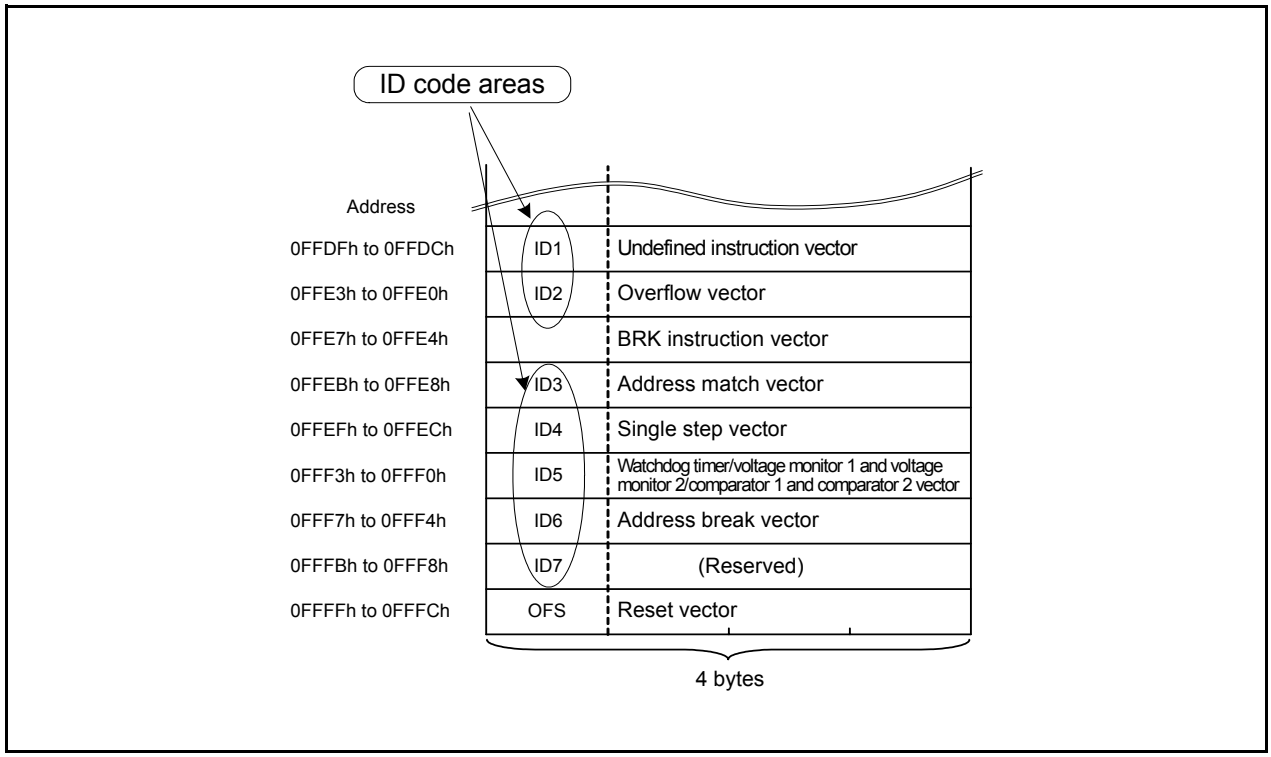


Figure 14.1 ID Code Areas

14.2 Functions

The ID code areas are used in standard serial I/O mode. Unless 3 bytes (addresses from 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes stored in the ID code areas and the ID codes sent from the serial programmer or the on-chip debugging emulator are checked to see if they match. If the ID codes match, the commands sent from the serial programmer or the on-chip debugging emulator are acknowledged. If the ID codes do not match, the commands are not acknowledged. To use the serial programmer or the on-chip debugging simulator, first write predetermined ID codes to the ID code areas.
As the ID code areas are allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program.

14.3 Notes on ID Code Areas

14.3.1 Setting Example of ID Code Areas

As the ID code areas are allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

15. Option Function Select Area

15.1 Overview

The option function select area is used to select the MCU state after reset or the function to prevent rewriting in parallel I/O mode. The reset vector highest-order-address, 0FFFFh, is assigned as the option function select area. Figure 15.1 shows the Option Function Select Area.

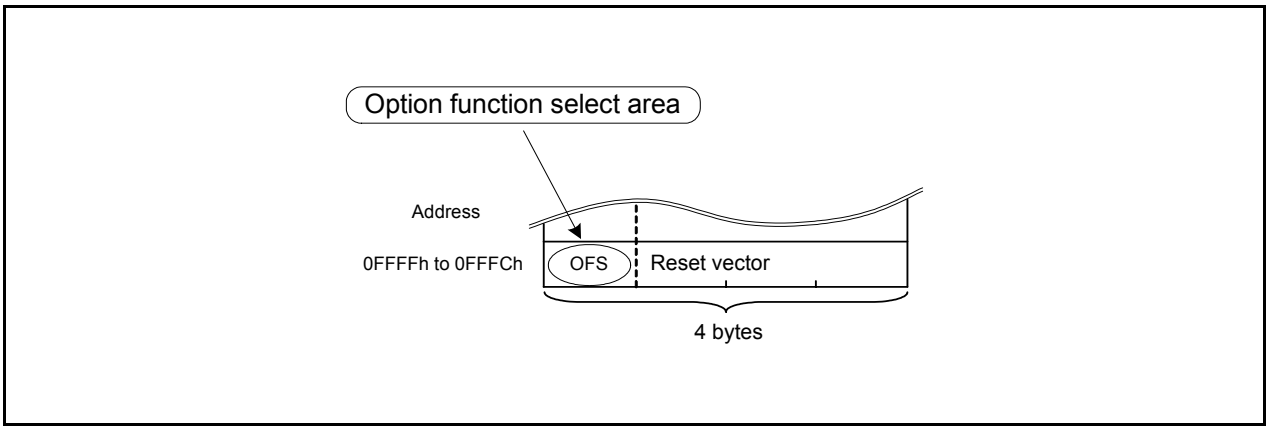


Figure 15.1 Option Function Select Area

15.2 OFS Register

The OFS register is used to select the MCU state after reset or the function to prevent rewriting in parallel I/O mode. Figure 15.2 shows the OFS Register.

Option Function Select Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
	1		1			1	

Symbol: OFS | Address: 0FFFFh | When Shipping: FFh(3)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b4)	Reserved bit	Set to 1.	RW
LVD0ON	Voltage detection 0 circuit start bit(2)	0 : Voltage monitor 0 reset enabled after hardware reset 1 : Voltage monitor 0 reset disabled after hardware reset	RW
— (b6)	Reserved bit	Set to 1.	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. Setting the LVD0ON bit is only valid after a hardware reset. To use the power-on reset, set the LVD0ON bit to 0 (voltage monitor 0 reset enabled after hardware reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Figure 15.2 OFS Register

15.3 Notes on Option Function Select Area

15.3.1 Setting Example of Option Function Select Area

As the option function select area is allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)      ; RESET
```

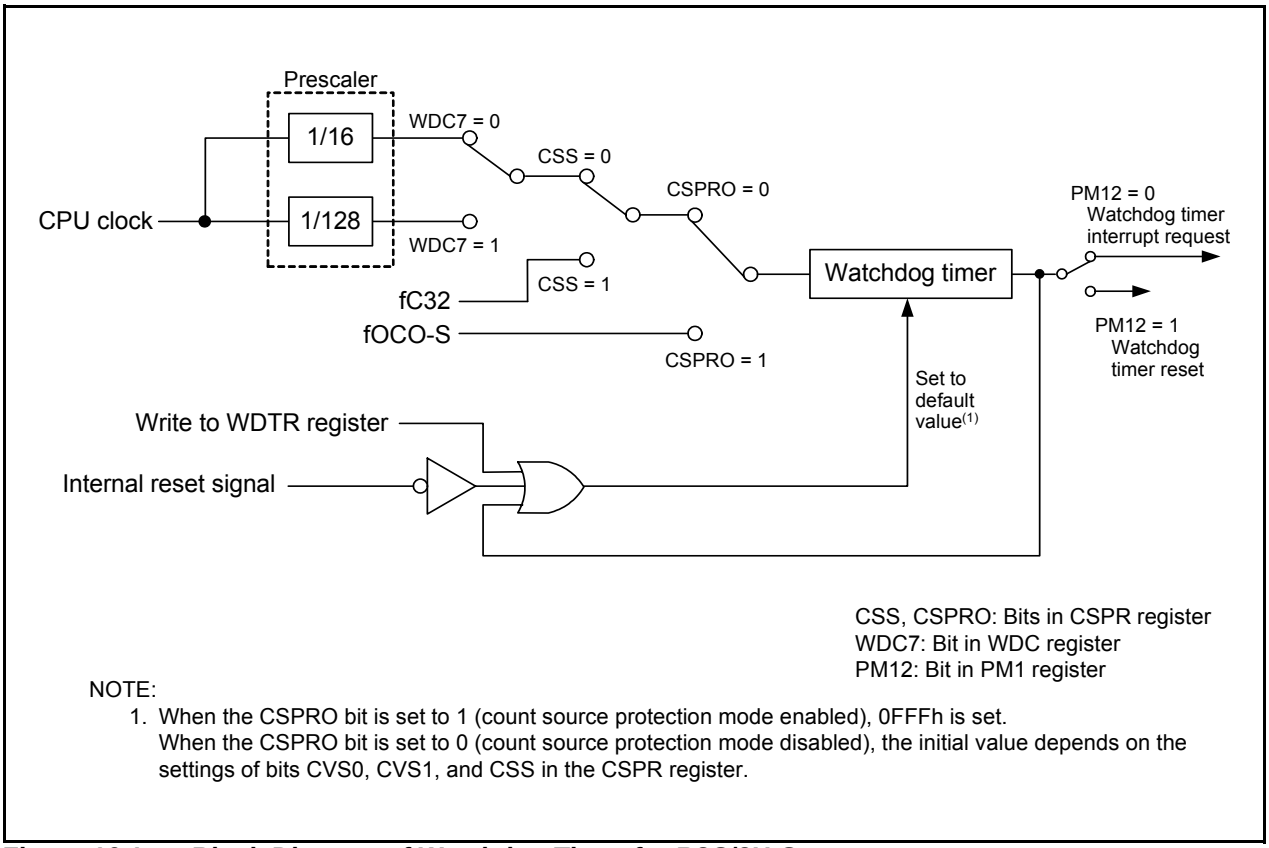
(Programming formats vary depending on the compiler. Check the compiler manual.)

16. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system. The watchdog timer contains a 15-bit counter and allows selection of count source protection mode enable or disable.
Table 16.1 lists information on the Watchdog Timer Specifications for R8C/2H Group and Table 16.2 lists information on the Watchdog Timer Specifications for R8C/2J Group.
Refer to **5.6 Watchdog Timer Reset** for details on the watchdog timer.
Figure 16.1 shows the Block Diagram of Watchdog Timer for R8C/2H Group and Figure 16.2 shows the Block Diagram of Watchdog Timer for R8C/2J Group. Figure 16.3 shows the Registers WDTR, and WDTS. Figure 16.4 shows the WDC Register. Figure 16.5 shows the CSPR Register. Figure 16.6 shows the OFS Register.

Table 16.1 Watchdog Timer Specifications for R8C/2H Group

Item	Count Source Protection Mode Disabled		Count Source Protection Mode Enabled
Count source	CPU clock	XCIN clock divided by 32 (fC32)	Low-speed on-chip oscillator clock
Count operation	Decrement		
Count start condition	Either of the following can be selected • After reset, count starts automatically • Count starts by writing to WDTS register		
Count stop condition	Stop mode, wait mode	Stop mode	None
Reset condition of watchdog timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow		
Operation at the time of underflow	Watchdog timer interrupt or watchdog timer reset		Watchdog timer reset
Select functions	• Division ratio of prescaler (when select the CPU clock as the count source) Selected by the WDC7 bit in the WDC register • The default value of the watchdog timer (when select fC32 as the count source) Selected by bits CVS0 to CVS1 in the CSPR register • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Starts or stops of the watchdog timer after a reset Selected by the WDTON bit in the OFS register (flash memory).		

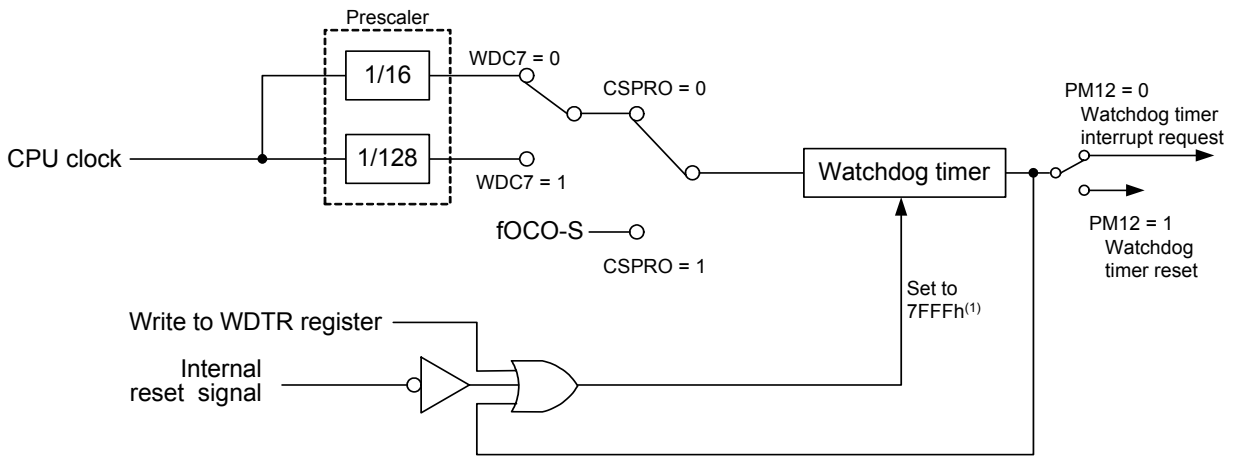


NOTE:
1. When the CSPRO bit is set to 1 (count source protection mode enabled), 0FFFh is set.
When the CSPRO bit is set to 0 (count source protection mode disabled), the initial value depends on the settings of bits CVS0, CVS1, and CSS in the CSPR register.

Figure 16.1 Block Diagram of Watchdog Timer for R8C/2H Group

Table 16.2 Watchdog Timer Specifications for R8C/2J Group

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock
Count operation	Decrement	
Count start condition	Either of the following can be selected • After reset, count starts automatically • Count starts by writing to WDTS register	
Count stop condition	Stop mode, wait mode	None
Reset condition of watchdog timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow	
Operation at the time of underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Select functions	• Division ratio of prescaler (when select the CPU clock as the count source) Selected by the WDC7 bit in the WDC register • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Starts or stops of the watchdog timer after a reset Selected by the WDTON bit in the OFS register (flash memory).	



NOTE:
1. When the CSPRO bit is set to 1 (count source protection mode enabled), 0FFFh is set.

Figure 16.2 Block Diagram of Watchdog Timer for R8C/2J Group

Watchdog Timer Reset Register (R8C/2H Group)

b7 b0

Symbol	Address	After Reset
WDTR	000Dh	Undefined

Function	RW
When 00h is written before writing FFh, the watchdog timer is reset.(1) The watchdog timer initial value depends on the CSPR register setting.	WO

CSPR register				Default value
CSPRO	CSS	CVS1	CVS0	
0	0	X	X	7FFFh
0	1	0	0	01FFh
0	1	0	1	03FFh
0	1	1	0	07FFh
0	1	1	1	0FFFh
1(2)	X	X	X	0FFFh

X: 0 or 1

NOTES:
1. Do not generate an interrupt between when 00h and FFh are written.
2. When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled), 0FFFh is set in the watchdog timer.

Watchdog Timer Reset Register (R8C/2J Group)

b7 b0

Symbol	Address	After Reset
WDTR	000Dh	Undefined

Function	RW
When 00h is written before writing FFh, the watchdog timer is reset.(1) The default value of the watchdog timer is 7FFFh when count source protection mode is disabled and 0FFFh when count source protection mode is enabled.(2)	WO

NOTES:
1. Do not generate an interrupt between when 00h and FFh are written.
2. When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled), 0FFFh is set in the watchdog timer.

Watchdog Timer Start Register

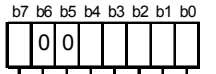
b7 b0

Symbol	Address	After Reset
WDTS	000Eh	Undefined

Function	RW
The watchdog timer starts counting after a write instruction to this register.	WO

Figure 16.3 Registers WDTR, and WDTS

Watchdog Timer Control Register

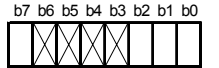


Symbol	Address	After Reset
WDC	000Fh	00X11111b

Bit Symbol	Bit Name	Function	RW
— (b4-b0)	High-order bits of watchdog timer		RO
— (b5)	Reserved bit	Set to 0. When read, the content is undefined.	RW
— (b6)	Reserved bit	Set to 0.	RW
WDC7	Prescaler select bit	0 : Divide-by-16 1 : Divide-by-128	RW

Figure 16.4 WDC Register

Count Source Protection Mode Register (R8C/2H Group)

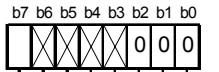


Symbol	Address	After Reset(1)
CSPR	001Ch	00h

Bit Symbol	Bit Name	Function	RW
CVS0	Watchdog timer default value select bit(2)	b1 b0 0 0 : 01FFh (512) 0 1 : 03FFh (1024) 1 0 : 07FFh (2048) 1 1 : 0FFFh (4096)	RW
CVS1			RW
CSS	Count source select bit(3)	0 : CPU clock 1 : fC32	RW
— (b6-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
CSPRO	Count source protection mode select bit(4)	0 : Count source protection mode disabled 1 : Count source protection mode enabled	RW

NOTES:
1. When 0 is written to the CSPROINI bit in the OFS register, the value after reset is 10000000b.
2. When the CSS bit is set to 1 (fC32), Bits CVS0 to CVS1 are enabled.
3. When the CSPRO bit is set to 0 (count source protection mode disabled), the CSS bit is enabled.
4. Write 0 before writing 1 to set the CSPRO bit to 1. 0 cannot be set by a program.

Count Source Protection Mode Register (R8C/2J Group)



Symbol	Address	After Reset(1)
CSPR	001Ch	00h

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved Bits	Set to 0.	RW
— (b6-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		RW
CSPRO	Count Source Protection Mode Select Bit(2)	0 : Count source protection mode disabled 1 : Count source protection mode enabled	RW

NOTES:
1. When 0 is written to the CSPROINI bit in the OFS register, the value after reset is 10000000b.
2. Write 0 before writing 1 to set the CSPRO bit to 1.
   0 cannot be set by a program.

Figure 16.5 CSPR Register

Option Function Select Register[1]

b7	b6	b5	b4	b3	b2	b1	b0
	1		1			1	

Symbol: OFS | Address: 0FFFFh | When Shipping: FFh[3]

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b4)	Reserved bit	Set to 1.	RW
LVD0ON	Voltage detection 0 circuit start bit[2]	0 : Voltage monitor 0 reset enabled after hardware reset 1 : Voltage monitor 0 reset disabled after hardware reset	RW
— (b6)	Reserved bit	Set to 1.	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. Setting the LVD0ON bit is only valid after a hardware reset. To use the power-on reset, set the LVD0ON bit to 0 (voltage monitor 0 reset enabled after hardware reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Figure 16.6 OFS Register

16.1 Count Source Protection Mode Disabled (R8C/2H Group)

The count source of the watchdog timer is either the CPU clock or the XCIN clock divided by 32 (fC32) can be selected when count source protection mode for the R8C/2H Group is disabled. fC32 does not stop in wait mode, the watchdog timer to count continues.
Table 16.3 lists the Watchdog Timer Specifications (with Count Source Protection Mode Disabled) for R8C/2H Group.

Table 16.3 Watchdog Timer Specifications (with Count Source Protection Mode Disabled) for R8C/2H Group

Item	Specification	
Count source	CPU clock	XCIN clock divided by 32 (fC32)
Count operation	Decrement	
Period	$\frac{\text{Division ratio of prescaler (n)}}{\text{CPU clock}} \times$ count value of watchdog timer (32768)(1, 2) n: 16 or 128 (selected by WDC7 bit in WDC register) Example: When the CPU clock frequency is 8 MHz and prescaler divided by 16, the period is approximately 65.5 ms	$\frac{32}{\text{XCIN clock}} \times$ count value of watchdog timer (m)(1) m: 512, 1024, 2048 or 4096 (selected by bits CVS0 to CVS1 in the CSPR register) Example: When the XCIN clock frequency is 32.768 kHz and the count value by 512, the period is 0.5 s
Reset condition of watchdog timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow	
Count start condition	The WDTON bit(3) in the OFS register (0FFFFh) selects the operation of the watchdog timer after a reset • When the WDTON bit is set to 1 (watchdog timer is in stop state after reset) The watchdog timer and prescaler stop after a reset and the count starts when the WDTS register is written to • When the WDTON bit is set to 0 (watchdog timer starts automatically after exiting) The watchdog timer and prescaler start counting automatically after a reset	
Count stop condition	Stop and wait modes (inherit the count from the held value after exiting modes)	Stop mode (inherit the count from the held value after exiting modes)
Operation at time of underflow	• When the PM12 bit in the PM1 register is set to 0 Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1 Watchdog timer reset (refer to **5.6 Watchdog Timer Reset**)	

NOTES:
1. The watchdog timer is reset when 00h is written to the WDTR register before FFh.
2. The prescaler is reset after the MCU is reset. Some errors in the period of the watchdog timer may be caused by the prescaler.
3. The WDTON bit cannot be changed by a program. To set the WDTON bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.

16.2 Count Source Protection Mode Disabled (R8C/2J Group)

The count source of the watchdog timer is the CPU clock when count source protection mode for the R8C/2J Group is disabled.
Table 16.4 lists the Watchdog Timer Specifications (with Count Source Protection Mode Disabled) for R8C/2J Group.

Table 16.4 Watchdog Timer Specifications (with Count Source Protection Mode Disabled) for R8C/2J Group

Item	Specification
Count source	CPU clock
Count operation	Decrement
Period	Division ratio of prescaler (n) × count value of watchdog timer (32768)(1) CPU clock n: 16 or 128 (selected by WDC7 bit in WDC register) Example: When the CPU clock frequency is 8 MHz and prescaler divides by 16, the period is approximately 65.5 ms
Reset condition of watchdog timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow
Count start condition	The WDTON bit(2) in the OFS register (0FFFFh) selects the operation of the watchdog timer after a reset • When the WDTON bit is set to 1 (watchdog timer is in stop state after reset) The watchdog timer and prescaler stop after a reset and the count starts when the WDTS register is written to • When the WDTON bit is set to 0 (watchdog timer starts automatically after exiting) The watchdog timer and prescaler start counting automatically after a reset
Count stop condition	Stop and wait modes (inherit the count from the held value after exiting modes)
Operation at time of underflow	• When the PM12 bit in the PM1 register is set to 0 Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1 Watchdog timer reset (refer to **5.6 Watchdog Timer Reset**)

NOTES:
1. The watchdog timer is reset when 00h is written to the WDTR register before FFh. The prescaler is reset after the MCU is reset. Some errors in the period of the watchdog timer may be caused by the prescaler.
2. The WDTON bit cannot be changed by a program. To set the WDTON bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.

16.3 Count Source Protection Mode Enabled

The count source of the watchdog timer is the low-speed on-chip oscillator clock when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.
Table 16.5 lists the Watchdog Timer Specifications (with Count Source Protection Mode Enabled).

Table 16.5 Watchdog Timer Specifications (with Count Source Protection Mode Enabled)

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	Count value of watchdog timer (4096) Low-speed on-chip oscillator clock Example: Period is approximately 32.8 ms when the low-speed on-chip oscillator clock frequency is 125 kHz
Reset condition of watchdog timer	• Reset • Write 00h to the WDTR register before writing FFh • Underflow
Count start condition	The WDTON bit(1) in the OFS register (0FFFFh) selects the operation of the watchdog timer after a reset. • When the WDTON bit is set to 1 (watchdog timer is in stop state after reset) The watchdog timer and prescaler stop after a reset and the count starts when the WDTS register is written to • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset) The watchdog timer and prescaler start counting automatically after a reset
Count stop condition	None (The count does not stop in wait mode after the count starts. The MCU does not enter stop mode.)
Operation at time of underflow	Watchdog timer reset (refer to **5.6 Watchdog Timer Reset**)
Registers, bits	• When setting the CSPPRO bit in the CSPR register to 1 (count source protection mode is enabled)(2), the following are set automatically - Set 0FFFh to the watchdog timer - Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on) - Set the PM12 bit in the PM1 register to 1 (The watchdog timer is reset when watchdog timer underflows) • The following conditions apply in count source protection mode - Writing to the CM10 bit in the CM1 register is disabled (It remains unchanged even if it is set to 1. The MCU does not enter stop mode.) - Writing to the CM14 bit in the CM1 register is disabled (It remains unchanged even if it is set to 1. The low-speed on-chip oscillator does not stop.)

NOTES:
1. The WDTON bit cannot be changed by a program. To set the WDTON bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. To set the CSPROINI bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.

17. Timers

The MCU has two 8-bit timers with 8-bit prescalers and one 16-bit timer. Additionally, a timer with a 4-bit counter and an 8-bit counter are implemented in the R8C/2H Group. The two 8-bit timers with 8-bit prescalers are timer RA and timer RB. These timers contain a reload register to store the default value of the counter. The one 16-bit timer is timer RF and have input capture and output compare functions. The 4-bit and 8-bit counters in the R8C/2H Group compose timer RE, which has an output compare function. All the timers operate independently.
Table 17.1 lists Functional Comparison of Timers.

Table 17.1 Functional Comparison of Timers

Item		Timer RA	Timer RB	Timer RE(2)	Timer RF
Configuration		8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	4-bit counter 8-bit counter	16-bit timer (with input capture and output compare)
Count		Decrement	Decrement	Increment	Increment
Count sources		• f1 • f2 • f8 • fOCO • fC32(3)	• f1 • f2 • f8 • Timer RA underflow	• f4 • f8 • f32 • fC4	• f1 • f8 • f32
Function	Count of the internal count source	Timer mode	Timer mode	—	Output compare mode
	Count of the external count source	Event counter mode	—	—	—
	External pulse width/ period measurement	Pulse width measurement mode, pulse period measurement mode	—	—	Input capture mode
	PWM output	Pulse output mode(1), Event counter mode(1)	Programmable waveform generation mode	Output compare mode(1)	Output compare mode
	One-shot waveform output	—	Programmable one-shot generation mode, Programmable wait one-shot generation mode	—	—
	Timer	Timer mode (only fC32 count)	—	Real-time clock mode	—
Input pin		TRAIO	$\overline{\text{INT0}}$	—	TRFI
Output pin		TRAO TRAIO	TRBO	—	TRFO00 to TRFO02, TRFO10 to TRFO11
Related interrupt		Timer RA interrupt, $\overline{\text{INT1}}$ interrupt	Timer RB interrupt, $\overline{\text{INT0}}$ interrupt	Timer RE interrupt	Timer RF interrupt, Compare 0 interrupt, Compare 1 interrupt, Capture interrupt
Timer stop		Provided	Provided	Provided	Provided

NOTES:
1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.
2. Implemented in the R8C/2H Group only.
3. Available in the R8C/2H Group only.

17.1 Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.
The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA (refer to **Tables 17.2 to 17.6 the Specifications of Each Mode**).
The count source for timer RA is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 17.1 shows a Block Diagram of Timer RA. Figures 17.2 and 17.3 show the registers associated with timer RA.

Timer RA has the following five operating modes:

- Timer mode: The timer counts the internal count source.
- Pulse output mode: The timer counts the internal count source and outputs pulses of which polarity inverted by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

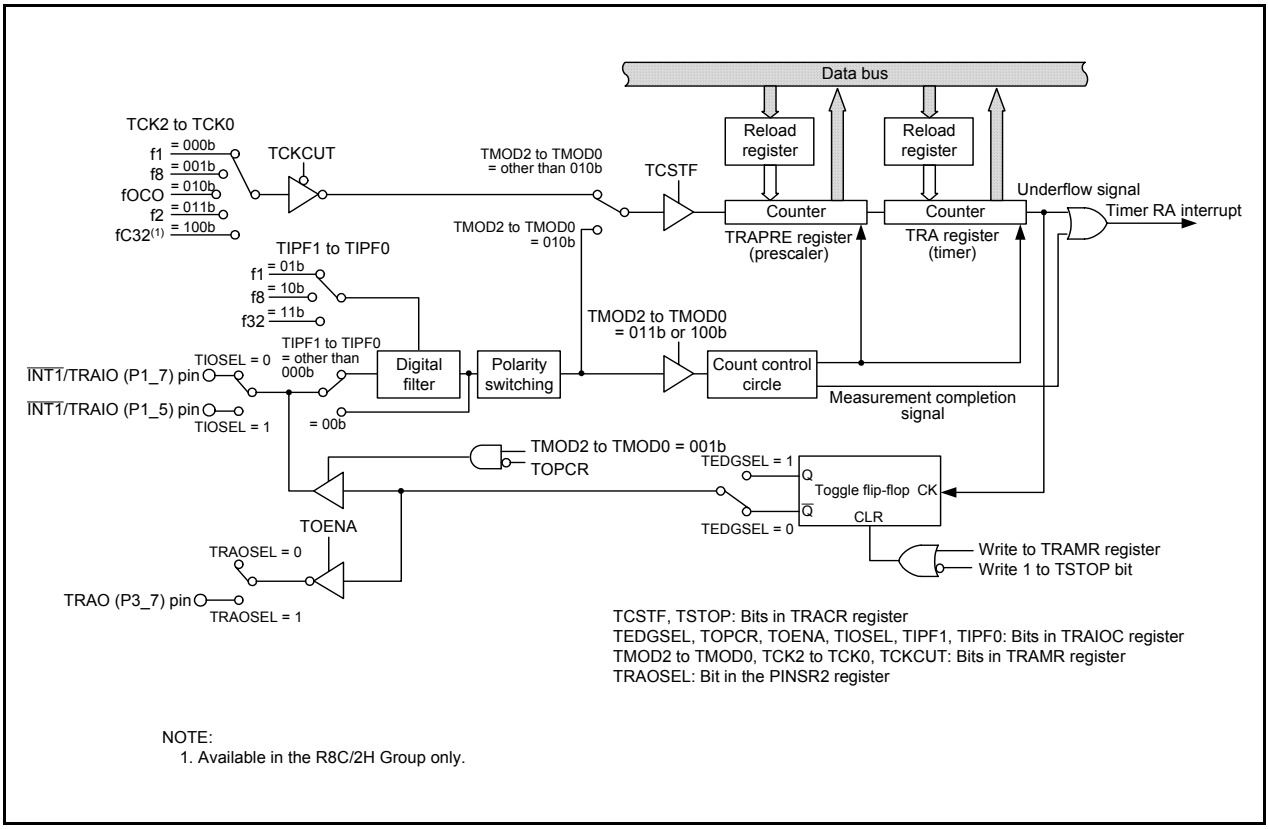
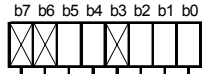


Figure 17.1 Block Diagram of Timer RA

Timer RA Control Register(4)

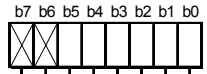


Symbol	Address	After Reset
TRACR	0100h	00h

Bit Symbol	Bit Name	Function	RW
TSTART	Timer RA count start bit(1)	0 : Count stops 1 : Count starts	RW
TCSTF	Timer RA count status flag(1)	0 : Count stops 1 : During count	RO
TSTOP	Timer RA count forcible stop bit(2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TEDGF	Active edge judgment flag(3, 5)	0 : Active edge not received 1 : Active edge received (end of measurement period)	RW
TUNDF	Timer RA underflow flag(3, 5)	0 : No underflow 1 : Underflow	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Refer to **17.1.6 Notes on Timer RA**.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TRAPRE and TRA are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.
5. Set to 0 in timer mode, pulse output mode, and event counter mode.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	Function varies depending on operating mode.	RW
TOPCR	TRAIO output control bit		RW
TOENA	TRAO output enable bit		RW
TIOSEL	INT1/TRAIO select bit		RW
TIPF0 TIPF1	TRAIO input filter select bits		RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 17.2 Registers TRACR and TRAIOC

Timer RA Mode Register(1)

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRAMR	0102h	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Timer RA operating mode select bits	b2 b1 b0 0 0 0 : Timer mode 0 0 1 : Pulse output mode 0 1 0 : Event counter mode 0 1 1 : Pulse w idth measurement mode 1 0 0 : Pulse period measurement mode 1 0 1 : 1 1 0 : Do not set. 1 1 1 :	RW
TMOD1			RW
TMOD2			RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCK0	Timer RA count source select bits	b6 b5 b4 0 0 0 : f1 0 0 1 : f8 0 1 0 : fOCO 0 1 1 : f2 1 0 0 : fC32(2) 1 0 1 : 1 1 0 : Do not set. 1 1 1 :	RW
TCK1			RW
TCK2			RW
TCKCUT	Timer RA count source cutoff bit	0 : Provides count source 1 : Cuts off count source	RW

NOTES:
1. When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rew rite this register.
2. Do not set in the R8C/2J Group.

Timer RA Prescaler Register

b7 b0

Symbol	Address	After Reset
TRAPRE	0103h	FFh(1)

Mode	Function	Setting Range	RW
Timer mode	Counts an internal count source	00h to FFh	RW
Pulse output mode	Counts an internal count source	00h to FFh	RW
Event counter mode	Counts an external count source	00h to FFh	RW
Pulse w idth measurement mode	Counts internal count source	00h to FFh	RW
Pulse period measurement mode		00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

Timer RA Register

b7 b0

Symbol	Address	After Reset
TRA	0104h	FFh(1)

Mode	Function	Setting Range	RW
All modes	Counts on underflow of timer RA prescaler register	00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRACR register is set to 1, the TRA register is set to FFh.

Figure 17.3 Registers TRAMR, TRAPRE, and TRA

17.1.1 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 17.2 Timer Mode Specifications**).
Figure 17.4 shows TRAIOC Register in Timer Mode.

Table 17.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32(1)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
$\overline{\text{INT1}}$/TRAIO pin function	Programmable I/O port, or $\overline{\text{INT1}}$ interrupt input
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.1.1.1 Timer Write Control during Count Operation**).

NOTE:
1. Available in the R8C/2H Group only.

Timer RA I/O Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	0	0		0	0	0

Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	RW
TOPCR	TRAIO output control bit		RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0 TIPF1	TRAIO input filter select bits	Set to 0 in timer mode.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 17.4 TRAIOC Register in Timer Mode

17.1.1.1 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed.

Figure 17.5 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.

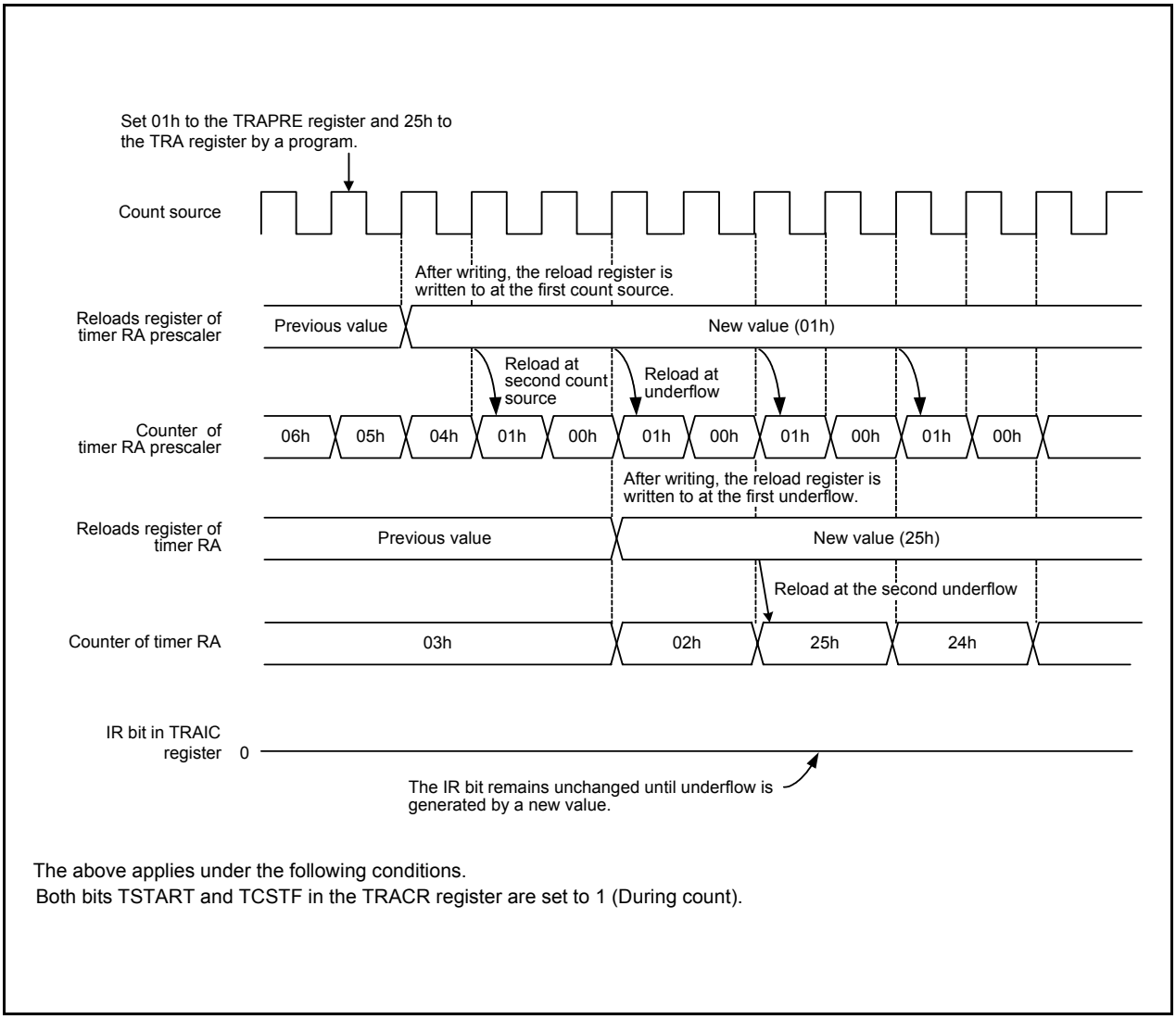


Figure 17.5 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

17.1.2 Pulse Output Mode

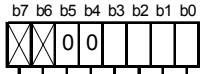
In pulse output mode, the internally generated count source is counted, and a pulse with inverted polarity is output from the TRAIO pin each time the timer underflows (refer to **Table 17.3 Pulse Output Mode Specifications**).
Figure 17.6 shows TRAIOC Register in Pulse Output Mode.

Table 17.3 Pulse Output Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32(2)
Count operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
$\overline{\text{INT1}}$/TRAIO pin function	Pulse output, programmable output port, or $\overline{\text{INT1}}$ interrupt(1)
TRAO pin function	Programmable I/O port or inverted output of TRAIO(1)
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.1.1.1 Timer Write Control during Count Operation**).
Select functions	• TRAIO output polarity switch function The TEDGSEL bit in the TRAIOC register selects the level at the start of pulse output.(1) • TRAO output function Pulses inverted from the TRAIO output polarity can be output from the TRAO pin (selectable by the TOENA bit in the TRAIOC register). • TRAO pin select function P3_7 is selected by the TRAOSEL bit in the PINSR2 register. • Pulse output stop function Output from the TRAIO pin is stopped by the TOPCR bit in the TRAIOC register. • $\overline{\text{INT1}}$/TRAIO pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register.

NOTES:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.
2. Available in the R8C/2H Group only.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : TRAIO output starts at "H" 1 : TRAIO output starts at "L"	RW
TOPCR	TRAIO output control bit	0 : TRAIO output 1 : Port P1_7 or P1_5	RW
TOENA	TRAO output enable bit	0 : Port P3_7 1 : TRAO output (inverted TRAIO output from P3_7)	RW
TIOSEL	$\overline{\text{INT1}}$/TRAIO select bit	0 : $\overline{\text{INT1}}$/TRAIO pin (P1_7) 1 : $\overline{\text{INT1}}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits	Set to 0 in pulse output mode.	RW
TIPF1			RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 17.6 TRAIOC Register in Pulse Output Mode

17.1.3 Event Counter Mode

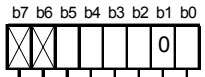
In event counter mode, external signal inputs to the $\overline{\text{INT1}}$/TRAIO pin are counted (refer to **Table 17.4 Event Counter Mode Specifications**).
Figure 17.7 shows TRAIOC Register in Event Counter Mode.

Table 17.4 Event Counter Mode Specifications

Item	Specification
Count source	External signal which is input to TRAIO pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: setting value of TRAPRE register, m: setting value of TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt].
$\overline{\text{INT1}}$/TRAIO pin function	Count source input ($\overline{\text{INT1}}$ interrupt input)
TRAO pin function	Programmable I/O port or pulse output(1)
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.1.1.1 Timer Write Control during Count Operation**).
Select functions	• $\overline{\text{NT1}}$ input polarity switch function The TEDGSEL bit in the TRAIOC register selects the active edge of the count source. • Count source input pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register. • Pulse output function Pulses of inverted polarity can be output from the TRAO pin each time the timer underflows (selectable by the TOENA bit in the TRAIOC register).(1) • TRAO pin select function P3_7 is selected by the TRAOSEL bit in the PINSR2 register. • Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.

NOTE:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : Starts counting at rising edge of the TRAIO input or TRAIO starts output at "L" 1 : Starts counting at falling edge of the TRAIO input or TRAIO starts output at "H"	RW
TOPCR	TRAIO output control bit	Set to 0 in event counter mode.	RW
TOENA	TRAO output enable bit	0 : Port P3_7 1 : TRAO output	RW
TIOSEL	$\overline{INT1}$/TRAIO select bit	0 : $\overline{INT1}$/TRAIO pin (P1_7) 1 : $\overline{INT1}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits(1)	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

Figure 17.7 TRAIOC Register in Event Counter Mode

17.1.4 Pulse Width Measurement Mode

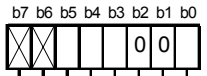
In pulse width measurement mode, the pulse width of an external signal input to the $\overline{\text{INT1}}$/TRAIO pin is measured (refer to **Table 17.5 Pulse Width Measurement Mode Specifications**).
Figure 17.8 shows TRAIOC Register in Pulse Width Measurement Mode and Figure 17.9 shows an Operating Example of Pulse Width Measurement Mode.

Table 17.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32(1)
Count operations	• Decrement • Continuously counts the selected signal only when measurement pulse is “H” level, or conversely only “L” level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
$\overline{\text{INT1}}$/TRAIO pin function	Measured pulse input ($\overline{\text{INT1}}$ interrupt input)
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.1.1.1 Timer Write Control during Count Operation**).
Select functions	• Measurement level select • The TEDGSEL bit in the TRAIOC register selects the “H” or “L” level period. • Measured pulse input pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register. • Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.

NOTE:
1. Available in the R8C/2H Group only.

Timer RA I/O Control Register



Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : TRAIO input starts at "L" 1 : TRAIO input starts at "H"	RW
TOPCR	TRAIO output control bit	Set to 0 in pulse width measurement mode.	RW
TOENA	TRAO output enable bit		RW
TIOSEL	$\overline{INT1}$/TRAIO select bit	0 : $\overline{INT1}$/TRAIO pin (P1_7) 1 : $\overline{INT1}$/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits(1)	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

Figure 17.8 TRAIOC Register in Pulse Width Measurement Mode

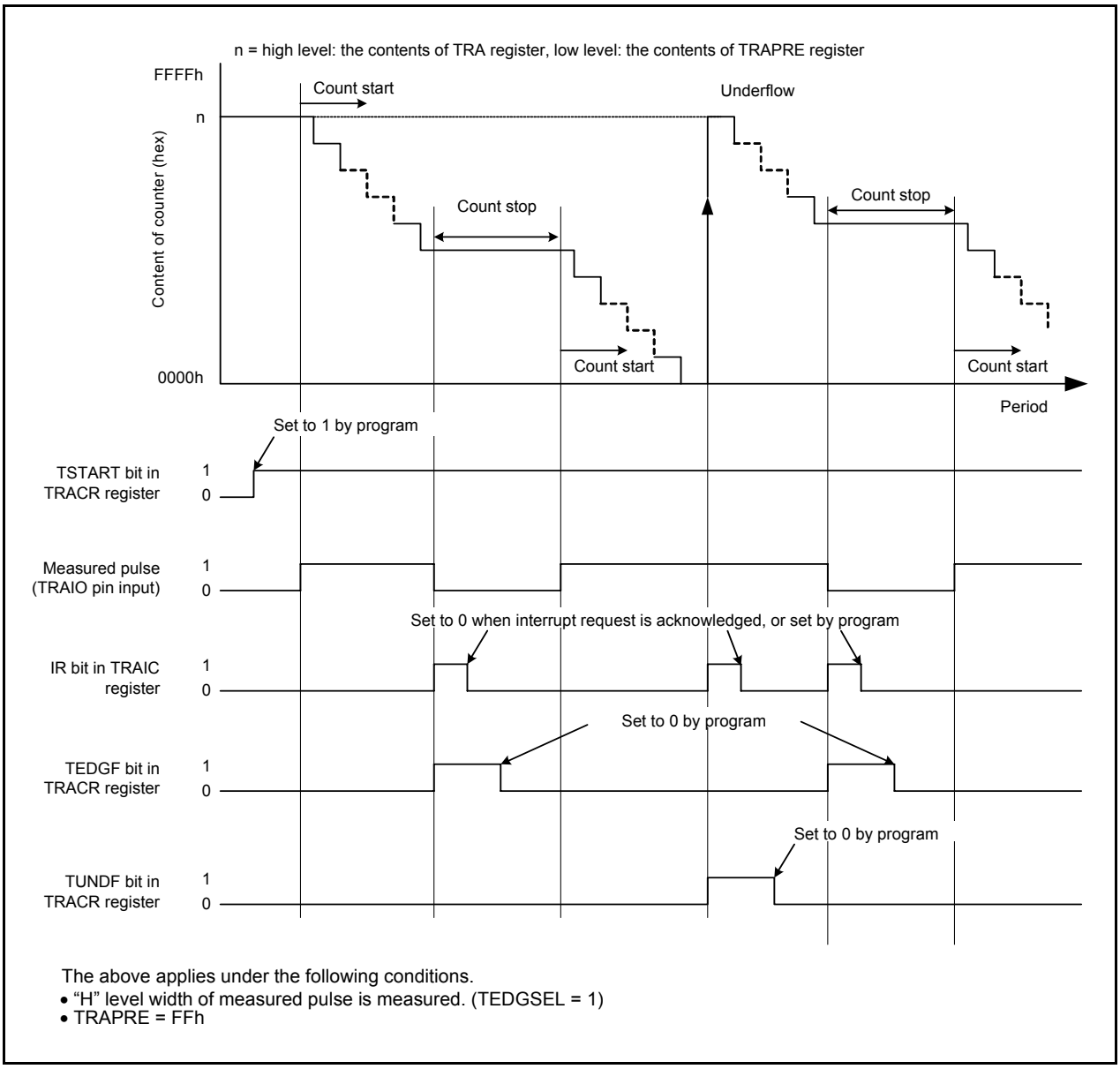


Figure 17.9 Operating Example of Pulse Width Measurement Mode

17.1.5 Pulse Period Measurement Mode

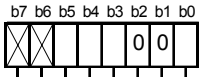
In pulse period measurement mode, the pulse period of an external signal input to the $\overline{\text{INT1}}$/TRAIO pin is measured (refer to **Table 17.6 Pulse Period Measurement Mode Specifications**).
Figure 17.10 shows TRAIOC Register in Pulse Period Measurement Mode and Figure 17.11 shows an Operating Example of Pulse Period Measurement Mode.

Table 17.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32(2)
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents in the reload register at the second underflow of timer RA prescaler and continues counting.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows or reloads [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
$\overline{\text{INT1}}$/TRAIO pin function	Measured pulse input(1) ($\overline{\text{INT1}}$ interrupt input)
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.1.1.1 Timer Write Control during Count Operation**).
Select functions	• Measurement period select The TEDGSEL bit in the TRAIOC register selects the measurement period of the input pulse. • Measured pulse input pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAIOC register. • Digital filter function Bits TIPF0 and TIPF1 in the TRAIOC register enable or disable the digital filter and select the sampling frequency.

NOTES:
1. Input a pulse with a period longer than twice the timer RA prescaler period. Input a pulse with a longer “H” and “L” width than the timer RA prescaler period. If a pulse with a shorter period is input to the TRAIO pin, the input may be ignored.
2. Available in the R8C/2H Group only.

Timer RA I/O Control Register

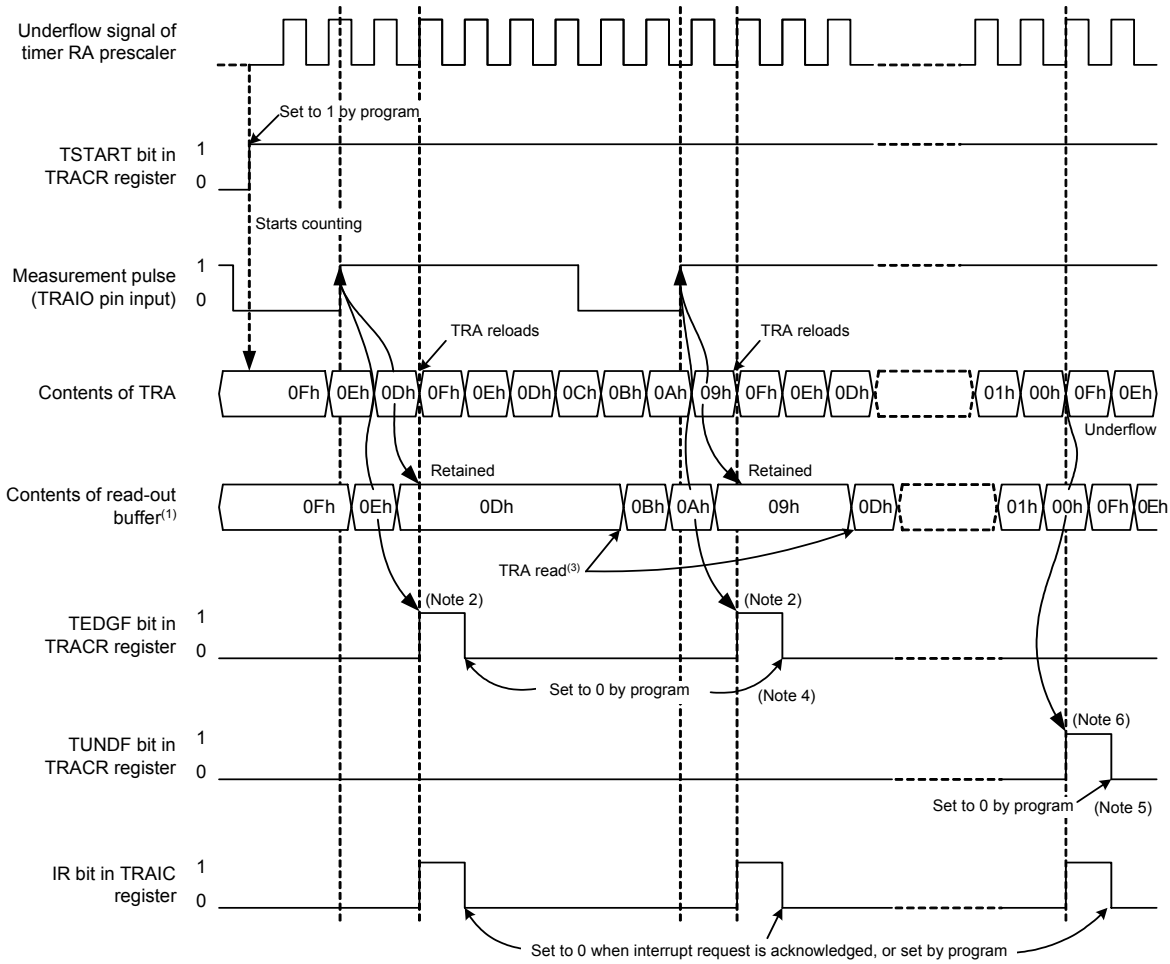


Symbol	Address	After Reset
TRAIOC	0101h	00h

Bit Symbol	Bit Name	Function	RW
TEDGSEL	TRAIO polarity switch bit	0 : Measures measurement pulse from one rising edge to next rising edge 1 : Measures measurement pulse from one falling edge to next falling edge	RW
TOPCR	TRAIO output control bit	Set to 0 in pulse period measurement mode.	RW
TOENA	TRAO output enable bit		RW
TIOSEL	INT1/TRAIO select bit	0 : INT1/TRAIO pin (P1_7) 1 : INT1/TRAIO pin (P1_5)	RW
TIPF0	TRAIO input filter select bits(1)	b5 b4 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

Figure 17.10 TRAIOC Register in Pulse Period Measurement Mode



Conditions: The period from one rising edge to the next rising edge of the measured pulse is measured (TEDGSEL = 0) with the default value of the TRA register as 0Fh.

NOTES:
1. The contents of the read-out buffer can be read by reading the TRA register in pulse period measurement mode.
2. After an active edge of the measured pulse is input, the TEDGF bit in the TRACR register is set to 1 (active edge found) when the timer RA prescaler underflows for the second time.
3. The TRA register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge found). The contents in the read-out buffer are retained until the TRA register is read. If the TRA register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRACR register. At the same time, write 1 to the TUNDF bit in the TRACR register.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit. At the same time, write 1 to the TEDGF bit.
6. Bits TUNDF and TEDGF are both set to 1 if timer RA underflows and reloads on an active edge simultaneously.

Figure 17.11 Operating Example of Pulse Period Measurement Mode

17.1.6 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count).

  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

17.2 Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.
The prescaler and timer each consist of a reload register and counter (refer to **Tables 17.7 to 17.10 the Specifications of Each Mode**). Timer RB has timer RB primary and timer RB secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 17.12 shows a Block Diagram of Timer RB. Figures 17.13 to 17.15 show the registers associated with timer RB.

Timer RB has four operation modes listed as follows:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.

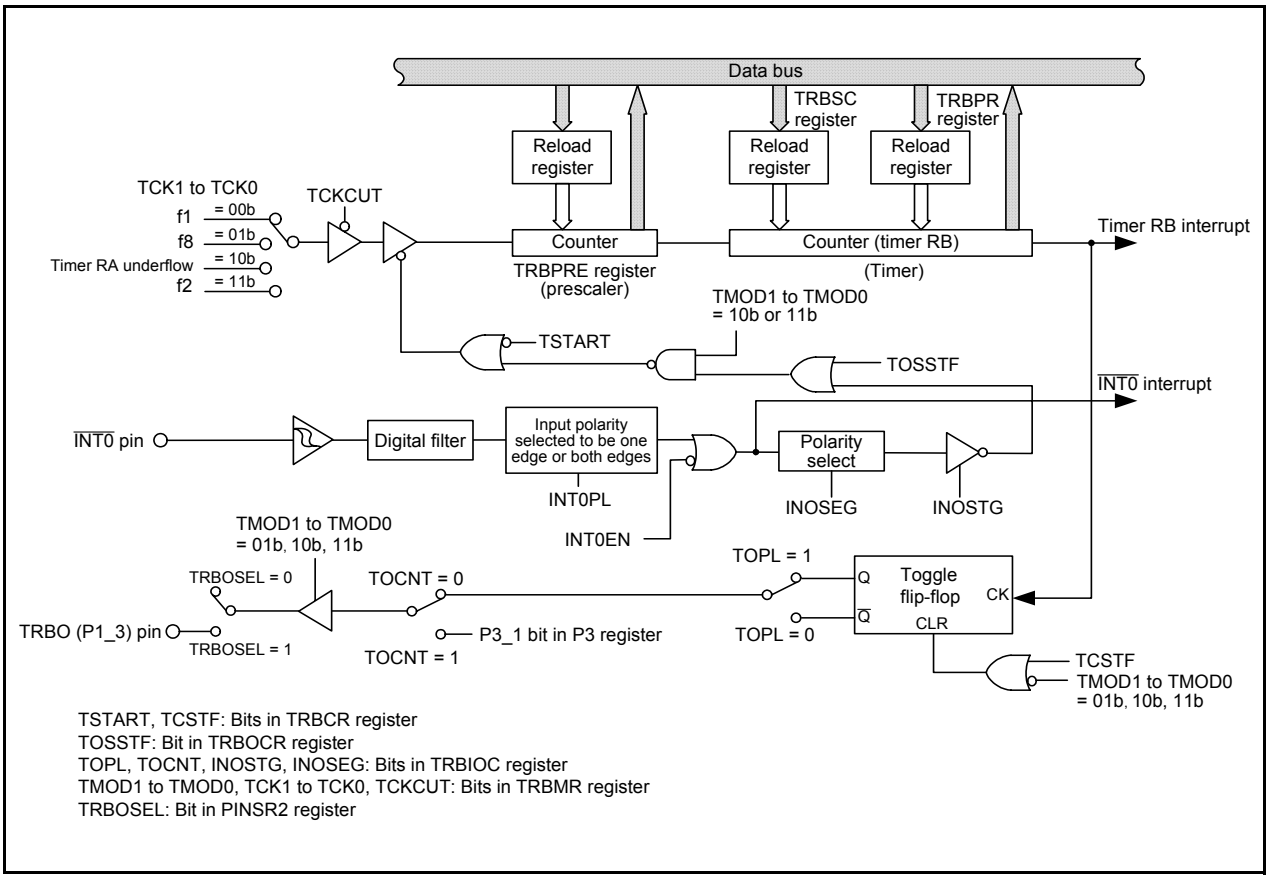
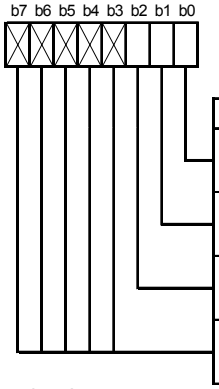


Figure 17.12 Block Diagram of Timer RB

Timer RB Control Register

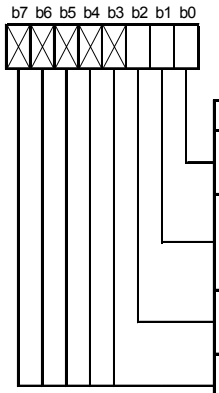


Symbol	Address	After Reset
TRBCR	0108h	00h

Bit Symbol	Bit Name	Function	RW
TSTART	Timer RB count start bit(1)	0 : Count stops 1 : Count starts	RW
TCSTF	Timer RB count status flag(1)	0 : Count stops 1 : During count(3)	RO
TSTOP	Timer RB count forcible stop bit(1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	RW
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Refer to **17.2.5 Notes on Timer RB** for precautions regarding bits TSTART, TCSTF and TSTOP.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable w aveform mode. In programmable one-shot generation mode or programmable w ait one-shot generation mode, indicates that a one-shot pulse trigger has been acknow ledged.

Timer RB One-Shot Control Register(2)



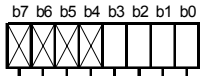
Symbol	Address	After Reset
TRBOCR	0109h	00h

Bit Symbol	Bit Name	Function	RW
TOSST	Timer RB one-shot start bit	When this bit is set to 1, one-shot trigger generated. When read, its content is 0.	RW
TOSSP	Timer RB one-shot stop bit	When this bit is set to 1, counting of one-shot pulses (including programmable w ait one-shot pulses) stops. When read, its content is 0.	RW
TOSSTF	Timer RB one-shot status flag(1)	0 : One-shot stopped 1 : One-shot operating (Including w ait period)	RO
— (b7-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. When 1 is set to the TSTOP bit in the TRBCR register, the TOSSTF bit is set to 0.
2. This register is enabled w hen bits TMOD1 to TMOD0 in the TRBMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable w ait one-shot generation mode).

Figure 17.13 Registers TRBCR and TRBOCR

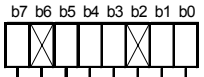
Timer RB I/O Control Register



Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	Function varies depending on operating mode.	RW
TOCNT	Timer RB output switch bit		RW
INOSTG	One-shot trigger control bit		RW
INOSEG	One-shot trigger polarity select bit		RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Timer RB Mode Register



Symbol	Address	After Reset
TRBMR	010Bh	00h

Bit Symbol	Bit Name	Function	RW
TMOD0	Timer RB operating mode select bits(1)	b1 b0 0 0 : Timer mode 0 1 : Programmable waveform generation mode 1 0 : Programmable one-shot generation mode 1 1 : Programmable wait one-shot generation mode	RW
TMOD1			RW
— (b2)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TWRC	Timer RB write control bit(2)	0 : Write to reload register and counter 1 : Write to reload register only	RW
TCK0	Timer RB count source select bits(1)	b5 b4 0 0 : f1 0 1 : f8 1 0 : Timer RA underflow 1 1 : f2	RW
TCK1			RW
— (b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCKCUT	Timer RB count source cutoff bit(1)	0 : Provides count source 1 : Cuts off count source	RW

NOTES:
1. Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).

Figure 17.14 Registers TRBIOC and TRBMR

Timer RB Prescaler Register(1)

b7 b0

Symbol	Address	After Reset
TRBPRE	010Ch	FFh

Mode	Function	Setting Range	RW
Timer mode	Counts an internal count source or timer RA underflows	00h to FFh	RW
Programmable waveform generation mode		00h to FFh	RW
Programmable one-shot generation mode		00h to FFh	RW
Programmable wait one-shot generation mode		00h to FFh	RW

NOTE:
1. When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

Timer RB Secondary Register(3, 4)

b7 b0

Symbol	Address	After Reset
TRBSC	010Dh	FFh

Mode	Function	Setting Range	RW
Timer mode	Disabled	00h to FFh	—
Programmable waveform generation mode	Counts timer RB prescaler underflows(1)	00h to FFh	WO(2)
Programmable one-shot generation mode	Disabled	00h to FFh	—
Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	WO(2)

NOTES:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. The count value can be read out by reading the TRBPR register even when the secondary period is being counted.
3. When the TSTOP bit in the TRBCR register is set to 1, the TRBSC register is set to FFh.
4. To write to the TRBSC register, perform the following steps.
   (1) Write the value to the TRBSC register.
   (2) Write the value to the TRBPR register. (If the value does not change, write the same value second time.)

Timer RB Primary Register(2)

b7 b0

Symbol	Address	After Reset
TRBPR	010Eh	FFh

Mode	Function	Setting Range	RW
Timer mode	Counts timer RB prescaler underflows	00h to FFh	RW
Programmable waveform generation mode	Counts timer RB prescaler underflows(1)	00h to FFh	RW
Programmable one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	RW
Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (wait period width is counted)	00h to FFh	RW

NOTES:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. When the TSTOP bit in the TRBCR register is set to 1, the TRBPR register is set to FFh.

Figure 17.15 Registers TRBPRE, TRBSC, and TRBPR

17.2.1 Timer Mode

In timer mode, a count source which is internally generated or timer RA underflows are counted (refer to **Table 17.7 Timer Mode Specifications**). Registers TRBOCR and TRBSC are not used in timer mode.
Figure 17.16 shows TRBIOC Register in Timer Mode.

Table 17.7 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register contents before the count continues (when timer RB underflows, the contents of timer RB primary reload register is reloaded).
Divide ratio	1/(n+1)(m+1) n: setting value in TRBPRE register, m: setting value in TRBPR register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	When timer RB underflows [timer RB interrupt].
TRBO pin function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written to while count operation is in progress: If the TWRC bit in the TRBMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only. (Refer to **17.2.1.1 Timer Write Control during Count Operation**.)

Timer RB I/O Control Register

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	0	0	0	0

Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	Set to 0 in timer mode.	RW
TOCNT	Timer RB output sw itch bit		RW
INOSTG	One-shot trigger control bit		RW
INOSEG	One-shot trigger polarity select bit		RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 17.16 TRBIOC Register in Timer Mode

17.2.1.1 Timer Write Control during Count Operation

Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. In addition, if the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted if the prescaler value changes. Figure 17.17 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.

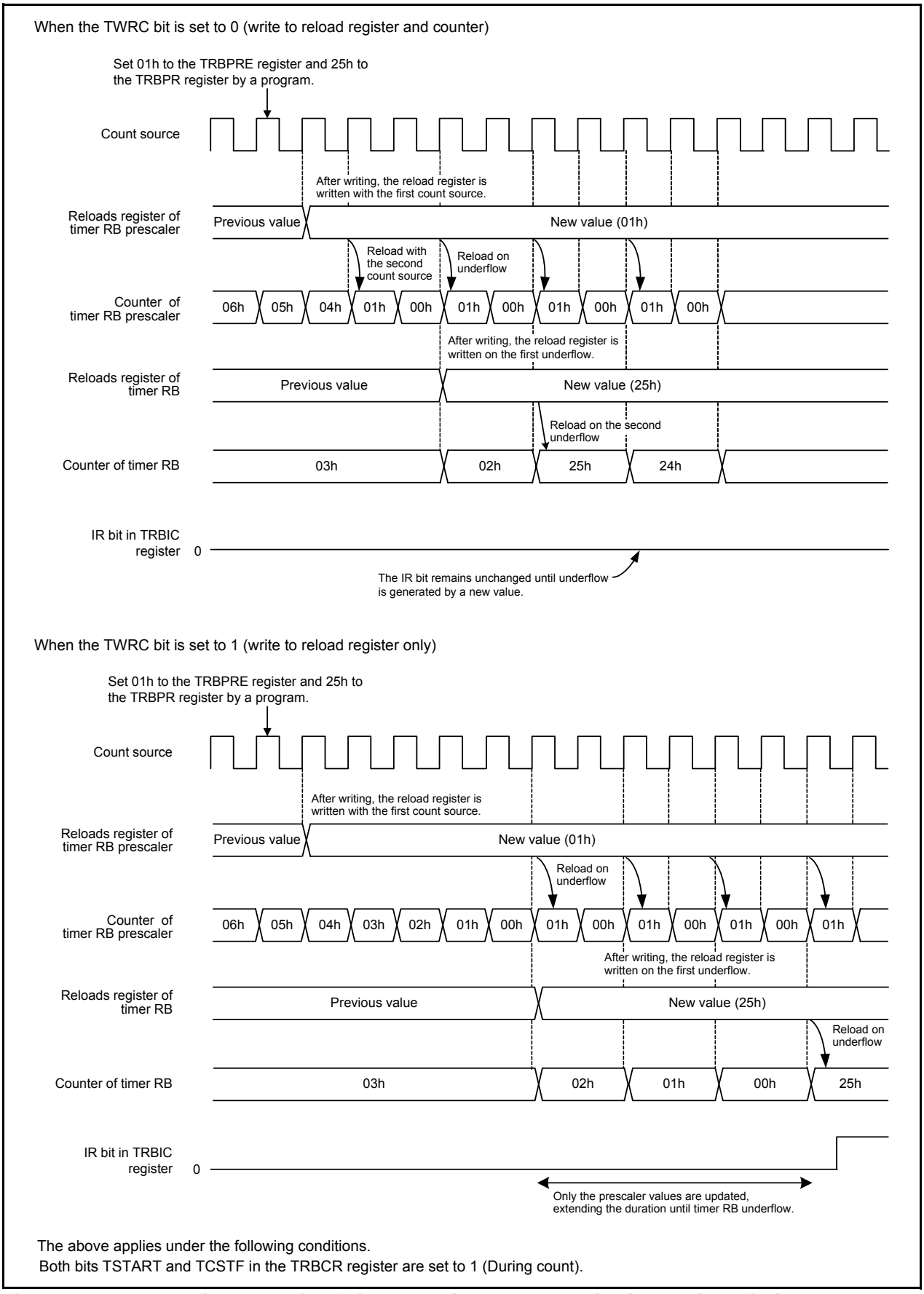


Figure 17.17 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation

17.2.2 Programmable Waveform Generation Mode

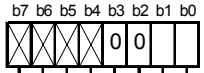
In programmable waveform generation mode, the signal output from the TRBO pin is inverted each time the counter underflows, while the values in registers TRBPR and TRBSC are counted alternately (refer to **Table 17.8 Programmable Waveform Generation Mode Specifications**). Counting starts by counting the setting value in the TRBPR register. The TRBOCR register is unused in this mode.
Figure 17.18 shows TRBIOC Register in Programmable Waveform Generation Mode. Figure 17.19 shows an Operating Example of Timer RB in Programmable Waveform Generation Mode.

Table 17.8 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Count source frequency n: Value set in TRBPRE register m: Value set in TRBPR register p: Value set in TRBSC register
Count start condition	1 (count start) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stop) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]
TRBO pin function	Programmable output port or pulse output
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.(1)
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only.(2)
Select functions	• Output level select function The TOPL bit in the TRBIOC register selects the output level during primary and secondary periods. • TRBO pin output switch function Timer RB pulse output or P1_3 latch output is selected by the TOCNT bit in the TRBIOC register.(3) • TRBO pin select function P1_3 is selected by the TRBOSEL bit in the PINSR2 register.

NOTES:
1. Even when counting the secondary period, the TRBPR register may be read.
2. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBPR register.
3. The value written to the TOCNT bit is enabled by the following.
   - When counting starts.
   - When a timer RB interrupt request is generated.
     The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

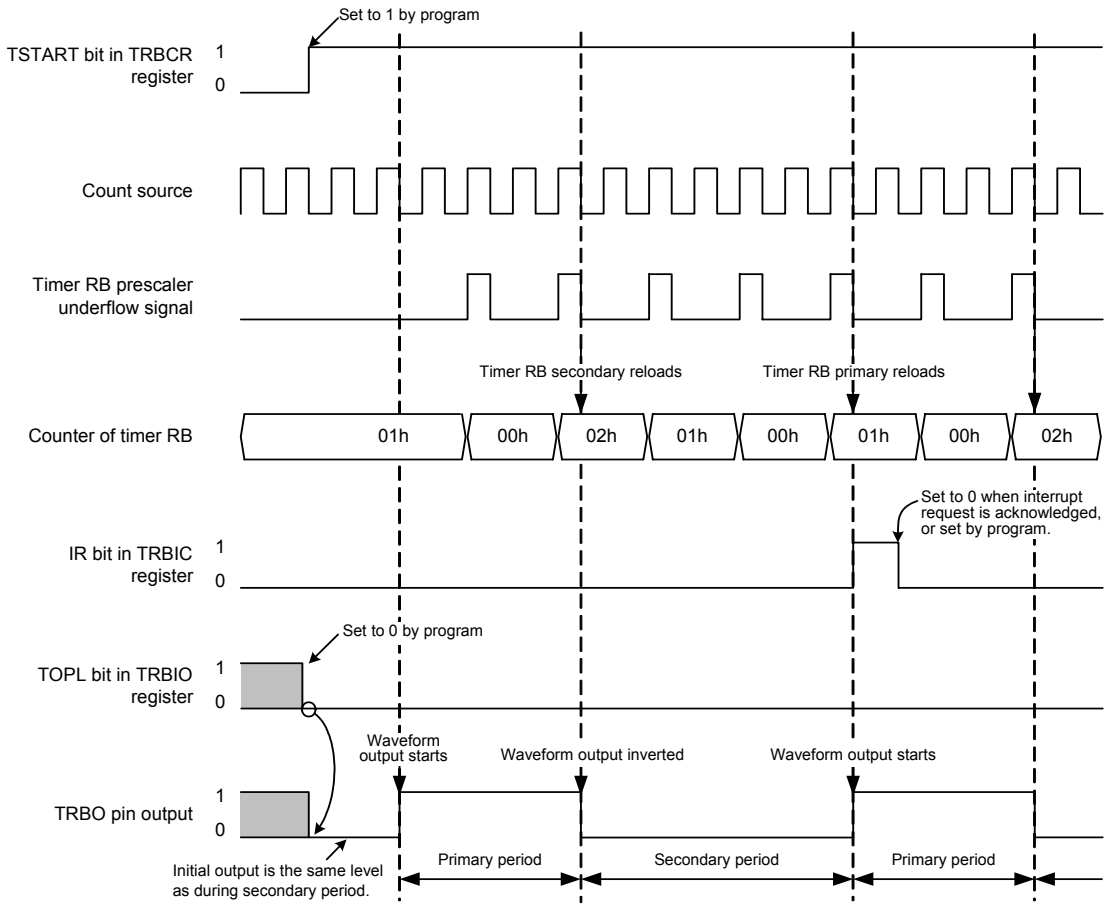
Timer RB I/O Control Register



Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	0 : Outputs “H” for primary period Outputs “L” for secondary period Outputs “L” when the timer is stopped 1 : Outputs “L” for primary period Outputs “H” for secondary period Outputs “H” when the timer is stopped	RW
TOCNT	Timer RB output switch bit	0 : Outputs timer RB waveform 1 : Outputs value in P1_3 port register	RW
INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	RW
INOSEG	One-shot trigger polarity select bit		RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 17.18 TRBIOC Register in Programmable Waveform Generation Mode



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 02h
TRBIOC register TOCNT = 0 (timer RB waveform is output from the TRBO pin)

Figure 17.19 Operating Example of Timer RB in Programmable Waveform Generation Mode

17.2.3 Programmable One-shot Generation Mode

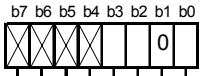
In programmable one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 17.9 Programmable One-Shot Generation Mode Specifications**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBPR register. The TRBSC register is not used in this mode.
Figure 17.20 shows TRBIOC Register in Programmable One-Shot Generation Mode. Figure 17.21 shows an Operating Example of Programmable One-Shot Generation Mode.

Table 17.9 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the setting value in the TRBPR register • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
One-shot pulse output time	(n+1)(m+1)/fi fi: Count source frequency, n: Setting value in TRBPRE register, m: Setting value in TRBPR register(2)
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during primary period • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops) • When the TSTART bit in the TRBCR register is set to 0 (stops counting) • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting)
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the TRBO output ends) [timer RB interrupt]
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written during the count, values are written to the reload register only (the data is transferred to the counter at the following reload).(1)
Select functions	• Output level select function The TOPL bit in the TRBIOC register selects the output level of the one-shot pulse waveform. • One-shot trigger select function Refer to **17.2.3.1 One-Shot Trigger Selection**. • TRBO pin select function P1_3 is selected by the TRBOSEL bit in the PINSR2 register.

NOTES:
1. The set value is reflected at the following one-shot pulse after writing to the TRBPR register.
2. Do not set both the TRBPRE and TRBPR registers to 00h.

Timer RB I/O Control Register

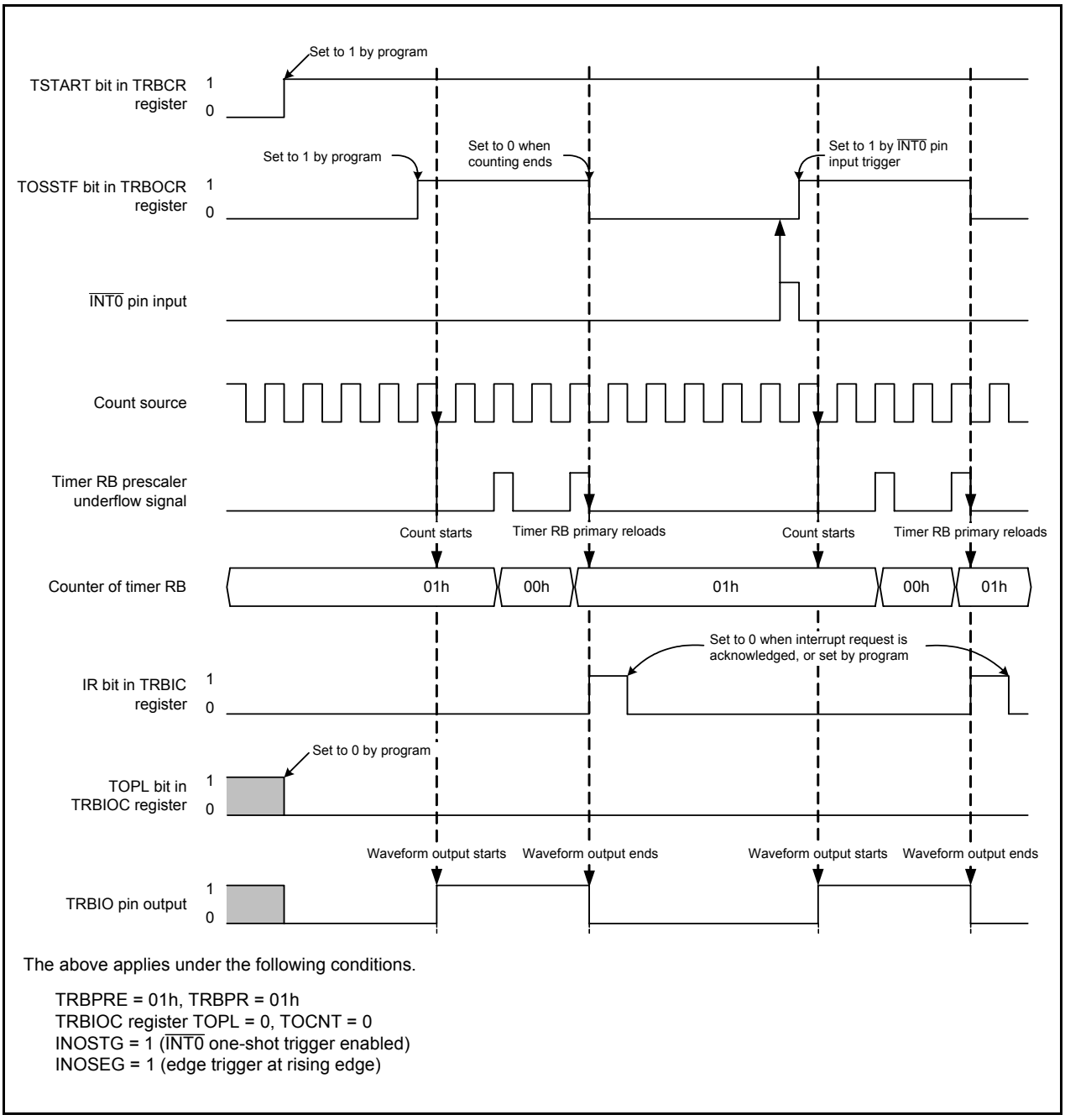


Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB Output Level Select Bit	0 : Outputs one-shot pulse “H” Outputs “L” when the timer is stopped 1 : Outputs one-shot pulse “L” Outputs “H” when the timer is stopped	RW
TOCNT	Timer RB Output Switch Bit	Set to 0 in programmable one-shot generation mode.	RW
INOSTG	One-Shot Trigger Control Bit(1)	0 : $\overline{\text{INT0}}$ pin one-shot trigger disabled 1 : $\overline{\text{INT0}}$ pin one-shot trigger enabled	RW
INOSEG	One-Shot Trigger Polarity Select Bit(1)	0 : Falling edge trigger 1 : Rising edge trigger	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, its content is 0.		—

NOTE:
1. Refer to **17.2.3.1 One-Shot Trigger Selection**.

Figure 17.20 TRBIOC Register in Programmable One-Shot Generation Mode



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h
TRBIOC register TOPL = 0, TOCNT = 0
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 17.21 Operating Example of Programmable One-Shot Generation Mode

17.2.3.1 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:

- 1 is written to the TOSST bit in the TRBOCR register by a program.
- Trigger input from the $\overline{\text{INT0}}$ pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INT0}}$ pin, input the trigger after making the following settings:

- Set the PD4_5 bit in the PD4 register to 0 (input port).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F1 and INT0F0 in the INTF register.
- Select both edges or one edge with the INT0PL bit in INTEN register. If one edge is selected, further select falling or rising edge with the INOSEG bit in TRBIOC register.
- Set the INT0EN bit in the INTEN register to 0 (enabled).
- After completing the above, set the INOSTG bit in the TRBIOC register to 1 ($\overline{\text{INT}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INT0}}$ pin.

- Processing to handle the interrupts is required. Refer to **13. Interrupts**, for details.
- If one edge is selected, use the POL bit in the INT0IC register to select falling or rising edge. (The INOSEG bit in the TRBIOC register does not affect $\overline{\text{INT0}}$ interrupts).
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INT0IC register changes.

17.2.4 Programmable Wait One-Shot Generation Mode

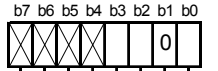
In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 17.10 Programmable Wait One-Shot Generation Mode Specifications**). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value in the TRBSC register after waiting for a given length of time equal to the setting value in the TRBPR register.
Figure 17.22 shows TRBIOC Register in Programmable Wait One-Shot Generation Mode. Figure 17.23 shows an Operating Example of Programmable Wait One-Shot Generation Mode.

Table 17.10 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the timer RB primary setting value. • When a count of the timer RB primary underflows, the timer reloads the contents of timer RB secondary before the count continues. • When a count of the timer RB secondary underflows, the timer reloads the contents of timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
Wait time	(n+1)(m+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, m Value set in the TRBPR register(2)
One-shot pulse output time	(n+1)(p+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, p: Value set in the TRBSC register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts). • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during secondary period. • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops). • When the TSTART bit in the TRBCR register is set to 0 (starts counting). • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting).
Interrupt request generation timing	In half a cycle of the count source after timer RB underflows during secondary period (complete at the same time as waveform output from the TRBO pin) [timer RB interrupt].
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count stops, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only.(1)
Select functions	• Output level select function The TOPL bit in the TRBIOC register selects the output level of the one-shot pulse waveform. • One-shot trigger select function Refer to **17.2.3.1 One-Shot Trigger Selection**. • TRBO pin select function P1_3 is selected by the TRBOSEL bit in the PINSR2 register.

NOTES:
1. The set value is reflected at the following one-shot pulse after writing to registers TRBSC and TRBPR.
2. Do not set both the TRBPRE and TRBPR registers to 00h.

Timer RB I/O Control Register



Symbol	Address	After Reset
TRBIOC	010Ah	00h

Bit Symbol	Bit Name	Function	RW
TOPL	Timer RB output level select bit	0: Outputs one-shot pulse “H”. Outputs “L” when the timer stops or during wait. 1: Outputs one-shot pulse “L”. Outputs “H” when the timer stops or during wait.	RW
TOCNT	Timer RB output switch bit	Set to 0 in programmable wait one-shot generation mode.	RW
INOSTG	One-shot trigger control bit(1)	0 : $\overline{\text{INT0}}$ pin one-shot trigger disabled 1 : $\overline{\text{INT0}}$ pin one-shot trigger enabled	RW
INOSEG	One-shot trigger polarity select bit(1)	0 : Falling edge trigger 1 : Rising edge trigger	RW
— (b7-b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Refer to **17.2.3.1 One-Shot Trigger Selection**.

Figure 17.22 TRBIOC Register in Programmable Wait One-Shot Generation Mode

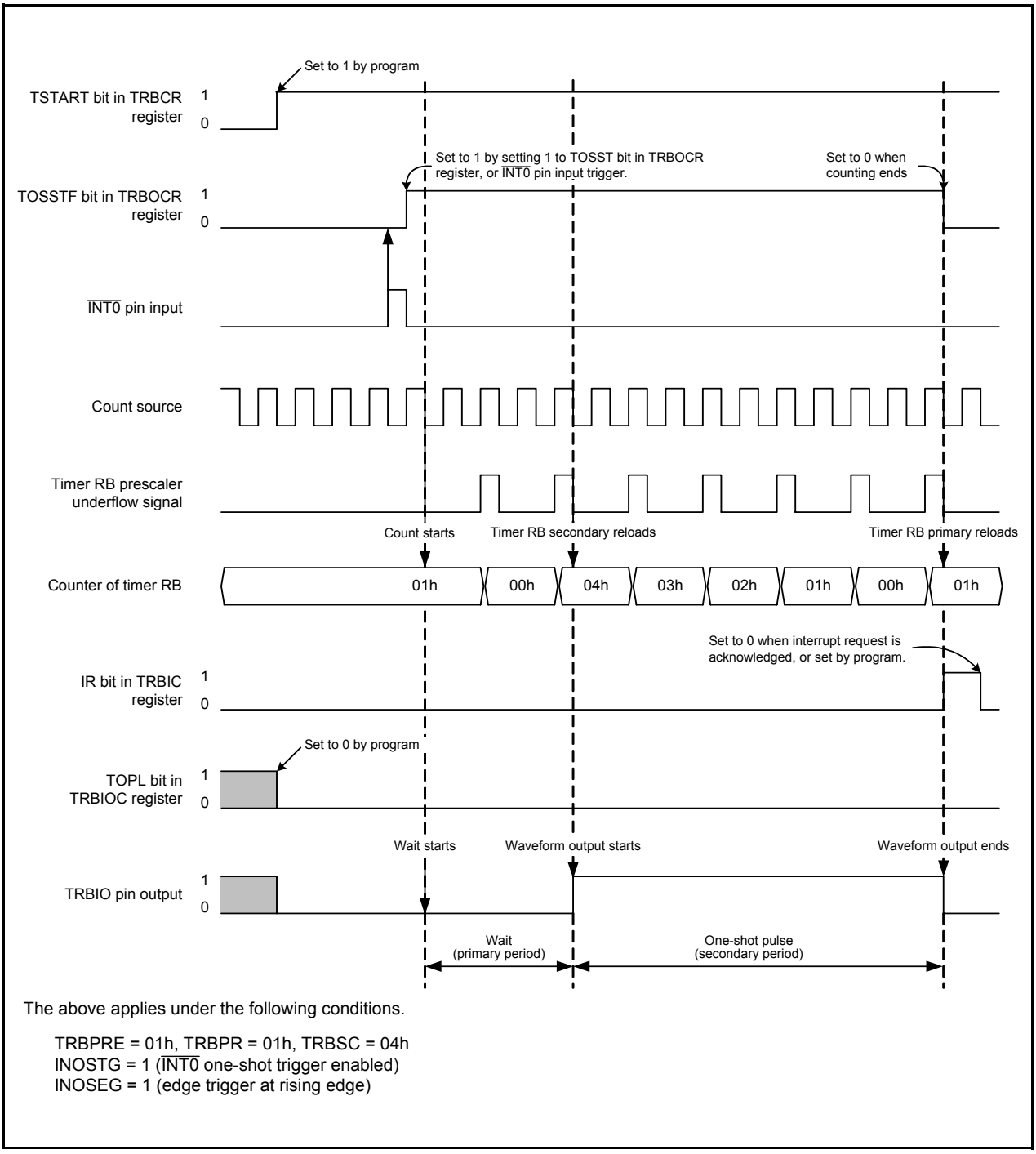


Figure 17.23 Operating Example of Programmable Wait One-Shot Generation Mode

17.2.5 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0, 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB(1)other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.

17.2.5.1 Timer mode

The following workaround should be performed in timer mode.
To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

17.2.5.2 Programmable waveform generation mode

The following three workarounds should be performed in programmable waveform generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) To change registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), synchronize the TRBO output cycle using a timer RB interrupt, etc. This operation should be preformed only once in the same output cycle. Also, make sure that writing to the TRBPR register does not occur during period A shown in Figures 17.24 and 17.25.

The following shows the detailed workaround examples.

- Workaround example (a):
  As shown in Figure 17.24, write to registers TRBSC and TRBPR in the timer RB interrupt routine. These write operations must be completed by the beginning of period A.

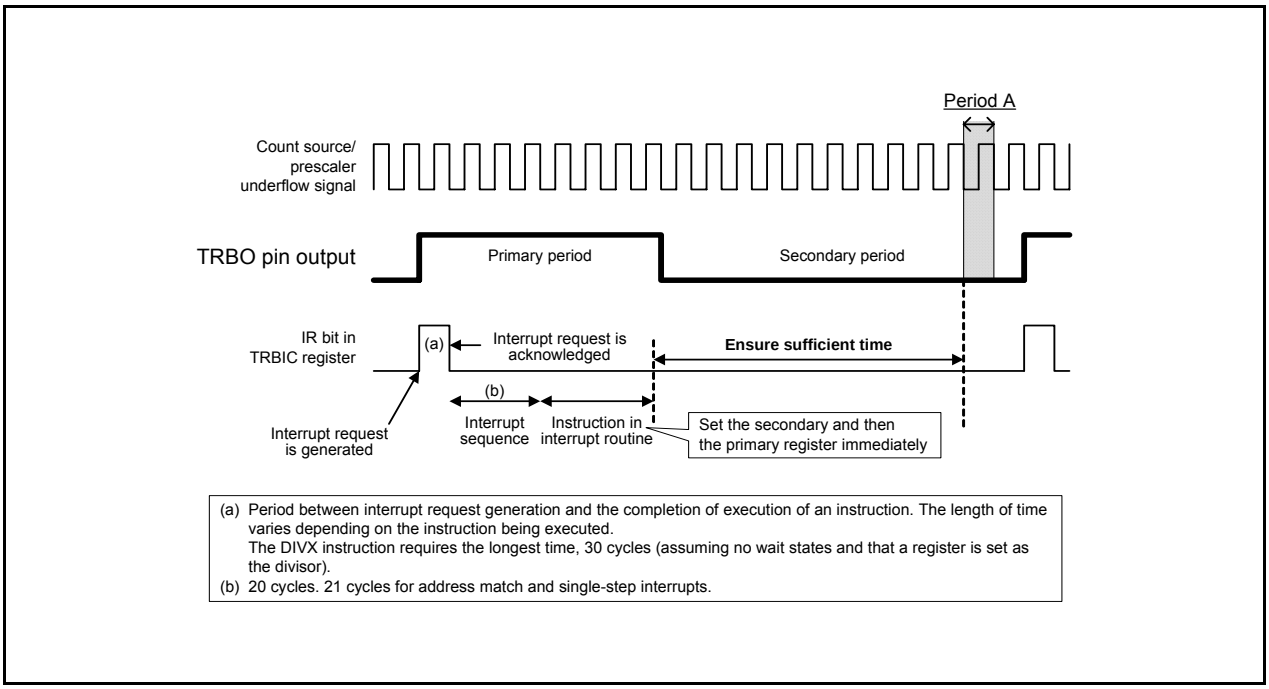


Figure 17.24 Workaround Example (a) When Timer RB interrupt is Used

• Workaround example (b):
As shown in Figure 17.25 detect the start of the primary period by the TRBO pin output level and write to registers TRBSC and TRBPR. These write operations must be completed by the beginning of period A.
If the port register's bit value is read after the port direction register's bit corresponding to the TRBO pin is set to 0 (input mode), the read value indicates the TRBO pin output value.

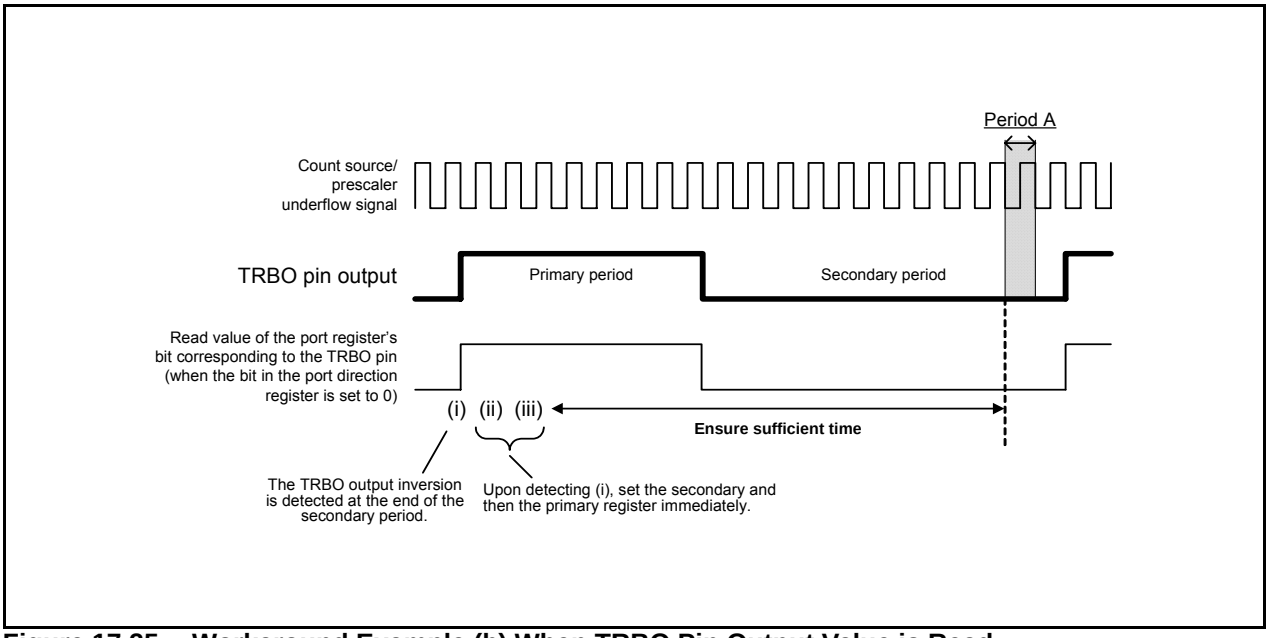


Figure 17.25 Workaround Example (b) When TRBO Pin Output Value is Read

(3) To stop the timer counting in the primary period, use the TSTOP bit in the TRBCR register. In this case, registers TRBPRE and TRBPR are initialized and their values are set to the values after reset.

17.2.5.3 Programmable one-shot generation mode

The following two workarounds should be performed in programmable one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

• When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.

• When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

17.2.5.4 Programmable wait one-shot generation mode

The following three workarounds should be performed in programmable wait one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

(3) Set registers TRBSC and TRBPR using the following procedure.

(a) To use "$\overline{\text{INT0}}$ pin one-shot trigger enabled" as the count start condition
Set the TRBSC register and then the TRBPR register. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before trigger input from the $\overline{\text{INT0}}$ pin.

(b) To use "writing 1 to TOSST bit" as the start condition
Set the TRBSC register, the TRBPR register, and then TOSST bit. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before writing to the TOSST bit.

17.3 Timer RE (for R8C/2H Group only)

Timer RE has the 4-bit counter and 8-bit counter. Timer RE has the following 2 modes:

- Real-time clock mode Generate 1-second signal from fC4 and count seconds, minutes, hours, and days of the week.
- Output compare mode Count a count source and detect compare matches.

The count source for timer RE is the operating clock that regulates the timing of timer operations.

Timer RE is not implemented in the R8C/2J Group.

17.3.1 Real-Time Clock Mode

In real-time clock mode, a 1-second signal is generated from fC4 using a divide-by-2 frequency divider, 4-bit counter, and 8-bit counter and used to count seconds, minutes, hours, and days of the week. Figure 17.26 shows a Block Diagram of Real-Time Clock Mode and Table 17.11 lists the Real-Time Clock Mode Specifications. Figures 17.27 to 17.31 and 17.33 to 17.35 show the Registers Associated with Real-Time Clock Mode. Table 17.12 lists the Interrupt Sources, Figure 17.32 shows the Definition of Time Representation and Figure 17.36 shows the Operating Example in Real-Time Clock Mode.

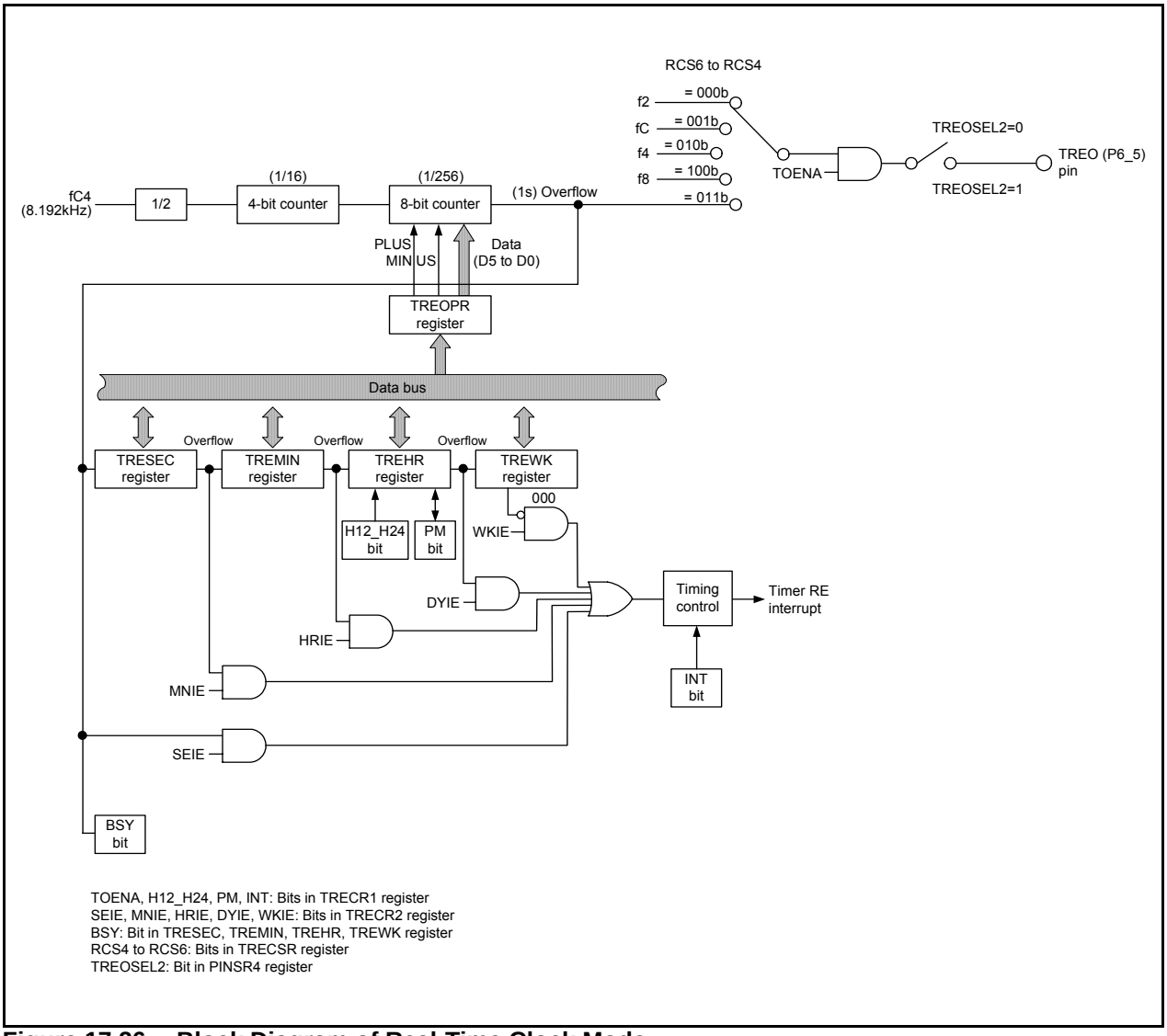


Figure 17.26 Block Diagram of Real-Time Clock Mode

Table 17.11 Real-Time Clock Mode Specifications

Item	Specification
Count source	fC4
Count operation	Increment
Count start condition	1 (count starts) is written to TSTART bit in TRECR1 register
Count stop condition	0 (count stops) is written to TSTART bit in TRECR1 register
Interrupt request generation timing	Select any one of the following: • Update second data • Update minute data • Update hour data • Update day of week data • When day of week data is set to 000b (Sunday)
TREO pin function	Programmable I/O ports or output of f2, fC, f4, f8 or, 1Hz
Read from timer	When reading TRESEC, TREMIN, TREHR, or TREWK register, the count value can be read. The values read from registers TRESEC, TREMIN, and TREHR are represented by the BCD code.
Write to timer	When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), the value can be written to registers TRESEC, TREMIN, TREHR, and TREWK. The values written to registers TRESEC, TREMIN, and TREHR are represented by the BCD codes.
Select function	• 12-hour mode/24-hour mode switch function • Counter precision adjustment function

Timer RE Second Data Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRESEC	0118h	Undefined

Bit Symbol	Bit Name	Function	Setting Range	RW
SC00	1st digit of second count bits	Count 0 to 9 every second. When the digit moves up, 1 is added to the 2nd digit of second.	0 to 9 (BCD code)	RW
SC01				RW
SC02				RW
SC03				RW
SC10	2nd digit of second count bits	When counting 0 to 5, 60 seconds are counted.	0 to 5 (BCD code)	RW
SC11				RW
SC12				RW
BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.		RO

Figure 17.27 TRESEC Register in Real-Time Clock Mode

Timer RE Minute Data Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TREMIN	0119h	Undefined

Bit Symbol	Bit Name	Function	Setting Range	RW
MN00	1st digit of minute count bits	Count 0 to 9 every minute. When the digit moves up, 1 is added to the 2nd digit of minute.	0 to 9 (BCD code)	RW
MN01				RW
MN02				RW
MN03				RW
MN10	2nd digit of minute count bits	When counting 0 to 5, 60 minutes are counted.	0 to 5 (BCD code)	RW
MN11				RW
MN12				RW
BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.		RO

Figure 17.28 TREMIN Register in Real-Time Clock Mode

Timer RE Hour Data Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TREHR	011Ah	X0XXXXXXb

Bit Symbol	Bit Name	Function	Setting Range	RW
HR00	1st digit of hour count bits	Count 0 to 9 every hour. When the digit moves up, 1 is added to the 2nd digit of hour.	0 to 9 (BCD code)	RW
HR01				RW
HR02				RW
HR03				RW
HR10	2nd digit of hour count bits	Count 0 to 1 when the H12_H24 bit is set to 0 (12-hour mode). Count 0 to 2 when the H12_H24 bit is set to 1 (24-hour mode).	0 to 2 (BCD code)	RW
HR11				RW
— (b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—
BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.		RO

Figure 17.29 TREHR Register in Real-Time Clock Mode

Timer RE Day of Week Data Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TREWK	011Bh	X0000XXXb

Bit Symbol	Bit Name	Function	RW
WK0	Day of week count bits	b2 b1 b0 0 0 0 : Sunday 0 0 1 : Monday 0 1 0 : Tuesday 0 1 1 : Wednesday 1 0 0 : Thursday 1 0 1 : Friday 1 1 0 : Saturday 1 1 1 : Do not set.	RW
WK1			RW
WK2			RW
— (b6-b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.	RO

Figure 17.30 TREWK Register in Real-Time Clock Mode

Timer RE Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRECR1	011Ch	XXX0X0X0b

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCSTF	Timer RE count status flag	0 : Count stopped 1 : Counting	RO
TOENA	TREO pin output enable bit	0 : Disable clock output 1 : Enable clock output	RW
INT	Interrupt request timing bit	Set to 1 in real-time clock mode.	RW
TRERST	Timer RE reset bit	When setting this bit to 0, after setting it to 1, the follow ings w ill occur. • Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h. • Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	RW
PM	A.m./p.m. bit	When the H12_H24 bit is set to 0 (12-hour mode)(1) 0 : a.m. 1 : p.m. When the H12_H24 bit is set to 1 (24-hour mode), its value is undefined.	RW
H12_H24	Operating mode select bit	0 : 12-hour mode 1 : 24-hour mode	RW
TSTART	Timer RE count start bit	0 : Count stops 1 : Count starts	RW

NOTE:
1. This bit is automatically modified w hile timer RE counts.

Figure 17.31 TRECR1 Register in Real-Time Clock Mode

Noon

Contents of TREHR Register	H12_H24 bit = 1 (24-hour mode)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	H12_H24 bit = 0 (12-hour mode)	0	1	2	3	4	5	6	7	8	9	10	11	0	1	2	3	4	5
Contents of PM bit		0 (a.m.)												1 (p.m.)					
Contents in TREWK register		000 (Sunday)																	

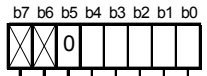
Date changes

Contents of TREHR Register	H12_H24 bit = 1 (24-hour mode)	18	19	20	21	22	23	0	1	2	3	...
	H12_H24 bit = 0 (12-hour mode)	6	7	8	9	10	11	0	1	2	3	...
Contents of PM bit		1 (p.m.)						0 (a.m.)				...
Contents in TREWK register		000 (Sunday)						001 (Monday)				...

PM bit and H12_H24 bits: Bits in TRECR1 register
The above applies to the case when count starts from a.m. 0 on Sunday.

Figure 17.32 Definition of Time Representation

Timer RE Control Register 2



Symbol	Address	After Reset
TRECR2	011Dh	00XXXXXXb

Bit Symbol	Bit Name	Function	RW
SEIE	Periodic interrupt triggered every second enable bit(1)	0 : Disable periodic interrupt triggered every second 1 : Enable periodic interrupt triggered every second	RW
MNIE	Periodic interrupt triggered every minute enable bit(1)	0 : Disable periodic interrupt triggered every minute 1 : Enable periodic interrupt triggered every minute	RW
HRIE	Periodic interrupt triggered every hour enable bit(1)	0 : Disable periodic interrupt triggered every hour 1 : Enable periodic interrupt triggered every hour	RW
DYIE	Periodic interrupt triggered every day enable bit(1)	0 : Disable periodic interrupt triggered every day 1 : Enable periodic interrupt triggered every day	RW
WKIE	Periodic interrupt triggered every week enable bit(1)	0 : Disable periodic interrupt triggered every week 1 : Enable periodic interrupt triggered every week	RW
COMIE	Compare match interrupt enable bit	Set to 0 in real-time clock mode.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

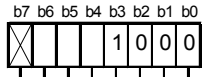
NOTE:
1. Do not set multiple enable bits to 1 (enable interrupt).

Figure 17.33 TRECR2 Register in Real-Time Clock Mode

Table 17.12 Interrupt Sources

Factor	Interrupt Source	Interrupt Enable Bit
Periodic interrupt triggered every week	Value in TREWK register is set to 000b (Sunday) (1-week period)	WKIE
Periodic interrupt triggered every day	TREWK register is updated (1-day period)	DYIE
Periodic interrupt triggered every hour	TREHR register is updated (1-hour period)	HRIE
Periodic interrupt triggered every minute	TREMIN register is updated (1-minute period)	MNIE
Periodic interrupt triggered every second	TRESEC register is updated (1-second period)	SEIE

Timer RE Count Source Select Register



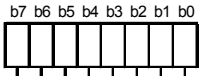
Symbol	Address	After Reset
TRECSR	011Eh	00001000b

Bit Symbol	Bit Name	Function	RW
RCS0	Count source select bits	Set to 00b in real-time clock mode.	RW
RCS1			RW
RCS2	4-bit counter select bit	Set to 0 in real-time clock mode.	RW
RCS3	Real-time clock mode select bit	Set to 1 in real-time clock mode.	RW
RCS4	Clock output select bits(1)	b6 b5 b4 0 0 0 : f2 0 0 1 : fC 0 1 0 : f4 0 1 1 : 1Hz 1 0 0 : f8 Other than above : Do not set.	RW
RCS5			RW
RCS6			RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTE:
1. Write to bits RCS4 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (disable clock output).

Figure 17.34 TRECSR Register in Real-Time Clock Mode

Timer RE Real-Time Clock Precision Adjust Register(1)



Symbol	Address	After Reset
TREOPR	011Fh	00h

Bit Symbol	Bit Name	Function	Setting Range	RW
D0	8-bit counter adjust bit	The correction value of the 8-bit counter is stored. When read, the content is 000000b.	00h to 3Ch	RW
D1				RW
D2				RW
D3				RW
D4				RW
D5				RW
MINUS	8-bit counter subtract bit(2)	When this bit is set to 1, the correction value set by D0 to D5 is subtracted from the 8-bit counter value. When read, the content is 0.		RW
PLUS	8-bit counter add bit(2)	When this bit is set to 1, the correction value set by D0 to D5 is added to the 8-bit counter value. When read, the content is 0.		RW

NOTES:
1. Use the MOV instruction for setting the TREOPR register.
   Allow a period (s) of the XCIN clock × 2064 or more between writes to the TREOPR register.
2. Write 1 to either the MINUS bit or the PLUS bit only once during each interrupt routine for the week/day/hour/minute/second cycle.
   When 00b or 11b is written to bits MINUS and PLUS, the 8-bit counter value is not added or subtracted.

Figure 17.35 TREOPR Register in Real-Time Clock Mode

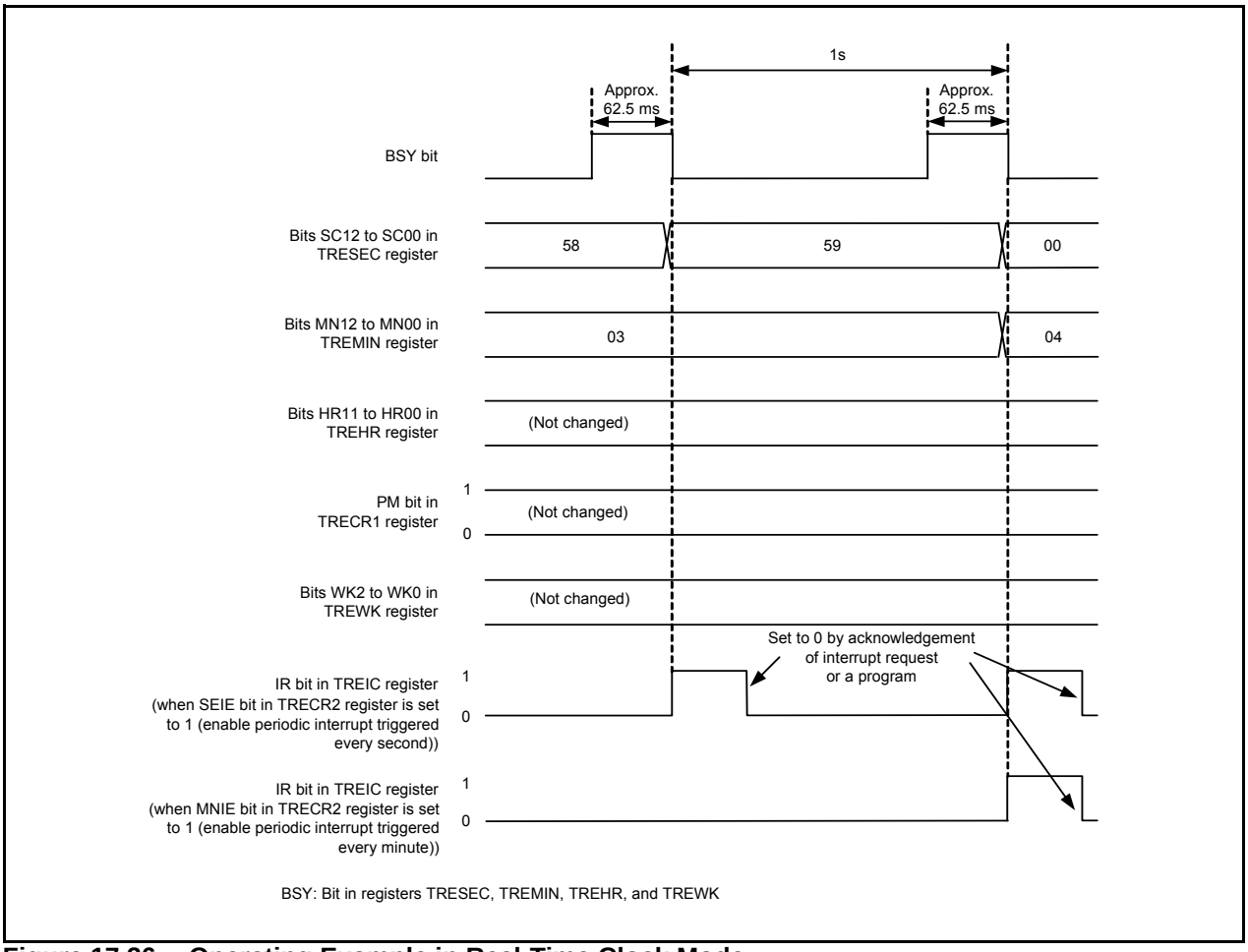


Figure 17.36 Operating Example in Real-Time Clock Mode

17.3.2 Output Compare Mode

In output compare mode, the internal count source divided by 2 is counted using the 4-bit or 8-bit counter and compare value match is detected with the 8-bit counter. Figure 17.37 shows a Block Diagram of Output Compare Mode and Table 17.13 lists the Output Compare Mode Specifications. Figures 17.38 to 17.42 show the Registers Associated with Output Compare Mode, and Figure 17.43 shows the Operating Example in Output Compare Mode.

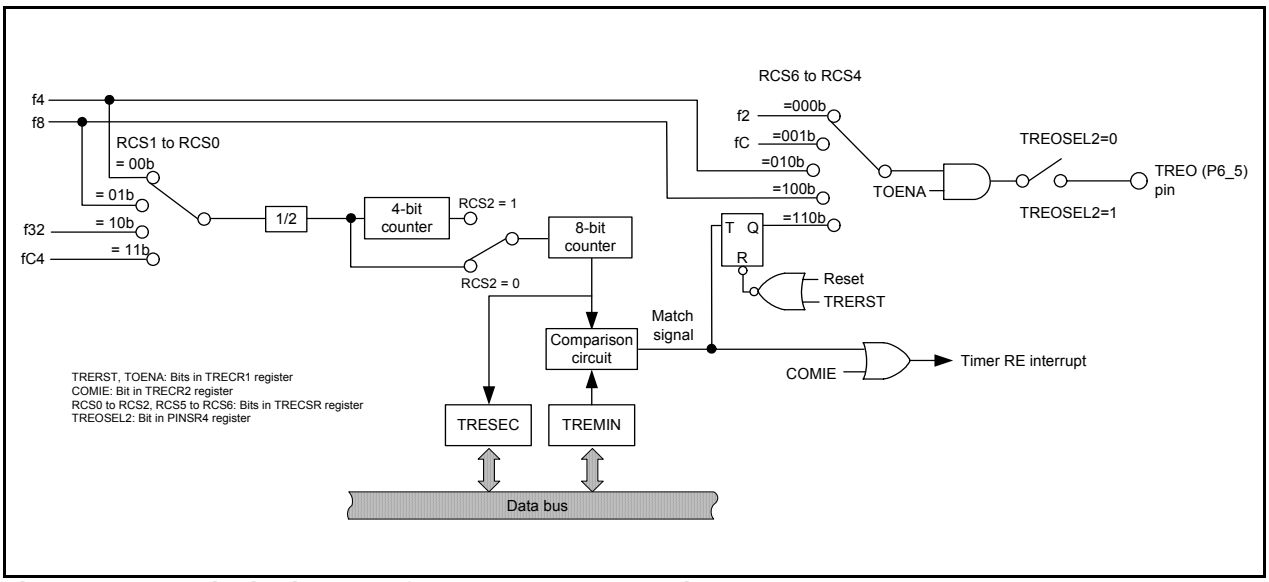


Figure 17.37 Block Diagram of Output Compare Mode

Table 17.13 Output Compare Mode Specifications

Item	Specification
Count sources	f4, f8, f32, fC4
Count operations	• Increment • When the 8-bit counter content matches with the TREMIN register content, the value returns to 00h and count continues. The count value is held while count stops.
Count period	• When RCS2 = 0 (4-bit counter is not used) 1/fi x 2 x (n+1) • When RCS2 = 1 (4-bit counter is used) 1/fi x 32 x (n+1) fi: Frequency of count source n: Setting value of TREMIN register
Count start condition	1 (count starts) is written to the TSTART bit in the TRECR1 register
Count stop condition	0 (count stops) is written to the TSTART bit in the TRECR1 register
Interrupt request generation timing	When the 8-bit counter content matches with the TREMIN register content
TREO pin function	Select any one of the following: • Programmable I/O ports • Output f2, fC, f4, or f8 • Compare output
Read from timer	When reading the TRESEC register, the 8-bit counter value can be read. When reading the TREMIN register, the compare value can be read.
Write to timer	Writing to the TRESEC register is disabled. When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), writing to the TREMIN register is enabled.
Selectable functions	• Select use of 4-bit counter • Compare output function Every time the 8-bit counter value matches the TREMIN register value, TREO output polarity is reversed. The TREO pin outputs “L” after reset is deasserted and the timer RE is reset by the TRERST bit in the TRECR1 register. Output level is held by setting the TSTART bit to 0 (count stops).

Timer RE Counter Data Register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRESEC	0118h	Undefined

Function	RW
8-bit counter data can be read. Although Timer RE stops counting, the count value is held. The TRESEC register is set to 00h at the compare match.	RO

Figure 17.38 TRESEC Register in Output Compare Mode

Timer RE Compare Data Register

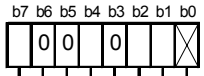
b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TREMIN	0119h	Undefined

Function	RW
8-bit compare data is stored.	RW

Figure 17.39 TREMIN Register in Output Compare Mode

Timer RE Control Register 1

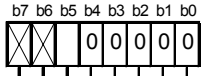


Symbol	Address	After Reset
TRECR1	011Ch	XXX0X0X0b

Bit Symbol	Bit Name	Function	RW
— (b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
TCSTF	Timer RE count status flag	0 : Count stopped 1 : Counting	RO
TOENA	TREO pin output enable bit	0 : Disable clock output 1 : Enable clock output	RW
INT	Interrupt request timing bit	Set to 0 in output compare mode.	RW
TRERST	Timer RE reset bit	When setting this bit to 0, after setting it to 1, the following will occur. • Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h. • Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	RW
PM	A.m./p.m. bit	Set to 0 in output compare mode.	RW
H12_H24	Operating mode select bit		RW
TSTART	Timer RE count start bit	0 : Count stops 1 : Count starts	RW

Figure 17.40 TRECR1 Register in Output Compare Mode

Timer RE Control Register 2

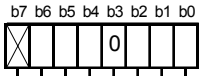


Symbol	Address	After Reset
TRECR2	011Dh	00XXXXXXb

Bit Symbol	Bit Name	Function	RW
SEIE	Periodic interrupt triggered every second enable bit	Set to 0 in output compare mode.	RW
MNIE	Periodic interrupt triggered every minute enable bit		RW
HRIE	Periodic interrupt triggered every hour enable bit		RW
DYIE	Periodic interrupt triggered every day enable bit		RW
WKIE	Periodic interrupt triggered every week enable bit		RW
COMIE	Compare match interrupt enable bit	0 : Disable compare match interrupt 1 : Enable compare match interrupt	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 17.41 TRECR2 Register in Output Compare Mode

Timer RE Count Source Select Register



Symbol	Address	After Reset
TRECSR	011Eh	00001000b

Bit Symbol	Bit Name	Function	RW
RCS0	Count source select bits(1)	b1 b0 0 0 : f4 0 1 : f8 1 0 : f32 1 1 : fC4	RW
RCS1			RW
RCS2	4-bit counter select bit	0 : Not used 1 : Used	RW
RCS3	Real-time clock mode select bit	Set to 0 in output compare mode.	RW
RCS4	Clock output select bits(2)	b6 b5 b4 0 0 0 : f2 0 0 1 : fC 0 1 0 : f4 1 0 0 : f8 1 1 0 : Compare output Other than above : Do not set.	RW
RCS5			RW
RCS6			RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. Write to bits RCS0 to RCS1 when the TCSTF bit in the TRECR1 register is set to 0 (count stopped).
2. Write to bits RCS4 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (disable clock output).

Figure 17.42 TRECSR Register in Output Compare Mode

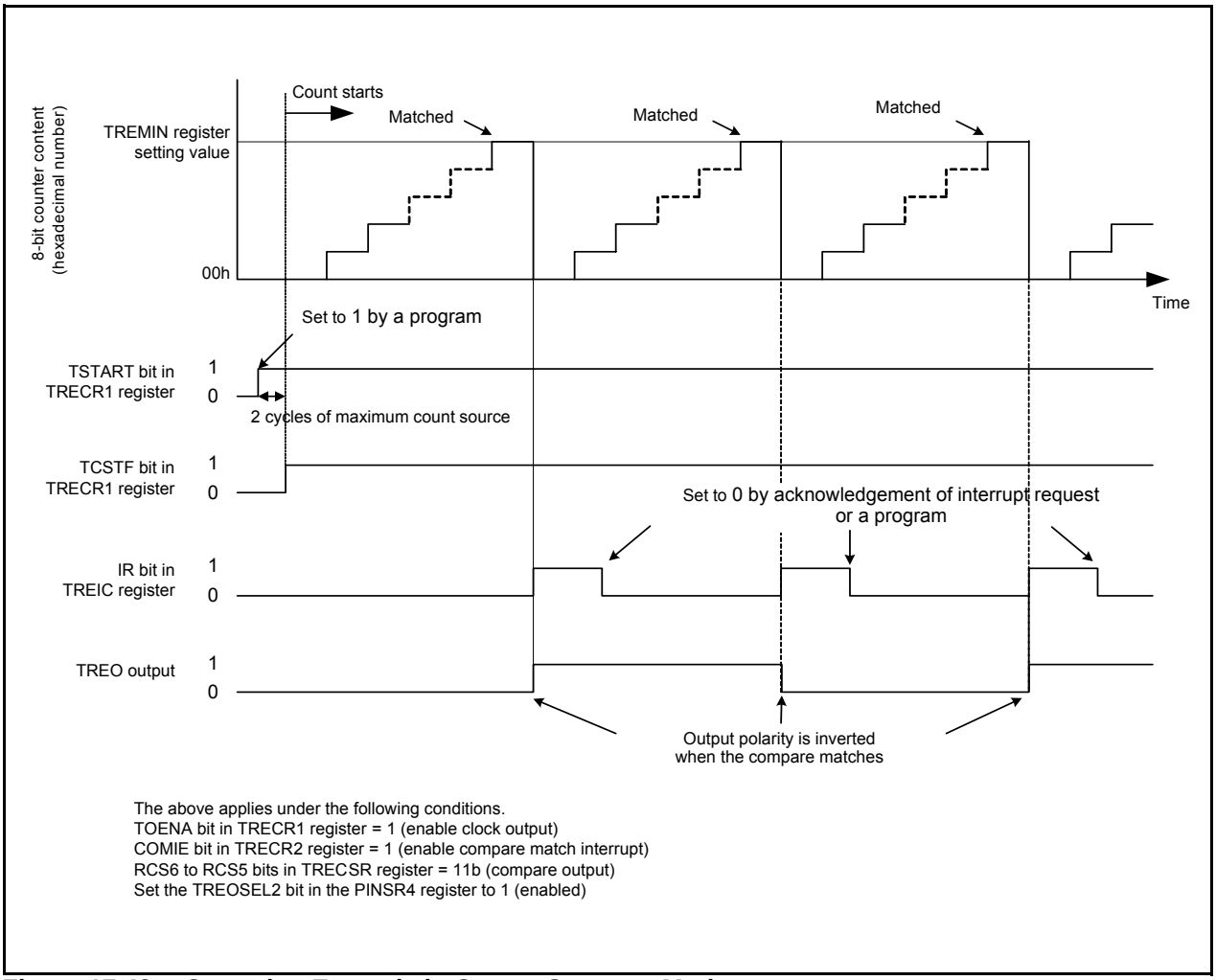


Figure 17.43 Operating Example in Output Compare Mode

17.3.3 Notes on Timer RE (for R8C/2H Group only)

17.3.3.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE(1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

NOTE:
1. Registers associated with timer RE: TRESEC, TREMIN, TREHR, TREWK, TRECR1, TRECR2, TRECSR, and TREOPR.

17.3.3.2 Register Setting

Write to the following registers or bits when timer RE is stopped.

- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24, PM, and INT in TRECR1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.
Figure 17.44 shows a Setting Example in Real-Time Clock Mode.

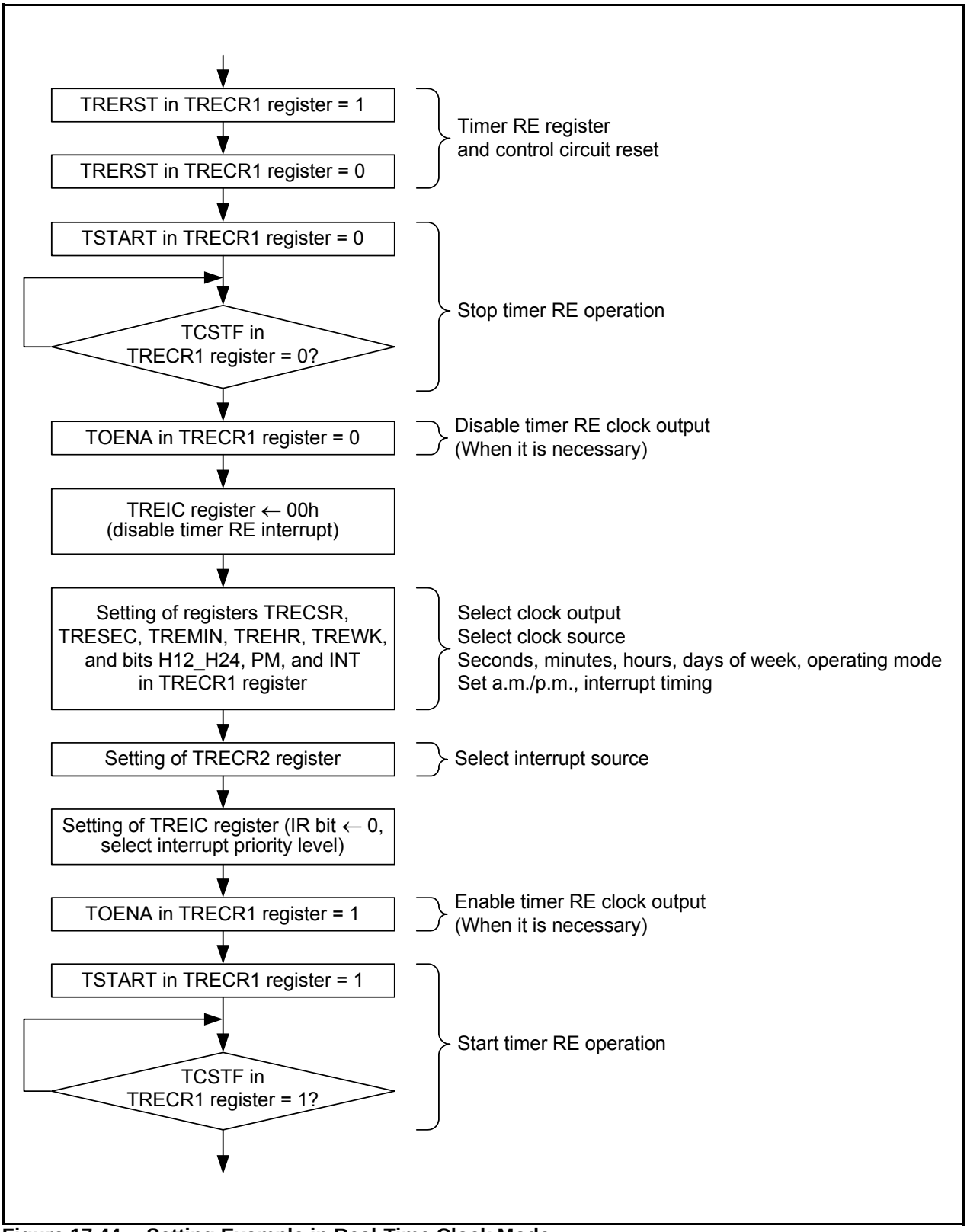


Figure 17.44 Setting Example in Real-Time Clock Mode

17.3.3.3 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECR1 register when the BSY bit is set to 0 (not while data is updated).
Also, when reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.

In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register in the timer RE interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).
(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register.
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

17.4 Timer RF

Timer RF is a 16-bit timer. The count source for timer RF is the operating clock that regulates the timing of timer operations. Figure 17.45 shows a Block Diagram of Timer RF. Figure 17.46 shows a Block Diagram of CMP Waveform Generation Unit. Figure 17.47 shows a Block Diagram of CMP Waveform Output Unit.
Timer RF has two modes: input capture mode and output compare mode. Figures 17.48 to 17.51 show the timer RF associated registers.

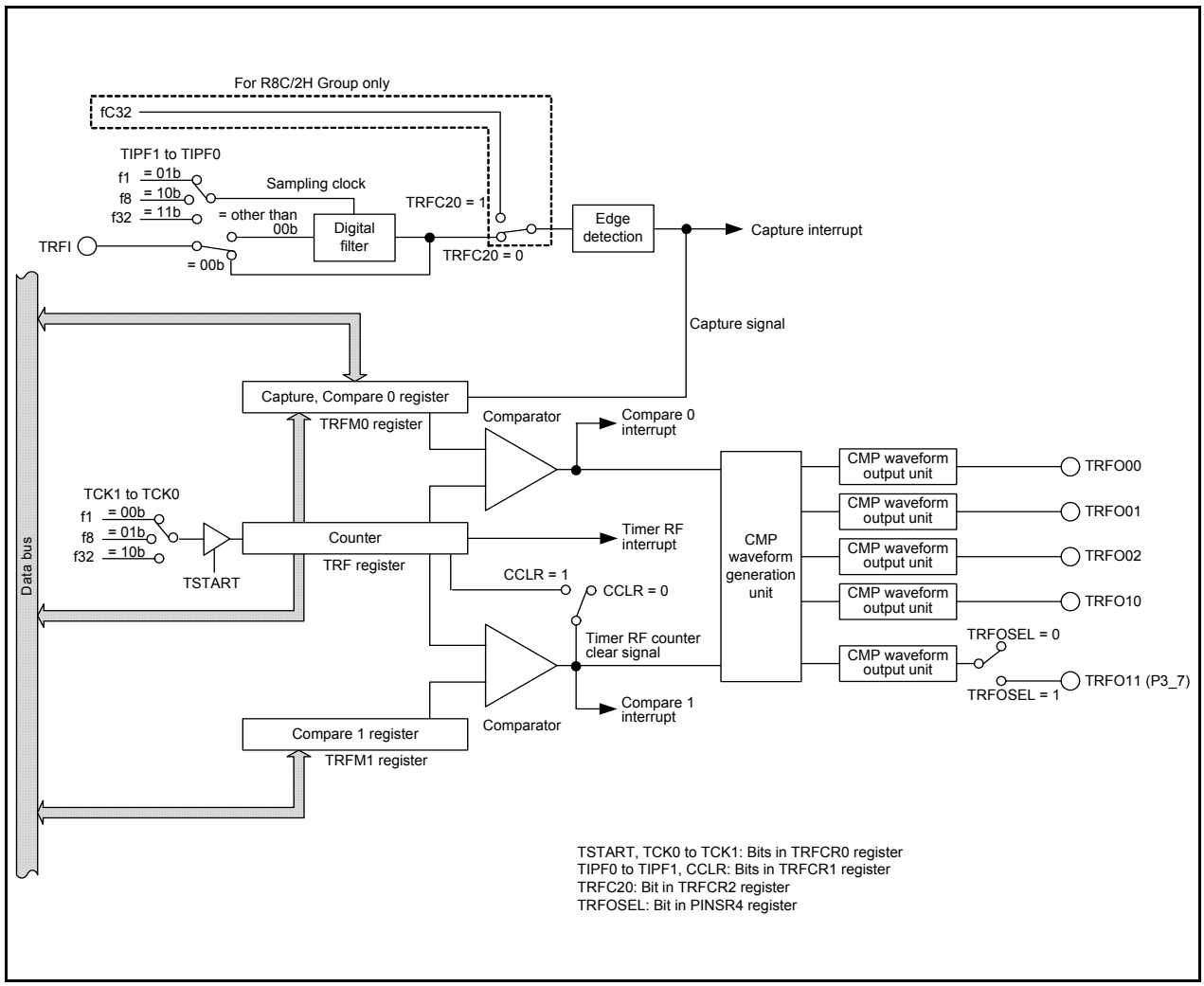


Figure 17.45 Block Diagram of Timer RF

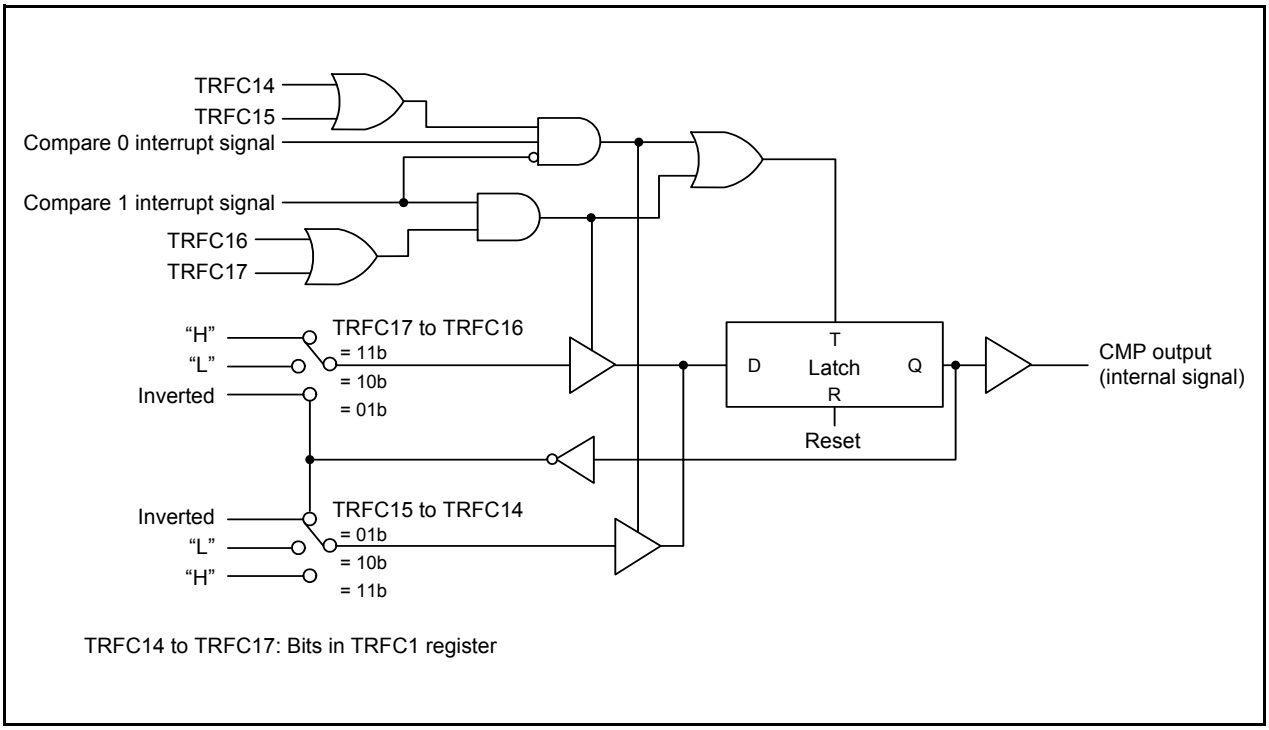


Figure 17.46 Block Diagram of CMP Waveform Generation Unit

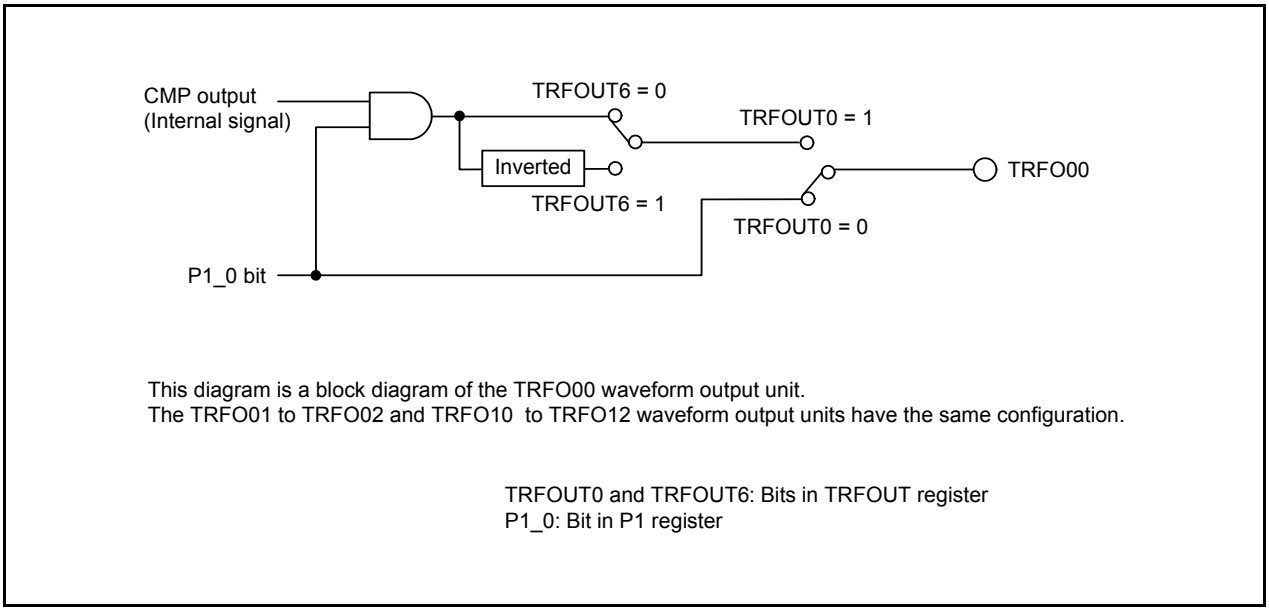


Figure 17.47 Block Diagram of CMP Waveform Output Unit

Timer RF Register(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRF	0291h-0290h	0000h

Function	RW
Count source increment . 0000h can be read when the TSTART bit is set to 0 (count stops). Count value can be read when the TSTART bit is set to 1 (count starts).	RO

NOTE:
1. Access the TRF register in 16-bit units.

Capture and Compare 0 Register(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRFM0	029Dh-029Ch	0000h(2)

Mode	Function	Setting Range	RW
Input capture mode	When the active edge of the measured pulse is input, store the value in the TRF register	—	RO
Output compare mode(3)	Store the value compared with TRF register (counter)	0000h to FFFFh	RW

NOTES:
1. Access the TRFM0 register in 16-bit units.
2. When the TMOD bit in the TRFCR1 register is set to 1, the value is set to FFFFh.
3. When setting a value in the TRFM0 register, set the TMOD bit in the TRFCR1 register to 1 (output compare mode). When the TMOD bit is set to 0 (input capture mode), no value can be written.

Compare 1 Register(1)

(b15) (b8) b7 b0 b7 b0

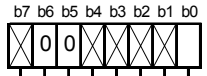
Symbol	Address	After Reset
TRFM1	029Fh-029Eh	FFFFh

Mode	Function	Setting Range	RW
Output compare mode	Store the value compared with TRF register (counter)	0000h to FFFFh	RW

NOTE:
1. Access the TRFM1 register in 16-bit units.

Figure 17.48 Registers TRF, TRFM0, and TRFM1

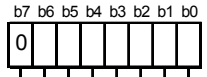
Timer RF Control Register 2 (for R8C/2H Group only)



Symbol	Address	After Reset
TRFCR2	0299h	00h

Bit Symbol	Bit Name	Function	RW
TRFC20	Timer RF capture input select bit	0 : TRFI pin input 1 : fC32	RW
— (b4-b1)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
— (b6-b5)	Reserved bits	Set to 0.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Timer RF Control Register 0



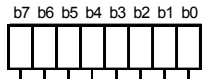
Symbol	Address	After Reset
TRFCR0	029Ah	00h

Bit Symbol	Bit Name	Function	RW
TSTART	Timer RF count start bit	0 : Count stops 1 : Count starts	RW
TCK0	Timer RF count source select bits(1)	b2 b1 0 0 : f1 0 1 : f8 1 0 : f32 1 1 : Do not set.	RW
TCK1			RW
TRFC03	Capture polarity select bits(1)	b4 b3 0 0 : Rising edge 0 1 : Falling edge 1 0 : Both edges 1 1 : Do not set.	RW
TRFC04			RW
TRFC05	CMP output select bit 0 when count stops	0 : TRFC06 bit disabled Holds output level before count stops 1 : TRFC06 bit enabled	RW
TRFC06	CMP output select bit 1 when count stops	0 : "L" output when count stops 1 : "H" output when count stops	RW
— (b7)	Reserved bit	Set to 0.	RW

NOTE:
1. Rewrite this bit when the TSTART bit is set to 0 (count stops).

Figure 17.49 Registers TRFCR2 (for R8C/2H Group only) and TRFCR0

Timer RF Control Register 1



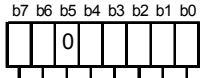
Symbol	Address	After Reset
TRFCR1	029Bh	00h

Bit Symbol	Bit Name	Function	RW
TIPF0	TRFI filter select bits(1)	b1 b0 0 0 : No filter 0 1 : Filter with f1 sampling 1 0 : Filter with f8 sampling 1 1 : Filter with f32 sampling	RW
TIPF1			RW
CCLR	TRF register count operation select bit(2, 3)	0 : Free-running operation 1 : Set TRF register to 0000h when compare 1 is matched.	RW
TMOD	Timer RF operation mode select bit(3)	0 : Input capture mode(2, 4) 1 : Output compare mode	RW
TRFC14	Compare 0 output select bits(2)	b5 b4 CMP output when compare 0 is matched 0 0 : Unchanged 0 1 : Inverted 1 0 : "L" 1 1 : "H"	RW
TRFC15			
TRFC16	Compare 1 output select bits(2)	b7 b6 CMP output when compare 0 is matched 0 0 : Unchanged 0 1 : Inverted 1 0 : "L" 1 1 : "H"	RW
TRFC17			

NOTES:
1. If filter enabled, when the same value from the TRFI pin is sampled three times continuously, the input is determined.
2. When the TMOD bit is set to 0 (input capture mode), set bits CCLR, and TRFC14 to TRFC17 to 0.
3. When the TSTART bit in the TRFCR0 register is set to 0 (count stops), rewrite bits CCLR and TMOD.
4. When the TMOD bit is set to 0 (input capture mode), set bits ILVL2 to ILVL0 in the CMP1IC register to 000b (level 0) and set the IR bit to 0 (no interrupt requested).

Figure 17.50 TRFCR1 Register

Timer RF Output Control Register



Symbol	Address	After Reset
TRFOUT	02FFh	00h

Bit Symbol	Bit Name	Function	RW
TRFOUT0	TRFO00 output enable bit	0 : Output disabled 1 : Output enabled	RW
TRFOUT1	TRFO01 output enable bit		RW
TRFOUT2	TRFO02 output enable bit		RW
TRFOUT3	TRFO10 output enable bit		RW
TRFOUT4	TRFO11 output enable bit		RW
— (b5)	Reserved bit	Set to 0.	RW
TRFOUT6	TRFO00 to TRFO02 output invert bit	0 : Output not inverted 1 : Output inverted	RW
TRFOUT7	TRFO10 to TRFO11 output invert bit		RW

Figure 17.51 TRFOUT Register

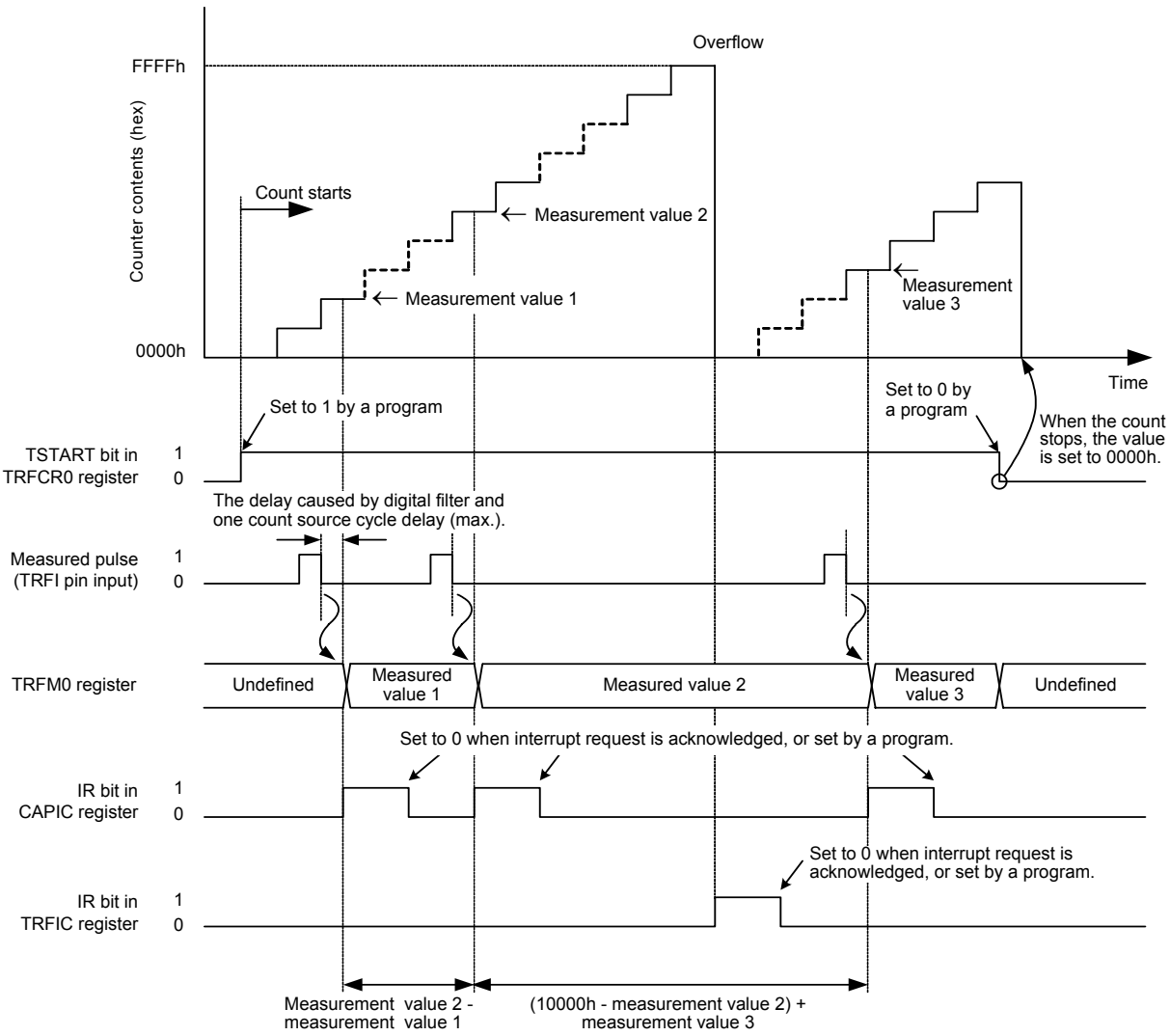
17.4.1 Input Capture Mode

In input capture mode, the edge of the TRFI pin input signal or fC32 is used as a trigger to latch the timer value and the width or the period of external signal is measured. The TRFI input is equipped with a digital filter, and this prevents errors caused by noise or the like from occurring. Table 17.14 shows the Input Capture Mode Specifications. Figure 17.52 shows an Operating Example in Input Capture Mode.

Table 17.14 Input Capture Mode Specifications

Item	Specification
Count sources	f1, f8, f32
Count operations	• Increment • Transfer the value in the TRF register to the TRFM0 register at the valid edge of the measured pulse.
Count period	1/fk × 65536 fk: Frequency of count source
Count start condition	The TSTART bit in the TRFCR0 register is set to 1 (count starts).
Count stop condition	The TSTART bit in the TRFCR0 register is set to 0 (count stops).
Interrupt request generation timing	• The valid edge of TRFI input or fC32 [capture interrupt] • When timer RF overflows [timer RF interrupt]
TRFI pin function	Measured pulse input
TRFO00 to TRFO02, TRFO11 pin functions	Programmable I/O port
Counter value reset timing	In the following cases, the value in the TRF register is set to 0000h. • When the TSTART bit in the TRFCR0 register is set to 0 (count stops).
Read from timer	• The count value can be read out by reading the TRF register. • The count value at the measured pulse valid edge input can be read out by reading the TRFM0 register.
Write to timer	Write to the TRF and TRFM0 registers is disabled.
Select functions	• TRFI or fC32(1) polarity selected Selects the valid edge of the measured pulse. (Bits TRFC03 to TRFC04 in the TRFCR0 register.) • Digital filter function The TRFI input is sampled, and when the sampled input level matches as three times, the level is determined. Selects the sampling clock of the digital filter. (Bits TIPF0 to TIPF1 in the TRFCR1 register.)

NOTE:
1. Available in the R8C/2H Group only.



The above applies under the following conditions.

Bits TRFC04 to TRFC03 in TRFCR0 register = 01b (Capture input polarity is set for falling edge.)
TRFC20 bit in TRFCR2 register = 0 (TRFI pin input) (Applicable to the R8C/2H Group only)

Figure 17.52 Operating Example in Input Capture Mode

17.4.1.1 Digital Filter

The TRFI input is sampled, and when the sampled input level matches three times, its level is determined. Select the digital filter function and sampling clock by the TRFCR1 register.
Figure 17.53 shows a Block Diagram of Digital Filter.

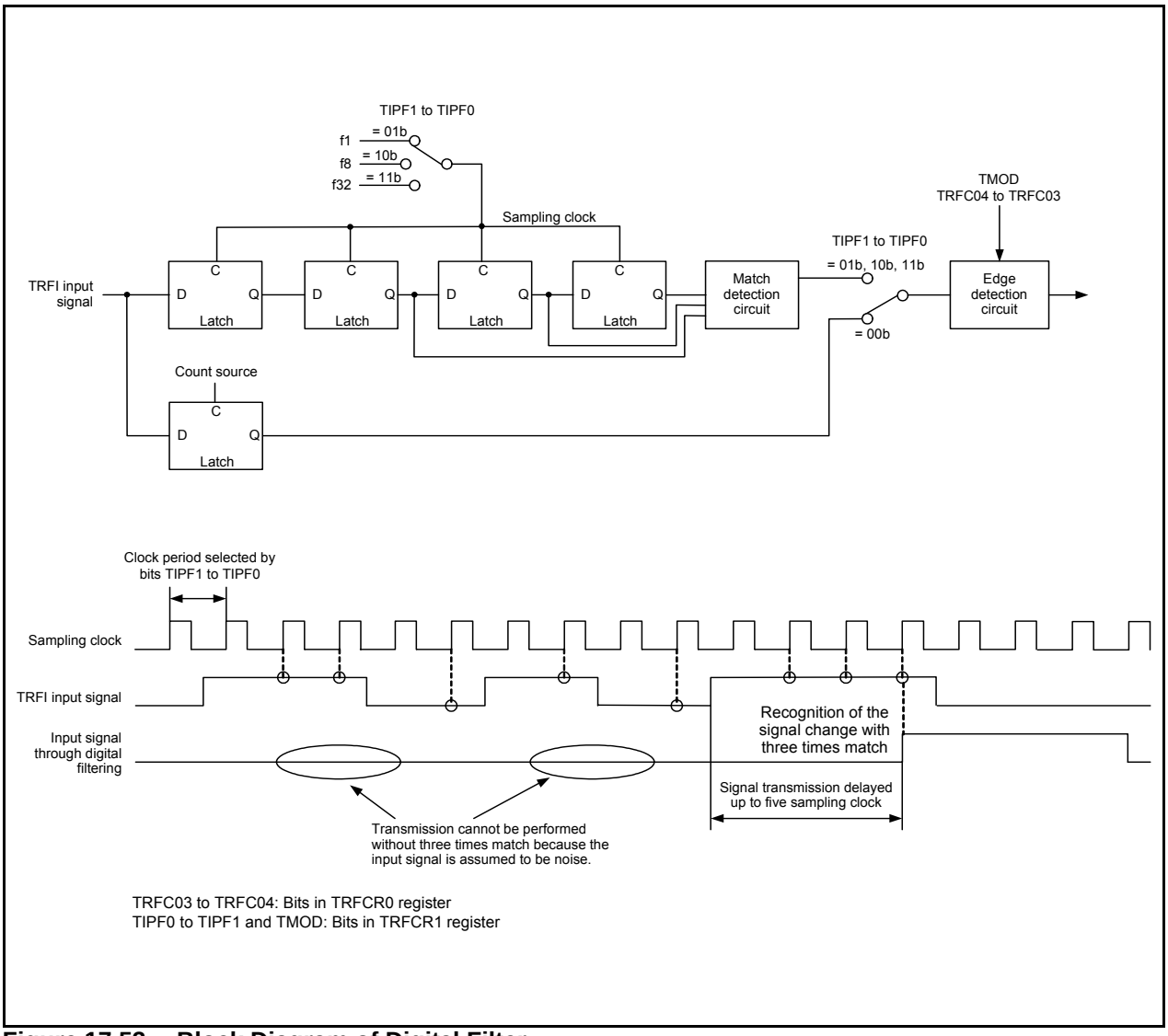


Figure 17.53 Block Diagram of Digital Filter

17.4.2 Output Compare Mode

In output compare mode, when the value of the TRF register matches the value of the TRFM0 (compare 0 match) or TRFM1 (compare 1 match) register, a user-set level is output mode from the output-compare output pin.

Table 17.15 shows the Output Compare Mode Specifications. Table 17.16 shows the Output in Output Compare Mode (Example of TRFO00 Pin). Figure 17.54 shows an Operating Example in Output Compare Mode. Figure 17.55 shows an Operating Example in Output Compare Mode ("L" and "H" Held Output in Count Stops).

Table 17.15 Output Compare Mode Specifications

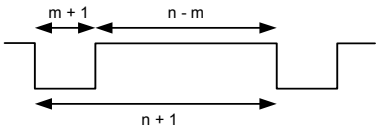
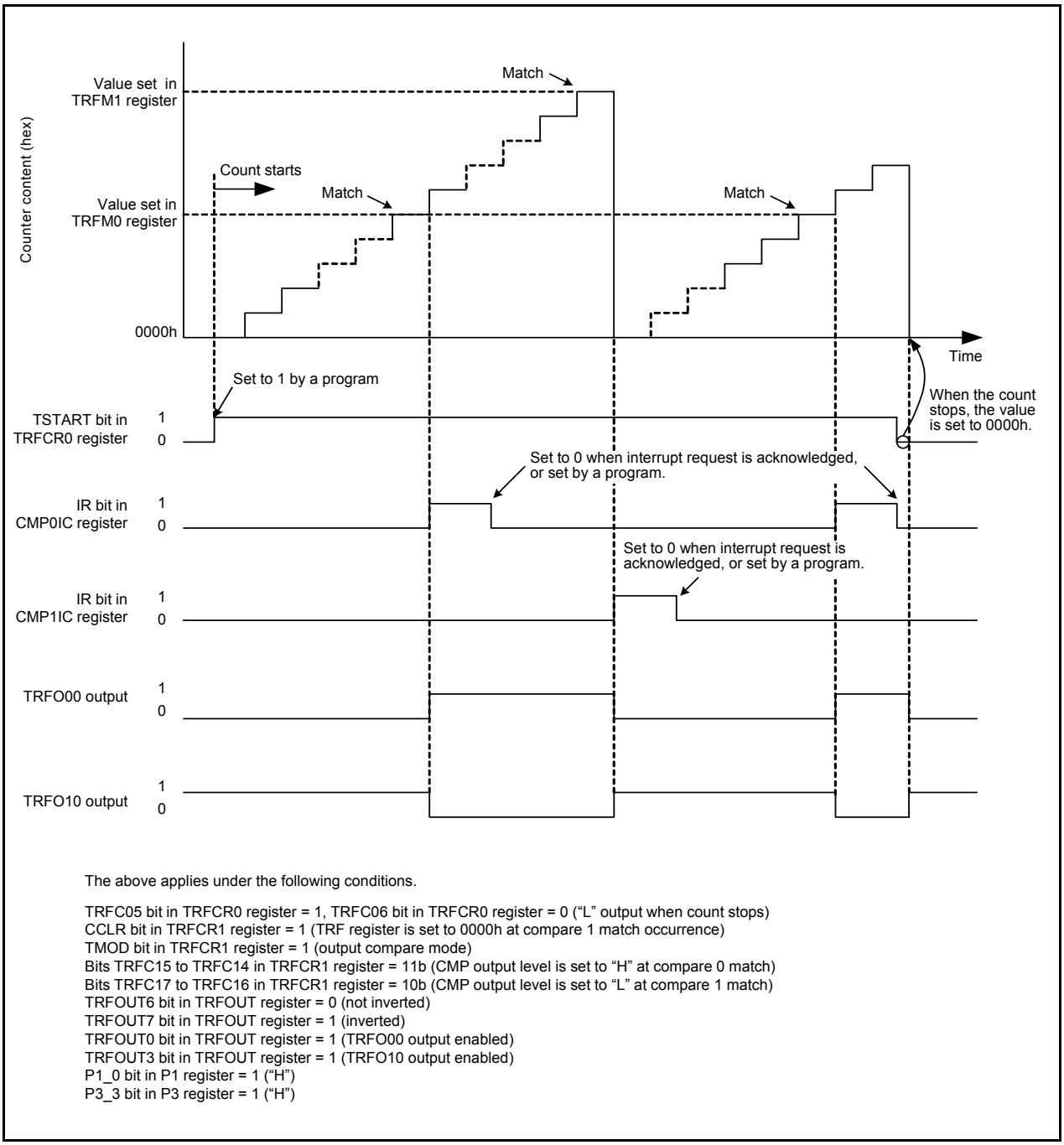
Item	Specification
Count sources	f1, f8, f32
Count operations	Increment
PWM waveform	PWM period: 1/fk × (n + 1) "L" level width: 1/fk × (m + 1) "H" level width: 1/fk × (n - m) fk: Frequency of count source m: Value set in the TRFM0 register n: Value set in the TRFM1 register  It applies under the following conditions. • CMP output "H" when compare 0 is matched • CMP output "L" when compare 1 is matched • CMP output not inverted
Count start condition	The TSTART bit in the TRFCR0 register is set to 1 (count starts).
Count stop condition	The TSTART bit in the TRFCR0 register is set to 0 (count stops).
Interrupt request generation timing	• When compare 0 match is generated [compare 0 interrupt] • When compare 1 match is generated [compare 1 interrupt] • When time RF overflows [timer RF interrupt].
TRFO00 to TRFO11 pin functions	Programmable I/O port or output-compare output
Counter value reset timing	In the following cases, the value in the TRF register is set to 0000h. • When the TSTART bit in the TRFCR0 register is set to 0 (count stops). • The CCLR bit in the TRFCR1 register is set to 1 (the TRF register is set to 0000h at compare 1 match) in the compare 1 matches.
Read from timer	• The count value can be read out by reading the TRF register. • The value in the compare register can be read out by reading registers TRFM0 and TRFM1.
Write to timer	Write to the TRF register is disabled
Select functions	• Output-compare output pin selected Either 1 pin or multiple pins among TRFO00 to TRFO02, or TRFO10 to TRFO11 (bits TRFOUT0 to TRFOUT4 in the TRFOUT register). • Output level at the compare match Selects "H", "L", inverted, or unchanged (bits TRFC14 to TRFC17 in the TRFCR1 register). • Output level inverted Selects output level inverted or not inverted (bits TRFOUT6 to TRFOUT7 in the TRFOUT register). • Output level at the count stops Selects "H", "L", or unchanged (bits TRFC05 to TRFC06 in the TRFCR0 register). • Timing to set the TRF register to 0000h Overflow or compare 1 match in the TRFM1 register (the CCLR bit in the TRFCR1 register). • TRFO11 pin select function P3_7 is selected by the TRFOSEL bit in the PINSR4 register.

Table 17.16 Output in Output Compare Mode (Example of TRFO00 Pin)

TRFO00 Output		Bit Setting Value					
		TRFCR0 Register			TRFOUT Register		P1 Register
		TRFC06	TRFC05	TSTART	TRFOUT6	TRFOUT0	P1_0
Counting	CMP output	X	X	1	0	1	1
	Inverted output of CMP output	X	X	1	1	1	1
	“L” output	X	X	1	0	1	0
	“H” output	X	X	1	1	1	0
Count stops	Holds output level before count stops	X	0	0	X	1	1
	“L” output	0	1	0	X	1	1
	“H” output	1	1	0	X	1	1

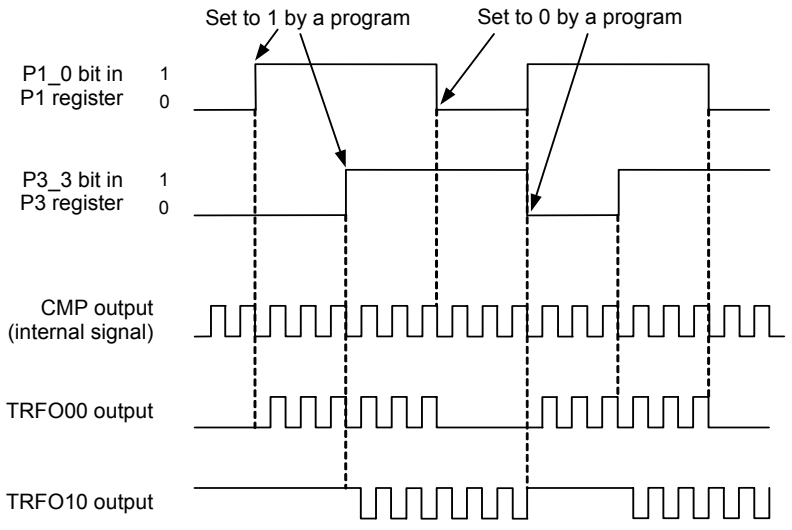
X: 0 or 1



The above applies under the following conditions.

TRFC05 bit in TRFCR0 register = 1, TRFC06 bit in TRFCR0 register = 0 (“L” output when count stops)
CCLR bit in TRFCR1 register = 1 (TRF register is set to 0000h at compare 1 match occurrence)
TMOD bit in TRFCR1 register = 1 (output compare mode)
Bits TRFC15 to TRFC14 in TRFCR1 register = 11b (CMP output level is set to “H” at compare 0 match)
Bits TRFC17 to TRFC16 in TRFCR1 register = 10b (CMP output level is set to “L” at compare 1 match)
TRFOUT6 bit in TRFOUT register = 0 (not inverted)
TRFOUT7 bit in TRFOUT register = 1 (inverted)
TRFOUT0 bit in TRFOUT register = 1 (TRFO00 output enabled)
TRFOUT3 bit in TRFOUT register = 1 (TRFO10 output enabled)
P1_0 bit in P1 register = 1 (“H”)
P3_3 bit in P3 register = 1 (“H”)

Figure 17.54 Operating Example in Output Compare Mode



The above applies under the following conditions.

TRFOUT0 bit in TRFOUT register = 1 (TRFO00 output enabled)
TRFOUT3 bit in TRFOUT register = 1 (TRFO10 output enabled)
TRFOUT6 bit in TRFOUT register = 0 (TRFO00 to TRFO02 output not inverted)
TRFOUT7 bit in TRFOUT register = 1 (TRFO10 to TRFO11 output inverted)
TSTART bit in TRFCR0 register = 1 (count starts)

Figure 17.55 Operating Example in Output Compare Mode (“L” and “H” Held Output in Count Stops)

In output compare mode, the same PWM waveform is output from all of pins TRFO00 to TRFO02 and TRFO10 to TRFO11 during count operation. Note that the output waveform can be inverted for pins TRFO00 to TRFO02 or for pins TRFO10 to TRFO11. The output can also be fixed at “L” or “H” for individual pins for a given period.
The behavior when count operation stops can be selected from the following two options: the output level before the count stops is maintained, or output is fixed at “L” or “H”.

The values in the compare i register can be read by reading the TRFMi (i = 0 or 1) register. Writing to the TRFMi register causes the values to be stored in the compare i register in the following timing:

- If the TSTART bit is set to 0 (count stops)
  Values are stored simultaneously with the write to the TRFMi register.
- If the TSTART bit is set to 1 (count starts) and the CCLR bit in the TRFCR1 register is set to 0 (free running)
  Values are stored when the TRF register (counter) overflows.
- If the TSTART bit is set to 1 and the CCLR bit is set to 1 (TRF register set to 0000h at compare 1 match)
  Values are stored when the compare 1 and TRF register (counter) values match.

17.4.3 Notes on Timer RF

- Access registers TRF, TRFM0, and TRFM1 in 16-bit units.

Example of reading timer RF:

```
MOV.W    0290H,R0    ; Read out timer RF
```

- In input capture mode, a capture interrupt request is generated by inputting an edge selected by bits TRFC03 and TRFC04 in the TRFCR0 register even when the TSTART bit in the TRFCR0 register is set to 0 (count stops).

18. Serial Interface

The serial interface in the R8C/2H Group consists of two channels (UART0 and UART2). The serial interface in the R8C/2J Group consists of one channel (UART0). Each UARTi (i = 0 or 2) has an exclusive timer to generate the transfer clock and operates independently.
Figure 18.1 shows a UARTi (i = 0 or 2 (for R8C/2H Group only)) Block Diagram. Figure 18.2 shows a UARTi Transmit/Receive Unit.
UARTi has two modes: clock synchronous serial I/O mode and clock asynchronous serial I/O mode (UART mode).
Figures 18.3 to 18.5 show the Registers Associated with UARTi.

> UART2 is not implemented in the R8C/2J Group. The description about UART2 in this chapter applies to the R8C/2H Group only.

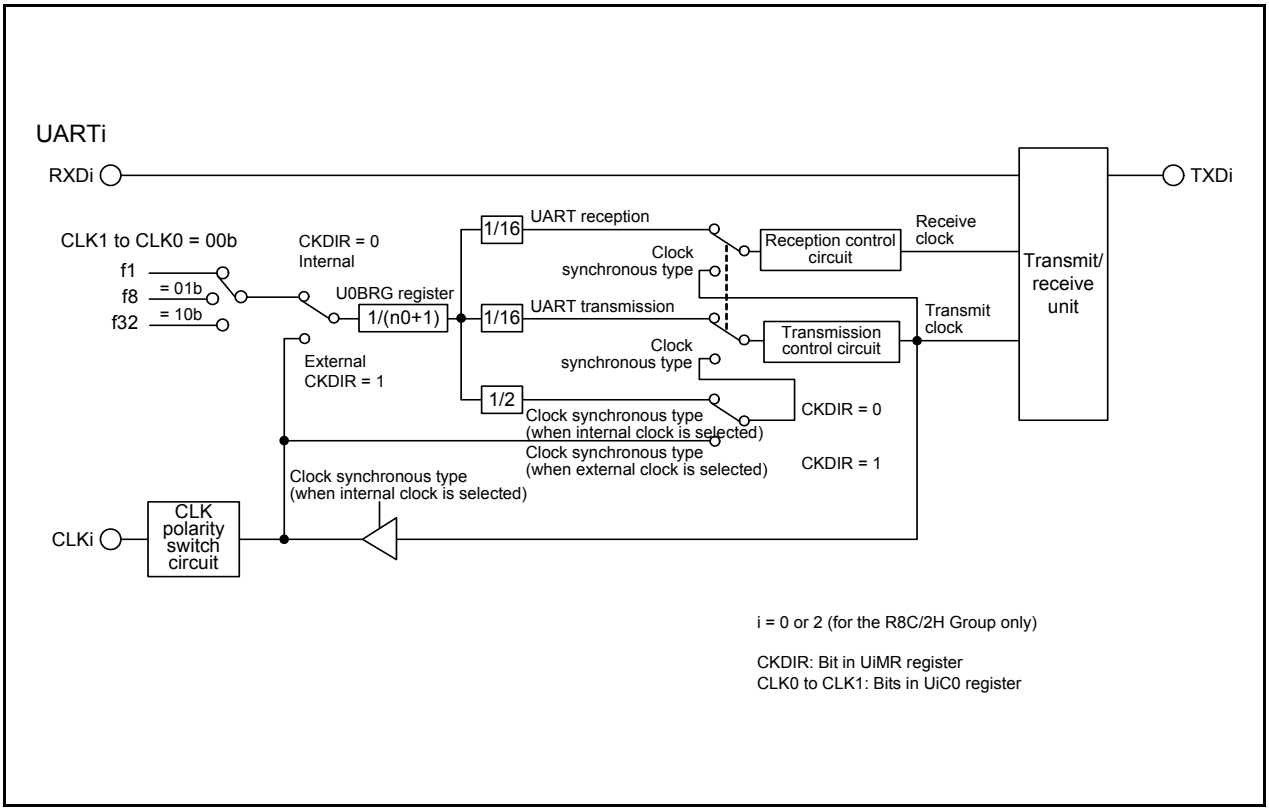


Figure 18.1 UARTi (i = 0 or 2 (for R8C/2H Group only)) Block Diagram

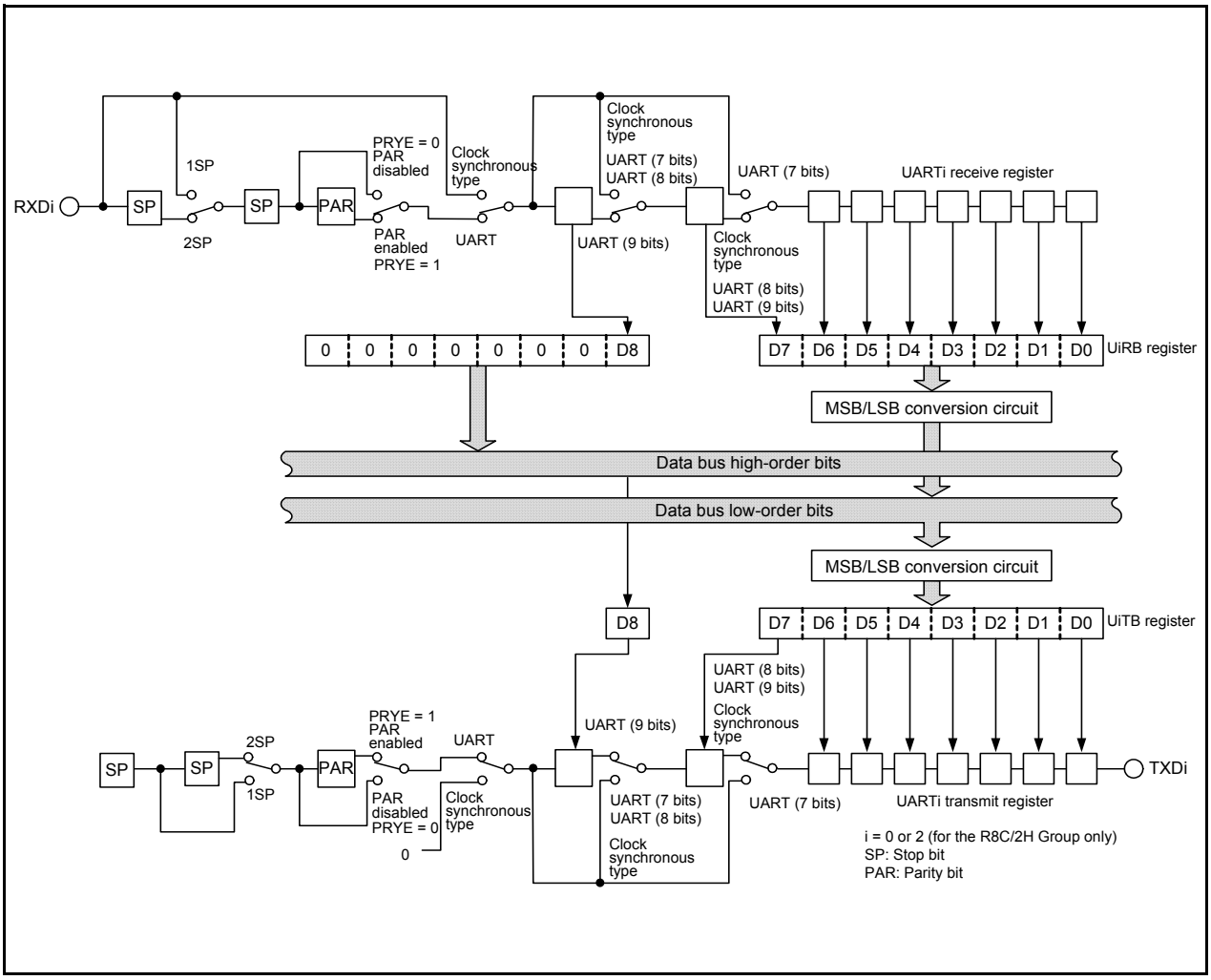
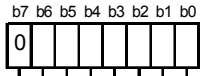


Figure 18.2 UARTi Transmit/Receive Unit

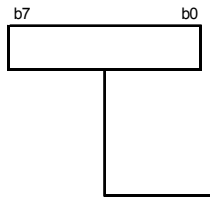
UARTi Transmit/Receive Mode Register (i = 0 or 2 (for R8C/2H Group only))



Symbol	Address	After Reset
U0MR	00A0h	00h
U2MR	0160h	00h

Bit Symbol	Bit Name	Function	RW
SMD0	Serial I/O mode select bits	b2 b1 b0 0 0 0 : Serial interface disabled 0 0 1 : Clock synchronous serial I/O mode 1 0 0 : UART mode transfer data 7 bits long 1 0 1 : UART mode transfer data 8 bits long 1 1 0 : UART mode transfer data 9 bits long Other than above : Do not set.	RW
SMD1			RW
SMD2			RW
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock	RW
STPS	Stop bit length select bit	0 : 1 stop bit 1 : 2 stop bits	RW
PRY	Odd/even parity select bit	Enable when PRYE = 1 0 : Odd parity 1 : Even parity	RW
PRYE	Parity enable bit	0 : Parity disabled 1 : Parity enabled	RW
— (b7)	Reserved bit	Set to 0.	RW

UARTi Bit Rate Register (i = 0 or 2 (for R8C/2H Group only))(1, 2, 3)



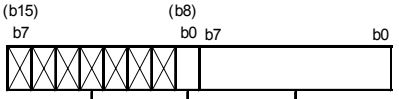
Symbol	Address	After Reset
U0BRG	00A1h	Undefined
U2BRG	0161h	Undefined

Function	Setting Range	RW
Assuming the set value is n, UiBRG divides the count source by n+1	00h to FFh	WO

NOTES:
1. Write to this register while the serial I/O is neither transmitting nor receiving.
2. Use the MOV instruction to write to this register.
3. After setting the CLK0 to CLK1 bits of the UiC0 register, write to the UiBRG register.

Figure 18.3 Registers U0MR, U2MR and U0BRG, U2BRG

UARTi Transmit Buffer Register (i = 0 or 2 (for R8C/2H Group only))(1, 2)

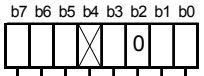


Symbol	Address	After Reset
U0TB	00A3h-00A2h	Undefined
U2TB	0163h-0162h	Undefined

Function		RW
— (b8-b0)	Transmit data	WO
— (b15-b9)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.	—

NOTES:
1. When the transfer data length is 9 bits, write data to high byte first, then low byte.
2. Use the MOV instruction to write to this register.

UARTi Transmit/Receive Control Register 0 (i = 0 or 2 (for R8C/2H Group only))



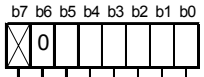
Symbol	Address	After Reset
U0C0	00A4h	00001000b
U2C0	0164h	00001000b

Bit Symbol	Bit Name	Function	RW
CLK0	BRG count source select bits(1)	b1 b0 0 0 : Selects f1 0 1 : Selects f8 1 0 : Selects f32 1 1 : Do not set.	RW
CLK1			RW
— (b2)	Reserved bit	Set to 0.	RW
TXEPT	Transmit register empty flag	0 : Data in transmit register (during transmit) 1 : No data in transmit register (transmit completed)	RO
— (b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
NCH	Data output select bit	0 : TXDi pin is for CMOS output 1 : TXDi pin is for N-channel open-drain output	RW
CKPOL	CLK polarity select bit	0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge	RW
UFORM	Transfer format select bit	0 : LSB first 1 : MSB first	RW

NOTE:
1. If the BRG count source is switched, set the UiBRG register again.

Figure 18.4 Registers U0TB, U2TB and U0C0, U2C0

UARTi Transmit/Receive Control Register 1 (i = 0 or 2 (for R8C/2H Group only))

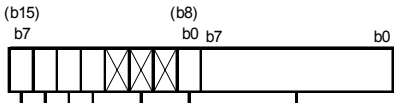


Symbol	Address	After Reset
U0C1	00A5h	00000010b
U2C1	0165h	00000010b

Bit Symbol	Bit Name	Function	RW
TE	Transmit enable bit	0 : Disables transmission 1 : Enables transmission	RW
TI	Transmit buffer empty flag	0 : Data in UiTB register 1 : No data in UiTB register	RO
RE	Receive enable bit	0 : Disables reception 1 : Enables reception	RW
RI	Receive complete flag(1)	0 : No data in UiRB register 1 : Data in UiRB register	RO
UiIRS	UARTi transmit interrupt cause select bit	0 : Transmission buffer empty (TI=1) 1 : Transmission completed (TXEPT=1)	RW
UiRRM	UARTi continuous receive mode enable bit(2)	0 : Disables continuous receive mode 1 : Enables continuous receive mode	RW
— (b6)	Reserved bit	Set to 0.	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

NOTES:
1. The RI bit is set to 0 when the higher byte of the UiRB register is read out.
2. Set the UiRRM bit to 0 (disables continuous receive mode) in UART mode.

UARTi Receive Buffer Register (i = 0 or 2 (for R8C/2H Group only))(1)



Symbol	Address	After Reset
U0RB	00A7h-00A6h	Undefined
U2RB	0167h-0166h	Undefined

Bit Symbol	Bit Name	Function	RW
— (b7-b0)	—	Receive data (D7 to D0)	RO
— (b8)	—	Receive data (D8)	RO
— (b11-b9)	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
OER	Overrun error flag(2)	0 : No overrun error 1 : Overrun error	RO
FER	Framing error flag(2)	0 : No framing error 1 : Framing error	RO
PER	Parity error flag(2)	0 : No parity error 1 : Parity error	RO
SUM	Error sum flag(2)	0 : No error 1 : Error	RO

NOTES:
1. Read out the UiRB register in 16-bit units.
2. Bits SUM, PER, FER, and OER are set to 0 (no error) when bits SMD2 to SMD0 in the UiMR register are set to 000b (serial interface disabled) or the RE bit in the UiC1 register is set to 0 (receive disabled). The SUM bit is set to 0 (no error) when bits PER, FER, and OER are set to 0 (no error). Bits PER and FER are set to 0 even when the higher byte of the UiRB register is read out.
   Also, bits PER and FER are set to 0 when reading the high-order byte of the UiRB register.

Figure 18.5 Registers U0C1, U2C1 and U0RB, U2RB

18.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 18.1 lists the Clock Synchronous Serial I/O Mode Specifications. Table 18.2 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode(1).

Table 18.1 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits
Transfer clocks	• CKDIR bit in UiMR register is set to 0 (internal clock): fi/(2(n+1)) fi = f1, f8, f32 n = value set in UiBRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): input from CLKi pin
Transmit start conditions	• Before transmission starts, the following requirements must be met(1) - The TE bit in the UiC1 register is set to 1 (transmission enabled) - The TI bit in the UiC1 register is set to 0 (data in the UiTB register)
Receive start conditions	• Before reception starts, the following requirements must be met(1) - The RE bit in the UiC1 register is set to 1 (reception enabled) - The TE bit in the UiC1 register is set to 1 (transmission enabled) - The TI bit in the UiC1 register is set to 0 (data in the UiTB register)
Interrupt request generation timing	• When transmitting, one of the following conditions can be selected - The UiIRS bit is set to 0 (transmit buffer empty): When transferring data from the UiTB register to UARTi transmit register (when transmission starts). - The UiIRS bit is set to 1 (transmission completes): When completing data transmission from UARTi transmit register. • When receiving When data transfer from the UARTi receive register to the UiRB register (when reception completes).
Error detection	• Overrun error(2) This error occurs if the serial interface starts receiving the next data item before reading the UiRB register and receives the 7th bit of the next data.
Select functions	• CLK polarity selection Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock. • LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Receive is enabled immediately by reading the UiRB register.

i = 0 or 2 (for the R8C/2H Group only)
NOTES:

1. If an external clock is selected, ensure that the external clock is “H” when the CKPOL bit in the UiC0 register is set to 0 (transmit data output at falling edge and receive data input at rising edge of transfer clock), and that the external clock is “L” when the CKPOL bit is set to 1 (transmit data output at rising edge and receive data input at falling edge of transfer clock).
2. If an overrun error occurs, the receive data (b0 to b8) of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 18.2 Registers Used and Settings in Clock Synchronous Serial I/O Mode(1)

Register	Bit	Function
UiTB	0 to 7	Set data transmission
UiRB	0 to 7	Data reception can be read
	OER	Overrun error flag
UiBRG	0 to 7	Set bit rate
UiMR	SMD2 to SMD0	Set to 001b
	CKDIR	Select the internal clock or external clock
UiC0	CLK1 to CLK0	Select the count source in the UiBRG register
	TXEPT	Transmit register empty flag
	NCH	Select TXDi pin output mode
	CKPOL	Select the transfer clock polarity
	UFORM	Select the LSB first or MSB first
UiC1	TE	Set this bit to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set this bit to 1 to enable reception
	RI	Reception complete flag
	UiIRS	Select the UARTi transmit interrupt source
	UiRRM	Set this bit to 1 to use continuous receive mode

i = 0 or 2 (for the R8C/2H Group only)

NOTE:

1. Set bits which are not in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 18.3 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode. The TXDi pin outputs “H” level between the operating mode selection of UARTi (i = 0 or 2 (for the R8C/2H Group only)) and transfer start. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in a high-impedance state.)

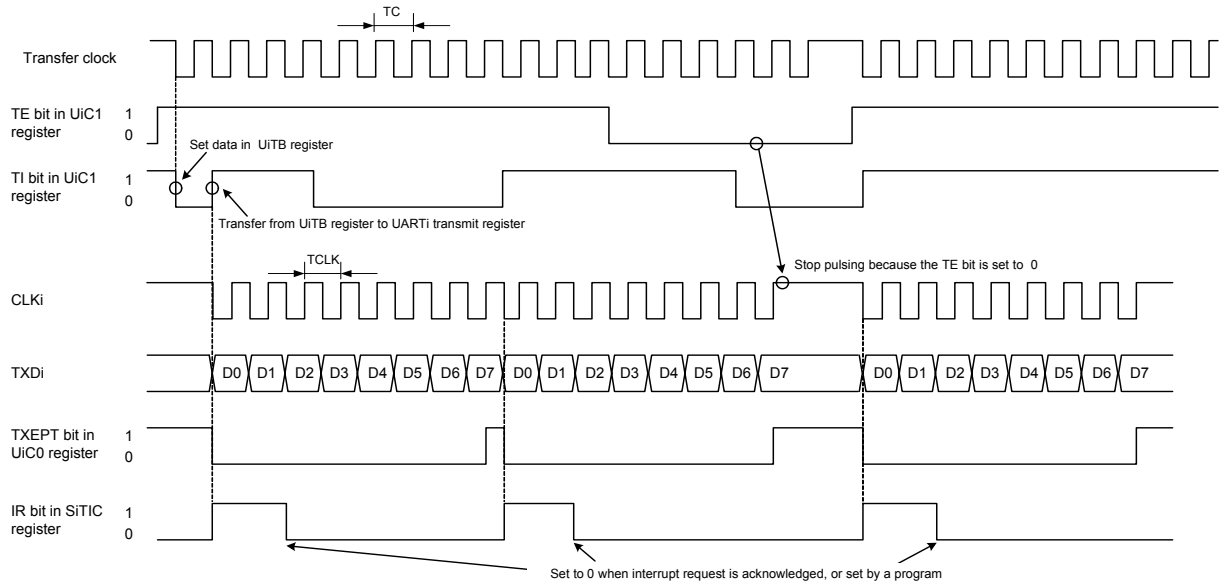
Table 18.3 I/O Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Selection Method
TXD0 (P1_4)	Output serial data	(Outputs dummy data when performing reception only)
RXD0 (P1_5)	Input serial data	PD1_5 bit in PD1 register = 0 (P1_5 can be used as an input port when performing transmission only)
CLK0 (P1_6)	Output transfer clock	CKDIR bit in U0MR register = 0
	Input transfer clock	CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0
TXD2 (P6_3)(1)	Output serial data	(Outputs dummy data when performing reception only)
RXD2 (P6_4)(1)	Input serial data	PD6_4 bit in PD6 register = 0 (P6_4 can be used as an input port when performing transmission only)
CLK2 (P6_5)(1)	Output transfer clock	CKDIR bit in U2MR register = 0
	Input transfer clock	CKDIR bit in U2MR register = 1 PD6_5 bit in PD6 register = 0

NOTE:

1. Applicable to the R8C/2H Group only.

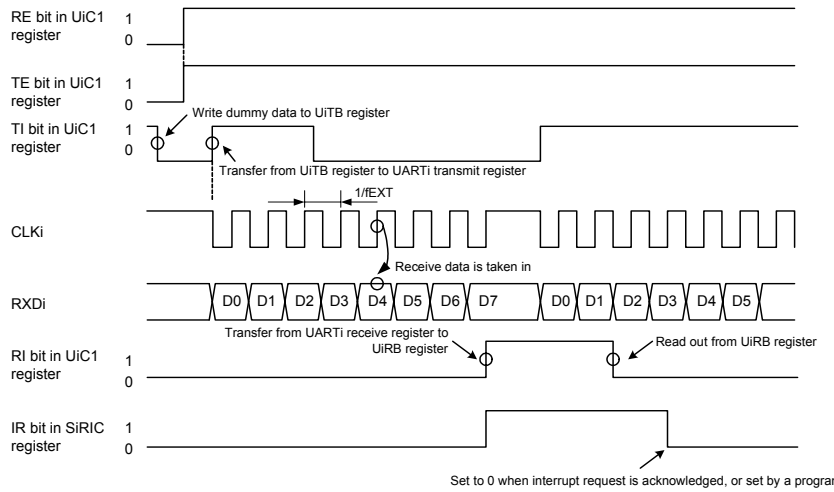
• Example of transmit timing (when internal clock is selected)



TC=TCLK=2(n+1)/fi
fi: Frequency of UiBRG count source (f1, f8, f32)
n: Setting value to UiBRG register

The above applies under the following settings:
- CKDIR bit in UiMR register = 0 (internal clock)
- CKPOL bit in UiC0 register = 0 (output transmit data at the falling edge and input receive data at the rising edge of the transfer clock)
- UiIRS bit in UiC1 register = 0 (an interrupt request is generated when the transmit buffer is empty)

• Example of receive timing (when external clock is selected)



The above applies under the following settings:
- CKDIR bit in UiMR register = 1 (external clock)
- CKPOL bit in UiC0 register = 0 (output transmit data at the falling edge and input receive data at the rising edge of the transfer clock)

The following conditions are met when “H” is applied to the CLKi pin before receiving data:
- TE bit in UiC1 register = 1 (enables transmit)
- RE bit in UiC1 register = 1 (enables receive)
- Write dummy data to the UiTB register

fEXT: Frequency of external clock

i = 0 or 2 (for the R8C/2H Group only)

Figure 18.6 Transmit and Receive Timing Example in Clock Synchronous Serial I/O Mode

18.1.1 Polarity Select Function

Figure 18.7 shows the Transfer Clock Polarity. Use the CKPOL bit in the UiC0 (i = 0 or 2 (for the R8C/2H Group only)) register to select the transfer clock polarity.

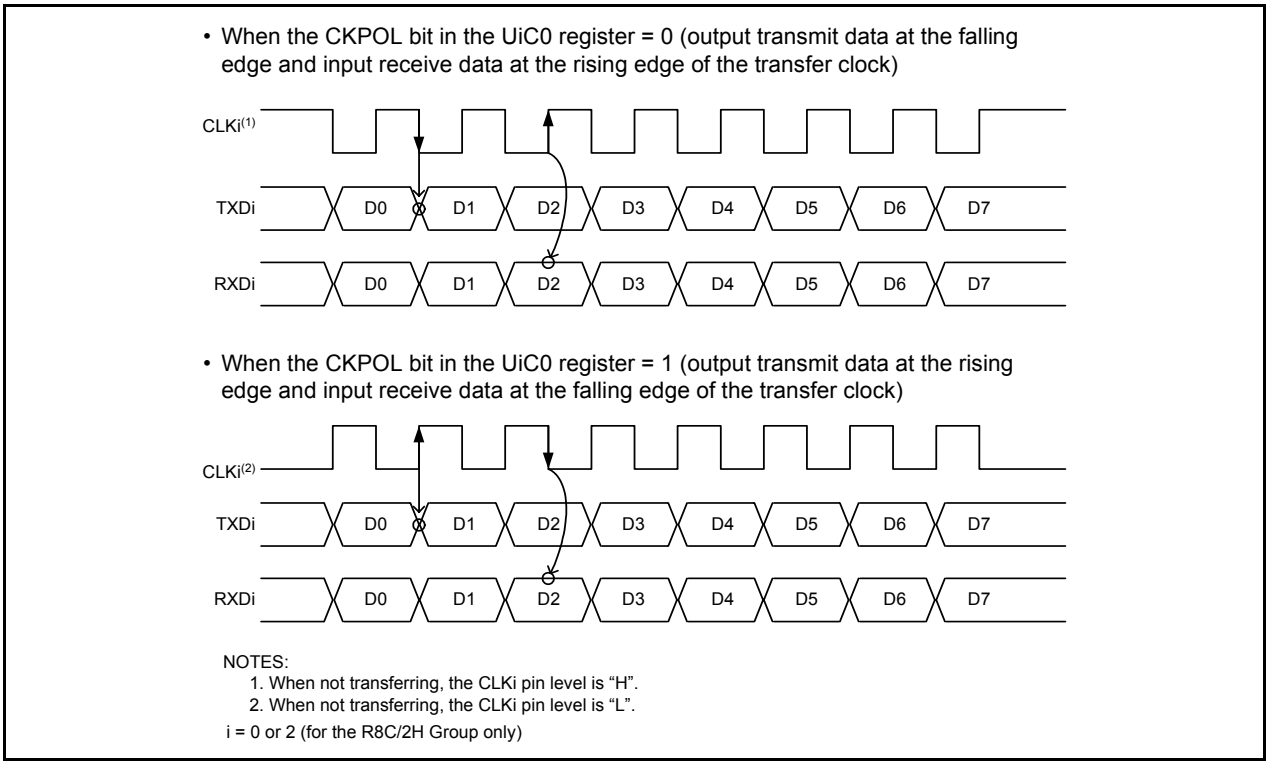


Figure 18.7 Transfer Clock Polarity

18.1.2 LSB First/MSB First Select Function

Figure 18.8 shows the Transfer Format. Use the UFORM bit in the UiC0 (i = 0 or 2 (for the R8C/2H Group only)) register to select the transfer format.

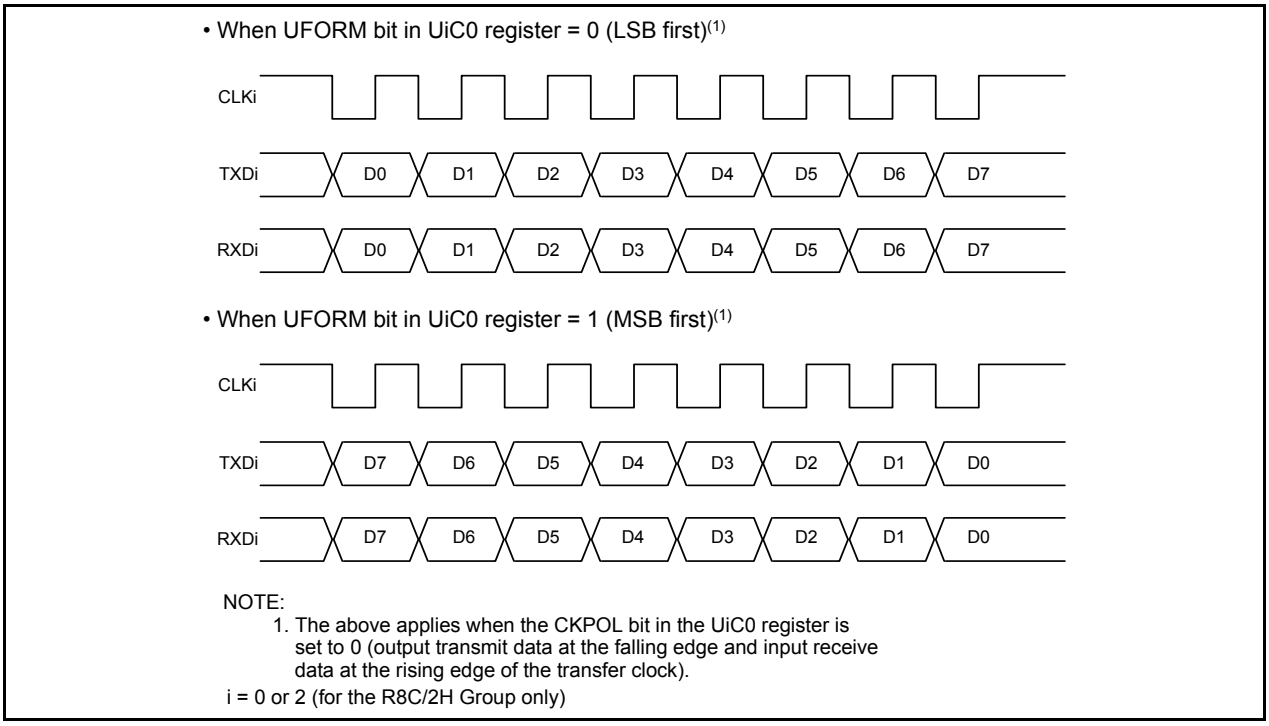


Figure 18.8 Transfer Format

18.1.3 Continuous Receive Mode

Continuous receive mode is selected by setting the UiRRM (i = 0 or 2 (for the R8C/2H Group only)) bit in the UiC1 register to 1 (enables continuous receive mode). In this mode, reading the UiRB register sets the TI bit in the UiC1 register to 0 (data in the UiTB register). When the UiRRM bit is set to 1, do not write dummy data to the UiTB register by a program.

18.2 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired bit rate and transfer data format. Table 18.4 lists the UART Mode Specifications. Table 18.5 lists the Registers Used and Settings for UART Mode.

Table 18.4 UART Mode Specifications

Item	Specification
Transfer data formats	• Character bit (transfer data): Selectable among 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable among odd, even, or none • Stop bit: Selectable among 1 or 2 bits
Transfer clocks	• CKDIR bit in UiMR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32 n = value set in UiBRG register: 00h to FFh • CKDIR bit is set to 1 (external clock): fEXT/(16(n+1)) fEXT: Input from CLKi pin, n = value set in UiBRG register: 00h to FFh
Transmit start conditions	• Before transmission starts, the following are required - TE bit in UiC1 register is set to 1 (transmission enabled) - TI bit in UiC1 register is set to 0 (data in UiTB register)
Receive start conditions	• Before reception starts, the following are required - RE bit in UiC1 register is set to 1 (reception enabled) - Start bit detected
Interrupt request generation timing	• When transmitting, one of the following conditions can be selected - UiIRS bit is set to 0 (transmit buffer empty): When transferring data from the UiTB register to UARTi transmit register (when transmission starts). - UiIRS bit is set to 1 (transfer ends): When serial interfac.e completes transmitting data from the UARTi transmit register • When receiving When transferring data from the UARTi receive register to UiRB register (when reception ends).
Error detection	• Overrun error(1) This error occurs if the serial interface starts receiving the next data item before reading the UiRB register and receive the bit preceding the final stop bit of the next data item. • Framing error This error occurs when the set number of stop bits is not detected. • Parity error This error occurs when parity is enabled, and the number of 1's in parity and character bits do not match the number of 1's set. • Error sum flag This flag is set is set to 1 when an overrun, framing, or parity error is generated.

i = 0 or 2 (for the R8C/2H Group only)

NOTE:

1. If an overrun error occurs, the receive data (b0 to b8) of the UiRB register will be undefined. The IR bit in the SiRIC register remains unchanged.

Table 18.5 Registers Used and Settings for UART Mode

Register	Bit	Function
UiTB	0 to 8	Set transmit data(1)
UiRB	0 to 8	Receive data can be read(1, 2)
	OER,FER,PER,SUM	Error flag
UiBRG	0 to 7	Set a bit rate
UiMR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long Set to 101b when transfer data is 8 bits long Set to 110b when transfer data is 9 bits long
	CKDIR	Select the internal clock or external clock
	STPS	Select the stop bit
	PRY, PRYE	Select whether parity is included and whether odd or even
UiC0	CLK0, CLK1	Select the count source for the UiBRG register
	TXEPT	Transmit register empty flag
	NCH	Select TXDi pin output mode
	CKPOL	Set to 0
	UFORM	LSB first or MSB first can be selected when transfer data is 8 bits long. Set to 0 when transfer data is 7 or 9 bits long.
UiC1	TE	Set to 1 to enable transmit
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable receive
	RI	Receive complete flag
	UiIRS	Select the source of UARTi transmit interrupt
	UiRRM	Set to 0

i = 0 or 2 (for the R8C/2H Group only)

NOTES:

1. The bits used for transmit/receive data are as follows: Bits 0 to 6 when transfer data is 7 bits long; bits 0 to 7 when transfer data is 8 bits long; bits 0 to 8 when transfer data is 9 bits long.
2. The following bits are undefined: Bits 7 and 8 when transfer data is 7 bits long; bit 8 when transfer data is 8 bits long.

Table 18.6 lists the I/O Pin Functions in UART Mode. After the UARTi (i = 0 or 2 (for the R8C/2H Group only)) operating mode is selected, the TXDi pin outputs “H” level. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in a high-impedance state) until transfer starts.)

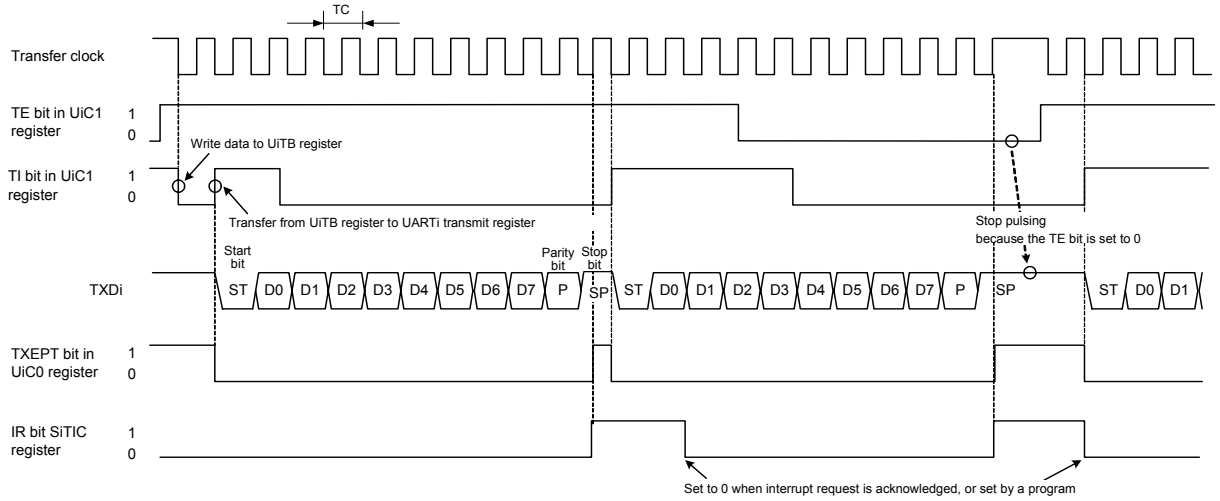
Table 18.6 I/O Pin Functions in UART Mode

Pin name	Function	Selection Method
TXD0 (P1_4)	Output serial data	(Cannot be used as a port when performing reception only)
RXD0 (P1_5)	Input serial data	PD1_5 bit in PD1 register = 0 (P1_5 can be used as an input port when performing transmission only)
CLK0 (P1_6)	Programmable I/O Port	CKDIR bit in U0MR register = 0
	Input transfer clock	CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0
TXD2 (P6_3)(1)	Output serial data	(Cannot be used as a port when performing reception only)
RXD2 (P6_4)(1)	Input serial data	PD6_4 bit in PD6 register = 0 (P6_4 can be used as an input port when performing transmission only)
CLK2 (P6_5)(1)	Programmable I/O Port	CKDIR bit in U2MR register = 0
	Input transfer clock	CKDIR bit in U2MR register = 1 PD6_5 bit in PD6 register = 0

NOTE:

1. Applicable to the R8C/2H Group only.

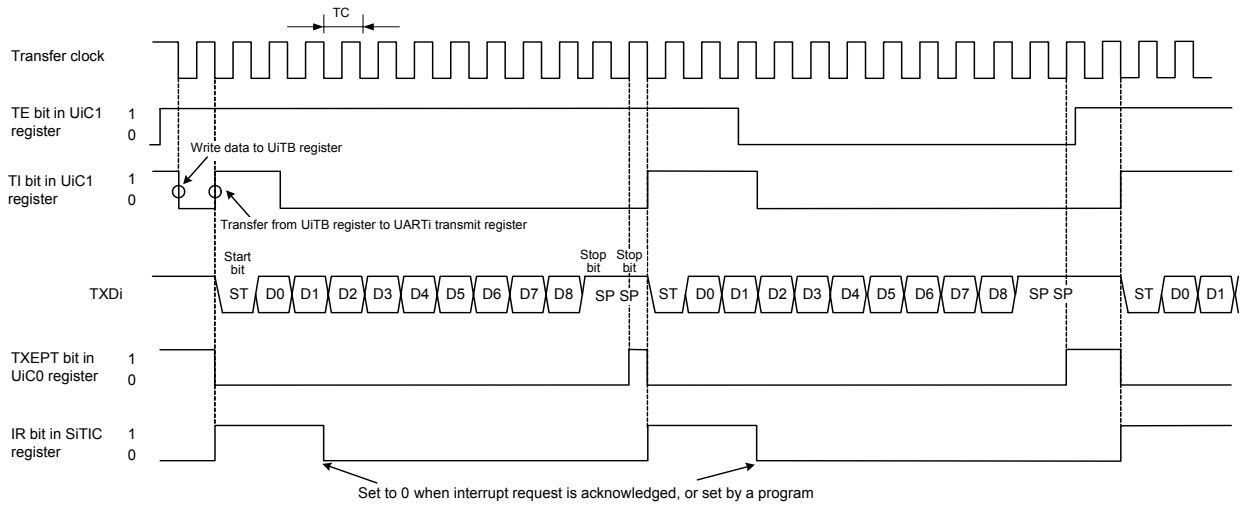
• Transmit timing when transfer data is 8 bits long (parity enabled, 1 stop bit)



The above timing diagram applies under the following conditions:
- PRYE bit in UiMR register = 1 (parity enabled)
- STPS bit in UiMR register = 0 (1 stop bit)
- UiIRS bit in UiC1 register = 1 (an interrupt request is generated when transmit completes)

TC=16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value to UiBRG register
i = 0 or 2 (for the R8C/2H Group only)

• Transmit timing when transfer data is 9 bits long (parity disabled, 2 stop bits)



The above timing diagram applies under the following conditions:
- PRYE bit in UiMR register = 0 (parity disabled)
- STPS bit in UiMR register = 1 (2 stop bits)
- UiIRS bit in UiC1 register = 0 (an interrupt request is generated when transmit buffer is empty)

TC=16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value to UiBRG register
i = 0 or 2 (for the R8C/2H Group only)

Figure 18.9 Transmit Timing in UART Mode

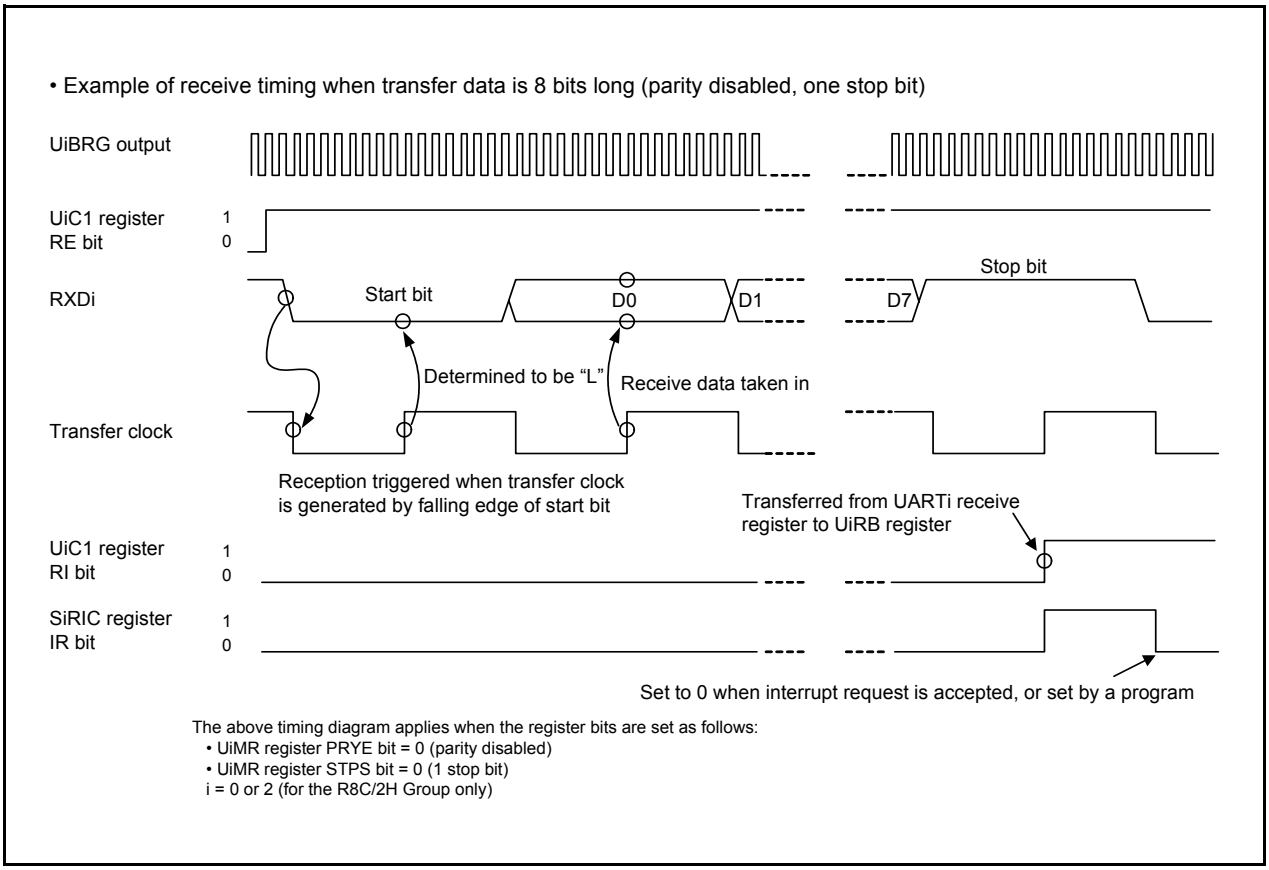


Figure 18.10 Receive Timing Example in UART Mode

18.2.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the UiBRG (i = 0 or 2 (for the R8C/2H Group only)) register.

UART mode

• Internal clock selected

$$\text{UiBRG register setting value} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

Fj: Count source frequency of the UiBRG register (f1, f8, or f32)

• External clock selected

$$\text{UiBRG register setting value} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT: Count source frequency of the UiBRG register (external clock)

i = 0 or 2 (for the R8C/2H Group only)

Figure 18.11 Calculation Formula of UiBRG (i = 0 or 2 (for R8C/2H Group only)) Register Setting Value

Table 18.7 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	BRG Count Source	System Clock = 8 MHz		
		UiBRG Setting Value	Actual Time (bps)	Error (%)
1200	f8	51 (33h)	1201.92	0.16
2400	f8	25 (19h)	2403.85	0.16
4800	f8	12 (0Ch)	4807.69	0.16
9600	f1	51 (33h)	9615.38	0.16
14400	f1	34 (22h)	14285.71	-0.79
19200	f1	25 (19h)	19230.77	0.16
28800	f1	16 (10h)	29411.76	2.12
31250	f1	15 (0Fh)	31250.00	0.00
38400	f1	12 (0Ch)	38461.54	0.16
51200	f1	9 (09h)	50000.00	-2.34

18.3 Notes on Serial Interface

- When reading data from the UiRB (i = 0 or 2 (for the R8C/2H Group only)) register either in the clock synchronous serial I/O mode or in the clock asynchronous serial I/O mode. Ensure the data is read in 16-bit units. When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0.
  To check receive errors, read the UiRB register and then use the read data.

Example (when reading receive buffer register):

```
MOV.W    00A6H,R0    ; Read the U0RB register
```

- When writing data to the UiTB register in the clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first then the low-order byte, in 8-bit units.

Example (when reading transmit buffer register):

```
MOV.B    #XXH,00A3H  ; Write the high-order byte of U0TB register
MOV.B    #XXH,00A2H  ; Write the low-order byte of U0TB register
```

19. Hardware LIN

The hardware LIN performs LIN communication in cooperation with timer RA and UART0.

19.1 Features

The hardware LIN has the features listed below.
Figure 19.1 shows a Block Diagram of Hardware LIN.

Master mode

- Generates Synch Break
- Detects bus collision

Slave mode

- Detects Synch Break
- Measures Synch Field
- Controls Synch Break and Synch Field signal inputs to UART0
- Detects bus collision

NOTE:
1. The WakeUp function is detected by INT1.

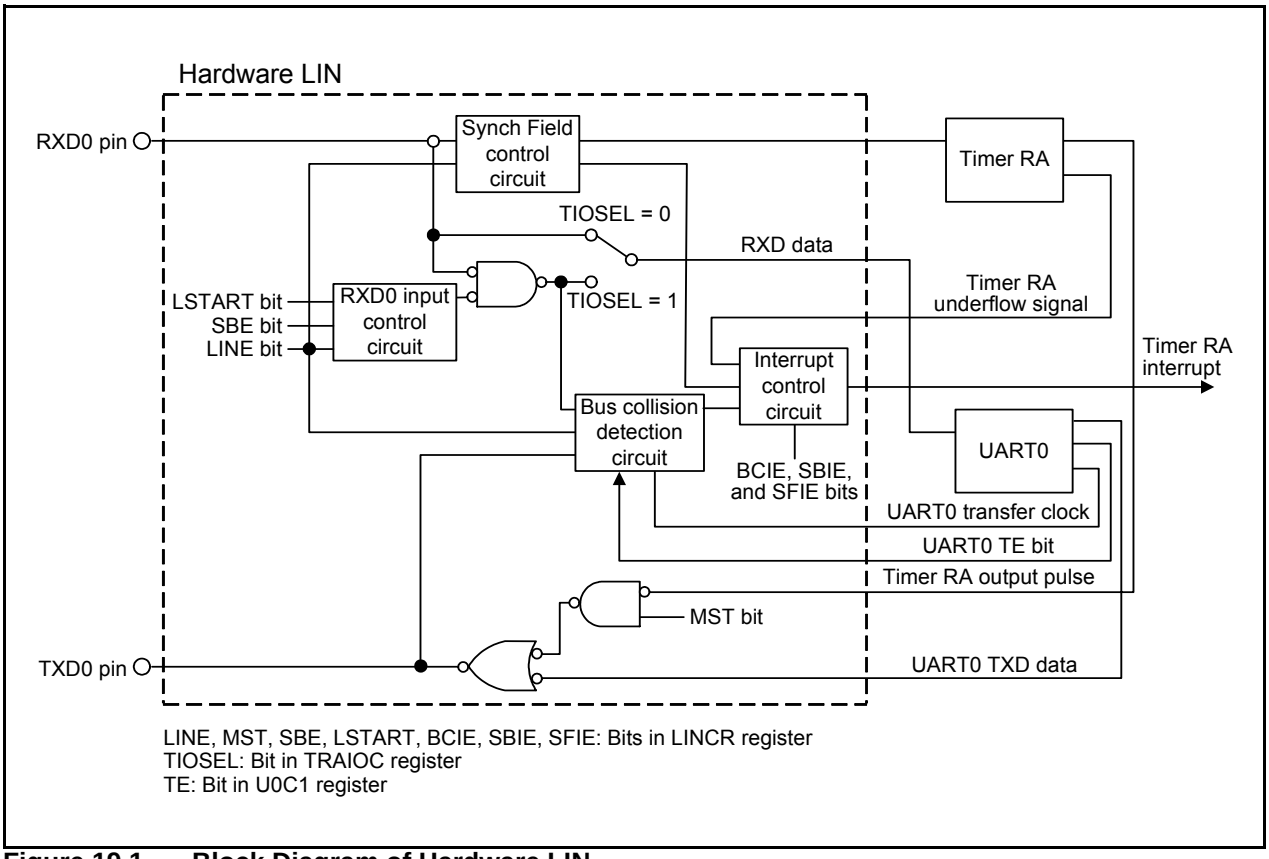


Figure 19.1 Block Diagram of Hardware LIN

19.2 Input/Output Pins

The pin configuration of the hardware LIN is listed in Table 19.1.

Table 19.1 Pin Configuration

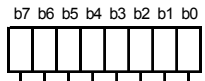
Name	Abbreviation	Input/Output	Function
Receive data input	RXD0	Input	Receive data input pin of the hardware LIN
Transmit data output	TXD0	Output	Transmit data output pin of the hardware LIN

19.3 Register Configuration

The hardware LIN contains the registers listed below.
These registers are detailed in Figures 19.2 and 19.3.

- LIN Control Register (LINCR)
- LIN Status Register (LINST)

LIN Control Register



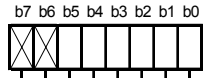
Symbol	Address	After Reset
LINCR	0106h	00h

Bit Symbol	Bit Name	Function	RW
SFIE	Synch Field measurement-completed interrupt enable bit	0 : Disables Synch Field measurement-completed interrupt 1 : Enables Synch Field measurement-completed interrupt	RW
SBIE	Synch Break detection interrupt enable bit	0 : Disables Synch Break detection interrupt 1 : Enables Synch Break detection interrupt	RW
BCIE	Bus collision detection interrupt enable bit	0 : Disables bus collision detection interrupt 1 : Enables bus collision detection interrupt	RW
RXDSF	RXD0 input status flag	0 : RXD0 input enabled 1 : RXD0 input disabled	RO
LSTART	Synch Break detection start bit(1)	When this bit is set to 1, timer RA input is enabled and RXD0 input is disabled. When read, the content is 0.	RW
SBE	RXD0 input unmasking timing select bit (effective only in slave mode)	0 : Unmasked after Synch Break is detected 1 : Unmasked after Synch Field measurement is completed	RW
MST	LIN operation mode setting bit(2)	0 : Slave mode (Synch Break detection circuit actuated) 1 : Master mode (timer RA output OR'ed with TXD0)	RW
LINE	LIN operation start bit	0 : Causes LIN to stop 1 : Causes LIN to start operating(3)	RW

NOTES:
1. After setting the LSTART bit, confirm that the RXDSF flag is set to 1 before Synch Break input starts.
2. Before changing LIN operation modes, temporarily stop the LIN operation (LINE bit = 0).
3. Inputs to timer RA and UART0 are prohibited immediately after this bit is set to 1. (Refer to **Figure 19.5 Example of Header Field Transmission Flowchart (1)** and **Figure 19.9 Example of Header Field Reception Flowchart (2)**.)

Figure 19.2 LINCR Register

LIN Status Register



Symbol	Address	After Reset
LINST	0107h	00h

Bit Symbol	Bit Name	Function	RW
SFDCT	Synch Field measurement-completed flag	1 shows Synch Field measurement completed.	RO
SBDCT	Synch Break detection flag	1 shows Synch Break detected or Synch Break generation completed.	RO
BCDCT	Bus collision detection flag	1 shows Bus collision detected.	RO
B0CLR	SFDCT bit clear bit	When this bit is set to 1, the SFDCT bit is set to 0. When read, the content is 0.	RW
B1CLR	SBDCT bit clear bit	When this bit is set to 1, the SBDCT bit is set to 0. When read, the content is 0.	RW
B2CLR	BCDCT bit clear bit	When this bit is set to 1, the BCDCT bit is set to 0. When read, the content is 0.	RW
— (b7-b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Figure 19.3 LINST Register

19.4 Functional Description

19.4.1 Master Mode

Figure 19.4 shows typical operation of the hardware LIN when transmitting a header field in master mode. Figures 19.5 and 19.6 show an Example of Header Field Transmission Flowchart.
When transmitting a header field, the hardware LIN operates as described below.

(1) When the TSTART bit in the TRACR register for timer RA is set by writing 1 in software, the hardware LIN outputs “L” level from the TXD0 pin for the period that is set in registers TRAPRE and TRA for timer RA.
(2) When timer RA underflows upon reaching the terminal count, the hardware LIN reverses the output of the TXD0 pin and sets the SBDCT flag in the LINST register to 1. Furthermore, if the SBIE bit in the LINCR register is set to 1, it generates a timer RA interrupt.
(3) The hardware LIN transmits 55h via UART0.
(4) The hardware LIN transmits an ID field via UART0 after it finishes sending 55h.
(5) The hardware LIN performs communication for a response field after it finishes sending the ID field.

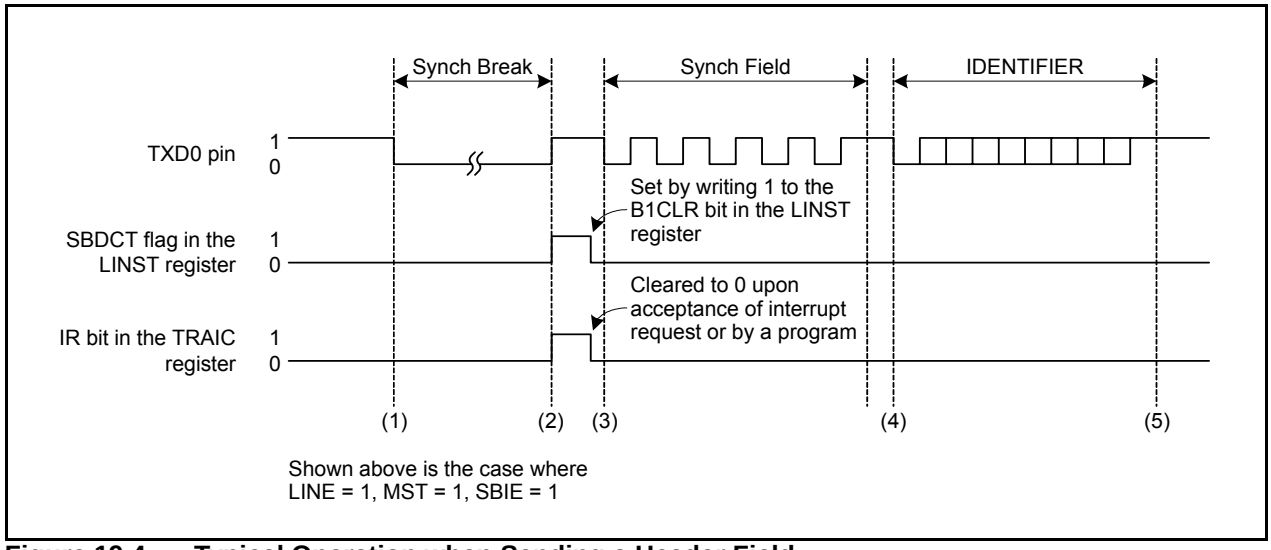


Figure 19.4 Typical Operation when Sending a Header Field

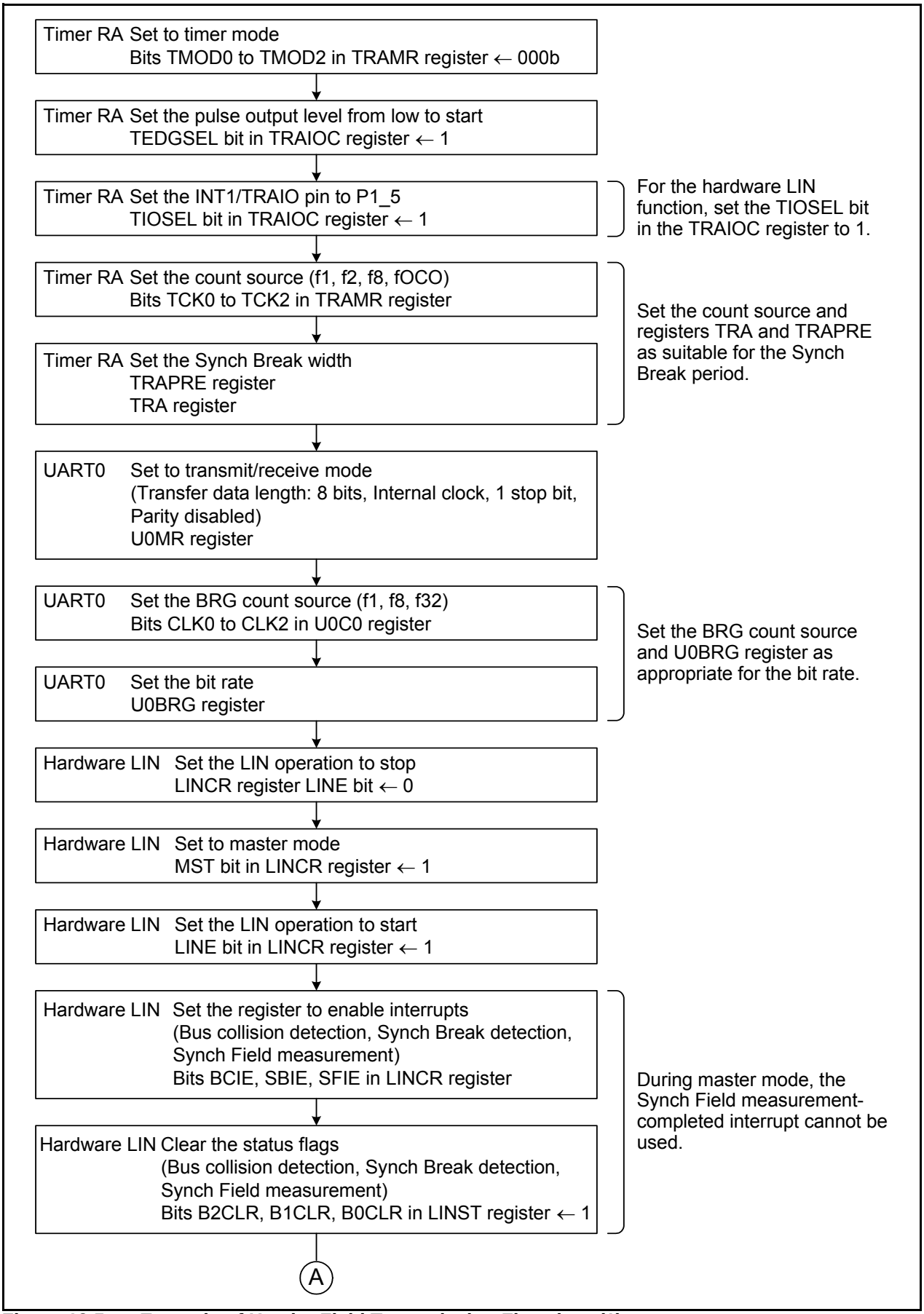


Figure 19.5 Example of Header Field Transmission Flowchart (1)

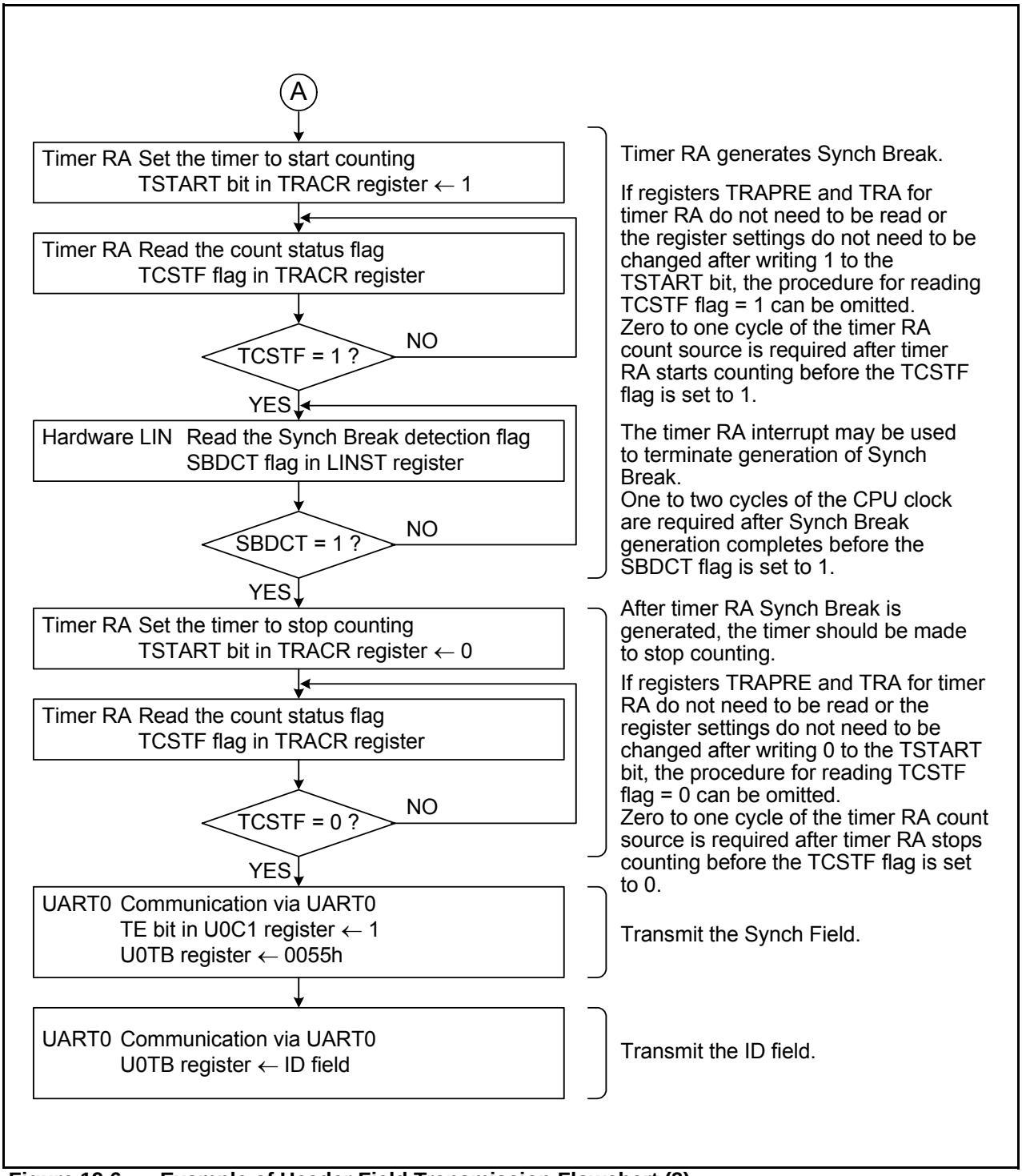


Figure 19.6 Example of Header Field Transmission Flowchart (2)

19.4.2 Slave Mode

Figure 19.7 shows typical operation of the hardware LIN when receiving a header field in slave mode. Figure 19.8 through Figure 19.10 show an Example of Header Field Reception Flowchart.
When receiving a header field, the hardware LIN operates as described below.

(1) Synch Break detection is enabled by writing 1 to the LSTART bit in the LINCR register of the hardware LIN.
(2) When "L" level is input for a duration equal to or greater than the period set in timer RA, the hardware LIN detects it as Synch Break. At this time, the SBDCT flag in the LINST register is set to 1. Furthermore, if the SBIE bit in the LINCR register is set to 1, the hardware LIN generates a timer RA interrupt. Then it goes to Synch Field measurement.
(3) The hardware LIN receives a Synch Field (55h). At this time, it measures the period of the start bit and bits 0 to 6 by using timer RA. In this case, it is possible to select whether to input the Synch Field signal to RXD0 of UART0 by setting the SBE bit in the LINCR register accordingly.
(4) The hardware LIN sets the SFDCT flag in the LINST register to 1 when it finishes measuring the Synch Field. Furthermore, if the SFIE bit in the LINCR register is set to 1, it generates a timer RA interrupt.
(5) After it finishes measuring the Synch Field, calculate a transfer rate from the count value of timer RA and set to UART0 and registers TRAPRE and TRA of timer RA again. Then it receives an ID field via UART0.
(6) The hardware LIN performs communication for a response field after it finishes receiving the ID field.

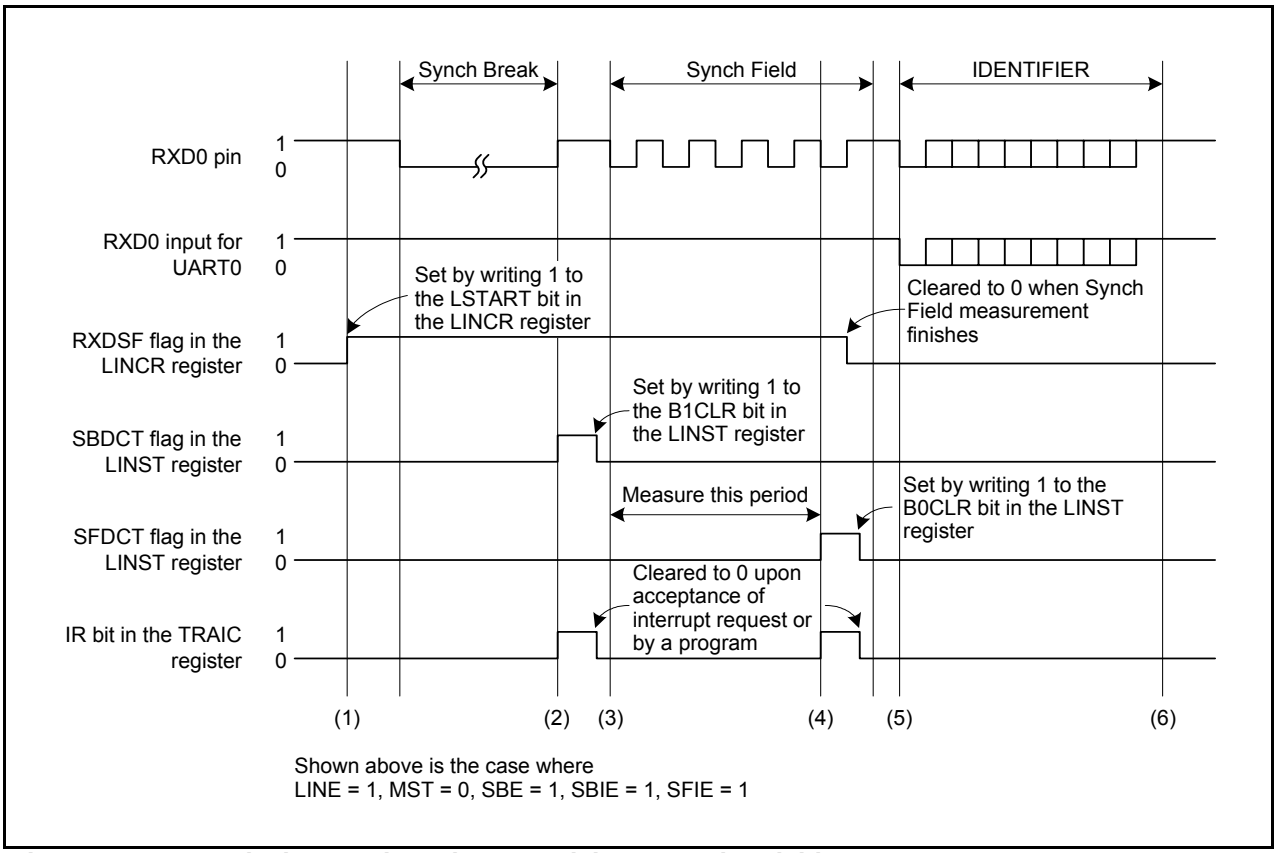


Figure 19.7 Typical Operation when Receiving a Header Field

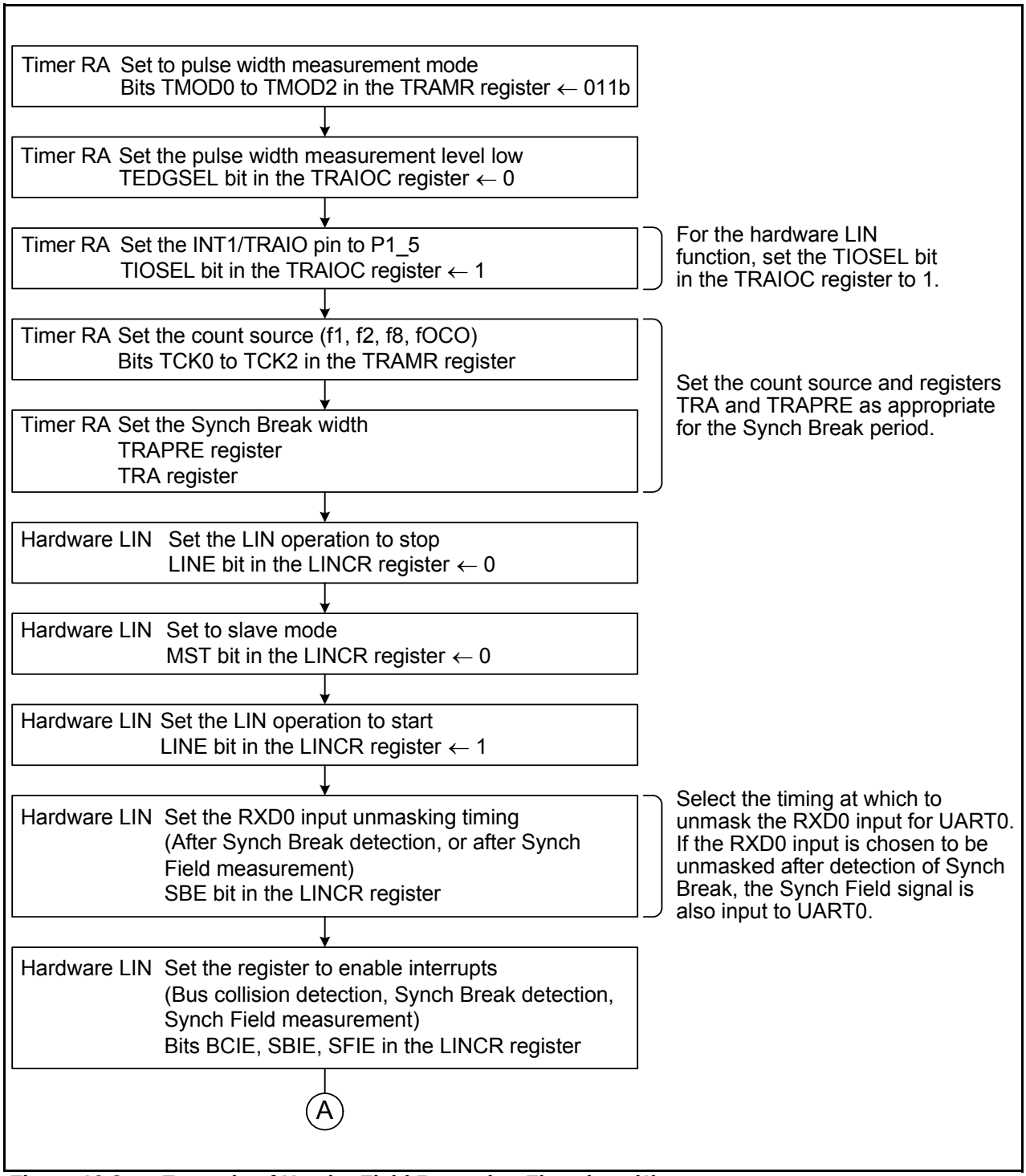


Figure 19.8 Example of Header Field Reception Flowchart (1)

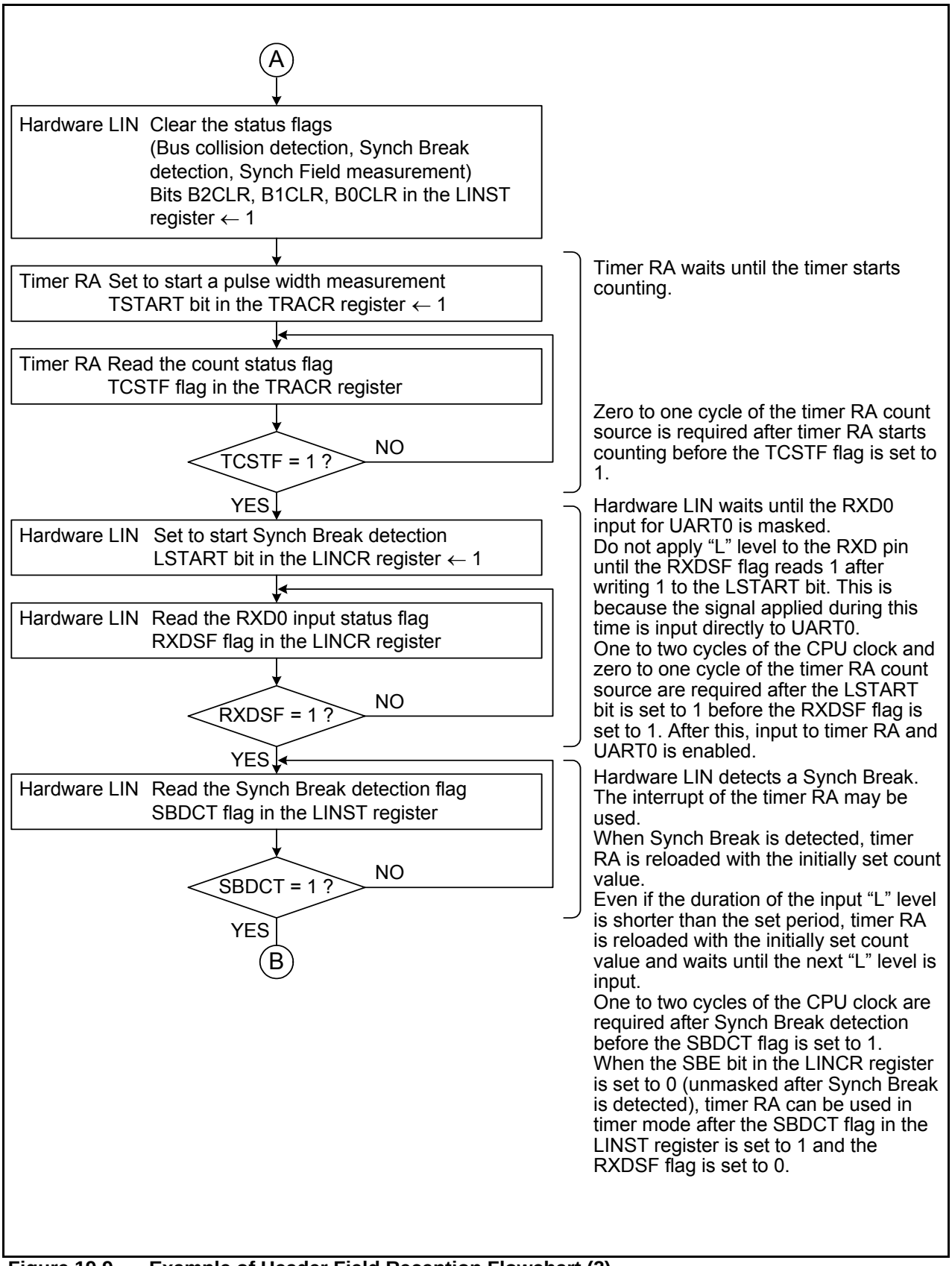


Figure 19.9 Example of Header Field Reception Flowchart (2)

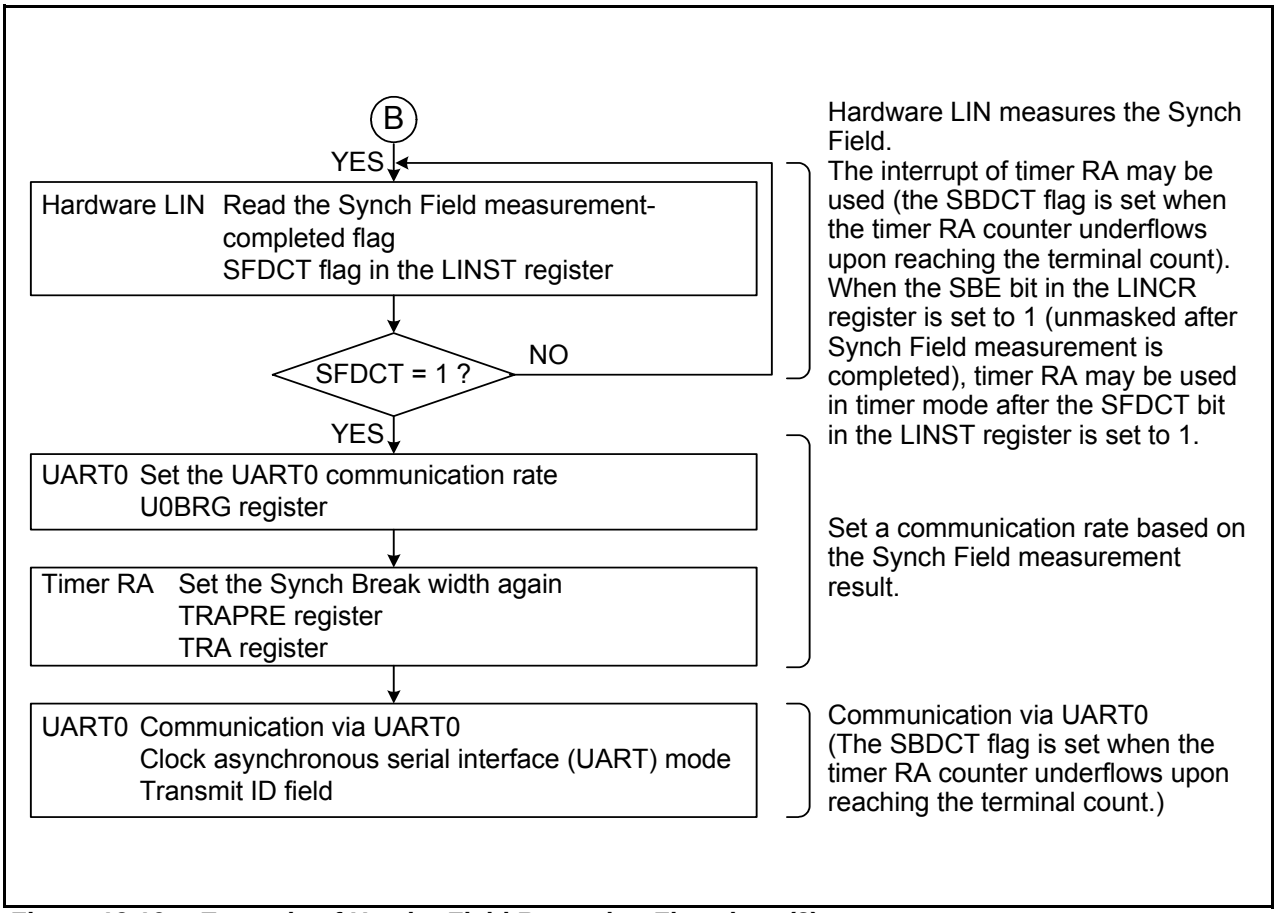


Figure 19.10 Example of Header Field Reception Flowchart (3)

19.4.3 Bus Collision Detection Function

The bus collision detection function can be used when UART0 is enabled for transmission (TE bit in the U0C1 register = 1).
Figure 19.11 shows the Typical Operation when a Bus Collision is Detected.

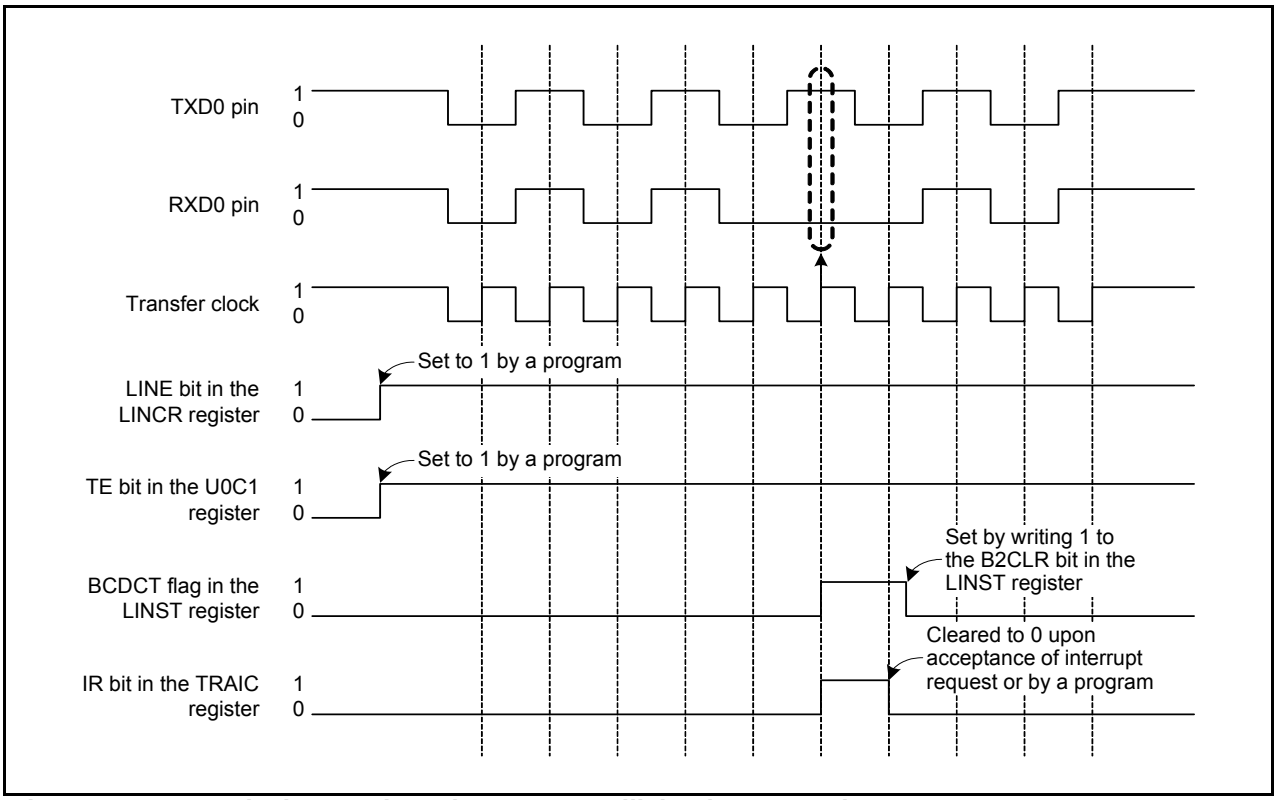


Figure 19.11 Typical Operation when a Bus Collision is Detected

19.4.4 Hardware LIN End Processing

Figure 19.12 shows an Example of Hardware LIN Communication Completion Flowchart.
Use the following timing for hardware LIN end processing:

- If the hardware bus collision detection function is used
  Perform hardware LIN end processing after checksum transmission completes.
- If the bus collision detection function is not used
  Perform hardware LIN end processing after header field transmission and reception complete.

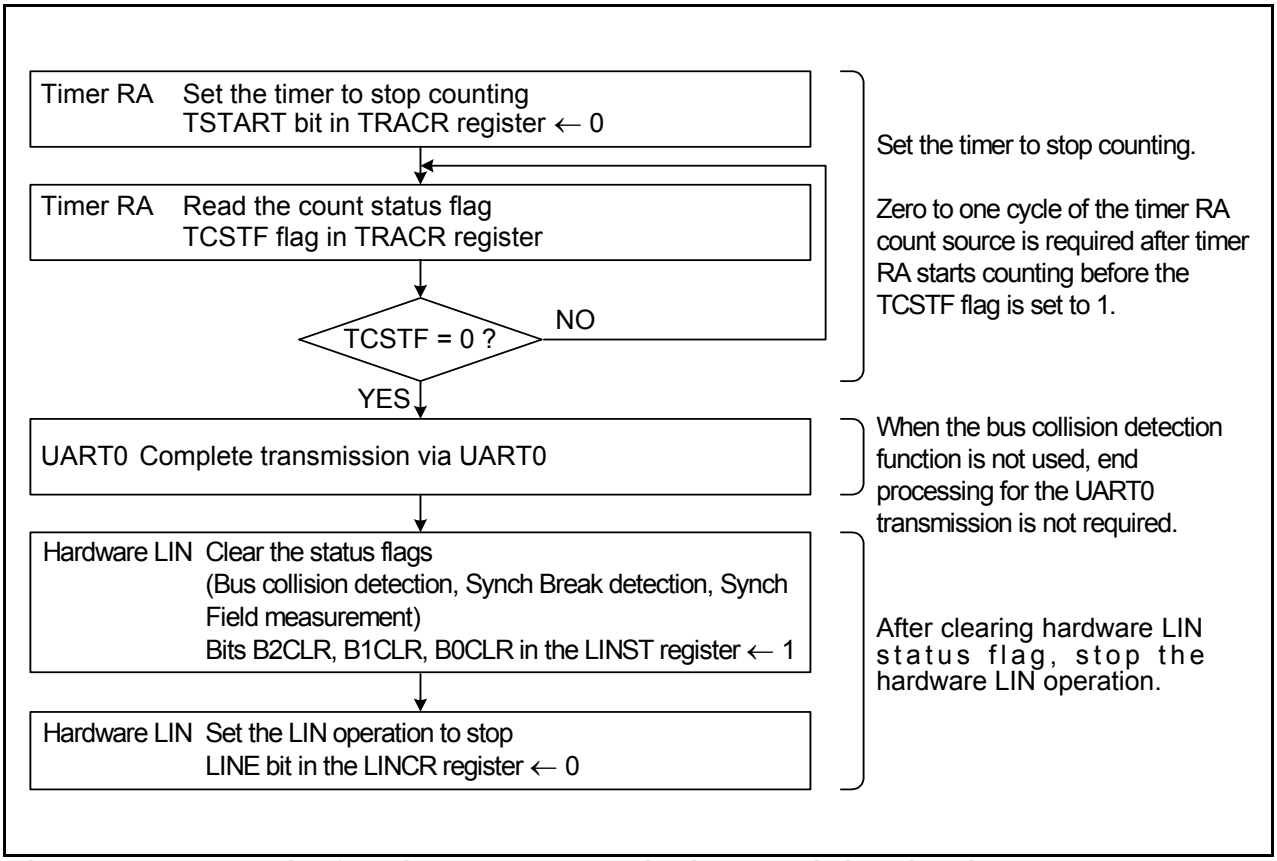


Figure 19.12 Example of Hardware LIN Communication Completion Flowchart

19.5 Interrupt Requests

There are four interrupt requests that are generated by the hardware LIN: Synch Break detection, Synch Break generation completed, Synch Field measurement completed, and bus collision detection. These interrupts are shared with timer RA.
Table 19.2 lists the Interrupt Requests of Hardware LIN.

Table 19.2 Interrupt Requests of Hardware LIN

Interrupt Request	Status Flag	Cause of Interrupt
Synch Break detection	SBDCT	Generated when timer RA has underflowed after measuring the “L” level duration of RXD0 input, or when a “L” level is input for a duration longer than the Synch Break period during communication.
Synch Break generation completed		Generated when “L” level output to TXD0 for the duration set by timer RA completes.
Synch Field measurement completed	SFDCT	Generated when measurement for 6 bits of the Synch Field by timer RA is completed.
Bus collision detection	BCDCT	Generated when the RXD0 input and TXD0 output values differed at data latch timing while UART0 is enabled for transmission.

19.6 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

20. Flash Memory

20.1 Overview

Rewrite operations to the flash memory can be performed in three modes: CPU rewrite, standard serial I/O, and parallel I/O.
Table 20.1 lists the Flash Memory Performance (refer to **Table 1.1 Specifications for R8C/2H Group** and **Table 1.2 Specifications for R8C/2J Group** for items not listed in **Table 20.1**). Table 20.2 lists the Flash Memory Rewrite Modes.

Table 20.1 Flash Memory Performance

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase block		Refer to **Figure 20.1**
Programming method		Byte unit
Erase method		Block erase
Programming and erasure control method		Program and erase control by software command
Protection method		Program ROM protection by FMR0 register
Number of commands		5 commands
Programming and erasure endurance(1)	Block 0 (program ROM)	100 times
Programming and erasure voltage		VCC = 2.7 to 5.5 V
ID code check function		Standard serial I/O mode supported
ROM code protect		Parallel I/O mode supported

NOTE:
1. Definition of programming and erasure endurance.
The programming and erasure endurance is defined on a per-block basis.

Table 20.2 Flash Memory Rewrite Modes

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU.	User ROM area is rewritten by a dedicated serial programmer.	User ROM area is rewritten by a dedicated parallel programmer.
Areas which can be rewritten	User ROM area	User ROM area	User ROM area
Rewrite Program	User program	Standard boot program	–

20.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figure 20.1 shows the Flash Memory Block Diagram.
The user ROM area contains program ROM.
The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode and standard serial I/O and parallel I/O modes.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area and the user ROM area share the same address, but have separate memory areas.

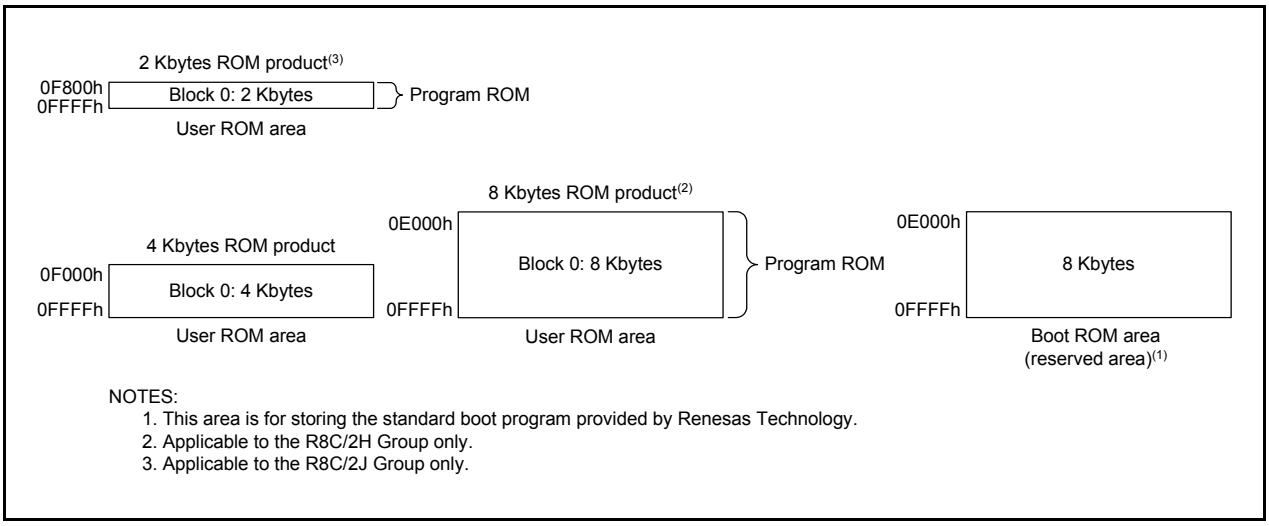


Figure 20.1 Flash Memory Block Diagram

20.3 Functions to Prevent Rewriting of Flash Memory

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten or erasure easily.

20.3.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. Unless 3 bytes (addresses from 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not acknowledged. For details of the ID code check function, refer to **14. ID Code Areas**.

20.3.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased by means of the OFS register when parallel I/O mode is used.
Figure 20.2 shows the OFS Register. Refer to **15. Option Function Select Area** for details of the OFS register.

The ROM code protect function is enabled by writing 0 to the ROMCP1 bit and 1 to the ROMCR bit. It disables reading or changing the contents of the on-chip flash memory.
Once ROM code protect is enabled, the content in the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protect, erase the block including the OFS register with CPU rewrite mode or standard serial I/O mode.

Option Function Select Register(1)

b7	b6	b5	b4	b3	b2	b1	b0
	1		1			1	

Symbol: OFS | Address: 0FFFFh | When Shipping: FFh(3)

Bit Symbol	Bit Name	Function	RW
WDTON	Watchdog timer start select bit	0 : Starts watchdog timer automatically after reset 1 : Watchdog timer is inactive after reset	RW
— (b1)	Reserved bit	Set to 1.	RW
ROMCR	ROM code protect disabled bit	0 : ROM code protect disabled 1 : ROMCP1 enabled	RW
ROMCP1	ROM code protect bit	0 : ROM code protect enabled 1 : ROM code protect disabled	RW
— (b4)	Reserved bit	Set to 1.	RW
LVD0ON	Voltage detection 0 circuit start bit(2)	0 : Voltage monitor 0 reset enabled after hardware reset 1 : Voltage monitor 0 reset disabled after hardware reset	RW
— (b6)	Reserved bit	Set to 1.	RW
CSPROINI	Count source protect mode after reset select bit	0 : Count source protect mode enabled after reset 1 : Count source protect mode disabled after reset	RW

NOTES:
1. The OFS register is on the flash memory. Write to the OFS register with a program. After writing is completed, do not write additions to the OFS register.
2. Setting the LVD0ON bit is only valid after a hardware reset. To use the power-on reset, set the LVD0ON bit to 0 (voltage monitor 0 reset enabled after hardware reset).
3. If the block including the OFS register is erased, FFh is set to the OFS register.

Figure 20.2 OFS Register

20.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.
Table 20.3 lists the EW0 Mode.

Table 20.3 EW0 Mode

Item	EW0 Mode
Operating mode	Single-chip mode
Areas in which a rewrite control program can be executed	RAM (Rewrite control program is executed after being transferred)
Areas which can be rewritten	User ROM
Software command restrictions	None
Modes after program or erase	Read status register mode
Modes after read status register	Read status register mode
CPU status during auto- write and auto-erase	Operating
Flash memory status detection	• Read bits FMR00, FMR06, and FMR07 in the FMR0 register by a program • Execute the read status register command and read bits SR7, SR5, and SR4 in the status register.
CPU clock	5 MHz or below

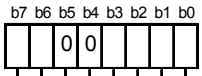
20.4.1 Register Description

The registers used in CPU rewrite mode are described.

20.4.1.1 FMR0 Register (FMR0)

Figure 20.3 shows the FMR0 Register.

Flash Memory Control Register 0



Symbol	Address	After Reset
FMR0	01B7h	00000001b

Bit Symbol	Bit Name	Function	RW
FMR00	RY/BY status flag	0 : Busy (writing or erasing in progress) 1 : Ready	RO
FMR01	CPU rewrite mode select bit(1)	0 : CPU rewrite mode disabled 1 : CPU rewrite mode enabled	RW
FMR02	Block 0 rewrite enable bit(2, 6)	0 : Disables rewrite 1 : Enables rewrite	RW
FMSTP	Flash memory stop bit(3, 5)	0 : Enables flash memory operation 1 : Stops flash memory (enters low-power consumption state and flash memory is reset)	RW
— (b5-b4)	Reserved bits	Set to 0.	RW
FMR06	Program status flag(4)	0 : Completed successfully 1 : Terminated by error	RO
FMR07	Erase status flag(4)	0 : Completed successfully 1 : Terminated by error	RO

NOTES:

1. To set this bit to 1, set it to 1 immediately after setting it first to 0. Do not generate an interrupt between setting the bit to 0 and setting it to 1. Enter read array mode and set this bit to 0.
2. Set this bit to 1 immediately after setting it first to 0 while the FMR01 bit is set to 1. Do not generate an interrupt between setting the bit to 0 and setting it to 1.
3. Set this bit by a program located in a space other than the flash memory.
4. This bit is set to 0 by executing the clear status command.
5. This bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode). When the FMR01 bit is set to 0, writing 1 to the FMSTP bit causes the FMSTP bit to be set to 1. The flash memory does not enter low-power consumption state nor is it reset.
6. When setting the FMR01 bit to 0 (CPU rewrite mode disabled), the FMR02 bit is set to 0 (disables rewrite).

Figure 20.3 FMR0 Register

- FMR00 Bit
  This bit indicates the operating status of the flash memory. The bits value is 0 during programming, erasure, or erase-suspend mode; otherwise, it is 1.

- FMR01 Bit
  The MCU is made ready to accept commands by setting the FMR01 bit to 1 (CPU rewrite mode).

- FMR02 Bit
  Rewriting of block 0 does not accept program or block erase commands if the FMR02 bit is set to 0 (rewrite disabled).
  Rewriting of block 0 is controlled by FMR15 bit if the FMR02 bit is set to 1 (rewrite enabled).

- FMSTP Bit
  This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1. Therefore, the FMSTP bit must be written to by a program transferred to the RAM.
  In the following cases, set the FMSTP bit to 1:

  - When flash memory access resulted in an error while erasing or programming in EW0 mode (FMR00 bit not reset to 1 (ready))
  - To provide lower consumption in low-speed on-chip oscillator mode and low-speed clock mode.

  Note that when going to stop or wait mode while the CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on again after returning from stop or wait mode.

- FMR06 Bit
  This is a read-only bit indicating the status of an auto-program operation. The bit is set to 1 when a program error occurs; otherwise, it is set to 0. For details, refer to the description in **Table 20.4 Errors and FMR0 Register Status**.

- FMR07 Bit
  This is a read-only bit indicating the status of an auto-erase operation. The bit is set to 1 when an erase error occurs; otherwise, it is set to 0. Refer to **Table 20.4 Errors and FMR0 Register Status** for details.

Table 20.4 Errors and FMR0 Register Status

FMR0 Register (Status Register) Status		Error	Error Occurrence Condition
FMR07(SR5)	FMR06(SR4)		
1	1	Command sequence error	• When a command is not written correctly. • When D0h or FFh is not written in the 2nd byte of the block erase command.(1) • When the program command or block erase command is executed while rewriting is disabled by the FMR02 bit in the FMR0 register, or the FMR15 bit in the FMR1 register. • When an address not allocated in flash memory is input during erase command input • When attempting to erase the block for which rewriting is disabled during erase command input. • When an address not allocated in flash memory is input during write command input. • When attempting to write to a block for which rewriting is disabled during write command input.
1	0	Erase error	• When the block erase command is executed but auto-erasure does not complete correctly
0	1	Program error	• When the program command is executed but not auto-programming does not complete.
0	0	Completed successfully	–

NOTE:
1. When FFh is written in the 2nd byte of the block erase command, the MCU enters read array mode, and the command code written in the 1st byte is disabled.

20.4.1.2 FMR1 Register (FMR1)

Figure 20.4 shows the FMR1 Register.

Flash Memory Control Register 1

b7	b6	b5	b4	b3	b2	b1	b0
1	0		0	0	0	0	

Symbol	Address	After Reset
FMR1	01B5h	1000000Xb

Bit Symbol	Bit Name	Function	RW
— (b0)	Reserved bit	When read, the content is undefined.	RO
— (b4-b1)	Reserved bits	Set to 0.	RW
FMR15	Block 0 rewrite disable bit(1,2)	0 : Enables rewrite 1 : Disables rewrite	RW
— (b6)	Reserved bit	Set to 0.	RW
— (b7)	Reserved bit	Set to 1.	RW

NOTES:
1. This bit is set to 0 by setting the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).
2. While the FMR01 bit is set to 1 (CPU rewrite mode enabled), FMR15 bit can be written to.
   To set this bit to 0, set it to 0 immediately after setting it first to 1.
   To set this bit to 1, set it to 1.

Figure 20.4 FMR1 Register

- FMR15 Bit
  When the FMR02 bit is set to 1 (rewrite enabled) and the FMR15 bit is set to 0 (rewrite enabled), block 0 accepts program and block erase commands.

20.4.1.3 FMR4 Register (FMR4)

Figure 20.5 shows the FMR4 Register.

Flash Memory Control Register 4

b7	b6	b5	b4	b3	b2	b1	b0
		X			0	0	0

Symbol	Address	After Reset
FMR4	01B3h	01000000b

Bit Symbol	Bit Name	Function	RW
— (b2-b0)	Reserved bits	Set to 0.	RW
FMR43	Erase command flag	0 : Erase not executed 1 : Erase execution in progress	RO
FMR44	Program command flag	0 : Program not executed 1 : Program execution in progress	RO
— (b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
FMR46	Read status flag	0 : Disables reading 1 : Enables reading	RO
FMR47	Low-current-consumption read mode enable bit (1, 2, 3)	0 : Disable 1 : Enable	RW

NOTES:
1. To set this bit to 1, set it to 1 immediately after setting it first to 0. Do not generate an interrupt between setting the bit to 0 and setting it to 1.
2. In high-speed on-chip oscillator mode, set the FMR47 bit to 0 (disabled).
3. Set the FMR01 bit to 0 (CPU rewrite mode disabled) in low-current-consumption read mode.

Figure 20.5 FMR4 Register

- FMR43 Bit
  When the auto-erase operation starts, the FMR43 bit is set to 1 (erase execution in progress).
  When the auto-erase operation ends, the FMR43 bit is set to 0 (erase not executed).

- FMR44 Bit
  When the auto-program operation starts, the FMR44 bit is set to 1 (program execution in progress).
  When the auto-program operation ends, the FMR44 bit is set to 0 (program not executed).

- FMR46 Bit
  The FMR46 bit is set to 0 (reading disabled) during auto-program or auto-erase execution. Do not access the flash memory while this bit is set to 0.

- FMR47 Bit
  Current consumption when reading the flash memory can be reduced by setting the FMR47 bit to 1 (enabled) in low-speed clock mode and low-speed on-chip oscillator mode.
  Refer to **21.2.10 Low-Current-Consumption Read Mode** for details of the handling procedure.

20.4.2 Status Check Procedure

When an error occurs, bits FMR06 to FMR07 in the FMR0 register are set to 1, indicating the occurrence of an error. Therefore, checking these status bits (full status check) can be used to determine the execution result. Figure 20.6 shows the Full Status Check and Handling Procedure for Individual Errors.

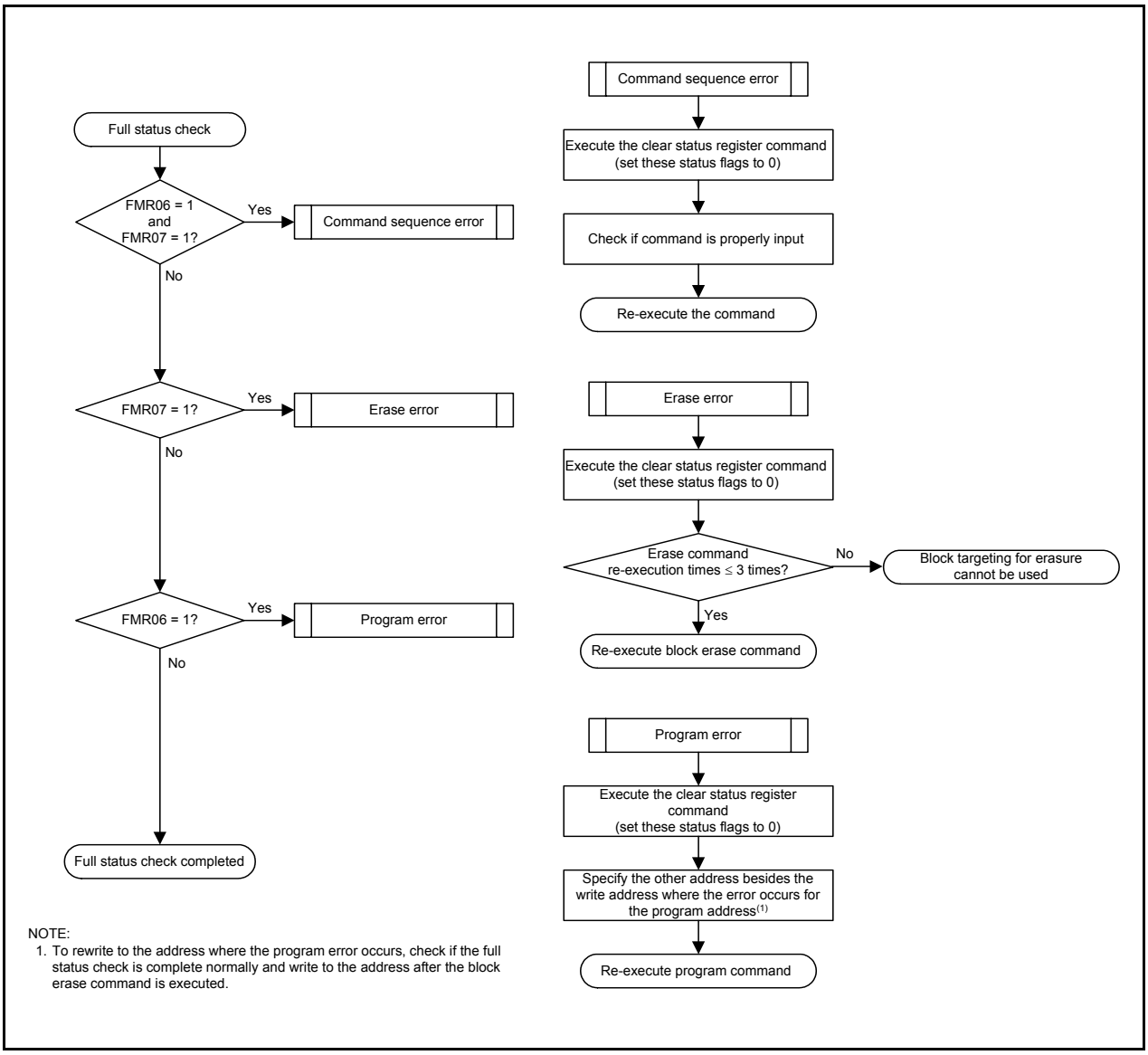


Figure 20.6 Full Status Check and Handling Procedure for Individual Errors

20.4.3 EW0 Mode

The MCU enters CPU rewrite mode and software commands can be acknowledged by setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled). In this case, since the FMR11 bit in the FMR1 register is set to 0, EW0 mode is selected.
Use software commands to control program and erase operations. The FMR0 register or the status register can be used to determine when program and erase operations complete.
Figure 20.7 shows How to Set and Exit EW0 Mode.

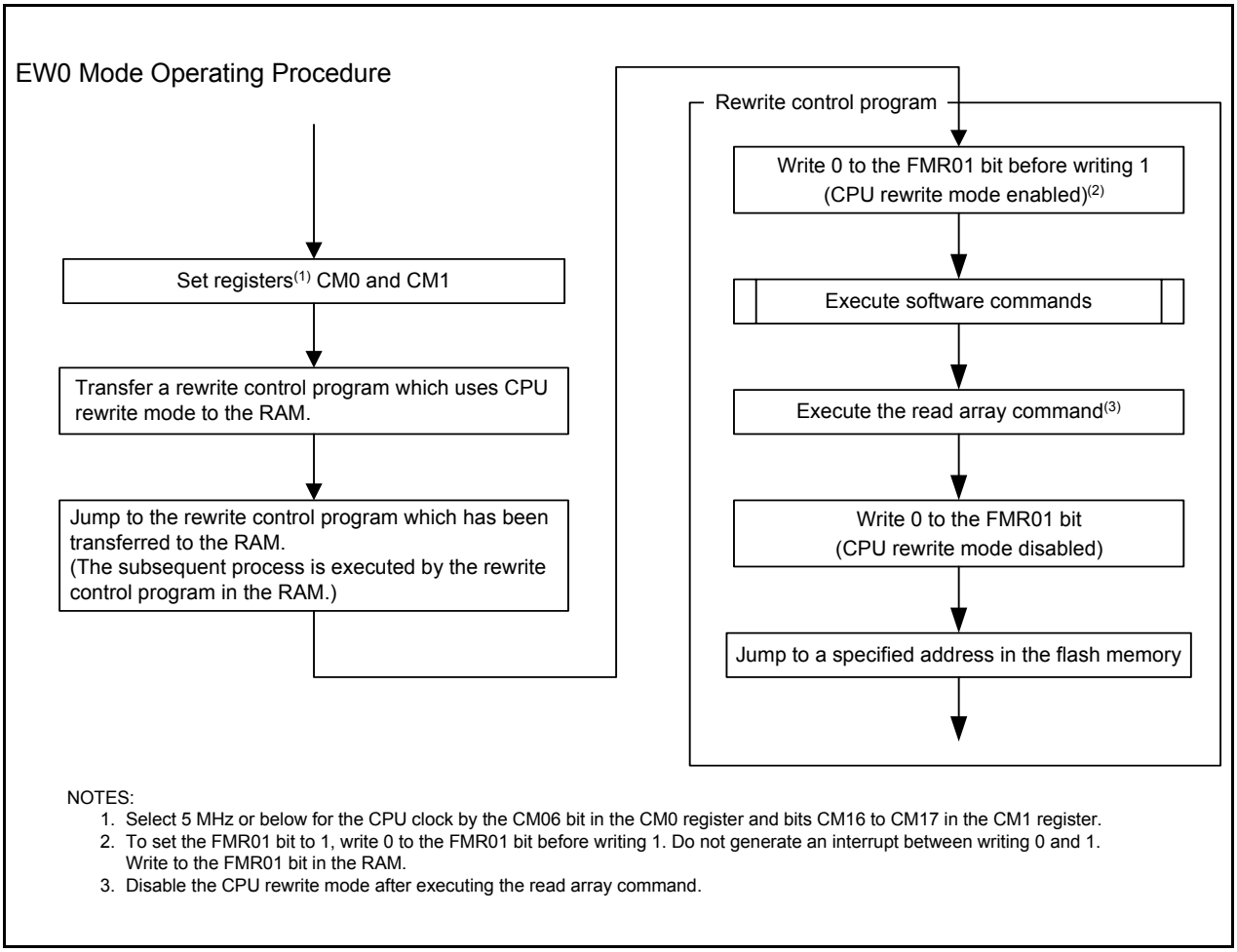


Figure 20.7 How to Set and Exit EW0 Mode

20.4.3.1 Software Commands

There are five types of software commands:

- Read array
- Read status register
- Clear status register
- Program
- Block erase

Figure 20.8 shows Software Command Status Transition Diagram in EW0 Mode.

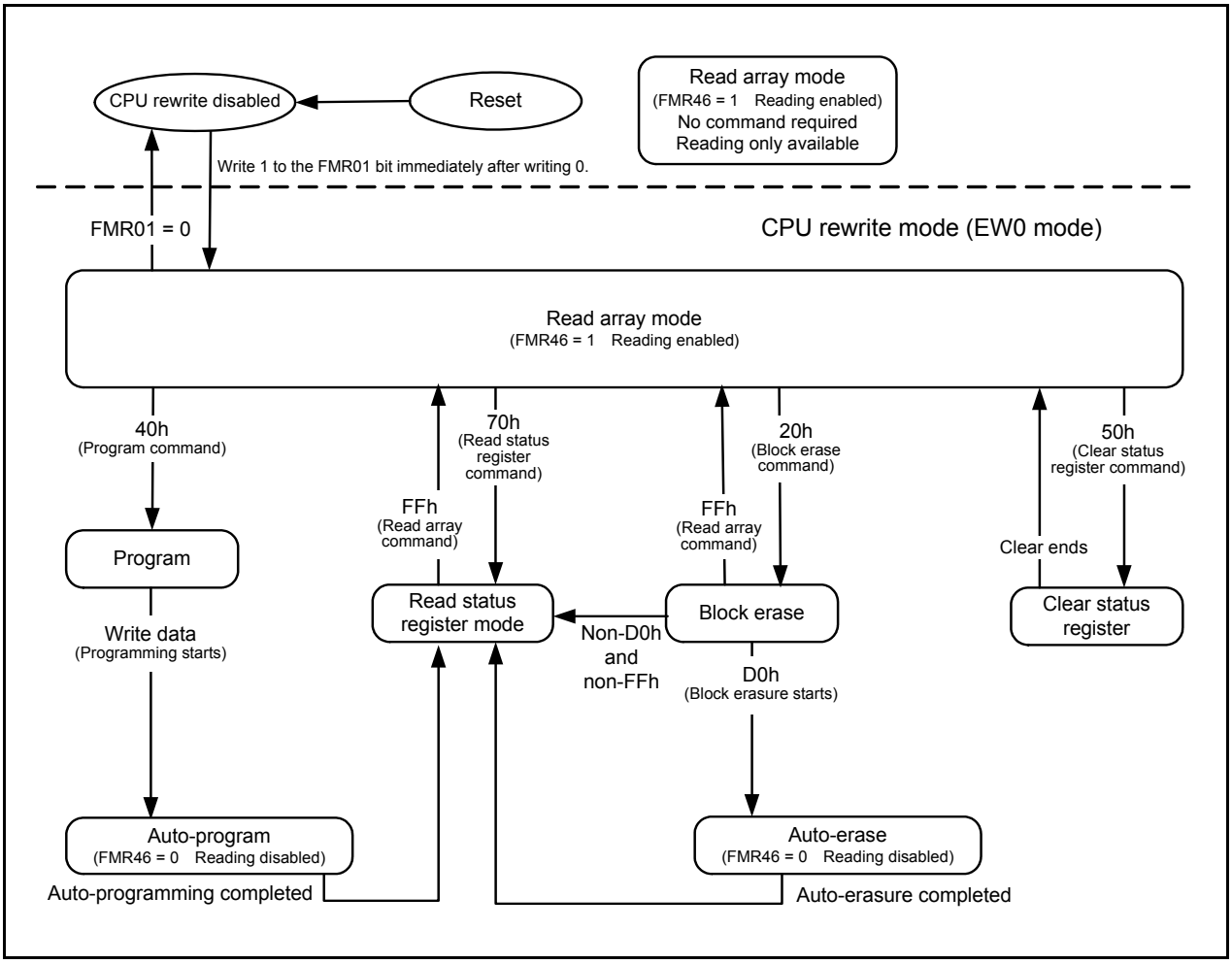


Figure 20.8 Software Command Status Transition Diagram in EW0 Mode

- Read Array Command
  The read array command reads the flash memory.
  When FFh is written to an address in the user ROM area, the MCU enters read array mode. In this mode, the contents of the specified address can be read.
  Read array mode continues until other commands are written. The MCU enters this mode after a reset is deasserted.

- Read Status Register Command
  The read status register command is used to read the status register. Figure 20.9 shows Status Register.
  The status register indicates the operating status of the flash memory and whether an erase or program operation has completed normally or in error (refer to **Table 20.4 Errors and FMR0 Register Status**).
  When 70h is written to an address in the user ROM area, the MCU enters read status register mode. When the address in the user ROM area is read subsequently, the status register can be read.
  The MCU remains in read status register mode until the next read array command is written.
  The status of the status register can be determined by reading bits FMR00, FMR06, and FMR07 in the FMR0 register.

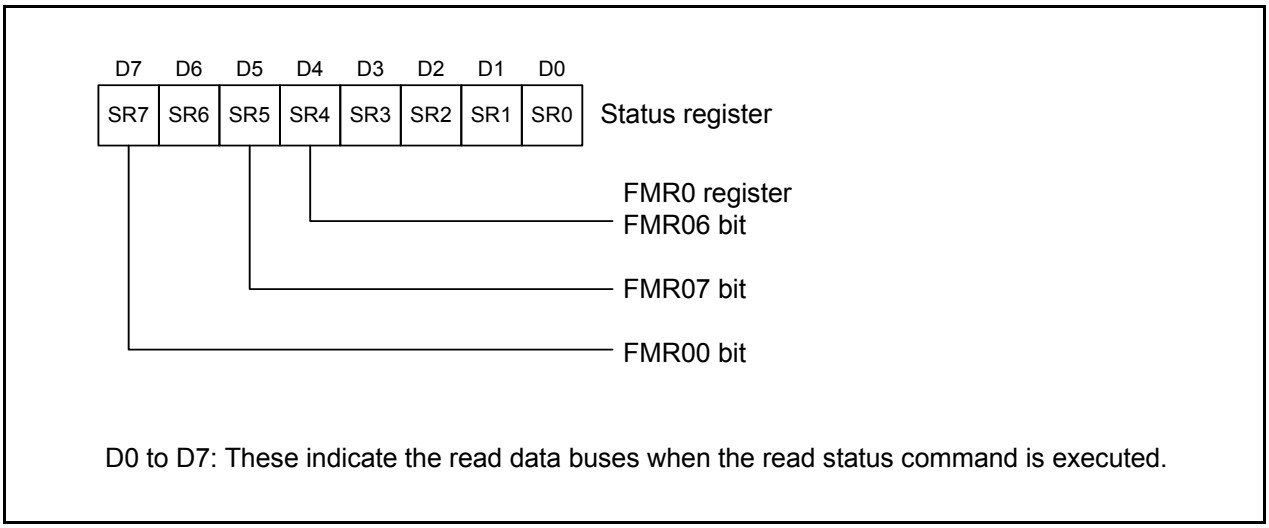


Figure 20.9 Status Register

- Clear Status Register Command
  The clear status register command sets the status register to 0.
  When 50h is written to an address in the user ROM area, bits FMR07 and FMR06 in the FMR0 register and bits SR5 and SR4 in the status register are set to 00b.

- Program Command
  The program command writes data to the flash memory in 1-byte units.
  When 40h is written and then data is written to the write address, an auto-program operation (data program and verify) starts.
  The FMR00 bit in the FMR0 register can be used to determine whether auto-programming has completed. The FMR00 bit is set to 0 during auto-programming and set to 1 when auto-programming completes.
  The FMR06 bit in the FMR0 register can be used to determine the result of auto-programming after it has been finished (refer to **20.4.2 Status Check Procedure**).

  Do not write additions to the already programmed addresses.
  Also, when the FMR02 bit in the FMR0 register is set to 0 (rewrite disabled), or the FMR02 bit is set to 1 (rewrite enabled) and the FMR15 bit in the FMR1 register is set to 1 (rewrite disabled), program commands targeting block 0 are not acknowledged.

  Figure 20.10 shows the Program Command in EW0 Mode.

  In EW0 mode, the MCU enters read status register mode at the same time auto-programming starts and the status register can be read. In this case, the MCU remains in read status register mode until the next read array command is written.

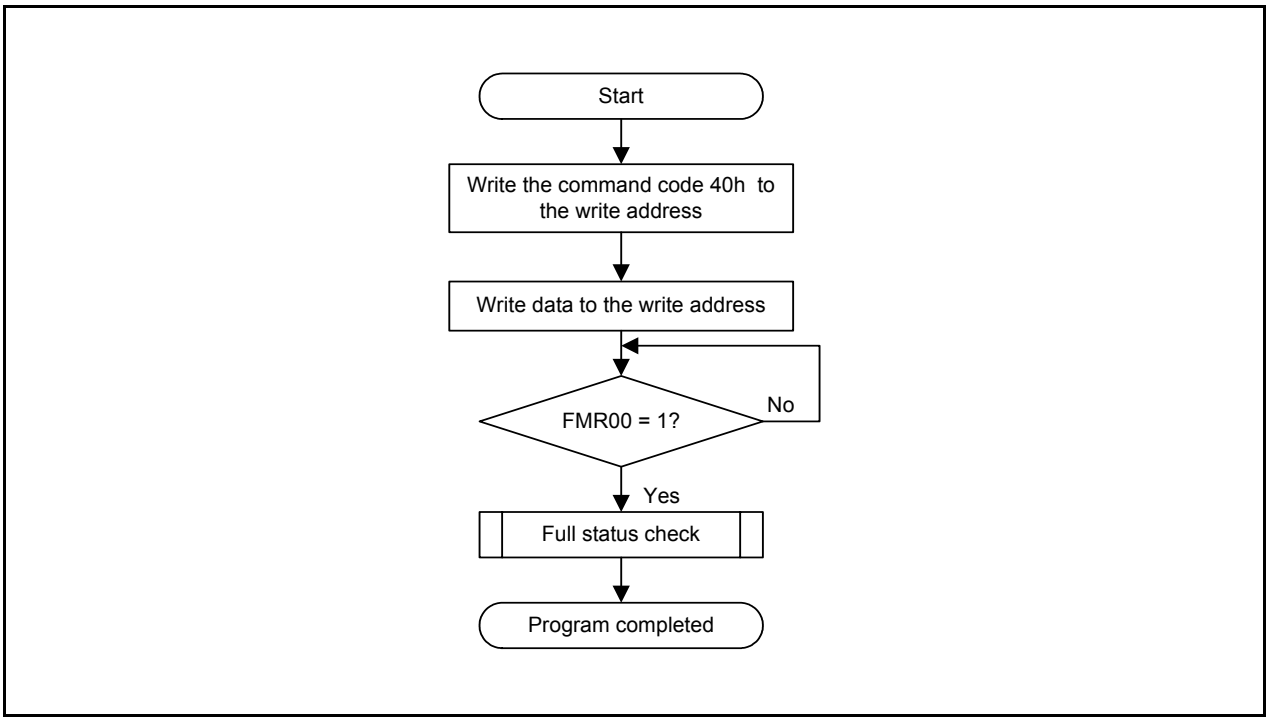


Figure 20.10 Program Command in EW0 Mode

- Block Erase
  When 20h is first written and then D0h is written to a given block address, an auto-erase operation (erase and verify) of the specified block starts.
  The FMR00 bit in the FMR0 register can be used to determine whether auto-erasure has completed.
  The FMR00 bit is set to 0 during auto-erasure and set to 1 when auto-erasure completes.
  The FMR07 bit in the FMR0 register can be used to determine the result of auto-erasure after auto-erasure has completed (refer to **20.4.2 Status Check Procedure**).

  Also, when the FMR02 bit in the FMR0 register is set to 0 (rewrite disabled), or the FMR02 bit is set to 1 (rewrite enabled) and the FMR15 bit in the FMR1 register is set to 1 (rewrite disabled), block erase commands targeting block 0 are not acknowledged.

  In EW0 mode, the MCU enters read status register mode at the same time auto-erasure starts and the status register can be read. In this case, the MCU remains in read status register mode until the next read array command is written.

  Figure 20.11 shows the Block Erase Command in EW0 Mode.

  If the programming and erasure endurance is n (n = 100, 1000, or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1-Kbyte block, and then the block is erased, the erase count stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing programming operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.

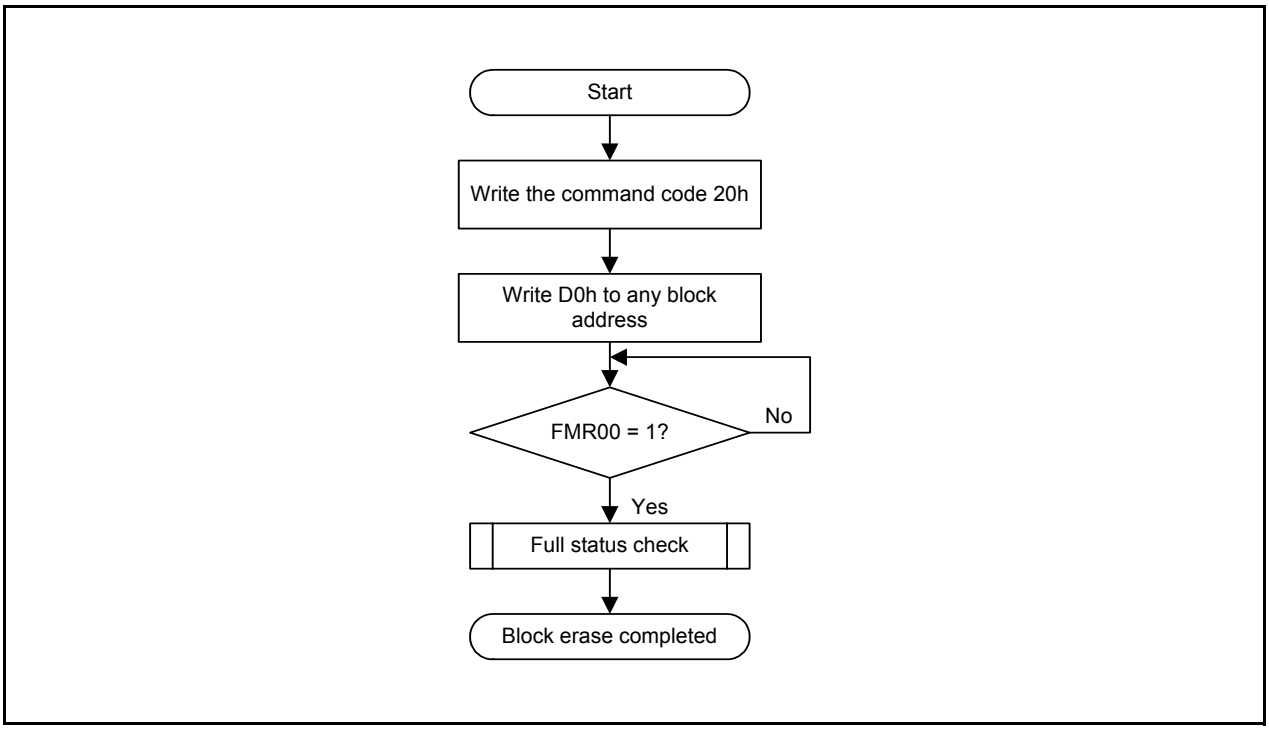


Figure 20.11 Block Erase Command in EW0 Mode

20.4.3.2 EW0 Mode Interrupts

In EW0 mode, maskable interrupts can be used by allocating a vector in RAM. Table 20.5 lists the EW0 Mode Interrupts. Refer to **20.7.1.3 Non-Maskable Interrupts** for details of the non-maskable interrupt.

Table 20.5 EW0 Mode Interrupts

Status	When Maskable Interrupt Request is Acknowledged
During auto-erasure	Interrupt handling is executed.
Auto-programming	

20.5 Standard Serial I/O Mode

In standard serial I/O mode, the user ROM area can be rewritten while the MCU is mounted on-board by using a serial programmer which is suitable for the MCU.
There are three types of standard serial I/O modes:

- Standard serial I/O mode 1 .....Clock synchronous serial I/O used to connect with a serial programmer
- Standard serial I/O mode 2 .....Clock asynchronous serial I/O used to connect with a serial programmer
- Standard serial I/O mode 3 .....Special clock asynchronous serial I/O used to connect with a serial programmer

This MCU uses Standard serial I/O mode 3.

Refer to **Appendix 2. Connection Examples with On-Chip Debugging Emulator**. Contact the manufacturer of your serial programmer for details. Refer to the user's manual of your serial programmer for instructions on how to use it.

Table 20.6 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3), and Figure 20.12 shows an Example of Pin Processing in Standard Serial I/O Mode 3.
After processing the pins shown in Table 20.6 and rewriting the flash memory using the programmer, apply "H" to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

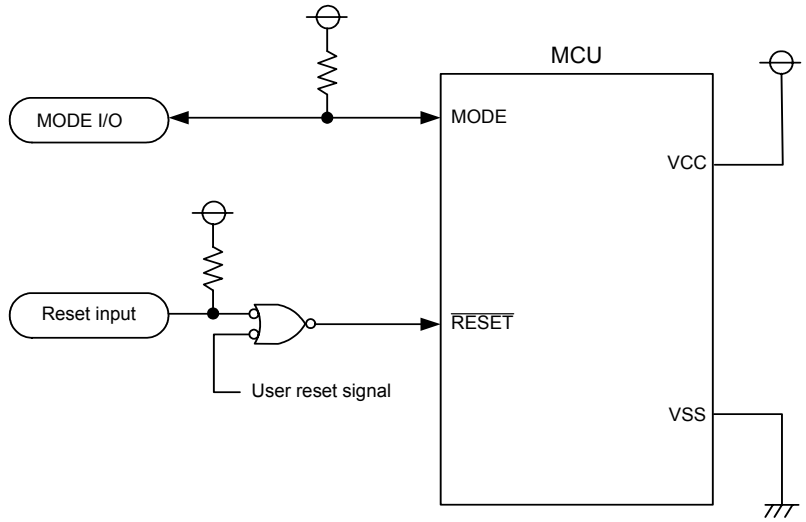
20.5.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.
Refer to **14. ID Code Areas** for details of the ID code check.

Table 20.6 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC,VSS	Power input		Apply the voltage guaranteed for programming and erasure to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
P4_3/XCIN(1)	P4_3 input/clock input	I	Connect crystal oscillator between pins XCIN and XCOUT when connecting external oscillator. To use P4_3 as an input port, input a “H” or “L” level signal or leave the pin open. To use P4_4 as an output port, leave the pin open.
P4_4/XCOUT(1)	P4_4 output/clock output	O	
P1_0 to P1_7	Input port P1	I	Input a “H” or “L” level signal or leave the pin open.
P3_3, P3_7	Input port P3	I	
P4_5	Input port P4	I	
P6_3 to P6_5(1)	Input port P6	I	
MODE	MODE	I/O	Serial data I/O pin. Connect to the flash programmer.

NOTE:
1. Ports P4_3, P4_4, P6_3, and P6_4 are not available in the R8C/2J Group.



NOTES:
1. Controlled pins and external circuits vary depending on the programmer. Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillating circuit.

Figure 20.12 Example of Pin Processing in Standard Serial I/O Mode 3

20.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory. Use a parallel programmer which supports this MCU. Contact the manufacturer of the parallel programmer for more information, and refer to the user's manual of the parallel programmer for details on how to use it.
ROM areas shown in Figure 20.1 can be rewritten in parallel I/O mode.

20.6.1 ROM Code Protect Function

The ROM code protect function disables the reading and rewriting of the flash memory. (Refer to **20.3.2 ROM Code Protect Function**.)

20.7 Notes on Flash Memory

20.7.1 CPU Rewrite Mode

20.7.1.1 Operating Speed

Before entering CPU rewrite mode (EW0 mode), select 5 MHz or below for the CPU clock using the CM06 bit in the CM0 register and bits CM16 to CM17 in the CM1 register.

20.7.1.2 Prohibited Instructions

The following instructions cannot be used in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

20.7.1.3 Non-Maskable Interrupts

- EW0 Mode
  Once a watchdog timer, voltage monitor1, voltage monitor 2, comparator 1, or comparator 2 interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts after a fixed period and the flash memory restarts.
  As the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be readable. Execute auto-erasure again and ensure it completes normally.
  The watchdog timer does not stop during command operation, so that interrupt requests may be generated. Initialize the watchdog timer regularly.
  Do not use the address match interrupt while a command is being executed because the vector of the address match interrupt is allocated in ROM.
  Do not use a non-maskable interrupt while block 0 is being automatically erased because the fixed vector is allocated in block 0.

20.7.1.4 How to Access

Write 0 before writing 1 when setting Bits FMR01, FMR02 in the FMR0 register, or FMR11 bit in the FMR1 register to 1. Do not generate an interrupt between writing 0 and 1.

20.7.1.5 Rewriting User ROM Area

In EW0 Mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

20.7.1.6 Program

Do not write additions to the already programmed address.

20.7.1.7 Program and Erase Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

21. Reducing Power Consumption

21.1 Overview

This chapter describes key points and processing methods for reducing power consumption.

21.2 Key Points and Processing Methods for Reducing Power Consumption

Key points for reducing power consumption are shown below. They should be referred to when designing a system or creating a program.

21.2.1 Voltage Detection Circuit

When voltage monitor 1 and comparator 1 are not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). When voltage monitor 2 and comparator 2 are not used, set the VCA27 bit in the VCA2 register to 0 (voltage detection 2 circuit disabled).
If the power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

21.2.2 Ports

Even after the MCU enters wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state, and shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before the MCU enters wait mode or stop mode.

21.2.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases. Unnecessary clocks should be stopped accordingly.

Stopping low-speed on-chip oscillator oscillation: CM14 bit in CM1 register (for R8C/2H Group only)
Stopping high-speed on-chip oscillator oscillation: HRA00 bit in HRA0 register

21.2.4 Selecting Oscillation Drive Capacity (for R8C/2H Group only)

Set the drive capacity of the XCIN clock oscillation circuit to “LOW”. Confirm that the circuit oscillates stably while it is in the “LOW” state.

Selecting XCIN-XCOUT drive capacity: CM03 bit in CM0 register

21.2.5 Wait Mode, Stop Mode

Power consumption can be reduced in wait mode and stop mode. Refer to **11.4 Power Control** for details.

21.2.6 Stopping Peripheral Function Clocks

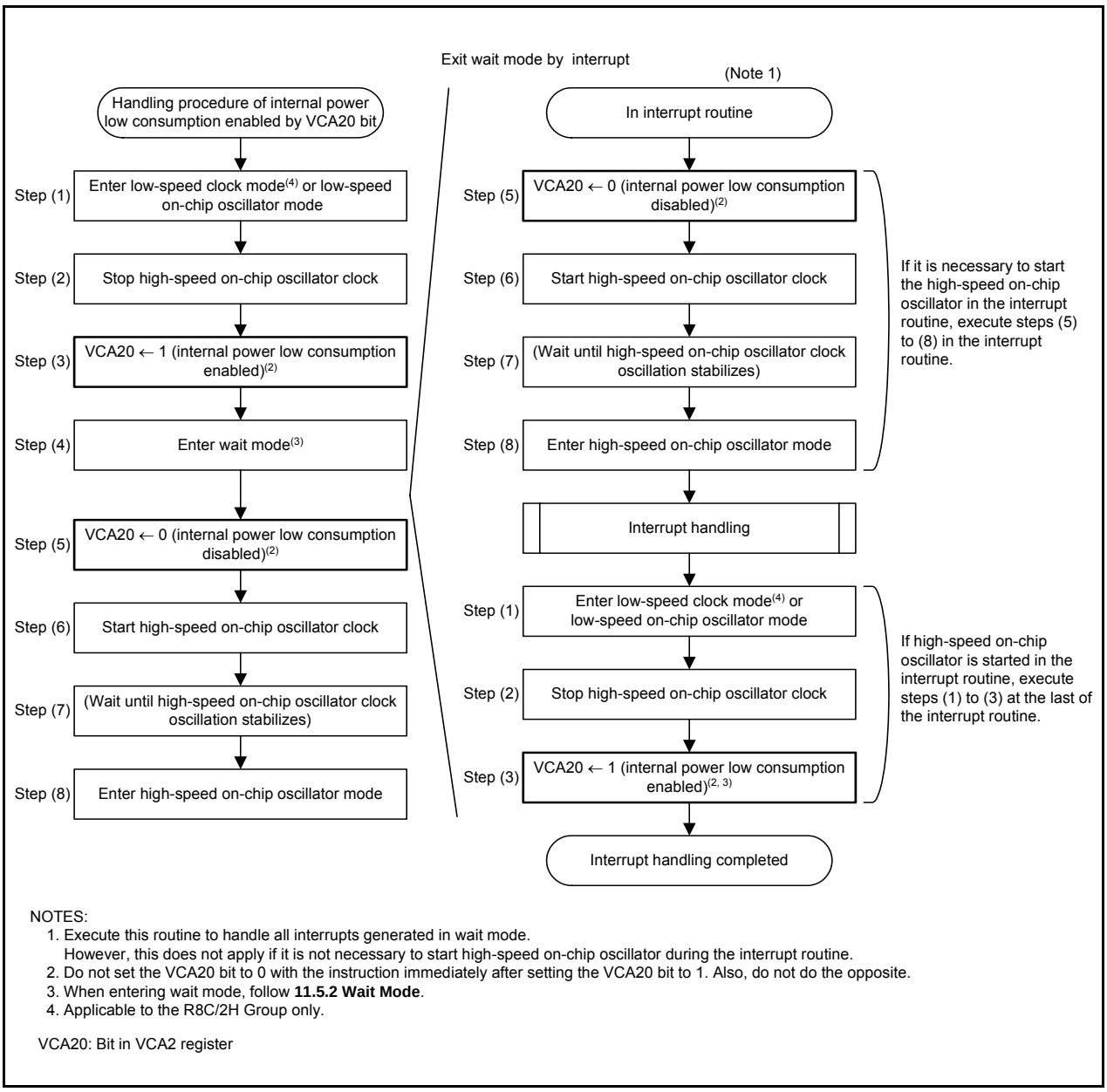
If the peripheral function f1, f2, f4, f8, and f32 clocks are not necessary in wait mode, set the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode). This will stop the f1, f2, f4, f8, and f32 clocks in wait mode.

21.2.7 Timers

If timer RA is not used, set the TCKCUT bit in the TRAMR register to 1 (count source cutoff).
If timer RB is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff).

21.2.8 Reducing Internal Power Consumption

When the MCU enters wait mode using low-speed clock mode or low-speed on-chip oscillator mode, internal power consumption can be reduced by using the VCA20 bit in the VCA2 register. Figure 21.1 shows the Handling Procedure of Internal Power Low Consumption Using VCA20 Bit. To enable internal power low consumption by the VCA20 bit, follow Figure 21.1 Handling Procedure of Internal Power Low Consumption Using VCA20 Bit.



NOTES:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When entering wait mode, follow **11.5.2 Wait Mode**.
4. Applicable to the R8C/2H Group only.

VCA20: Bit in VCA2 register

Figure 21.1 Handling Procedure of Internal Power Low Consumption Using VCA20 Bit

21.2.9 Stopping Flash Memory

In low-speed on-chip oscillator mode and low-speed clock mode, power consumption can be further reduced by stopping the flash memory using the FMSTP bit in the FMR0 register.
Access to the flash memory is disabled by setting the FMSTP bit to 1 (flash memory stops). The FMSTP bit must be written to by a program transferred to RAM.
When the MUC enters stop mode or wait mode while CPU rewrite mode is disabled, the power for the flash memory is automatically turned off. It is turned back on again after the MCU exit stop mode or wait mode. This eliminates the need to set the FMR0 register.
Figure 21.2 shows the Handling Procedure Example of Low Power Consumption Using FMSTP Bit.

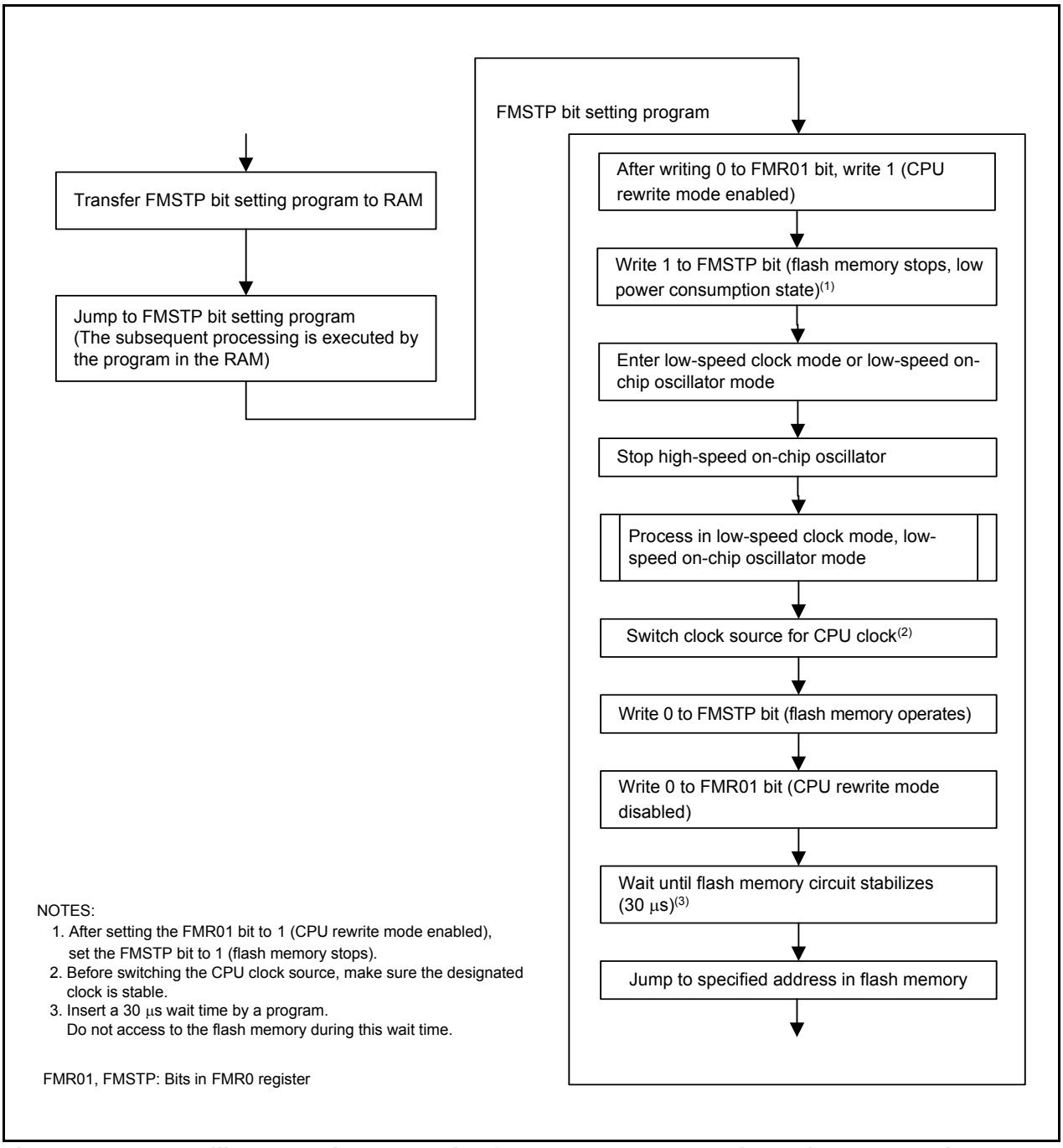
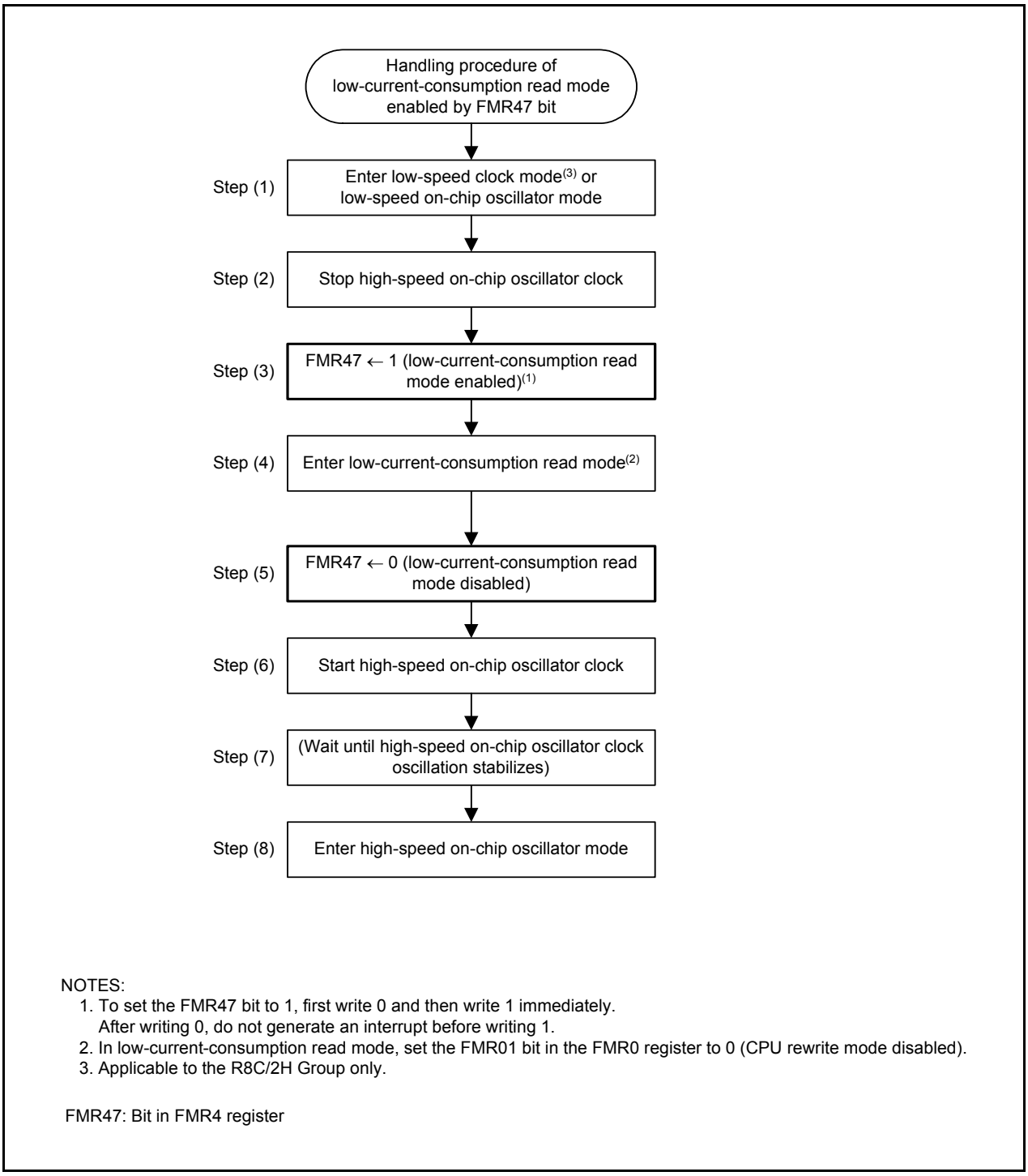


Figure 21.2 Handling Procedure Example of Low Power Consumption Using FMSTP Bit

21.2.10 Low-Current-Consumption Read Mode

In low-speed clock mode (for the R8C/2H Group only) and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR47 bit in the FMR4 register to 1 (enabled).
Figure 21.3 shows the Handling Procedure Example of Low-Current-Consumption Read Mode.



NOTES:
1. To set the FMR47 bit to 1, first write 0 and then write 1 immediately.
   After writing 0, do not generate an interrupt before writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).
3. Applicable to the R8C/2H Group only.

FMR47: Bit in FMR4 register

Figure 21.3 Handling Procedure Example of Low-Current-Consumption Read Mode

22. Electrical Characteristics

22.1 R8C/2H Group

Table 22.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	T_{opr} = 25°C	500	mW
T_{opr}	Operating ambient temperature		–20 to 85 (N version) / –40 to 85 (D version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Table 22.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.2	–	5.5	V
V_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	–160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$		–	–	–80	mA
$I_{OH(peak)}$	Peak output “H” current	All pins		–	–	–10	mA
$I_{OH(avg)}$	Average output “H” current	All pins		–	–	–5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL(peak)}$		–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” currents	Sum of all pins $I_{OL(avg)}$		–	–	80	mA
$I_{OL(peak)}$	Peak output “L” currents	All pins		–	–	10	mA
$I_{OL(avg)}$	Average output “L” current	All pins		–	–	5	mA
$f_{(XCIN)}$	XCIN clock input oscillation frequency		2.2 V ≤ V_{CC} ≤ 5.5 V	0	–	70	kHz
–	System clock	OCD2 = 0 XCIN clock selected	2.2 V ≤ V_{CC} ≤ 5.5 V	0	–	70	kHz
		OCD2 = 1 On-chip oscillator clock selected	HRA01 = 0 Low-speed on-chip oscillator selected	–	125	–	kHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	8	MHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.2 V ≤ V_{CC} ≤ 5.5 V	–	–	4	MHz

NOTES:
1. V_{CC} = 2.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

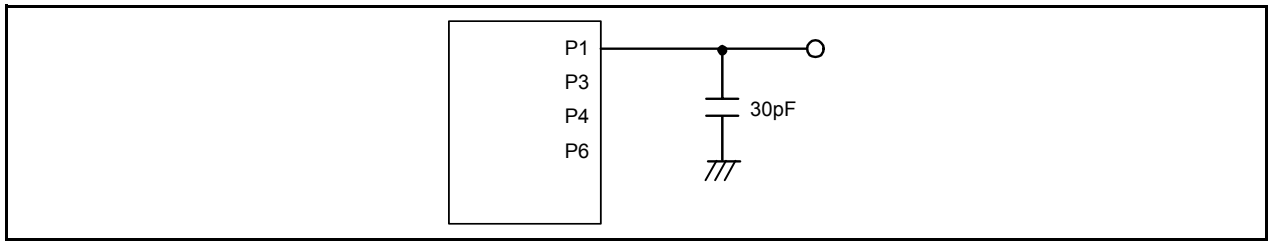


Figure 22.1 Ports P1, P3, P4, and P6 Timing Measurement Circuit

Table 22.3 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		100(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 22.4 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level		2.2	2.3	2.4	V
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	0.9	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	300	µs
Vccmin	MCU operating voltage minimum value		2.2	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 22.5 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(4)		2.70	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 22.6 Voltage Detection 2 Circuit Electrical Characteristics

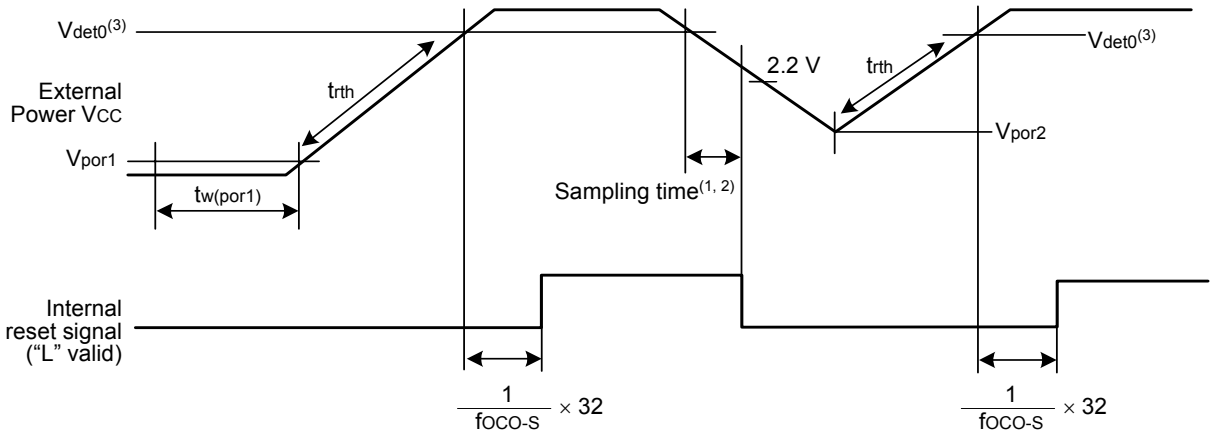
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 22.7 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V_{det0}	V
t_{rth}	External power V_{CC} rise gradient(2)		20	–	–	mV/msec

NOTES:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if –20°C ≤ T_{opr} ≤ 85°C, maintain $t_{w(por1)}$ for 3,000 s or more if –40°C ≤ T_{opr} < –20°C.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.

Figure 22.2 Reset Circuit Electrical Characteristics

Table 22.8 Comparator Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	Internal reference voltage	V_{CC} = 2.2 V to 5.5 V, T_{opr} = 25°C	1.15	1.25	1.35	V
		V_{CC} = 2.2 V to 5.5 V, T_{opr} = –40 to 85°C	–	1.25	–	V
Vcref	External input reference voltage	V_{CC} = 2.2 V to 4.0 V	0.5	–	V_{CC} – 1.1	V
		V_{CC} = 4.0 V to 5.5 V	0.5	–	V_{CC} – 1.5	V
Vcin	External comparison voltage input range		–0.3	–	V_{CC} + 0.3	V
Vofs	Input offset voltage		–	20	120	mV
Tcrsp	Response time		–	4	–	µs

NOTE:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.9 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-F	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 V to 5.25 V, T_{opr} = 0 to 60°C(2)	7.76	8	8.24	MHz
		V_{CC} = 2.7 V to 5.5 V, T_{opr} = –20 to 85°C(2)	7.68	8	8.32	MHz
		V_{CC} = 2.7 V to 5.5 V, T_{opr} = –40 to 85°C(2)	7.44	8	8.32	MHz
		V_{CC} = 2.2 V to 5.5 V, T_{opr} = –20 to 85°C(3)	7.04	8	8.96	MHz
		V_{CC} = 2.2 V to 5.5 V, T_{opr} = –40 to 85°C(3)	6.8	8	9.2	MHz

NOTES:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the HRA1 register is set to the value before shipment and the HRA2 register is set to 00h.
3. These standard values show when the correction value in the FRA6 register is written into the HRA1 register.

Table 22.10 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 22.12 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = –200 μA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		I_{OL} = 5 mA	–	–	2.0	V
			I_{OL} = 200 μA	–	–	0.45	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, RXD0, RXD2, CLK0, CLK2		0.1	0.5	–	V
		$\overline{RESET}$		0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V	–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V	–	–	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5 V	30	50	167	kΩ
R_{fXCIN}	Feedback resistance	XCIN		–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	2.0	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.13 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are VSS	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	8	mA
			High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	–	130	300	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	4	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	2.2	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	8	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	6	–	µA
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.8	3	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.2	–	µA
			XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	8	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	µA

Timing Requirements
(Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 5 V]

Table 22.14 XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

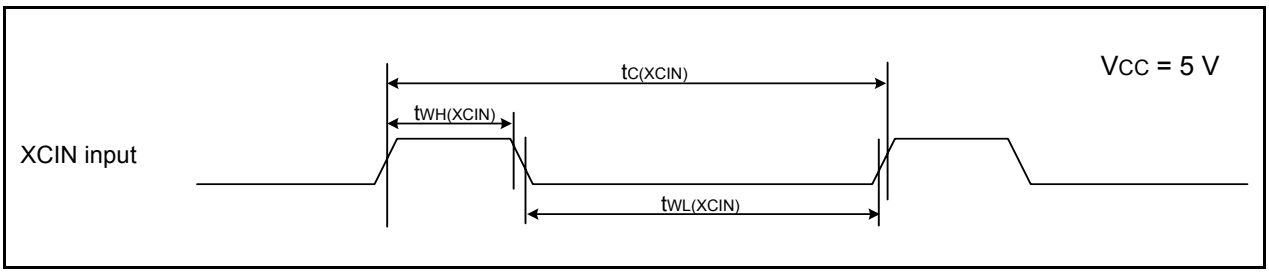


Figure 22.3 XCIN Input Timing Diagram when V_{CC} = 5 V

Table 22.15 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

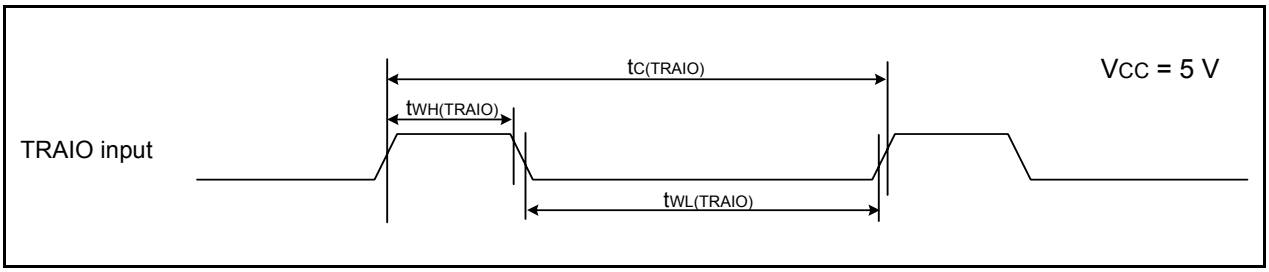


Figure 22.4 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 22.16 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width	100	–	ns
$t_{W(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 2

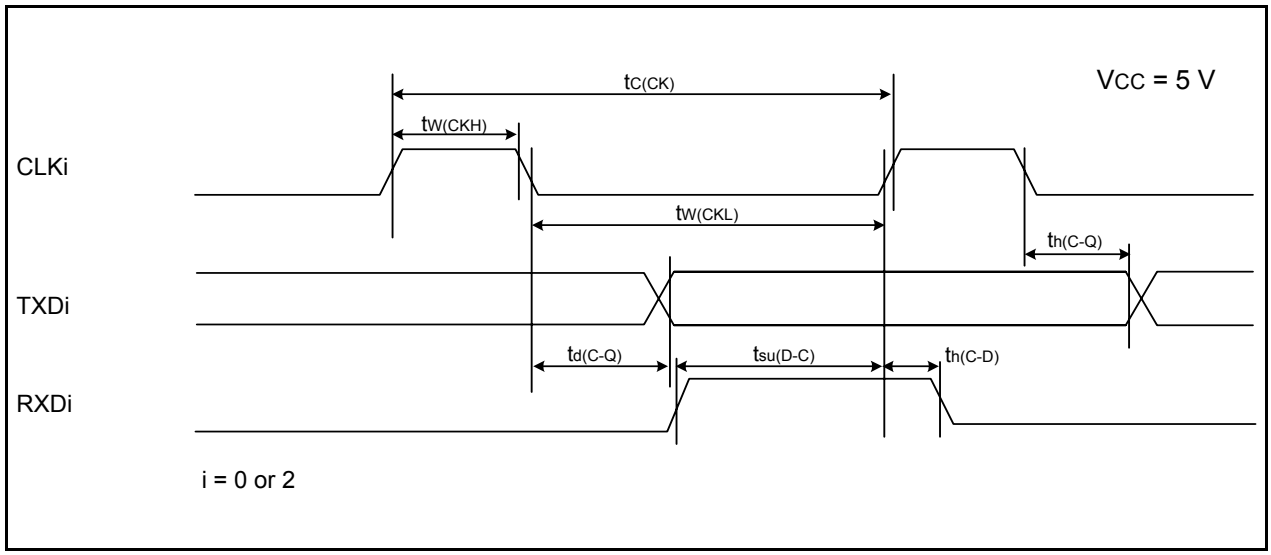


Figure 22.5 Serial Interface Timing Diagram when VCC = 5 V

Table 22.17 External Interrupt $\overline{INTi}$ (i = 0 or 1) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

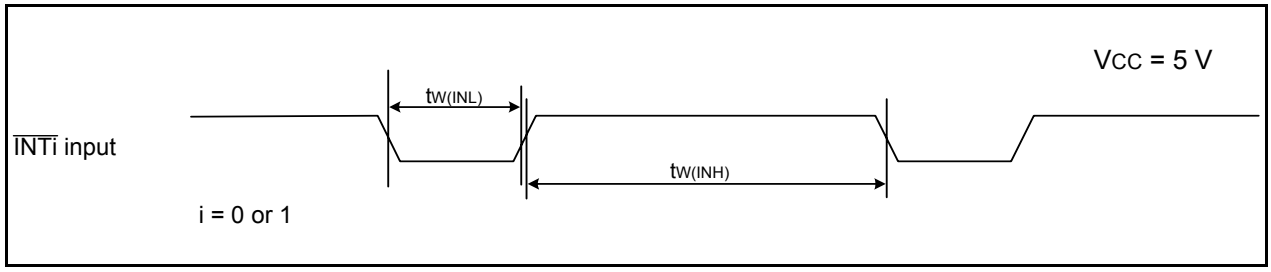


Figure 22.6 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V

Table 22.18 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, RXD0, RXD2, CLK0, CLK2		0.1	0.3	–	V
		$\overline{RESET}$		0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3 V	–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3 V	–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3 V	66	160	500	kΩ
R_{fXCIN}	Feedback resistance	XCIN		–	18	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	–	–	V

NOTE:
1. V_{CC} =2.7 to 3.3 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.19 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	–	mA
			High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	–	130	300	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	–	30	–	µA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	70	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	55	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	3.8	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	2	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	8	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	6	–	µA
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.7	3	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.1	–	µA
			XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	7	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	µA

Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 3 V]

Table 22.20 XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

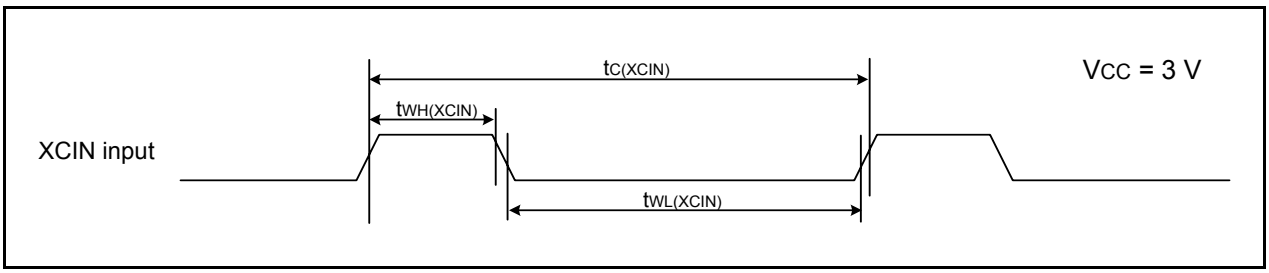


Figure 22.7 XCIN Input Timing Diagram when V_{CC} = 3 V

Table 22.21 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

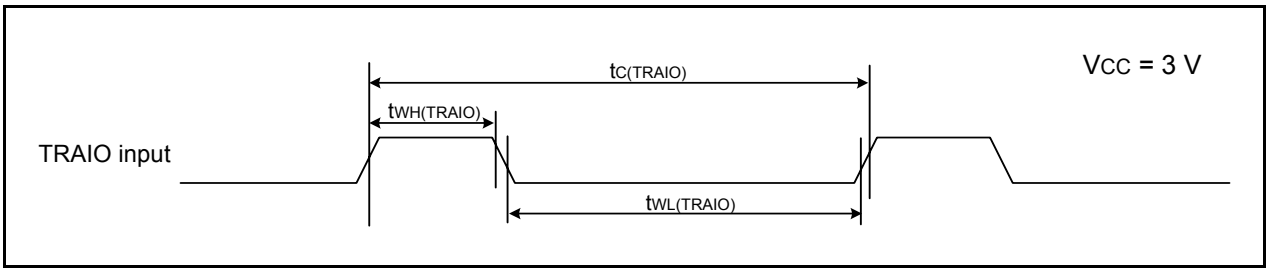


Figure 22.8 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 22.22 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 2

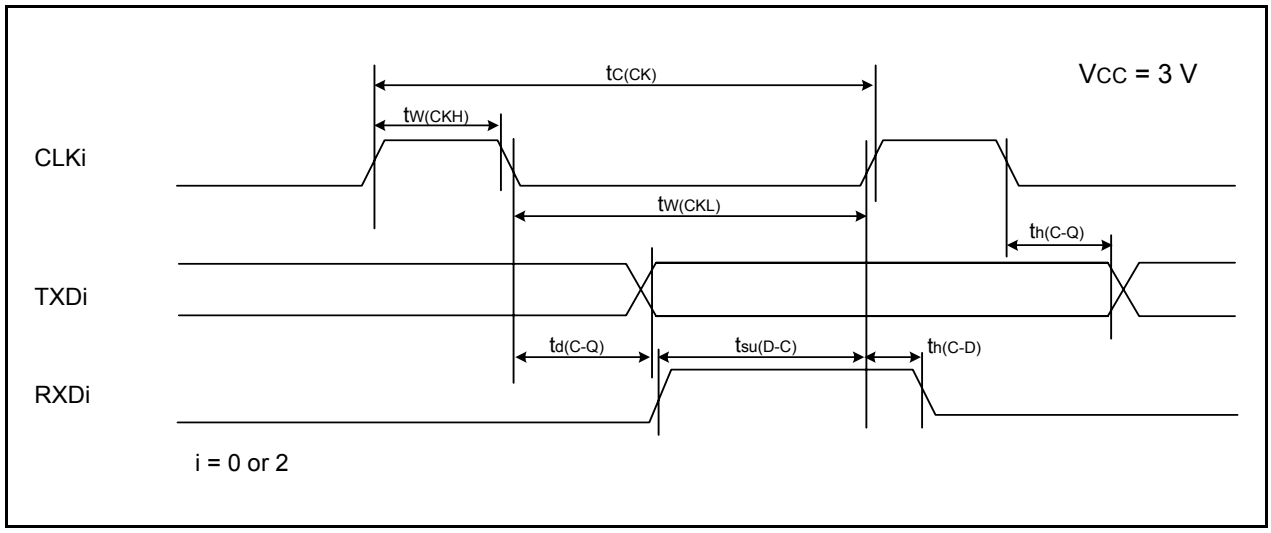


Figure 22.9 Serial Interface Timing Diagram when Vcc = 3 V

Table 22.23 External Interrupt $\overline{INTi}$ (i = 0 or 1) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

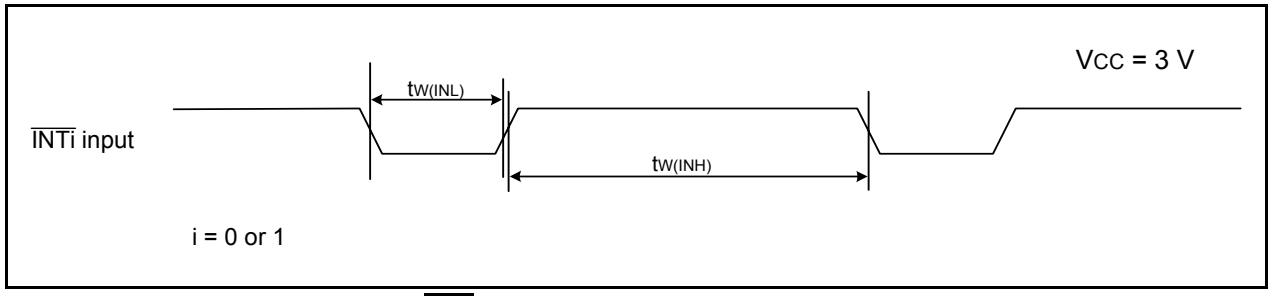


Figure 22.10 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V

Table 22.24 Electrical Characteristics (5) [V_{CC} = 2.2 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, RXD0, RXD2, CLK0, CLK2		0.05	0.3	–	V
		$\overline{RESET}$		0.05	0.15	–	V
I_{IH}	Input “H” current		VI = 2.2 V	–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V	–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V	100	200	600	kΩ
R_{fXCIN}	Feedback resistance	XCIN		–	35	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	–	–	V

NOTE:
1. V_{CC} = 2.2 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.25 Electrical Characteristics (6) [Vcc = 2.2 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are VSS	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	–	100	230	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	–	25	–	µA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	3	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.8	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	7	–	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	–	6	–	µA
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.7	3	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.1	–	µA
			XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	7	µA
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	µA

Timing requirements
(Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 2.2 V]

Table 22.26 XCIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

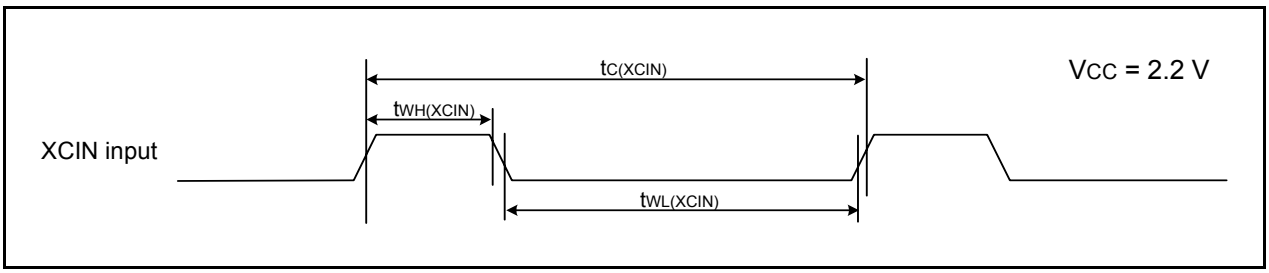


Figure 22.11 XCIN Input Timing Diagram when V_{CC} = 2.2 V

Table 22.27 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

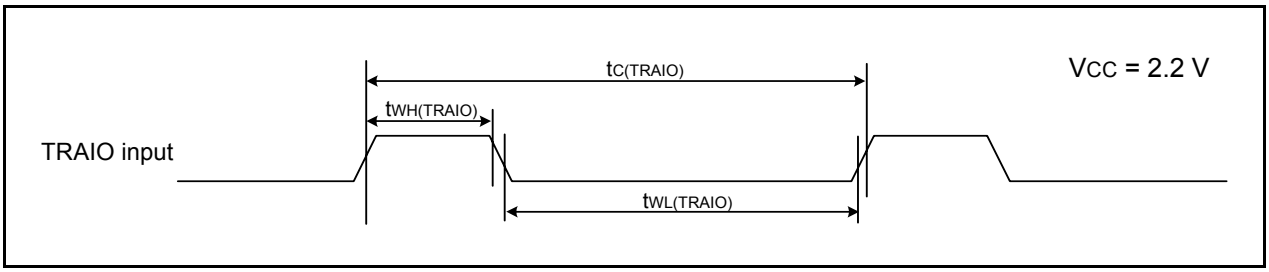


Figure 22.12 TRAIO Input Timing Diagram when V_{CC} = 2.2 V

Table 22.28 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{W(CKH)}$	CLKi input “H” width	400	–	ns
$t_{W(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 2

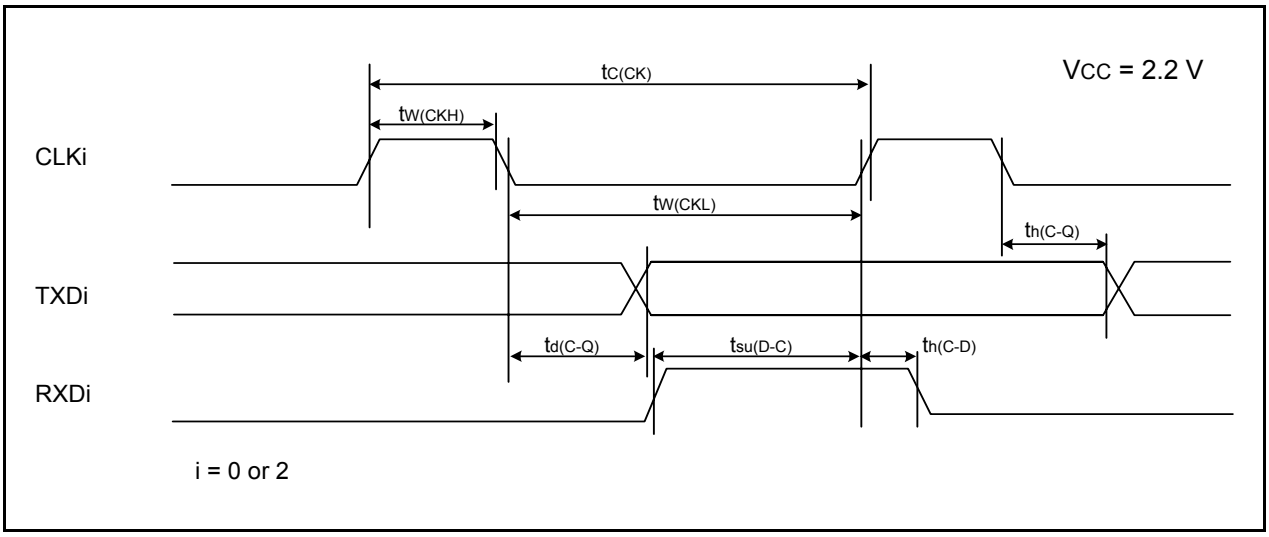


Figure 22.13 Serial Interface Timing Diagram when VCC = 2.2 V

Table 22.29 External Interrupt $\overline{INTi}$ (i = 0 or 1) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	1000(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	1000(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

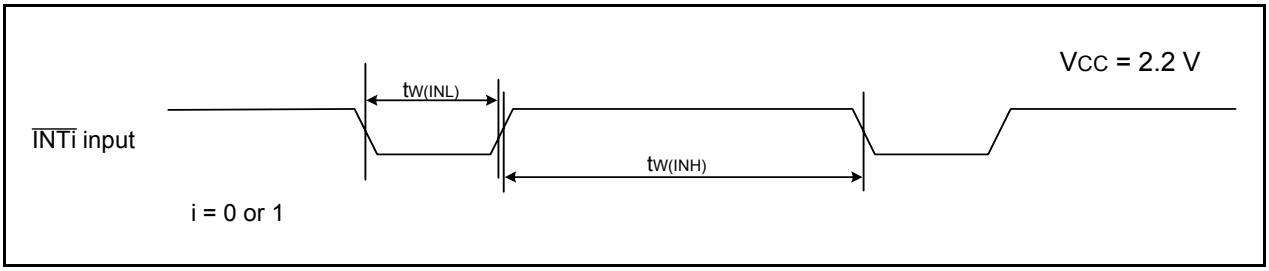


Figure 22.14 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 2.2 V

22.2 R8C/2J Group

Table 22.30 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	T_{opr} = 25°C	500	mW
T_{opr}	Operating ambient temperature		–20 to 85 (N version) / –40 to 85 (D version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Table 22.31 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.2	–	5.5	V
V_{SS}	Supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8 V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2 V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$		–	–	–160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$		–	–	–80	mA
$I_{OH(peak)}$	Peak output “H” current	All pins		–	–	–10	mA
$I_{OH(avg)}$	Average output “H” current	All pins		–	–	–5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL(peak)}$		–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” currents	Sum of all pins $I_{OL(avg)}$		–	–	80	mA
$I_{OL(peak)}$	Peak output “L” currents	All pins		–	–	10	mA
$I_{OL(avg)}$	Average output “L” current	All pins		–	–	5	mA
–	System clock		HRA01 = 0 Low-speed on-chip oscillator selected	–	125	–	kHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	8	MHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.2 V ≤ V_{CC} ≤ 5.5 V	–	–	4	MHz

NOTES:
1. V_{CC} = 2.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

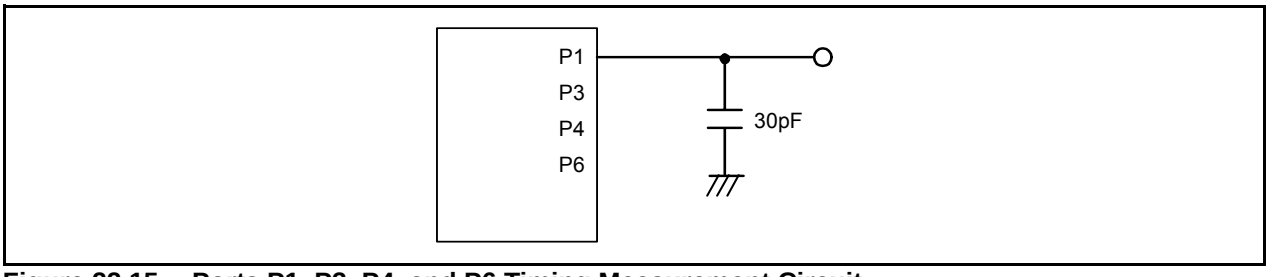


Figure 22.15 Ports P1, P3, P4, and P6 Timing Measurement Circuit

Table 22.32 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)		100(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.2	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(7)	Ambient temperature = 55°C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 22.33 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level		2.2	2.3	2.4	V
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	0.9	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(2)		–	–	300	µs
Vccmin	MCU operating voltage minimum value		2.2	–	–	V

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 22.34 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level(4)		2.70	2.85	3.00	V
–	Voltage monitor 1 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
4. This parameter shows the voltage detection level when the power supply drops.
   The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 22.35 Voltage Detection 2 Circuit Electrical Characteristics

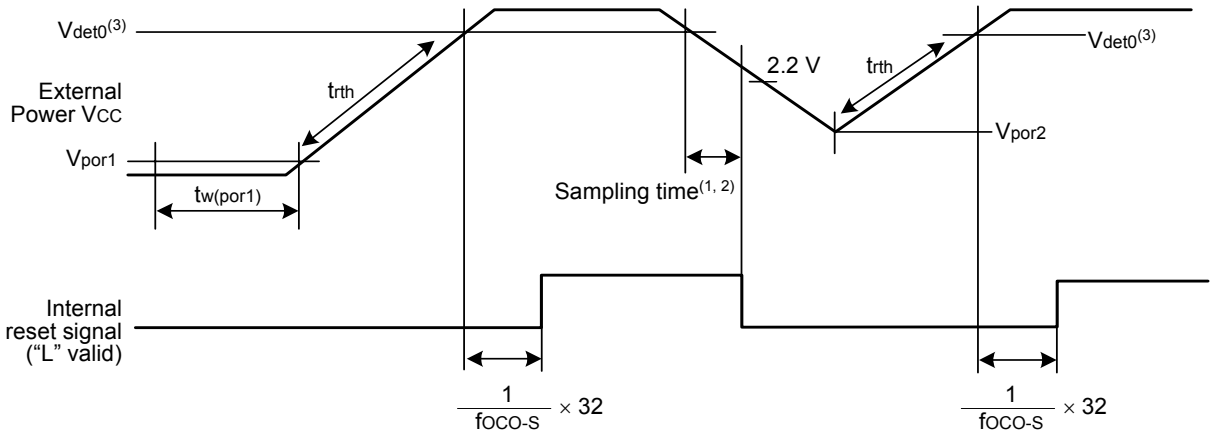
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level		3.3	3.6	3.9	V
–	Voltage monitor 2 interrupt request generation time(2)		–	40	–	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	0.6	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 22.36 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(3)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage(4)		–	–	0.1	V
V_{por2}	Power-on reset or voltage monitor 0 reset valid voltage		0	–	V_{det0}	V
t_{rth}	External power V_{CC} rise gradient(2)		20	–	–	mV/msec

NOTES:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. This condition (external power V_{CC} rise gradient) does not apply if $V_{CC} \geq 1.0$ V.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
4. $t_{w(por1)}$ indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain $t_{w(por1)}$ for 30 s or more if $-20°C \leq T_{opr} \leq 85°C$, maintain $t_{w(por1)}$ for 3,000 s or more if $-40°C \leq T_{opr} < -20°C$.



NOTES:
1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** for details.
3. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.

Figure 22.16 Reset Circuit Electrical Characteristics

Table 22.37 Comparator Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	Internal reference voltage	V_{CC} = 2.2 V to 5.5 V, T_{opr} = 25°C	1.15	1.25	1.35	V
		V_{CC} = 2.2 V to 5.5 V, T_{opr} = –40 to 85°C	–	1.25	–	V
Vcref	External input reference voltage	V_{CC} = 2.2 V to 4.0 V	0.5	–	V_{CC} – 1.1	V
		V_{CC} = 4.0 V to 5.5 V	0.5	–	V_{CC} – 1.5	V
Vcin	External comparison voltage input range		–0.3	–	V_{CC} + 0.3	V
Vofs	Input offset voltage		–	20	120	mV
Tcrsp	Response time		–	4	–	µs

NOTE:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.38 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-F	High-speed on-chip oscillator frequency temperature • supply voltage dependence	V_{CC} = 4.75 V to 5.25 V, T_{opr} = 0 to 60°C(2)	7.76	8	8.24	MHz
		V_{CC} = 2.7 V to 5.5 V, T_{opr} = –20 to 85°C(2)	7.68	8	8.32	MHz
		V_{CC} = 2.7 V to 5.5 V, T_{opr} = –40 to 85°C(2)	7.44	8	8.32	MHz
		V_{CC} = 2.2 V to 5.5 V, T_{opr} = –20 to 85°C(3)	7.04	8	8.96	MHz
		V_{CC} = 2.2 V to 5.5 V, T_{opr} = –40 to 85°C(3)	6.8	8	9.2	MHz

NOTES:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. These standard values show when the HRA1 register is set to the value before shipment and the HRA2 register is set to 00h.
3. These standard values show when the correction value in the FRA6 register is written into the HRA1 register.

Table 22.39 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
–	Oscillation stability time		–	10	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	15	–	µA

NOTE:
1. V_{CC} = 2.2 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.40 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 22.41 Electrical Characteristics (1) [V_{CC} = 5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = –200 μA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		I_{OL} = 5 mA	–	–	2.0	V
			I_{OL} = 200 μA	–	–	0.45	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, RXD0, CLK0		0.1	0.5	–	V
		$\overline{RESET}$		0.1	1.0	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5 V	–	–	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5 V	–	–	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5 V	30	50	167	kΩ
V_{RAM}	RAM hold voltage		During stop mode	2.0	–	–	V

NOTE:
1. V_{CC} = 4.2 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.42 Electrical Characteristics (2) [Vcc = 5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	8	mA
			High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	75	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	60	µA
		Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.8	3	µA
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.2	–	µA
			Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	8	µA
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	µA

Timing Requirements
(Unless Otherwise Specified: V_{CC} = 5 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 5 V]

Table 22.43 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

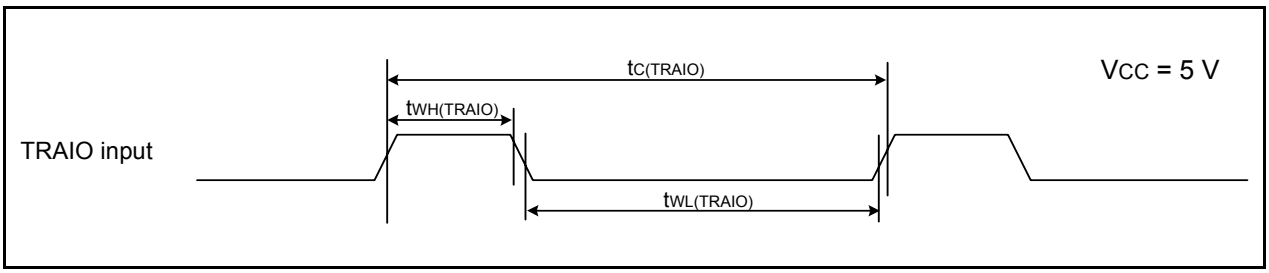


Figure 22.17 TRAIO Input Timing Diagram when V_{CC} = 5 V

Table 22.44 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	200	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	100	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	100	–	ns
$t_{d(C-Q)}$	TXD0 output delay time	–	50	ns
$t_{h(C-Q)}$	TXD0 hold time	0	–	ns
$t_{su(D-C)}$	RXD0 input setup time	50	–	ns
$t_{h(C-D)}$	RXD0 input hold time	90	–	ns

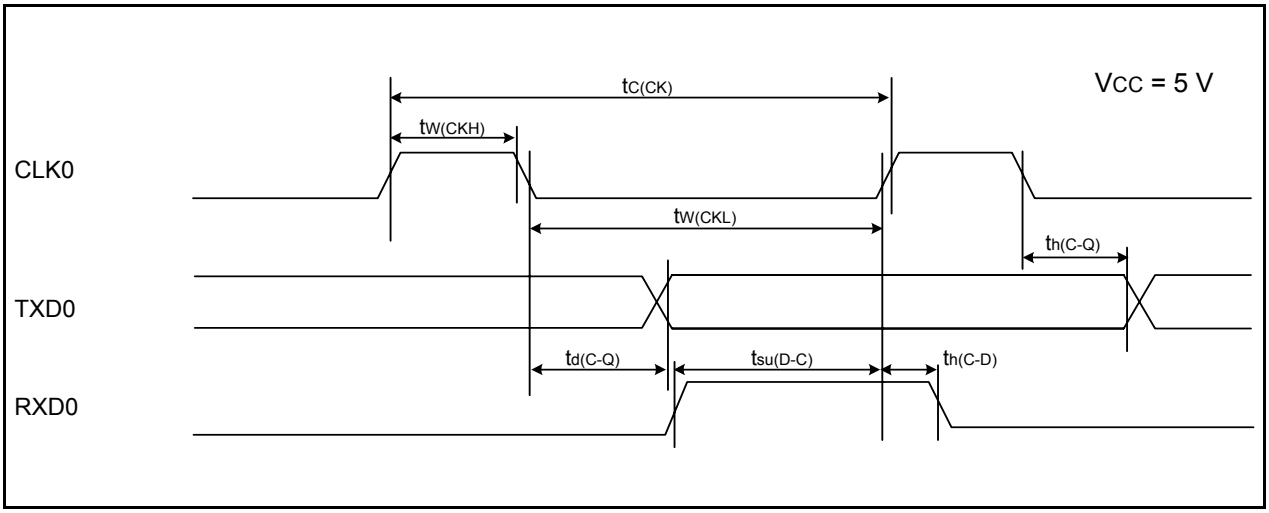


Figure 22.18 Serial Interface Timing Diagram when VCC = 5 V

Table 22.45 External Interrupt $\overline{INTi}$ (i = 0 or 1) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

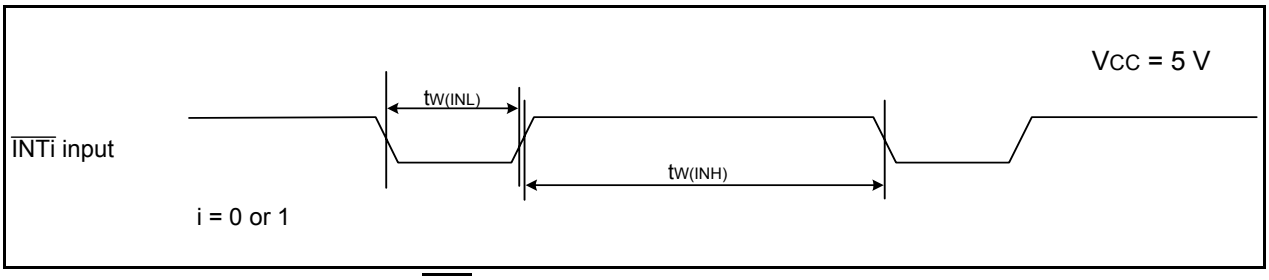


Figure 22.19 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 5 V

Table 22.46 Electrical Characteristics (3) [V_{CC} = 3 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, RXD0, CLK0		0.1	0.3	–	V
		$\overline{RESET}$		0.1	0.4	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3 V	–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3 V	–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3 V	66	160	500	kΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	–	–	V

NOTE:
1. V_{CC} =2.7 to 3.3 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.47 Electrical Characteristics (4) [Vcc = 3 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	5	–	mA
			High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	130	300	µA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	25	70	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	23	55	µA
		Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.7	3	µA
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.1	–	µA
			Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	7	µA
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	µA

Timing requirements
(Unless Otherwise Specified: V_{CC} = 3 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 3 V]

Table 22.48 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

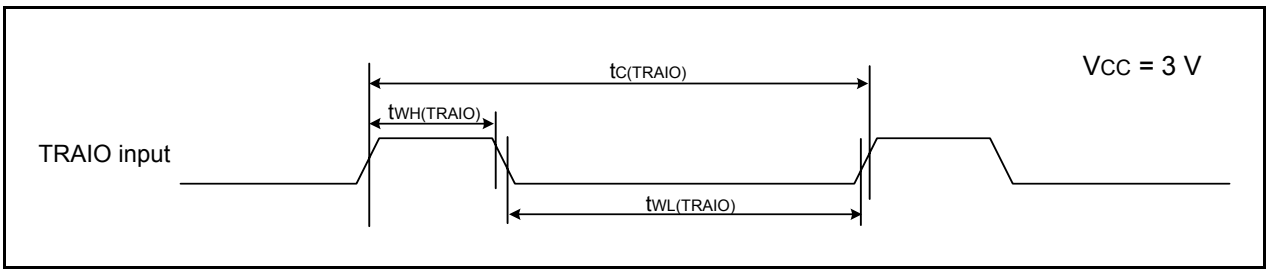


Figure 22.20 TRAIO Input Timing Diagram when V_{CC} = 3 V

Table 22.49 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	300	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	150	–	ns
$t_{W(CKL)}$	CLK0 Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXD0 output delay time	–	80	ns
$t_{h(C-Q)}$	TXD0 hold time	0	–	ns
$t_{su(D-C)}$	RXD0 input setup time	70	–	ns
$t_{h(C-D)}$	RXD0 input hold time	90	–	ns

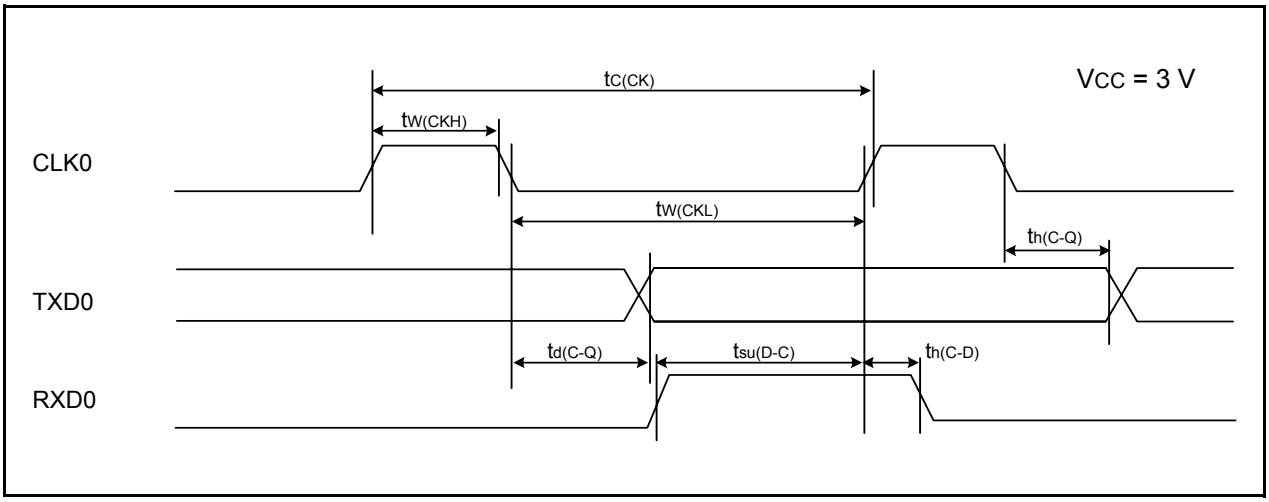


Figure 22.21 Serial Interface Timing Diagram when Vcc = 3 V

Table 22.50 External Interrupt $\overline{INTi}$ (i = 0 or 1) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

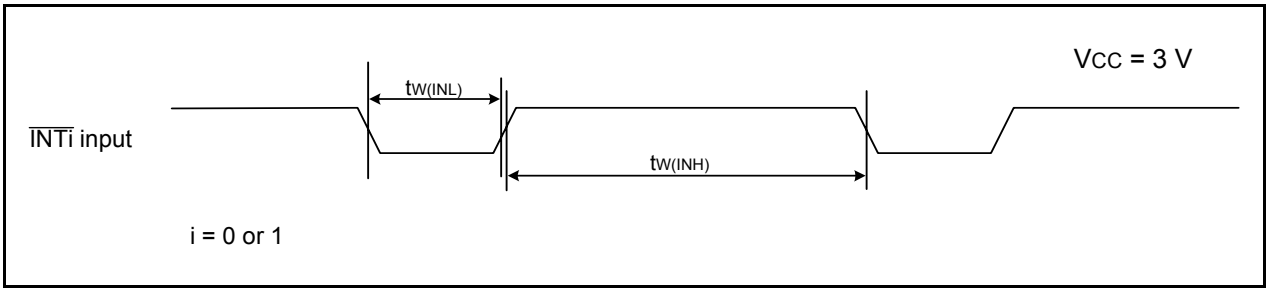


Figure 22.22 External Interrupt $\overline{INTi}$ Input Timing Diagram when Vcc = 3 V

Table 22.51 Electrical Characteristics (5) [V_{CC} = 2.2 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage		I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage		I_{OL} = 1 mA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, RXD0, CLK0		0.05	0.3	–	V
		$\overline{RESET}$		0.05	0.15	–	V
I_{IH}	Input “H” current		VI = 2.2 V	–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V	–	–	–4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V	100	200	600	kΩ
R_{fXCIN}	Feedback resistance	XCIN		–	35	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	–	–	V

NOTE:
1. V_{CC} = 2.2 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 22.52 Electrical Characteristics (6) [Vcc = 2.2 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	–	mA
			High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	–	100	230	µA
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	22	60	µA
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	20	55	µA
		Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	0.7	3	µA
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	–	1.1	–	µA
			Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5	7	µA
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	–	5.5	–	µA

Timing requirements
(Unless Otherwise Specified: V_{CC} = 2.2 V, V_{SS} = 0 V at T_{opr} = 25°C) [V_{CC} = 2.2 V]

Table 22.53 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	–	ns

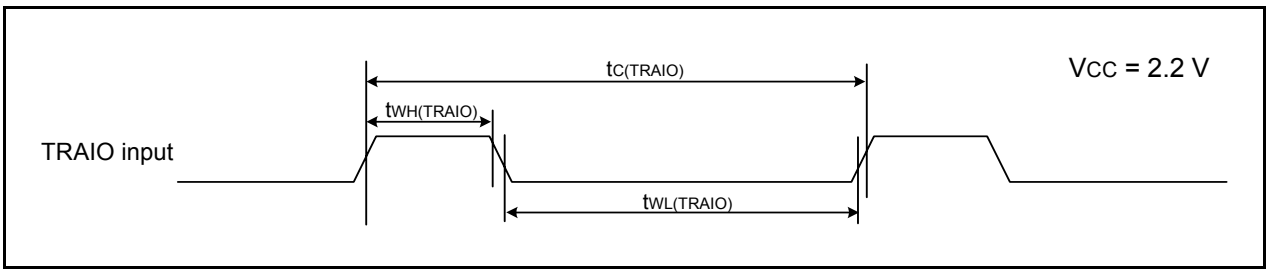


Figure 22.23 TRAIO Input Timing Diagram when V_{CC} = 2.2 V

Table 22.54 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	800	–	ns
$t_{W(CKH)}$	CLK0 input “H” width	400	–	ns
$t_{W(CKL)}$	CLK0 input “L” width	400	–	ns
$t_{d(C-Q)}$	TXD0 output delay time	–	200	ns
$t_{h(C-Q)}$	TXD0 hold time	0	–	ns
$t_{su(D-C)}$	RXD0 input setup time	150	–	ns
$t_{h(C-D)}$	RXD0 input hold time	90	–	ns

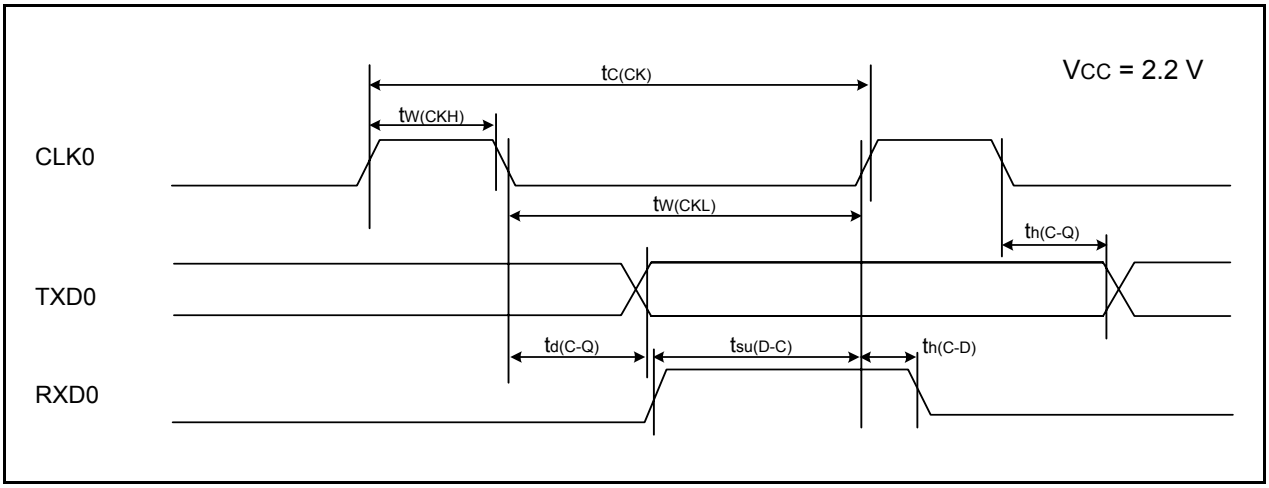


Figure 22.24 Serial Interface Timing Diagram when VCC = 2.2 V

Table 22.55 External Interrupt $\overline{INTi}$ (i = 0 or 1) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width	1000(1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width	1000(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

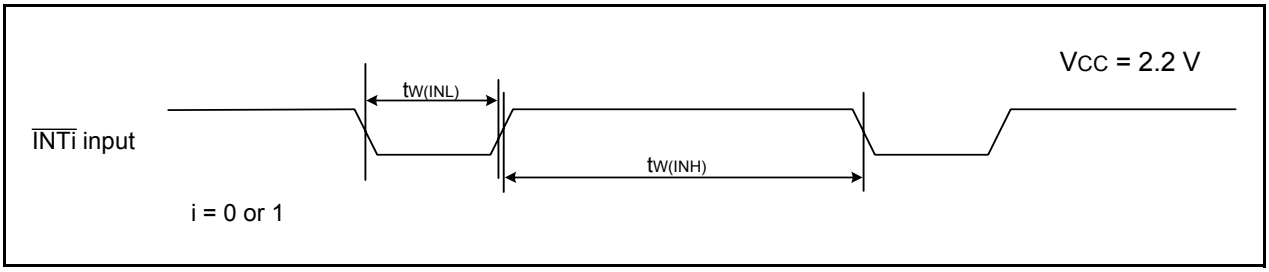


Figure 22.25 External Interrupt $\overline{INTi}$ Input Timing Diagram when VCC = 2.2 V

23. Usage Notes

23.1 Notes on I/O Ports

23.1.1 Port P4_3, P4_4 (for R8C/2H Group only)

Ports P4_3 and P4_4 are also used as the XCIN function and the XCOUT function, respectively. During a reset period and after a reset release, these ports are set to the XCIN and XCOUT functions. Pins P4_3 and P4_4 can be switched to the port functions by setting the CM04 bit in the CM0 register to 0 (ports P4_3 and P4_4) by a program.

To use ports P4_3 and P4_4 as ports, note the following:

- Port P4_3

After a reset until the CM04 bit is set to 0 (ports P4_3 and P4_4) by a program, a typical 10 MΩ impedance is connected between the P4_3 pin and the MCU power supply or GND. If the XCIN is set to intermediate-level input or left floating, a shoot-through current flows into the oscillation driver.

- Port P4_4

Use port P4_4 as an output port by setting the PD4_4 bit in the PD4 register to 1 (output mode). After a reset until the CM04 bit is set to 0 (ports P4_3 and P4_4) by a program, the P4_4 pin may output an intermediate potential of about 2.0 V.

23.2 Notes on Clock Generation Circuit

23.2.1 Stop Mode

When entering stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least 4 NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter stop mode

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        BSET    0,PRCR          ; Protect disabled
        FSET    I               ; Enable interrupt
        BSET    0,CM1           ; Stop mode
        JMP.B   LABEL_001
LABEL_001 :
        NOP
        NOP
        NOP
        NOP
```

23.2.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the WAIT instruction and the program stops. Insert at least 4 NOP instructions after the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1,FMR0          ; CPU rewrite mode disabled
        FSET    I               ; Enable interrupt
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

23.2.3 Oscillation Circuit Constants

Ask the manufacturer of the oscillator to specify the best oscillation circuit constants for your system.

23.3 Notes on Interrupts

23.3.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the acknowledged interrupt IR bit is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

23.3.2 SP Setting

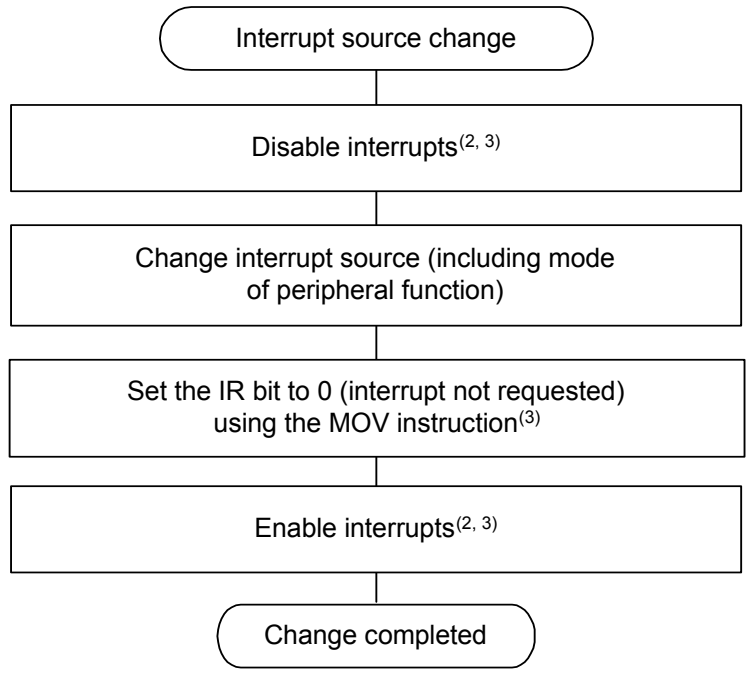
Set any value in the SP before an interrupt is acknowledged. The SP is set to 0000h after reset. Therefore, if an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

23.3.3 External Interrupt and Key Input Interrupt

Either "L" level or an "H" level of width shown in the Electrical Characteristics is necessary for the signal input to pins $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 22.17** (VCC = 5V), **Table 22.23** (VCC = 3V), **Table 22.29** (VCC = 2.2V), **Table 22.45** (VCC = 5V), **Table 22.50** (VCC = 3V), and **Table 22.55** (VCC = 2.2V) **External Interrupt $\overline{\text{INTi}}$ (i = 0 or 1) Input**.

23.3.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. When using an interrupt, set the IR bit to 0 (no interrupt requested) after changing the interrupt source. In addition, changes of interrupt sources include all factors that change the interrupt sources assigned to individual software interrupt numbers, polarities, and timing. Therefore, if a mode change of a peripheral function involves interrupt sources, edge polarities, and timing, set the IR bit to 0 (no interrupt requested) after the change. Refer to the individual peripheral function for its related interrupts.
Figure 23.1 shows an Example of Procedure for Changing Interrupt Sources.



IR bit: The interrupt control register bit of an interrupt whose source is changed.

NOTES:
1. Execute the above settings individually. Do not execute two or more settings at once (by one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled. If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 of the interrupt whose source is changed.
3. Refer to **13.5.5 Changing Interrupt Control Register Contents** for the instructions to be used and usage notes.

Figure 23.1 Example of Procedure for Changing Interrupt Sources

23.3.5 Changing Interrupt Control Register Contents

(a) The contents of an interrupt control register can only be changed while no interrupt requests corresponding to that register are generated. If interrupt requests may be generated, disable interrupts before changing the interrupt control register contents.

(b) When changing the contents of an interrupt control register after disabling interrupts, be careful to choose appropriate instructions.
Changing any bit other than IR bit
If an interrupt request corresponding to a register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt request may be ignored. If this causes a problem, use the following instructions to change the register: AND, OR, BCLR, BSET
Changing IR bit
If the IR bit is set to 0 (interrupt not requested), it may not be set to 0 depending on the instruction used. Therefore, use the MOV instruction to set the IR bit to 0.

(c) When disabling interrupts using the I flag, set the I flag as shown in the sample programs below. Refer to (b) regarding changing the contents of interrupt control registers by the sample programs.

Sample programs 1 to 3 are for preventing the I flag from being set to 1 (interrupts enabled) before the interrupt control register is changed for reasons of the internal bus or the instruction queue buffer.

Example 1: Use NOP instructions to prevent I flag from being set to 1 before interrupt control register is changed

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use dummy read to delay FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use POPC instruction to change I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

23.4 Notes on ID Code Areas

23.4.1 Setting Example of ID Code Areas

As the ID code areas are allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

23.5 Notes on Option Function Select Area

23.5.1 Setting Example of Option Function Select Area

As the option function select area is allocated in the flash memory (not in the SFRs), they cannot be rewritten by executing an instruction. Write appropriate values when creating a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)      ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

23.6 Notes on Timers

23.6.1 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RA(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

23.6.2 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0, 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB(1)other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB(1) other than the TCSTF bit.

  NOTE:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.

23.6.2.1 Timer mode

The following workaround should be performed in timer mode.
To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

23.6.2.2 Programmable waveform generation mode

The following three workarounds should be performed in programmable waveform generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) To change registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), synchronize the TRBO output cycle using a timer RB interrupt, etc. This operation should be preformed only once in the same output cycle. Also, make sure that writing to the TRBPR register does not occur during period A shown in Figures 23.2 and 23.3.

The following shows the detailed workaround examples.

- Workaround example (a):
  As shown in Figure 23.2, write to registers TRBSC and TRBPR in the timer RB interrupt routine. These write operations must be completed by the beginning of period A.

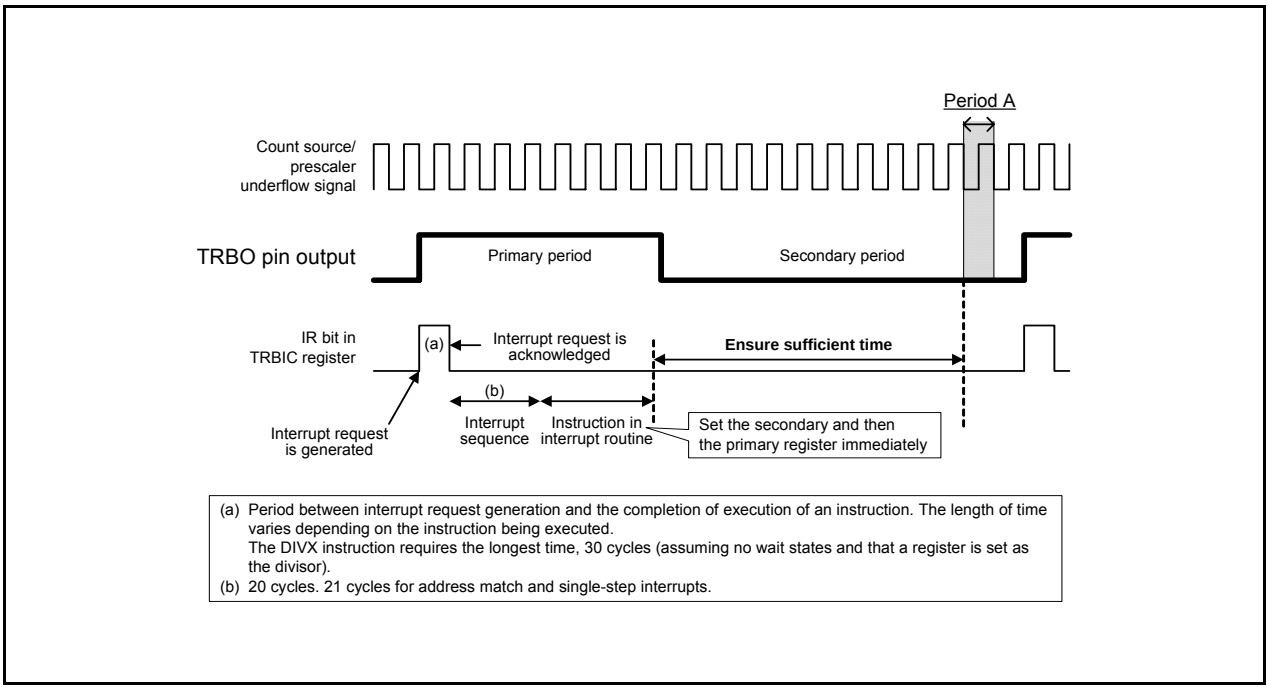


Figure 23.2 Workaround Example (a) When Timer RB interrupt is Used

• Workaround example (b):
As shown in Figure 23.3 detect the start of the primary period by the TRBO pin output level and write to registers TRBSC and TRBPR. These write operations must be completed by the beginning of period A.
If the port register's bit value is read after the port direction register's bit corresponding to the TRBO pin is set to 0 (input mode), the read value indicates the TRBO pin output value.

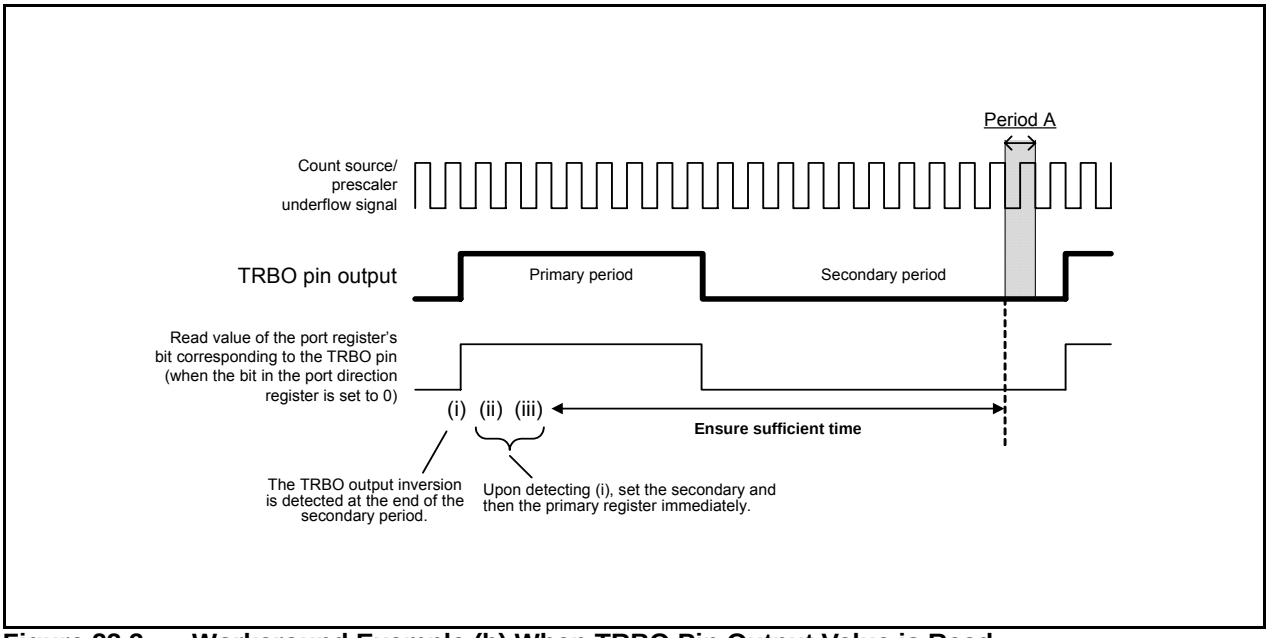


Figure 23.3 Workaround Example (b) When TRBO Pin Output Value is Read

(3) To stop the timer counting in the primary period, use the TSTOP bit in the TRBCR register. In this case, registers TRBPRE and TRBPR are initialized and their values are set to the values after reset.

23.6.2.3 Programmable one-shot generation mode

The following two workarounds should be performed in programmable one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

• When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.

• When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

23.6.2.4 Programmable wait one-shot generation mode

The following three workarounds should be performed in programmable wait one-shot generation mode.

(1) To write to registers TRBPRE and TRBPR during count operation (TCSTF bit is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

(2) Do not set both the TRBPRE and TRBPR registers to 00h.

(3) Set registers TRBSC and TRBPR using the following procedure.

(a) To use "$\overline{\text{INT0}}$ pin one-shot trigger enabled" as the count start condition
Set the TRBSC register and then the TRBPR register. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before trigger input from the $\overline{\text{INT0}}$ pin.

(b) To use "writing 1 to TOSST bit" as the start condition
Set the TRBSC register, the TRBPR register, and then TOSST bit. At this time, after writing to the TRBPR register, allow an interval of 0.5 or more cycles of the count source before writing to the TOSST bit.

23.6.3 Notes on Timer RE (for R8C/2H Group only)

23.6.3.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE(1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

NOTE:
1. Registers associated with timer RE: TRESEC, TREMIN, TREHR, TREWK, TRECR1, TRECR2, TRECSR, and TREOPR.

23.6.3.2 Register Setting

Write to the following registers or bits when timer RE is stopped.

- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24, PM, and INT in TRECR1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.
Figure 23.4 shows a Setting Example in Real-Time Clock Mode.

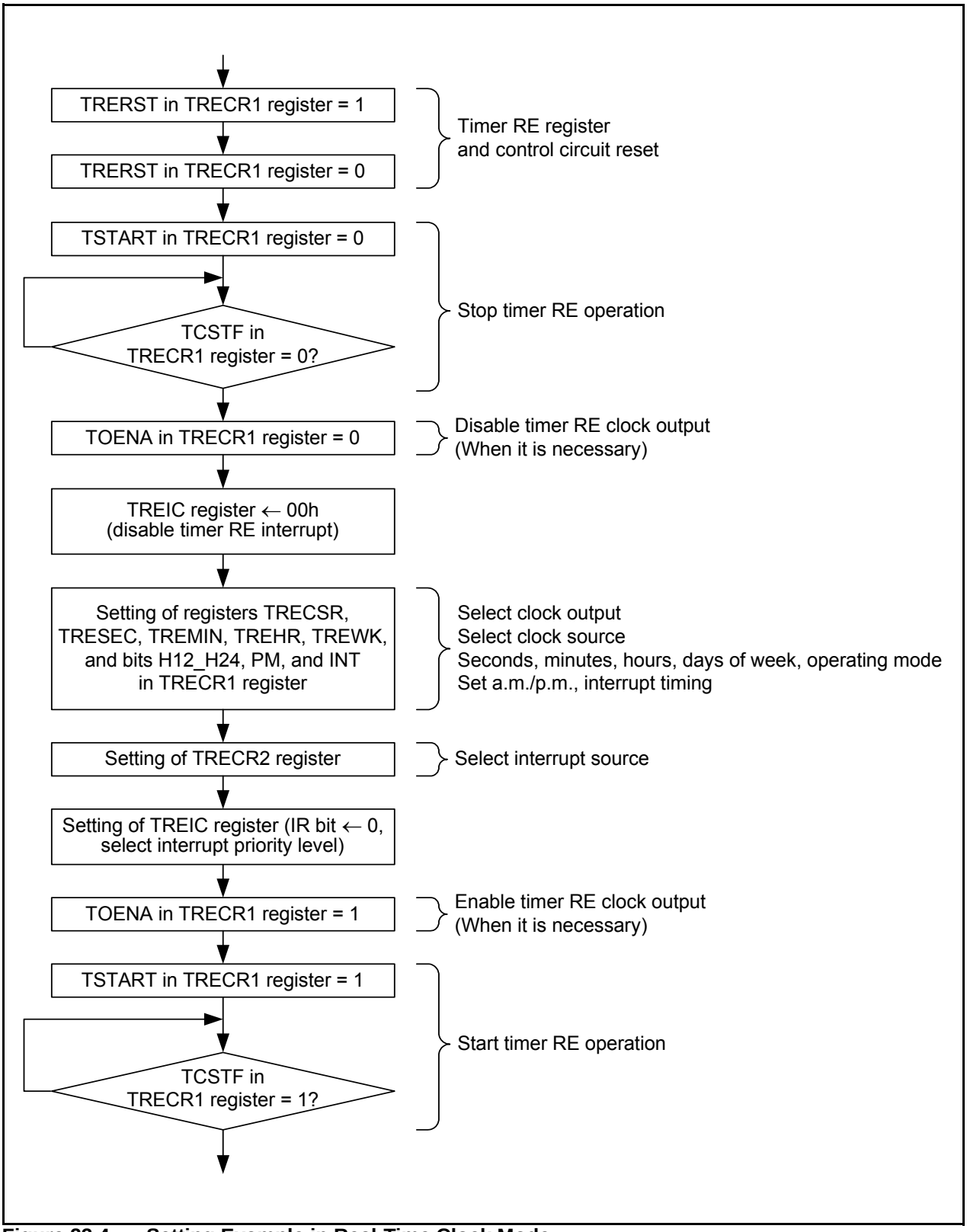


Figure 23.4 Setting Example in Real-Time Clock Mode

23.6.3.3 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECR1 register when the BSY bit is set to 0 (not while data is updated).
Also, when reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.

In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register in the timer RE interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).
(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register.
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

23.6.4 Notes on Timer RF

- Access registers TRF, TRFM0, and TRFM1 in 16-bit units.

Example of reading timer RF:

```
MOV.W    0290H,R0    ; Read out timer RF
```

- In input capture mode, a capture interrupt request is generated by inputting an edge selected by bits TRFC03 and TRFC04 in the TRFCR0 register even when the TSTART bit in the TRFCR0 register is set to 0 (count stops).

23.7 Notes on Serial Interface

- When reading data from the UiRB (i = 0 or 2 (for the R8C/2H Group only)) register either in the clock synchronous serial I/O mode or in the clock asynchronous serial I/O mode. Ensure the data is read in 16-bit units. When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0.
  To check receive errors, read the UiRB register and then use the read data.

Example (when reading receive buffer register):

```
MOV.W    00A6H,R0    ; Read the U0RB register
```

- When writing data to the UiTB register in the clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first then the low-order byte, in 8-bit units.

Example (when reading transmit buffer register):

```
MOV.B    #XXH,00A3H  ; Write the high-order byte of U0TB register
MOV.B    #XXH,00A2H  ; Write the low-order byte of U0TB register
```

23.8 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

23.9 Notes on Flash Memory

23.9.1 CPU Rewrite Mode

23.9.1.1 Operating Speed

Before entering CPU rewrite mode (EW0 mode), select 5 MHz or below for the CPU clock using the CM06 bit in the CM0 register and bits CM16 to CM17 in the CM1 register.

23.9.1.2 Prohibited Instructions

The following instructions cannot be used in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

23.9.1.3 Non-Maskable Interrupts

- EW0 Mode
  Once a watchdog timer, voltage monitor1, voltage monitor 2, comparator 1, or comparator 2 interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts after a fixed period and the flash memory restarts.
  As the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be readable. Execute auto-erasure again and ensure it completes normally.
  The watchdog timer does not stop during command operation, so that interrupt requests may be generated. Initialize the watchdog timer regularly.
  Do not use the address match interrupt while a command is being executed because the vector of the address match interrupt is allocated in ROM.
  Do not use a non-maskable interrupt while block 0 is being automatically erased because the fixed vector is allocated in block 0.

23.9.1.4 How to Access

Write 0 before writing 1 when setting Bits FMR01, FMR02 in the FMR0 register, or FMR11 bit in the FMR1 register to 1. Do not generate an interrupt between writing 0 and 1.

23.9.1.5 Rewriting User ROM Area

In EW0 Mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

23.9.1.6 Program

Do not write additions to the already programmed address.

23.9.1.7 Program and Erase Voltage for Flash Memory

To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.

23.10 Notes on Noise

23.10.1 Inserting a Bypass Capacitor between VCC and VSS Pins as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (at least 0.1 μF) using the shortest and thickest write possible.

23.10.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

24. Notes for On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/2H Group and R/2J Group, take note of the following:

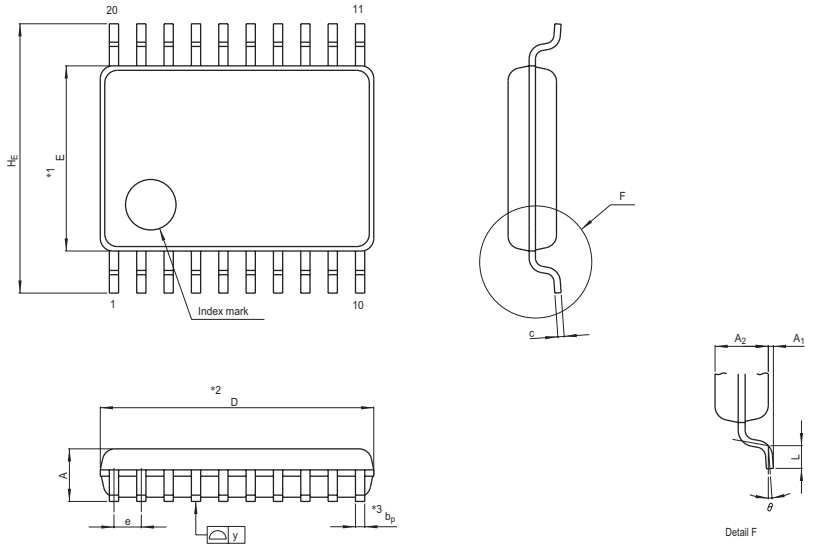
(1) Some of the user flash memory and RAM areas are used by the on-ship debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIER, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(3) Do not use the BRK instruction in a user system.
(4) Debugging is available under the condition of supply voltage VCC = 2.7 to 5.5 V. Debugging with the on-chip debugger under less than 2.7 V is not allowed.

Connecting and using the on-chip debugger has some special restrictions. Refer to the on-chip debugger manual for details.

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g

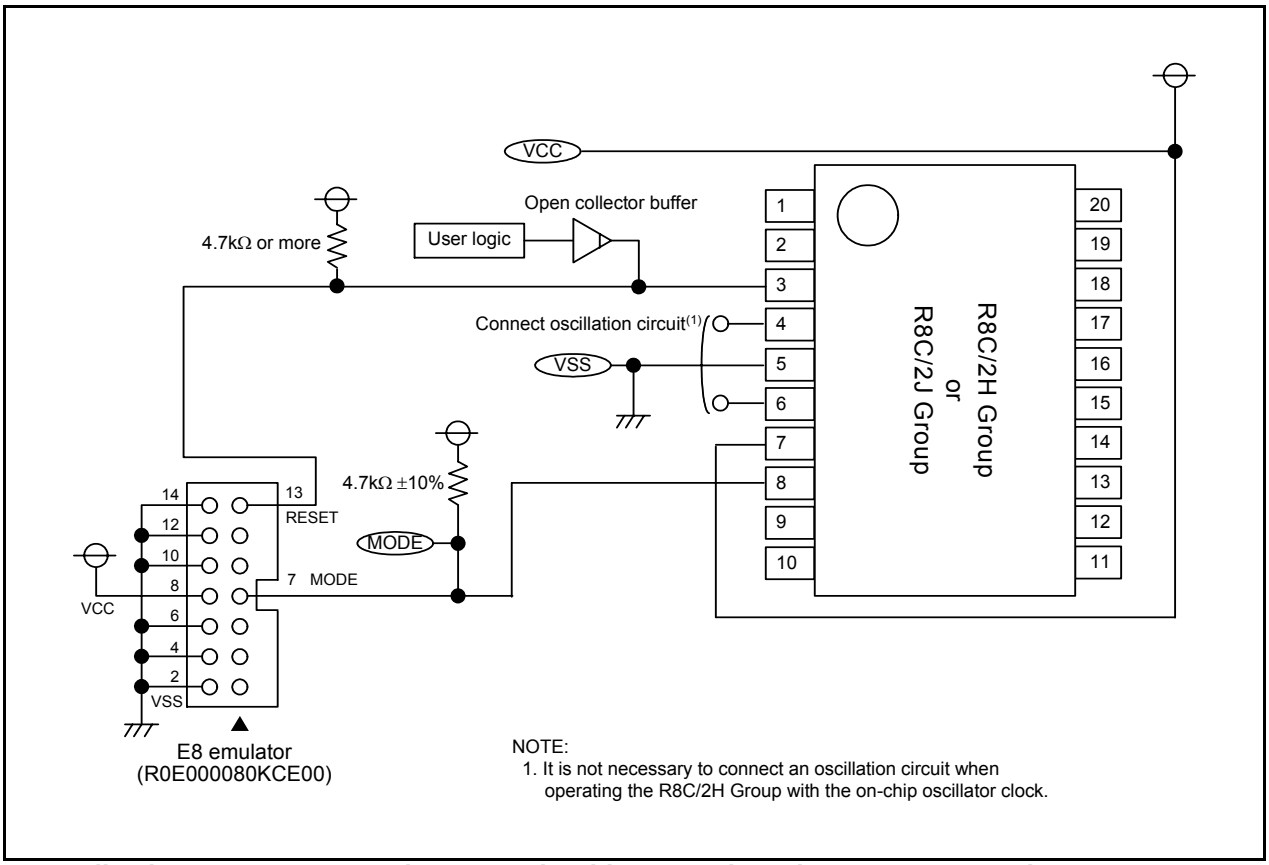


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

Appendix 2. Connection Examples with On-Chip Debugging Emulator

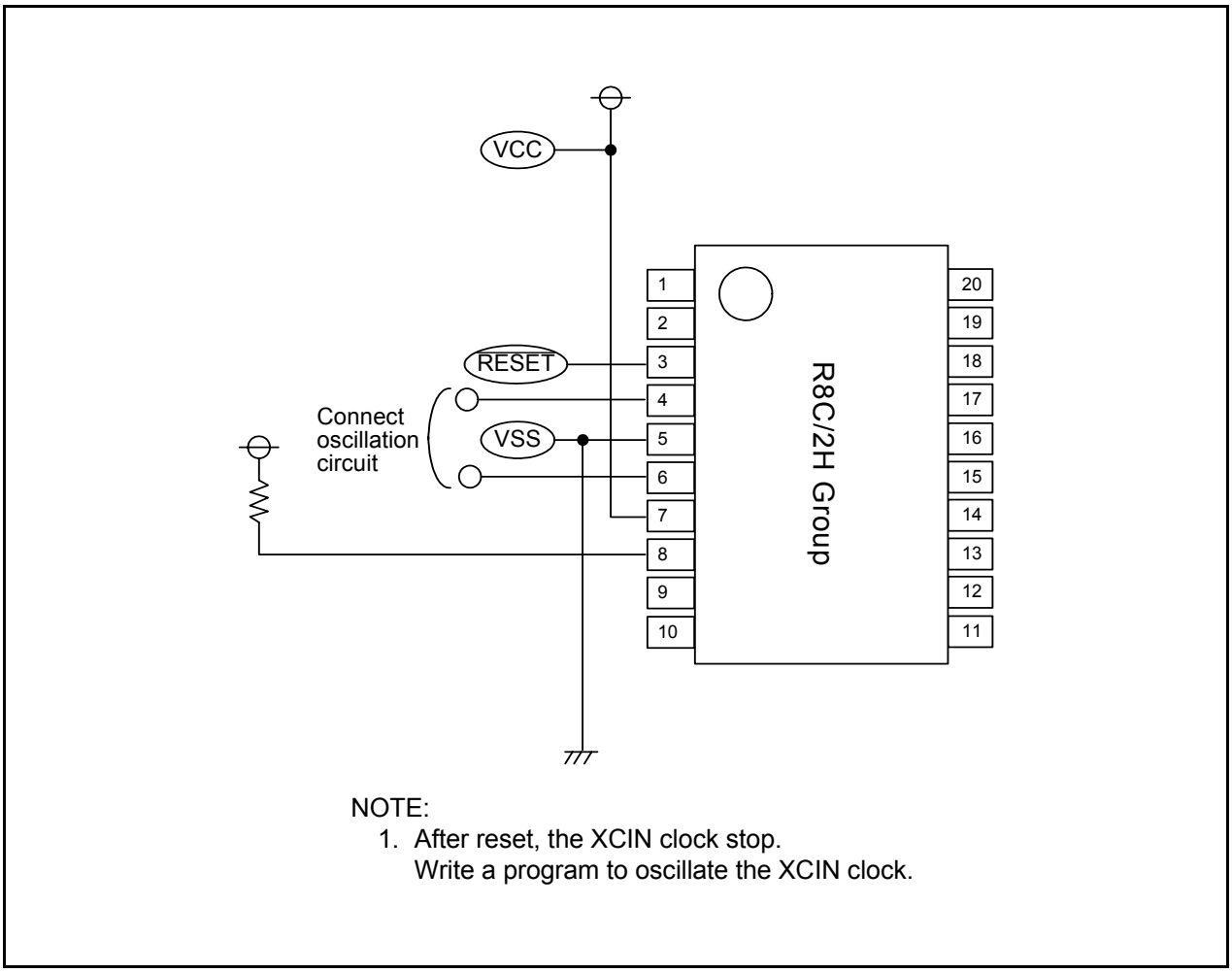
Appendix Figure 2.1 shows a Connection Example with E8 Emulator (R0E000080KCE00).



Appendix Figure 2.1 Connection Example with E8 Emulator (R0E000080KCE00)

Appendix 3. Example of Oscillation Evaluation Circuit

Appendix Figure 3.1 shows an Example of Oscillation Evaluation Circuit.



NOTE:
1. After reset, the XCIN clock stop.
   Write a program to oscillate the XCIN clock.

Appendix Figure 3.1 Example of Oscillation Evaluation Circuit

Index

REVISION HISTORY	R8C/2H Group, R8C/2J Group Hardware Manual

Rev.	Date	Description	
		Page	Summary
0.01	Apr 06, 2007	–	First Edition issued
0.10	Jul 20, 2007	–	Descriptions about “R8C/2J” added
		–	“RENESAS TECHNICAL UPDATE” reflected: TN-16C-A164A/E, TN-16C-A167A/E
		–	Register/bit symbols revised: “CM1POR” → “LCM1POR”, “CM2POR” → “LCM2POR”, “ACMR” → “ALCMR”
		2	Table 1.1: Clock; “Real-time clock (timer RE)” added
		20, 43	Table 4.2, Figure 6.6: 0038h After reset; “0000X010b” → “1000X010b”, “0100X011b” → “1100X011b”
		32	Figure 5.3 revised
		33, 139, 147, 252	Figure 5.4, Figure 15.2, Figure 16.6, Figure 20.2: OFS Register; NOTE1 revised
		69	Table 8.3, Table 8.4: NOTE1 revised
		74	Figure 8.5, Figure 8.6: revised
		78	Figure 8.11 revised
		157	Figure 17.5 “Both bits .... register are set to 0 (During count).” → “Both bits .... register are set to 1 (During count).”
		175	Figure 17.17 “Both bits .... register are set to 0 (During count).” → “Both bits .... register are set to 1 (During count).”
		186	NOTE: “TRBIOC” added
		240	Figure 19.6 revised
		241	Figure 19.7: SFDCT flag in the LINST register; “Set by ....the B1CLR bit in the LINST register” → “Set by ....the B0CLR bit in the LINST register”
		243	Figure 19.9 revised
		250	Figure 20.1 revised
		286	Figure 21.2 NOTE4 deleted
0.20	Nov 12, 2007	2	Table 1.1 I/O Ports: “• Output-only: 1” added “• CMOS I/O ports: 16” → “• CMOS I/O ports: 15”
		6	Figure 1.3 revised
		8	Figure 1.5 revised
		9	Table 1.5 Pin Number: 4, 6, 16 revised
		12	Table 1.7 I/O port: “P4_3 to P4_5” → “P4_3, P4_5” Timer RE, Output port added
		19	Table 4.1 0006h “01001000b” → “01011000b”
		23	Table 4.5 0118h to 011Dh: After reset revised 011Fh “Timer RE Real-Time Clock Precision Adjust Register” added
		52	Figure 6.13 revised

Rev.	Date	Description	
		Page	Summary
0.20	Nov 12, 2007	68	8. “There are 16 input/output .... oscillation circuit is not used.” → “There are 15 input/output .... used as an output port. Table 8.1 revised, NOTE3 added
		72	Figure 8.3 revised
		74	Figure 8.5 NOTE2 “To use port P4_4 as ... an input port.” added
		78	Figure 8.11 Pull-Up Control Register 1 (R8C/2H Group): b1 revised
		83	Table 8.16 NOTE2 added Table 8.17 revised
		84	Table 8.21 revised
		86	8.6 added
		89	Table 11.1 Oscillator status after reset: XCIN Clock Oscillation Circuit “Stop” → “Oscillate”
		92	Figure 11.3 revised
		102	11.2 “During and after reset, the XCIN clock stops.” → “During and after reset, the XCIN clock oscillates.”
		154	Figure 17.1 “TSTART” → “TCSTF”
		192	Figure 17.26 revised
		193	Table 17.11 revised
		194	Figure 17.27, Figure 17.28 After Reset “00h” → “Undefined”
		195	Figure 17.29 After Reset “00h” → “X0XXXXXXb” Figure 17.30 After Reset “00h” → “X0000XXXb”
		196	Figure 17.31 After Reset “00h” → “XXX0X0X0b”
		197	Figure 17.33 After Reset “00h” → “00XXXXXXb”
		198	Figure 17.34 revised Figure 17.35 added
		200	Figure 17.37 revised
		201	Table 17.13 revised
		202	Figure 17.38, Figure 17.39 After Reset “00h” → “Undefined”
		203	Figure 17.40 revised Figure 17.41 After Reset “00h” → “00XXXXXXb”
		204	Figure 17.42 revised
		205	Figure 17.43 revised
		206	17.3.3.1 NOTE1 “TREOPR” added
		207	Figure 17.44 revised
		213	Figure 17.50 NOTE4 added
		247	Figure 19.9 revised
		283	Table 22.2 NOTE2 revised
		300	Table 22.31 NOTE2 revised
		306, 310, 314	Table 22.42, Table 22.47, Table 22.52 revised

Rev.	Date	Description	
		Page	Summary
0.20	Nov 12, 2007	330	Figure 23.4 revised
1.00	Mar 28, 2008	All pages	“Under development” deleted
		2, 3	Table 1.1, Table 1.2 revised
		4, 5	Table 1.3, Table 1.4; “(D): Under development” deleted
		17, 18	Figure 3.1, Figure 3.2; “Expanded area” deleted
		19	Table 4.1 “002Eh” “002Fh” revised
		20	Table 4.2 “003Eh” “003Fh” revised
		31	Figure 5.1 NOTE1 added
		32	Table 5.2 revised
		45, 58	Figure 6.8, Figure 7.5; “7. The VW2C7 ... 1.” → “7. The VW2C7 ... 0.”
		55	Figure 7.2 added
		60, 61	Figure 7.9, Figure 7.10 added
		70, 71	7.6, Figure 7.16, Figure 7.17 added
		89	Table 8.23 NOTE4 revised Figure 8.12 NOTE2 revised
		93	Table 11.2 revised
		97	Figure 11.4; “01001000b” → “01011000b”, b4 revised, NOTE3 added
		99	Figure 11.6 b4 revised
		107, 109	11.3.1, 11.4.1.1, 11.4.1.2; “(for R8C/2H Group only)” added
		110	11.4.2 “(for R8C/2H Group only)” added Table 11.5; Timer RA interrupt: CM02 = 1 “NOTE1” added
		117	12, Figure 12.1; “BGRCR, and BGRTRM” added
		157	Table 17.1 Timer RF “Capture interrupt” added
		174	Figure 17.12 “TSTRAT” → “TSTART”
		181	Table 17.8 “... P3_1 (P1_3) ...” → “... P1_3 ...”
		184	Table 17.9 “TRBP pin function” → “TRBO pin function”
		248	Figure 19.6 “Three to five ...” → “One to two ...”
		251	Figure 19.9 revised
		257	Table 20.1 “Suspend ...” deleted, “Blocks 0 and 1 ...” → “Block 0 ...”
		261	20.4 “The flash module ... (EW0 mode).” deleted Table 20.3 “... to erase-suspend” “... to program-suspend” deleted
		263	• FMR00 Bit “(including suspend periods)” deleted
		264	Table 20.4 “FRM0 Register ...” → “FMR0 Register ...”
		266	Figure 20.5 revised • FMR40 Bit, • FMR41 Bit, • FMR42 Bit; deleted • FMR43 Bit, • FMR44 Bit, • FMR46 Bit; revised
		269	Figure 20.8 revised
		271	• Program Command; revised Old Figure 20.11 deleted

Rev.	Date	Description	
		Page	Summary
1.00	Mar 28, 2008	272	• Block Erase; revised Old Figure 20.13, Old 20.4.3.2, Old Figure 20.14, Old Figure 20.15; deleted
		275	Table 20.6 revised
		277	Old 20.7.1.7, Old 20.7.1.8 deleted
		278	21.2.3 “(for R8C/2H Group only)” added
		283	Table 22.3 revised Old Figure 22.2 deleted
		286	Table 22.8, Table 22.11 revised Table 22.9 revised, NOTE3 added
		288	Table 22.13 revised
		292	Table 22.19 revised
		296	Table 22.25 revised
		300	Table 22.32 revised Old Figure 22.17 deleted
		303	Table 22.37, Table 22.40 revised Table 22.38 revised, NOTE3 added
		305	Table 22.42 revised
		309	Table 22.47 revised
		313	Table 22.52 revised
		334	Old 23.9.1.7, Old 23.9.1.8 deleted

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