

# MC100EL39

## 5 V ECL ÷2/4, ÷4/6 Clock Generation Chip

### Description

The MC100EL39 is a low skew  $\pm 2/4$ ,  $\pm 4/6$  clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu\text{F}$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The common enable ( $\overline{\text{EN}}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EL39s, the Master Reset (MR) input must be asserted to ensure synchronization. For systems which only use one EL39, the MR pin need not be exercised as the internal divider design ensures synchronization between the  $\pm 2/4$  and the  $\pm 4/6$  outputs of a single device.

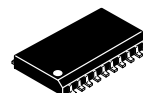
### Features

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection:
  - ◆ > 2 kV Human Body Model
  - ◆ > 100 V Machine Model
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 4.2 \text{ V}$  to  $5.7 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -4.2 \text{ V}$  to  $-5.7 \text{ V}$
- Internal Input Pulldown Resistors on  $\overline{\text{EN}}$ , MR, CLK(s), and DIVSEL(s)
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity: Level 3 (Pb-Free)  
(For Additional Information, see Application Note [AND8003/D](#))
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index 28 to 34
- Transistor Count = 419 Devices
- This Device is Pb-Free, Halogen Free and is RoHS Compliant



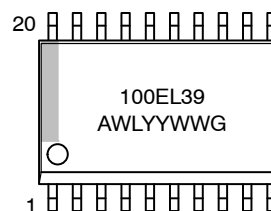
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SOIC-20 WB  
DW SUFFIX  
CASE 751D-05

### MARKING DIAGRAM\*



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

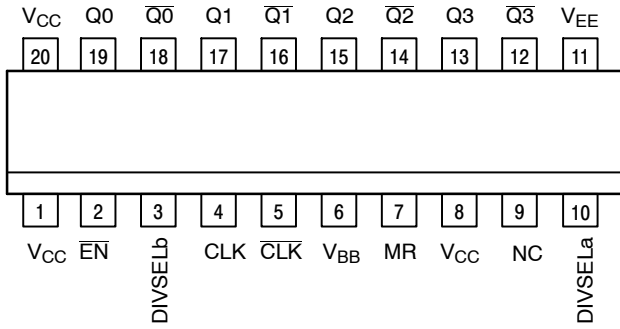
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping†
MC100EL39DWR2G	SOIC-20 WB (Pb-Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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NOTE: All V<sub>CC</sub> pins are tied together on the die.

Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout: SOIC-20 (Top View)

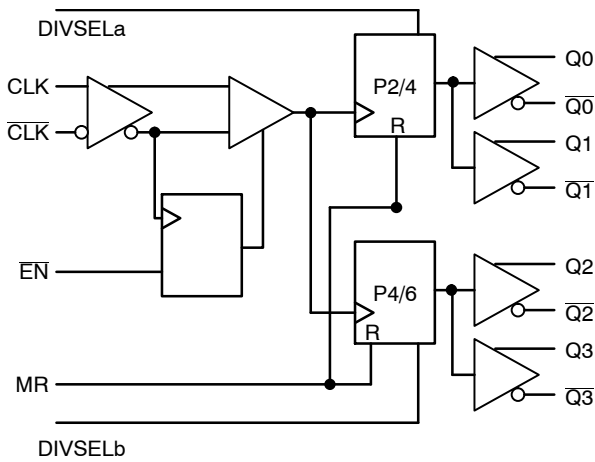


Figure 2. Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
CLK, $\overline{\text{CLK}}$	ECL Diff Clock Inputs
EN	ECL Sync Enable
MR	ECL Master Reset
Q0, $\overline{\text{Q0}}$ ; Q1, $\overline{\text{Q1}}$	ECL Diff $\pm 2/4$ Outputs
Q2, $\overline{\text{Q2}}$ ; Q3, $\overline{\text{Q3}}$	ECL Diff $\pm 4/6$ Outputs
DIVSELa, DIVSELb	ECL Frequency Select Input
V <sub>BB</sub>	Reference Voltage Output
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
NC	No Connect

Table 2. FUNCTION TABLE

Function	CLK*	EN*	MR*
Divide	Z	L	L
Hold Q <sub>0-3</sub>	ZZ	H	L
Reset Q <sub>0-3</sub>	X	X	H

Z = Low-to-High Transition

ZZ = High-to-Low Transition

\*Pin will default low when left open.

DIVSELa**	Q <sub>0</sub> , Q <sub>1</sub> Outputs
0	Divide by 2
1	Divide by 4
DIVSELb**	Q <sub>2</sub> , Q <sub>3</sub> Outputs
0	Divide by 4
1	Divide by 6

\*\*Pin will default low when left open.

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**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-8	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 -6	V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			±0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-20 WB SOIC-20 WB	90 60	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20 WB	30 to 35	°C/W
T <sub>sol</sub>	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260°C		265 265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 4. 100EL SERIES PECL DC CHARACTERISTICS** (V<sub>CC</sub> = 5.0 V; V<sub>EE</sub> = 0.0 V (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		50	59		50	59		54	61	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V <sub>BB</sub>	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V <sub>IHCMR</sub>	Common Mode Range (Differential) (Note 3) V <sub>PP</sub> < 500 mV V <sub>PP</sub> ≥ 500 mV	1.3 1.5		4.6 4.6	1.2 1.4		4.6 4.6	1.2 1.4		4.6 4.6	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> - 2.0 V.
3. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>. V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V<sub>PPmin</sub> and 1.0 V.

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**Table 5. 100EL SERIES NECL DC CHARACTERISTICS** ( $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		50	59		50	59		54	61	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Common Mode Range (Differential) (Note 3) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$										V
		-3.7		-0.4	-3.8		-0.4	-3.8		-0.4	
		-3.5		-0.4	-3.6		-0.4	-3.6		-0.4	
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ;  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and 1.0 V.

**Table 6. AC CHARACTERISTICS** ( $V_{CC} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency	1.0			1.0			1.0			GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output CLK $\rightarrow$ Q (Differential) CLK $\rightarrow$ Q (Single-Ended) MR $\rightarrow$ Q	850 850 600		1150 1150 900	900 900 610		1200 1200 910	950 950 630		1250 1250 930	ps
$t_{SKEW}$	Within-Device Skew (Note 2) Part-to-Part $Q_0-Q_3$ $Q_0-Q_3$ (Diff)			50 200			50 200			50 200	ps
$t_{JITTER}$	Random CLOCK Jitter (RMS) @ 1.0 GHz		2.0	3.0		2.0	3.0		2.0	3.0	ps
$t_S$	Setup Time $\overline{EN} \rightarrow \overline{CLK}$ DIVSEL $\rightarrow$ CLK	250 400			250 400			250 400			ps
$t_H$	Hold Time CLK $\rightarrow$ EN CLK $\rightarrow$ Div_Sel	100 150			100 150			100 150			ps
$V_{PP}$	Input Swing (Note 3)	150		1000	150		1000	150		1000	mV
$t_{RR}$	Reset Recovery Time			100			100			100	ps
$t_{PW}$	Minimum Pulse Width CLK MR	500 700			500 700			500 700			ps
$t_r, t_f$	Output Rise/Fall Times Q (20%–80%)	280		550	280		550	280		550	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1.  $V_{EE}$  can vary +0.8 V / -0.5 V. Outputs are terminated through 50  $\Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
2. Skew is measured between outputs under identical transitions.
3.  $V_{PP(min)}$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .

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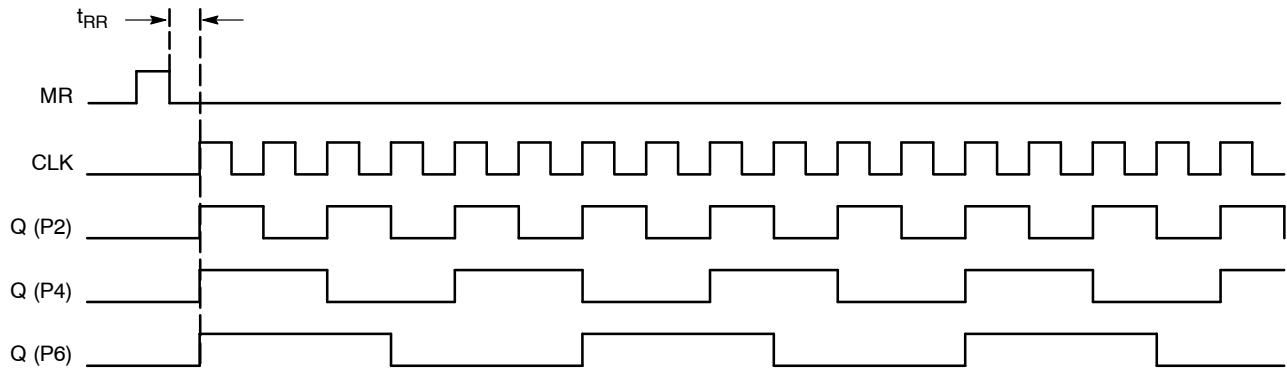


Figure 3. Timing Diagram

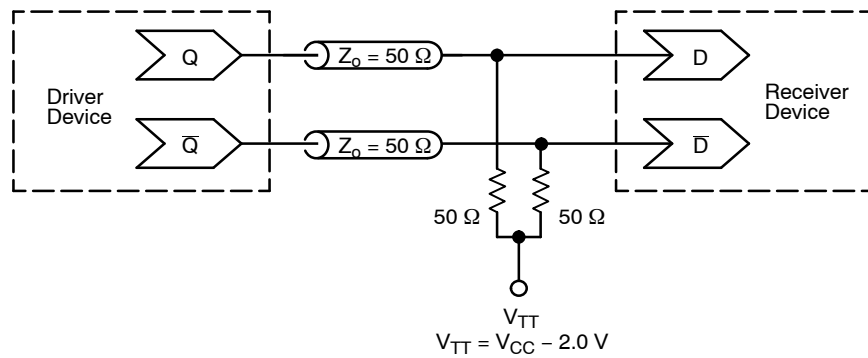



Figure 4. Typical Termination for Output Driver and Device Evaluation  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

## Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices



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