# Octal D-Type Latch with 3-State Output

The MC74VHCT573A is an advanced high speed CMOS octal latch with 3-state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT573A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage—input/output voltage mismatch, battery backup, hot insertion, etc.

#### **Features**

- High Speed:  $t_{PD} = 7.7 \text{ ns (Typ)}$  at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- TTL-Compatible Inputs:  $V_{IL} = 0.8 \text{ V}$ ;  $V_{IH} = 2.0 \text{ V}$
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise: V<sub>OLP</sub> = 1.6 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:

Human Body Model > 2000 V; Machine Model > 200 V

- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

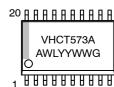


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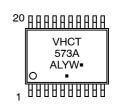
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# MARKING DIAGRAMS









A = Assembly Location

WL, L = Wafer Lot YY, Y = Year WW, W = Work Week G or ■ = Pb-Free Package

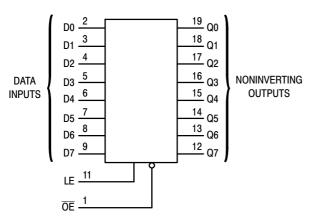
(Note: Microdot may be in either location)

#### **FUNCTION TABLE**

	INPUTS	OUTPUT	
ŌĒ	LE	D	Q
L	H	H	T T
L	H	L	
L	L	X	No Change
H	X		Z

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.





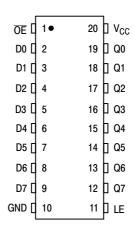


Figure 2. Pin Assignment

# **MAXIMUM RATINGS**

Symbol	Paramete	Parameter		
V <sub>CC</sub>	DC Supply Voltage	DC Supply Voltage		
V <sub>in</sub>	DC Input Voltage		- 0.5 to + 7.0	V
V <sub>out</sub>	DC Output Voltage	Outputs in 3-State High or Low State	- 0.5 to + 7.0 - 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current		- 20	mA
I <sub>OK</sub>	Output Diode Current (V <sub>OUT</sub> < 0	GND; V <sub>OUT</sub> > V <sub>CC</sub> )	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin		± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and G	ND Pins	± 75	mA
P <sub>D</sub>	Power Dissipation in Still Air,	SOIC Package† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature		- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating – SOIC Packages: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	4.5	5.5	٧
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage Outputs in 3-State High or Low State	0 0	5.5 V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	- 40	+ 85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time V <sub>CC</sub> =5.0V ±0.5V	0	20	ns/V

#### DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = - 40 to 85°C		
Symbol	Parameter	Test Conditions	V	Min	Тур	Max	Min	Max	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V <sub>OH</sub>	Minimum High-Level Output	I <sub>OH</sub> = - 50μA	4.5	4.4	4.5		4.4		V
	Voltage $V_{in} = V_{IH}$ or $V_{IL}$	I <sub>OH</sub> = - 8mA	4.5	3.94			3.80		
V <sub>OL</sub>	Maximum Low-Level Output	I <sub>OL</sub> = 50μA	4.5		0.0	0.1		0.1	V
	Voltage $V_{in} = V_{IH}$ or $V_{IL}$	I <sub>OL</sub> = 8mA	4.5			0.36		0.44	
l <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μΑ
l <sub>OZ</sub>	Maximum 3-State Leakage Current	$V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5			± 0.25		± 2.5	μΑ
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0	μΑ
I <sub>CCT</sub>	Quiescent Supply Current	Per Input: V <sub>IN</sub> = 3.4V Other Input: V <sub>CC</sub> or GND	5.5			1.35		1.50	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5V	0			0.5		5.0	μА

# AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$ )

				-	T <sub>A</sub> = 25	°C	T <sub>A</sub> = - 40	) to 85°C	
Symbol	Parameter	Test Conditions		Min	Тур	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, LE to Q	$V_{CC} = 5.0 \pm 0.5 V$	$C_L = 15pF$ $C_L = 50pF$		7.7 8.5	12.3 13.3	1.0 1.0	13.5 14.5	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, D to Q	$V_{CC} = 5.0 \pm 0.5 V$	C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		5.1 5.9	8.5 9.5	1.0 1.0	9.5 10.5	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time, OE to Q	$\begin{aligned} V_{CC} &= 5.0 \pm 0.5 V \\ R_L &= 1 k \Omega \end{aligned}$	$C_L = 15pF$ $C_L = 50pF$		6.3 7.1	10.9 11.9	1.0 1.0	12.5 13.5	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time, OE to Q	$\begin{aligned} V_{CC} &= 5.0 \pm 0.5 V \\ R_L &= 1 k \Omega \end{aligned}$	C <sub>L</sub> = 50pF		8.8	11.2	1.0	12.0	ns
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew	V <sub>CC</sub> = 5.5 ± 0.5V (Note 1)	C <sub>L</sub> = 50pF			1.0		1.0	ns
C <sub>in</sub>	Maximum Input Capacitance				4	10		10	pF
C <sub>out</sub>	Maximum 3-State Output Capacitance (Output in High-Impedance State)				6				pF

		Typical @ 25°C, V <sub>CC</sub> = 5.0V	
$C_{PD}$	Power Dissipation Capacitance (Note 2)	25	pF

# NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}, \ C_L = 50 \ \text{pF}, \ V_{CC} = 5.0 \text{V})$

			T <sub>A</sub> = 25°C		
Symbol	Parameter	Тур	Max	Unit	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	1.2	1.6	٧	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>		-1.6	٧	
V <sub>IHD</sub>	V <sub>IHD</sub> Minimum High Level Dynamic Input Voltage		2.0	٧	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.8	V	

Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PLHn</sub>|.
 C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per latch). C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## **TIMING REQUIREMENTS** (Input $t_r = t_f = 3.0 \text{ns}$ )

			T <sub>A</sub> = 25°C		T <sub>A</sub> = - 40 to 85°C	
Symbol	Parameter	Test Conditions	Тур	Limit	Limit	Unit
t <sub>w(h)</sub>	Minimum Pulse Width, LE	$V_{CC} = 5.0 \pm 0.5 V$		6.5	8.5	ns
t <sub>su</sub>	Minimum Setup Time, D to LE	$V_{CC} = 5.0 \pm 0.5 V$		1.5	1.5	ns
t <sub>h</sub>	Minimum Hold Time, D to LE	$V_{CC} = 5.0 \pm 0.5 V$		3.5	3.5	ns

# **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74VHCT573ADWG	SOIC-20WB (Pb-Free)	38 Units / Rail
MC74VHCT573ADWRG	SOIC-20WB (Pb-Free)	1000 / Tape & Reel
MC74VHCT573ADTG	TSSOP-20*	75 Units / Rail
MC74VHCT573ADTRG	TSSOP-20*	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

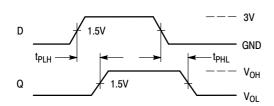


Figure 3. Switching Waveform

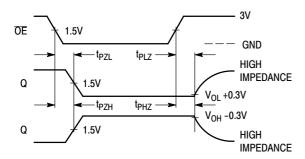


Figure 5. Switching Waveform

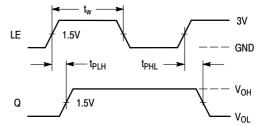


Figure 4. Switching Waveform

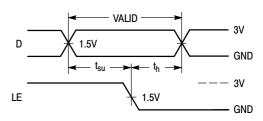
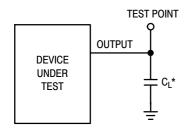
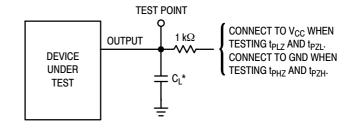


Figure 6. Switching Waveform

<sup>\*</sup>This package is inherently Pb-Free.





\*Includes all probe and jig capacitance

Figure 7. Test Circuit

Figure 8. Test Circuit

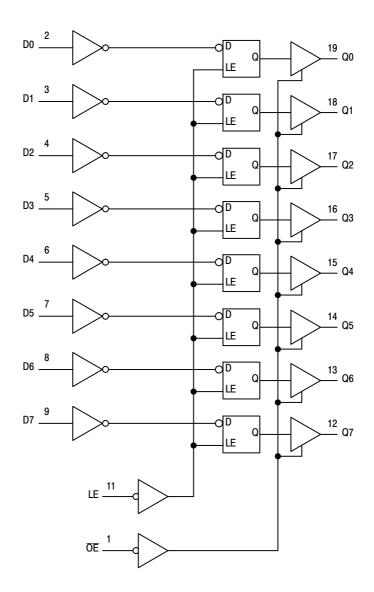
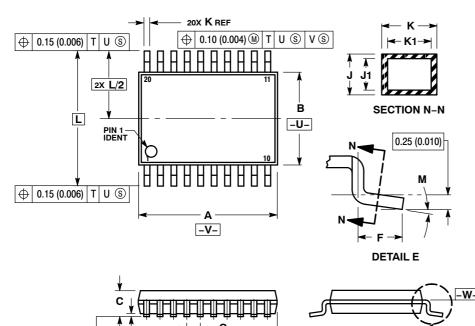


Figure 9. Expanded Logic Diagram

<sup>\*</sup>Includes all probe and jig capacitance

#### PACKAGE DIMENSIONS

TSSOP-20 CASE 948E-02 ISSUE C



0.100 (0.004)

-T- SEATING

#### NOTES:

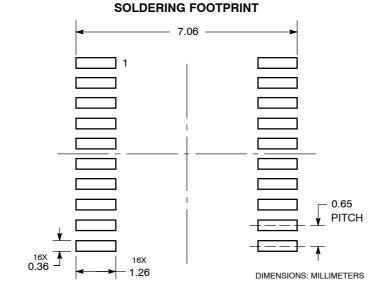
- DTES:

  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION:
  MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE
  MOLD FLASH, PROTRUSIONS OR GATE
  BURRS. MOLD FLASH OR GATE BURRS.
  BUALL NOT EXCEED A 15 (100 DEP. DEP. SIDE.) SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

  4. DIMENSION B DOES NOT INCLUDE
- INTERLEAD FLASH OR PROTRUSION.
  INTERLEAD FLASH OR PROTRUSION
- INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE. 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE —W—

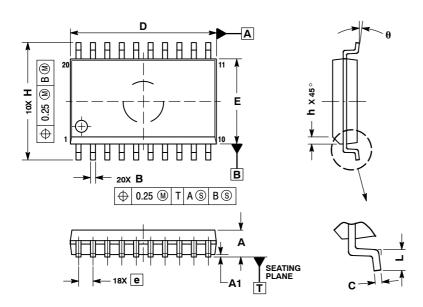
MILLIMETERS   INCHES	BETEINMINED TO BYTOMITE WILL W					
A		MILLIMETERS		INC	HES	
B     4.30     4.50     0.169     0.177       C      1.20      0.047       D     0.05     0.15     0.002     0.006       F     0.50     0.75     0.020     0.30       G     0.65 BSC     0.026 BSC       H     0.27     0.37     0.011     0.015       J     0.09     0.20     0.004     0.008       J1     0.09     0.16     0.004     0.006       K     0.19     0.30     0.007     0.012       K1     0.19     0.25     0.007     0.010	DIM	MIN	MAX	MIN	MAX	
C          1.20          0.047           D         0.05         0.15         0.002         0.006           F         0.50         0.75         0.020         0.030           G         0.65 BSC         0.026 BSC           H         0.27         0.37         0.011         0.015           J         0.09         0.20         0.004         0.008           J1         0.09         0.16         0.004         0.006           K         0.19         0.30         0.007         0.012           K1         0.19         0.25         0.007         0.010	Α	6.40	6.60	0.252	0.260	
D   0.05   0.15   0.002   0.006   F   0.50   0.75   0.020   0.030   G   0.65 BSC   0.026 BSC   D.026	В	4.30	4.50	0.169	0.177	
F         0.50         0.75         0.020         0.030           G         0.65 BSC         0.026 BSC           H         0.27         0.37         0.011         0.015           J         0.09         0.20         0.004         0.008           J1         0.09         0.16         0.004         0.006           K         0.19         0.30         0.007         0.012           K1         0.19         0.25         0.007         0.010	C	-	1.20		0.047	
G 0.65 BSC 0.026 BSC H 0.27 0.37 0.011 0.015 J 0.09 0.20 0.004 0.008 J1 0.09 0.16 0.004 0.006 K 0.19 0.30 0.007 0.012 K1 0.19 0.25 0.007 0.010	D	0.05	0.15	0.002	0.006	
H   0.27   0.37   0.011   0.015   J   0.09   0.20   0.004   0.008   J1   0.09   0.16   0.004   0.006   K   0.19   0.30   0.007   0.012   K1   0.19   0.25   0.007   0.010	F	0.50	0.75	0.020	0.030	
J         0.09         0.20         0.004         0.008           J1         0.09         0.16         0.004         0.006           K         0.19         0.30         0.007         0.012           K1         0.19         0.25         0.007         0.010	G	0.65	BSC	0.026	BSC	
J1         0.09         0.16         0.004         0.006           K         0.19         0.30         0.007         0.012           K1         0.19         0.25         0.007         0.010	Н	0.27	0.37	0.011	0.015	
K         0.19         0.30         0.007         0.012           K1         0.19         0.25         0.007         0.010	J	0.09	0.20	0.004	0.008	
K1 0.19 0.25 0.007 0.010	J1	0.09	0.16	0.004	0.006	
111 0110 01001 01010	K	0.19	0.30	0.007	0.012	
	K1	0.19	0.25	0.007	0.010	
L 6.40 BSC 0.252 BSC	L	6.40	6.40 BSC		BSC	
M 0° 8° 0° 8°	M	0°	8°	0°	8°	



**DETAIL E** 

#### PACKAGE DIMENSIONS

SOIC-20 WB DW SUFFIX CASE 751D-05 ISSUE G



#### NOTES:

- DIMENSIONS ARE IN MILLIMETERS.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE. 5. DIMENSION B DOES NOT INCLUDE DAMBAR
- 5. DIMENSION B DOES NOT INCLUDE DAMBA PROTRUSION, ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION

	MILLIMETERS			
DIM	MIN	MAX		
Α	2.35	2.65		
A1	0.10	0.25		
В	0.35	0.49		
C	0.23	0.32		
D	12.65	12.95		
Е	7.40	7.60		
е	1.27	BSC		
Н	10.05	10.55		
h	0.25	0.75		
L	0.50	0.90		
θ	0 °	7 °		

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