Advance Information

MC92460EC/D
Rev. 1.0, 5/2002

MC92460 HDLC Controller
Hardware Specifications

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This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MC92460 Multichannel HDLC Controller.

The following topics are addressed:

Figure 1 shows a block diagram of the MC92460.

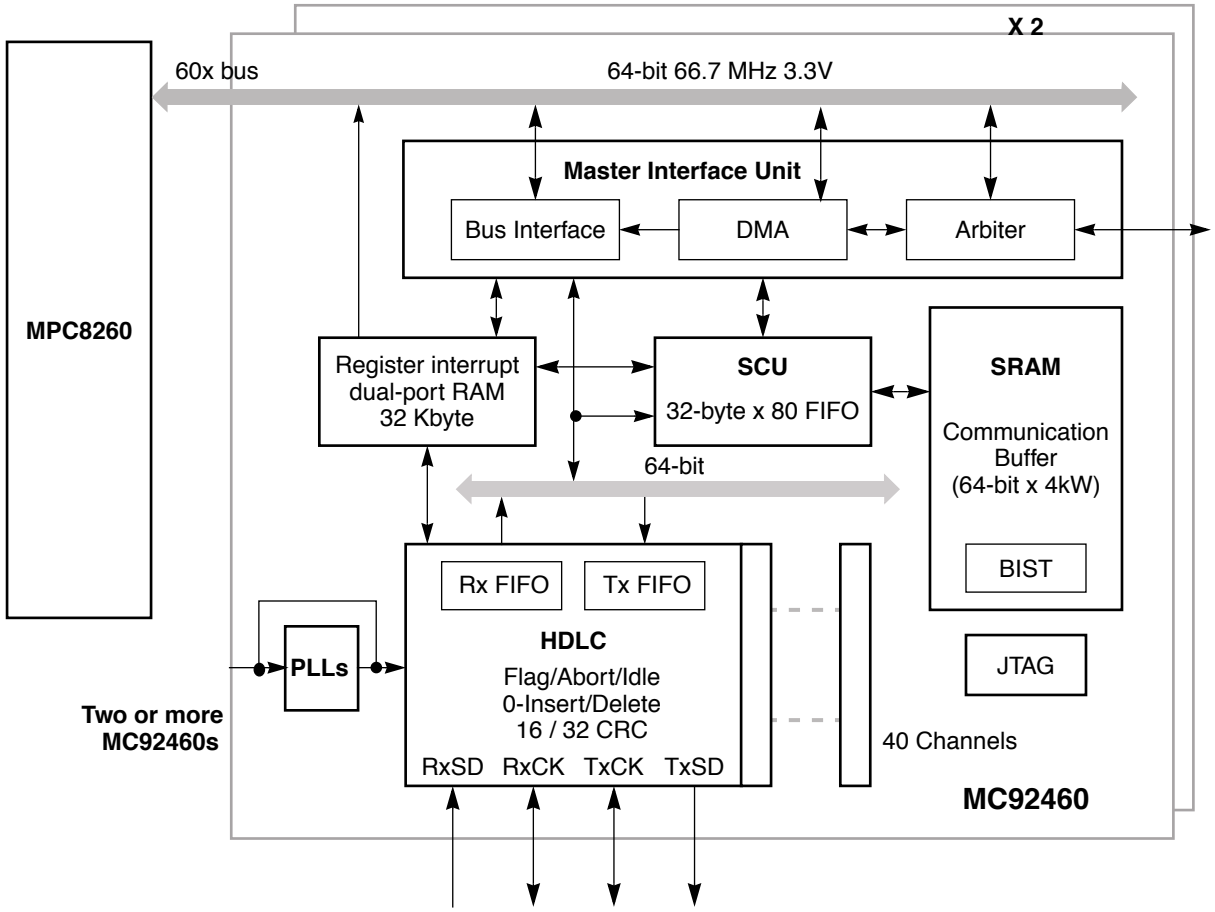

Figure 1. MC92460 Block Diagram

1.1 Features

The following is an overview of the MC92460 feature set:

- Channels
  - — 40 full-duplex HDLC channels
  - — Programmable channel assignment (any logical channel to any signal)
  - — Each channel has a default of 64 buffer descriptors (Rx and Tx) but the number of buffer descriptors per channel is configurable
- Controllers
  - — Maximum throughput of 1919 Mbps; individual controllers operate up to 66.7 Mbps
  - — All communication controllers operate asynchronously
  - — Programmable frame size (maximum 65,535 bytes)
  - — Transparent memory access with internal memory controller
- 60x Bus
  - — MC92460 directly connects with a 64-bit data and 32-bit address 60x bus
  - — Supports 66.7 MHz 60x bus speed, with aggregate bandwidth of up to 1919 Mbps depending

on the type of main memory used
  - Up to four MC92460's may be connected in parallel on the 60x bus
  - Bus supports multiple master design
- Communication Buffers
  - Data Buffer
    - 256 Kbits on-chip memory for data buffers
    - 256 Kbit communication buffer can store up to 819 bytes per frame.
    - 80 channel virtual DMA functionality executes between off-chip memory and the communication buffer
  - BD Buffer
    - 32 Kbyte on-chip dual-port RAM for buffer descriptors
    - A total of 4096 buffer descriptors (2048 TxBD and 2048 RxBD)
- JTAG Support
  - Supports the IEEE1149.1 JTAG controller standard
- Power and Clocks
  - Supports single-beat and burst accesses
  - On-chip PLL for baud rate generator (maximum of 66.7 MHz)
  - Separate power supplies for core internal logic (1.8V) and for I/O (3.3V)
- Package
  - 480 pin TPGA, 1.27 mm pitch

1.2 Electrical and Thermal Characteristics

This section provides AC and DC electical specifications and thermal characteristics for the MC92460.

1.2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MC92460. Table 1 shows the maximum electrical ratings.

Table 1. Maximum Temperatures and Voltages

Rating	Symbol	Value Name	Unit
Core supply voltage	VDD	-0.3 – 2.5	V
I/O supply voltage	VDDH	-0.3 – 3.6	V
Input voltage	VIN	GND-0.3 – 3.6	V
Junction temperature	Tj	120	^{o}C
Storage temperature range	T_{STG}	-55 – 150	^{o}C
Ambient temperature	T_A	-40 – 85	^{o}C

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	VDD	1.65 – 1.95	V
I/O supply voltage	VDDH	3.15 – 3.465	V
Input voltage	VIN	GND -0.3 – 3.6	V
Junction temperature	Tj	105	^{o}C

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics

TA=0 to 85°C; VDD=2.0±5% Vdc; VDDH=3.3±5% Vdc; GND=0Vdc; Load Capacitance < 10pF

Characteristics	Conditions	Symbol	Min	Max	Unit
Input high voltage		V_{IH}	2.0	3.465	V
Input low voltage		V_{IL}	GND	0.8	V
Input leakage current	V_{IN}=VDDH	I_{IN}	–	10	uA
HI-Z leakage current	V_{IN}=VDDH, GND	I_{OZ}	–10	+10	uA
Signal low input current	V_{IL}=0.8V	I_{IL}	–	60	uA
Signal high input current	V_{IH}=2.0V	I_{IH}	–	60	uA
Output high voltage	I_{OH}=-7.0mA	V_{OH}	2.4	-	V

Table 3. DC Electrical Characteristics (continued)

TA=0 to 85°C; VDD=2.0±5% Vdc; VDDH=3.3±5% Vdc; GND=0Vdc; Load Capacitance < 10pF

Output low voltage • BR • BG • ABB • TS • A[0-31] • AP[0-3] • APE • TT[0-4] • TBST • TSIZ[0-2] • GBL • CI • WT • LBCLAIM • BTO • INT • TC[0-1] • AACK • ARTRY • DBG • DBWO • DBB • DH[0-31],DL[0-31] • DP[0-7] • DPE • DBDIS • TA • DRTRY • TEA	I_{OL}=7.0mA	V_{OL}		0.4	V
Output low voltage • Rx CLK[0-39] • Tx CLK[0-39] • Tx SD[0-39] • TDO • SBG • SDBG • SBR • SIRQ • CS0 • CS1 • CS2	I_{OL}=5.0mA	V_{OL}		0.4	V

1.2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Maximum Temperatures and Voltages

Characteristics	Symbol	Thermal Resistance Value	Unit	Air Flow
Thermal resistance for 480 TBGA	θ_{JA}	10.48	°C/W	0 LFM
		8.61	°C/W	100 LFM
		7.78	°C/W	200 LFM
		6.89	°C/W	400 LFM
		5.52	°C/W	800 LFM

LFM = Linear Feet per Minute

1.2.3 Power Considerations

The average chip-junction temperature, Tj, can be obtained from the following:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where

θ_{JA} = package thermal resistance, junction to ambient, °C/W

T_A = ambient temperature, °C

Power equations are the following:

$P_D = P_{VDD} + P_{VDDH}$ = chip total power dissipation, W

$P_{VDD} = I_{VDD} \times VDD$ = chip core power, W

$P_{VDDH} = I_{VDDH} \times VDDH$

= user-determined power dissipation on input/output pins, W

1.2.4 Power Dissipation

Table 5 describes maximum chip core power dissipation.

Table 5. Maximum Core Power Dissipation (P_{VDD})

VDD(V)	SYSCLK Frequency (MHz)	I_{VDD} (mA)	P_{VDD} (mW)	P_{VDDH}(mW)
1.95	66.7	650	980	920

1.2.5 AC Specifications

These AC specifications are target specifications.

1.2.5.1 SYSCLK Timing

Table 6 shows the system clock timing.

Table 6. Clock Timing

Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	60.0	66.7	MHz
Clock period		15.0	16.7	nS
Clock pulse width	t_{CL},t_{CH}	7	8	nS
SYSCLK input high voltage	V_{IHC}	2.4	3.465	V
SYSCLK input low voltage	V_{ILC}	GND	0.4	V
SYSCLK Jitter			±200	pS

Figure 2 shows the SYSCLK.

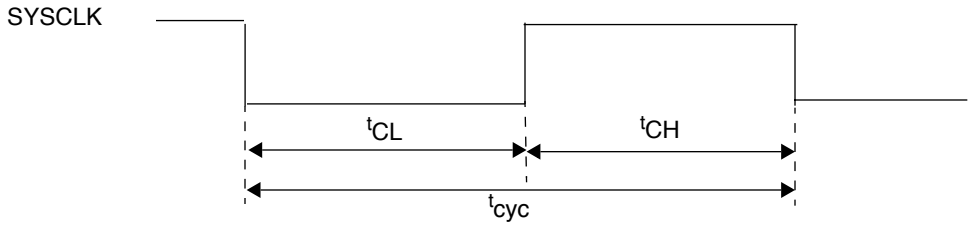

Figure 2. SYSCLK

1.2.5.2 EXCLK Timing

Table 7 shows the external clock timing.

Table 7. Clock Timing

Characteristics	Symbol	Min	Max	Unit
Operation Frequency	f	14.0	16.0	MHz
Clock duty		40	60	%
Clock Pulse width	t_{CL},t_{CH}	25	42.8	nS
EXCLK input high voltage	V_{IHC}	2.4	3.465	V
EXCLK input low voltage	V_{ILC}	GND	0.4	V
EXCLK Jitter			±200	pS

Figure 3 shows the EXCLK.

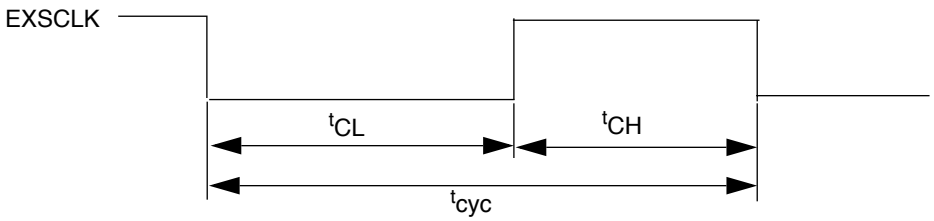

Figure 3. EXCLK

1.2.5.3 AC Timing

Figure 4 shows the HDLC external clock with polarity not inverted. All time specifications were measured at expected load capacitance C_L=8pF.

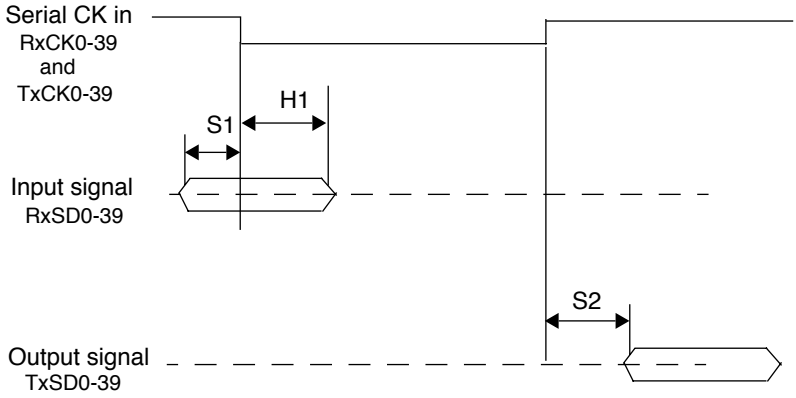

Figure 4. HDLC External Clock

Figure 5 shows an HDLC internal clock (TxCK/RxCK output mode) whose polarity is not inverted.

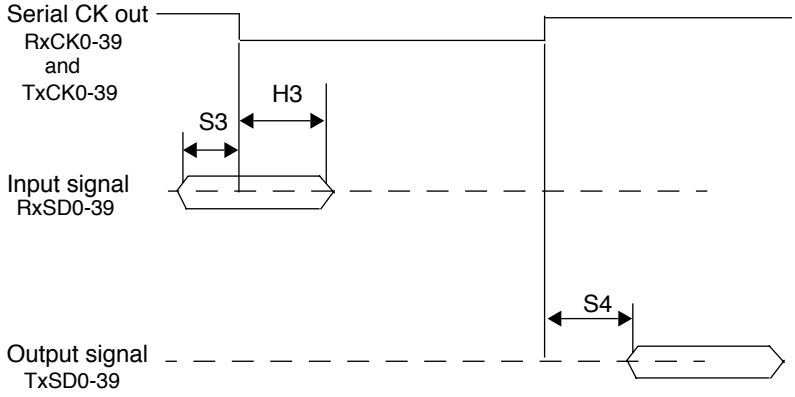

Figure 5. HDLC Internal Clock

Table 8 shows the AC electrical characteristics. The frequency is 20 MHz.

Table 8. AC Electrical Characteristics

Spec Num	Characteristic	Min	Max	Unit
S1	HDLC input- external clock setup time	2		nS
H1	HDLC input -external clock hold time	1		nS
S2	HDLC output- external clock setup time		14	nS
S3	HDLC input- internal clock setup time	12		nS
H3	HDLC input- internal clock hold time	0		nS
S4	HDLC output- internal clock setup time		4	nS

Figure 6 shows the interaction of several bus signals.

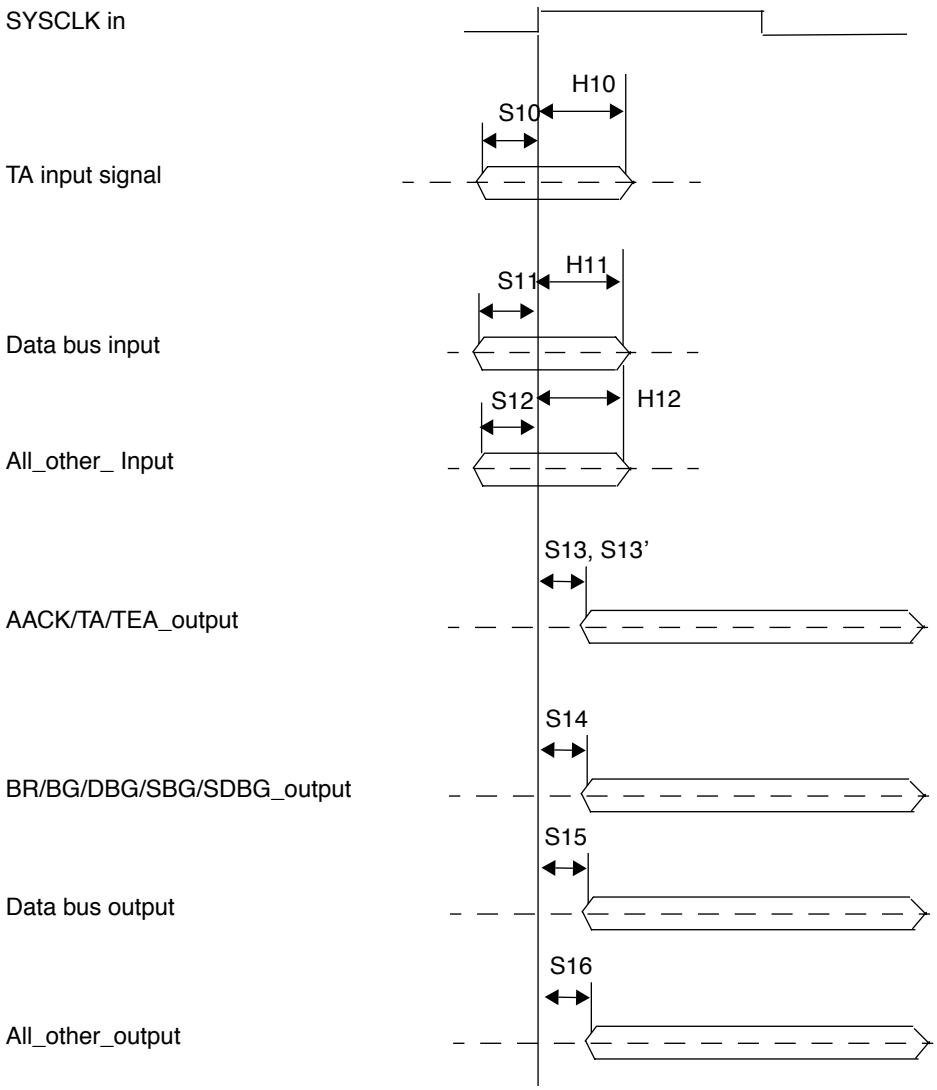

Figure 6. Bus Signals

Table 9 shows the bus signal I/O characteristics. The frequency is 20 MHz.

Table 9. Bus Input/Output Characteristics

Spec Num	Characteristic	Min	Max	Unit
S10	TA/TEA input	6		nS
H10	TA/TEA input		1	nS
S11	Data bus input signals	7		nS
H11	Data bus input signals		1	nS
S12	All other input signals	7		nS
H12	All other input signals		1	nS
S13	AACK/TEA output	1	7	nS
S13’	TA output	1	8.5	nS
S14	BR/BG/DBG/SBG/SDBG output	1	7	nS
S15	Data bus output signals	1	8.5	nS
S16	All other output signals	1	7	nS

1.3 Pinout

Table 10. Pin Assignments

Ball	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ball
A	PowVdd26	PowVdd28	PowVdd36	scan_out_e	PowGnd23	CoreGnd23	PowGnd24	D9	CoreVdd23	D57	D32	D42	D11	D35	D59	CoreVdd17	D28	D52	D21	D45	D61	PowGnd33	D54	CoreGnd19	D31	DP4	PowVdd29	PowVdd7	PowVdd5	A
B	PowVdd27	PowVdd25	TEST0	scan_out_k	CoreGnd15	CS1	scan_out_h	D1	D25	CoreGnd16	D10	PowGnd27	D3	PowGnd28	CoreGnd17	D20	PowGnd30	D60	DP7	PowGnd32	D6	D30	D62	D23	D39	D55	DP5	PowVdd4	PowVdd6	B
C	PowVdd35	TEST2	PowVdd24	PowGnd22	scan_out_j	CoreVdd15	scan_out_g	D56	PowGnd25	D49	CoreVdd16	D34	D58	CoreVdd24	PowGnd29	D4	D36	D5	D29	D53	D14	CoreGnd25	PowGnd34	CoreVdd25	D47	D8	PowVdd3	DP1	PowVdd30	C
D	$\overline{SEN}$	$\overline{POR}$	SMODE0	PowVdd23	scan_out_e	CSA2	scan_out_f	D48	D17	D41	D2	D26	CoreGnd24	D27	D43	D40	D44	PowGnd31	CoreGnd18	CoreVdd18	D22	D46	D15	PowGnd35	D0	PowVdd2	DP0	DP2	DP3	D
E	CSA5	CSA3	TEST3	SMODE1	PowVdd22	CS2	CS0	D24	D16	D33	PowGnd26	D18	D50	D19	D51	D12	scan_out_i	D13	D37	DP6	D38	D7	CoreVdd19	D63	PowVdd1	$\overline{TA}$	TSIZ0	PowGnd0	CoreGnd0	E
F	CSA1	PowGnd21	$\overline{DBWO}$	scan_out_d	AMODE																				$\overline{TBST}$	TSIZ1	$\overline{DBG}$	$\overline{TS}$	CoreVdd0	F
G	PCMD	TEST1	$\overline{DBDIS}$	CoreGnd14	CoreVdd14																				TSIZ2	$\overline{G\_DBG}$	$\overline{ABB}$	$\overline{AACK}$	$\overline{ARTRY}$	G
H	TCK	$\overline{TRST}$	TDI	$\overline{HRESET}$	CSA0																				$\overline{BG}$	PowGnd1	TT0	$\overline{DPE}$	TT2	H
J	PLL2O	ACoreVdd2	EXCLK	TDO	TMS																				TT1	TT3	TT4	$\overline{SDBG}$	PowGnd2	J
K	scan_out_c	RxSD39	CoreVdd13	RxCK39	ACoreGnd2																				$\overline{DBB}$	A0	CoreGnd1	A1	$\overline{SBG}$	K
L	RxSD38	RxCK38	TxSD39	CoreGnd13	TxCK39																				A2	A3	CoreVdd1	A4	PowGnd3	L
M	RxSD37	RxCK37	TxSD38	PowGnd20	TxCK38																				A5	A6	$\overline{BR}$	A7	A8	M
N	TxCK36	RxSD36	RxCK36	TxSD37	TxCK37																				A9	PowGnd4	A10	A11	$\overline{SBR}$	N
P	CoreVdd12	TxSD36	TxCK35	RxSD35	RxCK35																				A13	A14	PowGnd5	A12	A15	P
R	TxSD35	CoreGnd12	scan_out_b	RxSD34	RxCK34																				CoreGnd20	A16	A17	CoreGnd2	CoreVdd2	R
T	TxCK34	RxSD33	TxSD34	PowGnd19	RxCK33																				A20	PowGnd6	A19	A21	A18	T
U	TxCK33	TxSD33	RxCK32	RxSD32	TxCK32																				PowGnd7	A24	A23	CoreVdd20	A22	U
V	TxSD32	RxCK31	RxSD31	TxCK31	TxSD31																				$\overline{TEA}$	A28	A27	A26	A25	V
W	RxCK30	scan_out_a	RxSD30	CoreVdd11	TxCK30																				CoreGnd3	A31	PowGnd8	A30	A29	W
Y	CoreGnd11	TxSD30	PowGnd18	RxCK29	TxCK29																				$\overline{DRTRY}$	$\overline{LBCLAIM}$	$\overline{SIRQ}$	CoreVdd3	$\overline{INT}$	Y
AA	RxSD29	TxSD29	RxCK28	RxSD28	RxCK27																				AP3	PowGnd9	AP0	CSA6	BTO	AA
AB	TxCK28	TxSD28	RxSD27	TxCK27	scan_in_k																				$\overline{CI}$	$\overline{WT}$	$\overline{APE}$	AP2	AP1	AB
AC	TxSD27	RxCK26	RxSD26	CoreVdd10	CoreGnd10																				TC0	$\overline{GBL}$	MODE	PowGnd10	CSA4	AC
AD	TxCK26	PowGnd17	TxSD26	TxCK25	TxCK24																				PLL1O	TxCK0	CoreGnd4	TC1	CSA7	AD
AE	RxCK25	RxSD25	TxSD25	TxSD24	PowVdd15	RxSD22	CoreVdd9	RxSD20	TxSD19	PowGnd15	RxCK16	RxCK15	RxSD14	RxSD13	TxCK12	TxSD11	PowGnd13	RxCK8	RxCK7	RxSD6	RxSD5	TxSD4	CoreGnd5	PowGnd11	PowVdd8	RxSD0	ACoreVdd1	SYSCLK	CoreVdd4	AE
AF	RxSD24	RxCK24	RxCK23	PowVdd16	RxCK22	PowGnd16	TxSD21	RxSD19	CoreVdd22	RxSD17	CoreGnd8	RxSD15	CoreGnd22	TxCK13	CoreGnd7	TxCK11	TxSD10	TxSD9	CoreVdd6	TxSD7	TxSD6	TxSD5	RxSD3	RxSD2	RxCK1	PowVdd9	RxCK0	ACoreGnd1	TxSD0	AF
AG	PowVdd34	RxSD23	PowVdd17	TxSD23	TxSD22	CoreGnd9	TxCK20	TxCK19	TxCK18	TxCK17	RxSD16	TxCK15	TxCK14	TxSD13	RxSD12	RxSD11	TxCK10	TxCK9	TxSD8	TxCK7	TxCK6	TxCK5	TxCK4	CoreVdd5	CSA8	RxSD1	PowVdd10	TxSD1	PowVdd31	AG
AH	PowVdd21	PowVdd18	TxCK23	TxCK22	RxCK21	TxCK21	TxSD20	RxCK18	TxSD18	CoreVdd8	TxCK16	TxSD15	TxSD14	RxCK13	TxSD12	RxCK10	CoreVdd21	RxSD9	TxCK8	CoreGnd6	CoreGnd21	RxCK5	RxSD4	TxCK3	RxCK2	TxCK2	TxCK1	PowVdd11	PowVdd13	AH
AJ	PowVdd19	PowVdd20	PowVdd33	scan_in_j	RxSD21	RxCK20	RxCK19	RxSD18	RxCK17	TxSD17	TxSD16	RxCK14	PowGnd14	RxCK12	CoreVdd7	RxCK11	RxSD10	RxCK9	RxSD8	RxSD7	RxCK6	PowGnd12	RxCK4	RxCK3	TxSD3	TxSD2	PowVdd32	PowVdd14	PowVdd12	AJ
	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ball

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