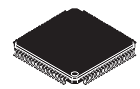
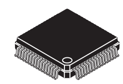
Document Number: MCF51AC256
Rev.7, 9/2011

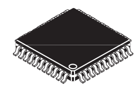
MCF51AC256 Series ColdFire Microcontroller

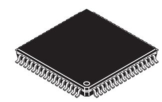
**Covers: MCF51AC256A
MCF51AC256B
MCF51AC128A
MCF51AC128C**

MCF51AC256


80 LQFP
14 mm × 14 mm


64 LQFP
10 mm × 10 mm


44 LQFP
10 mm × 10 mm


64 QFP
14 mm × 14 mm

The MCF51AC256 series are members of the ColdFire® family of 32-bit variable-length reduced instruction set (RISC) microcontroller. This document provides an overview of the MCF51AC256 series, focusing on its highly integrated and diverse feature set.

The MCF51AC256 series are based on the V1 ColdFire core and operates at processor core speeds up to 50.33 MHz. As part of Freescale's Controller Continuum®, it is an ideal upgrade for designs based on the MC9S08AC128 series of 8-bit microcontrollers.

The MCF51AC256 features the following functional units:

- V1 ColdFire core with background debug module
- Up to 256 KB of flash memory
- Up to 32 KB of static RAM (SRAM)
- Up to two analog comparators (ACMP)
- Analog-to-digital converter (ADC) with up to 24 channels
- Controller-area network (CAN)
- Cyclic redundancy check (CRC)
- Inter-integrated circuit (IIC)
- Keyboard interrupt (KBI)
- Multipurpose clock generator (MCG)
- Rapid general-purpose input/output (RGPIO)
- Two serial communications interfaces (SCI)
- Up to two serial peripheral interfaces (SPI)
- Two flexible timer modules (FTM)
- Timer pulse-width modulator (TPM)

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

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1 MCF51AC256 Family Configurations

1.1 Device Comparison

The MCF51AC256 series is summarized in Table 1.

Table 1. MCF51AC256 Series Device Comparison

<table>
<tr><th rowspan="2">Feature</th><th colspan="2">MCF51AC256A</th><th colspan="3">MCF51AC256B</th><th colspan="2">MCF51AC128A</th><th colspan="3">MCF51AC128C</th></tr>
<tr><th>80-pin</th><th>64-pin</th><th>80-pin</th><th>64-pin</th><th>44-pin</th><th>80-pin</th><th>64-pin</th><th>80-pin</th><th>64-pin</th><th>44-pin</th></tr>
<tr><td>Flash memory size (Kbytes)</td><td colspan="5">256</td><td colspan="5">128</td></tr>
<tr><td>RAM size (Kbytes)</td><td colspan="5">32</td><td colspan="5">32 or 16[1]</td></tr>
<tr><td>V1 ColdFire core with BDM (background debug module)</td><td colspan="10">Yes</td></tr>
<tr><td>ACMP1 (analog comparator)</td><td colspan="10">Yes</td></tr>
<tr><td>ACMP2 (analog comparator)</td><td colspan="2">Yes</td><td colspan="2">Yes</td><td>No</td><td colspan="4">Yes</td><td>No</td></tr>
<tr><td>ADC (analog-to-digital converter) channels (12-bit)</td><td>24</td><td>20</td><td>24</td><td>20</td><td>9</td><td>24</td><td>20</td><td>24</td><td>20</td><td>9</td></tr>
<tr><td>CAN (controller area network)</td><td colspan="2">Yes</td><td colspan="3">No</td><td colspan="2">Yes</td><td colspan="3">No</td></tr>
<tr><td>COP (computer operating properly)</td><td colspan="10">Yes</td></tr>
<tr><td>CRC (cyclic redundancy check)</td><td colspan="10">Yes</td></tr>
<tr><td>RTI</td><td colspan="10">Yes</td></tr>
<tr><td>DBG (debug)</td><td colspan="10">Yes</td></tr>
<tr><td>IIC1 (inter-integrated circuit)</td><td colspan="10">Yes</td></tr>
<tr><td>IRQ (interrupt request input)</td><td colspan="10">Yes</td></tr>
<tr><td>INTC (interrupt controller)</td><td colspan="10">Yes</td></tr>
<tr><td>KBI (keyboard interrupts)</td><td colspan="10">Yes</td></tr>
<tr><td>LVD (low-voltage detector)</td><td colspan="10">Yes</td></tr>
<tr><td>MCG (multipurpose clock generator)</td><td colspan="10">Yes</td></tr>
<tr><td>OSC (crystal oscillator)</td><td colspan="10">Yes</td></tr>
<tr><td>Port I/O[2]</td><td>69</td><td>54</td><td>69</td><td>54</td><td>36</td><td>69</td><td>54</td><td>69</td><td>54</td><td>36</td></tr>
<tr><td>RGPIO (rapid general-purpose I/O)</td><td colspan="4">16</td><td>12</td><td colspan="4">16</td><td>12</td></tr>
<tr><td>SCI1, SCI2 (serial communications interfaces)</td><td colspan="10">Yes</td></tr>
<tr><td>SPI1 (serial peripheral interface)</td><td colspan="10">Yes</td></tr>
<tr><td>SPI2 (serial peripheral interface)</td><td>Yes</td><td>No</td><td>Yes</td><td colspan="2">No</td><td>Yes</td><td>No</td><td>Yes</td><td colspan="2">No</td></tr>
<tr><td>FTM1 (flexible timer module) channels</td><td colspan="4">6</td><td>4</td><td colspan="4">6</td><td>4</td></tr>
<tr><td>FTM2 channels</td><td>6</td><td>2</td><td>6</td><td>2</td><td>2</td><td>6</td><td>2</td><td>6</td><td>2</td><td>2</td></tr>
</table>

Table 1. MCF51AC256 Series Device Comparison (continued)

Feature	MCF51AC256A		MCF51AC256B			MCF51AC128A		MCF51AC128C		
	80-pin	64-pin	80-pin	64-pin	44-pin	80-pin	64-pin	80-pin	64-pin	44-pin
TPM3 (timer pulse-width modulator) channels	2									
VBUS (debug visibility bus)	Yes	No	Yes	No		Yes	No	Yes	No	

1 The members of MCF51AC128A with CAN support have 32 KB RAM. The other members have 16 KB RAM.

2 Up to 16 pins on Ports E and F are shared with the ColdFire Rapid GPIO module.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51AC256 series pins and modules.

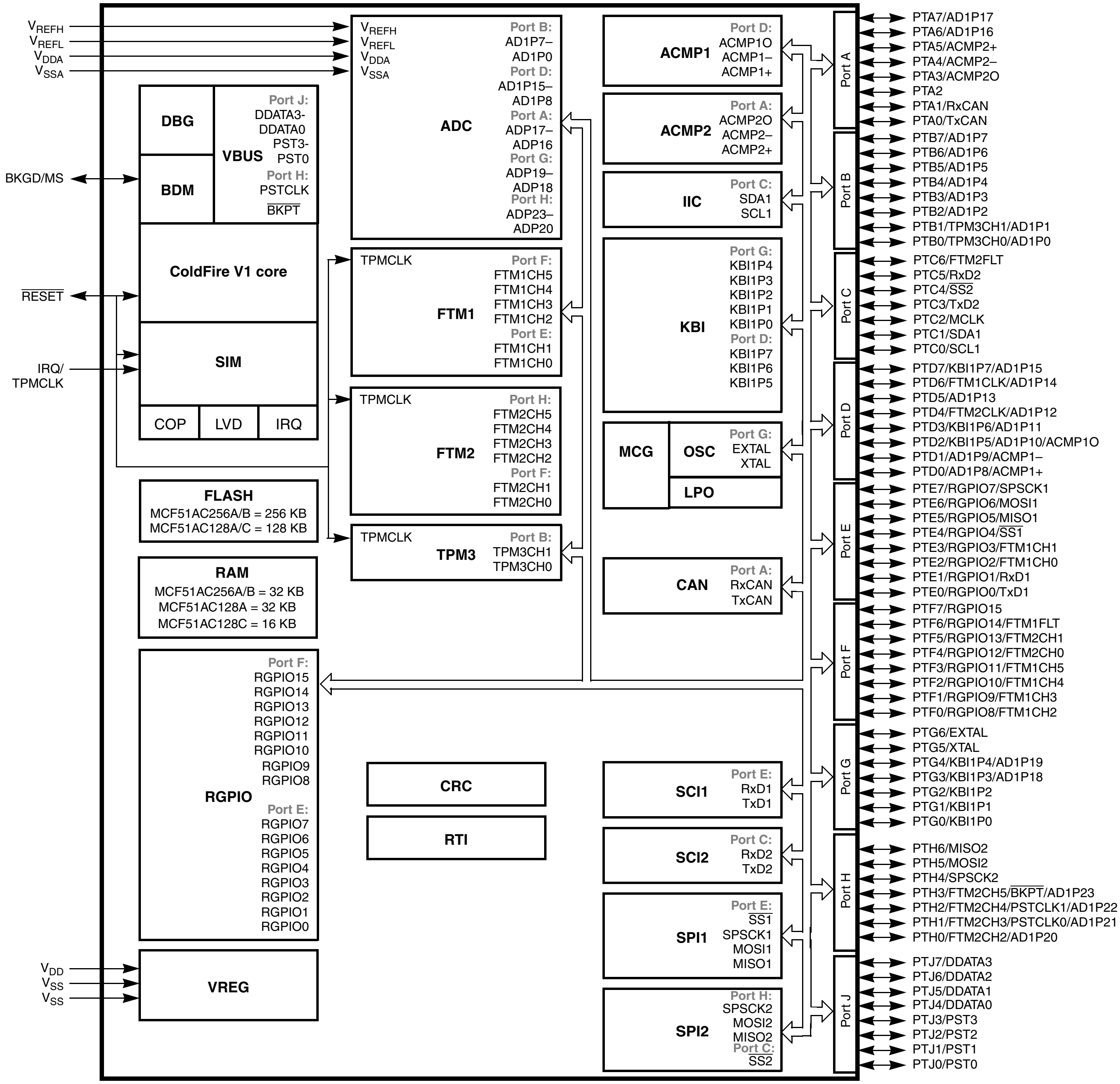


Figure 1. MCF51AC256 Series Block Diagram

1.3 Features

Table 2 describes the functional units of the MCF51AC256 series.

Table 2. MCF51AC256 Series Functional Units

Functional Unit	Function
CF1 Core (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
VBUS (debug visibility bus)	Allows for real-time program traces (part of the V1 ColdFire core)
SIM (system integration module)	Controls resets and chip level interfaces between modules
Flash (flash memory)	Provides storage for program code, constants and variables
RAM (random-access memory)	Provides storage for program variables
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management across the device
COP (computer operating properly)	Monitors a countdown timer and generates a reset if the timer is not regularly reset by the software
LVD (low-voltage detect)	Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
FTM1, FTM2 (flexible timer/pulse-width modulators)	Provides a variety of timing-based features
TPM3 (timer/pulse-width modulator)	Provides a variety of timing-based features
CRC (cyclic redundancy check)	Accelerates computation of CRC values for ranges of memory
ACMP1, ACMP2 (analog comparators)	Compares two analog inputs
IIC (inter-integrated circuit)	Supports standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
OSC (crystal oscillator)	Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the PLL or FLL
LPO (low-power oscillator)	Provides a second clock source for COP and RTI.
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SPI1 (8-bit serial peripheral interfaces)	Provides 8-bit 4-pin synchronous serial interface
SPI2 (16-bit serial peripheral interfaces)	Provides 16-bit 4-pin synchronous serial interface with FIFO

1.3.1 Feature List

- 32-bit Version 1 ColdFire® central processor unit (CPU)
  - Up to 50.33 MHz at 2.7 V – 5.5 V
  - Provide 0.94 Dhrystone 2.1 DMIPS per MHz performance when running from internal RAM (0.76 DMIPS per MHz when running from flash)
  - Implements instruction set revision C (ISA_C)
- On-chip memory
  - Up to 256 KB flash memory read/program/erase over full operating voltage and temperature
  - Up to 32 KB static random access memory (SRAM)
  - Security circuitry to prevent unauthorized access to SRAM and flash contents
- Power-Saving Modes
  - Three low-power stop plus wait modes
  - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
- System protection features
  - Watchdog computer operating properly (COP) reset with options to run from independent LPO clock or bus clock
  - Low-voltage detection with reset or interrupt
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Debug support
  - Single-wire background debug interface
  - Real-time debug support, with 6 hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into a 1- or 2-level trigger
  - On-chip trace buffer provides programmable start/stop recording conditions plus support for continuous or PC-profiling modes
  - Support for real-time program (and optional partial data) trace using the debug visibility bus
- V1 ColdFire interrupt controller (CF1_INTC)
  - Support of 40 peripheral I/O interrupt requests plus seven software (one per level) interrupt requests
  - Fixed association between interrupt request source and level plus priority, up to two requests can be remapped to the highest maskable level + priority
  - Unique vector number for each interrupt source
  - Support for service routine interrupt acknowledge (software IACK) read cycles for improved system performance
- Multipurpose clock generator (MCG)
  - Oscillator (XOSC); loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - LPO clock as an optional independent clock source for COP and RTI
  - FLL/PLL controlled by internal or external reference

- — Trimmable internal reference allows 0.2% resolution and 2% deviation
- Analog-to-digital converter (ADC)
  - — 24 analog inputs with 12 bits resolution
  - — Output formatted in 12-, 10- or 8-bit right-justified format
  - — Single or continuous conversion (automatic return to idle after single conversion)
  - — Operation in low-power modes for lower noise operation
  - — Asynchronous clock source for lower noise operation
  - — Automatic compare with interrupt for less-than, or greater-than or equal-to, programmable value
  - — On-chip temperature sensor
- Flexible timer/pulse-width modulators (FTM)
  - — 16-bit Free-running counter or a counter with initial and final value. The counting can be up and unsigned, up and signed, or up-down and unsigned
  - — Up to 6 channels, and each channel can be configured for input capture, output compare or edge-aligned PWM mode, all channels can be configured for center-aligned PWM mode
    - – Channels can operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs)
    - – Each pair of channels can be combined to generate a PWM signal (with independent control of both edges of PWM signal)
    - – Deadtime insertion is available for each complementary pair
  - — The load of the FTM registers which have write buffer can be synchronized; write protection for critical registers
  - — Generation of the triggers to ADC (hardware trigger)
  - — A fault input for global fault control
  - — Backwards compatible with TPM
- Timer/pulse width modulator (TPM)
  - — 16-bit free-running or modulo up/down count operation
  - — Two channels, each channel may be input capture, output compare, or edge-aligned PWM
  - — One interrupt per channel plus terminal count interrupt
- Cyclic redundancy check (CRC) generator
  - — High speed hardware CRC generator circuit using 16-bit shift register
  - — CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial
  - — Error detection for all single, double, odd, and most multi-bit errors
  - — Programmable initial seed value
- Analog comparators (ACMP)
  - — Full rail to rail supply operation
  - — Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
  - — Option to compare to fixed internal bandgap reference voltage
  - — Option to allow comparator output to be visible on a pin, ACMPxO

- Inter-integrated circuit (IIC)
  - — Compatible with IIC bus standard
  - — Multi-master operation
  - — Software programmable for one of 64 different serial clock frequencies
  - — Interrupt driven byte-by-byte data transfer
  - — Arbitration lost interrupt with automatic mode switching from master to slave
  - — Calling address identification interrupt
  - — Bus busy detection
  - — 10-bit address extension
- Controller area network (CAN)
  - — Implementation of the CAN protocol — Version 2.0A/B
    - – Standard and extended data frames
    - – Zero to eight bytes data length
    - – Programmable bit rate up to 1 Mbps
    - – Support for remote frames
  - — Five receive buffers with FIFO storage scheme
  - — Three transmit buffers with internal prioritization using a “local priority” concept
  - — Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, four 16-bit filters, or eight 8-bit filters
  - — Programmable wakeup functionality with integrated low-pass filter
  - — Programmable loopback mode supports self-test operation
  - — Programmable listen-only mode for monitoring of CAN bus
  - — Programmable bus-off recovery functionality
  - — Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
  - — Internal timer for time-stamping of received and transmitted messages
- Serial communications interfaces (SCI)
  - — Full-duplex, standard non-return-to-zero (NRZ) format
  - — Double-buffered transmitter and receiver with separate enables
  - — Programmable baud rates (13-bit modulo divider)
  - — Interrupt-driven or polled operation
  - — Hardware parity generation and checking
  - — Programmable 8-bit or 9-bit character length
  - — Receiver wakeup by idle-line or address-mark
  - — Optional 13-bit break character generation / 11-bit break character detection
  - — Selectable transmitter output polarity
- Serial peripheral interfaces (SPI)
  - — Master or slave mode operation
  - — Full-duplex or single-wire bidirectional option
  - — Programmable transmit bit rate

- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting
- 16-bit and FIFO operations in SPI2

• Input/Output
- 69 GPIOs
- 8 keyboard interrupt pins with selectable polarity
- Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins
- 16-bits Rapid GPIO pins connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

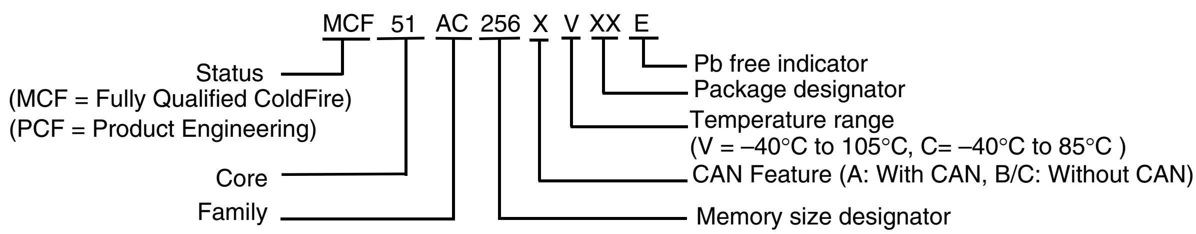


Table 3. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51AC256AVFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	–40°C to 105°C
MCF51AC256BVFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	–40°C to 105°C
MCF51AC256AVLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	–40°C to 105°C
MCF51AC256BVLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	–40°C to 105°C
MCF51AC256AVPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 105°C
MCF51AC256BVPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 105°C
MCF51AC128AVFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 105°C
MCF51AC128CVFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 105°C
MCF51AC128AVLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 105°C
MCF51AC128CVLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 105°C
MCF51AC128AVPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 105°C
MCF51AC128CVPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 105°C
MCF51AC256ACFUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 QFP	–40°C to 85°C
MCF51AC256BCFUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 QFP	–40°C to 85°C
MCF51AC256ACLKE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	80 LQFP	–40°C to 85°C
MCF51AC256BCLKE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	80 LQFP	–40°C to 85°C

Table 3. Orderable Part Number Summary

MCF51AC256ACPUE	MCF51AC256 ColdFire Microcontroller with CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCPUE	MCF51AC256 ColdFire Microcontroller without CAN	256 / 32	64 LQFP	–40°C to 85°C
MCF51AC256BCFGE	MCF51AC256 ColdFire Microcontroller without CAN	256/32	44 LQFP	–40°C to 85°C
MCF51AC128ACFUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 QFP	–40°C to 85°C
MCF51AC128CCFUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 QFP	–40°C to 85°C
MCF51AC128ACLKE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	80 LQFP	–40°C to 85°C
MCF51AC128CCLKE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	80 LQFP	–40°C to 85°CC
MCF51AC128ACPUE	MCF51AC128 ColdFire Microcontroller with CAN	128 / 32	64 LQFP	–40°C to 85°C
MCF51AC128CCPUE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	64 LQFP	–40°C to 85°C
MCF51AC128CCFGE	MCF51AC128 ColdFire Microcontroller without CAN	128 / 16	44 LQFP	–40°C to 85°C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

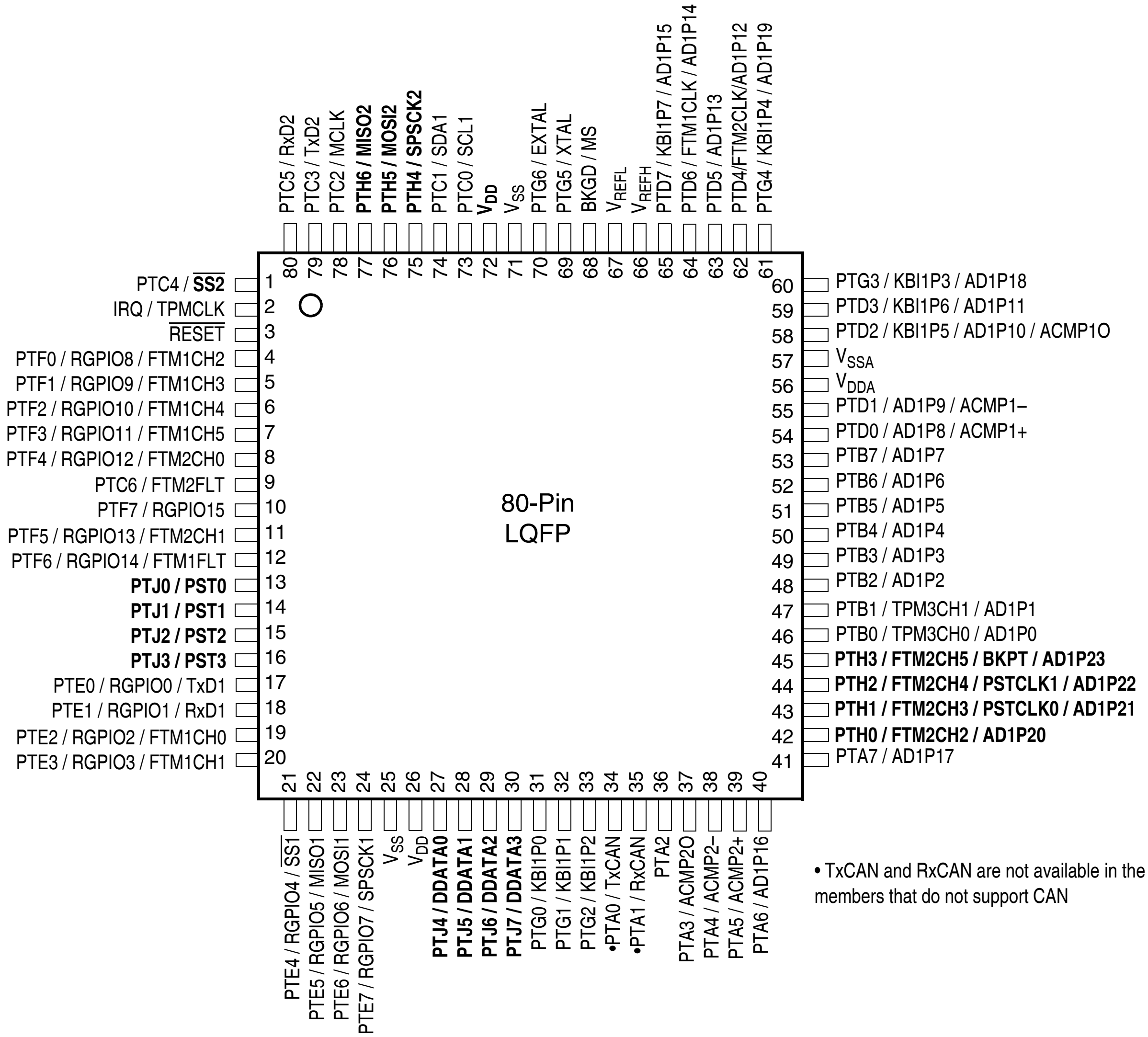


Figure 2. MCF51AC256 Series ColdFire Microcontroller 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

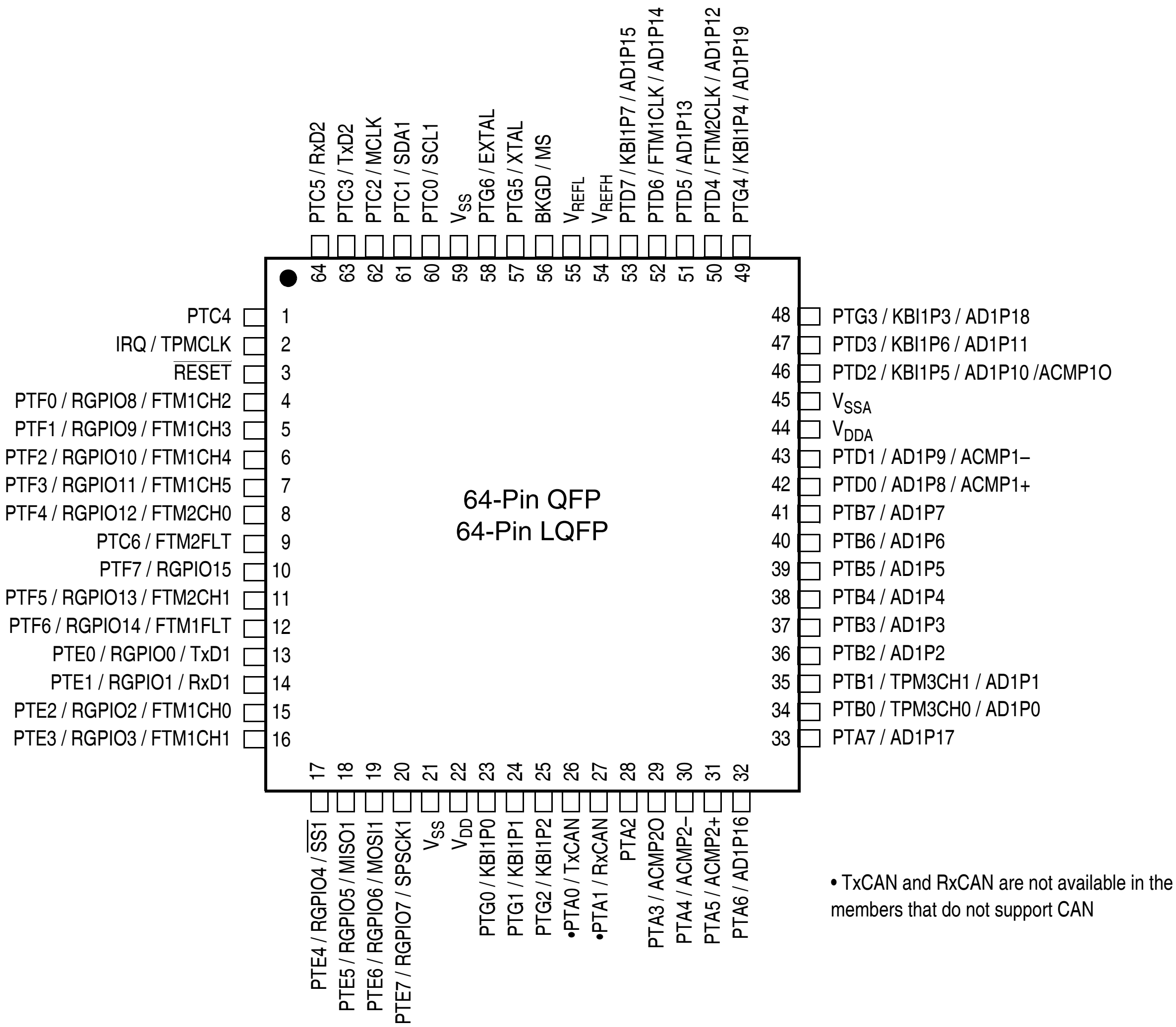


Figure 3. MCF51AC256 Series ColdFire Microcontroller 64-Pin QFP/LQFP

Figure 4 shows the pinout of the 44-pin LQFP.

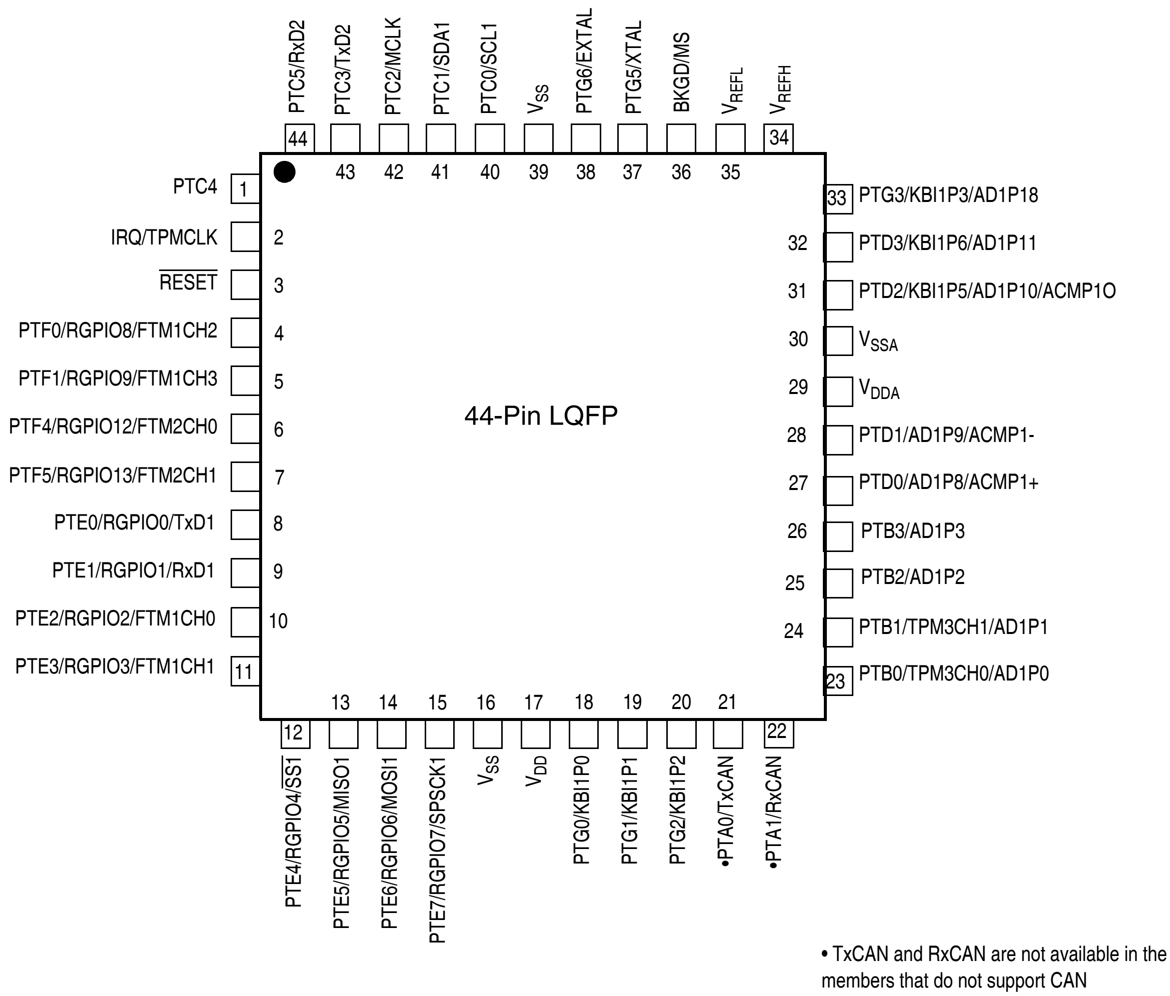


Figure 4. MCF51AC256 Series ColdFire Microcontroller 44-Pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest			
80	64	44	Port Pin	Alt 1	Alt 2	Alt 3
1	1	1	PTC4	$\overline{SS2}$		
2	2	2	IRQ	TPMCLK[1]		
3	3	3	$\overline{RESET}$			
4	4	4	PTF0	RGPIO8	FTM1CH2	
5	5	5	PTF1	RGPIO9	FTM1CH3	
6	6	—	PTF2	RGPIO10	FTM1CH4	
7	7	—	PTF3	RGPIO11	FTM1CH5	

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**
8	8	6	PTF4	RGPIO12	FTM2CH0	
9	9	—	PTC6	FTM2FLT		
10	10	—	PTF7	RGPIO15		
11	11	7	PTF5	RGPIO13	FTM2CH1	
12	12	—	PTF6	RGPIO14	FTM1FLT	
13	—	—	PTJ0	PST0		
14	—	—	PTJ1	PST1		
15	—	—	PTJ2	PST2		
16	—	—	PTJ3	PST3		
17	13	8	PTE0	RGPIO0	TxD1	
18	14	9	PTE1	RGPIO1	RxD1	
19	15	10	PTE2	RGPIO2	FTM1CH0	
20	16	11	PTE3	RGPIO3	FTM1CH1	
21	17	12	PTE4	RGPIO4	$\overline{SS1}$	
22	18	13	PTE5	RGPIO5	MISO1	
23	19	14	PTE6	RGPIO6	MOSI1	
24	20	15	PTE7	RGPIO7	SPSCK1	
25	21	16	V_{SS}			
26	22	17	V_{DD}			
27	—	—	PTJ4	DDATA0		
28	—	—	PTJ5	DDATA1		
29	—	—	PTJ6	DDATA2		
30	—	—	PTJ7	DDATA3		
31	23	18	PTG0	KBI1P0		
32	24	19	PTG1	KBI1P1		
33	25	20	PTG2	KBI1P2		
34	26	21	PTA0	TxCAN[2]		
35	27	22	PTA1	RxCAN[3]		
36	28	—	PTA2			
37	29	—	PTA3	ACMP2O		
38	30	—	PTA4	ACMP2–		
39	31	—	PTA5	ACMP2+		
40	32	—	PTA6	AD1P16		
41	33	—	PTA7	AD1P17		
42	—	—	PTH0	FTM2CH2	AD1P20	
43	—	—	PTH1	FTM2CH3	PSTCLK0	AD1P21
44	—	—	PTH2	FTM2CH4	PSTCLK1	AD1P22
45	—	—	PTH3	FTM2CH5	BKPT	AD1P23
46	34	23	PTB0	TPM3CH0	AD1P0	
47	35	24	PTB1	TPM3CH1	AD1P1	
48	36	25	PTB2	AD1P2		

Table 4. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest			
80	**64**	**44**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**
49	37	26	PTB3	AD1P3		
50	38	—	PTB4	AD1P4		
51	39	—	PTB5	AD1P5		
52	40	—	PTB6	AD1P6		
53	41	—	PTB7	AD1P7		
54	42	27	PTD0	AD1P8	ACMP1+	
55	43	28	PTD1	AD1P9	ACMP1–	
56	44	29	V_{DDA}			
57	45	30	V_{SSA}			
58	46	31	PTD2	KBI1P5	AD1P10	ACMP1O
59	47	32	PTD3	KBI1P6	AD1P11	
60	48	33	PTG3	KBI1P3	AD1P18	
61	49	—	PTG4	KBI1P4	AD1P19	
62	50	—	PTD4	FTM2CLK	AD1P12	
63	51	—	PTD5	AD1P13		
64	52	—	PTD6	FTM1CLK	AD1P14	
65	53	—	PTD7	KBI1P7	AD1P15	
66	54	34	V_{REFH}			
67	55	35	V_{REFL}			
68	56	36	BKGD	MS		
69	57	37	PTG5	XTAL		
70	58	38	PTG6	EXTAL		
71	59	39	V_{SS}			
72	—	—	V_{DD}			
73	60	40	PTC0	SCL1		
74	61	41	PTC1	SDA1		
75	—	—	PTH4	SPCK2		
76	—	—	PTH5	MOSI2		
77	—	—	PTH6	MISO2		
78	62	42	PTC2	MCLK		
79	63	43	PTC3	TxD2		
80	64	44	PTC5	RxD2		

1 TPMCLK, FTM1CLK, and FTM2CLK options are configured via software; out of reset, FTM1CLK, FTM2CLK, and TPMCLK are available to FTM1, FTM2, and TPM3 respectively.

2 TxCAN is available in the member that supports CAN.

3 RxCAN is available in the member that supports CAN.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AC256 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1], [2], [3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	–40 to 105	°C
Maximum junction temperature	T_J	150	°C
Thermal resistance [1,2,3,4]	θ_{JA}		°C/W
80-pin LQFP			
1s		51	
2s2p		38	
64-pin LQFP			
1s		59	
2s2p		41	
64-pin QFP			
		50	
1s		36	
2s2p			
44-pin LQFP			
1s		67	
2s2p		45	

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
[2] Junction to Ambient Natural Convection
[3] 1s — Single layer board, one signal layer
[4] 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulse per pin	—	3	
Charge device model	Series resistance	R1	0	Ω
	Storage capacitance	C	0	pF
	Number of pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Charge device model (CDM)	V_{CDM}	±500	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low drive (PTxDSn = 0) 5 V, I_{Load} = –4 mA 3 V, I_{Load} = –2 mA 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –1 mA	V_{OH}	 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	V
		Output high voltage — High drive (PTxDSn = 1) 5 V, I_{Load} = –15 mA 3 V, I_{Load} = –8 mA 5 V, I_{Load} = –8 mA 3 V, I_{Load} = –4 mA		 V_{DD} – 1.5 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.8	 — — — —	 — — — —	

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 4 mA 3 V, I_{Load} = 2 mA 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 1 mA	V_{OL}	—	—	1.5 1.5 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 15 mA 3 V, I_{Load} = 8 mA 5 V, I_{Load} = 8 mA 3 V, I_{Load} = 4 mA		—	—	1.5 1.5 0.8 0.8	
4	C	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	—	—	100 60	mA
5	C	Output low current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	—	—	100 60	mA
6	P	Input high voltage; all digital inputs	V_{IH}	$0.65 \times V_{DD}$	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	$0.35 \times V_{DD}$	V
8	D	Input hysteresis; all digital inputs	V_{hys}	$0.06 \times V_{DD}$	—	—	mV
9	P	Input leakage current; input only pins[2]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High impedance (off-state) leakage current[2]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[3]	R_{PU}	20	45	65	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t_{POR}	10	—	—	μs
16	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVDH}	4.2 4.27	4.35 4.4	4.5 4.6	V
17	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVDL}	2.48 2.5	2.68 2.7	2.7 2.72	V
18	P	Low-voltage warning threshold — high range V_{DD} falling V_{DD} rising	V_{LVWH}	4.2 4.27	4.4 4.45	4.5 4.6	V
19	P	Low-voltage warning threshold low range V_{DD} falling V_{DD} rising	V_{LVWL}	2.48 2.5	2.68 2.7	2.7 2.72	V
20	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	—	100 60	—	mV
21	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
22	D	DC injection current[5 6 7 8] (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	0 0	—	2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		0 0	—	25 –5	mA

1 Typical values are based on characterization data at 25°C unless otherwise stated.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

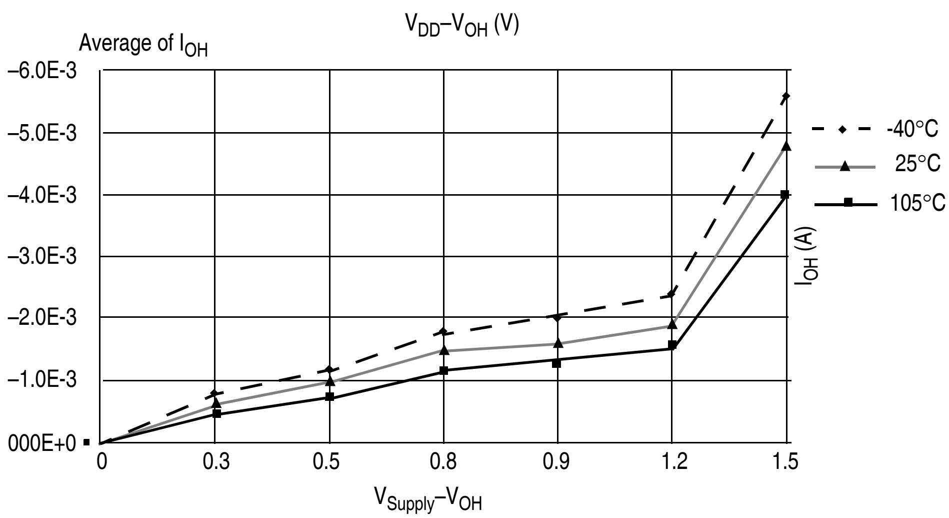


Figure 5. Typical I_{OH} vs. V_{DD}–V_{OH} at V_{DD} = 3 V (Low Drive, PTxDSn = 0)

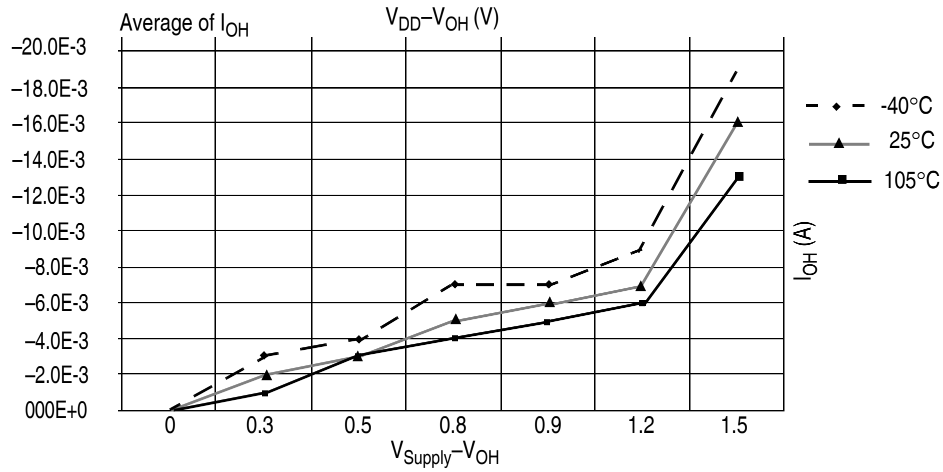


Figure 6. Typical I_{OH} vs. V_{DD}–V_{OH} at V_{DD} = 3 V (High Drive, PTxDSn = 1)

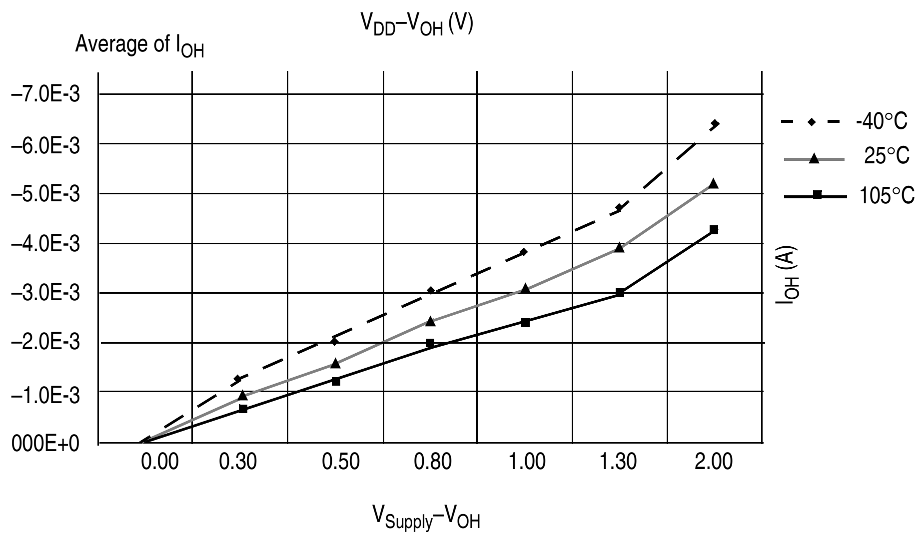


Figure 7. Typical I_{OH} vs. V_{DD}–V_{OH} at V_{DD} = 5 V (Low Drive, PTxDSn = 0)

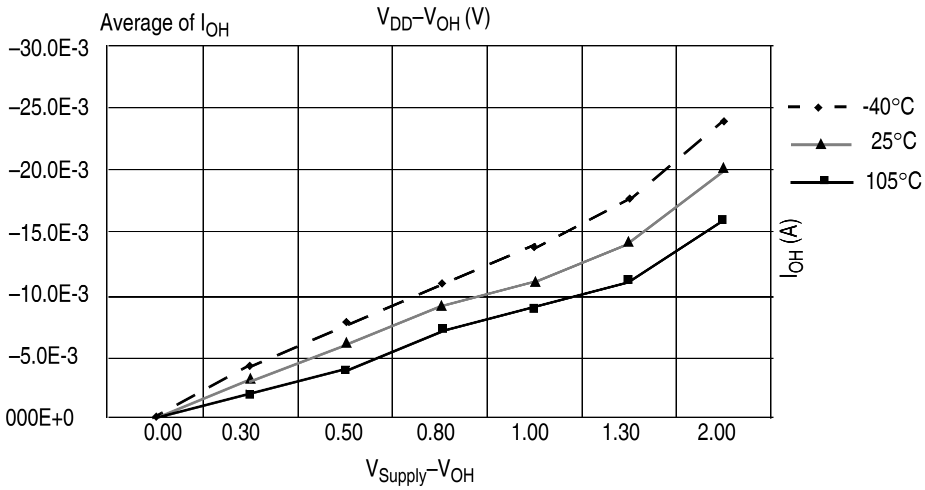


Figure 8. Typical I_{OH} vs. V_{DD}–V_{OH} at V_{DD} = 5 V (High Drive, PTxDSn = 1)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	T	Run supply current measured at FEI mode, all modules off, system clock at:	2 MHz	RI_{DD}	5	2.27	—	mA
					3.3	2.24	—	
			4 MHz		5	3.67	—	
					3.3	3.64	—	
			8 MHz		5	6.55	—	
					3.3	6.54	—	
			16 MHz		5	11.90	—	
					3.3	11.85	—	
2	T	Run supply current measured at FEI mode, all modules on, system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.33	—	
					3.3	4.32	—	
			8 MHz		5	8.17	—	
					3.3	8.05	—	
			16 MHz		5	14.8	—	
					3.3	14.74	—	
3	T	Run supply current measured at FBE mode, all modules off (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.28	—	
					3.3	3.26	—	
			4 MHz		5	4.69	—	
					3.3	4.67	—	
			8 MHz		5	7.48	—	
					3.3	7.46	—	
			16 MHz		5	13.10	—	
					3.3	13.07	—	
4	T	Run supply current measured at FBE mode, all modules on (RANGE = 1, HGO = 0), system clock at:	2 MHz		5	3.64	—	
					3.3	3.63	—	
			4 MHz		5	5.38	—	
					3.3	5.35	—	
			8 MHz		5	8.65	—	
					3.3	8.64	—	
			16 MHz		5	15.55	—	
					3.3	15.40	—	

Table 11. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
5	C	Wait mode supply[3] current measured at (CPU clock = 2 MHz, f_{Bus} = 1 MHz)	WI_{DD}	5	1.3	2	mA
				3	1.29	2	
6	C	Wait mode supply[3] current measured at (CPU clock = 16 MHz, f_{Bus} = 8 MHz)		5	5.11	8	mA
				3	5.1	8	
7	C	Wait mode supply[3] current measured at (CPU clock = 50 MHz, f_{Bus} = 25 MHz)		5	15.24	25	mA
				3	15.2	25	
8	C	Stop2 mode supply current –40 °C 25 °C 120 °C	$S2I_{DD}$	5	1.40	2.5 2.5 200	µA
		–40 °C 25 °C 120 °C		3	1.16	2.5 2.5 200	µA
9	C	Stop3 mode supply current –40 °C 25 °C 120 °C	$S3I_{DD}$	5	1.60	2.5 2.5 220	µA
		–40 °C 25 °C 120 °C		3	1.35	2.5 2.5 220	µA
10	C	RTI adder to stop2 or stop3[3], 25 °C	$S23I_{DDRTI}$	5	300		nA
				3	300		nA
11	C	Adder to stop3 for oscillator enabled[4] (ERCLKEN =1 and EREFSTEN = 1)	$S3I_{DDOSC}$	5, 3	5		µA

1 Typicals are measured at 25 °C.
2 Values given here are preliminary estimates prior to completing characterization.
3 Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.
4 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

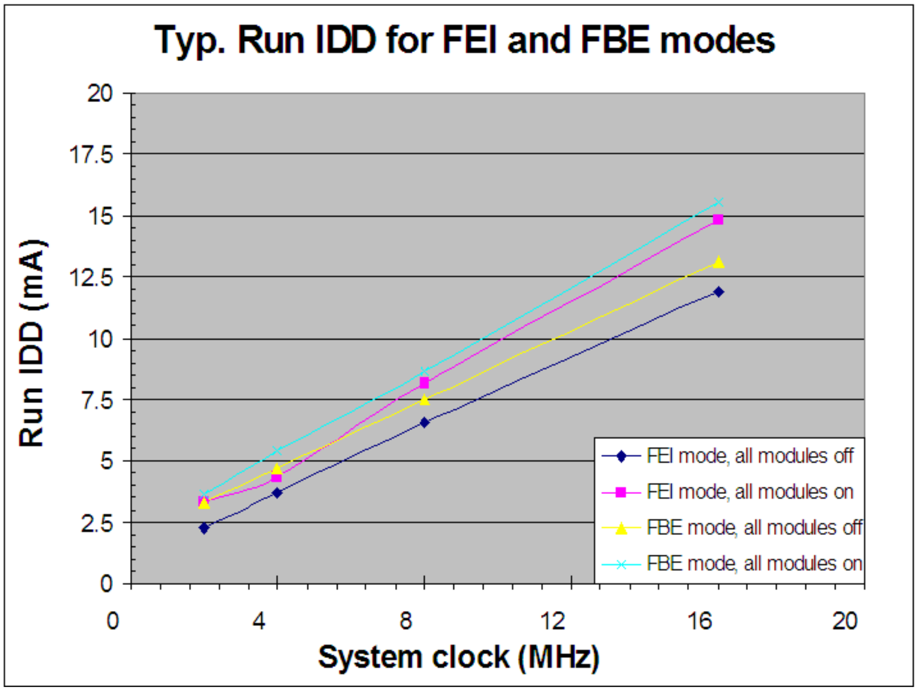


Figure 9. Typical Run I_{DD} vs. System Clock Freq. for FEI and FBE Modes

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current (active)	I_{DDAC}	—	20	35	µA
3	D	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
4	D	Analog input offset voltage	V_{AIO}	—	20	40	mV
5	D	Analog comparator hysteresis	V_H	3.0	6.0	20.0	mV
6	D	Analog input leakage current	I_{ALKG}	—	—	1.0	µA
7	D	Analog comparator initialization delay	t_{AINIT}	—	—	1.0	µs
8	P	Bandgap voltage reference factory trimmed at V_{DD} = 5.3248 V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	D		Delta to V_{DD} $(V_{DD} - V_{DDA})$[2]	ΔV_{DDA}	–100	0	100	mV	
2	D	Ground voltage	Delta to V_{SS} $(V_{SS} - V_{SSA})$[2]	ΔV_{SSA}	–100	0	100	mV	
3	D	Reference voltage high		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
4	D	Reference voltage low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
5	D	Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
6	C	Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
7	C	Input resistance		R_{ADIN}	—	3	5	kΩ	
8	C	Analog source resistance	12-bit mode $f_{ADCK} > 4MHz$ $f_{ADCK} < 4MHz$	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	C		10-bit mode $f_{ADCK} > 4MHz$ $f_{ADCK} < 4MHz$		— —	— —	5 10		
	C		8-bit mode (all valid f_{ADCK})		—	—	10		
9	D	ADC conversion clock frequency	High speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	
	D		Low power (ADLPC = 1)		0.4	—	4.0		

[1] Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

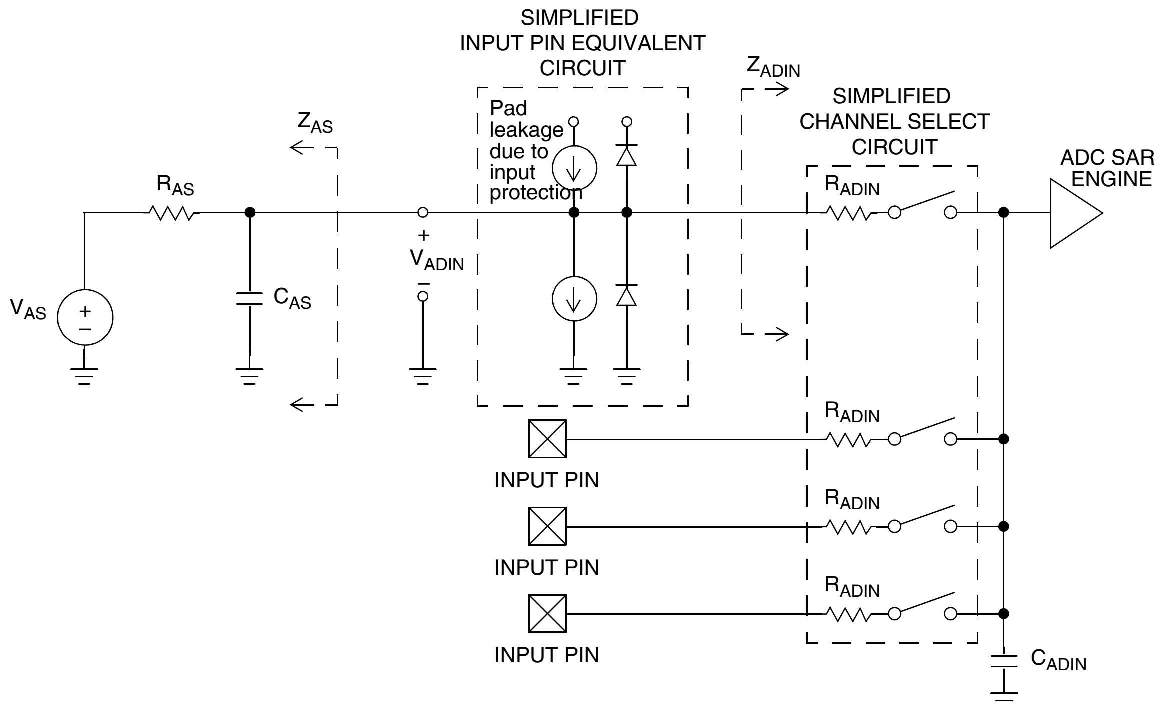


Figure 10. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	133	—	μA	
2	T	Supply current ADLPC = 1 ADLSM = 0 ADCO = 1		I_{DDA}	—	218	—	μA	
3	T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	327	—	μA	
4	D	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.582	1	mA	
5	T	Supply current	Stop, reset, module off	I_{DDA}	—	0.011	1	μA	
6	P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
			Low power (ADLPC = 1)		1.25	2	3.3		

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
7	P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See Table 10 for conversion time variances
			Long sample (ADLSMP = 1)		—	40	—		
8	T	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long sample (ADLSMP = 1)		—	23.5	—		
9	T	Total unadjusted error	12-bit mode	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantizatio n
	P		10-bit mode		—	±1	±2.5		
	T		8-bit mode		—	±0.5	±1.0		
10	T	Differential non-linearity	12-bit mode	DNL	—	±1.75	—	LSB[2]	
	P		10-bit mode[3]		—	±0.5	±1.0		
	T		8-bit mode[3]		—	±0.3	±0.5		
11	T	Integral non-linearity	12-bit mode	INL	—	±1.5	—	LSB[2]	
	T		10-bit mode		—	±0.5	±1.0		
	T		8-bit mode		—	±0.3	±0.5		
12	T	Zero-scale error	12-bit mode	E_{ZS}	—	±1.5	—	LSB[2]	$V_{ADIN} = V_{SSA}$
	P		10-bit mode		—	±0.5	±1.5		
	T		8-bit mode		—	±0.5	±0.5		
13	T	Full-scale error	12-bit mode	E_{FS}	—	±1	—	LSB[2]	$V_{ADIN} = V_{DDA}$
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.5	±0.5		
14	D	Quantization error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	
			10-bit mode		—	—	±0.5		
			8-bit mode		—	—	±0.5		
15	D	Input leakage error	12-bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10-bit mode		—	±0.2	±2.5		
			8-bit mode		—	±0.1	±1		
16	D	Temp sensor voltage	25°C	V_{TEMP25}	—	1.396	—	V	
17	D	Temp sensor slope	–40 °C–25 °C	m	—	3.266	—	mV/°C	
			25 °C–85 °C		—	3.638	—		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$.

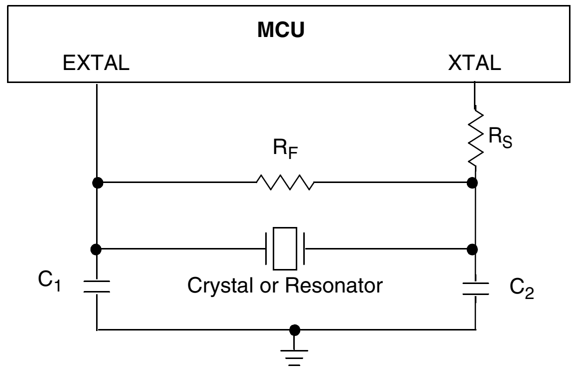
3 Monotonicity and No-Missing-Codes guaranteed in 10-bit and 8-bit modes
4 Based on input pad leakage current. Refer to pad electricals.

2.9 External Oscillator (XOSC) Characteristics

Table 15. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode[2] High range (RANGE = 1) PEE or PBE mode[3] High range (RANGE = 1, HGO = 1) BLPE mode High range (RANGE = 1, HGO = 0) BLPE mode	 f_{lo} $f_{hi\text{-}fll}$ $f_{hi\text{-}pll}$ $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	 32 1 1 1 1	 — — — — —	 38.4 5 16 16 8	 kHz MHz MHz MHz MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor Low range (32 kHz to 38.4 kHz) High range (1 MHz to 16 MHz)	R_F		 10 1		MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time [4] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[5] High range, high gain (RANGE = 1, HGO = 1)[5]	 $t_{CSTL\text{-}LP}$ $t_{CSTL\text{-}HGO}$ $t_{CSTH\text{-}LP}$ $t_{CSTH\text{-}HGO}$	 — — — —	 200 400 5 15	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE or FBE mode [2] PEE or PBE mode [3] BLPE mode	f_{extal}	 0.03125 1 0	 — — —	 5 16 40	MHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.
4 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.
5 4 MHz crystal



2.10 MCG Specifications

Table 16. MCG Frequency Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	C	Internal reference frequency — factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — untrimmed		f_{int_ut}	31.25	—	39.0625	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	C	DCO output frequency range — untrimmed[2]	Low range (DRS=00)	f_{dco_ut}	16	—	20	MHz
	C		Mid range (DRS=01)		32	—	40	
	C		High range (DRS=10)		48	—	60	
5	P	DCO output frequency[2] reference =32768Hz and DMX32 = 1	Low range (DRS=00)	f_{dco_DMX32}	—	16.82	—	MHz
	P		Mid range (DRS=01)		—	33.69	—	
	P		High range (DRS=10)		—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0–70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	D	FLL acquisition time[3]		$t_{fll\_acquire}$	—	—	1	ms
11	D	PLL acquisition time[4]		$t_{pll\_acquire}$	—	—	1	ms
12	D	Long term jitter of DCO output clock (averaged over 2ms interval)[5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
13	D	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz
16	D	Jitter of PLL output clock measured over 625 ns[6]		$f_{pll\_jitter\_625ns}$	—	0.566[6]	—	$\%f_{pll}$
17	D	Lock entry frequency tolerance[7]		D_{lock}	±1.49	—	±2.98	%

Table 16. MCG Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
18	D	Lock exit frequency tolerance [8]	D_{unl}	±4.47	—	±5.97	%
19	D	Lock time — FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
20	D	Lock time — PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
21	D	Loss of external clock minimum frequency — RANGE = 0	f_{loc_low}	(3/5) × f_{int}	—	—	kHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency must not exceed the maximum specified bus clock frequency of the device.

3 This specification applies when the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 This specification applies when the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

6 625 ns represents 5 time quanta for CAN applications, under worst case conditions of 8 MHz CAN bus clock, 1 Mbps CAN bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

7 Below D_{lock} minimum, the MCG enters lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

8 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 17. Control Timing

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	800	—	1500	μs
3	D	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	$66 \times t_{cyc}$	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
8	D	KBIPx pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns
9	D	Port rise and fall time (load = 50 pF)[4] Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive Slew rate control disabled (PTxSE = 0), Low Drive Slew rate control enabled (PTxSE = 1), Low Drive	t_{Rise}, t_{Fall}	— — — —	11 35 40 75	—	ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

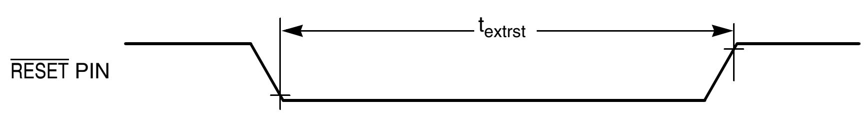


Figure 11. Reset Timing

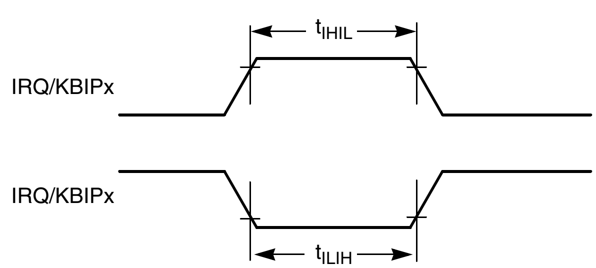


Figure 12. IRQ/KBIPx Timing

2.11.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM/FTM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

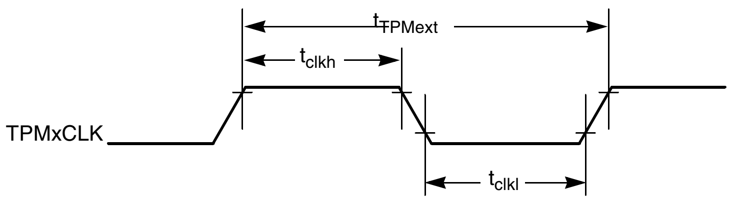


Figure 13. Timer External Clock

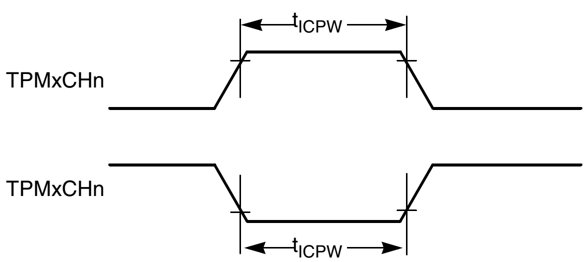


Figure 14. Timer Input Capture Pulse

2.11.3 MSCAN

Table 19. MSCAN Wake-Up Pulse Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	D	MSCAN wake-up dominant pulse filtered	t_{WUP}	—	—	2	µs
2	D	MSCAN wake-up dominant pulse pass	t_{WUP}	5	—	5	µs

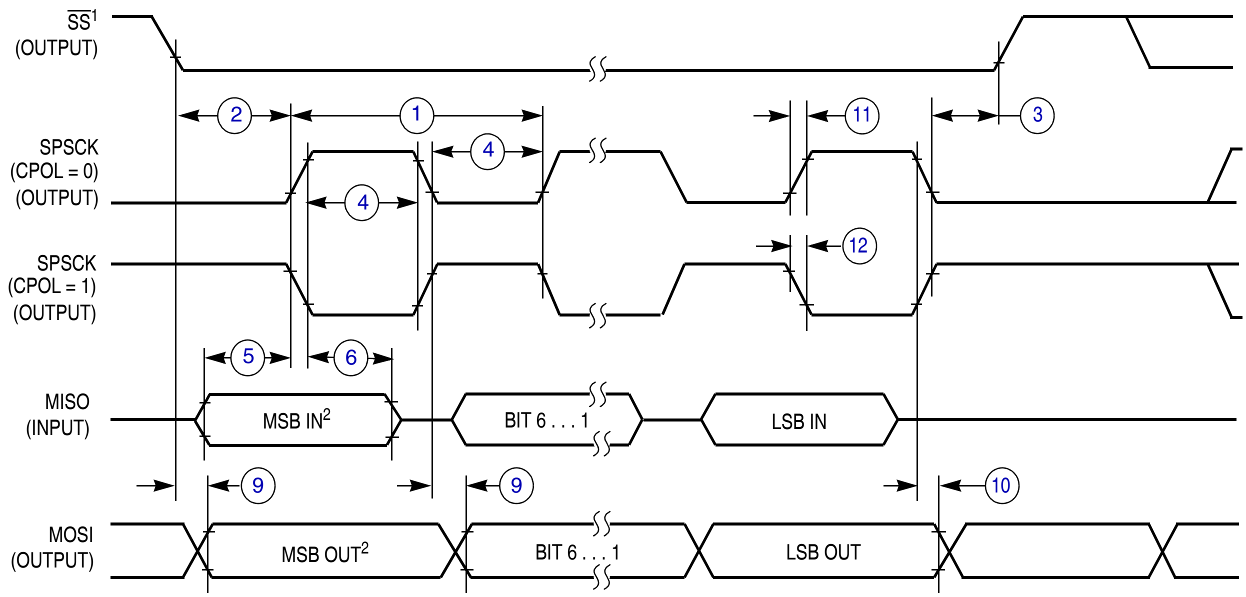
[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2.12 SPI Characteristics

Table 20 and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

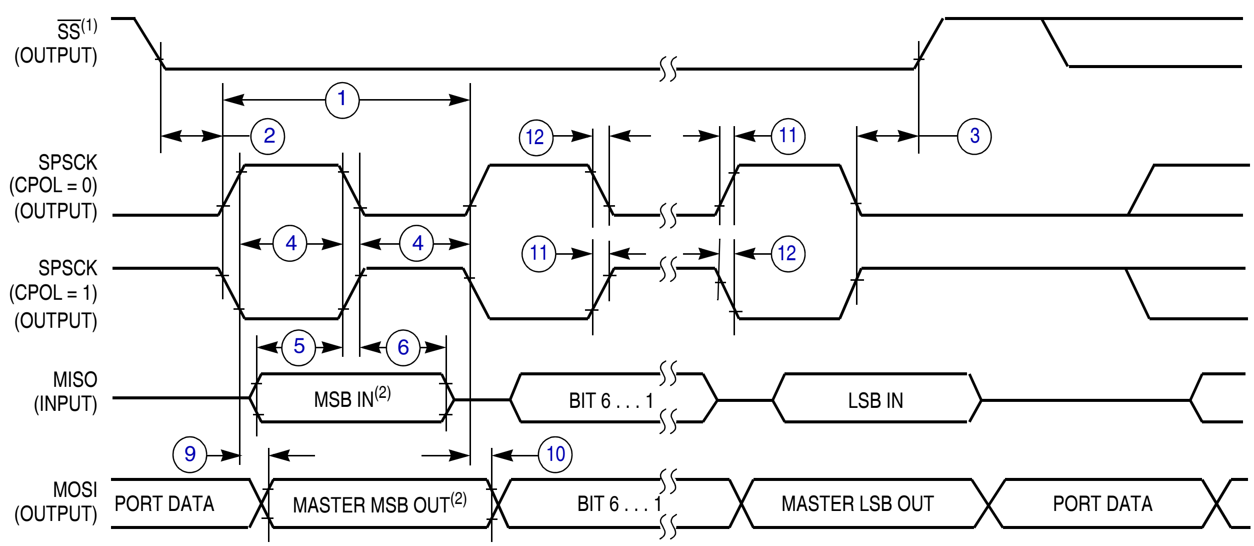
Table 20. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	f_{Bus}/2048 0	f_{Bus}/2 f_{Bus}/4	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	t_{cyc} – 30 t_{cyc} – 30	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	t_{cyc} – 25 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	t_{cyc} – 25 25	ns ns



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. SPI Master Timing (CPHA =1)

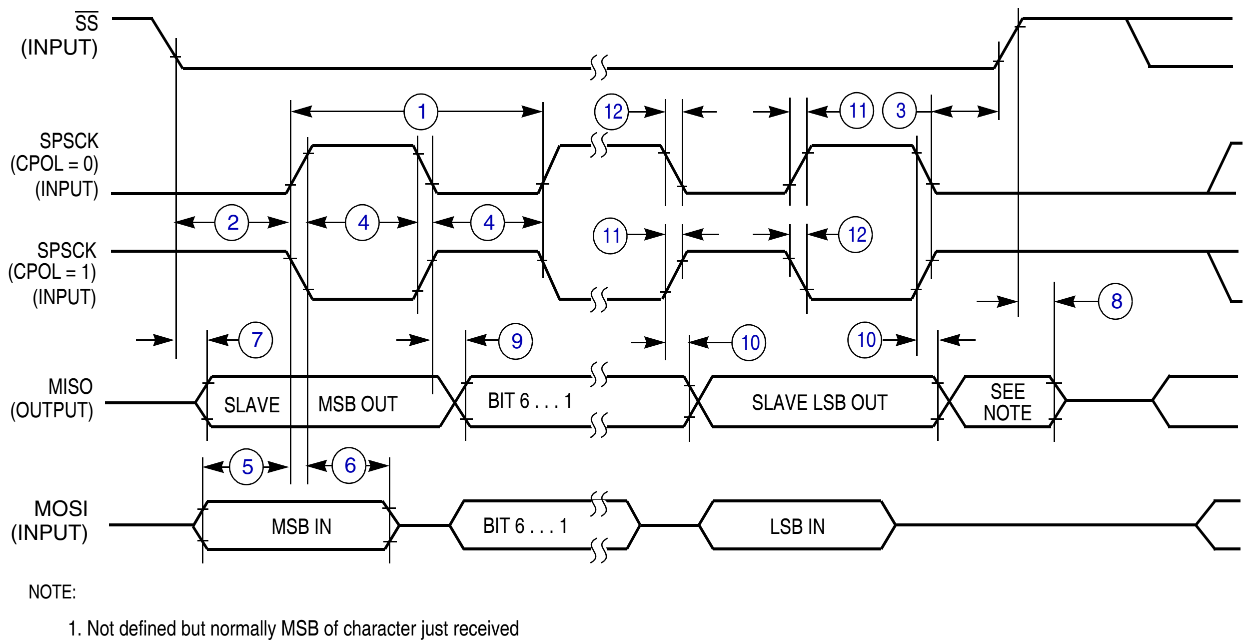


Figure 17. SPI Slave Timing (CPHA = 0)

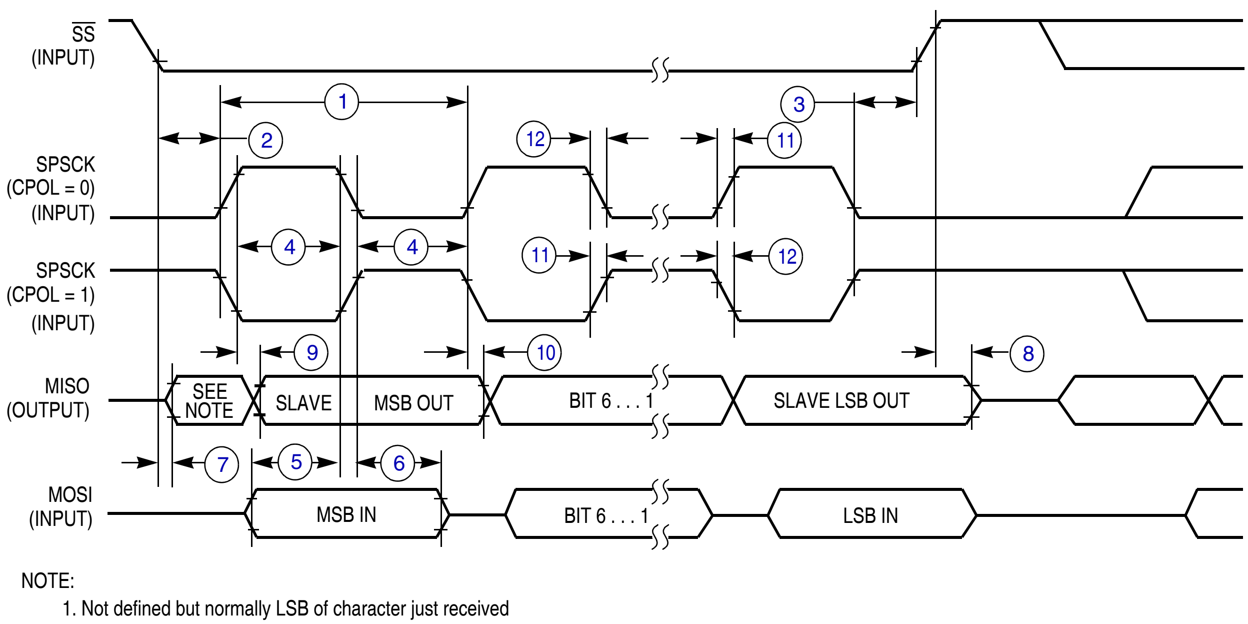


Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see Chapter 4, “Memory.”

Table 21. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	—	Supply voltage for program/erase	$V_{prog/erase}$	2.7	—	5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
3	—	Internal FCLK frequency[2]	f_{FCLK}	150	—	200	kHz
4	—	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	μs
5	—	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
6	—	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
7	—	Page erase time[3]	t_{Page}	4000			t_{Fcyc}
8	—	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40 °C to 105 °C T = 25 °C	—	 10,000 —	 — 100,000	 — —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. The frequency of this clock is controlled by a software setting.
3. These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.
4. **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.
5. **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

3 Mechanical Outline Drawings

Table 22 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51AC256 Series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 22, or
- Open a browser to the FreescaleÆ website (http://www.freescale.com), and enter the appropriate document number (from Table 22) in the “Enter Keyword” search box at the top of the page.

Table 22. Package Information

Pin Count	Type	Document No.
80	LQFP	98ARL10530D
64	LQFP	98ASS23234W
64	QFP	98ASB42844B
44	LQFP	98ASS23225W

4 Revision History

Table 23. Revision History

Revision	Description
1	Initial published
2	Updated ADC channels, Item 1, 4-5 on Table 2.10
3	Completed all theTBDs. Changed RTC to RTI in Figure 1. Corrected the block diagram. Changed V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA}. Added charge device model data and removed machine data in Table 8. Updated the specifications of V_{LVDH}, V_{LVDL}, V_{LVWH} and V_{LVWL} in Table 10. Updated $S2I_{DD}$, $S3I_{DD}$ in Table 11. Added C column in Table 14. Updated f_{dco_DMX32} in Table 16.
4	Corrected the expansion of SPI to serial peripheral interface.
5	Updated V_{LVDL} in the Table 10. Updated RI_{DD} in the Table 11.
6	Updated V_{LVDH}, V_{LVDL}, V_{LVWH} and V_{LVWL} in the Table 10. Added LPO on the Figure 1 and LPO features in the Section 1.3, "Features."
7	Added 44-pin LQFP package information for AC256 and AC128.

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