

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74AC00P, TC74AC00F, TC74AC00FT

### Quad 2-Input NAND Gate

The TC74AC00 is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

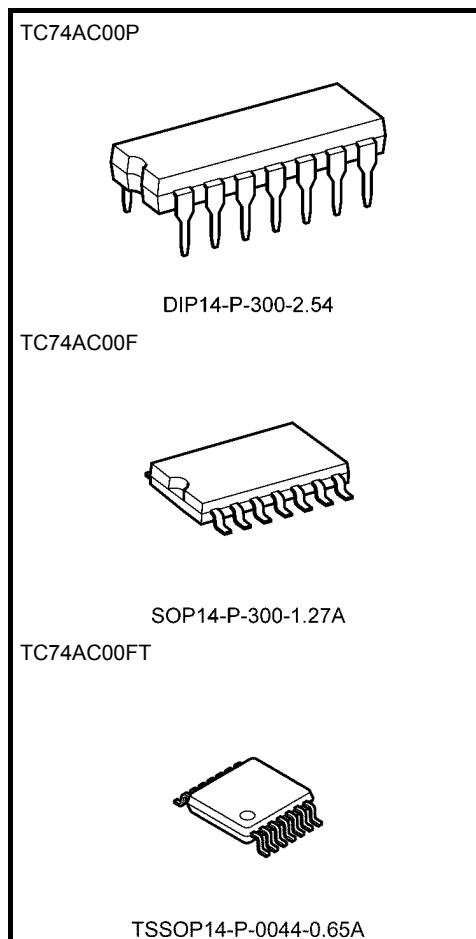
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

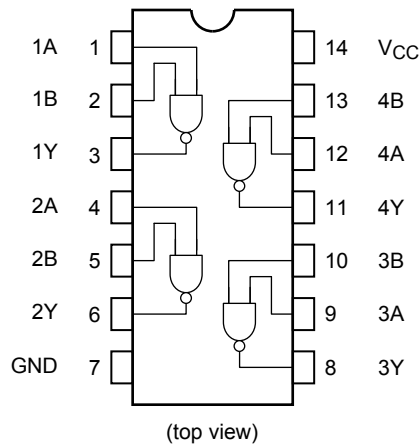
- High speed:  $t_{pd} = 3.8 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Symmetrical output impedance:  
 $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$   
 Capability of driving  $50 \Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} \text{ (opr)} = 2 \text{ V to } 5.5 \text{ V}$
- Pin and function compatible with 74F00



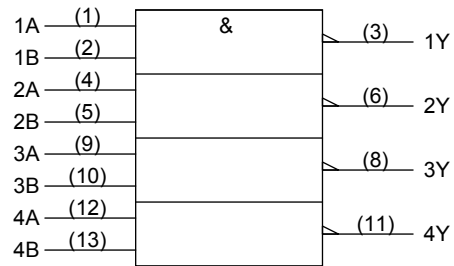
Weight	
DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)

Start of commercial production  
1986-05

## Pin Assignment



## IEC Logic Symbol



## Truth Table

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 100$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40^{\circ}C$  to  $65^{\circ}C$ . From  $T_a = 65^{\circ}C$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  should be applied up to 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $85^\circ\text{C}$		Unit	
				Min	Typ.	Max	Min	Max		
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	1.50	—	V	
			3.0	2.10	—	—	2.10	—		
			5.5	3.85	—	—	3.85	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	—	0.50	V	
			3.0	—	—	0.90	—	0.90		
			5.5	—	—	1.65	—	1.65		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -4 \text{ mA}$	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
$I_{OH} = -75 \text{ mA}$ (Note)	5.5	—	—	—	3.85	—				
	Low-level output voltage	$V_{IN} = V_{IH}$	$I_{OL} = 50 \mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
3.0				—	0.0	0.1	—	0.1		
4.5				—	0.0	0.1	—	0.1		
$I_{OL} = 12 \text{ mA}$			3.0	—	—	0.36	—	0.44		
			4.5	—	—	0.36	—	0.44		
$I_{OL} = 75 \text{ mA}$ (Note)	5.5	—	—	—	—	1.65				
	Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	$\mu\text{A}$	

Note: This spec indicates the capability of driving 50  $\Omega$  transmission lines.  
One output should be tested at a time for a 10 ms maximum duration.

### AC Characteristics ( $C_L = 50 \text{ pF}$ , $R_L = 500 \text{ } \Omega$ , input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			VCC (V)	Min	Typ.	Max	Min		Max
Propagation delay time	$t_{pLH}$	—	$3.3 \pm 0.3$	—	6.6	11.2	1.0	12.9	ns
	$t_{pHL}$		$5.0 \pm 0.5$	—	4.9	7.0	1.0	8.0	
Input capacitance	$C_{IN}$	—	—	5	10	—	10	pF	
Power dissipation capacitance	$C_{PD}$	(Note)	—	68	—	—	—	pF	

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

## Package Dimensions

DIP14-P-300-2.54

Unit : mm



Weight: 0.96 g (typ.)

**Package Dimensions**

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

**Package Dimensions**

TSSOP14-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

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