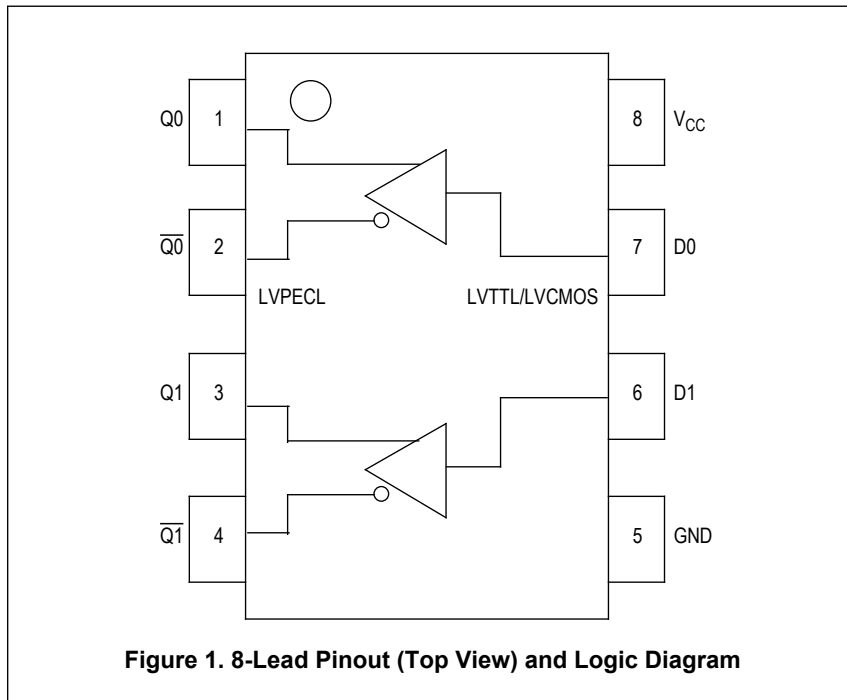


The MC100ES60T22 is a low skew dual LVTTTL/LVCMOS to differential LVPECL translator. The low voltage PECL levels, small package, and dual gate design are ideal for clock translation applications.

Features

- 280 ps typical propagation delay
- 100 ps max output-to-output skew
- LVPECL operating range: $V_{CC} = 3.135\text{ V to }3.8\text{ V}$
- 8-lead SOIC and 8-lead TSSOP packages
- Ambient temperature range $-40^{\circ}\text{C to }+85^{\circ}\text{C}$
- 8-lead SOIC Pb-free package available



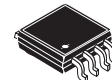
MC100ES60T22



**D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-07**



**EF SUFFIX
8-LEAD SOIC PACKAGE
Pb-FREE PACKAGE
CASE 751-07**



**DT SUFFIX
8-LEAD TSSOP PACKAGE
CASE 1640-01**

ORDERING INFORMATION

Device	Package
MC100ES60T22D	SOIC-8
MC100ES60T22DR2	SOIC-8
MC100ES60T22EF	SOIC-8 (Pb-Free)
MC100ES60T22EFR2	SOIC-8 (Pb-Free)
MC100ES60T22DT	TSSOP-8
MC100ES60T22DTR2	TSSOP-8

PIN DESCRIPTION

Pin	Function
D0, D1	LVTTTL/LVCMOS Inputs
Q_n, \overline{Q}_n	LVPECL Differential Outputs
V_{CC}	Positive Supply
GND	Negative Supply

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 k Ω
Internal Input Pullup Resistor		75 k Ω
ESD Protection	Human Body Model	> 2000 V
	Machine Model	> 200 V
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 8 SOIC	190°C/W
	500 LFPM, 8 SOIC	130°C/W
	0 LFPM, 8 TSSOP	185°C/W
	500 LFPM, 8 TSSOP	140°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	$V_{CC} + 0.3$ $V_{EE} - 0.3$	V V
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		-40 to +85	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics ($V_{CC} = 3.135$ V to 3.8 V; $V_{EE} = 0$ V)

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
$V_{OH}^{(1)}$	Output HIGH Voltage	$V_{CC} - 1150$	$V_{CC} - 1020$	$V_{CC} - 800$	$V_{CC} - 1200$	$V_{CC} - 970$	$V_{CC} - 750$	mV
$V_{OL}^{(1)}$	Output LOW Voltage	$V_{CC} - 1950$	$V_{CC} - 1620$	$V_{CC} - 1250$	$V_{CC} - 2000$	$V_{CC} - 1680$	$V_{CC} - 1300$	mV

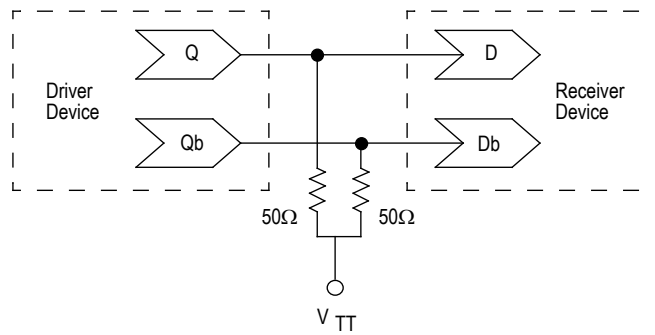
1. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2$ volts.

Table 4. LVTTTL / LVCMOS Input DC Characteristics ($V_{CC} = 3.135$ V to 3.8 V)

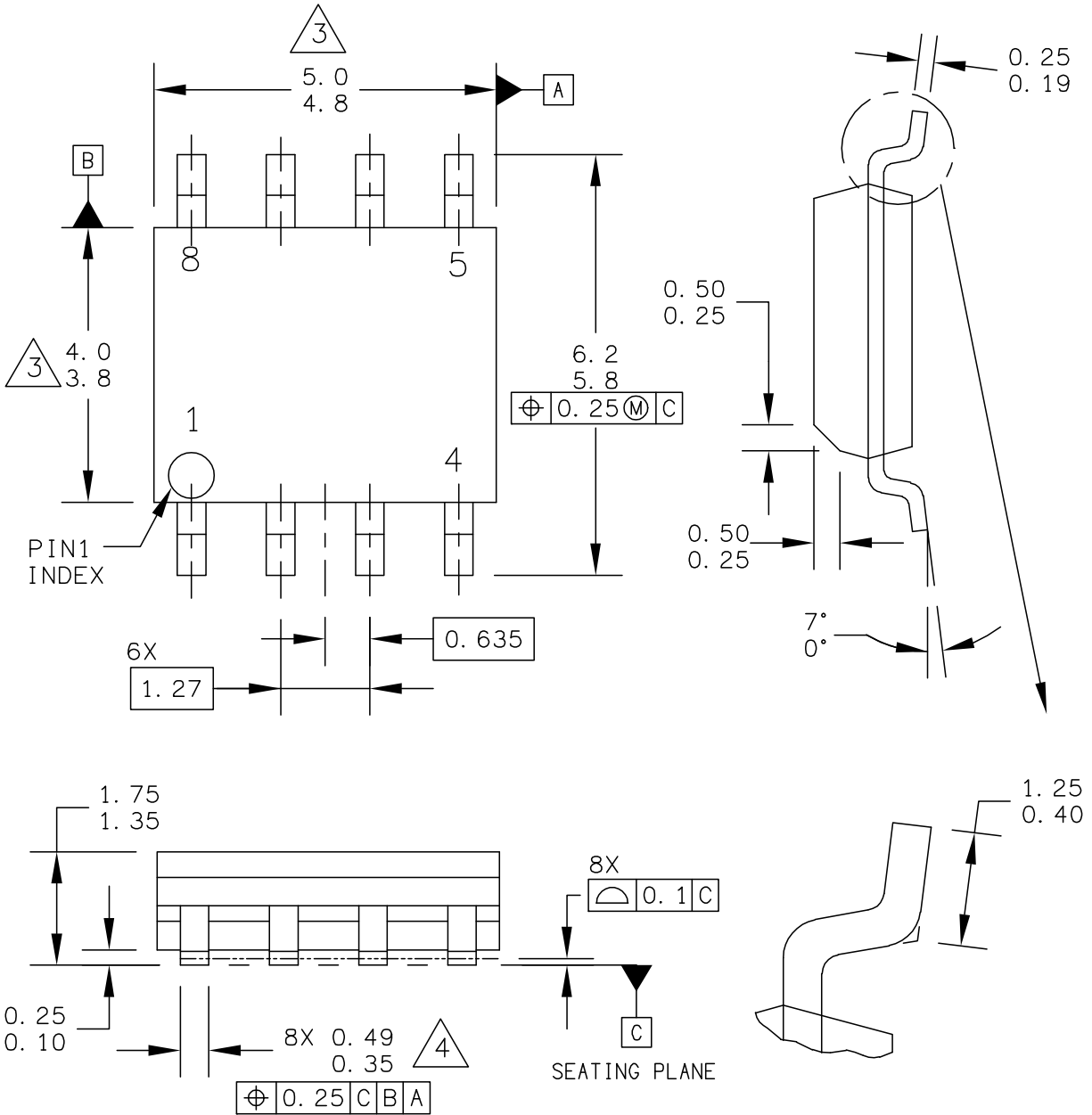
Symbol	Characteristic	Condition	-40°C			0°C to 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Current	$V_{IN} = V_{CC}$			± 150			± 150	μ A
V_{IK}	Input Clamp Voltage	$I_{IN} = -18$ mA			-1.2			-1.2	V
V_{IH}	Input HIGH Voltage		2.0		$V_{CC} + 0.3$	2.0		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage				0.8			0.8	V

Table 5. AC Characteristics ($V_{CC} = 3.134 \text{ V to } 3.8 \text{ V}$; $V_{EE} = 0 \text{ V}$)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Toggle Frequency			1			1			1	GHz
t_{PLH} , t_{PHL}	Propagation Delay	100	260	400	100	280	400	100	280	450	ps
t_{SKEW}	Skew part-to-part			300			300			350	ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V_{outPP}	Output Peak-to-Peak Voltage	350	750		350	750		350	750		mV
t_r / t_f	Output Rise/Fall Times (20% – 80%)	50		400	50		400	50		400	ps

**Figure 2. Typical Termination for Output Driver and Device Evaluation**

PACKAGE DIMENSIONS



	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: U	
	CASE NUMBER: 751-07	07 APR 2005	
	STANDARD: JEDEC MS-012AA		

**CASE 751-07
ISSUE U
8-LEAD SOIC PACKAGE**

PACKAGE DIMENSIONS

NOTES:

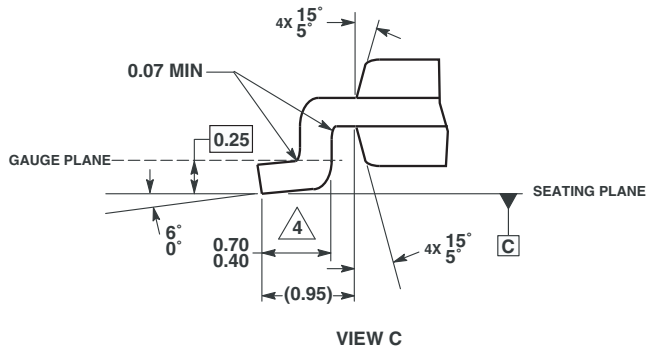
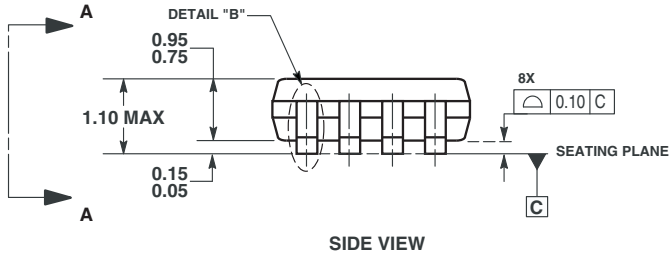
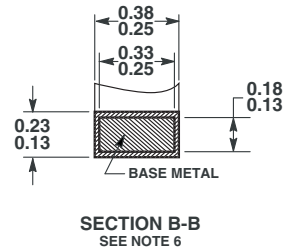
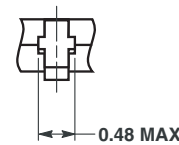
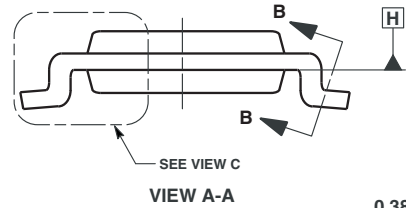
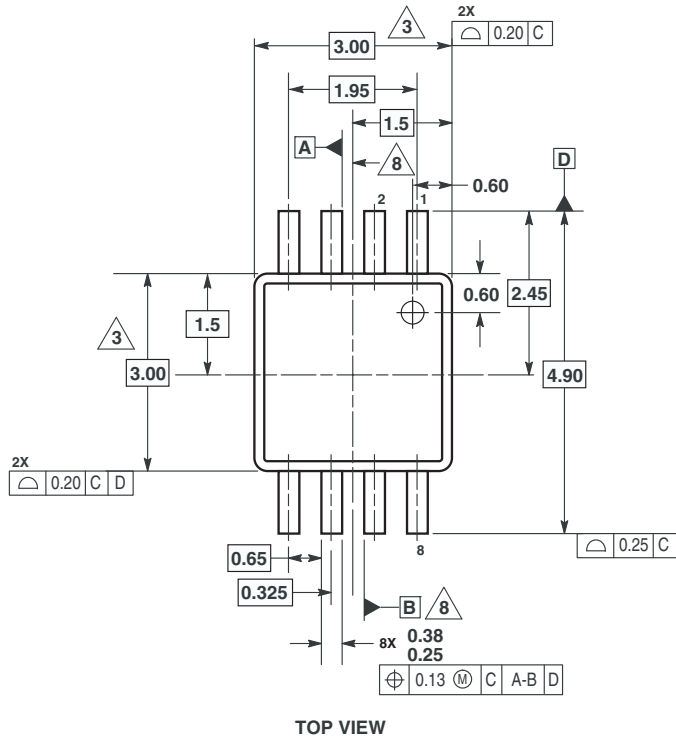
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 8LD SOIC NARROW BODY	DOCUMENT NO: 98ASB42564B	REV: U	
	CASE NUMBER: 751-07	07 APR 2005	
	STANDARD: JEDEC MS-012AA		

PAGE 2 OF 2

**CASE 751-07
ISSUE U
8-LEAD SOIC PACKAGE**

PACKAGE DIMENSIONS



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT DATUM H, MOLD FLASH OR PROTRUSIONS, SHALL NOT EXCEED 0.15mm PER SIDE.
4. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.14mm SEE DETAIL "B" AND SECTION B-B.
6. SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25mm FROM THE LEAD TIP.
7. THIS PART IS COMPLIANT WITH JEDEC REGISTRATION MO-187 AA.
8. DATUMS A AND B TO BE DETERMINED DATUM PLANE H.

**CASE 1640-01
ISSUE O
8-LEAD TSSOP PACKAGE**

Revision History Sheet

Rev	Table	Page	Description of Change	Date
3		1	Product Discontinuance Notice – Last Time Buy Expires on (12/12/2013)	1/9/13

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