# **Dual D-Type Flip-Flop with Set and Clear**

# With 5.0 V-Tolerant Inputs

The MC74LVX74 is an advanced high speed CMOS D-type flip-flop. The inputs tolerate voltages up to 7.0~V, allowing the interface of 5.0~V systems to 3.0~V systems.

The signal level applied to the D input is transferred to O output during the positive going transition of the Clock pulse.

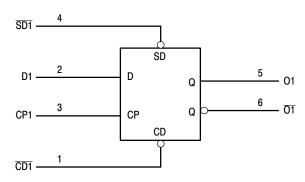
Clear  $(\overline{CD})$  and Set  $(\overline{SD})$  are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

# **Features**

- High Speed:  $f_{max} = 145 \text{ MHz}$  (Typ) at  $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2 \mu A$  (Max) at  $T_A = 25$ °C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.5 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:

Human Body Model > 2000 V; Machine Model > 200 V

• These Devices are Pb-Free and are RoHS Compliant



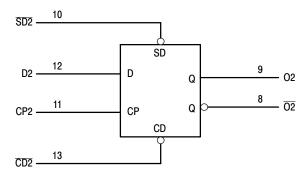


Figure 1. Logic Diagram



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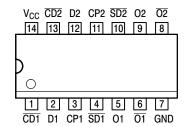
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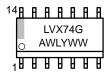
SOIC-14 NB D SUFFIX CASE 751A TSSOP-14 DT SUFFIX CASE 948G

#### **PIN ASSIGNMENT**



14-Lead (Top View)

## **MARKING DIAGRAMS**





SOIC-14 NB

TSSOP-14

LVX74 = Specific Device Code A = Assembly Location

WL, L = Wafer Lot
Y = Year
W, WW = Work Week
G or = Pb-Free Package

(Note: Microdot may be in either location)

# **PIN NAMES**

Pins	Function
CP1, CP2 D1, D2	Clock Pulse Inputs Data Inputs
CD1, CD2 SD1, SD2 On, On	Direct Clear Inputs Direct Set Inputs Outputs

# **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

	INPUTS			OUTPUTS		
SDn	CDn	CPn	Dn	On	On	OPERATING MODE
L H	H L	X X	X X	H L	L H	Asynchronous Set Asynchronous Clear
L	L	Х	Х	Н	Н	Undetermined
H H	H H	↑ ↑	h I	H L	L H	Load and Read Register
Н	Н	1	Х	NC	NC	Hold

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition; NC = No Change; X = High or Low Voltage Level or Transitions are Acceptable; ↑ = Low–to–High Transition; ↑ = Not a Low–to–High Transition; For I<sub>CC</sub> Reasons DO NOT FLOAT Inputs

# **MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
l <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

#### DC ELECTRICAL CHARACTERISTICS

	Parameter		v <sub>cc</sub>	T <sub>A</sub> = 25°C			$T_A = -40 \text{ to } 85^{\circ}\text{C}$		
Symbol		Test Conditions	V	Min	Тур	Max	Min	Max	Unit
V <sub>IH</sub>	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V <sub>IL</sub>	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	$I_{OH} = -50\mu A$ $I_{OH} = -50\mu A$ $I_{OH} = -4mA$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	$I_{OL} = 50\mu A$ $I_{OL} = 50\mu A$ $I_{OL} = 4mA$	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
l <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = 5.5V or GND	3.6			±0.1		±1.0	μΑ
Icc	Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	3.6			2.0		20.0	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$ )

				T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C			
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay CP to O or O	V <sub>CC</sub> = 2.7V	$C_L = 15pF$ $C_L = 50pF$		7.3 9.8	15.0 18.5	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 3.3 \pm 0.3 V$	$C_L = 15pF$ $C_L = 50pF$		5.7 8.2	9.7 13.2	1.0 1.0	11.5 15.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay SD or CD to O or O	V <sub>CC</sub> = 2.7V	$C_L = 15pF$ $C_L = 50pF$		8.4 10.9	15.6 19.1	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 3.3 \pm 0.3 V$	$C_L = 15pF$ $C_L = 50pF$		6.6 9.1	10.1 13.6	1.0 1.0	12.0 15.5	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)	V <sub>CC</sub> = 2.7V	$C_L = 15pF$ $C_L = 50pF$	55 45	135 60		50 40		MHz
		$V_{CC} = 3.3 \pm 0.3 V$	$C_L = 15pF$ $C_L = 50pF$	95 60	145 85		80 50		
t <sub>OSHL</sub>	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7V$ $V_{CC} = 3.3 \pm 0.3V$	$C_L = 50pF$ $C_L = 50pF$			1.5 1.5		1.5 1.5	ns

Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

# **TIMING REQUIREMENTS** (Input $t_f = t_f = 3.0 \text{ns}$ )

		V <sub>CC</sub> Guaranteed Limit		d Limit	
Symbol	Parameter	V	T <sub>A</sub> = 25°C	T <sub>A</sub> = -40 to 85°C	Unit
t <sub>w</sub>	Minimum Pulse Width, CP	2.7V 3.3V ±0.3	8.5 6.0	10.0 7.0	ns
t <sub>w</sub>	Minimum Pulse Width, CD or SD	2.7V 3.3V ±0.3	8.5 6.0	10.0 7.0	ns
t <sub>su</sub>	Minimum Setup Time, D to CP	2.7V 3.3V ±0.3	8.0 5.5	9.5 6.5	ns
t <sub>h</sub>	Minimum Hold Time, D to CP	2.7V 3.3V ±0.3	0.5 0.5	0.5 0.5	ns
t <sub>rec</sub>	Minimum Recovery Time, SD or CD to CP	2.7V 3.3V ±0.3	6.5 5.0	7.5 5.0	ns

# **CAPACITIVE CHARACTERISTICS**

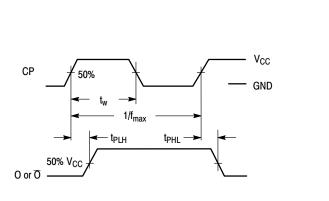
		T <sub>A</sub> = 25°C		T <sub>A</sub> = -40 to 85°C			
Symbol	Parameter	Min	Тур	Max	Min	Max	Unit
Cin	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 2)		25				pF

C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/2 (per flip–flop). C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

# **NOISE CHARACTERISTICS** (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

		T <sub>A</sub> = 25°C			
Symbol	Characteristic	Тур	Max	Unit	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.3	0.5	V	
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-0.3	-0.5	V	
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		2.0	V	
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.8	V	

# **SWITCHING WAVEFORMS**



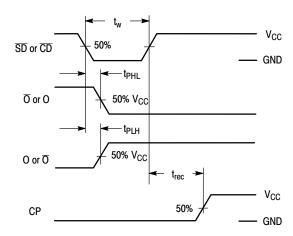


Figure 2.

Figure 3.

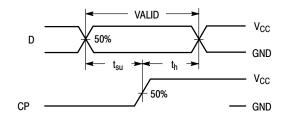
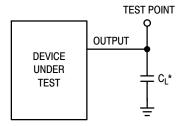


Figure 4.

# **TEST CIRCUIT**



\*Includes all probe and jig capacitance

Figure 5.

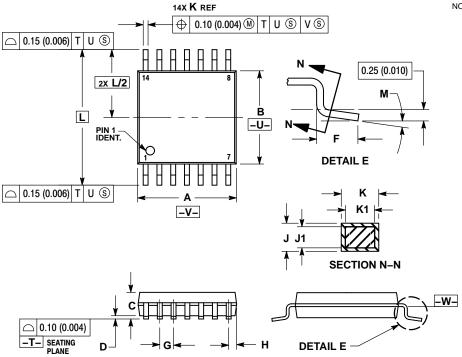
# **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74LVX74DR2G	SOIC-14 NB (Pb-Free)	2500 Tape & Reel
MC74LVX74DTG	TSSOP-14 (Pb-Free)	96 Units / Rail
MC74LVX74DTR2G	TSSOP-14 (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

# TSSOP-14 CASE 948G **ISSUE B**



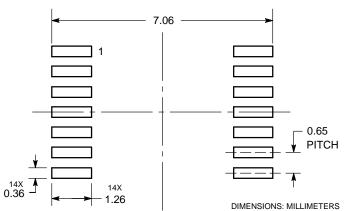
- NOTES:
  1. DIMENSIONING AND TOLERANCING PER

  - 1. DIMENSIONING AND TOLERANCING PER
    ANSI Y14.5M, 1982.
    2. CONTROLLING DIMENSION: MILLIMETER.
    3. DIMENSION A DOES NOT INCLUDE MOLD
    FLASH, PROTRUSIONS OR GATE BURRS.
    MOLD FLASH OR GATE BURRS SHALL NOT
    EXCEED 0.15 (0.006) PER SIDE.
    4. DIMENSION B DOES NOT INCLUDE
    INTERLEAD FLASH OR PROTRUSION.
    INTERLEAD FLASH OR PROTRUSION SHALL
    NOT EXCEED 0.25 (0.010) PER SIDE.
    5. DIMENSION K DOES NOT INCLUDE DAMBAR
    PROTRUSION. ALLOWABLE DAMBAR
    PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
    EXCESS OF THE K DIMENSION AT MAXIMUM
    MATERIAL CONDITION.
    6. TERMINAL NUMBERS ARE SHOWN FOR
    REFERENCE ONLY.
    7. DIMENSION A AND B ARE TO BE
    DETERMINED AT DATUM PLANE -W-.

    MILLIMETERS INCHES

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
٦	6.40		0.252 BSC		
М	0 °	8 °	0°	8 °	

# **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

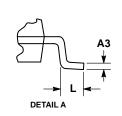
# SOIC-14 NB CASE 751A-03 ISSUE K

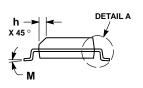
В

0.25 M C A S B S

C SEATING PLANE

13X **b** 

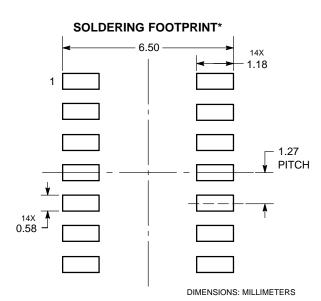




#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS.
- 3. DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION
- SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
- 5. MAXIMUM MOLD PROTRUSION 0.15 PER

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	1.35	1.75	0.054	0.068	
A1	0.10	0.25	0.004	0.010	
А3	0.19	0.25	0.008	0.010	
b	0.35	0.49	0.014	0.019	
D	8.55	8.75	0.337	0.344	
Е	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050	BSC	
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.019	
L	0.40	1.25	0.016	0.049	
м	0 °	7 °	0 °	7 °	



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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CY74FCT16374CTPACT MC74HC11ADR2G 74LVT74D,118 74VHCT9273FT(BJ) MM74HC374WM 74ALVCH162374PAG
TC7WZ74FK,LJ(CT CD54HCT273F HMC853LC3TR HMC723LC3CTR MM74HCT574MTCX MM74HCT273WM SN74LVC74APW
SN74LVC74AD MC74HC73ADTR2G MC74HC11ADG SN74ALVTH16374GR M74HCT273B1R M74HC377RM13TR
M74HC374RM13TR M74HC175B1R M74HC174RM13TR 74ALVTH16374ZQLR 74ALVTH32374ZKER 74AUP1G74DC,125
74VHC374FT(BJ) 74VHC9273FT(BJ) NLV14013BCPG