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Kind regards,

Team Nexperia

DATA SHEET

74ALVCH16825 18-bit buffer/driver (3-State)

Product specification

1998 Jul 27

IC24 Data Handbook

18-bit buffer/driver (3-State)

74ALVCH16825

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50 Ω transmission lines @ 85°C

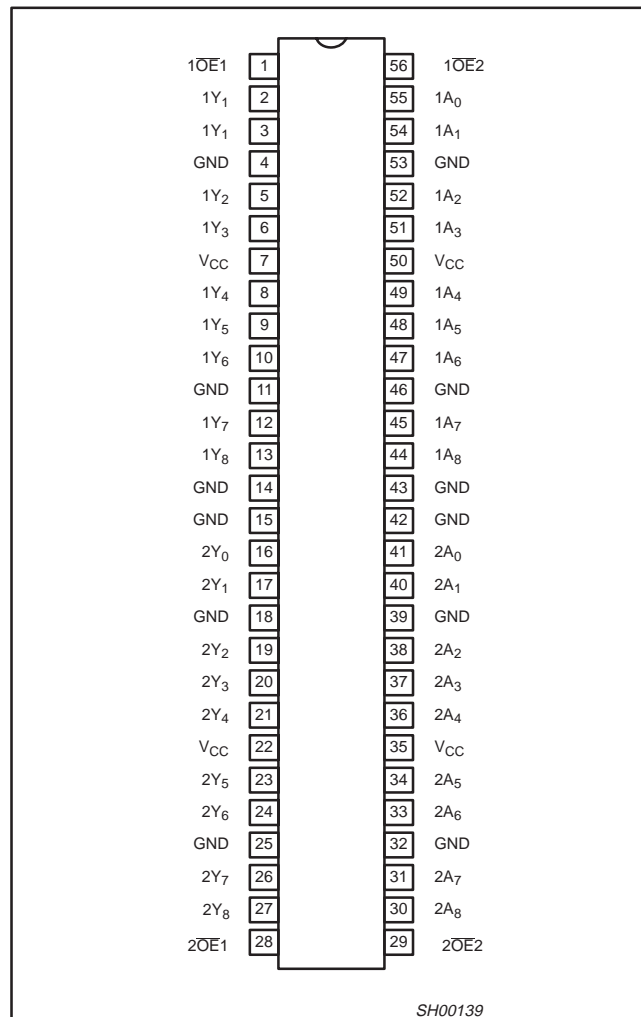
DESCRIPTION

The 74ALVCH16825 is an 18-bit non-inverting buffer/driver with 3-State outputs for bus-oriented applications.

The 74ALVCH16825 consists of two 9-bit sections with separate output enable signals. For either 9-bit buffer section, the two output enable ($1\overline{OE}1$ and $1\overline{OE}2$ or $2\overline{OE}1$ and $2\overline{OE}2$) inputs must both be LOW for corresponding D outputs to be active. If either output enable input is HIGH, the outputs of that 9-buffer section are in the high impedance state.

The 74ALVCH16825 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	$V_{CC} = 2.5\text{V}$, $C_L = 30\text{pF}$ $V_{CC} = 3.3\text{V}$, $C_L = 50\text{pF}$	2.0 2.0	ns
C_I	Input capacitance		4.0	pF
C_{PD}	Power dissipation capacitance per latch	$V_I = \text{GND to } V_{CC}^1$	Output enabled 19 Output disabled 3	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where: } f_i = \text{input frequency in MHz; } C_L = \text{output load capacitance in pF;}$$

$$f_o = \text{output frequency in MHz; } V_{CC} = \text{supply voltage in V; } \sum (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$$

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	-40°C to $+85^{\circ}\text{C}$	74ALVCH16825 DGG	ACH16825 DGG	SOT364-1

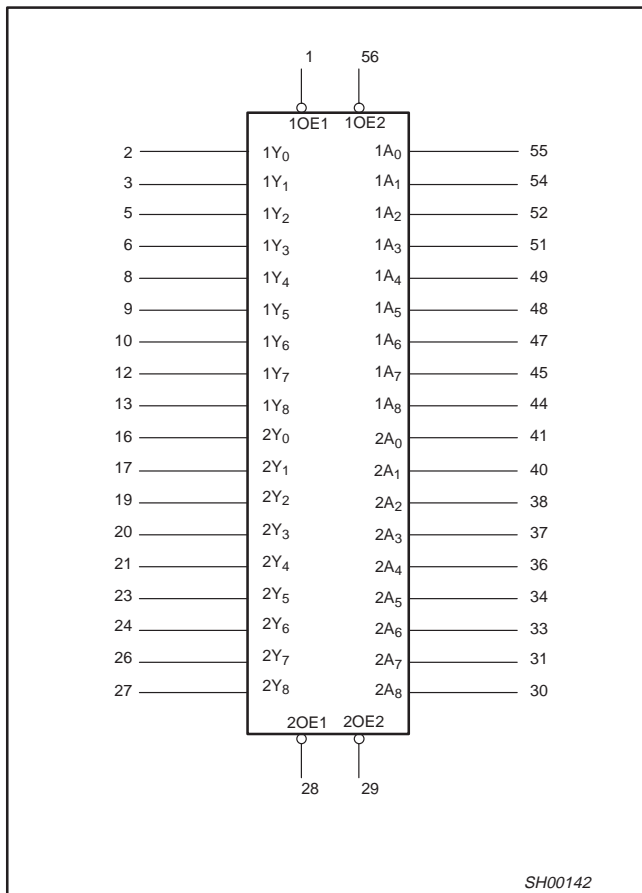
18-bit buffer/driver (3-State)

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}1$	Output enable input (active LOW)
56	$1\overline{OE}2$	
55, 54, 52, 51, 49, 48, 47, 45, 44	1A0 to 1A8	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13	1Y0 to 1Y8	Data outputs
4, 11, 14, 15, 18, 25, 32, 39, 42, 43, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
28	$2\overline{OE}1$	Output enable input (active LOW)
29	$2\overline{OE}2$	
43, 42, 41, 40, 38, 37, 36, 34, 33, 31	2A0 to 2A8	Data inputs
16, 17, 19, 20, 21, 23, 24, 26, 27	2Y0 to 2Y8	Data outputs

LOGIC SYMBOL

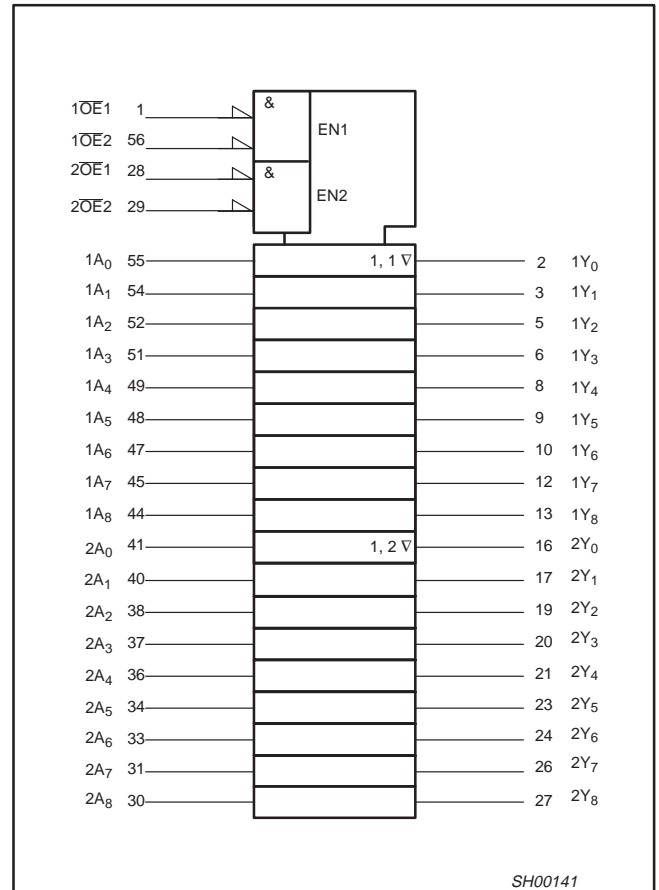


FUNCTION TABLE

INPUTS			OUTPUT Y
$n\overline{OE}1$	$n\overline{OE}2$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 Z = High impedance "off" state

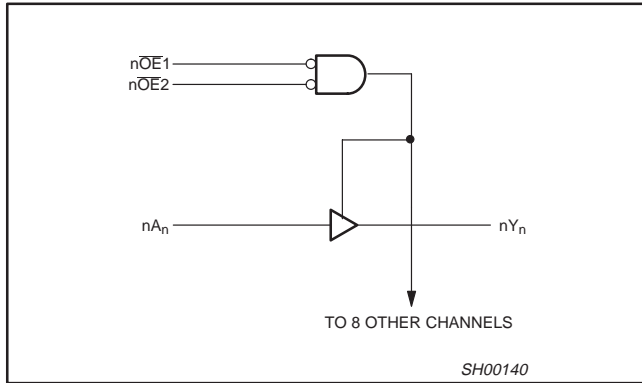
LOGIC SYMBOL (IEEE/IEC)



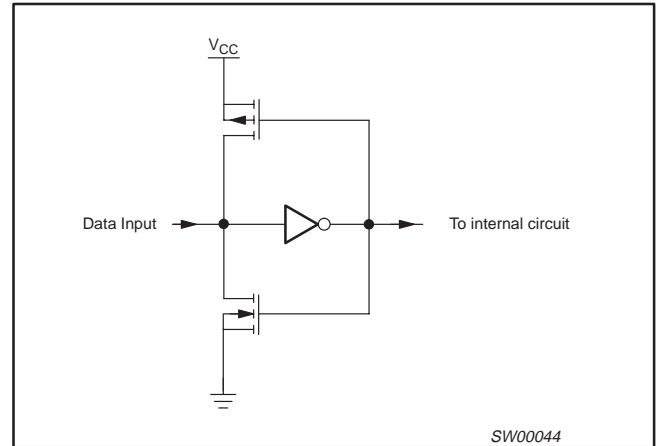
18-bit buffer/driver (3-State)

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LOGIC DIAGRAM



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V _{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V _I	DC Input voltage range		0	V _{CC}	V
V _O	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating free-air temperature range		-40	+85	°C
t _r , t _f	Input rise and fall times	V _{CC} = 2.3 to 3.0V V _{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
 Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage	For control pins ²	-0.5 to +4.6	V
		For data inputs ²	-0.5 to V _{CC} +0.5	
I _{OK}	DC output diode current	V _O > V _{CC} or V _O < 0	± 50	mA
V _O	DC output voltage	Note 2	-0.5 to V _{CC} +0.5	V
I _O	DC output source or sink current	V _O = 0 to V _{CC}	± 50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		± 100	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package -plastic medium-shrink (SSOP) -plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C	850	mW
		above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	600	

NOTE:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

18-bit buffer/driver (3-State)

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 2.3 to 2.7V	1.7	1.2		V
		V _{CC} = 2.7 to 3.6V	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{CC} = 2.3 to 2.7V		1.2	0.7	V
		V _{CC} = 2.7 to 3.6V		1.5	0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -6mA	V _{CC} -0.3	V _{CC} -0.08		
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} -0.6	V _{CC} -0.26		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} -0.5	V _{CC} -0.14		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} -0.6	V _{CC} -0.09		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} -1.0	V _{CC} -0.28		
V _{OL}	LOW level output voltage	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.07	0.40	V
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.15	0.70	V
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.14	0.40	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA		0.27	0.55	
I _I	Input leakage current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND		0.1	5	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 2.3 to 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	10	μA
I _{CC}	Quiescent supply current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND; I _O = 0		0.2	40	μA
ΔI _{CC}	Additional quiescent supply current	V _{CC} = 2.3V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		150	750	μA
I _{BHL} ²	Bus hold LOW sustaining current	V _{CC} = 2.3V; V _I = 0.7V	45	-		μA
		V _{CC} = 3.0V; V _I = 0.8V	75	150		
I _{BHH} ²	Bus hold HIGH sustaining current	V _{CC} = 2.3V; V _I = 1.7V	-45			μA
		V _{CC} = 3.0V; V _I = 2.0V	-75	-175		
I _{BHLO} ²	Bus hold LOW overdrive current	V _{CC} = 3.6V	500			μA
I _{BHHO} ²	Bus hold HIGH overdrive current	V _{CC} = 3.6V	-500			μA

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

18-bit buffer/driver (3-State)

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AC CHARACTERISTICS FOR $V_{CC} = 2.3V$ TO $2.7V$ RANGE

GND = 0V; $t_r = t_f \leq 2.0ns$; $C_L = 30pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.3$ to $2.7V$			
			MIN	TYP ¹	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA_n to nY_n	1, 3	1.0	2.0	4.1	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nY_n	2, 3	1.0	2.9	6.0	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nY_n	2,3	1.2	2.2	5.6	ns

NOTE:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

AC CHARACTERISTICS FOR $V_{CC} = 3.0V$ TO $3.6V$ RANGE AND $V_{CC} = 2.7V$

GND = 0V; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			$V_{CC} = 3.3 \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP ^{1, 2}	MAX	MIN	TYP ¹	MAX	
t_{PHL}/t_{PLH}	Propagation delay nA_n to nY_n	1, 3	1.0	2.0	3.4	1.0	2.1	3.9	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nY_n	2, 3	1.0	2.8	4.7	1.0	2.9	5.7	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nY_n	2, 3	1.3	2.9	4.5	1.3	3.0	4.9	ns

NOTES:

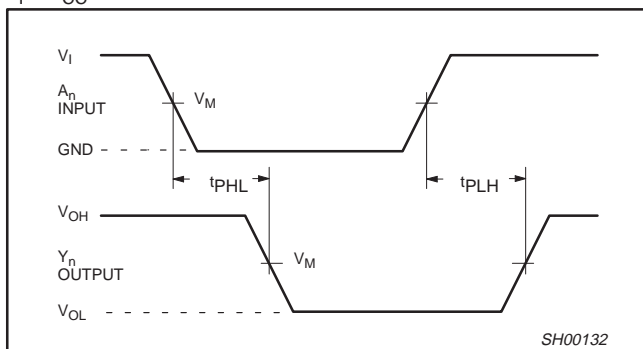
- All typical values are measured $T_{amb} = 25^\circ C$.
- Typical value is measured at $V_{CC} = 3.3V$

AC WAVEFORMS FOR $V_{CC} = 2.3V$ TO $2.7V$ AND $V_{CC} < 2.3V$ RANGE

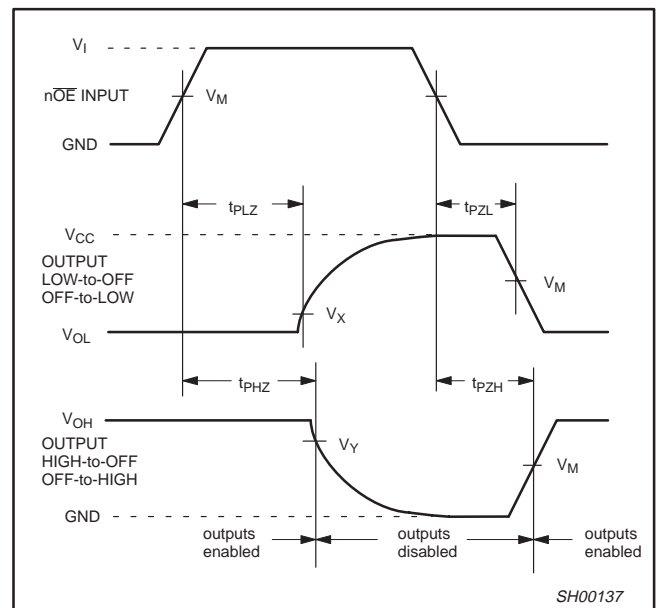
$V_M = 0.5 V_{CC}$
 $V_X = V_{OL} + 0.15V$
 $V_Y = V_{OH} - 0.15V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

AC WAVEFORMS FOR $V_{CC} = 3.0V$ TO $3.6V$ AND $V_{CC} = 2.7V$ RANGE

$V_M = 1.5 V$
 $V_X = V_{OL} + 0.3V$
 $V_Y = V_{OH} - 0.3V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = 2.7V$
 $V_I = V_{CC}$



Waveform 1. Input (Dn) to output (Yn) propagation delay

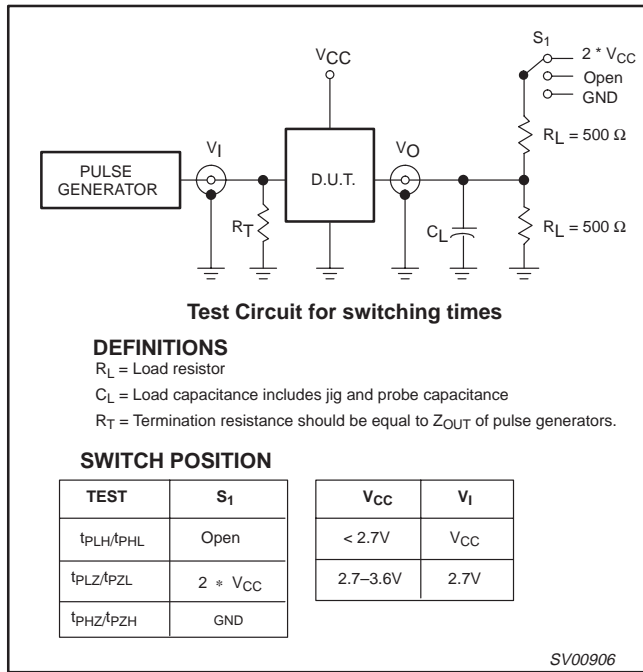


Waveform 2. 3-State enable and disable times

18-bit buffer/driver (3-State)

74ALVCH16825

TEST CIRCUIT



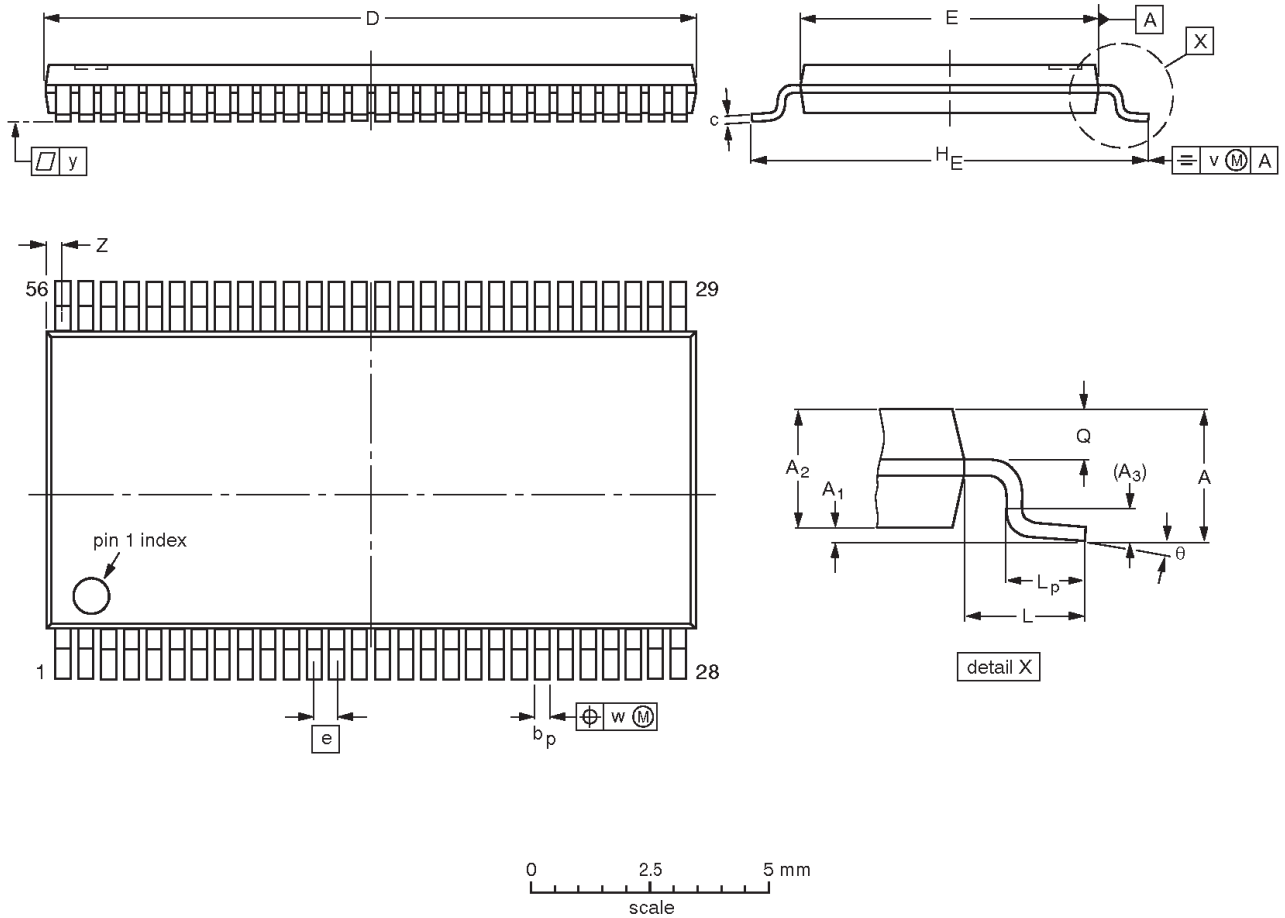
Waveform 3. Load circuitry for switching times

18-bit buffer/driver (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				93-02-03 95-02-10

18-bit buffer/driver (3-State)

74ALVCH16825

NOTES

18-bit buffer/driver (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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