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Kind regards,

Team Nexperia

# 74ALVT16823

18-bit bus-interface D-type flip-flop with reset and enable;  
3-state

Rev. 04 — 2 August 2005

Product data sheet

## 1. General description

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The 74ALVT16823 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ALVT16823 has two 9-bit wide buffered registers with clock enable (pin  $n\overline{CE}$ ) and master reset (pin  $n\overline{MR}$ ) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding Q output of the flip-flop.

It is designed for  $V_{CC}$  operation from 2.5 V to 3.0 V with I/O compatibility to 5 V.

## 2. Features

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- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- 5 V I/O compatible
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- Power-up reset
- No bus current loading when output is tied to 5 V bus
- Output capability: +64 mA to -32 mA
- Latch-up protection:
  - ◆ JESD78: exceeds 500 mA
- ESD protection:
  - ◆ MIL STD 883, method 3015: exceeds 2000 V
  - ◆ Machine Model: exceeds 200 V

**PHILIPS**

### 3. Quick reference data

**Table 1: Quick reference data**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>PLH</sub>	propagation delay nCP to nQx	C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 2.5 V	1.5	2.9	4.5	ns
		C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 3.3 V	1.0	2.3	3.1	ns
t <sub>PHL</sub>	propagation delay nCP to nQx	C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 2.5 V	1.4	2.7	4.2	ns
		C <sub>L</sub> = 50 pF; V <sub>CC</sub> = 3.3 V	1.0	2.1	2.9	ns
C <sub>i</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	3	-	pF
C <sub>o</sub>	output capacitance	V <sub>I/O</sub> = 0 V or V <sub>CC</sub>	-	9	-	pF
I <sub>CC</sub>	quiescent supply current	outputs disabled; V <sub>CC</sub> = 2.5 V	-	40	-	μA
		outputs disabled; V <sub>CC</sub> = 3.3 V	-	70	-	μA

### 4. Ordering information

**Table 2: Ordering information**

Type number	Package			Version
	temperature range	Name	Description	
74ALVT16823DL	-40 °C to +85 °C	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1
74ALVT16823DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

5. Functional diagram

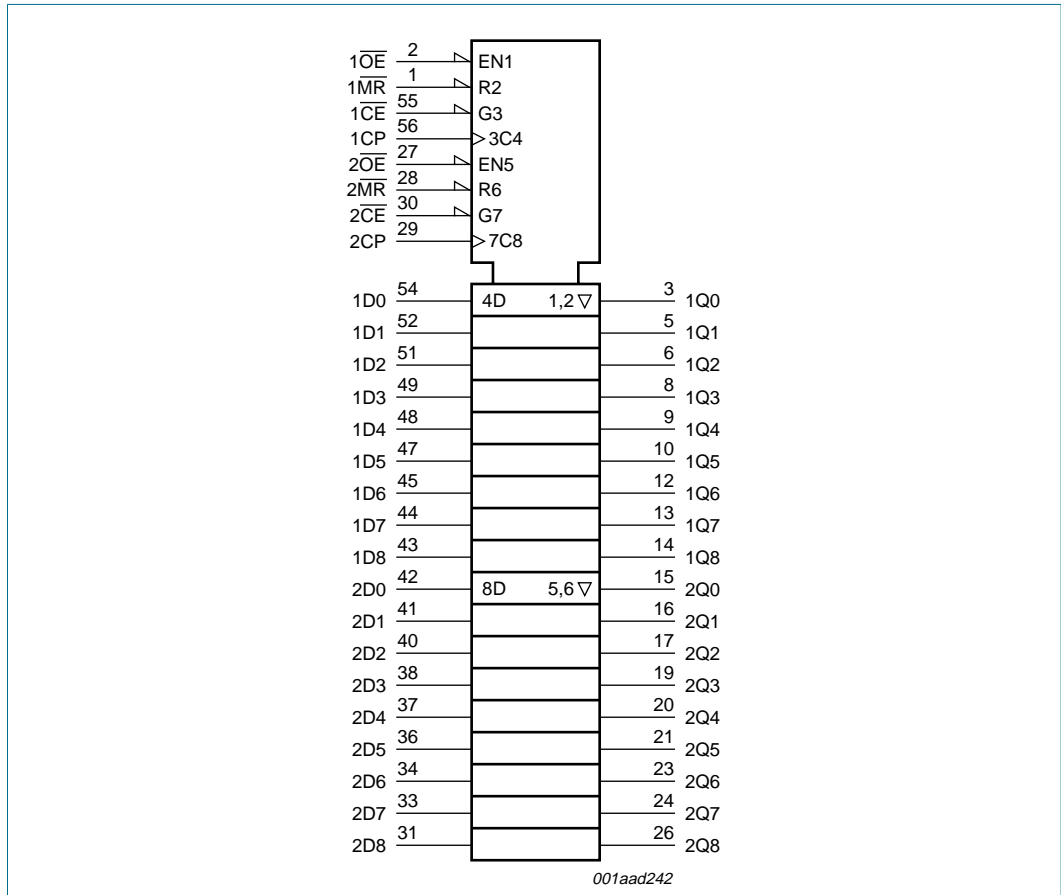


Fig 1. IEC logic symbol

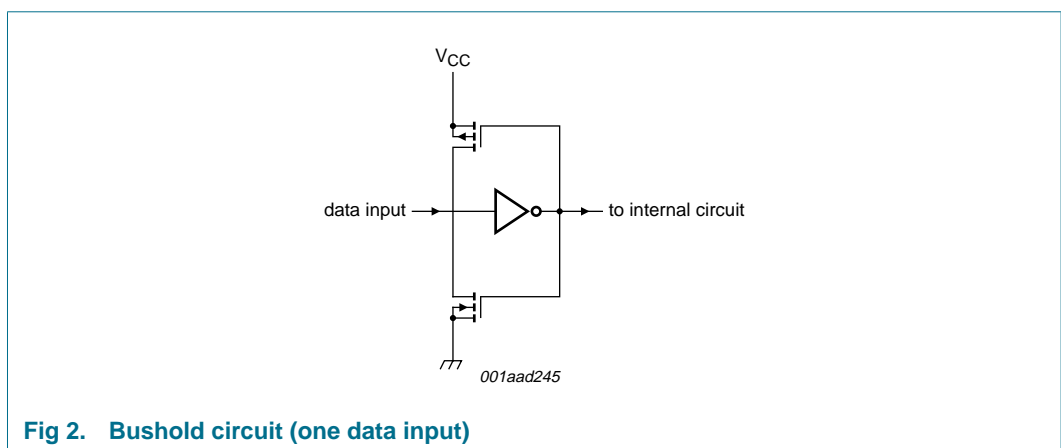


Fig 2. Bushold circuit (one data input)

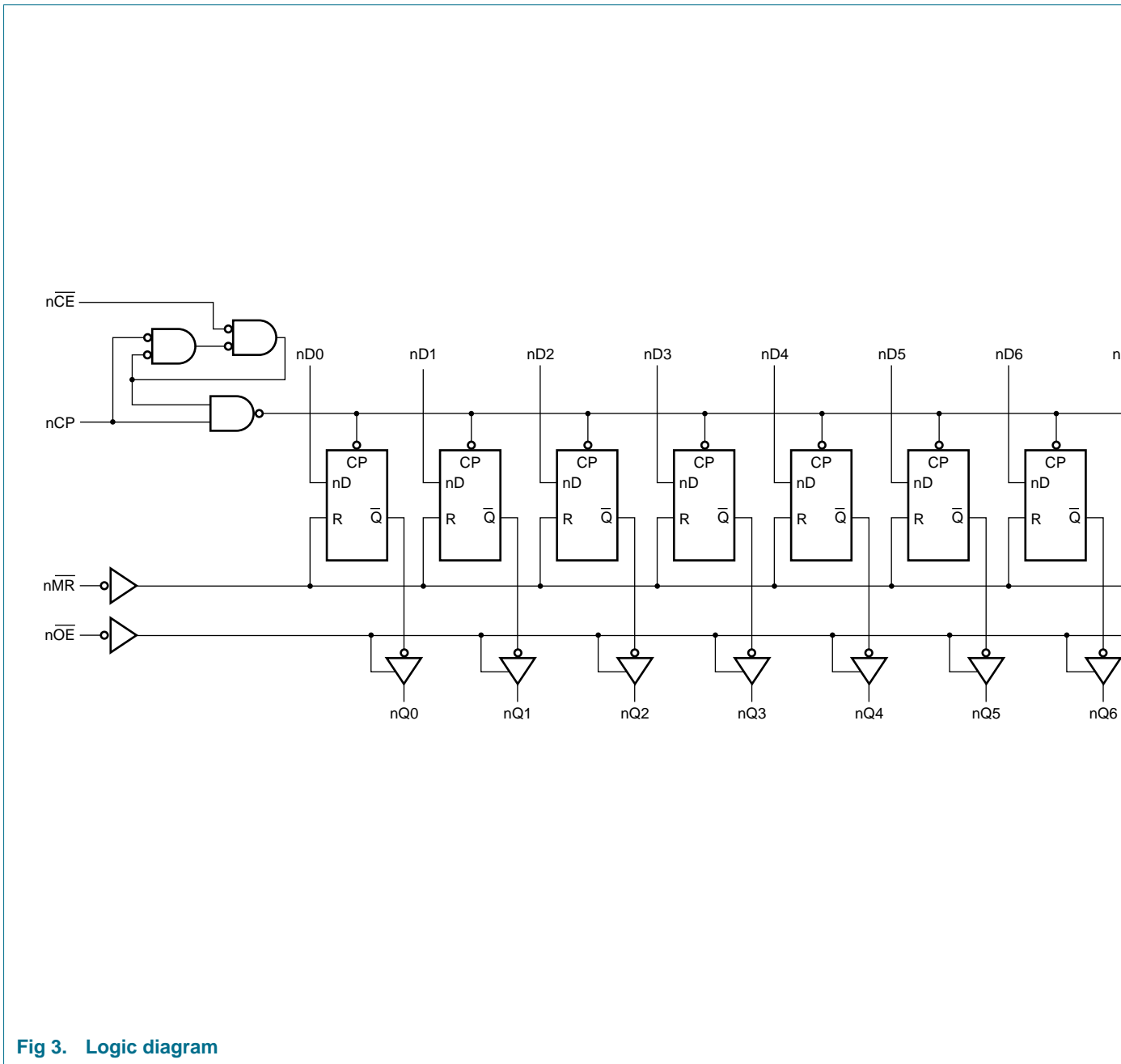
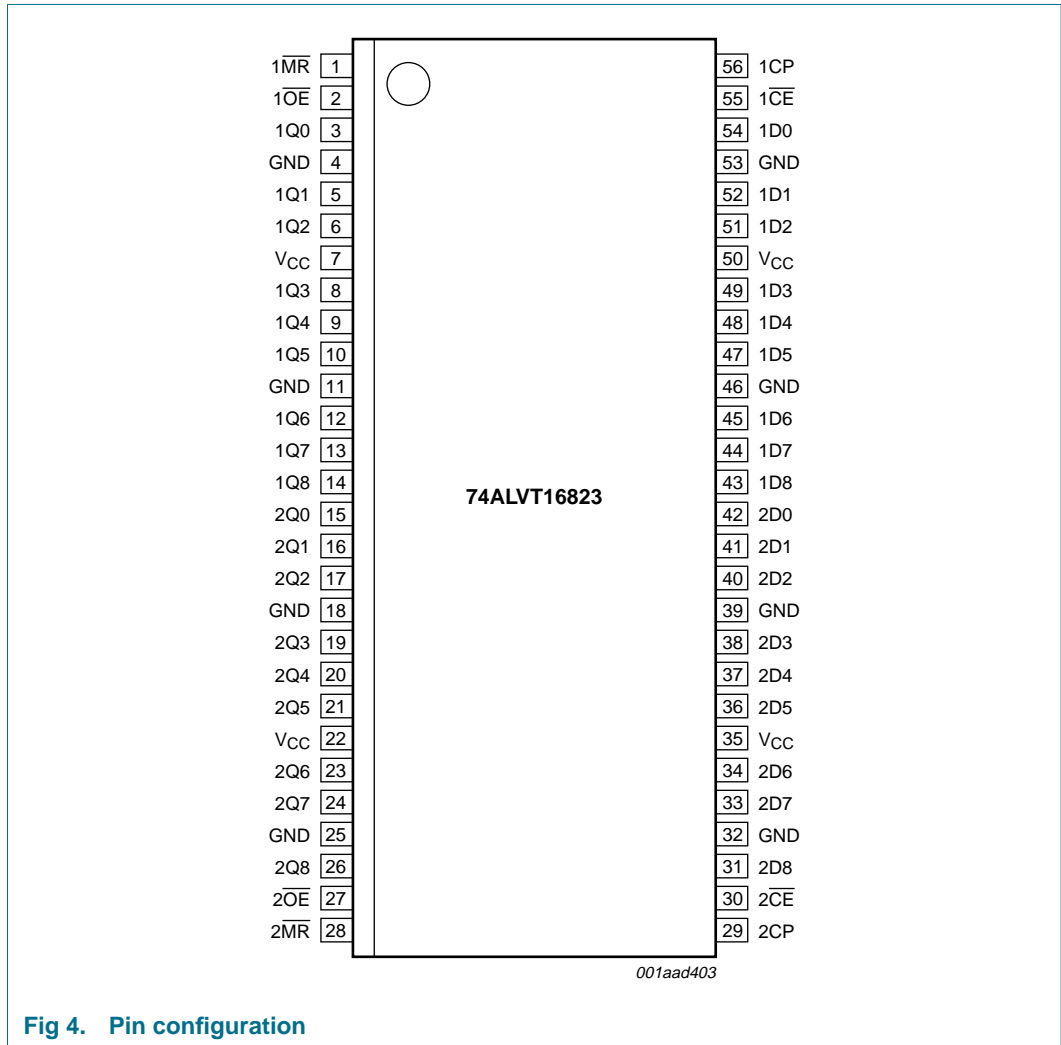


Fig 3. Logic diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1MR	1	1 master reset input (active-LOW)
1OE	2	1 output enable input (active-LOW)
1Q0	3	1 data output 0
GND	4	ground (0 V)
1Q1	5	1 data output 1
1Q2	6	1 data output 2
V <sub>CC</sub>	7	supply voltage
1Q3	8	1 data output 3

Table 3: Pin description ...continued

Symbol	Pin	Description
1Q4	9	1 data output 4
1Q5	10	1 data output 5
GND	11	ground (0 V)
1Q6	12	1 data output 6
1Q7	13	1 data output 7
1Q8	14	1 data output 8
2Q0	15	2 data output 0
2Q1	16	2 data output 1
2Q2	17	2 data output 2
GND	18	ground (0 V)
2Q3	19	2 data output 3
2Q4	20	2 data output 4
2Q5	21	2 data output 5
V <sub>CC</sub>	22	supply voltage
2Q6	23	2 data output 6
2Q7	24	2 data output 7
GND	25	ground (0 V)
2Q8	26	2 data output 8
2 $\overline{OE}$	27	2 output enable input (active-LOW)
2 $\overline{MR}$	28	2 master reset input (active-LOW)
2CP	29	2 clock pulse input (active rising edge)
2 $\overline{CE}$	30	2 clock enable input (active-LOW)
2D8	31	2 data input 8
GND	32	ground (0 V)
2D7	33	2 data input 7
2D6	34	2 data input 6
V <sub>CC</sub>	35	supply voltage
2D5	36	2 data input 5
2D4	37	2 data input 4
2D3	38	2 data input 3
GND	39	ground (0 V)
2D2	40	2 data input 2
2D1	41	2 data input 1
2D0	42	2 data input 0
1D8	43	1 data input 8
1D7	44	1 data input 7
1D6	45	1 data input 6
GND	46	ground (0 V)
1D5	47	1 data input 5
1D4	48	1 data input 4
1D3	49	1 data input 3

Table 3: Pin description ...continued

Symbol	Pin	Description
V <sub>CC</sub>	50	supply voltage
1D2	51	1 data input 2
1D1	52	1 data input 1
GND	53	ground (0 V)
1D0	54	1 data input 0
1 $\overline{\text{CE}}$	55	1 clock enable input (active-LOW)
1CP	56	1 clock pulse input (active rising edge)

## 7. Functional description

### 7.1 Function table

Table 4: Function table

Operating mode	Input					Output
	n $\overline{\text{OE}}$	n $\overline{\text{MR}}$	n $\overline{\text{CE}}$	nCP	nDx	nQx
clear	L	L	X	X	X	L
load and read data	L	H	L	$\uparrow$	h	H
					l	L
hold	L	H	H	$\uparrow$	X	NC
high-impedance	H	X	X	X	X	Z

- [1] H = HIGH voltage level;  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
L = LOW voltage level;  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;  
NC = no change;  
X = don't care;  
Z = high-impedance OFF-state;  
 $\uparrow$  = LOW-to-HIGH clock transition;  
 $\uparrow$  = not a LOW-to-HIGH clock transition.

## 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage		[1] -0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output diode current	V <sub>O</sub> < 0 V	-50	-	mA



**Table 5: Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		[2]	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>V<sub>CC</sub> = 2.5 V</b>						
V <sub>CC</sub>	supply voltage		2.3	-	2.7	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>IH</sub>	HIGH-level input voltage		1.7	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.7	V
I <sub>OH</sub>	HIGH-level output current		-	-	-8	mA
I <sub>OL</sub>	LOW-level output current	none	-	-	8	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	24	mA
Δt/Δv	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C
<b>V<sub>CC</sub> = 3.3 V</b>						
V <sub>CC</sub>	supply voltage		3.0	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-	-	-32	mA
I <sub>OL</sub>	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
Δt/Δv	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C

## 10. Static characteristics

**Table 7: Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b><math>V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}</math> [1]</b>							
$V_{IK}$	input clamping voltage	$V_{CC} = 2.3\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V	
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC}$	-	V	
		$V_{CC} = 2.3\text{ V}$ ; $I_{OH} = -8\text{ mA}$	1.8	2.5	-	V	
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.3\text{ V}$ ; $I_{OL} = 100\text{ }\mu\text{A}$	-	0.07	0.2	V	
		$V_{CC} = 2.3\text{ V}$ ; $I_{OL} = 24\text{ mA}$	-	0.3	0.5	V	
		$V_{CC} = 2.3\text{ V}$ ; $I_{OL} = 8\text{ mA}$	-	-	0.4	V	
$V_{OL(pu)}$	power-up LOW-level output voltage	$V_{CC} = 2.7\text{ V}$ ; $I_O = 1\text{ mA}$ ; $V_I = V_{CC}$ or GND	[2] -	-	0.55	V	
$I_{LI}$	input leakage current	control pins	$V_{CC} = 2.7\text{ V}$ ; $V_I = V_{CC}$ or GND	-	0.1	$\pm 1$	$\mu\text{A}$
			$V_{CC} = 0\text{ V}$ to $2.7\text{ V}$ ; $V_I = 5.5\text{ V}$	-	0.1	10	$\mu\text{A}$
	I/O data pins	$V_{CC} = 2.7\text{ V}$ ; $V_I = V_{CC}$	[3] -	0.1	1	$\mu\text{A}$	
		$V_{CC} = 2.7\text{ V}$ ; $V_I = 0\text{ V}$	[3] -	+0.1	-5	$\mu\text{A}$	
$I_{OFF}$	off current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V}$ to $4.5\text{ V}$	-	+0.1	$\pm 100$	$\mu\text{A}$	
$I_{HOLD}$	bus hold current data inputs	$V_{CC} = 2.3\text{ V}$ ; $V_I = 0.7\text{ V}$	[4] -	100	-	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V}$ ; $V_I = 1.7\text{ V}$	[4] -	-70	-	$\mu\text{A}$	
$I_{EX}$	external current into output	output HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}$ ; $V_{CC} = 2.3\text{ V}$	-	10	125	$\mu\text{A}$	
$I_{PU}$	power-up 3-state output current	$V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V}$ to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$	[5] -	1	$\pm 100$	$\mu\text{A}$	
$I_{PD}$	power-down 3-state output current	$V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V}$ to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$	[5] -	1	$\pm 100$	$\mu\text{A}$	
$I_{OZ}$	3-state output current	$V_{CC} = 2.7\text{ V}$ ; $V_I = V_{IL}$ or $V_{IH}$					
		output HIGH state; $V_O = 2.3\text{ V}$	-	0.5	5	$\mu\text{A}$	
		output LOW-state; $V_O = 0.5\text{ V}$	-	+0.5	-5	$\mu\text{A}$	
$I_{CC}$	quiescent supply current	$V_{CC} = 2.7\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $I_O = 0\text{ A}$					
		outputs HIGH-state	-	0.04	0.1	mA	
		outputs LOW-state	-	2.7	4.5	mA	
		outputs disabled	[6] -	0.04	0.1	mA	
$\Delta I_{CC}$	additional quiescent supply current per input pin	$V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ , other inputs at $V_{CC}$ or GND	[7] -	0.04	0.4	mA	
$C_I$	input capacitance	$V_I = 0\text{ V}$ or $V_{CC}$	-	3	-	pF	
$C_O$	output capacitance	$V_{I/O} = 0\text{ V}$ or $3.0\text{ V}$	-	9	-	pF	
<b><math>V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}</math> [8]</b>							
$V_{IK}$	input clamping voltage	$V_{CC} = 3.0\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-	-0.85	-1.2	V	
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC}$	-	V	
		$V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -32\text{ mA}$	2.0	2.3	-	V	

**Table 7: Static characteristics ...continued**At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 100 μA	-	0.07	0.2	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA	-	0.25	0.4	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 32 mA	-	0.3	0.5	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 64 mA	-	0.4	0.55	V
V <sub>OL(pu)</sub>	power-up LOW-level output voltage	V <sub>CC</sub> = 3.6 V; I <sub>O</sub> = 1 mA; V <sub>I</sub> = V <sub>CC</sub> or GND	[2] -	-	0.55	V
I <sub>LI</sub>	input leakage current	control pins				
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	±1	μA
		V <sub>CC</sub> = 0 V or 3.6 V; V <sub>I</sub> = 5.5 V	-	0.1	10	μA
	I/O data pins	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub>	[3] -	0.5	1	μA
	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V	[3] -	+0.1	-5	μA	
I <sub>OFF</sub>	off current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.5 V	-	0.1	±100	μA
I <sub>HOLD</sub>	bus hold current data inputs	V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V	75	130	-	μA
		V <sub>CC</sub> = 3 V; V <sub>I</sub> = 2.0 V	-75	-140	-	μA
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0V to 3.6 V	[9] ±500	-	-	μA
I <sub>EX</sub>	external current into output	output HIGH-state when V <sub>O</sub> > V <sub>CC</sub> ; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 3.0 V	-	10	125	μA
I <sub>PU</sub>	power-up 3-state output current	V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub>	[10] -	1	±100	μA
I <sub>PD</sub>	power-down 3-state output current	V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub>	[10] -	1	±100	μA
I <sub>OZ</sub>	3-state output current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>				
		output HIGH state; V <sub>O</sub> = 3.0 V	-	0.5	5	μA
		output LOW-state; V <sub>O</sub> = 0.5 V	-	+0.5	-5	μA
I <sub>CC</sub>	quiescent supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A				
		outputs HIGH-state	-	0.06	0.1	mA
		outputs LOW-state	-	3.9	5.5	mA
		outputs disabled	[6] -	0.06	0.1	mA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>CC</sub> = 3 V to 3.6 V; one input at V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND	[7] -	0.04	0.4	mA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	3	-	pF
C <sub>O</sub>	output capacitance	V <sub>I/O</sub> = 0 V or 3.0 V	-	9	-	pF

[1] All typical values are at V<sub>CC</sub> = 2.5 V and T<sub>amb</sub> = 25 °C.

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at V<sub>CC</sub> or GND.

[4] Not guaranteed.

[5] This parameter is valid for any V<sub>CC</sub> between 0 V and 1.2 V with a transition time of up to 10 ms. From V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 2.5 V ± 0.2 V a transition time of 100 μs is permitted. This parameter is valid for T<sub>amb</sub> = 25 °C only.[6] I<sub>CC</sub> is measured with outputs pulled up to V<sub>CC</sub> or pulled down to ground.[7] This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.[8] All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

[9] This is the bus hold overdrive current required to force the input to the opposite logic state.

[10] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2$  V to  $V_{CC} = 3.3$  V  $\pm 0.3$  V a transition time of 100  $\mu$ s is permitted. This parameter is valid for  $T_{amb} = 25$  °C only.

## 11. Dynamic characteristics

**Table 8: Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#);

$T_{amb} = -40$  °C to  $+85$  °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>V_{CC} = 2.5</math> V <math>\pm 0.2</math> V [1]</b>						
$f_{max}$	maximum clock frequency	see <a href="#">Figure 5</a>	150	-	-	MHz
$t_{PLH}$	propagation delay nCP to nQx	see <a href="#">Figure 5</a>	1.5	2.9	4.5	ns
$t_{PHL}$	HIGH-to-LOW propagation delay					
	nCP to nQx	see <a href="#">Figure 5</a>	1.4	2.7	4.2	ns
	$\overline{nMR}$ to nQx	see <a href="#">Figure 7</a>	1.5	2.7	4.2	ns
$t_{PZH}$	output enable time to HIGH-level	see <a href="#">Figure 8</a>	2.1	3.4	5.0	ns
$t_{PZL}$	output enable time to LOW-level	see <a href="#">Figure 9</a>	1.8	3.0	4.7	ns
$t_{PHZ}$	output disable time from HIGH-level	see <a href="#">Figure 8</a>	1.7	3.0	4.3	ns
$t_{PLZ}$	output disable time from LOW-level	see <a href="#">Figure 9</a>	1.4	2.3	3.3	ns
$t_{su(H)}$	set-up time HIGH					
	nDx to nCP	see <a href="#">Figure 6</a>	1.0	0.5	-	ns
	$\overline{nCE}$ to nCP	see <a href="#">Figure 6</a>	1.0	0.2	-	ns
$t_{su(L)}$	set-up time LOW					
	nDx to nCP	see <a href="#">Figure 6</a>	1.8	1.3	-	ns
	$\overline{nCE}$ to nCP	see <a href="#">Figure 6</a>	+0.5	-0.1	-	ns
$t_{h(H)}$	hold time HIGH					
	nDx to nCP	see <a href="#">Figure 6</a>	+0.1	-1.4	-	ns
	$\overline{nCE}$ to nCP	see <a href="#">Figure 6</a>	1.0	0.2	-	ns
$t_{h(L)}$	hold time LOW					
	nDx to nCP	see <a href="#">Figure 6</a>	+0.1	-0.5	-	ns
	$\overline{nCE}$ to nCP	see <a href="#">Figure 6</a>	+1.0	-0.1	-	ns
$t_{WH}$	pulse width HIGH nCP	see <a href="#">Figure 5</a>	2.0	0.8	-	ns
$t_{WL}$	pulse width LOW					
	nCP	see <a href="#">Figure 5</a>	3.0	2.1	-	ns
	$\overline{nMR}$	see <a href="#">Figure 7</a>	2.0	0.8	-	ns
$t_{rec}$	recovery time $\overline{nMR}$ to nCP	see <a href="#">Figure 7</a>	2.0	1.3	-	ns
<b><math>V_{CC} = 3.3</math> V <math>\pm 0.3</math> V [2]</b>						
$f_{max}$	maximum clock frequency	see <a href="#">Figure 5</a>	250	-	-	MHz
$t_{PLH}$	propagation delay nCP to nQx	see <a href="#">Figure 5</a>	1.0	2.3	3.1	ns
$t_{PHL}$	HIGH-to-LOW propagation delay					
	nCP to nQx	see <a href="#">Figure 5</a>	1.0	2.1	2.9	ns
	$\overline{nMR}$ to nQx	see <a href="#">Figure 7</a>	1.0	2.3	2.9	ns
$t_{PZH}$	output enable time to HIGH-level	see <a href="#">Figure 8</a>	1.7	2.7	4.0	ns
$t_{PZL}$	output enable time to LOW-level	see <a href="#">Figure 9</a>	1.4	2.3	3.5	ns

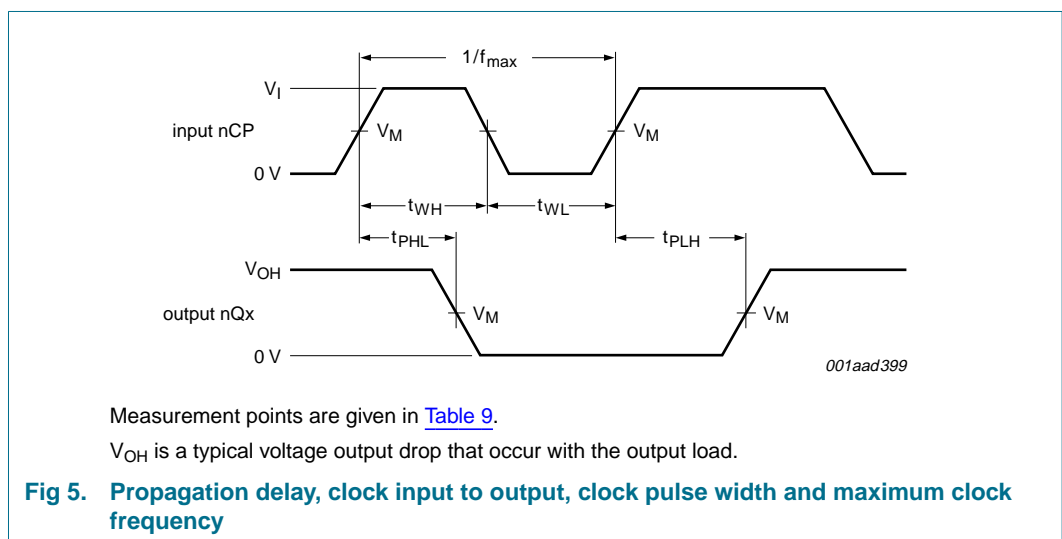
**Table 8: Dynamic characteristics ...continued**

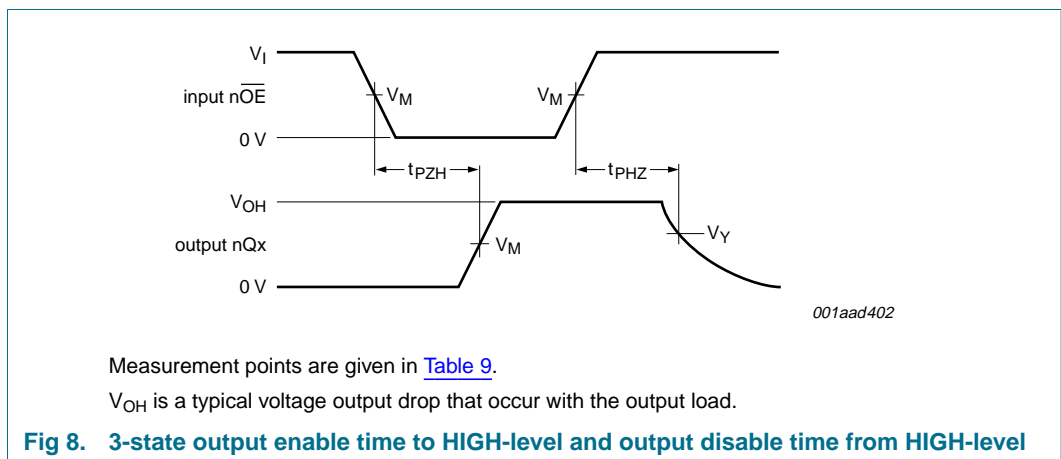
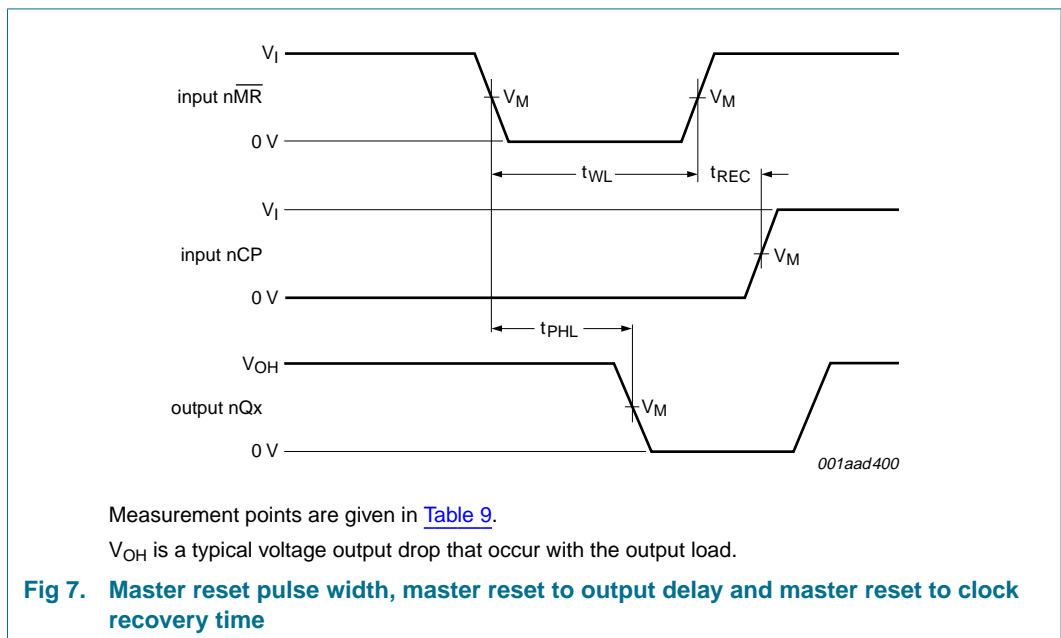
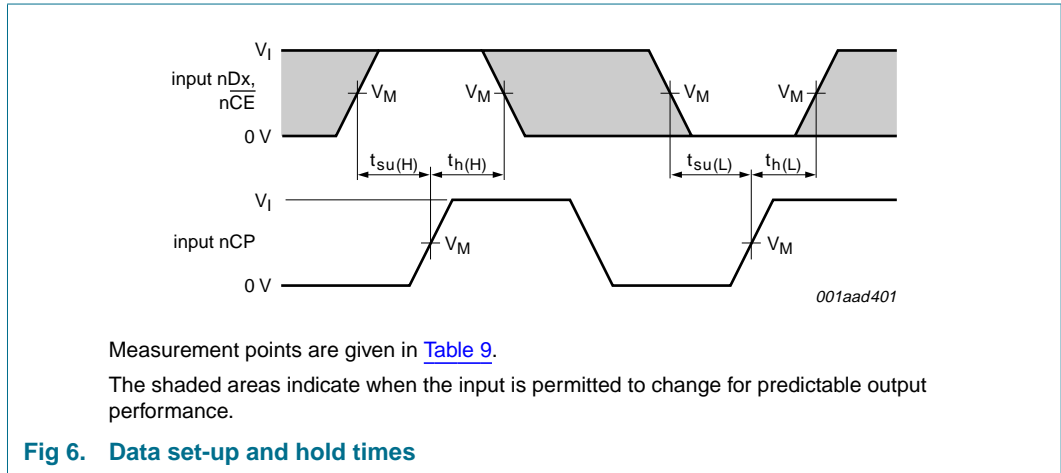
Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#);  
 $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

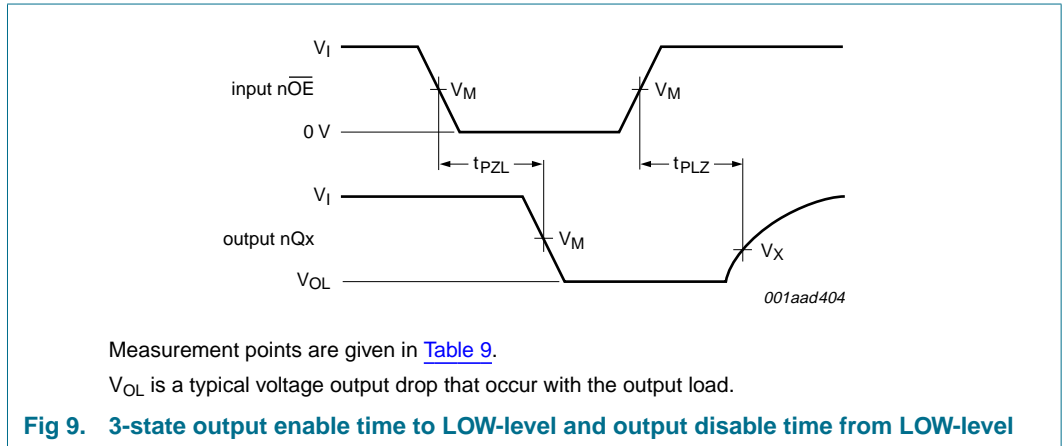
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHZ}$	output disable time from HIGH-level	see <a href="#">Figure 8</a>	2.2	3.1	4.0	ns
$t_{PLZ}$	output disable time from LOW-level	see <a href="#">Figure 9</a>	1.8	2.6	3.5	ns
$t_{su(H)}$	set-up time HIGH					
	nDx to nCP	see <a href="#">Figure 6</a>	1.0	0.5	-	ns
	$\overline{nCE}$ to nCP	see <a href="#">Figure 6</a>	1.0	0.1	-	ns
$t_{su(L)}$	set-up time LOW					
	nDx to nCP	see <a href="#">Figure 6</a>	1.6	1.1	-	ns
	$\overline{nCE}$ to nCP	see <a href="#">Figure 6</a>	+0.5	-0.5	-	ns
$t_{h(H)}$	hold time HIGH					
	nDx to nCP	see <a href="#">Figure 6</a>	+0.1	-0.7	-	ns
	$\overline{nCE}$ to nCP	see <a href="#">Figure 6</a>	1.0	0.5	-	ns
$t_{h(L)}$	hold time LOW					
	nDx to nCP	see <a href="#">Figure 6</a>	+0.1	-0.5	-	ns
	$\overline{nCE}$ to nCP	see <a href="#">Figure 6</a>	+1.0	-0.1	-	ns
$t_{WH}$	pulse width HIGH nCP	see <a href="#">Figure 5</a>	1.5	0.7	-	ns
$t_{WL}$	pulse width LOW					
	nCP	see <a href="#">Figure 5</a>	2.5	1.4	-	ns
	$\overline{nMR}$	see <a href="#">Figure 7</a>	2.0	1.5	-	ns
$t_{rec}$	recovery time $\overline{nMR}$ to nCP	see <a href="#">Figure 7</a>	2.0	1.1	-	ns

- [1] All typical values are measured at  $V_{CC} = 2.5\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .
- [2] All typical values are measured at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

## 12. Waveforms

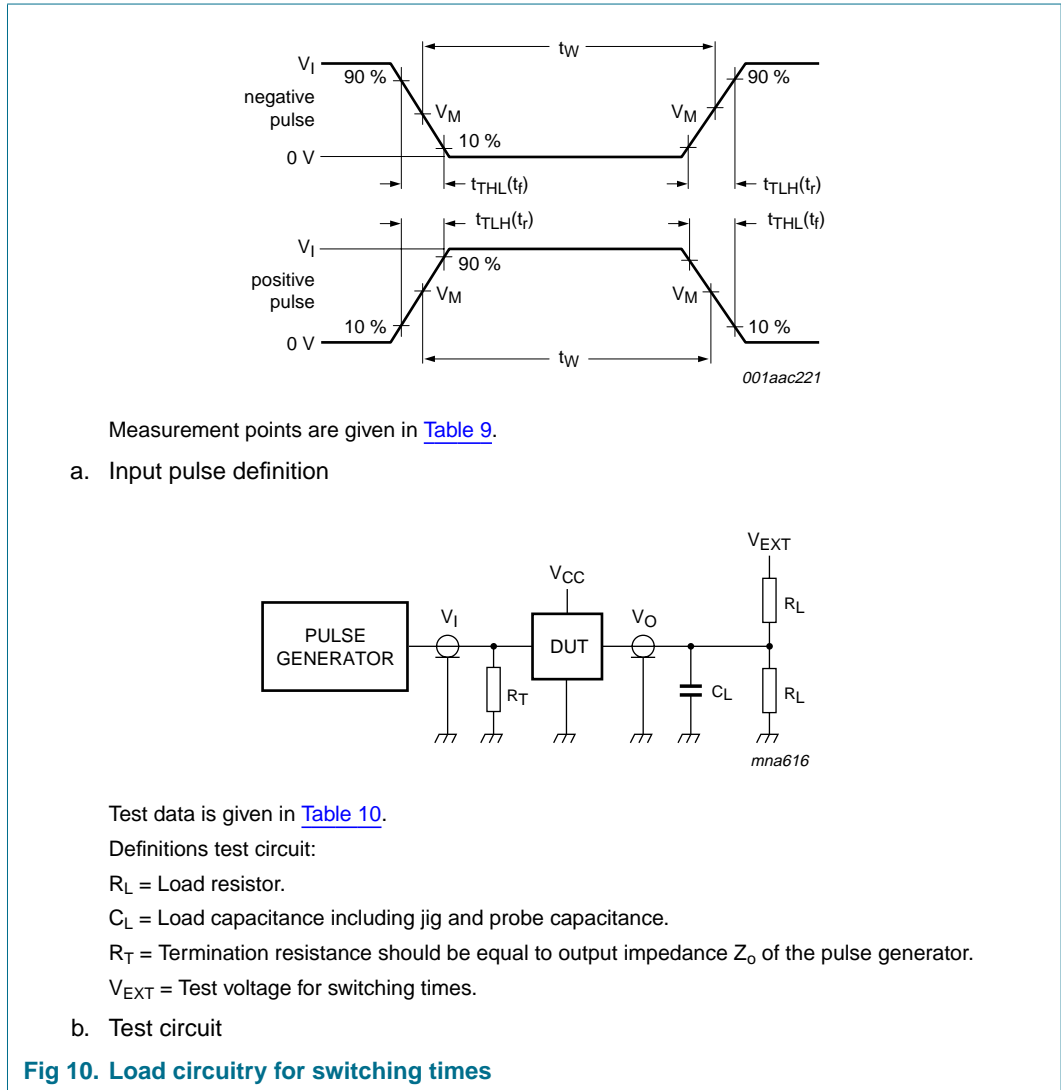






**Table 9: Measurement points**

Supply voltage	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
$\geq 3\text{ V}$	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$
$\leq 2.7\text{ V}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



**Table 10: Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$	$t_{PHZ}, t_{PZH}$
3.0 V or $V_{CC}$ whichever is less	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	6 V or $2 \times V_{CC}$	open	GND



13. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

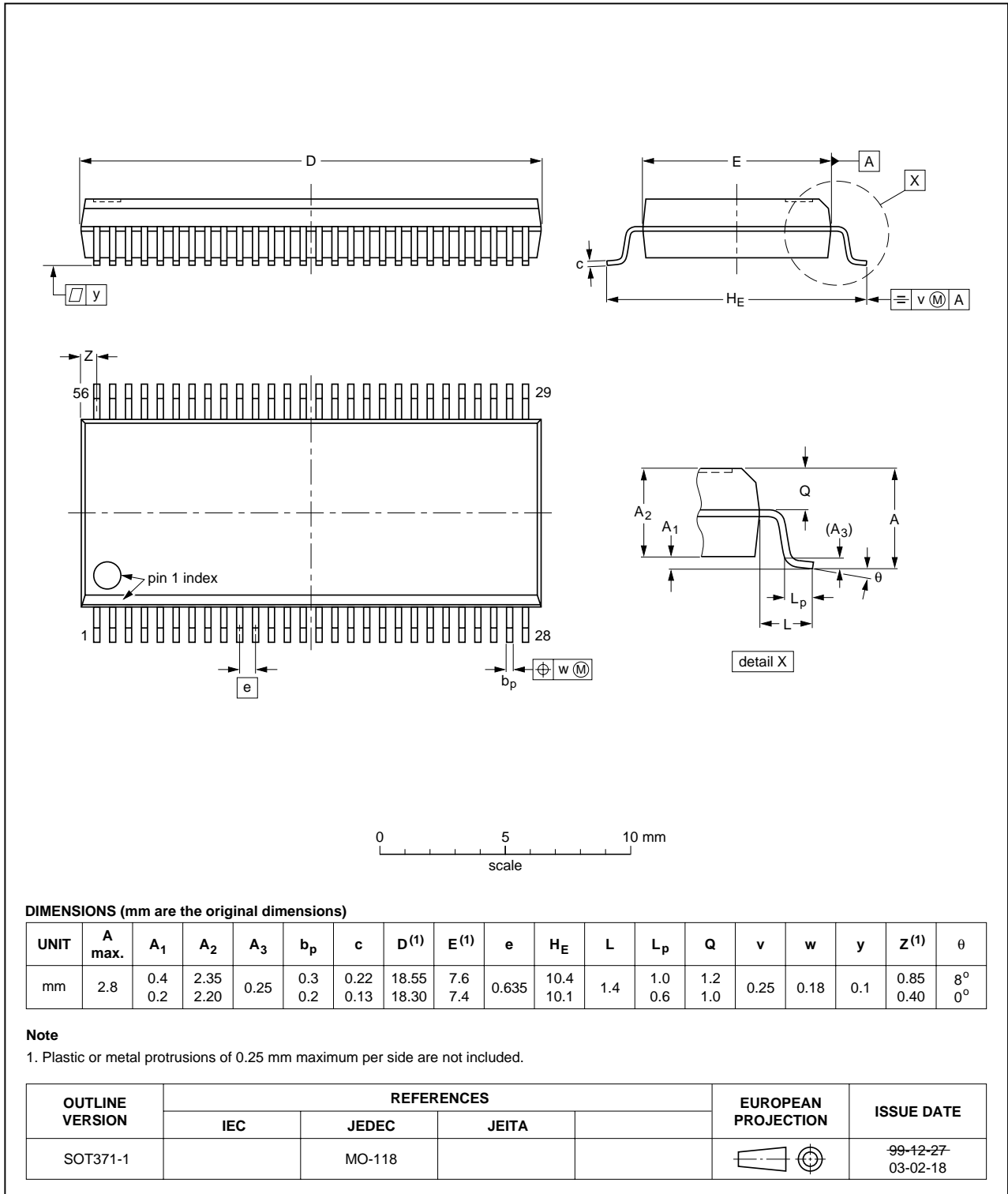


Fig 11. Package outline SOT371-1 (SSOP56)

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

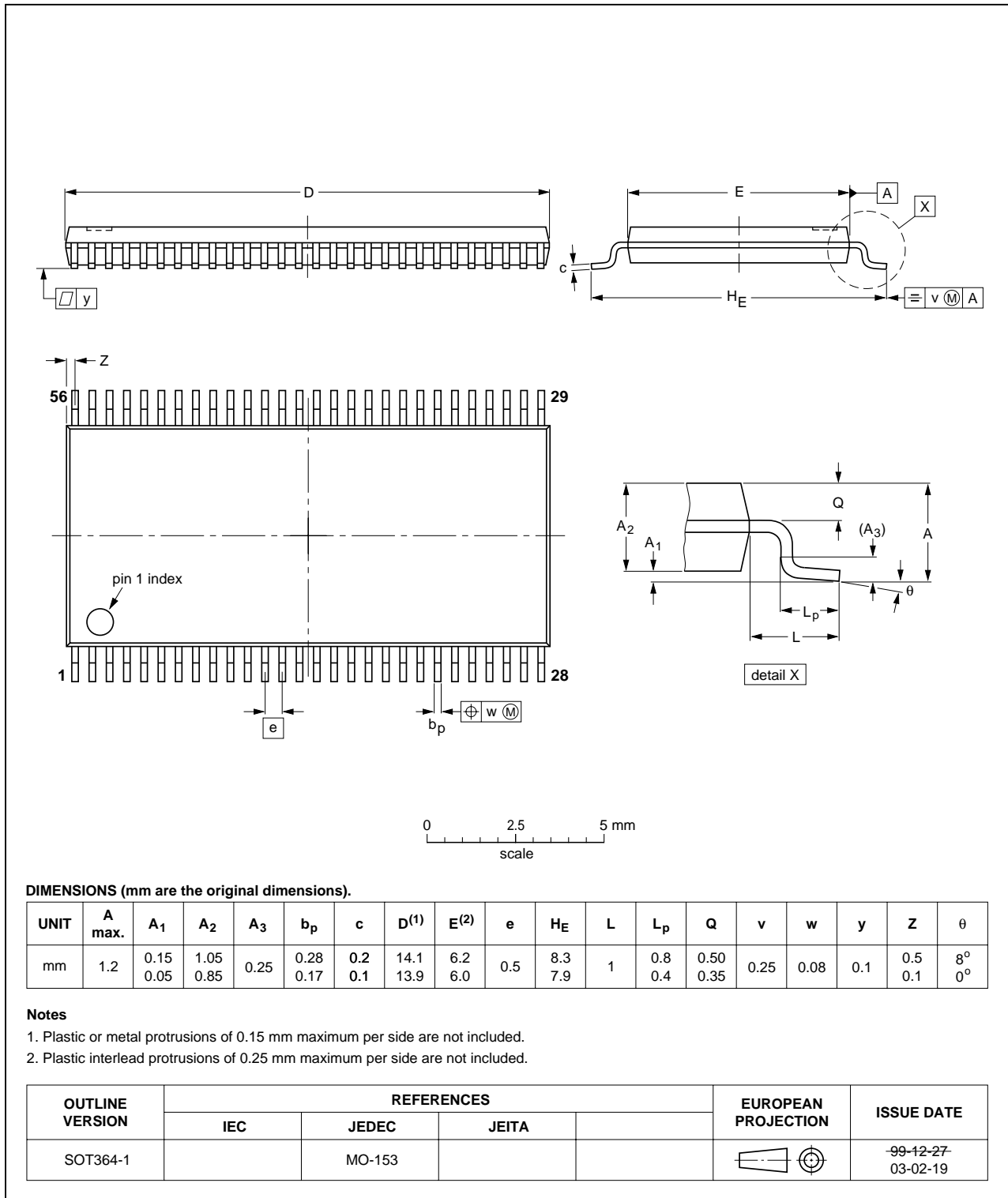


Fig 12. Package outline SOT364-1 (TSSOP56)

## 14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ALVT16823_4	20050802	Product data sheet	-	-	74ALVT16823_3
Modifications:					
					<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li><li>• <a href="#">Section 2</a>: modified 'Jedec Std 17' into 'JESD78'</li><li>• <a href="#">Table 8</a>: changed propagation delays.</li></ul>
74ALVT16823_3	19980612	Product specification	-	9397 750 04016	74ALVT16823_2
74ALVT16823_2	19980612	Product specification	-	9397 750 04016	74ALVT16823
74ALVT16823	19980303	-	-	-	-

## 15. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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