

MDV5524

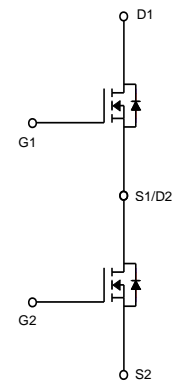
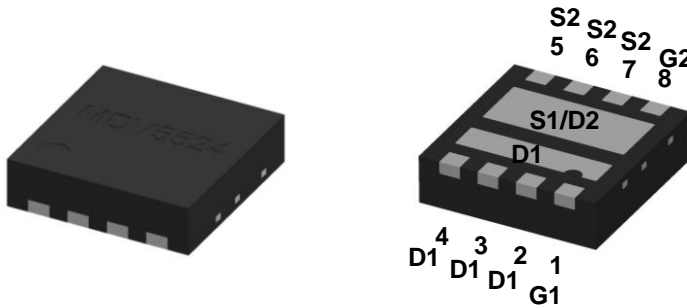
Asymmetric Dual N-channel Trench MOSFET 30V

General Description

The MDV5524 uses advanced MagnaChip's MOSFET Technology, which provides high performance in on-state resistance, fast switching performance and excellent quality. MDV5524 is suitable for DC/DC converter and general purpose applications.

Features

- | | |
|--|--|
| FET1
<ul style="list-style-type: none"> ▫ $V_{DS} = 30V$ ▫ $I_D = 24.5A$ ▫ $R_{DS(ON)} < 14.4m\Omega$ ▫ $< 21.3m\Omega$ ▫ 100% UIL Tested ▫ 100% Rg Tested | FET2
$V_{DS} = 30V$
$I_D = 31.2A @ V_{GS} = 10V$
$< 12.6m\Omega @ V_{GS} = 10V$
$< 15.6m\Omega @ V_{GS} = 4.5V$ |
|--|--|



Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	FET1	FET2	Unit
Drain-Source Voltage	V_{DSS}	30		V
Gate-Source Voltage	V_{GSS}	± 20	± 12	V
Continuous Drain Current ⁽¹⁾	$T_C=25^\circ C$	24.5	31.2	A
	$T_C=100^\circ C$	15.5	19.7	
	$T_A=25^\circ C$	8.5	9.9	
	$T_A=70^\circ C$	6.8	7.9	
Pulsed Drain Current	I_{DM}	100	125	A
Power Dissipation	$T_C=25^\circ C$	14.7	20.8	W
	$T_C=100^\circ C$	5.9	8.3	
	$T_A=25^\circ C$	1.8	2.1	
	$T_A=70^\circ C$	1.1	1.3	
Single Pulse Avalanche Energy ⁽²⁾	E_{AS}	12.1	25.6	mJ
Junction and Storage Temperature Range	T_J, T_{stg}	-55~150		°C

Thermal Characteristics

Characteristics	Symbol	FET1	FET2	Unit
Thermal Resistance, Junction-to-Ambient ⁽¹⁾	$R_{\theta JA}$	70	60	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	8.5	6.0	

Ordering Information

Part Number	Temp. Range	Package	Packing	Rohs Status
MDV5524URH	-55~150°C	Dual PDFN33	Tape & Reel	Halogen Free

FET1 Electrical Characteristics (Ta =25°C)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A, V_{GS} = 0V$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.3	1.8	2.4	
Drain Cut-Off Current	I_{DSS}	$V_{DS} = 30.0V, V_{GS} = 0V$	-	-	1	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20.0V, V_{DS} = 0V$	-	-	± 0.1	
Drain-Source ON Resistance	$R_{DS(on)}$	$V_{GS} = 10.0V, I_D = 6.0A$	-	12.0	14.4	m Ω
		$V_{GS} = 4.5V, I_D = 5.0A$	-	17.0	21.3	
Forward Transconductance	g_{fs}	$V_{DS} = 5.0V, I_D = 6.0A$	-	19.5	-	S
Dynamic Characteristics						
Total Gate Charge	$Q_{g(10V)}$	$V_{DS} = 15.0V, I_D = 6.0A, V_{GS} = 10.0V$	5.7	7.2	8.6	nC
Total Gate Charge	$Q_{g(4.5V)}$		2.8	3.6	4.3	
Gate-Source Charge	Q_{gs}		-	1.4	-	
Gate-Drain Charge	Q_{gd}		-	1.2	-	
Input Capacitance	C_{iss}	$V_{DS} = 15.0V, V_{GS} = 0V, f = 1.0MHz$	290	386	483	pF
Reverse Transfer Capacitance	C_{oss}		68	91	113	
Output Capacitance	C_{rss}		35	47	60	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15.0V, I_D = 6.0A, V_{GS} = 10.0V, R_g = 6.0\Omega$	-	6.7	-	ns
Rise Time	t_r		-	10.2	-	
Turn-Off Delay Time	$t_{d(off)}$		-	17.3	-	
Fall Time	t_f		-	6.5	-	
Gate Resistance	R_g	$f = 1 MHz$	-	3.0	-	Ω
Drain-Source Body Diode Characteristics						
Source-Drain Diode Forward Voltage	V_{SD}	$I_S = 1.0A, V_{GS} = 0V$	-	0.7	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 6.0A, di/dt = 100A/\mu s$	-	16.0	20.0	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	8.0	10.0	nC

Note :

- Surface mounted FR-4 board by JEDEC (jesd51-7). Continuous current at $T_C = 25^\circ C$ is silicon limited.
- E_{AS} is tested at starting $T_J = 25^\circ C, L = 0.1mH, I_{AS} = 11.0A, V_{DD} = 27V, V_{GS} = 10V$ (100% UIL Test).

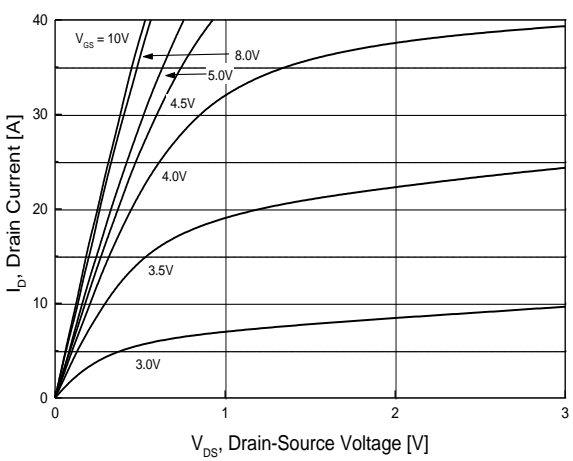


Fig.1 On-Region Characteristics

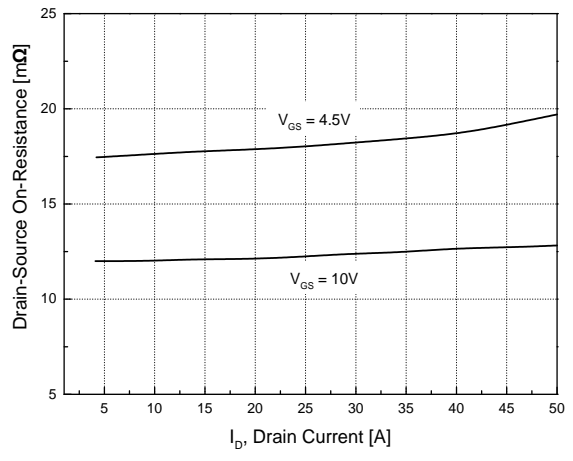


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

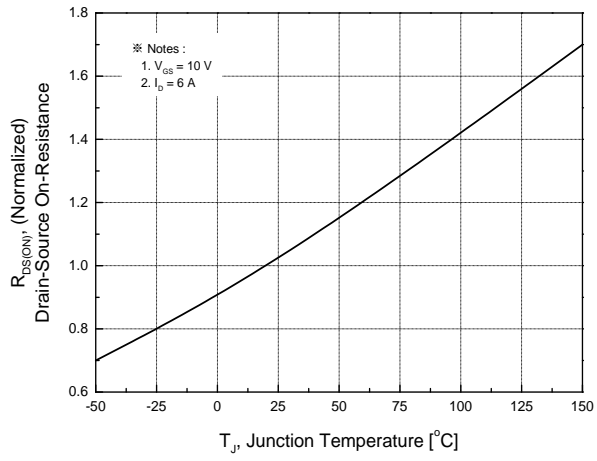


Fig.3 On-Resistance Variation with Junction Temperature

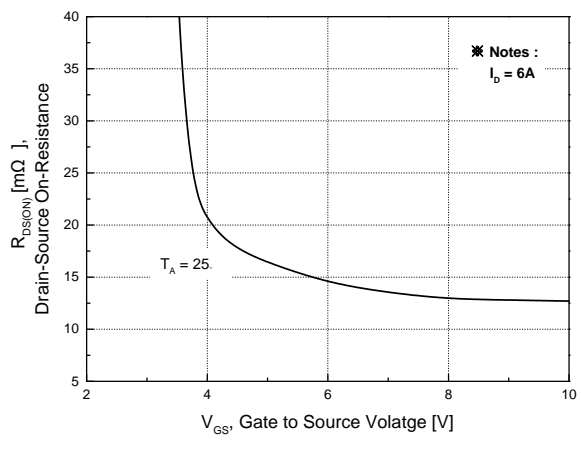


Fig.4 On-Resistance Variation with Gate to Source Voltage

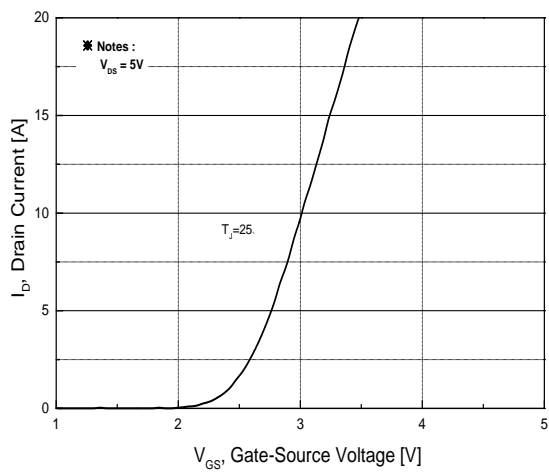


Fig.5 Transfer Characteristics

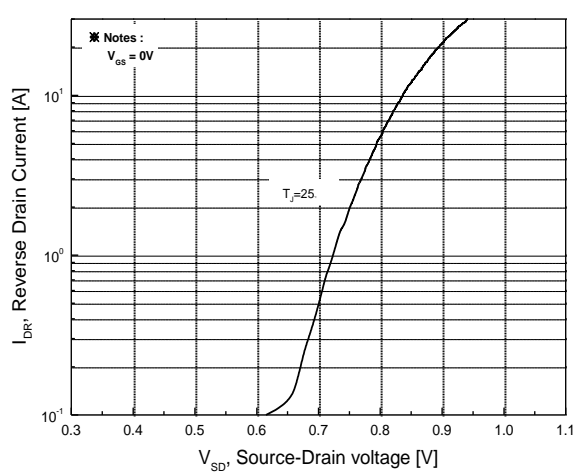


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature

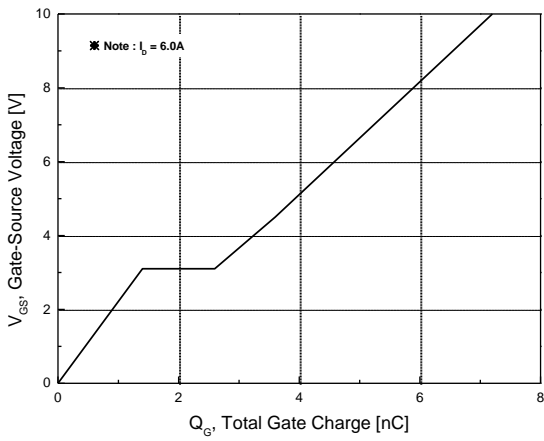


Fig.7 Gate Charge Characteristics

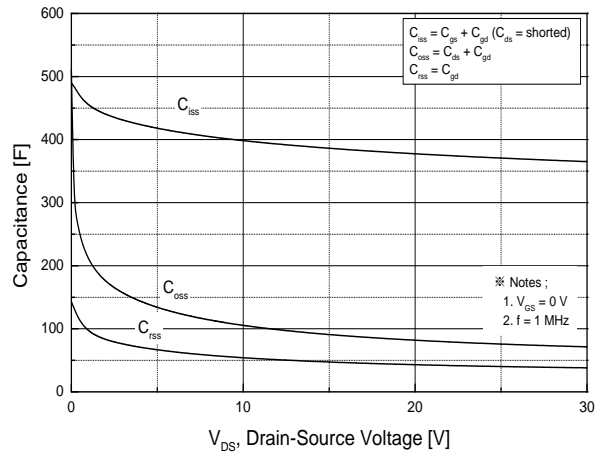


Fig.8 Capacitance Characteristics

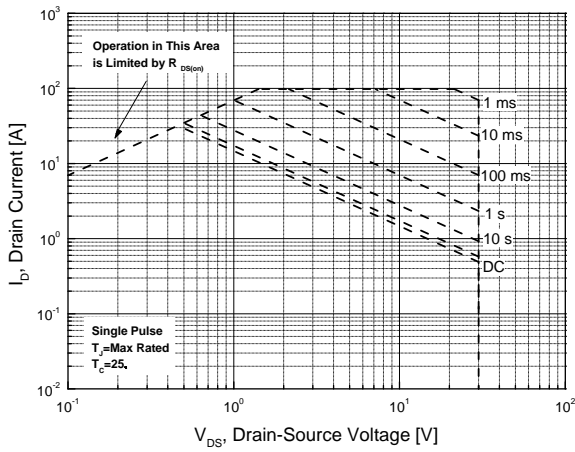


Fig.9 Maximum Safe Operating Area

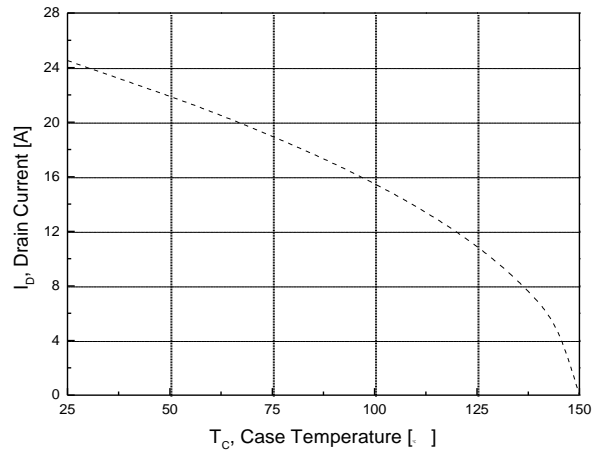


Fig.10 Maximum Drain Current vs. Case Temperature

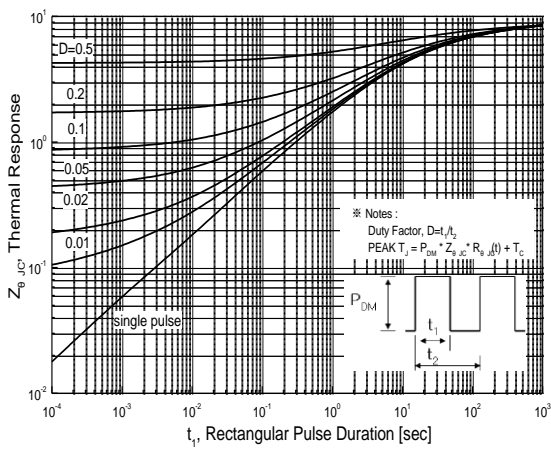


Fig.11 Transient Thermal Response Curve

FET2 Electrical Characteristics (Ta =25°C)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A, V_{GS} = 0V$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	1.5	2.0	
Drain Cut-Off Current	I_{DSS}	$V_{DS} = 30.0V, V_{GS} = 0V$	-	-	1	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 12.0V, V_{DS} = 0V$	-	-	± 0.1	
Drain-Source ON Resistance	$R_{DS(on)}$	$V_{GS} = 10.0V, I_D = 9.0A$	-	10.5	12.6	m Ω
		$V_{GS} = 4.5V, I_D = 7.0A$	-	12.5	15.6	
Forward Transconductance	g_{fs}	$V_{DS} = 5.0V, I_D = 9.0A$	-	38.6	-	S
Dynamic Characteristics						
Total Gate Charge	$Q_{g(10V)}$	$V_{DS} = 15.0V, I_D = 9.0A, V_{GS} = 10V$	14.3	18.0	21.5	nC
Total Gate Charge	$Q_{g(4.5V)}$		6.4	8.1	9.7	
Gate-Source Charge	Q_{gs}		-	2.5	-	
Gate-Drain Charge	Q_{gd}		-	2.0	-	
Input Capacitance	C_{iss}	$V_{DS} = 15.0V, V_{GS} = 0V, f = 1.0MHz$	778	1037	1297	pF
Reverse Transfer Capacitance	C_{oss}		107	143	179	
Output Capacitance	C_{riss}		42	56	70	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15.0V, I_D = 9.0A, V_{GS} = 10.0V, R_g = 6.0\Omega$	-	9.3	-	ns
Rise Time	t_r		-	10.4	-	
Turn-Off Delay Time	$t_{d(off)}$		-	41.8	-	
Fall Time	t_f		-	7.1	-	
Gate Resistance	R_g	$f = 1 MHz$	-	2.0	3.0	Ω
Drain-Source Body Diode Characteristics						
Source-Drain Diode Forward Voltage	V_{SD}	$I_S = 1.0A, V_{GS} = 0V$	-	0.7	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 9.0A, di/dt = 100A/\mu s$	-	19.1	23.8	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	12.0	15.0	nC

Note :

- Surface mounted FR-4 board by JEDEC (jesd51-7). Continuous current at $T_C = 25^\circ C$ is silicon limited.
- E_{AS} is tested at starting $T_j = 25^\circ C, L = 0.1mH, I_{AS} = 16.0A, V_{DD} = 27V, V_{GS} = 10V$ (100% UIL Test).

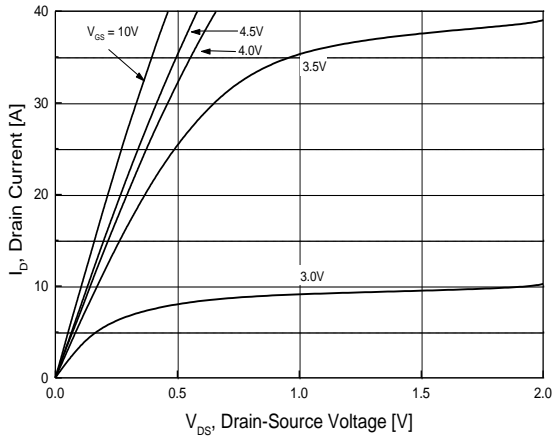


Fig.1 On-Region Characteristics

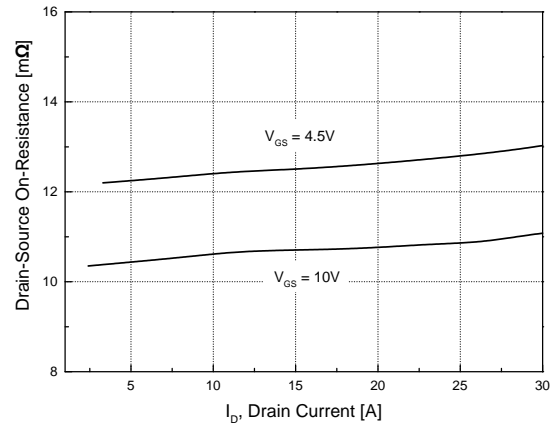


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

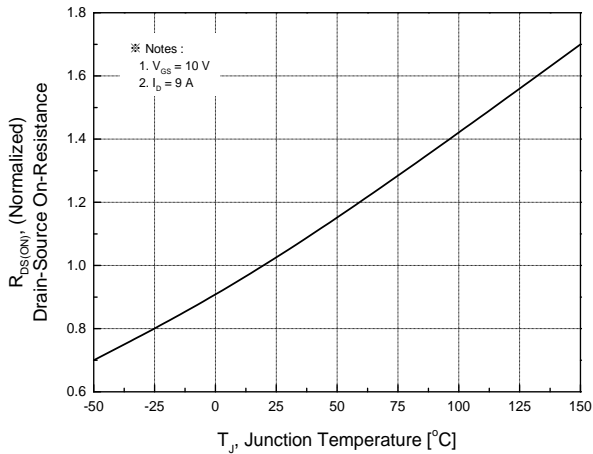


Fig.3 On-Resistance Variation with Junction Temperature

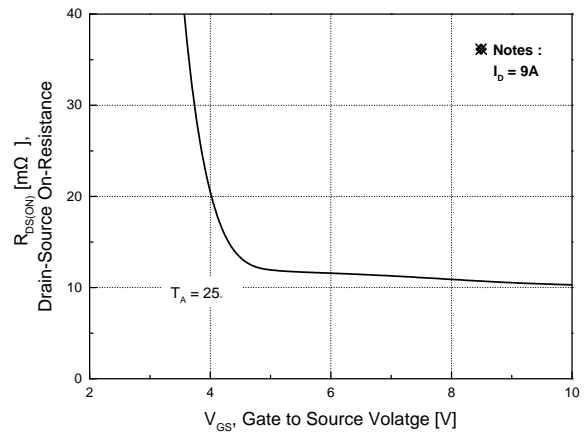


Fig.4 On-Resistance Variation with Gate to Source Voltage

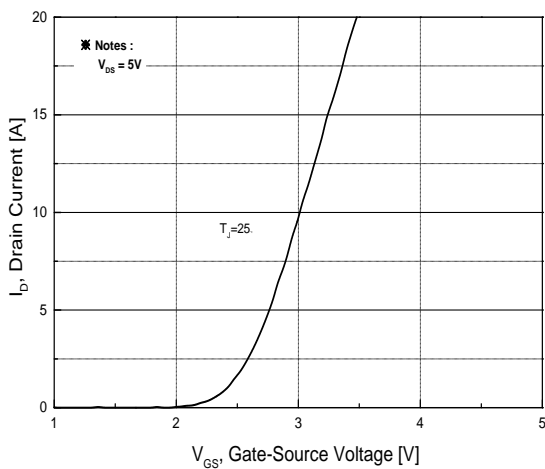


Fig.5 Transfer Characteristics

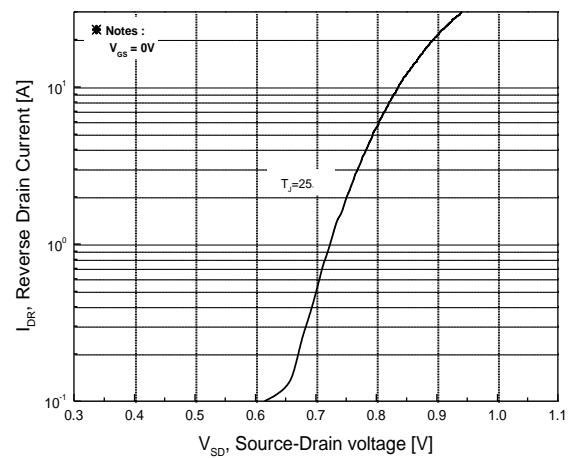
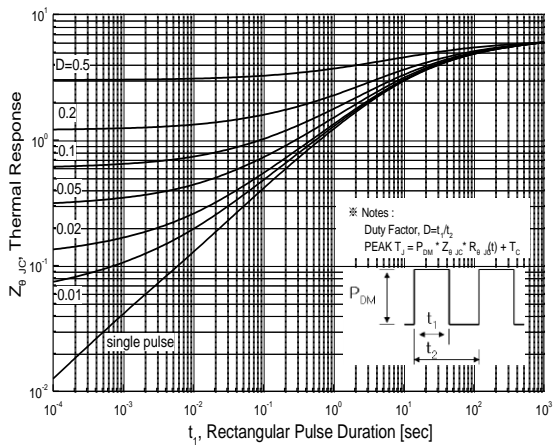
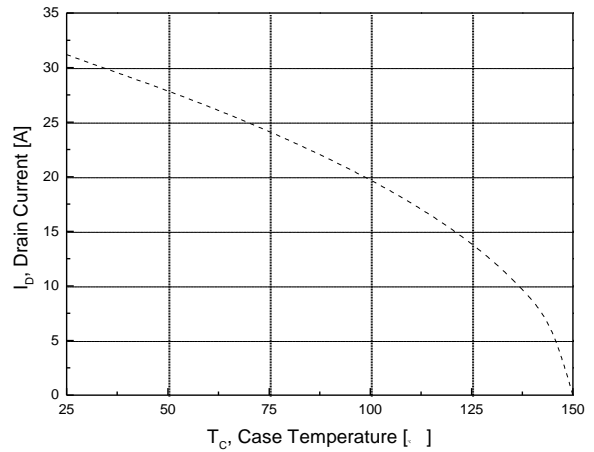
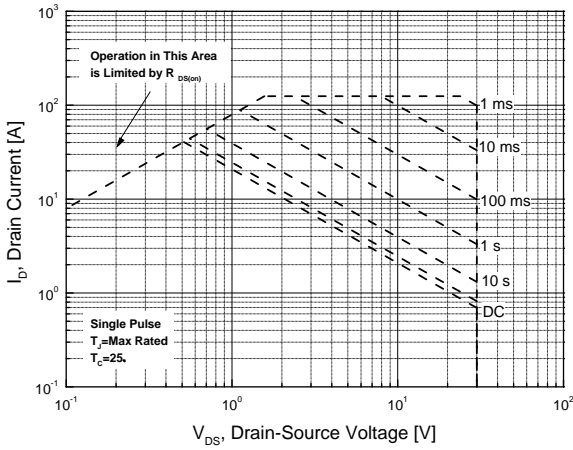
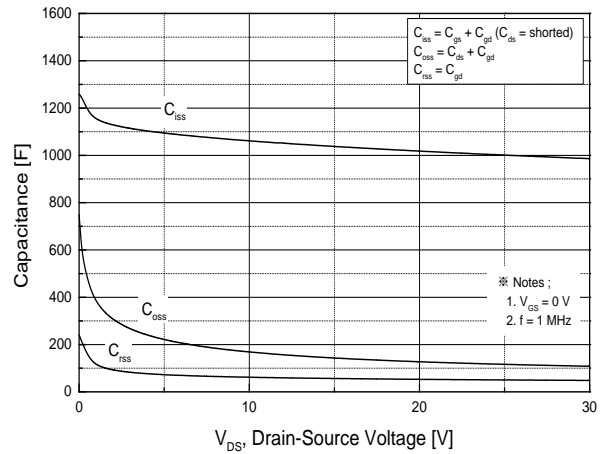
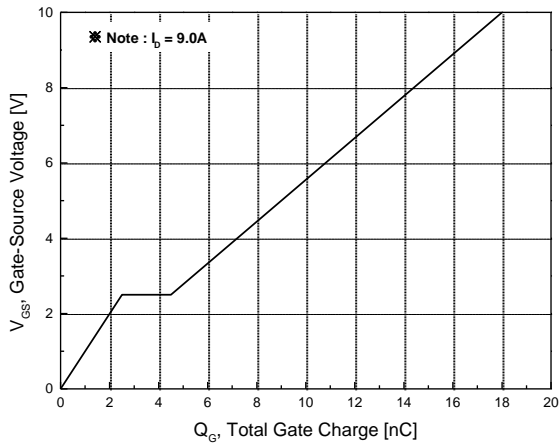


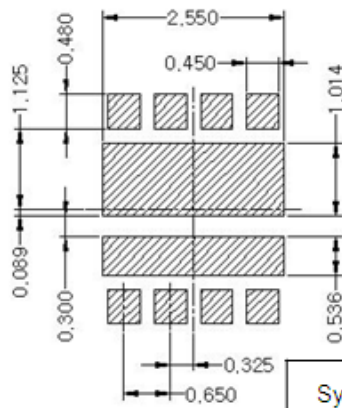
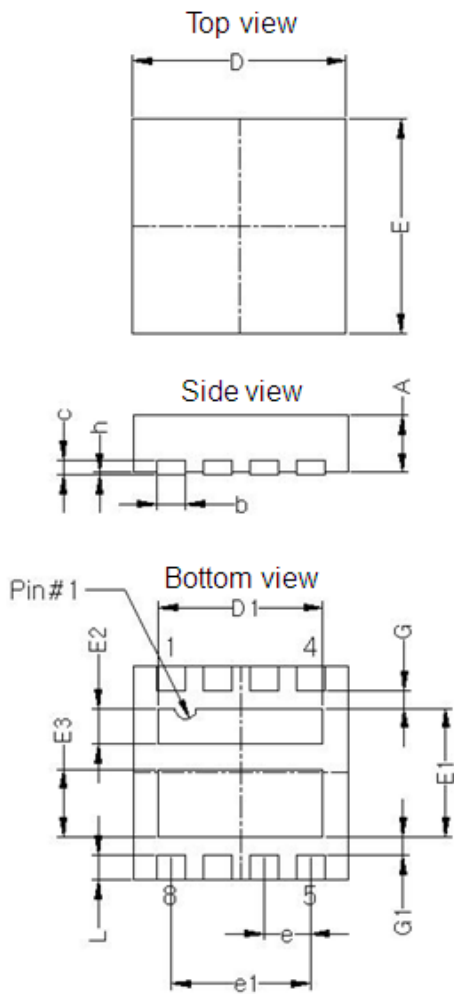
Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature



Package Dimension

Dual PDFN33 (3x3mm)

Dimensions are in millimeters, unless otherwise specified



Symbol	Dimension [mm]		
	Min	Nom	Max
A	-	-	0.80
b	0.35	0.40	0.45
c	0.15	0.20	0.25
D	3.00 BSC		
D1	2.25	2.30	2.35
E	3.00 BSC		
E1	1.70	1.80	1.90
E2	0.45	0.50	0.55
E3	0.90	0.95	1.00
e	0.65 BSC		
e1	1.95 BSC		
G	0.20	0.25	0.30
G1	0.20	0.25	0.30
L	0.30	0.35	0.40
h	0.00	-	0.05

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