DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT5555
Programmable delay timer with oscillator

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

Programmable delay timer with oscillator 74HC/HCT5555

FEATURES

- Positive and negative edge triggered
- Retriggerable or non-retriggerable
- Programmable delay

  minimum: 100 ns

  maximum: depends on input frequency and division ratio
- Divide-by range of 2 to 2^{24}
- Direct reset terminates output pulse
- Very low power consumption in triggered start mode
- 3 oscillator operating modes:
  - RC oscillator
  - Crystal oscillator
  - External oscillator
- Device is unaffected by variations in temperature and V_{CC} when using an external oscillator
- Automatic power-ON reset
- Schmitt trigger action on both trigger inputs
- Direct drive for a power transistor
- Low power consumption in active mode with respect to TTL type timers
- High precision due to digital timing
- Output capability: 20 mA
- I_{CC} category: MSI.

APPLICATIONS

- Motor control
- Attic fan timers
- Delay circuits
- Automotive applications
- Precision timing
- Domestic appliances.

GENERAL DESCRIPTION

The 74HC/HCT5555 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT5555 are precision programmable delay timers which consist of:

- 24-stage binary counter
- integrated oscillator (using external timing components)
- retriggerable/non-retriggerable monostable
- automatic power-ON reset
- output control logic
- oscillator control logic
- overriding asynchronous master reset (MR).

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	A, $\overline{B}$ to Q/$\overline{Q}$		24	24	ns
	MR to Q/$\overline{Q}$		19	20	ns
	RS to Q/$\overline{Q}$		26	28	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	23	36	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT5555N	16	DIL	plastic	SOT38Z
74HC/HCT5555D	16	SO16	plastic	SOT109A

PINNING

SYMBOL	PIN	DESCRIPTION
RS	1	clock input/oscillator pin
R_{TC}	2	external resistor connection
C_{TC}	3	external capacitor connection
A	4	trigger input (positive-edge triggered)
$\overline{B}$	5	trigger input (negative-edge triggered)
RTR/$\overline{RTR}$	6	retriggerable/non-retriggerable input (active HIGH/active LOW)
$\overline{Q}$	7	pulse output (active LOW)
GND	8	ground (0 V)
Q	9	pulse output (active HIGH)
$S_0 - S_3$	10, 11, 12, 13	programmable input
OSC CON	14	oscillator control
MR	15	master reset input (active HIGH)
V_{CC}	16	positive supply voltage

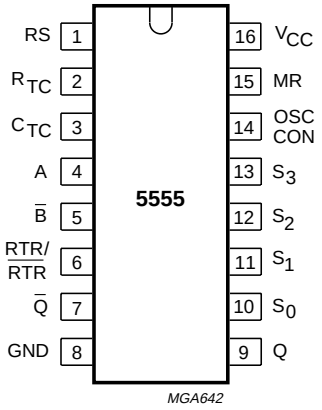


Fig.1 Pin configuration.

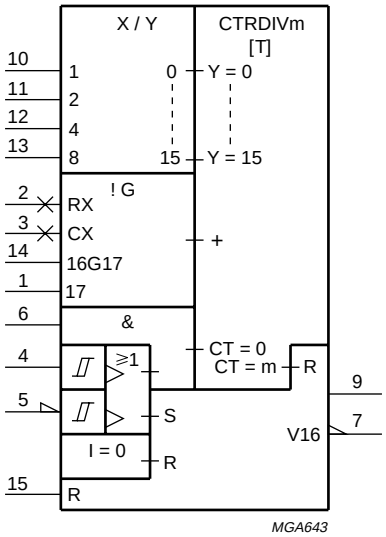


Fig.2 IEC logic diagram.

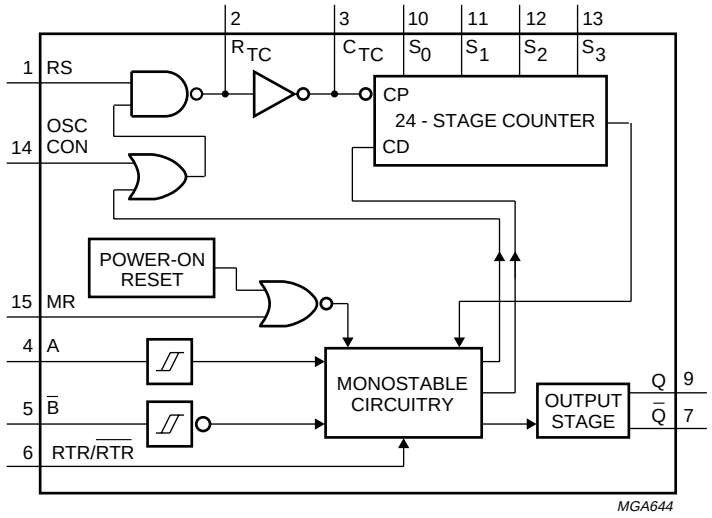


Fig.3 Functional diagram.

FUNCTIONAL DESCRIPTION

The oscillator configuration allows the design of RC or crystal oscillator circuits. The device can operate from an external clock signal applied to the RS input (R_{TC} and C_{TC} must not be connected). The oscillator frequency is determined by the external timing components (R_T and C_T), within the frequency range 1 Hz to 4 MHz (32 kHz to 20 MHz with crystal oscillator).

In the HCT version the MR input is TTL compatible but the RS input has CMOS input switching levels. The RS input can be driven by TTL input levels if RS is tied to V_{CC} via a pull-up resistor.

The counter divides the frequency to obtain a long pulse duration. The 24-stage is digitally programmed via the select inputs (S_0 to S_3). Pin S_3 can also be used to select the test mode, which is a convenient way of functionally testing the counter.

The “5555” is triggered on either the positive-edge, negative-edge or both.

- Trigger pulse applied to input A for positive-edge triggering
- Trigger pulse applied input $\overline{B}$ for negative-edge triggering
- Trigger pulse applied to inputs A and $\overline{B}$ (tied together) for both positive-edge and negative triggering.

The Schmitt trigger action in the trigger inputs, transforms slowly changing input signals into sharply defined jitter-free output signals and provides the circuit with excellent noise immunity.

The OSC CON input is used to select the oscillator mode, either continuously running (OSC CON = HIGH) or triggered start mode (OSC CON = LOW). The continuously running mode is selected where a start-up delay is an undesirable feature and the triggered start mode is selected where very low power consumption is the primary concern.

The start of the programmed time delay occurs when output Q goes HIGH (in the triggered start mode, the previously disabled oscillator will start-up). After the programmed time delay, the flip-flop stages are reset and the output returns to its original state.

An internal power-on reset is used to reset all flip-flop stages.

The output pulse can be terminated by the asynchronous overriding master reset (MR), this results in all flip-flop stages being reset. The output signal is capable of driving a power transistor. The output time delay is calculated using the following formula (minimum time delay is 100 ns):

$$\frac{1}{f_i} \times \text{division ratio (s)}.$$

Once triggered, the output width may be extended by retriggering the gated, active HIGH-going input A or the active LOW-going input $\overline{B}$. By repeating this process, the output pulse period (Q = HIGH, $\overline{Q}$ = LOW) can be made as long as desired. This mode is selected by RTR/$\overline{\text{RTR}}$ = HIGH. A LOW on RTR/$\overline{\text{RTR}}$ makes, once triggered, the outputs (Q, $\overline{Q}$) independent of further transitions of inputs A and $\overline{B}$.

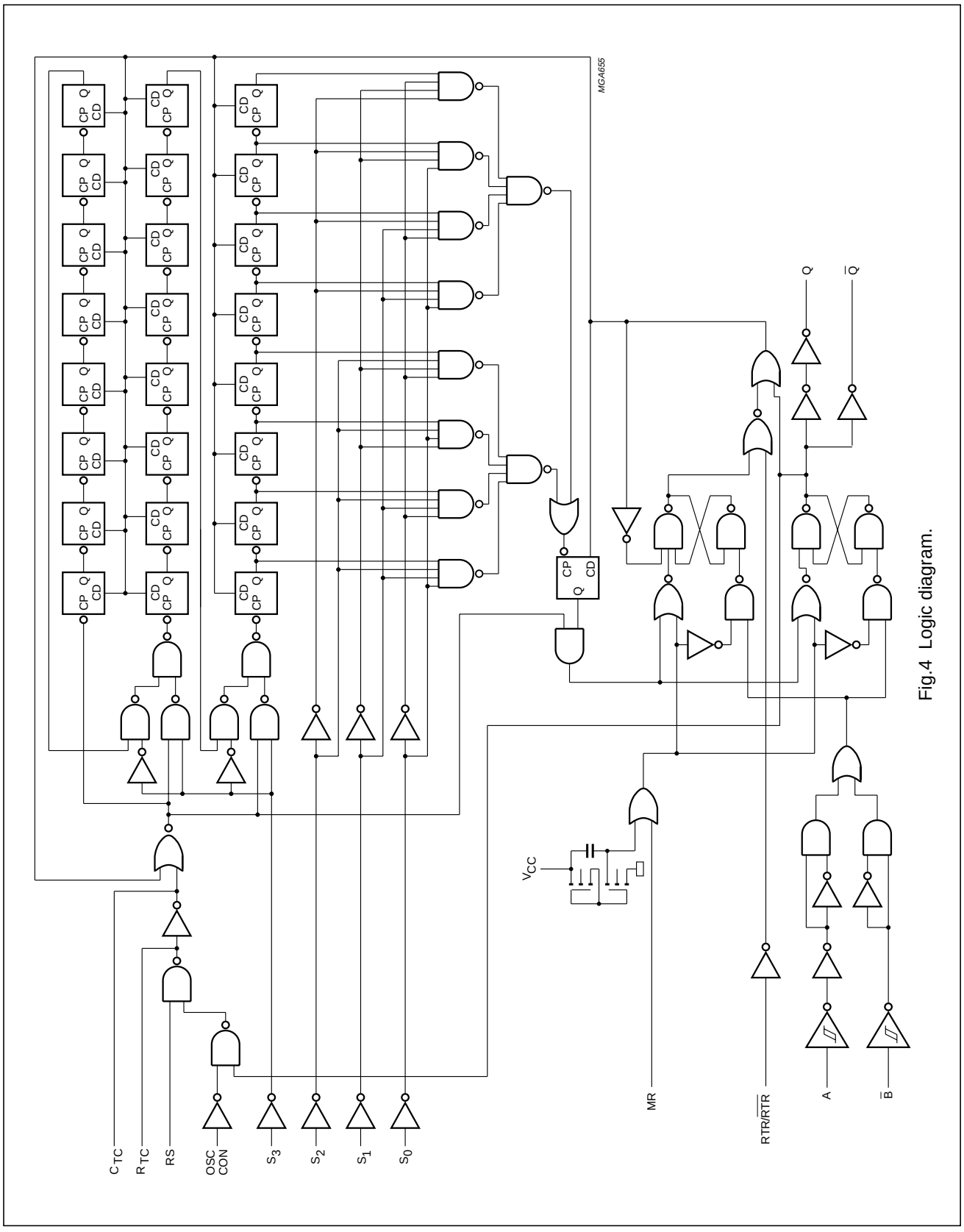


Fig.4 Logic diagram.

TEST MODE

Set S_3 to a logic LOW level, this will divide the 24 stage counter into three, parallel clocking, 8-stage counters. Set S_0, S_1 and S_2 to a logic HIGH level, this programs the counter to divide-by 2^8 (256). Apply a trigger pulse and clock in 255 pulses, this sets all flip-flop stages to a logic HIGH level. Set S_3 to a logic HIGH level, this causes the counter to divide-by 2^{24}. Clock one more pulse into the RS input, this causes a logic 0 to ripple through the counter and output Q/$\overline{Q}$ goes from HIGH-to-LOW level. This method of testing the delay counter is faster than clocking in 2^{24} (16 777 216) clock pulses.

FUNCTION TABLE

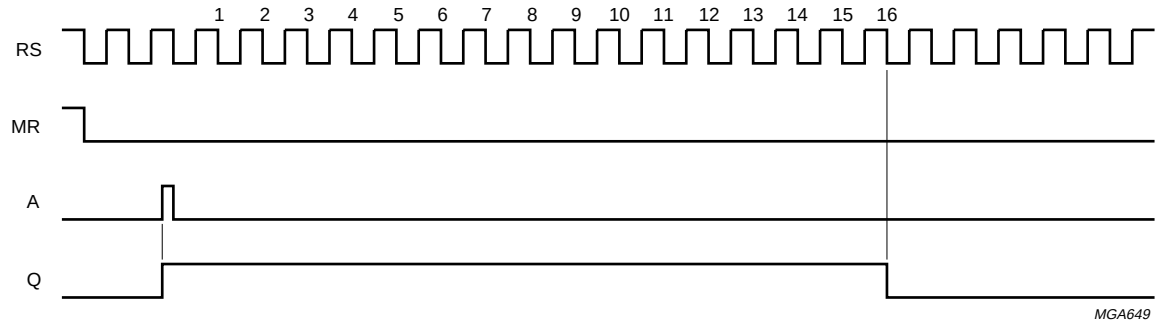
INPUTS			OUTPUTS	
MR	**A**	**$\overline{B}$**	**Q**	**$\overline{Q}$**
H	X	X	L	H
L	↑	X	one HIGH level output pulse	one LOW level output pulse
L	X	↓	one HIGH level output pulse	one LOW level output pulse

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH transition
   ↓ = HIGH-to-LOW transition.

DELAY TIME SELECTION

SELECT INPUTS				OUTPUT Q/$\overline{Q}$ (FREQUENCY DIVIDING)	
S_3	S_2	S_1	S_0	BINARY	DECIMAL
L	L	L	L	2^1	2
L	L	L	H	2^2	4
L	L	H	L	2^3	8
L	L	H	H	2^4	16
L	H	L	L	2^5	32
L	H	L	H	2^6	64
L	H	H	L	2^7	128
L	H	H	H	2^8	256
.	.	.	.	.	.
H	L	L	L	2^{17}	131 072
H	L	L	H	2^{18}	262 144
H	L	H	L	2^{19}	524 288
H	L	H	H	2^{20}	1 048 576
H	H	L	L	2^{21}	2 097 152
H	H	L	H	2^{22}	4 194 304
H	H	H	L	2^{23}	8 388 608
H	H	H	H	2^{24}	16 777 216



Timing example shown for S_3, S_2, S_1, S_0 = 0011 (binary 2^4, decimal 16).

Fig.5 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: parallel outputs, bus driver; serial output, standard I_{CC} category: MSI.

DC CHARACTERISTICS FOR 74HC

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	1.9 4.4 5.9	2 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0		I_o = –20 µA
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	3.98 5.48	4.32 5.81	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0		I_o = –6.0 mA I_o = –7.8 mA
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	3.3 4.8	– –	– –	3 4.5	– –	2.7 4.2	– –	V V	4.5 6.0		I_o = –20 mA I_o = –20 mA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6.0		I_o = 20 µA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	– –	0.15 0.15	0.26 0.26	– –	0.33 0.33	– –	0.40 0.40	V V	4.5 6.0		I_o = 6.0 mA I_o = 7.8 mA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	– –	– –	0.9 0.9	– –	1.14 1.14	– –	1.34 1.34	V V	4.5 6.0		I_o = 20 mA I_o = 25 mA
V_{IH}	HIGH level input voltage RS input	1.7 3.6 4.8	– – –	– – –	1.7 3.6 4.8	– – –	1.7 3.6 4.8	– – –	V V V	2 4.5 6.0		
V_{IL}	LOW level input voltage RS input	– – –	– – –	0.3 0.9 1.2	– – –	0.3 0.9 1.2	– – –	0.3 0.9 1.2	V V V	2.0 4.5 6.0		

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage R_{TC} output	3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	RS = GND; OSC CON = V_{CC}	I_o = –2.6 mA I_o = –3.3 mA
		3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	RS = V_{CC}; OSC CON = GND; untriggered	I_o = –0.65 mA I_o = –0.85 mA
		1.9 4.4 5.9	2.0 4.5 6	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2.0 4.5 6.0	RS = V_{CC}; OSC CON = V_{CC}	I_o = –20 µA
		1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	1.9 4.4 5.9	– – –	V V V	2 4.5 6.0	RS = V_{CC}; OSC CON = GND; untriggered	I_o = –20 µA
V_{OH}	HIGH level output voltage C_{TC} output	3.98 5.48	– –	– –	3.84 5.34	– –	3.7 5.2	– –	V V	4.5 6.0	RS = V_{IH}; OSC CON = V_{IH}	I_o = –3.2 mA I_o = –4.2 mA
V_{OL}	LOW level output voltage R_{TC} output	– –	– –	0.26 0.26	– –	0.33 0.33	– –	0.4 0.4	V V	4.5 6	RS = V_{CC}; OSC CON = V_{CC}	I_o = 2.6 mA I_o = 3.3 mA
		– – –	0 0 0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V V V	2.0 4.5 6	RS = V_{CC}; OSC CON = V_{CC}	I_o = 20 µA
V_{OL}	LOW level output voltage C_{TC} output	– –	– –	0.26 0.26	– –	0.33 0.33	– –	0.4 0.4	V V	4.5 6.0	RS = V_{IL}; OSC CON = V_{IL}; untriggered	I_o = 3.2 mA I_o = 4.2 mA

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PLH}/t_{PHL}	propagation delay A, $\overline{B}$ to Q, $\overline{Q}$	– – –	77 28 22	240 48 41	– – –	300 60 51	– – –	360 72 61	ns ns ns	2.0 4.5 6.0	Fig.6
t_{PLH}/t_{PHL}	propagation delay MR to Q, $\overline{Q}$	– – –	61 22 18	185 37 31	– – –	230 46 39	– – –	280 56 48	ns ns ns	2.0 4.5 6.0	Fig.7
t_{PLH}/t_{PHL}	propagation delay RS to Q, $\overline{Q}$	– – –	83 30 24	250 50 43	– – –	315 63 54	– – –	375 75 64	ns ns ns	2.0 4.5 6.0	Fig.8; note 1
t_{THL}/t_{TLH}	output transition time	– – –	19 7 6	75 15 13	– – –	95 19 16	– – –	110 22 19	ns ns ns	2.0 4.5 6.0	Fig.6
t_W	trigger pulse width A = HIGH $\overline{B}$ = LOW	70 14 12	17 6 5	– – –	90 18 15	– – –	105 21 18	– – –	ns ns ns	2.0 4.5 6.0	Fig.6
t_W	master reset pulse width HIGH	70 14 12	19 7 6	– – –	90 18 15	–	105 21 18	– – –	ns ns ns	2.0 4.5 6.0	Fig.7
t_W	clock pulse width RS; HIGH or LOW	80 16 14	25 9 7	– – –	100 20 17	– – –	120 24 20	– – –	ns ns ns	2.0 4.5 6.0	Fig.8
t_W	minimum output pulse width Q = HIGH, $\overline{Q}$ = LOW	– – –	275 100 80	– – –	– – –	– – –	– – –	– – –	ns ns ns	2.0 4.5 6.0	Fig.6; note 1
t_{rt}	retrigger time A, $\overline{B}$	– – –	0 0 0	– – –	– – –	– – –	– – –	– – –	ns ns ns	2.0 4.5 6.0	Fig.10; note 2
R_{EXT}	external timing resistor	5 1	– –	1000 1000	– –	– – –	– –	– – –	kΩ kΩ	2.0 5.0	Fig.13
C_{EXT}	external timing capacitor	50 50	no limits						pF pF	2.0 5.0	Fig.13
t_{rem}	removal time MR to A, $\overline{B}$	120 24 20	39 14 11	– – –	150 30 26	– – –	180 36 31	– – –	ns ns ns	2.0 4.5 6.0	Fig.7

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
f_{max}	maximum	2	5.9	–	1.8	–	1.3	–	MHz	2.0	Fig.8; note 3
	clock pulse	10	18	–	8	–	6.6	–	MHz	4.5	
	frequency	12	21	–	10	–	8	–	MHz	6.0	
f_{max}	maximum	6	24.8	–	4.8	–	4	–	MHz	2.0	Fig.9; note 4
	clock pulse	30	75	–	24	–	20	–	MHz	4.5	
	frequency	35	89	–	28	–	24	–	MHz	6.0	

Notes

1. One stage selected.
2. It is possible to retrigger directly after the trigger pulse, however the pulse will only be extended, if the time period exceeds the clock input cycle time divided by 2.
3. One stage selected. The termination of the output pulse remains synchronized with respect to the falling edge of the RS clock input.
4. One stage selected. The termination of the output pulse is no longer synchronized with respect to the falling edge of the RS clock input.

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.
Output capability: non-standard; bus driver with extended specification on V_{OH} and V_{OL}
I_{CC} category: MSI.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			–40 to +85		–0 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	4.4	4.5	–	4.4	–	4.4	–	V	4.5		I_o = –20 µA
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	3.98	4.32	–	3.84	–	3.7	–	V	4.5		I_o = –6 mA
V_{OH}	HIGH level output voltage Q and $\overline{Q}$ outputs	3.3	–	–	3	–	2.7	–	V	4.5		I_o = –20 mA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	–	0	0.1	–	0.1	–	0.1	V	4.5		I_o = 20 µA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	–	0.15	0.26	–	0.33	–	0.40	V	4.5		I_o = 6 mA
V_{OL}	LOW level output voltage Q and $\overline{Q}$ outputs	–	–	0.9	–	1.14	–	1.34	V	4.5	–	I_o = 20 mA

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION		
		+25			−40 to +85		−0 to +125			V_{CC} (V)	V_I	OTHER
		MIN	TYP	MAX	MIN	MAX	MIN	MAX				
V_{OH}	HIGH level output voltage R_{TC} output	3.98	–	–	3.84	–	3.7	–	V	4.5	RS = GND; OSC CON = V_{CC}	I_o = –2.6 mA
		3.98	–	–	3.84	–	3.7	–	V	4.5	RS = V_{CC}; OSC CON = GND; untriggered	I_o = –0.65 mA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5	RS = V_{CC}; OSC CON = V_{CC}	I_o = –20 µA
		4.4	4.5	–	4.4	–	4.4	–	V	4.5	RS = V_{CC}; OSC CON = GND; untriggered	I_o = –20 µA
V_{OH}	HIGH level output voltage C_{TC} output	3.98	–	–	3.84	–	3.7	–	V	4.5	RS = V_{IH}; OSC CON = V_{IH}	I_o = –3.2 mA
V_{OL}	LOW level output voltage R_{TC} output	–	–	0.26	–	0.33	–	0.4	V	4.5	RS = V_{CC}; OSC CON = V_{CC}	I_o = 2.6 mA
		–	0	0.1	–	0.1	–	0.1	V	4.5	RS = V_{CC}; OSC CON = V_{CC}	I_o = 20 µA
V_{OL}	LOW level output voltage C_{TC} output	–	–	0.26	–	0.33	–	0.4	V	4.5	RS = V_{IL}; OSC CON = V_{IL}; untriggered	I_o = 3.2 mA

Notes

1. The RS input has CMOS input switching levels.
2. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the following table.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
MR	0.35
A	0.69
$\overline{B}$	0.50
RTR/$\overline{RTR}$	0.35
OSC CON	1.20
S_0 - S_2	0.65
S_3	0.40

AC CHARACTERISTICS FOR 74HCT

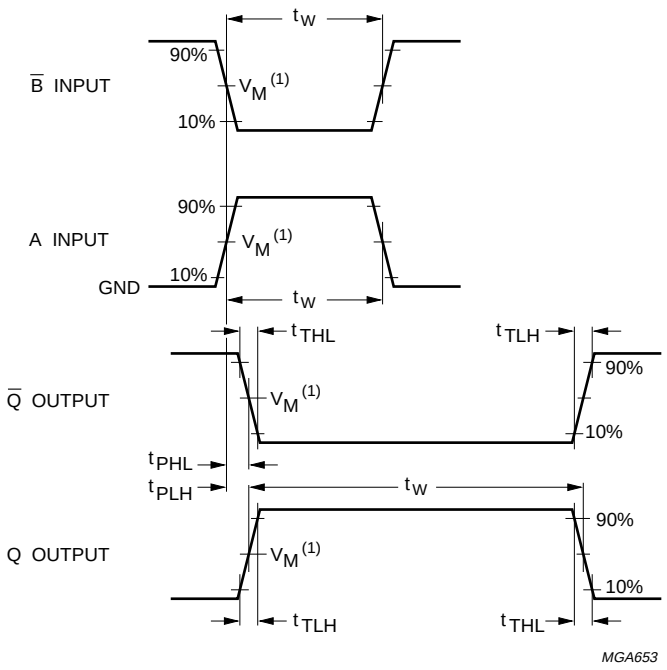
GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PLH}/t_{PHL}	propagation delay A, $\overline{B}$ to Q, $\overline{Q}$	–	28	48	–	60	–	72	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay MR to Q, $\overline{Q}$	–	24	41	–	51	–	62	ns	4.5	Fig.7
t_{PHL}/t_{PLH}	propagation delay RS to Q, $\overline{Q}$	–	32	54	–	68	–	81	ns	4.5	Fig.8; note 1
t_{THL}/t_{TLH}	output transition time	–	7	15	–	19	–	22	ns	4.5	Fig.6
t_W	trigger pulse width A = HIGH $\overline{B}$ = LOW	21	12	–	26	–	32	–	ns	4.5	Fig.6
t_W	master reset pulse width HIGH	14	5	–	18	–	21	–	ns	4.5	Fig.7
t_W	clock pulse width RS; HIGH or LOW	16	9	–	20	–	24	–	ns	4.5	Fig.8
t_W	minimum output pulse width Q = HIGH, $\overline{Q}$ = LOW	–	100	–	–	–	–	–	ns	4.5	Fig.6
t_{rt}	retrigger time A, $\overline{B}$	–	0	–	–	–	–	–	ns	4.5	Fig.10; note 2
R_{EXT}	external timing resistor	1	–	1000	–	–	–	–	kΩ	4.5	Fig.13
C_{EXT}	external timing capacitor	50	no limits						pF	4.5	Fig.13
t_{rem}	removal time MR to A, $\overline{B}$	24	14	–	30	–	36	–	ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency	10	18	–	8	–	6.6	–	MHz	4.5	Fig.8; note 3
f_{max}	maximum clock pulse frequency	30	75	–	24	–	20	–	MHz	4.5	Fig.9; note 4

Notes

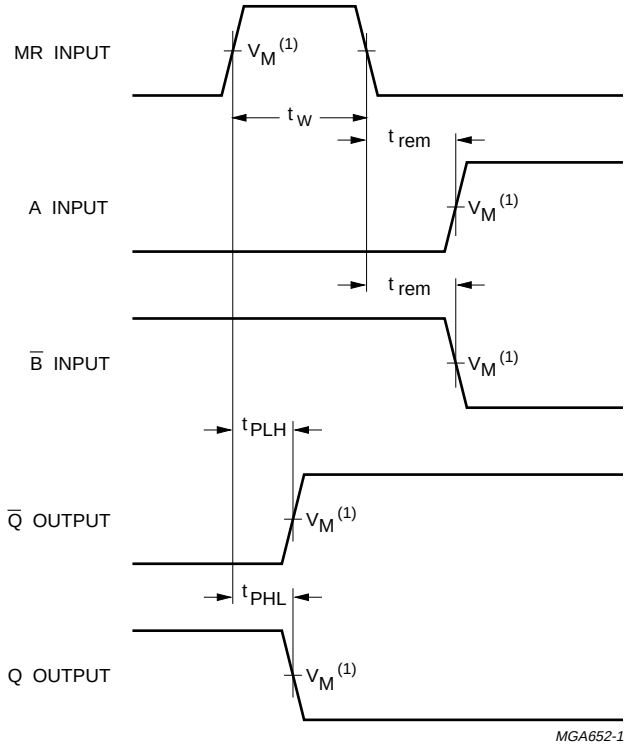
1. One stage selected.
2. It is possible to retrigger directly after the trigger pulse, however the pulse will only be extended, if the time period exceeds the clock input cycle time divided by 2.
3. One stage selected. The termination of the output pulse remains synchronized with respect to the falling edge of the RS clock input.
4. One stage selected. The termination of the output pulse is no longer synchronized with respect to the falling edge of the RS clock input.

AC WAVEFORMS



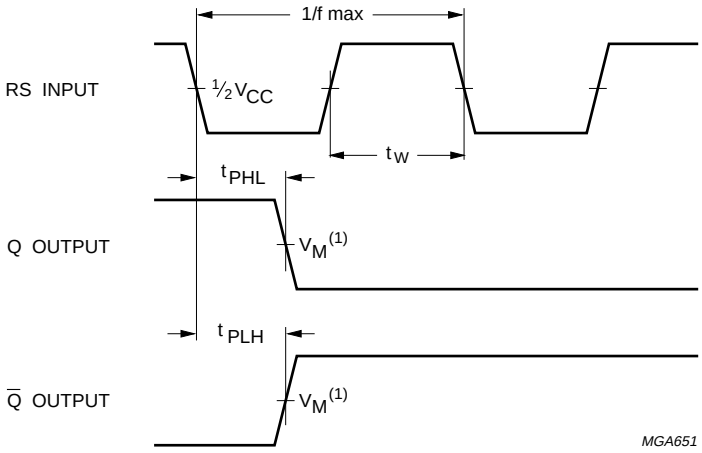
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the triggering of the delay timer by input A or $\overline{B}$, the minimum pulse widths of the trigger inputs A and $\overline{B}$, the output pulse width and output transition times.



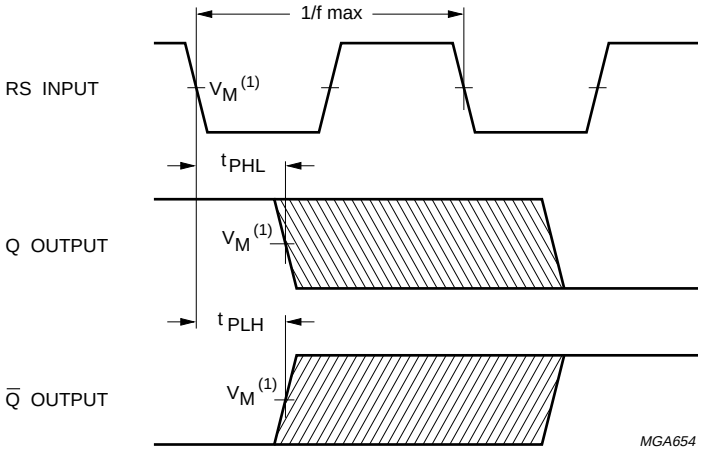
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the master reset (MR) pulse width, the master reset to outputs (Q and $\overline{Q}$) propagation delays and the master reset to trigger inputs (A and $\overline{B}$) removal time.



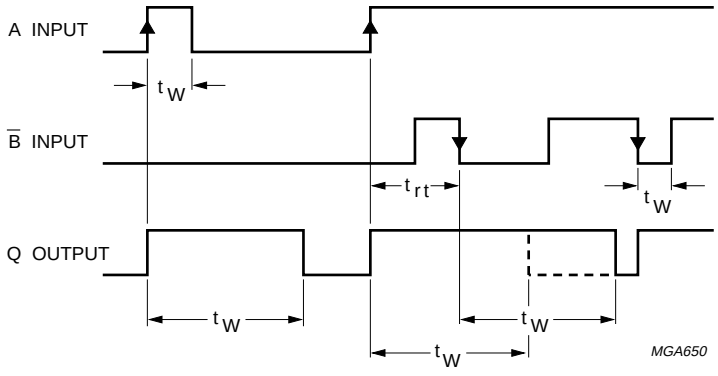
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the clock (RS) to outputs (Q and $\overline{Q}$) propagation delays, the clock pulse width and the maximum clock frequency.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the clock (RS) to outputs (Q and $\overline{Q}$) propagation delays, the clock pulse width and the maximum clock frequency (Output waveforms are not synchronized with respect to the RS waveform).



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.10 Output pulse control using retrigger pulse (RTR/$\overline{RTR}$ = HIGH).

APPLICATION INFORMATION

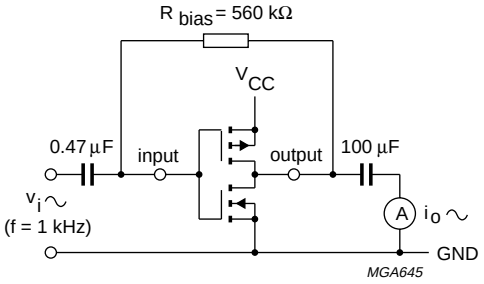


Fig.11 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see Fig.12) and MR = LOW.

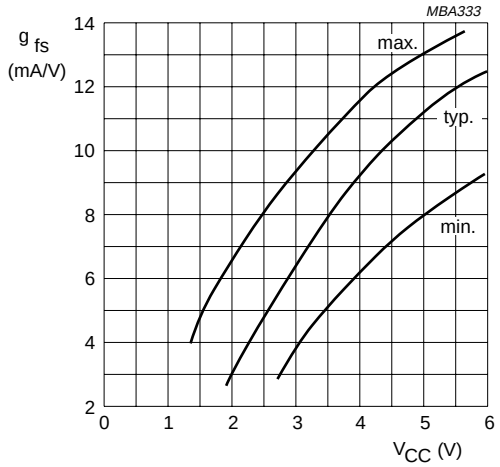
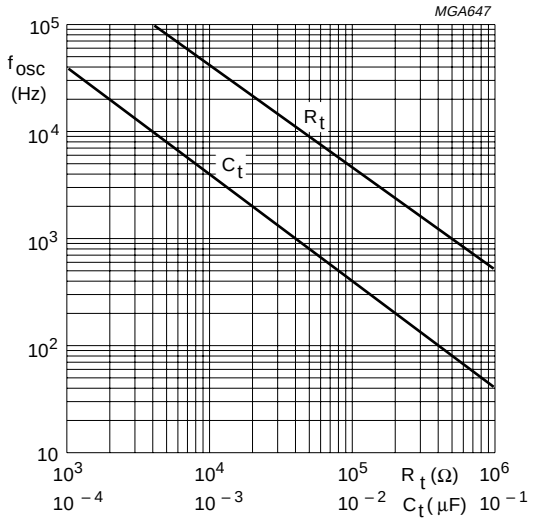


Fig.12 Typical forward transconductance g_{fs} as a function of the supply voltage at V_{CC} at T_{amb} = 25 °C.

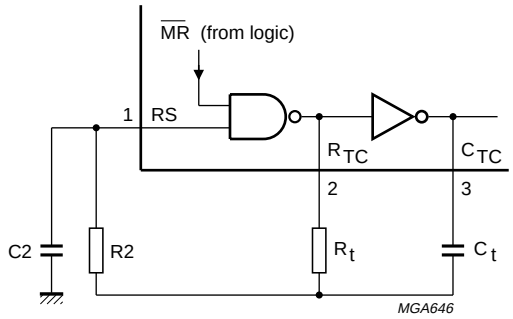


C_t curve at R_t = 100 kΩ; R2 = 200 kΩ.

R_t curve at C_t = 1 nF; R2 = 2 x R_t.

RC oscillator frequency as a function of R_t and C_t at V_{CC} = 2 to 6 V; T_{amb} = 25 °C.

Fig.13 Application information.



Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$$

Fig.14 Example of an RC oscillator.

Timing Component Limitations

The oscillator frequency is mainly determined by R_tC_t, provided R2 ≈ $2R_t$ and R2C2 << R_tC_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the "ON" resistance in series with it, which typically is 280 Ω at V_{CC} = 2 V, 130 Ω at V_{CC} = 4.5 V and 100 Ω at V_{CC} = 6 V. The recommended values for these components to maintain agreement with the typical oscillation formula are:

C_t > 50 pF, up to any practical value, 10 kΩ < R_t < 1 MΩ.

In order to avoid start-up problems, R_t >> 1 kΩ.

Typical Crystal Oscillator

In Fig.15, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ. Above 14 MHz it is recommended replacement of R2 by a capacitor with a typical value of 35 pF.

Accuracy

Device accuracy is very precise for long time delays and has an accuracy of better than 1% for short time delays (1% applies to values ≥ 400 ns). Tolerances are dependent on the external components used, either RC network or crystal oscillator.

Start-up Using External Clock

The start of the timing pulse is initiated directly by the trigger pulse (asynchronously with respect to the oscillator clock). Triggering on a clock HIGH or clock LOW results in the following:

- clock = HIGH; the timing pulse may be lengthened by a maximum of $t_W/2$ (t_W = clock pulse width)
- clock = LOW; the timing pulse may be shortened by a maximum of $t_W/2$ (t_W = clock pulse width).

This effect can be minimized by selecting more delay stages. When using only one or two delay stages, it is recommended to use an external time base that is synchronized with the negative-edge of the clock.

Start-up Using RC Oscillator

The first clock cycle is ≈35% of a time period too long. This effect can also be minimized by selecting more delay stages.

Start-up Using Crystal Oscillator

A crystal oscillator requires at least two clock cycles to start-up plus an unspecified period (ms) before the amplitude of the clock signal increases to its expected level. Although this device also operates at lower clock amplitudes, it is recommended to select the continuously running mode (OSC CON = HIGH) to prevent start-up delays.

Termination of the Timing Pulse

The end of the timing pulse is synchronized with the falling edge of the oscillator clock. The timing pulse may lose synchronization under the following conditions:

- high clock frequency and large number of stages are selected. This depends on the dynamic relationship that exists between the clock frequency and the ripple through delay of the subsequent stages.

Synchronization

When frequencies higher than those specified in the Table 'Synchronization limits' are used, the termination of timing pulse will lose synchronization with the falling edge of the oscillator. The unsynchronized timing pulse introduces errors, which can be minimized by increasing the number of stages used e.g. a 20 MHz clock frequency using all 24 stages will result in a frequency division of 16 777 225 instead of 16 777 216, an error of 0.0005%.

The amount of error increases at high clock frequencies as the number of stages decrease. A clock frequency of 40 MHz and 4 stages selected results in a division of 18 instead of 16, a 12.5% error. Application example:

- If a 400 ns timing pulse was required it would be more accurate to utilize a 5 MHz clock frequency using 1 stage or a 10 MHz clock frequency using 2 stages (due to synchronization with falling edge of the oscillator) than a 40 MHz clock frequency and 4 stages (synchronization is lost).

Minimum Output Pulse Width

The minimum output pulse width is determined by the minimum clock pulse width, plus the maximum propagation delay of A, $\overline{B}$ to Q. The rising edge of Q is dominated by the A, $\overline{B}$ to Q propagation delay, while the falling edge of Q is dominated by RS to Q propagation delay. These propagation delays are not equal. The RS to Q propagation delay is some what longer, resulting in inaccurate outputs for extremely short pulses. The propagation delays are listed in the section 'AC Characteristics'. With these numbers it is possible to calculate the maximum deviation (an example is shown in Fig.16).
Figure 16 is valid for an external clock where the trigger is synchronized to the falling edge of the clock only. The graph shows that the minimum programmed pulse width of 100 ns is:

- minimum of 4% too long
- typically 7% too long
- maximum of 10% too long.

SYNCHRONIZATION LIMITS

NUMBER OF STAGES SELECTED	CLOCK FREQUENCY (TYPICAL)
1	18 MHz
2	14 MHz
3	11 MHz
4	9.6 MHz
5	8.3 MHz
6	7.3 MHz
7	6.6 MHz
8	6 MHz
.	.
17	3.2 MHz
18	3.0 MHz
19	2.9 MHz
20	2.8 MHz
21	2.7 MHz
22	2.6 MHz
23	2.5 MHz
24	2.4 MHz

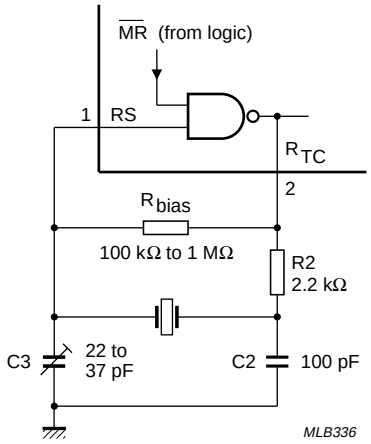


Fig.15 External components configuration for a crystal oscillator.

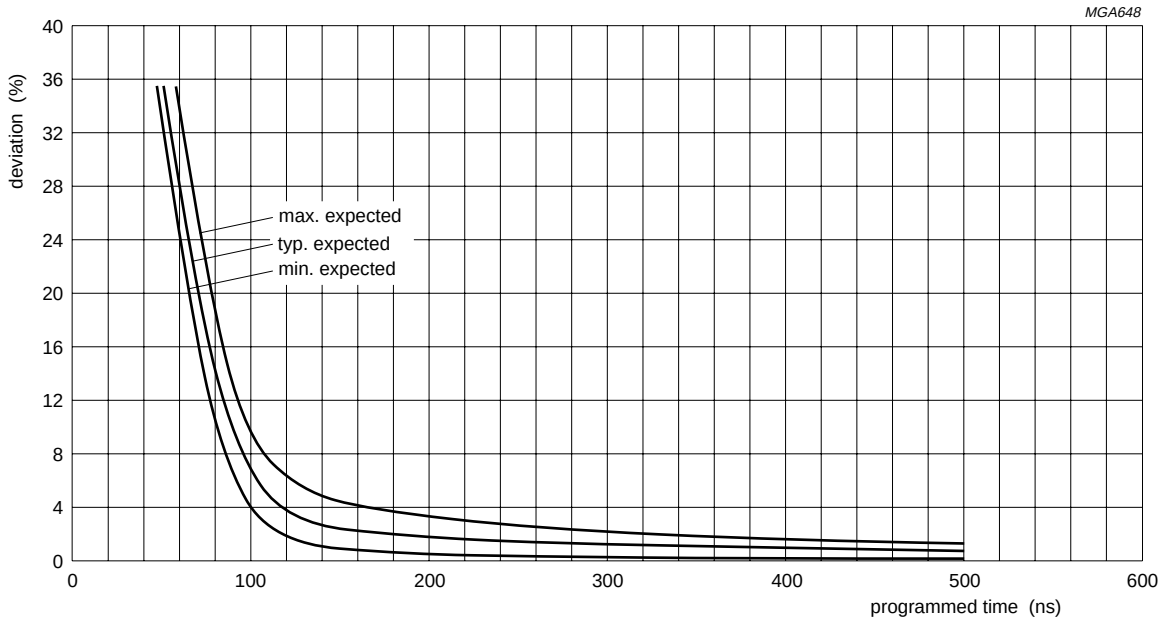


Fig.16 Graphic representation of short time delay accuracy; one stage selected; V_{CC} = 4.5 V.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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