



# **N-Channel Power MOSFET**

40V, 3.9A, 45mΩ

#### **FEATURES**

- Advance Trench Process Technology
- High density cell design for Ultra Low On-resistance
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

KEY PERFORMANCE PARAMETERS				
PARAMETER		VALUE	UNIT	
$V_{DS}$		40	V	
R <sub>DS(on)</sub> (max)	V <sub>GS</sub> = 10V	45	0	
	$V_{GS} = 4.5V$	62.5	mΩ	
Q	g	10	nC	



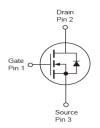




#### **APPLICATION**

- Load Switch
- Stepper Motors





Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V <sub>DS</sub>	40	V	
Gate-Source Voltage	$V_{GS}$	±20	V	
Continuous Drain Current (Note 1)	I <sub>D</sub>	3.9	А	
Pulsed Drain Current (Note 2)	I <sub>DM</sub>	16	А	
Total Power Dissipation @ T <sub>A</sub> = 25°C	P <sub>DTOT</sub>	1.25	W	
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	- 55 to +150	°C	

THERMAL PERFORMANCE					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction to Case Thermal Resistance	R <sub>eJC</sub>	50	°C/W		
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	100	°C/W		

**Notes:**  $R_{\Theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\Theta JA}$  is guaranteed by design while  $R_{\Theta CA}$  is determined by the user's board design.  $R_{\Theta JA}$  shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.



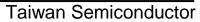


<b>ELECTRICAL SPECIFICATIONS</b> (T <sub>A</sub> = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 3)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV <sub>DSS</sub>	40			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V <sub>GS(TH)</sub>	1		3	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 32V, V_{GS} = 0V$	I <sub>DSS</sub>			1.0	μA
	$V_{GS} = 10V, I_D = 3.9A$	_		36	45	mΩ
Drain-Source On-State Resistance	$V_{GS} = 4.5V, I_D = 3.5A$	$R_{DS(on)}$		50	62.5	
Dynamic (Note 4)						
Total Gate Charge		Qg		10		
Gate-Source Charge	$V_{DS} = 20V, I_D = 3.9A,$	$Q_{gs}$		1.6		nC
Gate-Drain Charge	$V_{GS} = 10V$	$Q_{gd}$		2.1		
Input Capacitance		C <sub>iss</sub>		540		
Output Capacitance	$V_{DS} = 20V, V_{GS} = 0V,$ f = 1.0MHz	C <sub>oss</sub>		80		pF
Reverse Transfer Capacitance		C <sub>rss</sub>		45		
Switching (Note 5)						
Turn-On Delay Time		t <sub>d(on)</sub>		5		
Turn-On Rise Time	$\begin{aligned} V_{DD} &= 20 \text{V}, \ R_L &= 20 \Omega, \\ I_D &= 1 \text{A}, \ V_{GEN} &= 10 \text{V}, \\ R_G &= 6 \Omega \end{aligned}$	t <sub>r</sub>		12		
Turn-Off Delay Time		t <sub>d(off)</sub>		20		ns
Turn-Off Fall Time		t <sub>f</sub>		15		
Source-Drain Diode (Note 3)						
Forward On Voltage	I <sub>S</sub> = 1.25A, V <sub>GS</sub> = 0V	V <sub>SD</sub>		0.8	1.2	V

# Notes:

- 1. Current limited by package
- 2. Pulse width limited by the maximum junction temperature
- 3. Pulse test: PW  $\leq$  300 $\mu$ s, duty cycle  $\leq$  2%
- 4. For DESIGN AID ONLY, not subject to production testing.
- 5. Switching time is essentially independent of operating temperature.

Version: C15





# **ORDERING INFORMATION**

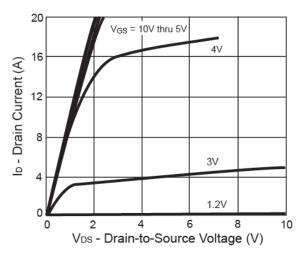
PART NO.	PACKAGE	PACKING
TSM2318CX RFG	SOT-23	3,000pcs / 7" Reel



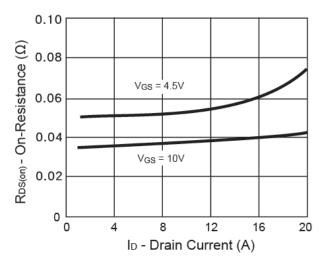
#### **CHARACTERISTICS CURVES**

 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$ 

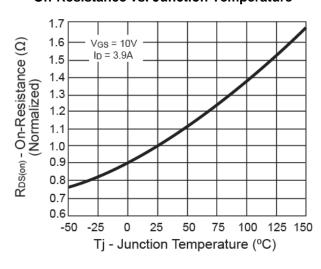
# **Output Characteristics**



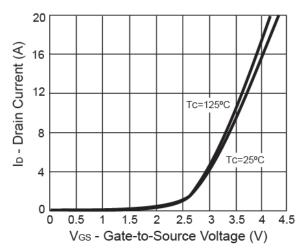
#### **On-Resistance vs. Drain Current**



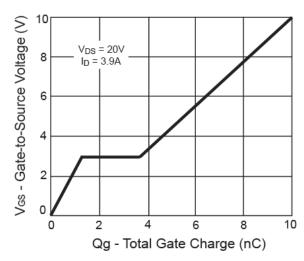
# On-Resistance vs. Junction Temperature



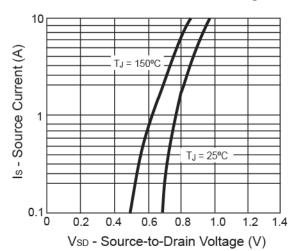
### **Transfer Characteristics**



### **Gate Charge**



### Source-Drain Diode Forward Voltage

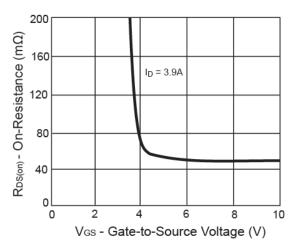




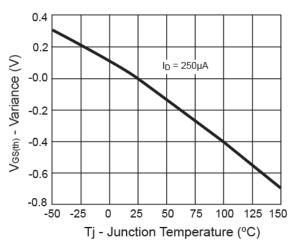
#### **CHARACTERISTICS CURVES**

(Tc = 25°C unless otherwise noted)

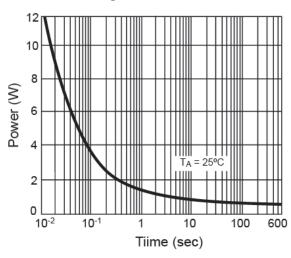
#### On-Resistance vs. Gate-Source Voltage



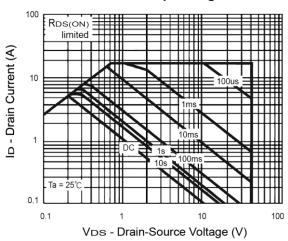
### Threshold Voltage



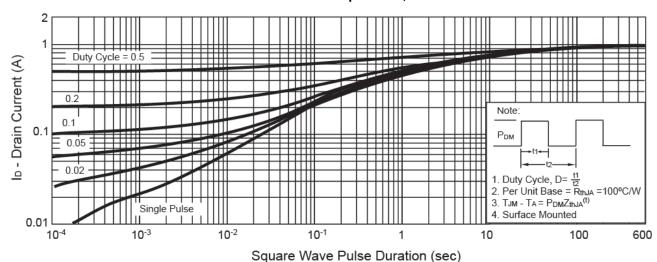
#### **Single Pulse Power**



#### Maximum Safe Operating Area

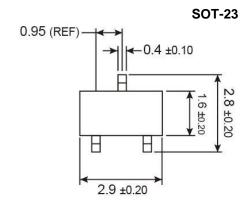


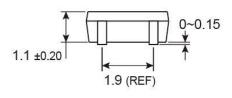
#### Normalized Thermal Transient Impedance, Junction-to-Ambient

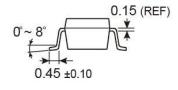




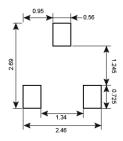
# PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



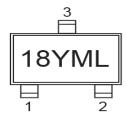




#### SUGGESTED PAD LAYOUT



# **MARKING DIAGRAM**



Y = Year Code

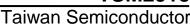
**M** = Month Code for Halogen Free Product

O =Jan P =Feb Q =Mar R =Apr

 $S = May \quad T = Jun \quad U = Jul \quad V = Aug$ 

W = Sep X = Oct Y = Nov Z = Dec

L = Lot Code (1~9, A~Z)





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