







Pin Definition: 1. Gate

Source
Drain

DDODUCT	
PRODUCI	SUMMARY

V _{DS} (V)	R _{DS(on)} (max)	I _D (mA)
	2 @ V _{GS} = 10V	300
60	4 @ V _{GS} = 4.5V	200

TSM2N7002K

60V N-Channel MOSFET

Features

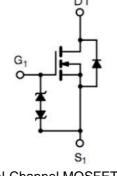
- Low On-Resistance
- ESD Protected 2KV
- High Speed Switching
- Low Voltage Drive

Ordering Information

Part No.	Package	Packing
TSM2N7002KCX RFG	SOT-23	3kpcs / 7" Reel

Note: "G" denotes for Halogen Free

Block Diagram



N-Channel MOSFET

Absolute Maximum Ratings (T _A =25°C unless otherwise noted)					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V _{GS}	±20	V	
Drain Current	Continuous @ T _A =25°C	I _D	300	mA	
	Pulsed	I _{DM}	800		
	Continuous @ T _A =25°C	I _{DR}	300	mA	
Drain Reverse Current	Pulsed	I _{DMR}	800		
Maximum Power Dissipation		P _D	300	mW	
Operating Junction Temperature		Τ _J	+150	°C	
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C	

Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	TL	5	S
Junction to Ambient Thermal Resistance (PCB mounted)	R _{eja}	350	°C/W

Notes:

a. Pulse width ≤300µs, Duty cycle ≤2%

b. When the device is mounted on a glass epoxy board with area measuring 1 x 0.75 x 0.62 inch.

c. The power dissipation of the package may result in a continuous drain current.



Electrical Specifications (T₄=25°C, unless otherwise noted)

TAIWAN

Pb

OH

COMPLIANCE

MICONDUCTOR

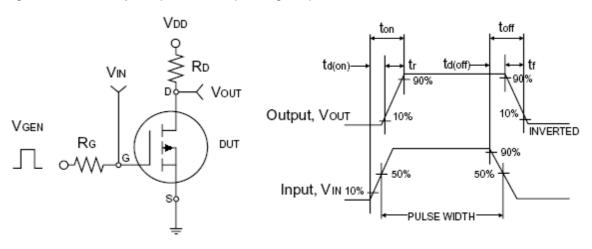
Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_{D} = 250 \mu A$	BV _{DSS}	60			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V _{GS(TH)}	1.0	1.5	2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I _{GSS}			±10	μA
Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V	I _{DSS}			1.0	μA
	V_{GS} =10V, I _D =300mA			1.2	2	Ω
Drain-Source On-State Resistance	V _{GS} =4.5V, I _D =200mA	R _{DS(ON)}		2	4	
Forward Transconductance	V _{DS} =10V, I _D =200mA	g _{fs}	100			mS
Diode Forward Voltage	I _S =300mA, V _{GS} =0V	V _{SD}		0.8	1.4	V
Dynamic ^b						
Total Gate Charge	$V_{DS} = 10V, I_D = 250mA, V_{GS} = 4.5V$	Qg		0.4	0.6	nC
Input Capacitance		C _{iss}		30		
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$	C _{oss}		6		pF
Reverse Transfer Capacitance	f = 1.0MHz	C _{rss}		2.5		
Switching ^c						
Turn-On Delay Time	V_{DD} =30V, R_{G} =10 Ω	t _{d(on)}			25	
Turn-Off Delay Time	I _D =200mA, V _{GEN} =10V,	t _{d(off)}			35	ns

Notes:

a. pulse test: PW \leq 300µs, duty cycle \leq 2%

b. For DESIGN AID ONLY, not subject to production testing.

c. Switching time is essentially independent of operating temperature.



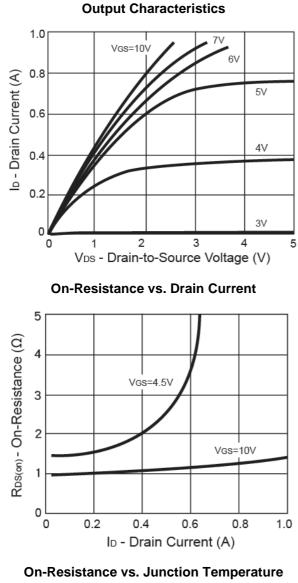
Switching Test Circuit

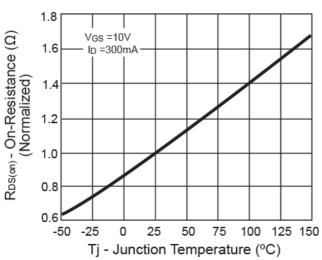
Switchin Waveforms

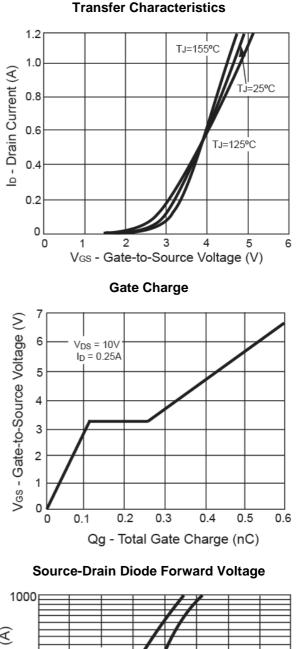


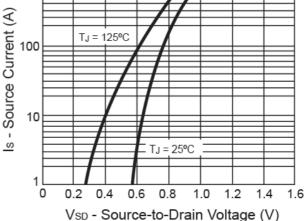
TSM2N7002K 60V N-Channel MOSFET

Electrical Characteristics Curve (T_A=25°C, unless otherwise noted)





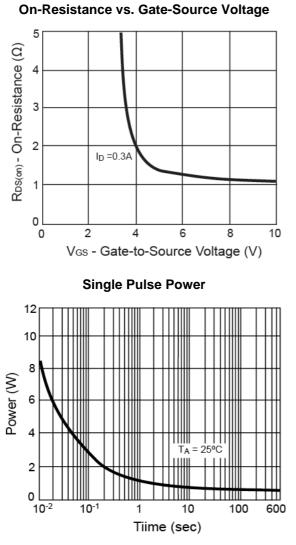


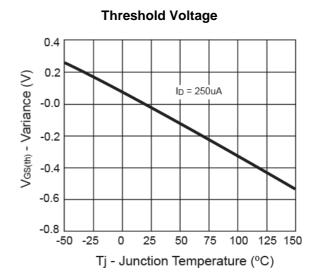




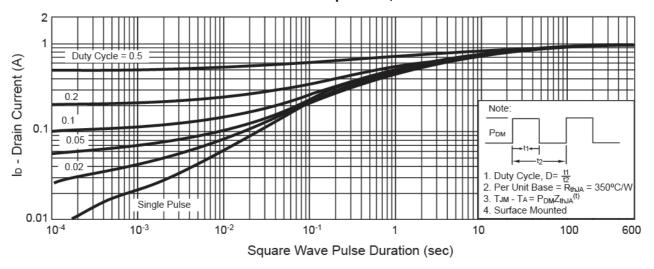
TSM2N7002K 60V N-Channel MOSFET

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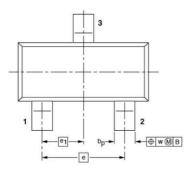


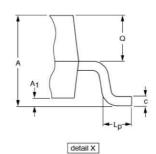
Normalized Thermal Transient Impedance, Junction-to-Ambient

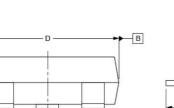


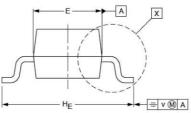


SOT-23 Mechanical Drawing



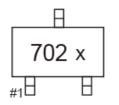






SOT-23 DIMENSION				
DIM	MILLIMETERS		ERS INCHES	
DIIVI	MIN	MAX	MIN	MAX.
А	1.00	BSC	0.039	BSC
A1	-	0.10	-	0.004
bp	0.37	0.42	0.014	0.016
С	0.09	0.15	0.004	0.005
D	2.80	3.00	0.110	0.118
Е	1.20	1.40	0.047	0.055
е	1.9	1.9 BSC		BSC
e1	0.95	BSC	0.037	BSC
H_{E}	2.35	2.45	0.093	0.096
L _P	0.15	0.45	0.005	0.018
Q	0.45	0.55	0.018	0.022
V	0.2 BSC		0.2 BSC 0.007 BSC	
W	0.1 BSC		0.004	BSC

Marking Diagram



- 702 = TSM2N7002KCX Device Code
 - = Internal Code

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TSM2N7002K 60V N-Channel MOSFET

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