



Features

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TSM35N10 100V N-Channel Power MOSFET

TO-252 (DPAK)

Advanced Trench Technology

Low Crss typical @ 45pF (Typ.)

Low gate charge typical @ 34nC (Typ.)

Note: "G" denote for Halogen Free Product

Low $R_{DS(ON)} 37m\Omega$ (Max.)

Ordering Information

Part No.

TSM35N10CP ROG

Pin Definition:

1. Gate 2. Drain

3. Source

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (mΩ)	I _D (A)
100	37 @ V _{GS} =10V	32

Block Diagram

Gate O

N-Channel MOSFET

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Package

TO-252

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	100	V	
Gate-Source Voltage		V _{GS}	±20	V	
	T _C =25℃		32		
	T _C =70℃		26	А	
Continuous Drain Current	T _A =25℃	– I _D	5		
	T _A =70℃		4		
Drain Current-Pulsed Note 1		I _{DM}	70	А	
Avalanche Current, L=0.1mH		I _{AS} , I _{AR}	35	А	
Avalanche Energy, L=0.1mH		E _{AS} , E _{AR}	61	mJ	
Movimum Dower Dissinction	T _C =25℃		83.3		
	T _C =70℃		53.3	W	
Maximum Power Dissipation	T _A =25℃	– P _D	2		
	T _A =70℃		1.3		
Storage Temperature Range		T _{STG}	-55 to +150	ĉ	
Operating Junction Temperature Range		TJ	-55 to +150	ĉ	

Packing

2.5Kpcs / 13" Reel

* Limited by maximum junction temperature

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	RƏ _{JC}	1.5	°C/W
Thermal Resistance - Junction to Ambient	RƏ _{JA}	62	°C/W



Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Uni
Static						1
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_{D} = 250uA$	BV _{DSS}	100			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 10A$	R _{DS(ON)}		30	37	mΩ
	$V_{GS} = 4.5V, I_D = 10A$	R _{DS(ON)}		32	42	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 uA$	V _{GS(TH)}	1	2	3	V
Zero Gate Voltage Drain Current	$V_{DS} = 100V, V_{GS} = 0V$	I _{DSS}			1	uA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I _{GSS}			±100	nA
Dynamic					•	
Total Gate Charge	$V_{DS} = 50V, I_D = 10A,$ $V_{GS} = 10V$	Qg		34		nC
Gate-Source Charge		Q _{gs}		6		
Gate-Drain Charge		Q_gd		9		
Input Capacitance	$V_{\rm DS} = 30 \text{V}, \text{ V}_{\rm GS} = 0 \text{V},$	C _{iss}		1598		pF
Output Capacitance		C _{oss}		132		
Reverse Transfer Capacitance	f = 1.0MHz	C _{rss}		45		
Switching						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 50V,$ $R_G = 3\Omega$	t _{d(on)}		7		
Turn-On Rise Time		t _r		7		
Turn-Off Delay Time		t _{d(off)}		29		nS
Turn-Off Fall Time		t _f		7		
Drain-Source Diode Characteristic	s and Maximum Rating					
Drain-Source Diode Forward Voltage	V _{GS} =0V, I _S =10A	V _{SD}		0.7		V
Reverse Recovery Time	I _S = 10A, T _J =25 °C	t _{fr}		32		nS
Reverse Recovery Charge	dl/dt = 500A/us	Q _{fr}		200		nC

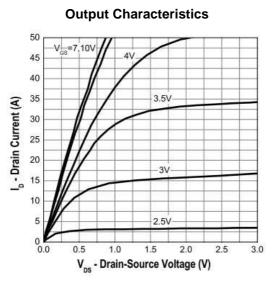
Notes:

1. Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2%.

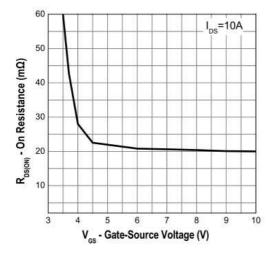
 $R\theta_{JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal 2. reference is defined as the solder mounting surface of the drain pins. $R\theta_{JC}$ is guaranteed by design while $R\theta_{CA}$ is determined by the user's board design. R0JA shown below for single device operation on FR-4 in still air



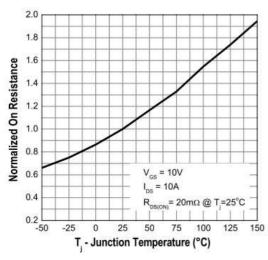
Electrical Characteristics Curve (Tc = 25°C, unless otherwise noted)

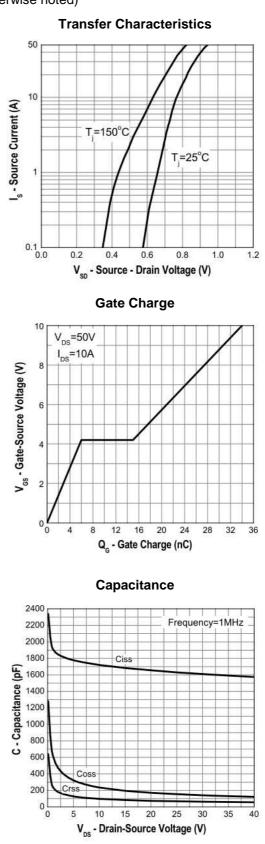


On-Resistance vs. Gate-Source Voltage



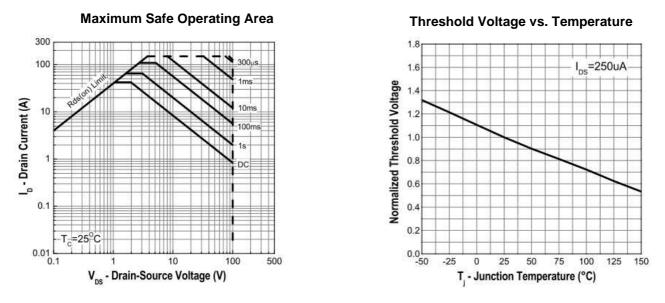
On-Resistance vs. Junction Temperature



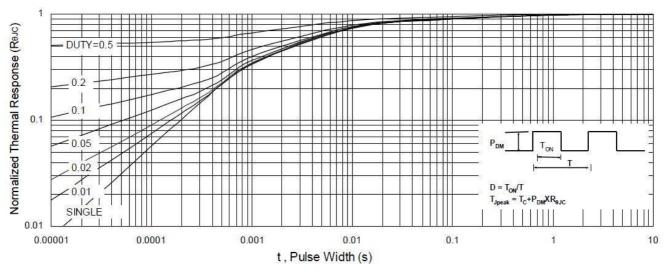




Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

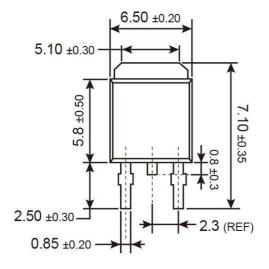


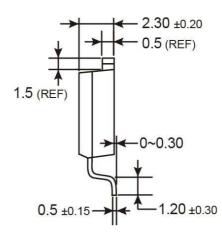
Normalized Thermal Transient Impedance, Junction-to-Ambient





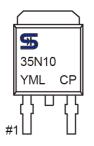
TO-252 Mechanical Drawing





Unit: Millimeters

Marking Diagram



- **Y** = Year Code
- M = Month Code for Halogen Free Product
 (O=Jan, P=Feb, Q=Mar, R=Apl, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)
- L = Lot Code



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