

TSM4424

20V N-Channel MOSFET



SOP-8



Pin Definition:

1. Source	8. Drain
Source	Drain
Source	Drain
4. Gate	5. Drain

Key Parameter Performance

Parameter	Value	Unit	
V _{DS}	20	V	
R _{DS(on)} (max)	30	mΩ	
Q_g	11.2	nC	

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

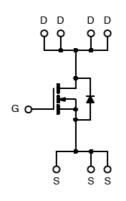
- Specially Designed for Li-on Battery Packs
- Battery Switch Application

Ordering Information

Part No.	Package	Packing
TSM4424CS RLG	SOP-8	2.5Kpcs / 13" Reel
TSM4424CS RVG	SOP-8	3Kpcs / 13" Reel

Note: "G" denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds

Block Diagram



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current		I _D	8	Α
Pulsed Drain Current (Note 1)		I _{DM}	30	Α
Continuous Source Current (Diode Conduction)		I _S	2.2	Α
Maximum Power Dissipation	Ta = 25°C	P _D	2.5	W
	Ta = 75°C		1.3	
Operating Junction Temperature		TJ	+150	°C
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance Junction to Foot	$R_{\Theta JF}$	25	°C/W
Thermal Resistance Junction to Ambient	R _{OJA}	52.5	°C/W





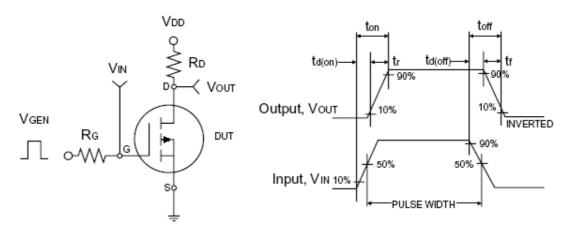
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Electrical Specifications

Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static ^(Note 2)						<u>'</u>
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250uA$	BV _{DSS}	20			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250uA$	V _{GS(TH)}	-	0.65	1	V
Gate Body Leakage	$V_{GS} = \pm 8V, V_{DS} = 0V$	I _{GSS}	1		±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 20V, V_{GS} = 0V$	I _{DSS}	-		1.0	uA
On-State Drain Current	$V_{DS} = 5V, V_{GS} = 4.5V$	I _{D(ON)}	30			Α
			1	23	30	mΩ
Drain-Source On-State Resistance		R _{DS(ON)}	1	25	35	
	$V_{GS} = 1.8V, I_D = 2.0A$		1	35	45	
Forward Transconductance	$V_{DS} = 10V, I_{D} = 6A$	g _{fs}	1	40		S
Diode Forward Voltage	$I_S = 1.7A, V_{GS} = 0V$	V_{SD}		0.8	1.2	V
Dynamic ^(Note 3)						
Total Gate Charge	101/ 1 154	Q_g		11.2	14	
Gate-Source Charge	$V_{DS} = 10V, I_D = 4.5A,$	Q_gs		1.4		nC
Gate-Drain Charge	V _{GS} = 4.5V	Q_{gd}		2.2		
Input Capacitance	101/1/	C_{iss}		500		
Output Capacitance	$V_{DS} = 10V, V_{GS} = 0V,$	C_{oss}	1	300		pF
Reverse Transfer Capacitance	f = 1.0MHz	C_{rss}	1	140		
Switching ^(Note 4)						
Turn-On Delay Time	$V_{DD} = 10V, R_{L} = 10\Omega,$ $I_{D} = 1A, V_{GEN} = 4.5V,$ $R_{G} = 6\Omega$	t _{d(on)}	1	15	25	
Turn-On Rise Time		t _r	-	30	60	
Turn-Off Delay Time		t _{d(off)}		35	70	ns
Turn-Off Fall Time		t _f		15	45	

Notes:

- 1. Pulse width limited by the maximum junction temperature
- 2. Pulse test: PW \leq 300 μ s, duty cycle \leq 2%
- 3. For DESIGN AID ONLY, not subject to production testing.
- 4. Switching time is essentially independent of operating temperature.



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Switching Test Circuit

Switchin Waveforms



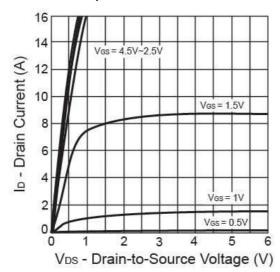
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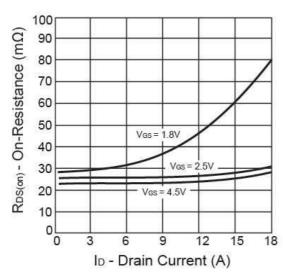


Electrical Characteristics Curve

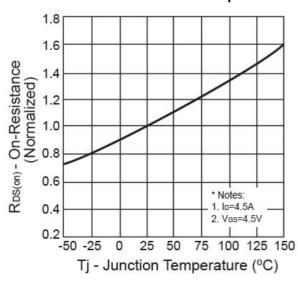
Output Characteristics



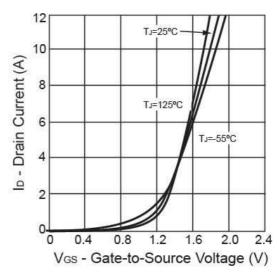
On-Resistance vs. Drain Current



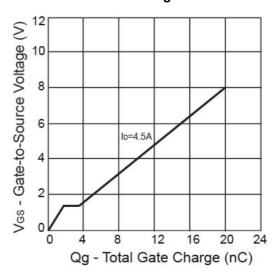
On-Resistance vs. Junction Temperature



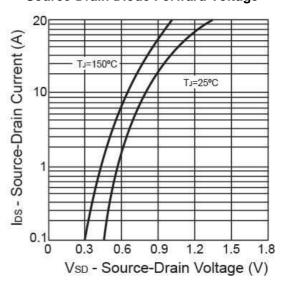
Transfer Characteristics



Gate Charge



Source-Drain Diode Forward Voltage



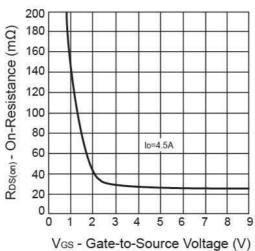
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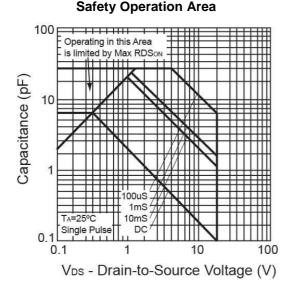


Electrical Characteristics Curve

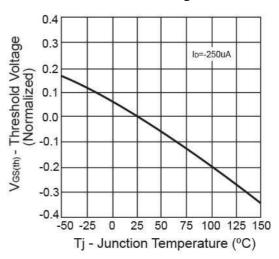
On-Resistance vs. Gate-Source Voltage



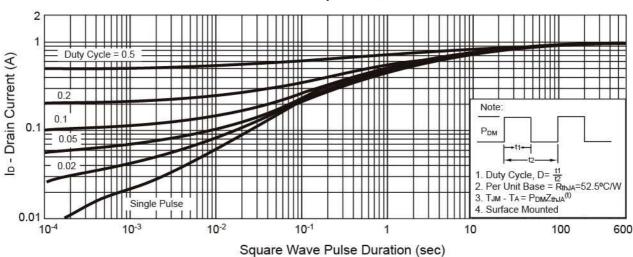
vos cute to course voltage



Threshold Voltage



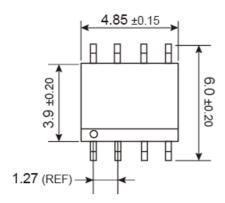
Normalized Thermal Transient Impedance, Junction-to-Ambient

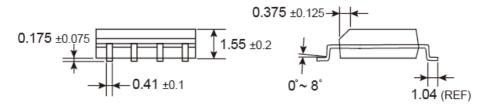






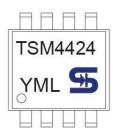
SOP-8 Mechanical Drawing





Unit: Millimeters

Marking Diagram



Y = Year Code

M = Month Code for Halogen Free Product

 $oldsymbol{O}$ =Jan $oldsymbol{P}$ =Feb $oldsymbol{Q}$ =Mar $oldsymbol{R}$ =Apr

 $S = May \quad T = Jun \quad U = Jul \quad V = Aug$

W =Sep X =Oct Y =Nov Z =Dec

L = Lot Code



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