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Kind regards,

Team Nexperia

DATA SHEET

74LVT162373

**3.3 V LVT 16-bit transparent D-type latch
with 30 Ω termination resistors (3-State)**

Product specification

1999 Sep 23

IC23 Data Handbook

3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

74LVT162373

FEATURES

- 16-bit transparent latch
- 3-State buffers
- Output capability: +12 mA / -12 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30 Ω making external resistors unnecessary
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74LVT162373 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) input is High, the Q outputs follow the data (D) inputs. When Latch Enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

The 74LVT162373 is designed with 30 Ω series resistance in both the High and Low states of the output. This design reduces the noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}$ | TYPICAL | UNIT |
|------------------------|---------------------------------|--|---------|---------------|
| t_{PLH} t_{PHL} | Propagation delay nDx to nQx | $C_L = 50\text{ pF}$; $V_{CC} = 3.3\text{ V}$ | 3.0 | ns |
| C_{IN} | Input capacitance | $V_I = 0\text{ V}$ or 3.0 V | 3 | pF |
| C_{OUT} | Output capacitance | Outputs disabled; $V_O = 0\text{ V}$ or 3.0 V | 9 | pF |
| I_{CCZ} | Total supply current | Outputs disabled; $V_{CC} = 3.6\text{ V}$ | 70 | μA |

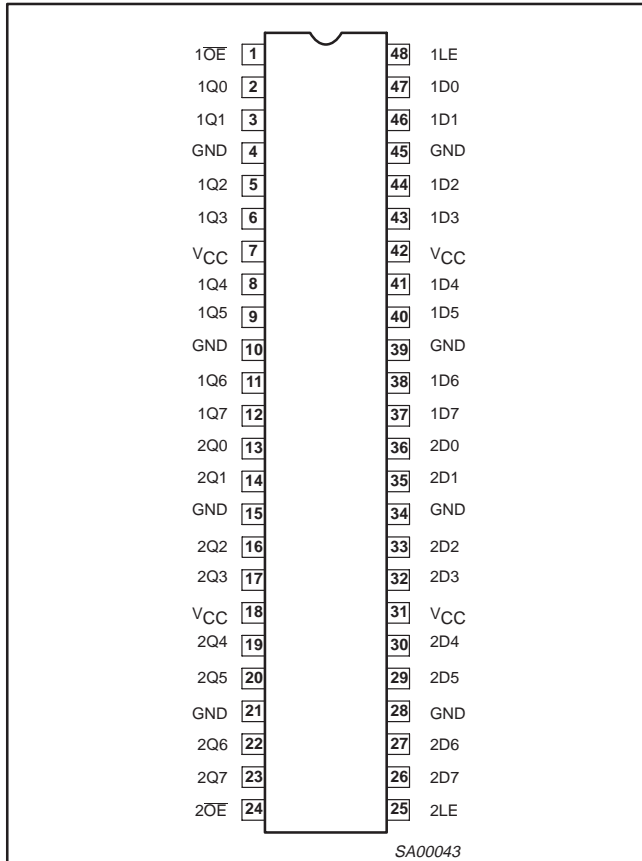
ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDERING CODE | DWG NUMBER |
|------------------------------|--|-----------------|------------|
| 48-Pin Plastic SSOP Type III | -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ | 74LVT162373 DL | SOT370-1 |
| 48-Pin Plastic TSSOP Type II | -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ | 74LVT162373 DGG | SOT362-1 |

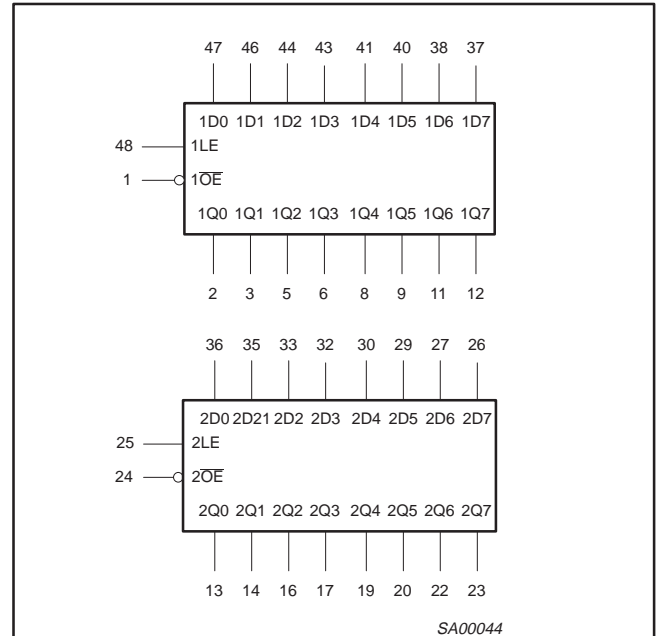
3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

74LVT162373

PIN CONFIGURATION



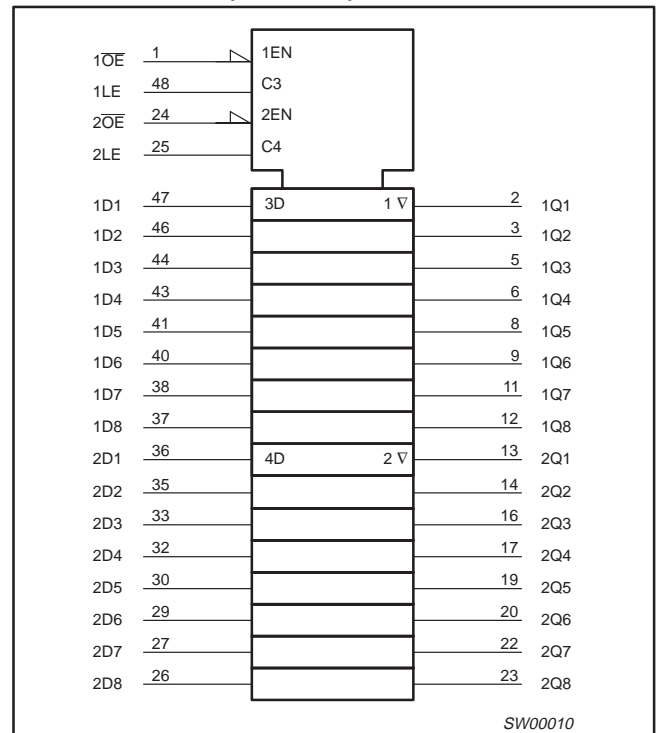
LOGIC SYMBOL



PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|--|------------------------|-----------------------------------|
| 47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26 | 1D0 – 1D7 2D0 – 2D7 | Data inputs |
| 2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23 | 1Q0 – 1Q7 2Q0 – 2Q7 | Data outputs |
| 1, 24 | 1OE, 2OE | Output Enable inputs (active-Low) |
| 48, 25 | 1LE, 2LE | Latch Enable inputs (active-High) |
| 4, 10, 15, 21, 28, 34, 39, 45 | GND | Ground (0V) |
| 7, 18, 31, 42 | VCC | Positive supply voltage |

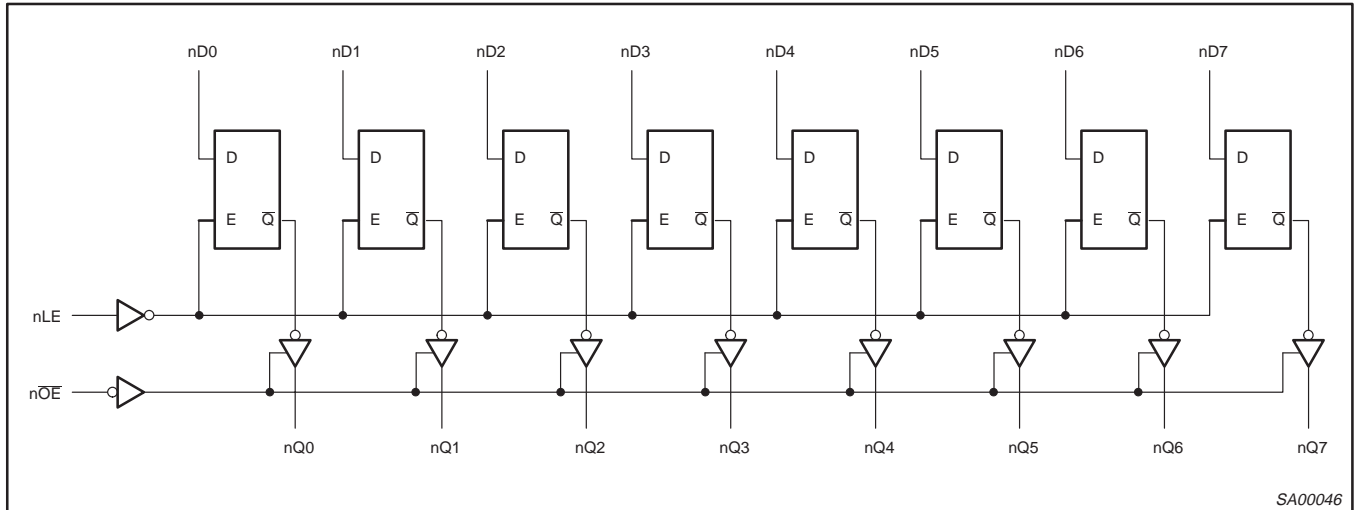
LOGIC SYMBOL (IEEE/IEC)



3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

74LVT162373

LOGIC DIAGRAM

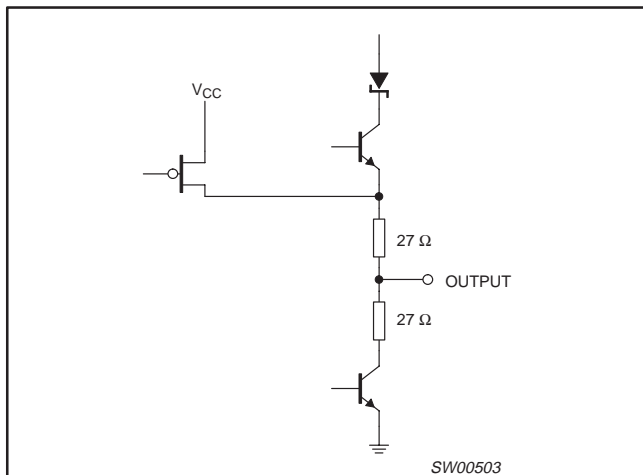


FUNCTION TABLE

| INPUTS | | | INTERNAL REGISTER | OUTPUTS | OPERATING MODE |
|--------|-----|-----|-------------------|-----------|--------------------------|
| nOE | nLE | nDx | | nQ0 – nQ7 | |
| L | H | L | L | L | Enable and read register |
| L | H | H | H | H | |
| L | ↓ | l | L | L | Latch and read register |
| L | ↓ | h | H | H | |
| L | L | X | NC | NC | Hold |
| H | L | X | NC | Z | Disable outputs |
| H | H | nDx | nDx | Z | |

- H = High voltage level
- h = High voltage level one set-up time prior to the High-to-Low E transition
- L = Low voltage level
- l = Low voltage level one set-up time prior to the High-to-Low E transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- ↓ = High-to-Low LE transition

SCHEMATIC OF EACH OUTPUT



3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

74LVT162373

ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|-----------|--------------------------------|-----------------------------|--------------|--------------------|
| V_{CC} | DC supply voltage | | -0.5 to +4.6 | V |
| I_{IK} | DC input diode current | $V_I < 0$ | -50 | mA |
| V_I | DC input voltage ³ | | -0.5 to +7.0 | V |
| I_{OK} | DC output diode current | $V_O < 0$ | -50 | mA |
| V_{OUT} | DC output voltage ³ | Output in Off or High state | -0.5 to +7.0 | V |
| I_{OUT} | DC output current | Output in Low state | 128 | mA |
| | | Output in High state | -64 | |
| T_{stg} | Storage temperature range | | -65 to +150 | $^{\circ}\text{C}$ |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 $^{\circ}\text{C}$.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---------------------|---|--------|-----|--------------------|
| | | MIN | MAX | |
| V_{CC} | DC supply voltage | 2.7 | 3.6 | V |
| V_I | Input voltage | 0 | 5.5 | V |
| V_{IH} | High-level input voltage | 2.0 | | V |
| V_{IL} | Input voltage | | 0.8 | V |
| I_{OH} | High-level output current | | -12 | mA |
| I_{OL} | Low-level output current | | 12 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate; Outputs enabled | | 10 | ns/V |
| T_{amb} | Operating free-air temperature range | -40 | +85 | $^{\circ}\text{C}$ |

3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

74LVT162373

DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|-----------------|--|--|------------------------|------------------|-----------|---------|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP ¹ | MAX | |
| V_{IK} | Input clamp voltage | $V_{CC} = 2.7V$; $I_{IK} = -18mA$ | | -0.85 | -1.2 | V |
| V_{OH} | High-level output voltage | $V_{CC} = 3.0V$; $I_{OH} = -12mA$ | 2.0 | | | |
| V_{OL} | Low-level output voltage | $V_{CC} = 3.0V$; $I_{OL} = 16mA$ | | | 0.8 | V |
| V_{RST} | Power-up output Low voltage ⁵ | $V_{CC} = 3.6V$; $I_O = 1mA$; $V_I = GND$ or V_{CC} | | 0.1 | 0.55 | V |
| I_I | Input leakage current | $V_{CC} = 3.6V$; $V_I = V_{CC}$ or GND | Control pins | 0.1 | ± 1 | μA |
| | | $V_{CC} = 0$ or $3.6V$; $V_I = 5.5V$ | | 0.4 | 10 | |
| | | $V_{CC} = 3.6V$; $V_I = V_{CC}$ | Data pins ⁴ | 0.1 | 1 | |
| | | $V_{CC} = 3.6V$; $V_I = 0$ | | -0.4 | -5 | |
| I_{OFF} | Output off current | $V_{CC} = 0V$; V_I or $V_O = 0$ to $4.5V$ | | 0.1 | ± 100 | μA |
| I_{HOLD} | Bus Hold current D inputs ⁷ | $V_{CC} = 3V$; $V_I = 0.8V$ | | 75 | 135 | μA |
| | | $V_{CC} = 3V$; $V_I = 2.0V$ | | -75 | -135 | |
| | | $V_{CC} = 0V$ to $3.6V$; $V_{CC} = 3.6V$ | | ± 500 | | |
| I_{EX} | Current into an output in the High state when $V_O > V_{CC}$ | $V_O = 5.5V$; $V_{CC} = 3.0V$ | | 50 | 125 | μA |
| $I_{PU/PD}$ | Power up/down 3-State output current ³ | $V_{CC} \leq 1.2V$; $V_O = 0.5V$ to V_{CC} ; $V_I = GND$ or V_{CC} ; OE/OE = Don't care | | 1 | ± 100 | μA |
| I_{OZH} | 3-State output High current | $V_{CC} = 3.6V$; $V_O = 3.0V$; $V_I = V_{IH}$ or V_{IL} | | 0.5 | 5 | μA |
| I_{OZL} | 3-State output Low current | $V_{CC} = 3.6V$; $V_O = 0.5V$; $V_I = V_{IH}$ or V_{IL} | | 0.5 | -5 | |
| I_{CCH} | Quiescent supply current | $V_{CC} = 3.6V$; Outputs High, $V_I = GND$ or V_{CC} , $I_O = 0$ | | 0.07 | 0.12 | mA |
| I_{CCL} | | $V_{CC} = 3.6V$; Outputs Low, $V_I = GND$ or V_{CC} , $I_O = 0$ | | 4.0 | 6 | |
| I_{CCZ} | | $V_{CC} = 3.6V$; Outputs Disabled; $V_I = GND$ or V_{CC} , $I_O = 0$ ⁶ | | 0.07 | 0.12 | |
| ΔI_{CC} | Additional supply current per input pin ² | $V_{CC} = 3V$ to $3.6V$; One input at $V_{CC}-0.6V$, Other inputs at V_{CC} or GND | | 0.1 | 0.2 | mA |

NOTES:

- All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From $V_{CC} = 1.2V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of 100 μ sec is permitted. This parameter is valid for $T_{amb} = 25^\circ C$ only.
- Unused pins at V_{CC} or GND.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

74LVT162373

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | UNIT |
|------------------------|--|----------|--------------------------|------------------|------------|-----------------|------|
| | | | $V_{CC} = 3.3V \pm 0.3V$ | | | $V_{CC} = 2.7V$ | |
| | | | MIN | TYP ¹ | MAX | MAX | |
| t_{PLH} t_{PHL} | Propagation delay nDx to nQx | 2 | 0.5 0.5 | 2.5 2.5 | 4.6 4.0 | 5.1 4.3 | ns |
| t_{PLH} t_{PHL} | Propagation delay nLE to nQx | 1 | 0.5 0.5 | 3.0 3.0 | 5.1 4.6 | 5.8 4.3 | ns |
| t_{PZH} t_{PZL} | Output enable time to High and Low level | 4 5 | 0.1 0.1 | 3.5 3.2 | 5.4 4.9 | 6.6 5.5 | ns |
| t_{PHZ} t_{PLZ} | Output disable time from High and Low Level | 4 5 | 0.1 0.1 | 3.5 3.2 | 5.4 5.1 | 5.7 5.0 | ns |

NOTE:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$.

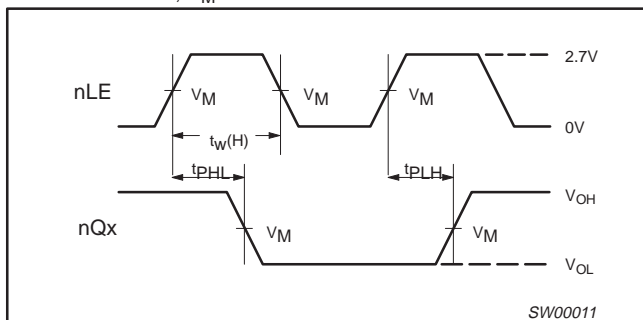
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

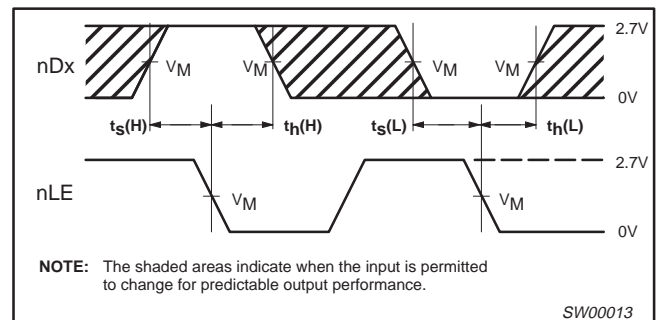
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|----------------------|--------------------------|----------|--------------------------|------------|-----------------|------|
| | | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | |
| | | | MIN | TYP | MIN | |
| $t_S(H)$ $t_S(L)$ | Setup time nDx to nLE | 3 | 1.5 2.0 | 0.1 0.2 | 1.0 2.0 | ns |
| $t_H(H)$ $t_H(L)$ | Hold time nDx to nLE | 3 | 1.0 1.5 | 0 0 | 1.0 2.0 | ns |
| $t_W(H)$ | nLE pulse width High | 1 | 1.5 | 0.5 | 1.5 | ns |

AC WAVEFORMS

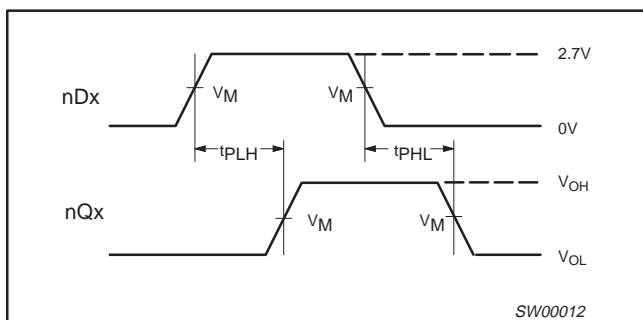
For all waveforms, $V_M = 1.5V$.



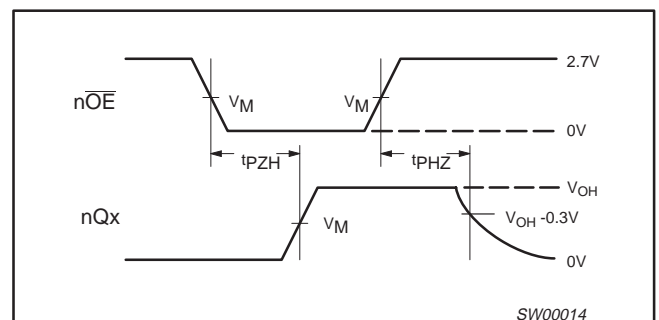
Waveform 1. Propagation Delay, Latch Enable to Output, and Latch Enable Pulse Width



Waveform 3. Data Setup and Hold Times



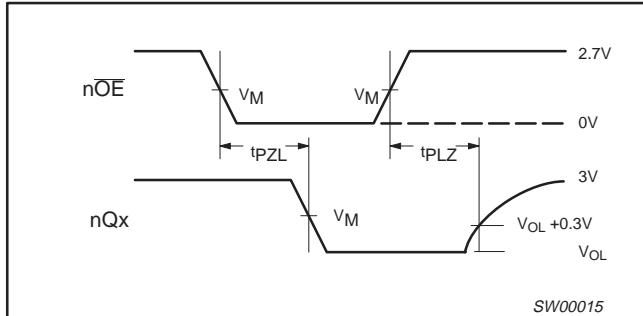
Waveform 2. Propagation Delay for Data to Outputs



Waveform 4. 3-State Output Enable time to High Level and Output Disable Time from High Level

3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

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Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION

| TEST | SWITCH |
|-------------------|--------|
| t_{PHZ}/t_{PZH} | GND |
| t_{PLZ}/t_{PZL} | 6V |
| t_{PLH}/t_{PHL} | open |

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

**$V_M = 1.5V$
Input Pulse Definition**

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|---------|--------------------------|---------------------|-------|---------------------|---------------------|
| | Amplitude | Rep. Rate | t_W | t_R | t_F |
| 74LVT16 | 2.7V | $\leq 10\text{MHz}$ | 500ns | $\leq 2.5\text{ns}$ | $\leq 2.5\text{ns}$ |

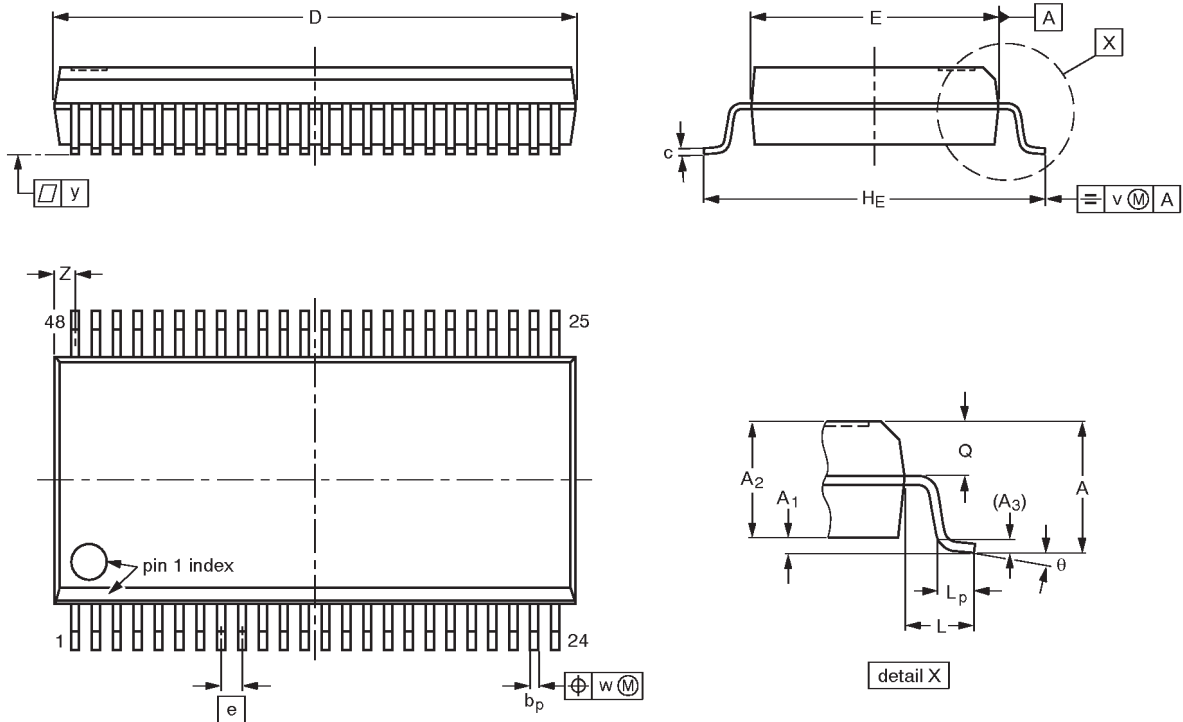
SW00003

3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

74LVT162373

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-------|----------------|-----|----------------|------------|------|------|-----|------------------|----------|
| mm | 2.8 | 0.4 0.2 | 2.35 2.20 | 0.25 | 0.3 0.2 | 0.22 0.13 | 16.00 15.75 | 7.6 7.4 | 0.635 | 10.4 10.1 | 1.4 | 1.0 0.6 | 1.2 1.0 | 0.25 | 0.18 | 0.1 | 0.85 0.40 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

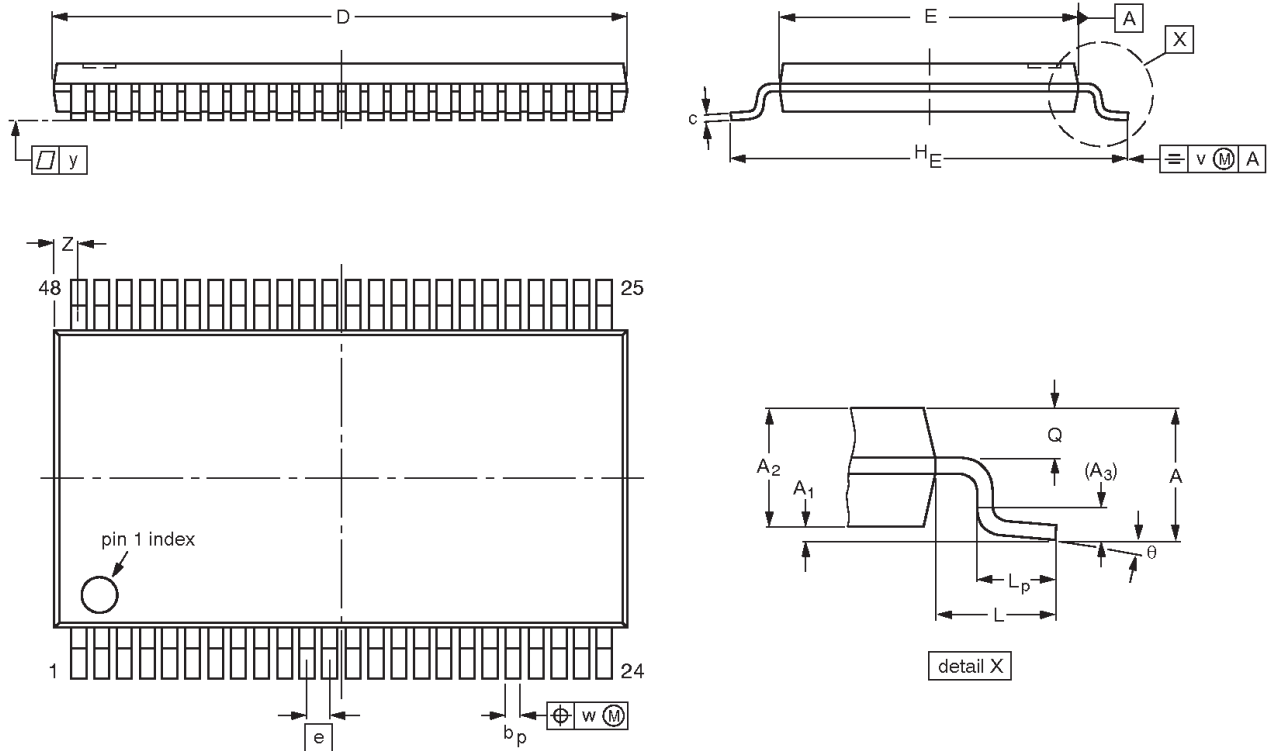
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|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT370-1 | | MO-118AA | | | | 93-11-02 95-02-04 |

3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

74LVT162373

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|-----|----------------|---|----------------|--------------|------|------|-----|------------|----------|
| mm | 1.2 | 0.15 0.05 | 1.05 0.85 | 0.25 | 0.28 0.17 | 0.2 0.1 | 12.6 12.4 | 6.2 6.0 | 0.5 | 8.3 7.9 | 1 | 0.8 0.4 | 0.50 0.35 | 0.25 | 0.08 | 0.1 | 0.8 0.4 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT362-1 | | MO-153ED | | | | 93-02-03 95-02-10 |

3.3 V LVT 16-bit transparent D-type latch
with 30 Ω termination resistors (3-State)

74LVT162373

NOTES

3.3 V LVT 16-bit transparent D-type latch with 30 Ω termination resistors (3-State)

74LVT162373

Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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[21](#) [2.T18.002-18](#) [2.T18.006-18](#) [CQ/AA-KEY](#) [CQ/A-M22X1,5-45-28](#) [CQ/A-M22X1,5-45-32](#) [M22-2-D5-2-21-01-P](#) [CY74FCT2373CTSOC](#)
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[74FCT573ATQG](#) [74LCX16373MTDX](#)