CMOS Digital Integrated Circuits Silicon Monolithic

# 74VHC573FT

## 1. Functional Description

- Octal D-Type Latch with 3-State Outputs

## 2. General

The 74VHC573FT is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate $C^2MOS$ technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

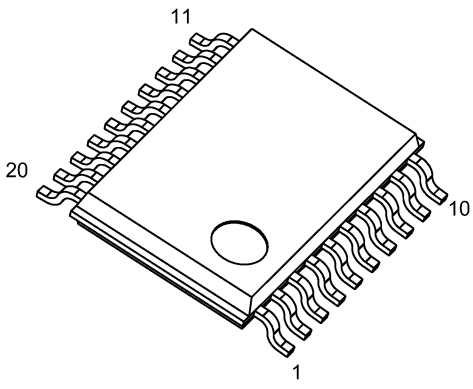
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## 3. Features

(1) AEC-Q100 (Rev. H) (Note 1)
(2) Wide operating temperature range: $T_{opr}$ = -40 to 125 °C
(3) High speed: $t_{pd}$ = 4.5 ns (typ.) at $V_{CC}$ = 5.0 V
(4) Low power dissipation: $I_{CC}$ = 4.0 μA (max) at $T_a$ = 25°C
(5) High noise immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (min)
(6) Power-down protection is provided on all inputs.
(7) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
(8) Wide operating voltage range: $V_{CC(opr)}$ = 2.0 V to 5.5 V
(9) Low noise: $V_{OLP}$ = 1.0 V (max)
(10) Pin and function compatible with the 74 series (74AC/HC/AHC/LV etc.) 573 type.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

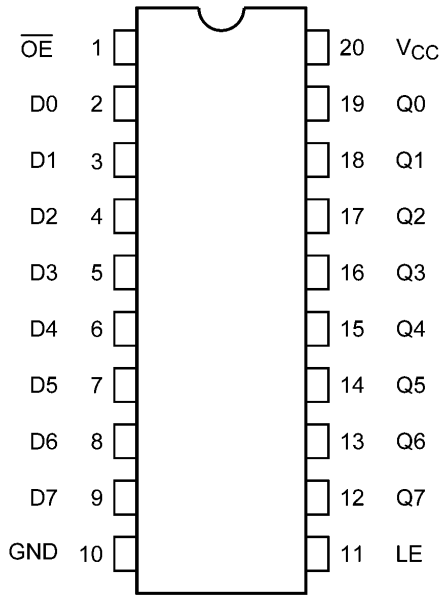
## 4. Packaging




TSSOP20B

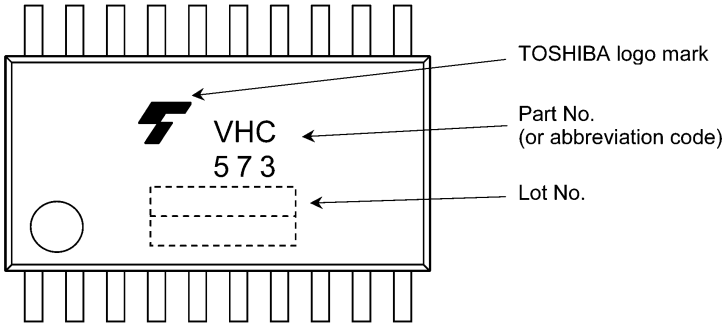
Start of commercial production
2013-03

## 5. Pin Assignment

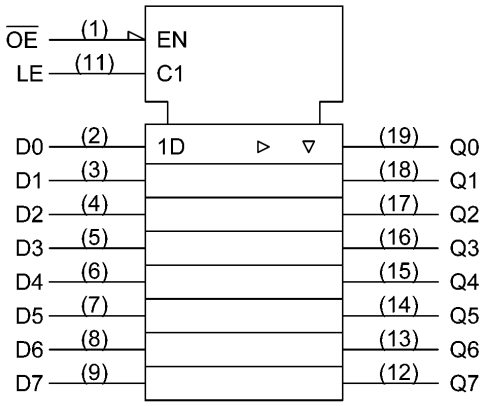



(top view)

## 6. Marking




## 7. IEC Logic Symbol

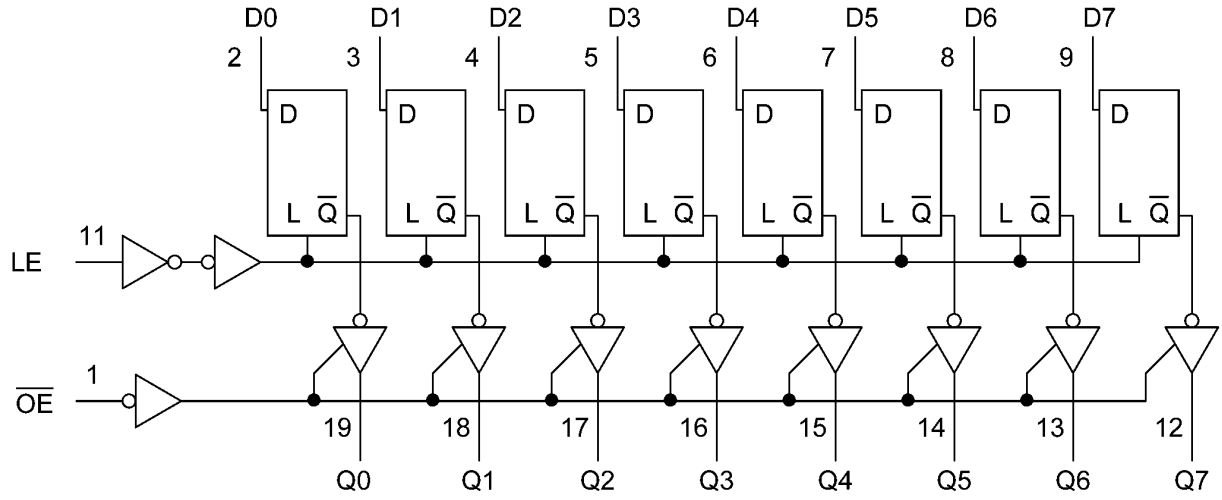


## 8. Truth Table

| INPUT $\overline{OE}$ | INPUT LE | INPUT D | OUTPUT |
|---|---|---|---|
| H | X | X | Z |
| L | L | X | Qn |
| L | H | L | L |
| L | H | H | H |

X: Don't care
Z: High impedance
Qn: Q outputs are latched at the time when the LE input is taken to low logic level.

## 9. System Diagram



## 10. Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Note | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | -0.5 to 7.0 | V |
| Input voltage | $V_{IN}$ | | -0.5 to 7.0 | V |
| Output voltage | $V_{OUT}$ | | -0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | | -20 | mA |
| Output diode current | $I_{OK}$ | | ±20 | mA |
| Output current | $I_{OUT}$ | | ±25 | mA |
| $V_{CC}$/ground current | $I_{CC}$ | | ±75 | mA |
| Power dissipation | $P_D$ | (Note 1) | 180 | mW |
| Storage temperature | $T_{stg}$ | | -65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of $T_a$ = -40 to 85 °C. From $T_a$ = 85 to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

## 11. Operating Ranges (Note)

| Characteristics | Symbol | Test Condition | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 2.0 to 5.5 | V |
| Input voltage | $V_{IN}$ | | 0 to 5.5 | V |
| Output voltage | $V_{OUT}$ | | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | | -40 to 125 | °C |
| Input rise and fall times | dt/dv | $V_{CC}$ = 3.3 ± 0.3 V | 0 to 100 | ns/V |
| | | $V_{CC}$ = 5.0 ± 0.5 V | 0 to 20 | |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either $V_{CC}$ or GND.

## 12. Electrical Characteristics

### 12.1. DC Characteristics (Unless otherwise specified, $T_a$ = 25 °C)

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 2.0 | 1.50 | — | — | V |
| | | | | 3.0 to 5.5 | $V_{CC}$ × 0.7 | — | — | |
| Low-level input voltage | $V_{IL}$ | — | | 2.0 | — | — | 0.50 | V |
| | | | | 3.0 to 5.5 | — | — | $V_{CC}$ × 0.3 | |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -50 μA | 2.0 | 1.9 | 2.0 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | |
| | | | $I_{OH}$ = -4 mA | 3.0 | 2.58 | — | — | |
| | | | $I_{OH}$ = -8 mA | 4.5 | 3.94 | — | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 2.0 | — | 0.0 | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 3.0 | — | — | 0.36 | |
| | | | $I_{OL}$ = 8 mA | 4.5 | — | — | 0.36 | |
| 3-state output OFF-state leakage current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.25 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 0 to 5.5 | — | — | ±0.1 | |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 4.0 | |

### 12.2. DC Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C)

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 2.0 | 1.50 | — | V |
| | | | | 3.0 to 5.5 | $V_{CC}$ × 0.7 | — | |
| Low-level input voltage | $V_{IL}$ | — | | 2.0 | — | 0.50 | V |
| | | | | 3.0 to 5.5 | — | $V_{CC}$ × 0.3 | |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -50 μA | 2.0 | 1.9 | — | V |
| | | | | 3.0 | 2.9 | — | |
| | | | | 4.5 | 4.4 | — | |
| | | | $I_{OH}$ = -4 mA | 3.0 | 2.48 | — | |
| | | | $I_{OH}$ = -8 mA | 4.5 | 3.80 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 2.0 | — | 0.1 | V |
| | | | | 3.0 | — | 0.1 | |
| | | | | 4.5 | — | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 3.0 | — | 0.44 | |
| | | | $I_{OL}$ = 8 mA | 4.5 | — | 0.44 | |
| 3-state output OFF-state leakage current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | ±2.50 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 0 to 5.5 | — | ±1.0 | |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | 40.0 | |

## 12.3. DC Characteristics (Unless otherwise specified, $T_a$ = -40 to 125 °C)

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 2.0 | 1.50 | — | V |
| | | | | 3.0 to 5.5 | $V_{CC}$ × 0.7 | — | |
| Low-level input voltage | $V_{IL}$ | — | | 2.0 | — | 0.50 | V |
| | | | | 3.0 to 5.5 | — | $V_{CC}$ × 0.3 | |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -50 μA | 2.0 | 1.9 | — | V |
| | | | | 3.0 | 2.9 | — | |
| | | | | 4.5 | 4.4 | — | |
| | | | $I_{OH}$ = -4 mA | 3.0 | 2.40 | — | |
| | | | $I_{OH}$ = -8 mA | 4.5 | 3.70 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 2.0 | — | 0.1 | V |
| | | | | 3.0 | — | 0.1 | |
| | | | | 4.5 | — | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 3.0 | — | 0.55 | |
| | | | $I_{OL}$ = 8 mA | 4.5 | — | 0.55 | |
| 3-state output OFF-state leakage current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | ±10.0 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 0 to 5.5 | — | ±2.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | 80.0 | μA |

### 12.4. Timing Requirements (Unless otherwise specified, $T_a$ = 25°C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Limit | Unit |
|---|---|---|---|---|---|
| Minimum pulse width (LE) | $t_{w(H)}$ | — | 3.3 ± 0.3 | 5.0 | ns |
| | | | 5.0 ± 0.5 | 5.0 | ns |
| Minimum setup time | $t_S$ | — | 3.3 ± 0.3 | 3.5 | ns |
| | | | 5.0 ± 0.5 | 3.5 | ns |
| Minimum hold time | $t_h$ | — | 3.3 ± 0.3 | 1.5 | ns |
| | | | 5.0 ± 0.5 | 1.5 | ns |

### 12.5. Timing Requirements (Unless otherwise specified, $T_a$ = -40 to 85°C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Limit | Unit |
|---|---|---|---|---|---|
| Minimum pulse width (LE) | $t_{w(H)}$ | — | 3.3 ± 0.3 | 5.0 | ns |
| | | | 5.0 ± 0.5 | 5.0 | |
| Minimum setup time | $t_S$ | — | 3.3 ± 0.3 | 3.5 | ns |
| | | | 5.0 ± 0.5 | 3.5 | |
| Minimum hold time | $t_h$ | — | 3.3 ± 0.3 | 1.5 | ns |
| | | | 5.0 ± 0.5 | 1.5 | |

### 12.6. Timing Requirements (Unless otherwise specified, $T_a$ = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Limit | Unit |
|---|---|---|---|---|---|
| Minimum pulse width (LE) | $t_{w(H)}$ | — | 3.3 ± 0.3 | 5.0 | ns |
| | | | 5.0 ± 0.5 | 5.0 | |
| Minimum setup time | $t_S$ | — | 3.3 ± 0.3 | 4.5 | ns |
| | | | 5.0 ± 0.5 | 4.0 | |
| Minimum hold time | $t_h$ | — | 3.3 ± 0.3 | 1.5 | ns |
| | | | 5.0 ± 0.5 | 1.5 | |

## 12.7. AC Characteristics (Unless otherwise specified, $T_a$ = 25 °C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | $C_L$ (pF) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time (LE-Q) | $t_{PLH}$,$t_{PHL}$ | | — | 3.3 ± 0.3 | 15 | — | 7.6 | 11.9 | ns |
| | | | | | 50 | — | 10.1 | 15.4 | |
| | | | | 5.0 ± 0.5 | 15 | — | 5.0 | 7.7 | |
| | | | | | 50 | — | 6.5 | 9.7 | |
| Propagation delay time (D-Q) | $t_{PLH}$,$t_{PHL}$ | | — | 3.3 ± 0.3 | 15 | — | 7.0 | 11.0 | ns |
| | | | | | 50 | — | 9.5 | 14.5 | |
| | | | | 5.0 ± 0.5 | 15 | — | 4.5 | 6.8 | |
| | | | | | 50 | — | 6.0 | 8.8 | |
| 3-state output enable time | $t_{PZL}$,$t_{PZH}$ | | $R_L$ = 1 kΩ | 3.3 ± 0.3 | 15 | — | 7.3 | 11.5 | ns |
| | | | | | 50 | — | 9.8 | 15.0 | |
| | | | | 5.0 ± 0.5 | 15 | — | 5.2 | 7.7 | |
| | | | | | 50 | — | 6.7 | 9.7 | |
| 3-state output disable time | $t_{PLZ}$,$t_{PHZ}$ | | $R_L$ = 1 kΩ | 3.3 ± 0.3 | 50 | — | 10.7 | 14.5 | ns |
| | | | | 5.0 ± 0.5 | 50 | — | 6.7 | 9.7 | |
| Output skew | $t_{osLH}$,$t_{osHL}$ | (Note 1) | — | 3.3 ± 0.3 | 50 | — | — | 1.5 | ns |
| | | | | 5.0 ± 0.5 | 50 | — | — | 1.0 | |
| Input capacitance | $C_{IN}$ | | — | | | — | 4 | 10 | pF |
| Output capacitance | $C_{OUT}$ | | — | | | — | 6 | — | pF |
| Power dissipation capacitance | $C_{PD}$ | (Note 2) | — | | | — | 29 | — | pF |

Note 1: Parameter guaranteed by design. ($t_{osLH}$ = $|t_{PLH}m - t_{PLH}n|$, $t_{osHL}$ = $|t_{PHL}m - t_{PHL}n|$)

Note 2: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per latch)

And the total $C_{PD}$ when n pcs. of latch operate can be gained by the following equation.

$C_{PD}$ (total) = 21 + 8 × n

## 12.8. AC Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | $C_L$ (pF) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time (LE-Q) | $t_{PLH}$,$t_{PHL}$ | | — | 3.3 ± 0.3 | 15 | 1.0 | 14.0 | ns |
| | | | | | 50 | 1.0 | 17.5 | |
| | | | | 5.0 ± 0.5 | 15 | 1.0 | 9.0 | |
| | | | | | 50 | 1.0 | 11.0 | |
| Propagation delay time (D-Q) | $t_{PLH}$,$t_{PHL}$ | | — | 3.3 ± 0.3 | 15 | 1.0 | 13.0 | ns |
| | | | | | 50 | 1.0 | 16.5 | |
| | | | | 5.0 ± 0.5 | 15 | 1.0 | 8.0 | |
| | | | | | 50 | 1.0 | 10.0 | |
| 3-state output enable time | $t_{PZL}$,$t_{PZH}$ | | $R_L$ = 1 kΩ | 3.3 ± 0.3 | 15 | 1.0 | 13.5 | ns |
| | | | | | 50 | 1.0 | 17.0 | |
| | | | | 5.0 ± 0.5 | 15 | 1.0 | 9.0 | |
| | | | | | 50 | 1.0 | 11.0 | |
| 3-state output disable time | $t_{PLZ}$,$t_{PHZ}$ | | $R_L$ = 1 kΩ | 3.3 ± 0.3 | 50 | 1.0 | 16.5 | ns |
| | | | | 5.0 ± 0.5 | 50 | 1.0 | 11.0 | |
| Output skew | $t_{osLH}$,$t_{osHL}$ | (Note 1) | — | 3.3 ± 0.3 | 50 | — | 1.5 | ns |
| | | | | 5.0 ± 0.5 | 50 | — | 1.0 | ns |
| Input capacitance | $C_{IN}$ | | — | | | — | 10 | pF |

Note 1: Parameter guaranteed by design. ($t_{osLH}$ = $|t_{PLH}m - t_{PLH}n|$, $t_{osHL}$ = $|t_{PHL}m - t_{PHL}n|$)

### 12.9. AC Characteristics (Unless otherwise specified, $T_a$ = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

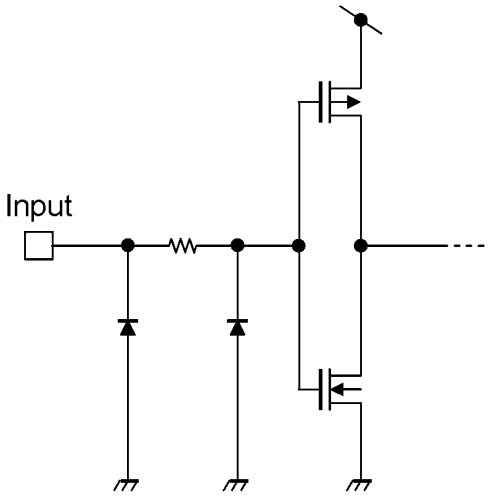
| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | $C_L$ (pF) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time (LE-Q) | $t_{PLH}$,$t_{PHL}$ | | — | 3.3 ± 0.3 | 15 | 1.0 | 16.0 | ns |
| | | | | | 50 | 1.0 | 19.5 | |
| | | | | 5.0 ± 0.5 | 15 | 1.0 | 10.5 | |
| | | | | | 50 | 1.0 | 12.5 | |
| Propagation delay time (D-Q) | $t_{PLH}$,$t_{PHL}$ | | — | 3.3 ± 0.3 | 15 | 1.0 | 15.0 | ns |
| | | | | | 50 | 1.0 | 18.5 | |
| | | | | 5.0 ± 0.5 | 15 | 1.0 | 9.0 | |
| | | | | | 50 | 1.0 | 11.0 | |
| 3-state output enable time | $t_{PZL}$,$t_{PZH}$ | | $R_L$ = 1 kΩ | 3.3 ± 0.3 | 15 | 1.0 | 15.5 | ns |
| | | | | | 50 | 1.0 | 19.0 | |
| | | | | 5.0 ± 0.5 | 15 | 1.0 | 10.5 | |
| | | | | | 50 | 1.0 | 12.5 | |
| 3-state output disable time | $t_{PLZ}$,$t_{PHZ}$ | | $R_L$ = 1 kΩ | 3.3 ± 0.3 | 50 | 1.0 | 18.5 | ns |
| | | | | 5.0 ± 0.5 | 50 | 1.0 | 12.5 | |
| Output skew | $t_{osLH}$,$t_{osHL}$ | (Note 1) | — | 3.3 ± 0.3 | 50 | — | 1.5 | ns |
| | | | | 5.0 ± 0.5 | 50 | — | 1.0 | |
| Input capacitance | $C_{IN}$ | | — | | | — | 10 | pF |

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLH}m - t_{PLH}n|$, $t_{osHL} = |t_{PHL}m - t_{PHL}n|$)

### 12.10. Noise Characteristics (Unless otherwise specified, $T_a$ = 25°C, Input: $t_r = t_f$ = 3 ns)

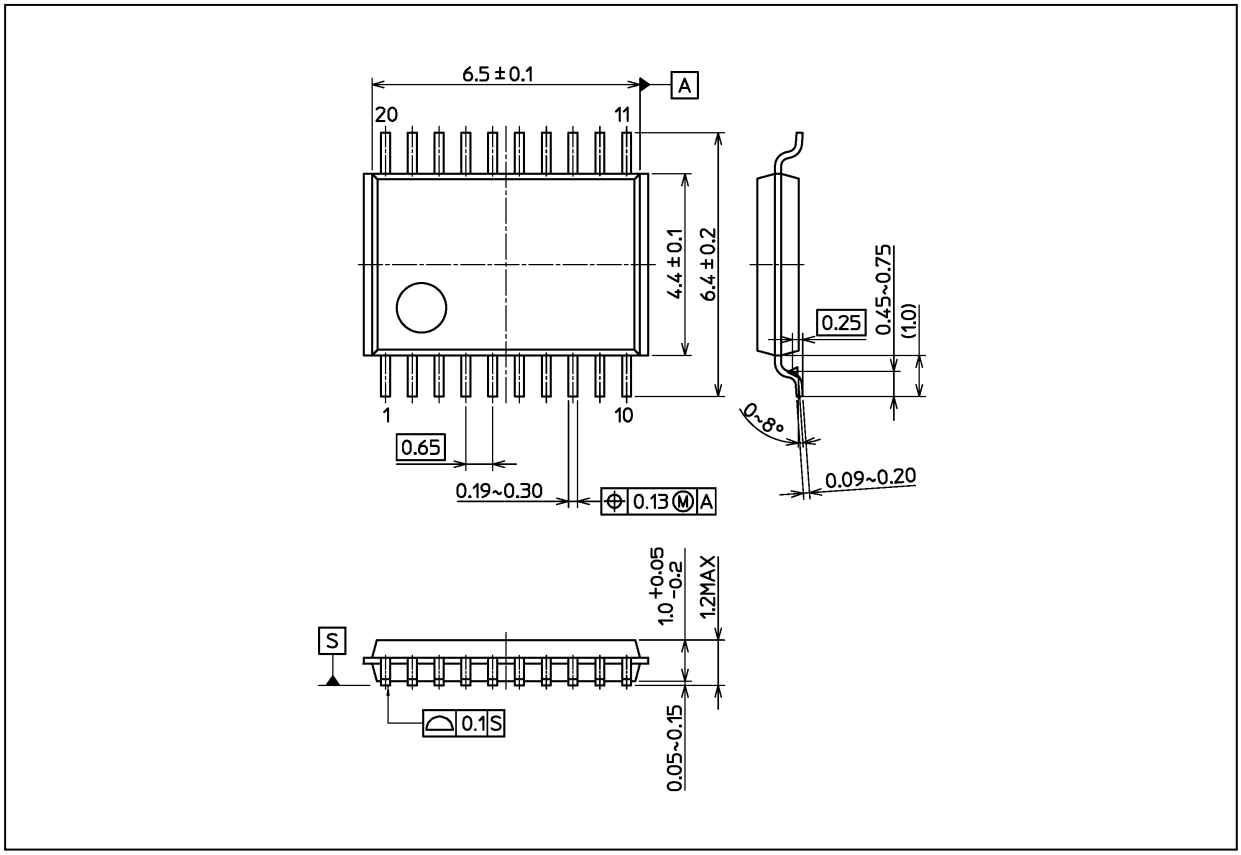
| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Typ. | Limit | Unit |
|---|---|---|---|---|---|---|
| Quiet output maximum dynamic $V_{OL}$ | $V_{OLP}$ | $C_L$ = 50 pF | 5.0 | 0.8 | 1.0 | V |
| Quiet output minimum dynamic $V_{OL}$ | $V_{OLV}$ | $C_L$ = 50 pF | 5.0 | -0.8 | -1.0 | |
| Minimum high-level dynamic input voltage | $V_{IHD}$ | $C_L$ = 50 pF | 5.0 | — | 3.5 | |
| Maximum low-level dynamic input voltage | $V_{ILD}$ | $C_L$ = 50 pF | 5.0 | — | 1.5 | |

## 13. Input Equivalent Circuit



## Package Dimensions

Unit: mm




Weight: 0.071 g (typ.)

| Package Name(s) |
| --- |
| Nickname: TSSOP20B |

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