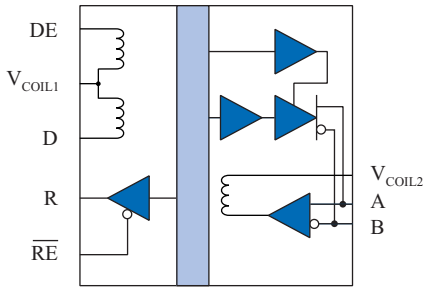
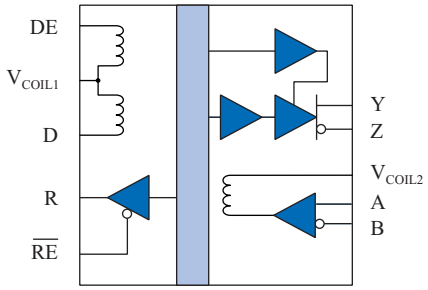
Fractional Load Passive Input RS-485 and RS-422 Isolated Transceivers

Functional Diagrams



IL3285



IL3222

IL3285 Truth Table

$V_{(A-B)}$	DE	D	R	$\overline{RE}$	Mode
≥ 200 mV	H	H	H	L	Drive
≤−200 mV	H	L	L	L	Drive
≥ 200 mV	L	X	H	L	Receive
≤−200 mV	L	X	L	L	Receive
X	X	X	Z	H	X
Open	L	X	H	L	Receive

Z = High Impedance X = Irrelevant

IL 3222 Receiver

$\overline{RE}$	R	$V_{(A-B)}$
H	Z	X
L	H	≥ 200 mV
L	L	≤−200 mV
L	H	Open

IL3222 Driver

DE	D	$V_{(Y-Z)}$
L	X	Z
H	H	≥ 200 mV
H	L	≤−200 mV

Selection Table

Model	Full/Half Duplex	No. of Devices Allowed on Bus	Data Rate Mbps	Fail-Safe
IL3285	half	256	5	yes
IL3222	full	256	5	yes

Features

- 3 V to 5 V power supplies
- 5 Mbps data rate
- ⅛ unit load
- 15 kV bus ESD protection
- 2,500 V_{RMS} isolation (1 minute)
- 20 kV/µs typical common mode rejection
- No carrier or clock for low EMI emissions and susceptibility
- −40°C to +85°C temperature range
- Thermal shutdown protection
- UL 1577 recognized; IEC 60747-5-5 (VDE 0884) certified
- 0.15", 0.3", or True 8™ mm 16-pin SOIC packages

Applications

- High node-count networks
- Security networks
- Building environmental controls
- Industrial control networks
- Gaming systems

Description

The IL3285 and IL3222 are galvanically isolated, differential bus transceivers designed for bidirectional data communication over balanced transmission lines. The devices use NVE's patented* IsoLoop spintronic Giant Magnetoresistance (GMR) technology. The IL3285 delivers at least 1.5 V into a 54 Ω load, and the IL3222 at least 2 V into a 100 Ω load for excellent data integrity over long cables. These devices are also compatible with 3.3 V input supplies, allowing interface to standard microcontrollers without additional level shifting.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

Both the IL3285 and IL3222 have current limiting and thermal shutdown features to protect against output short circuits and bus contentions that may cause excessive power dissipation. The receivers also incorporate a "fail-safe if open" design, ensuring a logic high on R if the bus lines are disconnected or "floating."

Receiver input resistance of 96 kΩ is eight times the RS-485 "Unit Load" (UL) minimum of 12 kΩ. Thus these products are known as "one-eighth UL" transceivers. There can be up to 256 on a network while still complying with the RS-485 loading specification.

REV. Q

Absolute Maximum Ratings

Operating at absolute maximum ratings will not damage the device. However, extended periods of operation at the absolute maximum ratings may affect performance and reliability.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	−55		150	°C	
Ambient Operating Temperature	T_A	−40		85	°C	
Voltage Range at A or B Bus Pins		−7		12	V	
Supply Voltage[1]	V_{DD1}, V_{DD2}	−0.5		7	V	
Digital Input Voltage		−0.5		V_{DD}+0.5	V	
Digital Output Voltage		−0.5		V_{DD}+1	V	
ESD Protection		±15			kV	
Input Current	I_{IN}	−25		+25	mA	
ESD (all bus nodes)		15			kV	HBM

Note 1. All voltage values are with respect to network ground except differential I/O bus voltages.

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	V_{DD1} V_{DD2}	3.0 4.5		5.5 5.5	V	
Ambient Operating Temperature	T_A	−40		85	°C	
Input Voltage at any Bus Terminal (separately or common mode)	V_I V_{IC}			12 −7	V	
Input Threshold for Output Logic High	I_{INH}		1.5	0.8	mA	
Input Threshold for Output Logic Low	I_{INL}	5	3.5		mA	
Differential Input Voltage	V_{ID}			+12/−7	V	
High-Level Output Current (Driver)	I_{OH}	−60		60	mA	
High-Level Digital Output Current (Receiver)	I_{OH}	−8		8	mA	
Low-Level Output Current (Driver)	I_{OL}	−60		60	mA	
Low-Level Digital Output Current (Receiver)	I_{OL}	−8		8	mA	
Ambient Operating Temperature	T_A	−40		85	°C	
Digital Input Signal Rise, Fall Times	t_{IR},t_{IF}			1	µs	

Insulation Specifications

Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Comparative Tracking Index		CTI	≥175			V	Per IEC 60112
Endurance Voltage (Maximum Working Voltage for Indefinite Life)	AC DC	V_{IO}	1000 1500			V_{RMS} V_{DC}	At maximum operating temperature
Creepage Distance (external)	0.15" SOIC 0.3" SOIC		4.03 8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)			0.012	0.013		mm	
Barrier Resistance		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance		C_{IO}		7		pF	f = 1 MHz
Leakage Current				0.2		µA	240 V_{RMS}, 60 Hz

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Safety Approvals

IEC 60747-5-5 (VDE 0884) (File Number 5016933-4880-0001)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Transient overvoltage (V_{IOTM}) and surge voltage (V_{IOSM}) 4000 V_{PK}
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)
Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-3	SOIC	150 V_{RMS}
None	Wide-body SOIC/True 8™	300 V_{RMS}

UL 1577 (Component Recognition Program File Number E207481)
Each part tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

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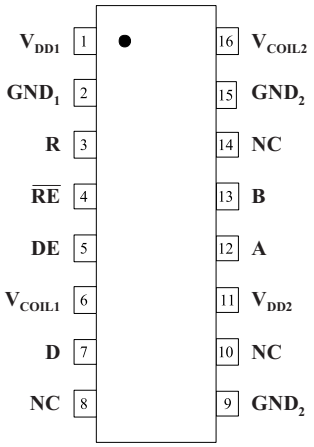
IL3285-3 Pin Connections (0.15" SOIC Package)

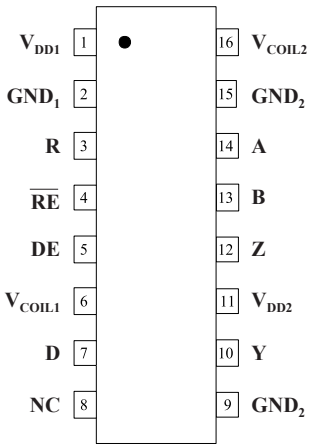
1	V_{DD1}	Input power supply
2	GND_1	Ground return for V_{DD1}
3	R	Output data from bus
4	$\overline{RE}$	Read enable (if RE is high, R is high impedance)
5	DE	Drive enable
6	V_{COIL1}	Coils for DE and D (connect to V_{DD1})
7	D	Data input to bus
8	NC	No internal connection
9	GND_2	Ground return for V_{DD2} (internally connected to pin 15)
10	NC	No internal connection
11	V_{DD2}	Output power supply
12	A	Non-inverting bus line
13	B	Inverting bus line
14	NC	No internal connection
15	GND_2	Ground return for V_{DD2} (internally connected to pin 9)
16	V_{COIL2}	Coil for R



IL3285-3

IL3222-3 Pin Connections (0.15" SOIC Package)

1	V_{DD1}	Input power supply
2	GND_1	Ground return for V_{DD1}
3	R	Output data from bus
4	$\overline{RE}$	Read enable (if RE is high, R is high impedance)
5	DE	Drive enable
6	V_{COIL1}	Coils for DE and D (connect to V_{DD1})
7	D	Data input to bus
8	NC	No internal connection
9	GND_2	Ground return for V_{DD2} (internally connected to pin 15)
10	Y	Non-inverting driver bus line
11	V_{DD2}	Output power supply
12	Z	Inverting driver bus line
13	B	Inverting receiver bus line
14	A	Non-inverting receiver bus line
15	GND_2	Ground return for V_{DD2} (internally connected to pin 9)
16	V_{COIL2}	Coil for R



IL3222-3

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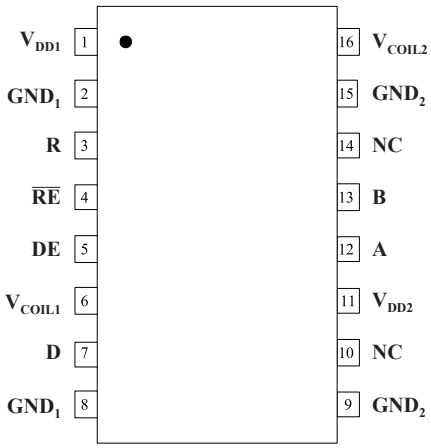
IL3285 Pin Connections (0.3" SOIC Package)

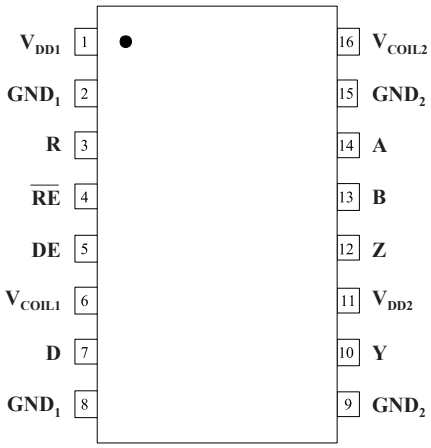
1	V_{DD1}	Input power supply
2	GND_1	Ground return for V_{DD1}
3	R	Output data from bus
4	$\overline{RE}$	Read enable (if RE is high, R is high impedance)
5	DE	Drive enable
6	V_{COIL1}	Coils for DE and D (connect to V_{DD1})
7	D	Data input to bus
8	GND_1	Internally connected to pin 2 for 0.3" package; no internal connection on 0.15" IL3285-3
9	GND_2	Ground return for V_{DD2} (internally connected to pin 15)
10	NC	No internal connection
11	V_{DD2}	Output power supply
12	A	Non-inverting bus line
13	B	Inverting bus line
14	NC	No internal connection
15	GND_2	Ground return for V_{DD2} (internally connected to pin 9)
16	V_{COIL2}	Coil for R



IL3285

IL3222 Pin Connections (0.3" SOIC Package)

1	V_{DD1}	Input power supply
2	GND_1	Ground return for V_{DD1}
3	R	Output data from bus
4	$\overline{RE}$	Read enable (if RE is high, R is high impedance)
5	DE	Drive enable
6	V_{COIL1}	Coils for DE and D (connect to V_{DD1})
7	D	Data input to bus
8	GND_1	Internally connected to pin 2 for 0.3" package; no internal connection on 0.15" IL3222-3
9	GND_2	Ground return for V_{DD2} (internally connected to pin 15)
10	Y	Non-inverting driver bus line
11	V_{DD2}	Output power supply
12	Z	Inverting driver bus line
13	B	Inverting receiver bus line
14	A	Non-inverting receiver bus line
15	GND_2	Ground return for V_{DD2} (internally connected to pin 9)
16	V_{COIL2}	Coil for R



IL3222

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Driver Section

Electrical Specifications (V_{DD1} = 3 V – 5.5 V; V_{DD2} = 4.5 V – 5.5 V; T = –40°C – 85°C unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Coil Input Resistance	R_{COIL}	47	85	112	Ω	T = 25°C
Coil Input Resistance	R_{COIL}	31	85	128	Ω	T = –40°C – 85°C
Coil Resistance Temperature Coefficient	TC R_{COIL}		0.2	0.25	Ω/°C	
Coil Inductance	L_{COIL}		9		nH	
High Level Input Current	I_{INH}	0.5	1		mA	t_{IR} = t_{IF} = 3 ns;
Low Level Input Current	I_{INL}		3.5	5	mA	C_{BOOST} = 16 pF
Output voltage				V_{DD}	V	I_O = 0
Differential Output Voltage	$\|V_{OD1}\|$			V_{DD}	V	I_O = 0
Differential Output Voltage	$\|V_{OD2}\|$	2	3		V	R_L = 100 Ω, V_{DD} = 5 V
Differential Output Voltage[6]	V_{OD3}	1.5	2.3		V	R_L = 54 Ω, V_{DD} = 5 V
Change in Magnitude[7] of Differential Output Voltage	$\Delta\|V_{OD}\|$			±0.2	V	R_L = 54 Ω or 100 Ω
Common Mode Output Voltage	V_{OC}			3	V	R_L = 54 Ω or 100 Ω
Change in Magnitude[7] of Common Mode Output Voltage	$\Delta\|V_{OC}\|$			0.2	V	R_L = 54 Ω or 100 Ω
Output Current[4]				1 –0.8	mA mA	Output disabled, V_O = 12 V V_O = –7 V
|Short-circuit Output Current|	I_{OS}	60		250	mA	–7 V < V_O < 12 V
Supply Current (V_{DD2} = +5 V) (V_{DD1} = +5 V)	I_{DD2} I_{DD1}		6 2.5	7 3	mA	No Load (Outputs Enabled)
Supply Current (V_{DD1} = +3.3 V)	I_{DD2}		1.3	2	mA	No Load (Outputs Enabled)
Common Mode Rejection	$\|CM_H\|$,$\|CM_L\|$	15	20		kV/µs	V_T = 300 V_{peak}

Switching Specifications (V_{DD1} = 5 V; V_{DD2} = 5 V; T = –40°C – 85°C)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		5			Mbps	R_L = 54 Ω; C_L = 50 pF; C_{boost} = 16pF
Differential Output Prop Delay	t_D(OD)		40	65	ns	
Pulse Skew[10]	t_{SK}(P)		6	20	ns	
Differential Output Rise and Fall Time	t_T(OD)	3	12	25	ns	
Drive Enable Time to High Level	t_{PZH}		25	80	ns	
Drive Enable Time to Low Level	t_{PZL}		25	80	ns	
Drive Disable Time from High Level	t_{PHZ}		25	80	ns	
Drive Disable Time from Low Level	t_{PLZ}		25	80	ns	
Skew Limit[3]	t_{SK}(LIM)			8	ns	

Switching Specifications (V_{DD1} = 3.3 V; V_{DD2} = 5 V; T = –40°C – 85°C)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		5			Mbps	R_L = 54 Ω; C_L = 50 pF; C_{boost} = 16pF
Differential Output Prop Delay	t_D(OD)		40	65	ns	
Pulse Skew[10]	t_{SK}(P)		6	20	ns	
Differential Output Rise and Fall Time	t_T(OD)	3	12	25	ns	
Drive Enable Time to High Level	t_{PZH}		25	80	ns	
Drive Enable Time to Low Level	t_{PZL}		25	80	ns	
Drive Disable Time from High Level	t_{PHZ}		25	80	ns	
Drive Disable Time from Low Level	t_{PLZ}		25	80	ns	
Skew Limit[3]	t_{SK}(LIM)			8	ns	

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Receiver Section

Electrical Specifications (V_{DD1} = 3 V – 5.5 V; V_{DD2} = 4.5 V – 5.5 V; T = –40°C – 85°C unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Coil Resistance	R_{COIL}	47	85	112	Ω	T = 25°C
		31	85	128	Ω	T = –40°C – 85°C
Coil Resistance Temperature Coefficient	TC R_{COIL}		0.2	0.25	Ω/°C	
Positive-going Input Threshold	V_{IT+}			0.2	V	–7 V < V_{CM} < 12 V
Negative-going Input Threshold	$V_{IT–}$	–0.2			V	–7 V < V_{CM} < 12 V
Hysteresis Voltage ($V_{it+} – V_{it–}$)	V_{HYS}		70		mV	V_{CM} = 0V, T = 25°C
High Level Digital Output Voltage	V_{OH}	V_{DD} – 0.2	V_{DD} – 0.2		V	V_{ID} = 200 mV
						I_{OH} = 4 mA
Low Level Digital Output Voltage	V_{OL}			0.8	V	V_{ID} = –200 mV
						I_{OL} = 4 mA
High impedance state output current	I_{OZ}			10	µA	0.4≤V_O≤(V_{DD2} – 0.5) V
Line Input Current[8]	I_I			1	mA	V_I = 12 V
				–0.8		V_I = –7 V
Input Resistance	r_I	96			kΩ	

Switching Characteristics (V_{DD1} = 5 V; V_{DD2} = 5 V; C_{boost} = 16pF; T = –40°C – 85°C)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		5			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay[9]	t_{PD}		90	150	ns	–1.5 ≤ V_O ≤ 1.5 V, C_L = 15 pF
Pulse Skew[10]	t_{SK}(P)		6	20	ns	–1.5 ≤ V_O ≤ 1.5 V, C_L = 15 pF
Skew Limit[3]	t_{SK}(LIM)		2	8	ns	R_L = 54 Ω, C_L = 50 pF
Read Enable Time to High Level	t_{PZH}		4	10	ns	C_L = 15 pF
Read Enable Time to Low Level	t_{PZL}		4	10	ns	
Read Disable Time from High Level	t_{PHZ}		4	10	ns	
Read Disable Time from Low Level	t_{PLZ}		4	10	ns	

Switching Characteristics (V_{DD1} = 3.3 V; V_{DD2} = 5 V; C_{boost} = 16pF; T = –40°C – 85°C)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		5			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay[9]	t_{PD}		100	150	ns	–1.5 ≤ V_O ≤ 1.5 V, C_L = 15 pF
Pulse Skew[10]	t_{SK}(P)		10	20	ns	–1.5 ≤ V_O ≤ 1.5 V, C_L = 15 pF
Skew Limit[3]	t_{SK}(LIM)		4	10	ns	R_L = 54 Ω, C_L = 50 pF
Read Enable Time to High Level	t_{PZH}		5	10	ns	C_L = 15 pF
Read Enable Time to Low Level	t_{PZL}		5	10	ns	
Read Disable Time from High Level	t_{PHZ}		5	10	ns	
Read Disable Time from Low Level	t_{PLZ}		17	10	ns	

Notes (apply to both driver and receiver sections):

1. All voltages are with respect to network ground except differential I/O bus voltages.
2. Differential input/output voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.
3. Skew limit is the maximum difference in any two channels in one device.
4. The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
5. All typical values are at V_{DD1}, V_{DD2} = 5 V or V_{DD1}= 3.3 V and T_A = 25°C.
6. While –7 V < V_{CM} < 12 V, the minimum V_{OD2} with a 54 Ω load is either ½ V_{OD1} or 1.5 V, whichever is greater.
7. Δ|VOD| and Δ|VOC| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
8. This applies for both power on and power off; refer to ANSI standard RS-485 for exact condition. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.
9. Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
10. Pulse skew is defined as the $|t_{PLH} – t_{PHL}|$ of each channel.

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Applications Information

Input Resistor Values

The IL3222 and IL3285 are current-mode devices. Changes in input coil current switch internal spintronic GMR sensors. Inputs are logically high when the coil voltage is high, that is when there is no coil current.

A single resistor is required to limit the input coil current to the 5 mA threshold current. The absolute maximum current through any coil is 25 mA.

Typical Input Resistor Values

V_{COIL}	0.125W, 5% Resistor
3.3 V	510 Ω
5 V	820 Ω

The table shows typical values for the external resistor in 5 V and 3 V logic systems. As always, these values as approximate and should be adjusted for temperature or other application specifics. If the expected temperature range is large, 1% tolerance resistors may provide additional design margin.

Boost Capacitor

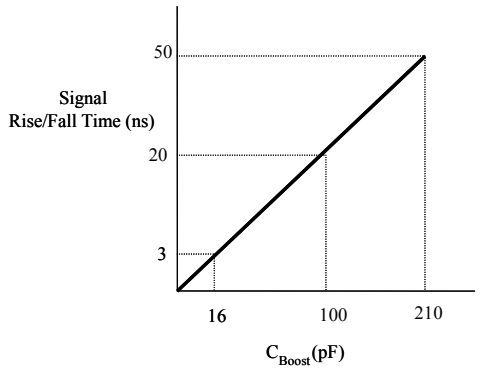

Figure 2. C_{boost} Selector

The boost capacitor in parallel with the current-limiting resistor boosts the instantaneous coil current at the signal transition. This ensures switching and reduces propagation delay and reduces pulse-width distortion.

Select the value of the boost capacitor based on the rise and fall times of the signal driving the inputs. The instantaneous boost capacitor current is proportional to input edge speeds ($C\frac{dV}{dt}$). Select a capacitor value based on the rise and fall times of the input signal to be isolated that provides approximately 20 mA of additional "boost" current. Figure 2 is a guide to boost capacitor selection. For high-speed logic signals (t_r,t_f < 10 ns), a 16 pF capacitor is recommended. The capacitor value is generally not critical; if in doubt, choose a higher value up to a maximum of 470 pF.

RS-485 and RS-422 Busses

RS-485 and RS-422 are differential (balanced) data transmission standards for use over long distances or in noisy environments. RS-422 is an RS-485 subset, so RS-485 transceivers are also RS-422-compliant. RS-422 is a multi-drop standard allowing only one driver and up to 10 receivers on each bus (assuming unit load receivers). RS-485 is a true multipoint standard which allows up to 32 unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, RS-485 requires drivers to handle bus contention without damage. Another important advantage of RS-485 is the extended common-mode range (CMR), which requires driver outputs and receiver inputs withstand +12 V to −7 V. RS-422 and RS-485 are intended for runs as long as 4,000 feet (1,200 m), so the wide CMR is necessary for ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

IL3000 transceivers have differential input receivers for maximum noise immunity and common-mode rejection. Input sensitivity is ±200 mV as required by the RS-422 and RS-485 specifications. The receivers include a "fail-safe if open" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating). Receivers easily meet the data rates supported by the corresponding driver. IL3000-Series receiver outputs have tri-state capabilities with active low RE inputs.

Driver Features

The RS485/422 driver is a differential output device that delivers at least 1.5 V across a 54 Ω load (RS-485), and at least 2 V across a 100 Ω load (RS-422). The driver features low propagation delay skew to maximize bit width and minimize EMI. IL3222 and IL3285 drivers have tri-state capability with an active high DE input.

Cabling, Data Rate and Terminations

Cabling

Use twisted-pair cable. The cable can be unshielded if it is short (less than 10 meters) and the data rate is slow (less than 100 Kbps). Otherwise, use screened cable with the shield tied to earth ground at one end only. Do not tie the shield to digital ground. The other end of the shield may be tied to earth ground through an RC network. This prevents a DC ground loop in the shield. Shielded cable minimizes EMI emissions and external noise coupling to the bus.

Data Rate

The longer the cable, the slower the data rate. The RS-485 bus can transmit ground over 4,000 feet (1,200 meters) or at 10 Mbps, but not both at the same time. Transducer and cable characteristics combine to act as a filter with the general response shown in Figure 3. Other parameters such as acceptable jitter affect the final cable length versus data rate tradeoff. Less jitter means better signal quality but shorter cable lengths or slower data rates. Figure 4 shows a generally accepted 30% jitter and a corresponding data rate versus cable length.

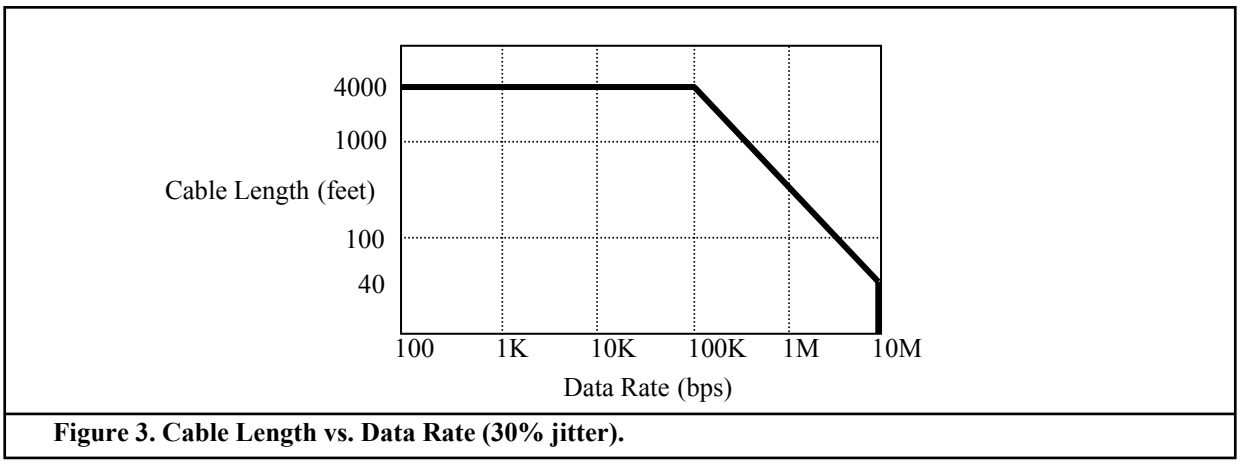

Figure 3. Cable Length vs. Data Rate (30% jitter).

Terminations

Transmission lines should be terminated to avoid reflections that cause data errors. In RS-485 systems both ends of the bus, not every node, should be terminated. In RS-422 systems only the receiver end should be terminated.

Unterminated Parallel

Proper termination is imperative when using IL3285 and IL3222 to minimize reflections. Unterminated lines are only suitable for very low data rates and very short cable runs, otherwise line reflections cause problems. Parallel terminations are the most popular. They allow high data rates and excellent signal quality.

Occasionally in noisy environments, fast pulses or noise appearing on the bus lines cause errors. One way of alleviating such errors without adding circuit delays is to place a series resistor in the bus line. Depending on the power supply, the resistor should be between 300 Ω (3 V supply) and 500 Ω (5 V supply).

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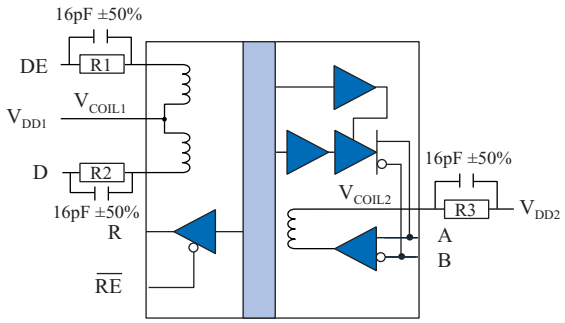
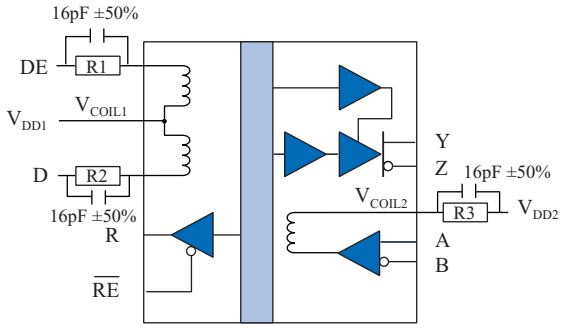
Typical Coil Connections



$V_{DD1} = V_{DD2} = 5$ V R1, R2, R3 = 820 Ω
$V_{DD1} = 3.3$ V R1, R2 = 510 Ω; R3 = 820 Ω



$V_{DD1} = V_{DD2} = 5$ V R1, R2, R3 = 820 Ω
$V_{DD1} = 3.3$ V R1, R2 = 510 Ω; R3 = 820 Ω

Fail-Safe Operation

"Fail-safe operation" is defined here as the forcing of a logic high state on the "R" output in response to an open-circuit condition between the "A" and "B" lines of the bus, or when no drivers are active on the bus.

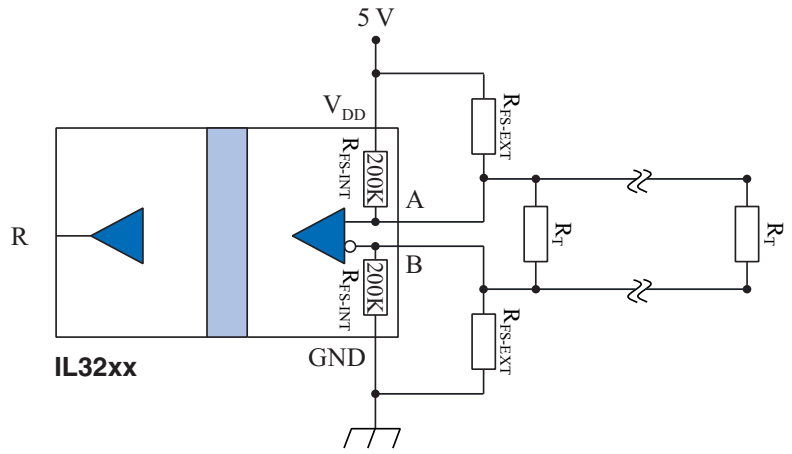
Proper biasing can ensure fail-safe operation, that is a known state when there are no active drivers on the bus. IL3285 and IL3222 Isolated Transceivers include internal pull-up and pull-down resistors of approximately 200 kΩ in the receiver section (R_{FS-INT}; see figure on following page). These internal resistors are designed to ensure failsafe operation but only if there are no termination resistors. The entire V_{DD} will appear between inputs "A" and "B" if there is no loading and no termination resistors, and there will be more than the required 200 mV with up to four RS-485/RS-422 worst-case one-eighth unit loads of 96 kΩ. Many designs operating below 1 Mbps or less than 1,000 feet are unterminated. Termination resistors may not be necessary for very low data rates and very short cable runs because reflections have time to settle before data sampling, which occurs at the middle of the bit interval.

In busses with low-impedance termination resistors, however, the differential voltage across the conductor pair will be close to zero with no active drivers. In this case the state of the bus is indeterminate, and the idle bus will be susceptible to noise. For example, with 120 Ω termination resistors (R_T) on each end of the cable, and four eighth unit loads (96 kΩ each), without external fail-safe biasing resistors the internal pull-up and pull-down resistors will produce a voltage between inputs "A" and "B" of only about one millivolt. This is not nearly enough to ensure a known state. External fail-safe biasing resistors (R_{FS-EXT}) at one end of the bus can ensure fail-safe operation with a terminated bus. Resistors should be selected so that under worst-case power supply and resistor tolerances there is at least 200 mV across the conductor pair with no active drivers to meet the input sensitivity specification of the RS-422 and RS-485 standards.

Using the same value for pull-up and pull-down biasing resistors maintains balance for positive- and negative going transitions. Lower-value resistors increase inactive noise immunity at the expense of quiescent power consumption. Note that each Unit Load on the bus adds a worst-case loading of 12 kΩ across the conductor pair, and 256 one-eighth unit loads add 375 Ω worst-case loading. The more loads on the bus, the lower the required values of the biasing resistors.

In the example with two 120 Ω termination resistors and four eighth unit loads, 560 Ω external biasing resistors provide more than 200 mV between "A" and "B" with adequate margin for power supply variations and resistor tolerances. This ensures a known state when there are no active drivers. Other illustrative examples are shown in the following table:

Fail-Safe Biasing



R_{FS-EXT}	R_T	Loading	Nominal V_{A-B} (inactive)	Fail-Safe Operation?
Internal Only	None	Four eighth-unit loads (96 kΩ ea.)	283 mV	Yes
Internal Only	120 Ω	Four eighth-unit loads (96 kΩ ea.)	1 mV	No
560 Ω	120 Ω	Four eighth-unit loads (96 kΩ ea.)	254 mV	Yes
510 Ω	120 Ω	256 eighth-unit loads (96 kΩ ea.)	243 mV	Yes

Power Supply Decoupling

Both V_{DD1} and V_{DD2} should be bypassed with 47 nF low-ESR ceramic capacitors. These should be placed as close as possible to V_{DD} pins. V_{DD2} should also be bypassed with a 10 µF tantalum capacitor.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Magnetic Field Immunity

IsoLoop Isolators operate by imposing a magnetic field on a GMR sensor, which translates the change in field into a change in logic state. A magnetic shield and a Wheatstone Bridge configuration provide good immunity to external magnetic fields. Immunity to external magnetic fields can be enhanced by proper orientation of the device with respect to the field direction and larger boost capacitors.

An applied field in the "H1" direction is the worst case for magnetic immunity. In this case the external field is in the same direction as the applied internal field. In one direction it will tend to help switching; in the other it will hinder switching. This can cause unpredictable operation.

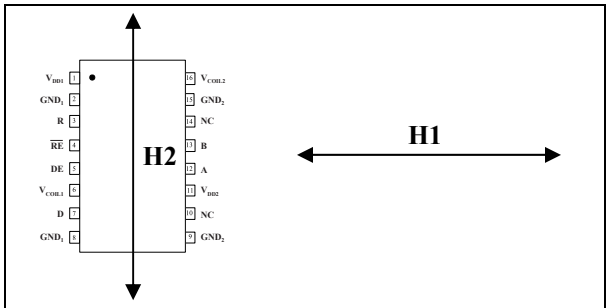


Figure 3. Orientation of External Magnetic Field

An applied field in the direction of "H2" has considerably less effect on the sensor and will result in significantly higher immunity levels as shown in Table 1.

The greatest magnetic immunity is achieved by adding a larger boost capacitor across the input resistor. Very high immunity can be achieved with this method.

Method	Approximate Immunity	Immunity Description
Field applied in direction H1	±20 Gauss	A DC current of 16 A flowing in a conductor 1 cm from the device could cause disturbance
Field applied in direction H2	±70 Gauss	A DC current of 56 A flowing in a conductor 1 cm from the device could cause disturbance
Field applied in any direction but with boost capacitor (470 pF) in circuit	±250 Gauss	A DC current of 200 A flowing in a conductor 1 cm from the device could cause disturbance

Table 1. Magnetic Immunity

Data Rate and Magnetic Field Immunity

It is easier to disrupt an isolated DC signal with an external magnetic field than it is to disrupt an isolated AC signal. Similarly, a DC magnetic field will have a greater effect on the device than an AC magnetic field of the same effective magnitude. For example, signals with pulses longer than 100 µs are more susceptible to magnetic fields than shorter pulse widths. For input signals faster than 1 MHz, rising in less than 3 ns, a 470 pF field-boost capacitor provides as much as 400 Gauss immunity, while the same input capacitor might provide just 70 Gauss immunity at 50 kHz.

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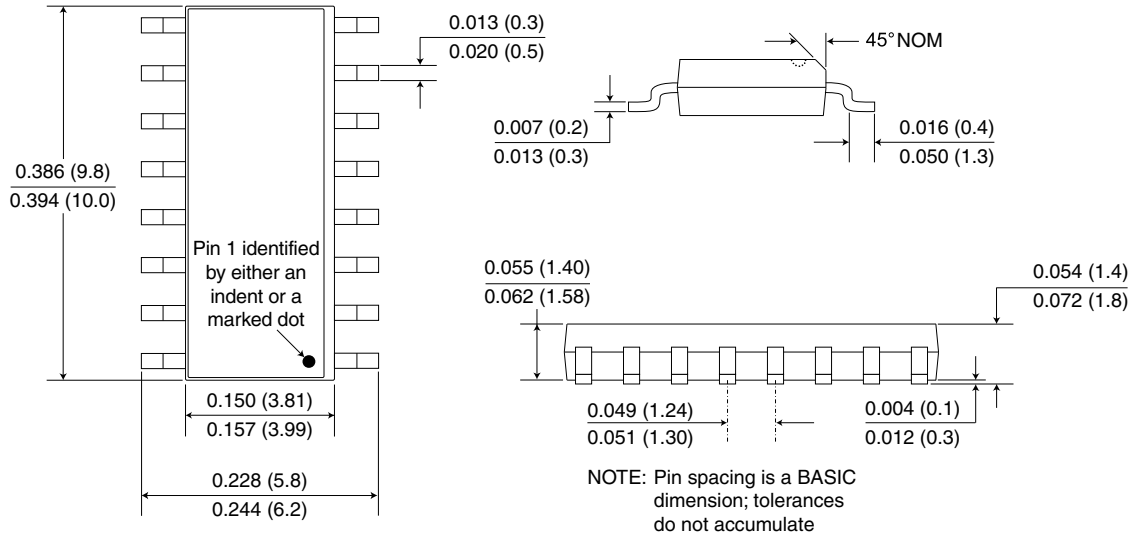
Package Drawings

0.15" 16-pin SOIC Package (-3 suffix)

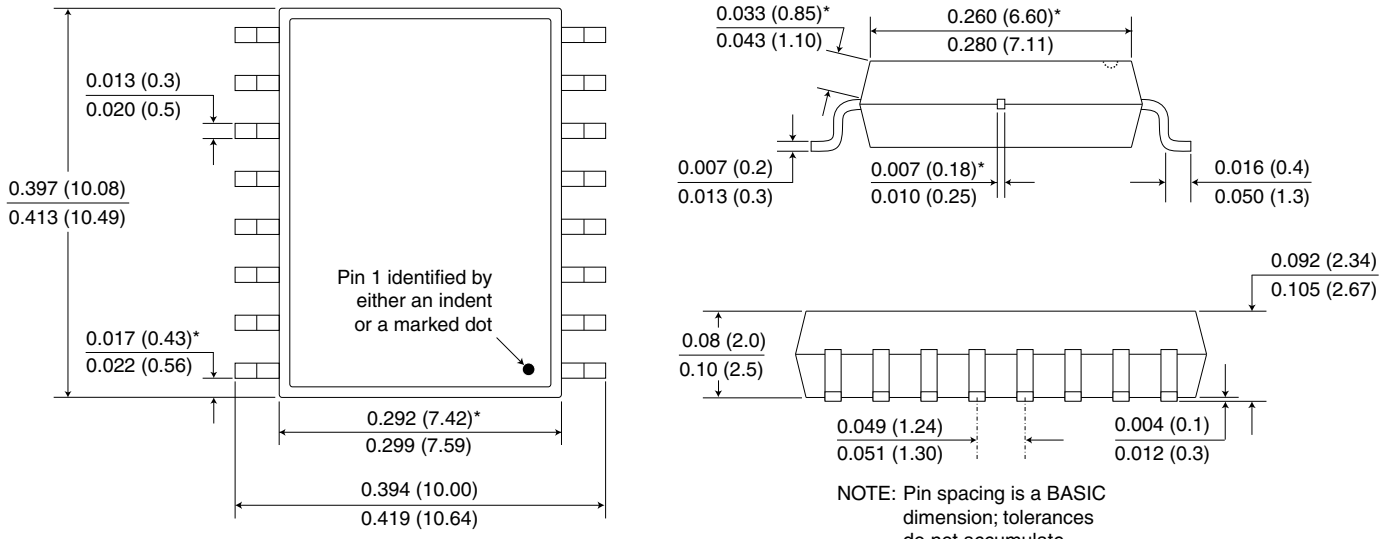
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

0.3" 16-pin SOIC Package (no suffix)

Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

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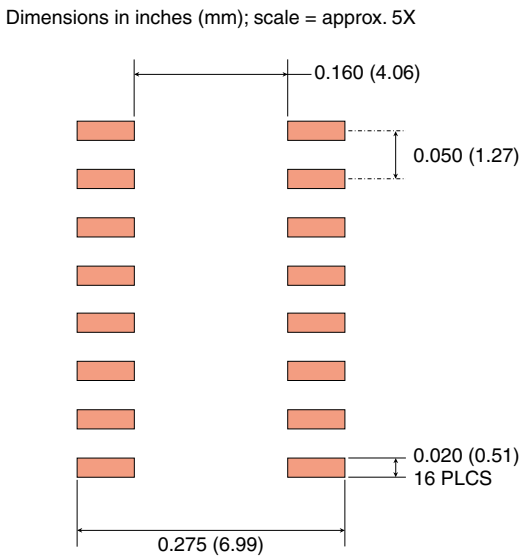
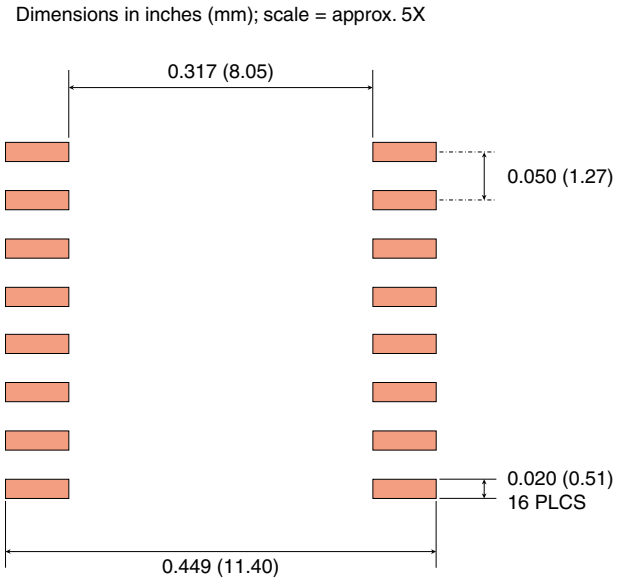
Recommended Pad Layouts

0.15" 16-pin SOIC Pad Layout



0.3" 16-pin SOIC Pad Layout



Ordering Information and Valid Part Numbers

IL 32 85 -3 E TR13

Bulk Packaging
Blank = Tube
TR13 = 13" Tape and Reel

Package
E = RoHS Compliant

Package Type
Blank = 0.3" SOIC
-3 = 0.15" SOIC

Channel Configuration
22 = RS-422
85 = RS-485

Base Part Number
32 = Passive-In, 1/8-Load Transceiver

Product Family
IL = Isolators

Valid Part Numbers

IL3285E
IL3285E TR13
IL3285-3E
IL3285-3E TR13

IL3222E
IL3222E TR13
IL3222-3E
IL3222-3E TR13

RoHS COMPLIANT

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Revision History

ISB-DS-001-IL3285/22-Q
November 2013

Changes

- IEC 60747-5-5 (VDE 0884) certification.
- Upgraded from MSL 2 to MSL 1.
- Rearranged low level input current specification so maximum is more than minimum.

ISB-DS-001-IL3285/22-P

Changes

- Added VDE 0884 pending.
- Clarified switching specifications.
- Updated package drawings.
- Added recommended solder pad layouts.

ISB-DS-001-IL3285/22-O

Changes

- Detailed isolation and barrier specifications.
- Cosmetic changes.

ISB-DC-001-IL3285/22-N

Changes

- Added minimum/maximum coil resistance specifications.
- Misc. cosmetic changes.

ISB-DS-001-IL3285/22-M

Changes

- Update terms and conditions.

ISB-DS-001-IL3285/22-L

Changes

- Clarified ground pin connections (pp. 3-4).

ISB-DS-001-IL3285/22-K

Changes

- Changes to current-limiting resistor values (pp. 7 and 10).
- Details for boost capacitor selection (p. 7).

ISB-DS-001-IL3285/22-J

Change

- Noted UL1577 Approval.

ISB-DS-001-IL3285/22-I

Change

- Added bus-protection ESD specification (15 kV).

ISB-DS-001-IL3285/22-H

Changes

- Added typical coil resistance and temperature coefficient specifications.
- Added note on package drawings that pin-spacing tolerances are non-accumulating.

ISB-DS-001-IL3285/22-G

Changes

- Changed ordering information to reflect that devices are now fully RoHS compliant with no exemptions.

ISB-DS-001-IL3285/22-F

Changes

- Eliminated soldering profile chart

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November 2013

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