

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ E6 600V

600V CoolMOS™ E6 Power Transistor
IPx60R190E6

Data Sheet

Rev. 2.3
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ E6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

Features

- Extremely low losses due to very low FOM $R_{ds(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

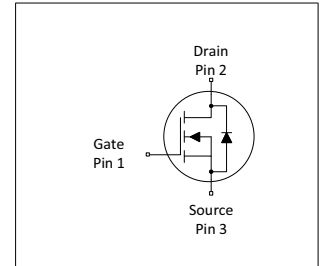
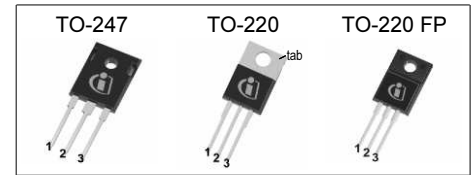


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.19	Ω
Q_g,typ	63	nC
$I_D,pulse$	59	A
$E_{oss} @ 400V$	5.2	μJ
Body diode di/dt	500	A/ μs

Type / Ordering Code	Package	Marking	Related Links
IPW60R190E6	PG-TO 247	6R190E6	see Appendix A
IPP60R190E6	PG-TO 220		
IPA60R190E6	PG-TO 220 FullPAK		



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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			20.2	A	$T_C = 25^\circ\text{C}$
				12.8		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			59	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			418	mJ	$I_D = 3.4\text{A}$, $V_{DD} = 50\text{V}$ (see table 11)
Avalanche energy, repetitive	E_{AR}			0.63	mJ	$I_D = 3.4\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			3.4	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 480\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation (non FullPAK) TO-247, TO-220	P_{tot}			151.0	W	$T_C = 25^\circ\text{C}$
Power dissipation (FullPAK) TO-220 FP	P_{tot}			34.0	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55		150	$^\circ\text{C}$	
Mounting torque (non FullPAK) TO-247, TO-220				60	Ncm	M3 and M3.5 screws
Mounting torque (FullPAK) TO-220 FP				50	Ncm	M2.5 screws
Continuous diode forward current	I_S			17.5	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			59	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$
Maximum diode commutation speed	di_f/dt			500	A/ μs	(see table 9)

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_θ

3 Thermal characteristics

Table 3 Thermal characteristics TO-247, TO-220

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			0.83	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics TO-220 FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			3.7	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600			V	$V_{GS} = 0V, I_D = 0.25\text{mA}$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	$V_{DS} = V_{GS}, I_D = 0.63\text{mA}$
Zero gate voltage drain current	I_{DSS}			1	μA	$V_{DS} = 600V, V_{GS} = 0V, T_j = 25^\circ\text{C}$
			10			$V_{DS} = 600V, V_{GS} = 0V, T_j = 150^\circ\text{C}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		0.170	0.19	Ω	$V_{GS} = 10V, I_D = 9.5A, T_j = 25^\circ\text{C}$
			0.440			$V_{GS} = 10V, I_D = 9.5A, T_j = 150^\circ\text{C}$
Gate resistance	R_G		6		Ω	$f = 1\text{MHz}$, open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		1400		pF	$V_{GS} = 0V, V_{DS} = 100V, f = 1\text{MHz}$
Output capacitance	C_{oss}		85		pF	
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$		56		pF	$V_{GS} = 0V, V_{DS} = 0 \dots 480V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$		266		pF	$I_D = \text{constant}, V_{GS} = 0V, V_{DS} = 0 \dots 480V$
Turn-on delay time	$t_{d(on)}$		12		ns	$V_{DD} = 400V, V_{GS} = 13V, I_D = 9.5A, R_G = 3.4\Omega$ (see table 10)
Rise time	t_r		10		ns	
Turn-off delay time	$t_{d(off)}$		90		ns	
Fall time	t_f		8		ns	

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		7.6		nC	$V_{DD} = 480V, I_D = 9.5A, V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	Q_{gd}		32		nC	
Gate charge total	Q_g		63		nC	
Gate plateau voltage	$V_{plateau}$		5.4		V	

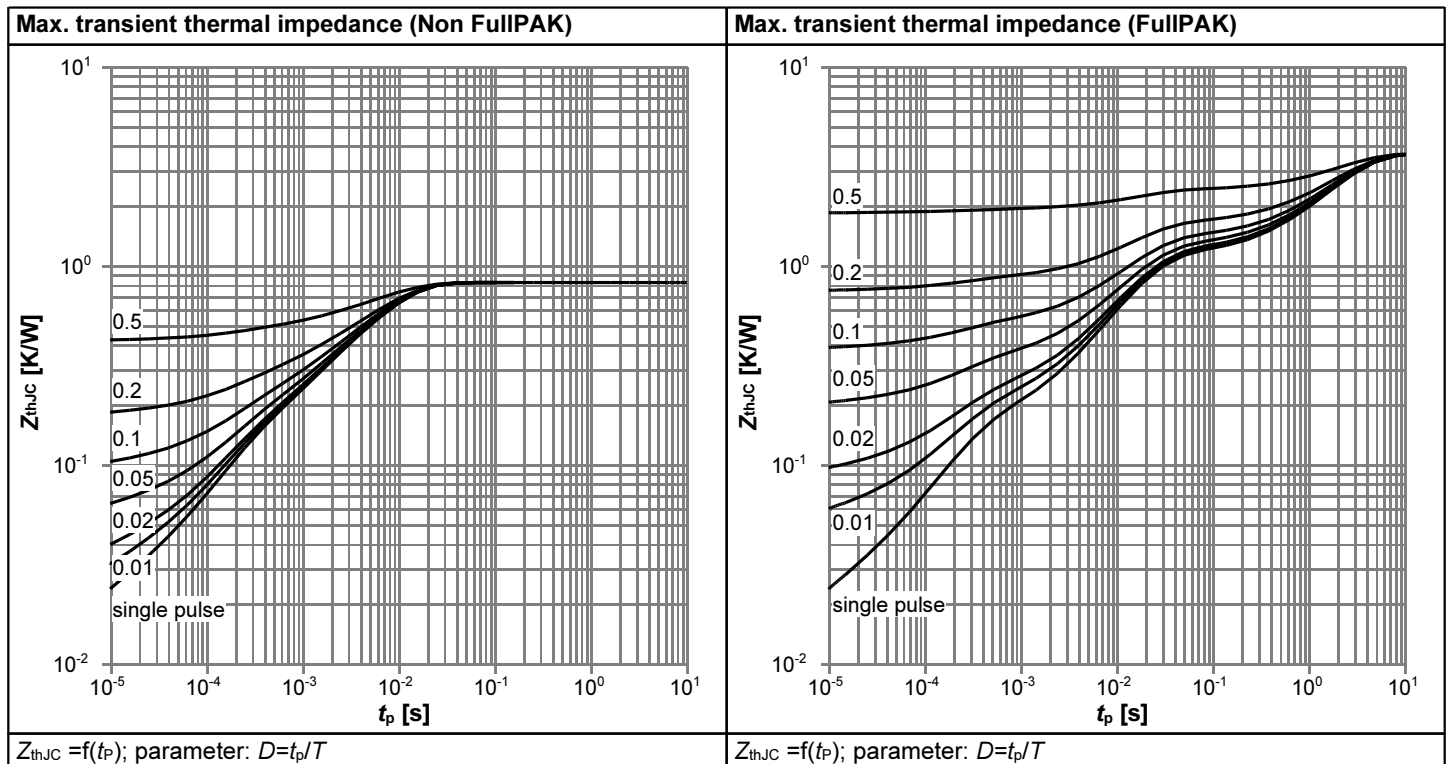
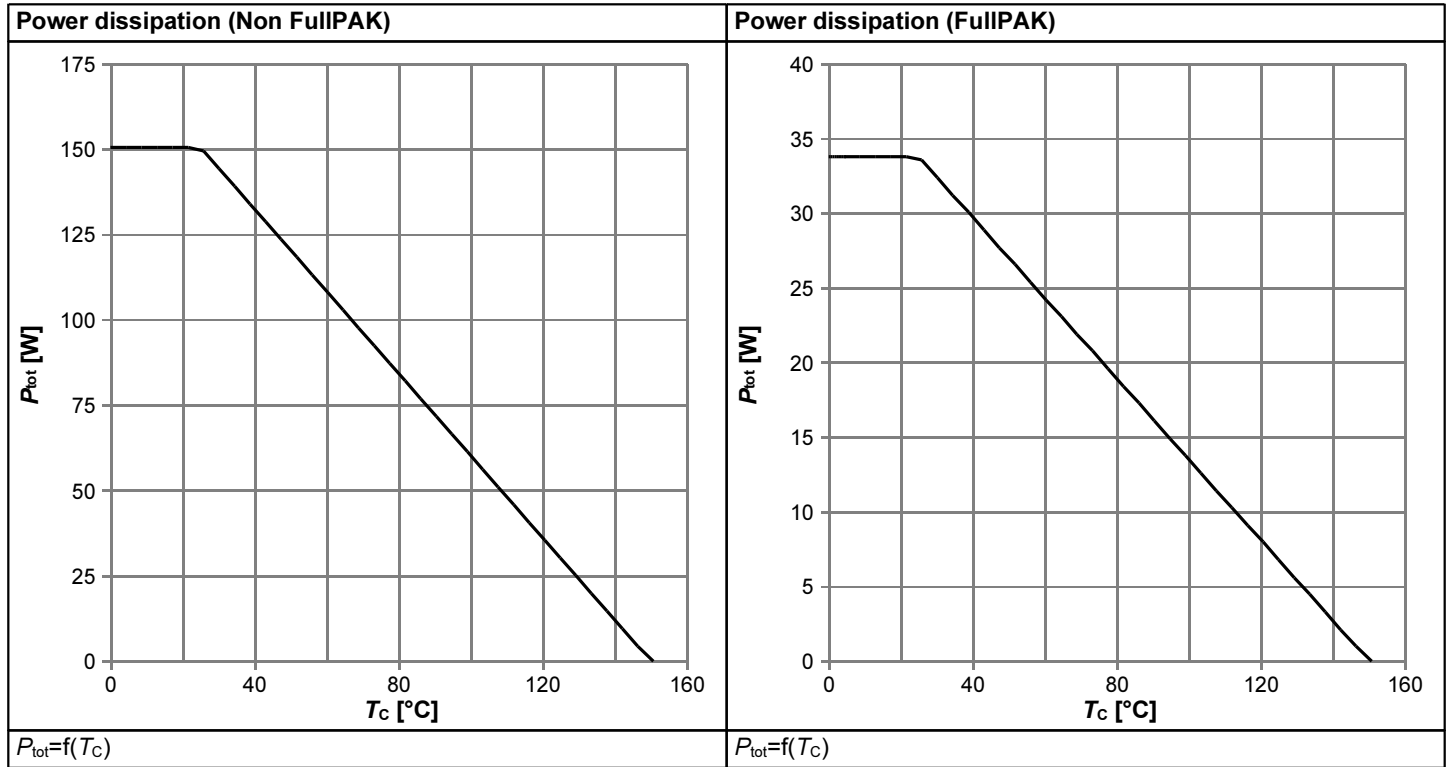
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

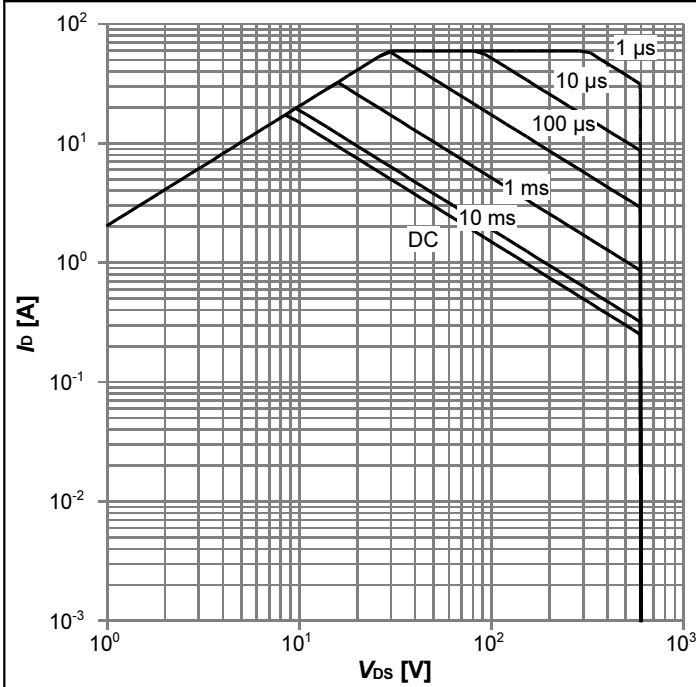
Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V, I_F = 9.5A, T_j = 25^\circ C$
Reverse recovery time	t_{rr}		430		ns	$V_R = 400V, I_F = 9.5A,$ $di_F/dt = 100A/\mu s$ (see table 9)
Reverse recovery charge	Q_{rr}		6.9		μC	
Peak reverse recovery current	I_{rrm}		30		A	

5 Electrical characteristics diagrams

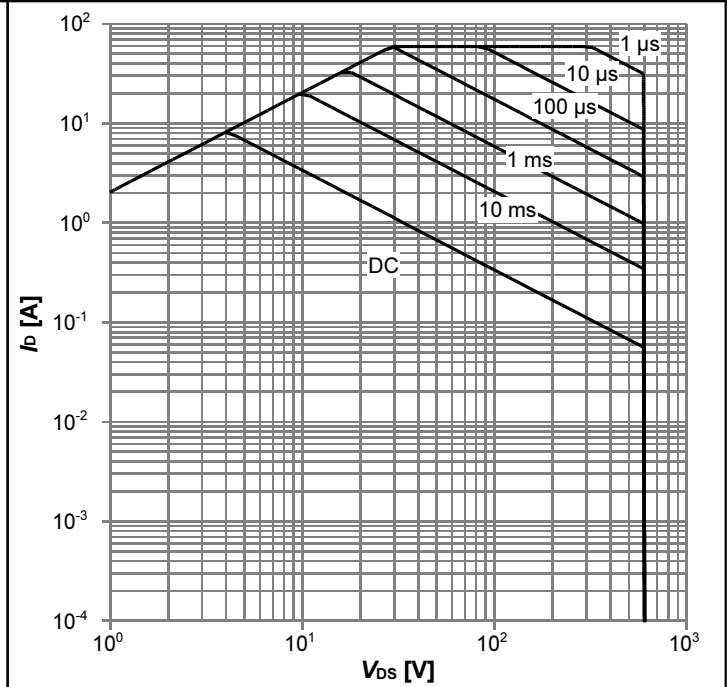


Safe operating area $T_c=25^\circ\text{C}$ (Non FullPAK)



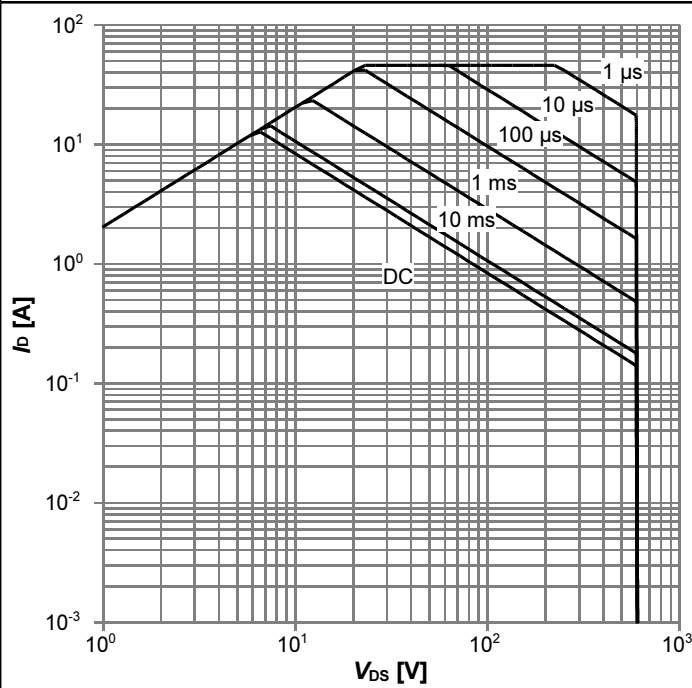
$I_D=f(V_{DS}); T_c=25^\circ\text{C}; D=0$; parameter: t_p

Safe operating area $T_c=25^\circ\text{C}$ (FullPAK)



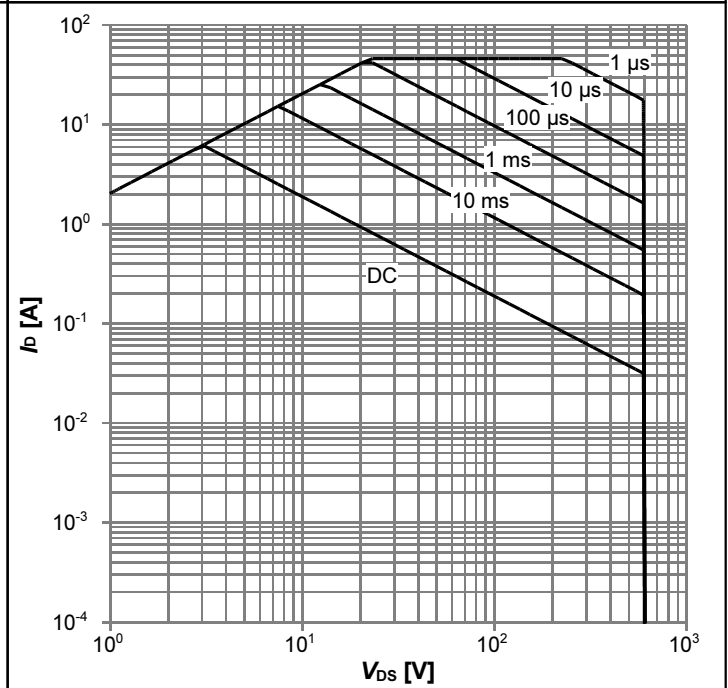
$I_D=f(V_{DS}); T_c=25^\circ\text{C}; D=0$; parameter: t_p

Safe operating area $T_c=80^\circ\text{C}$ (Non FullPAK)



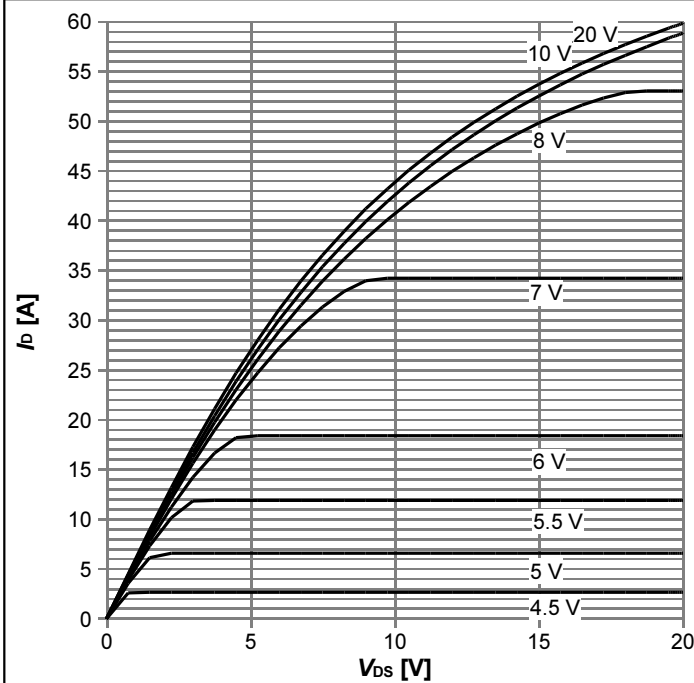
$I_D=f(V_{DS}); T_c=80^\circ\text{C}; D=0$; parameter: t_p

Safe operating area $T_c=80^\circ\text{C}$ (FullPAK)



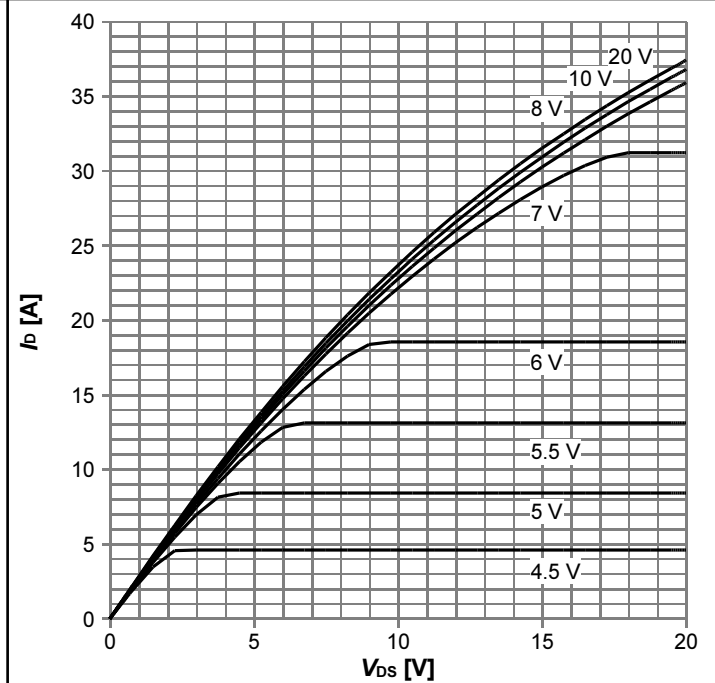
$I_D=f(V_{DS}); T_c=80^\circ\text{C}; D=0$; parameter: t_p

Typ. output characteristics $T_c=25^\circ\text{C}$



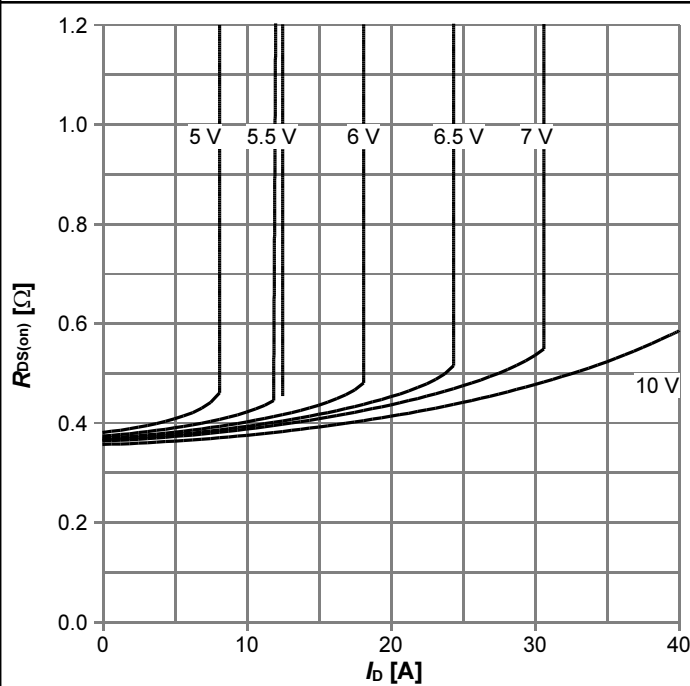
$I_D=f(V_{DS}); T_j=25^\circ\text{C};$ parameter: V_{GS}

Typ. output characteristics $T_c=125^\circ\text{C}$



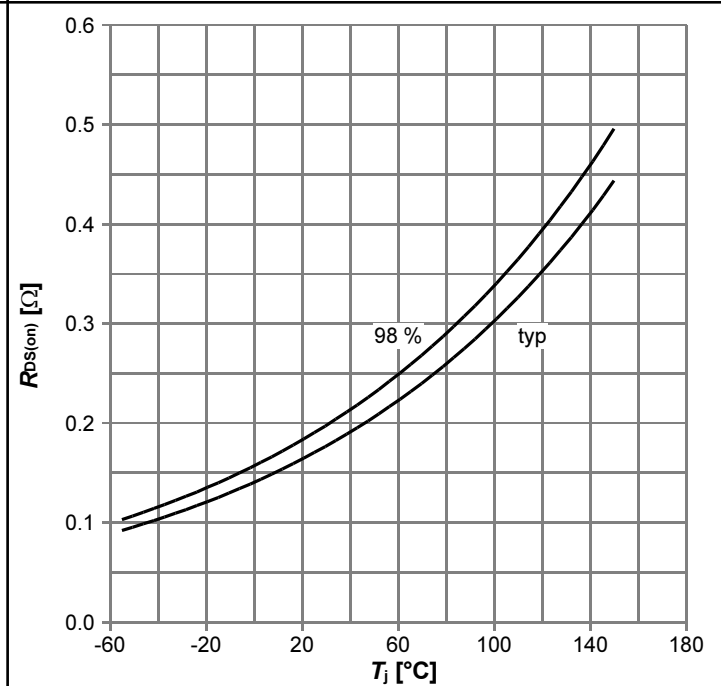
$I_D=f(V_{DS}); T_j=125^\circ\text{C};$ parameter: V_{GS}

Typ. drain-source on-state resistance

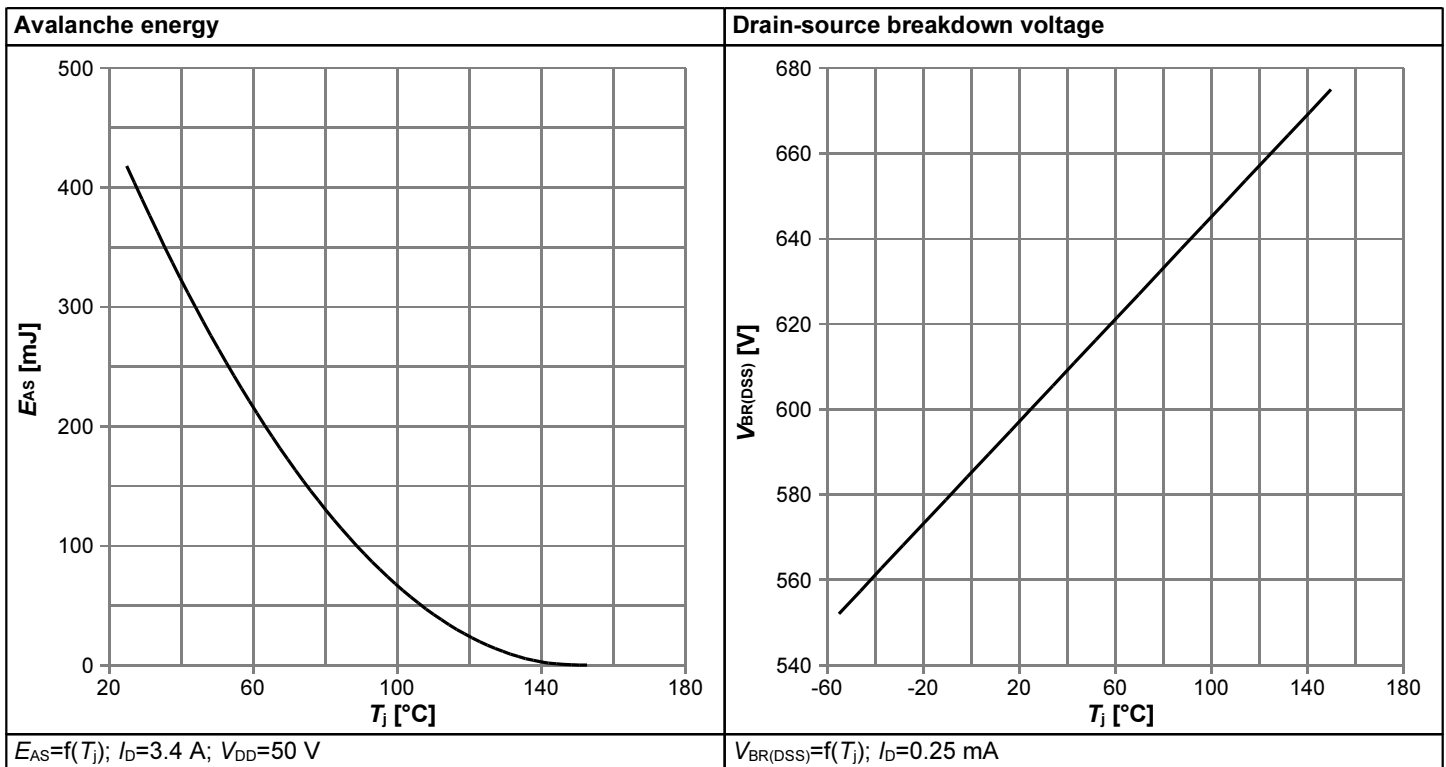
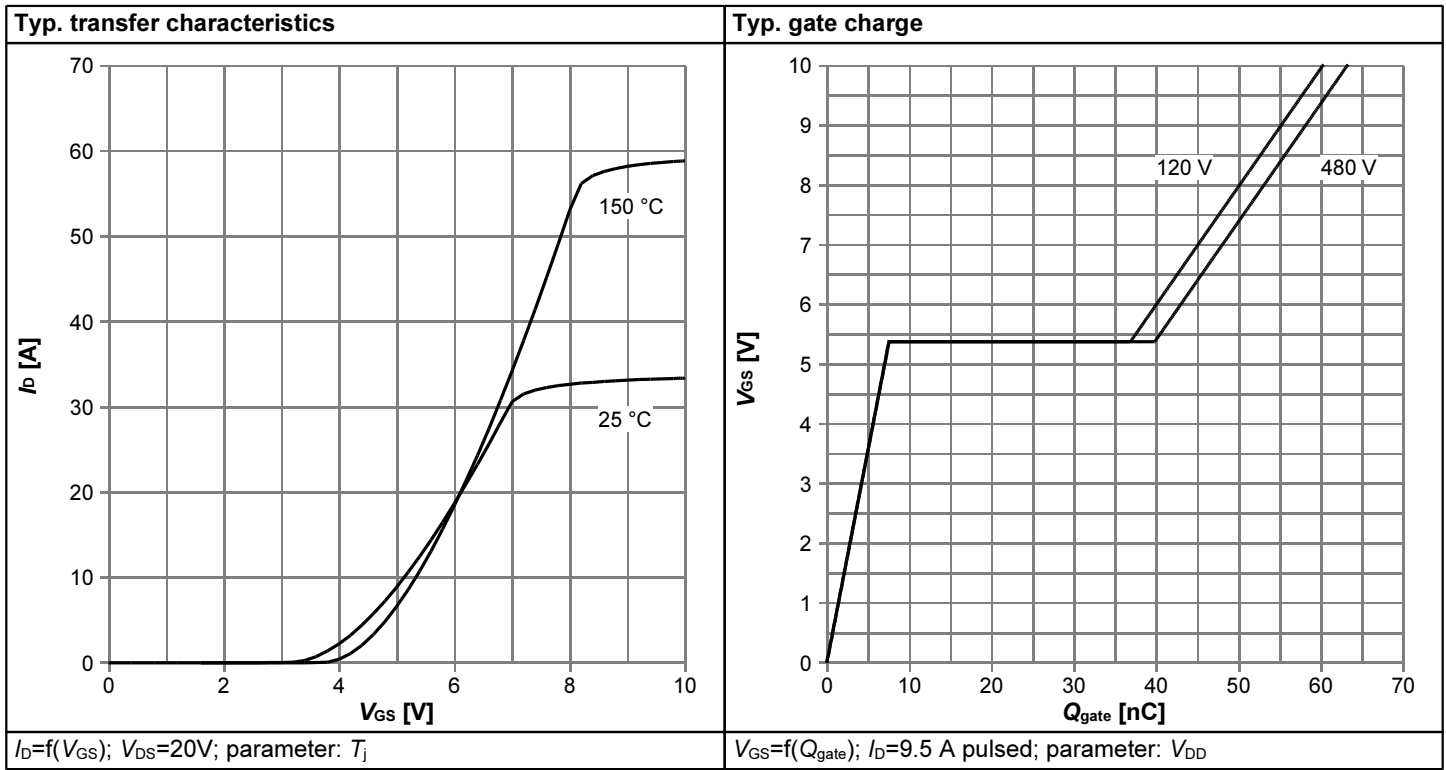


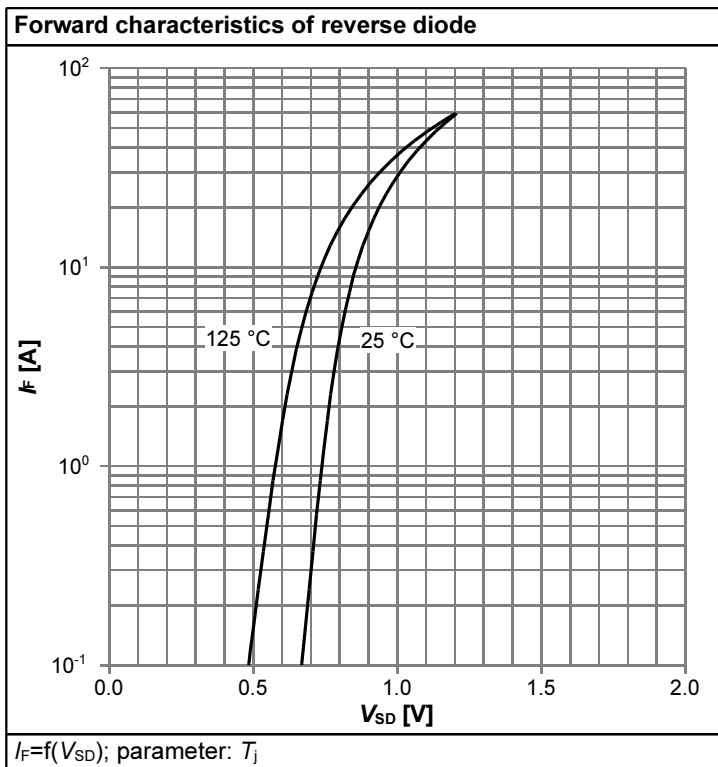
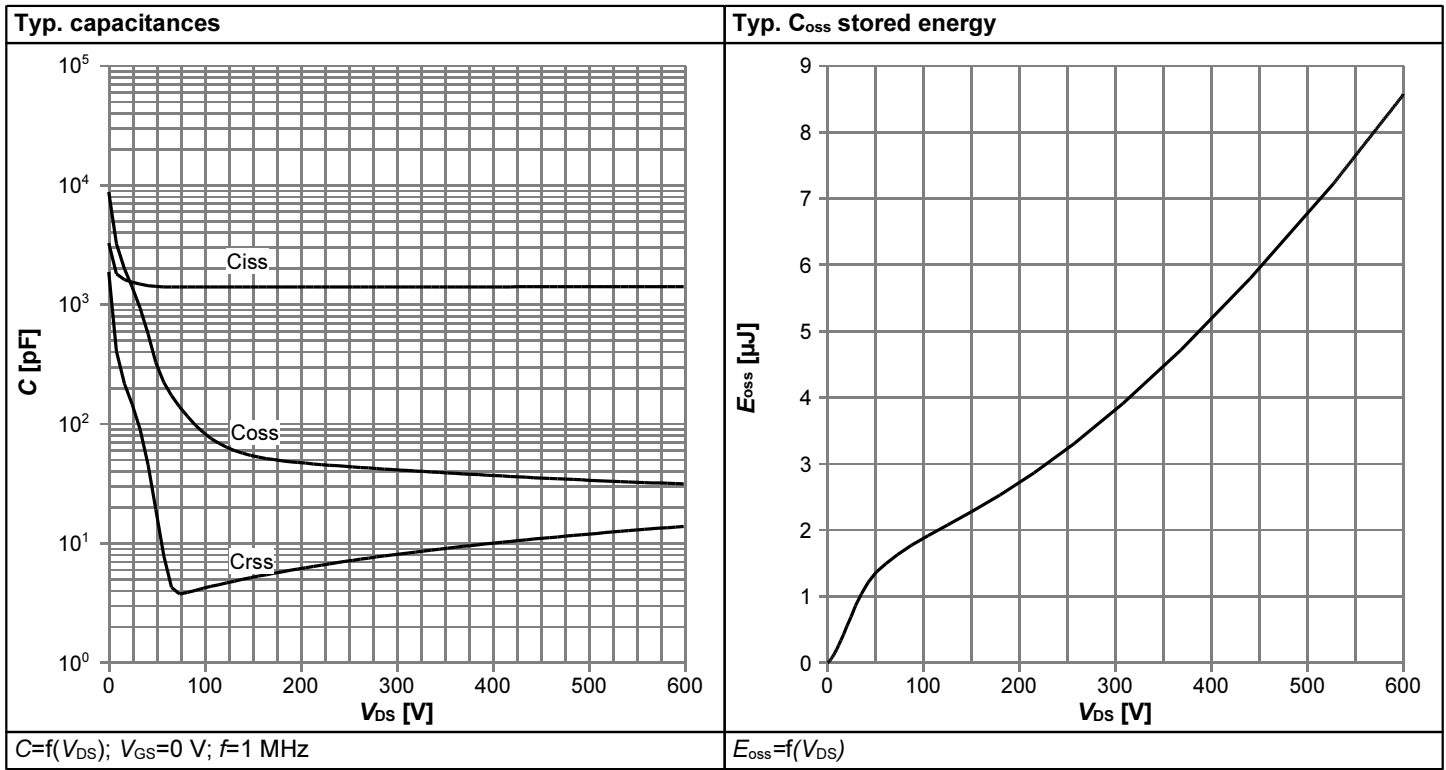
$R_{DS(on)}=f(I_D); T_j=125^\circ\text{C};$ parameter: V_{GS}

Drain-source on-state resistance



$R_{DS(on)}=f(T_j); I_D=9.5\text{ A}; V_{GS}=10\text{ V}$





6 Test Circuits

Table 9 Diode characteristics

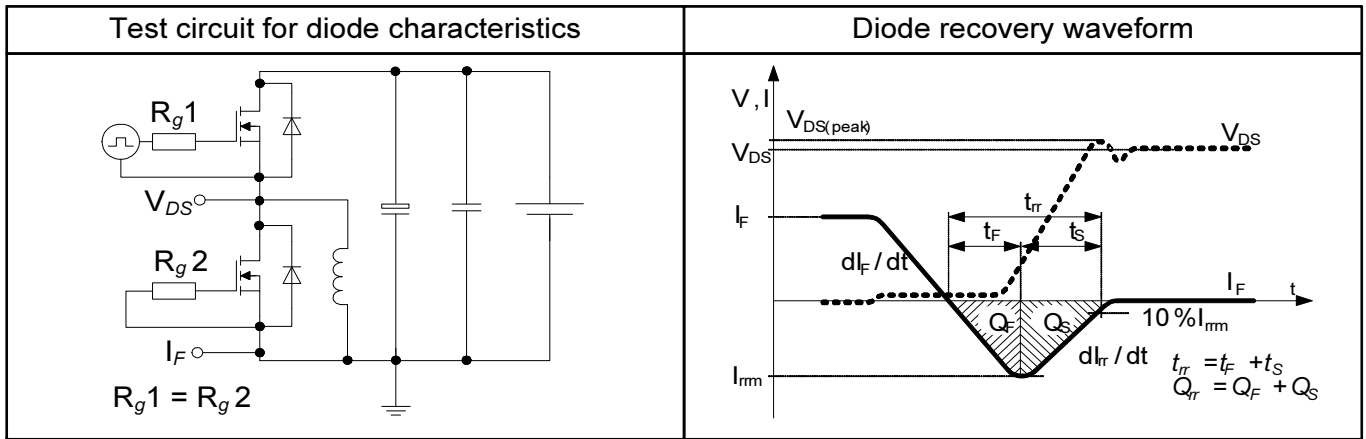


Table 10 Switching times

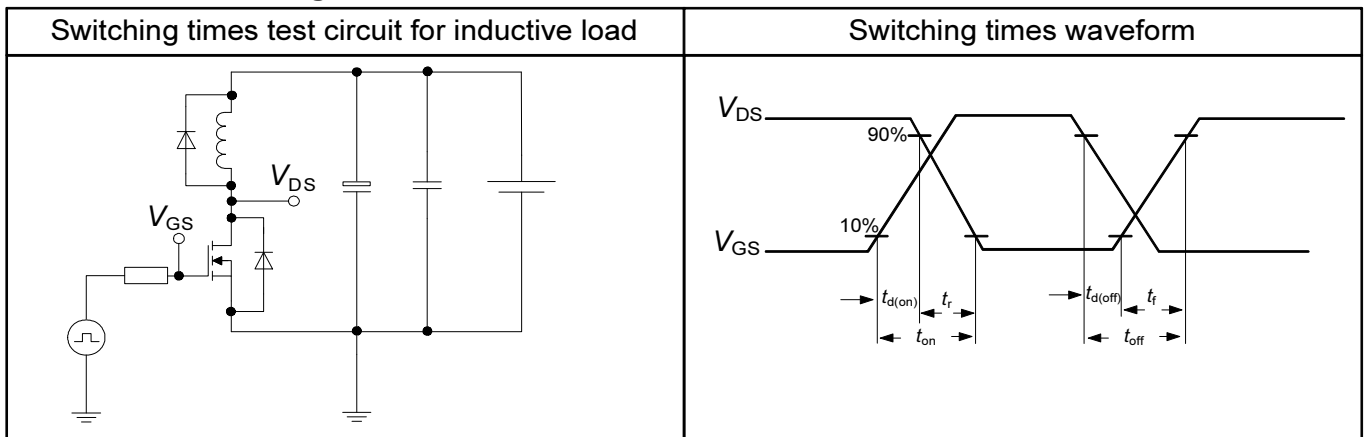
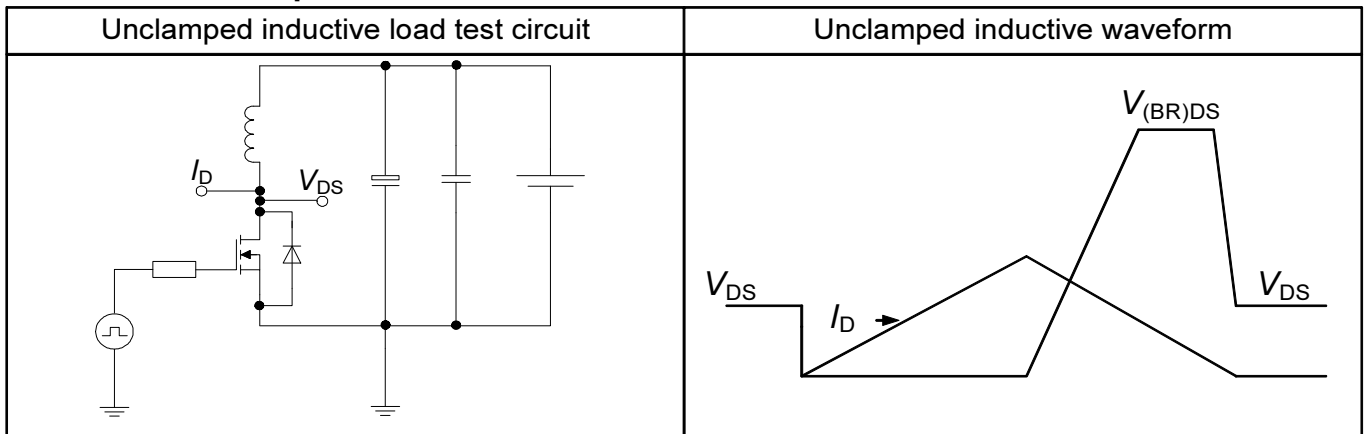


Table 11 Unclamped inductive load



7 Package Outlines

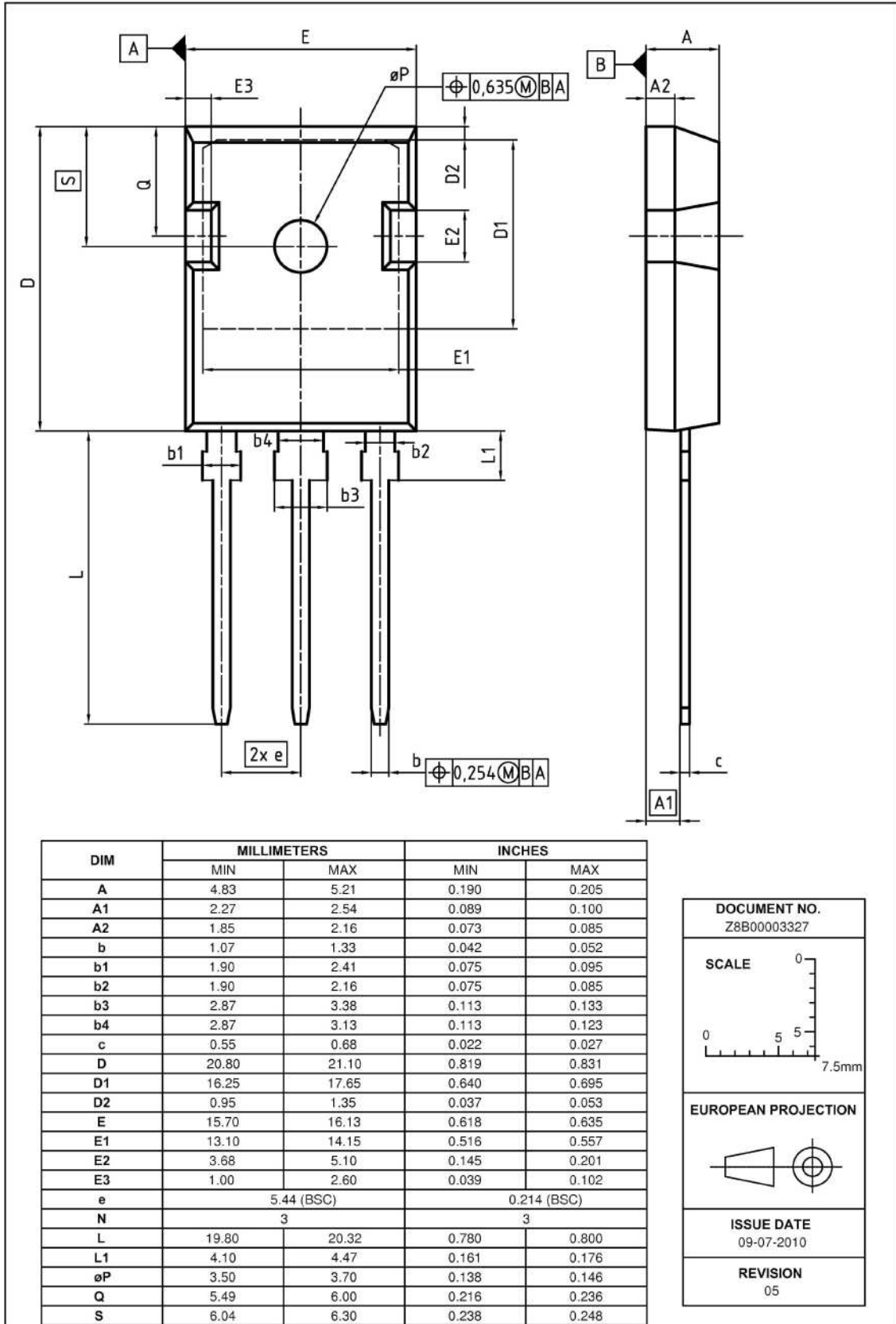


Figure 1 Outline PG-TO 247, dimensions in mm/inches

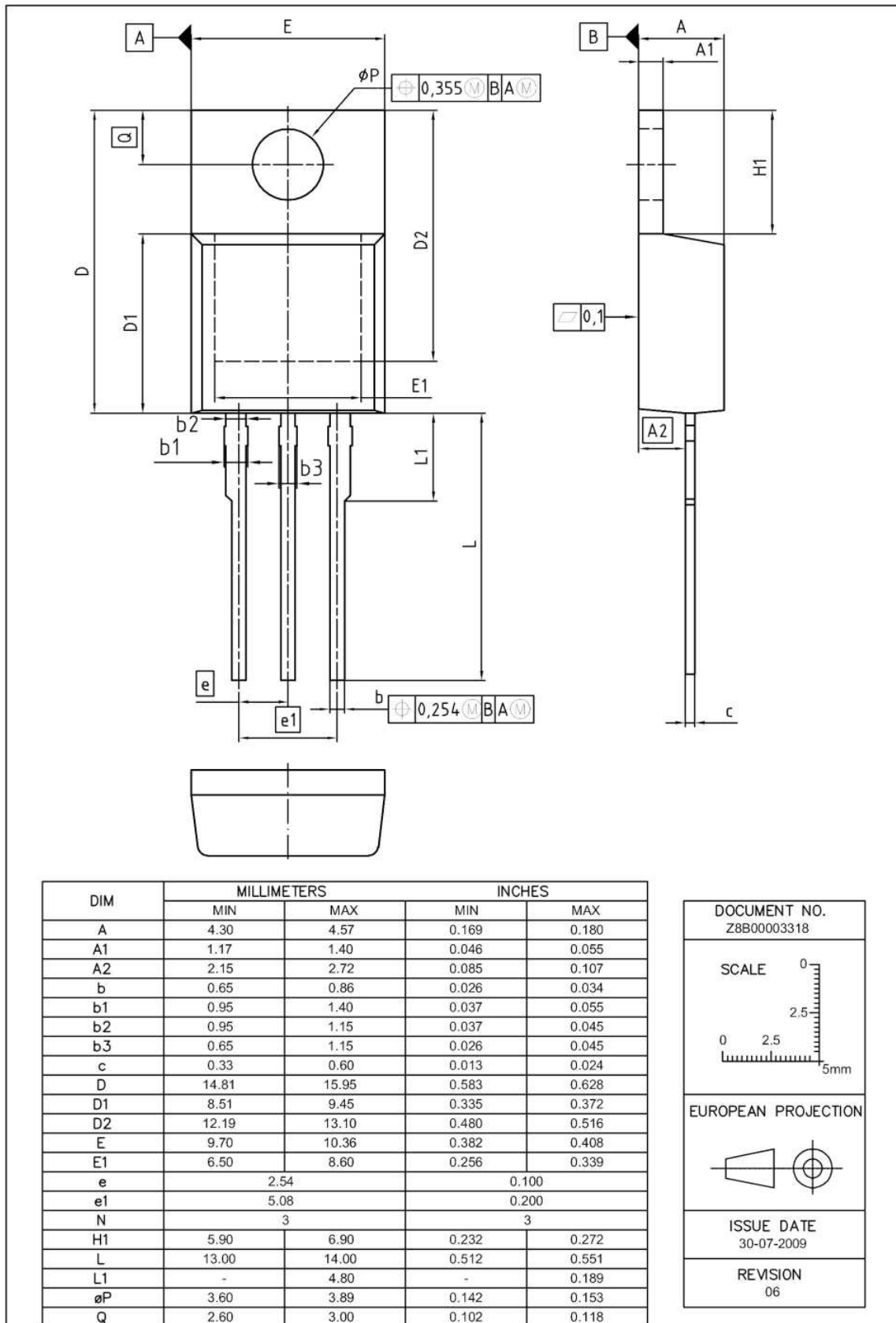
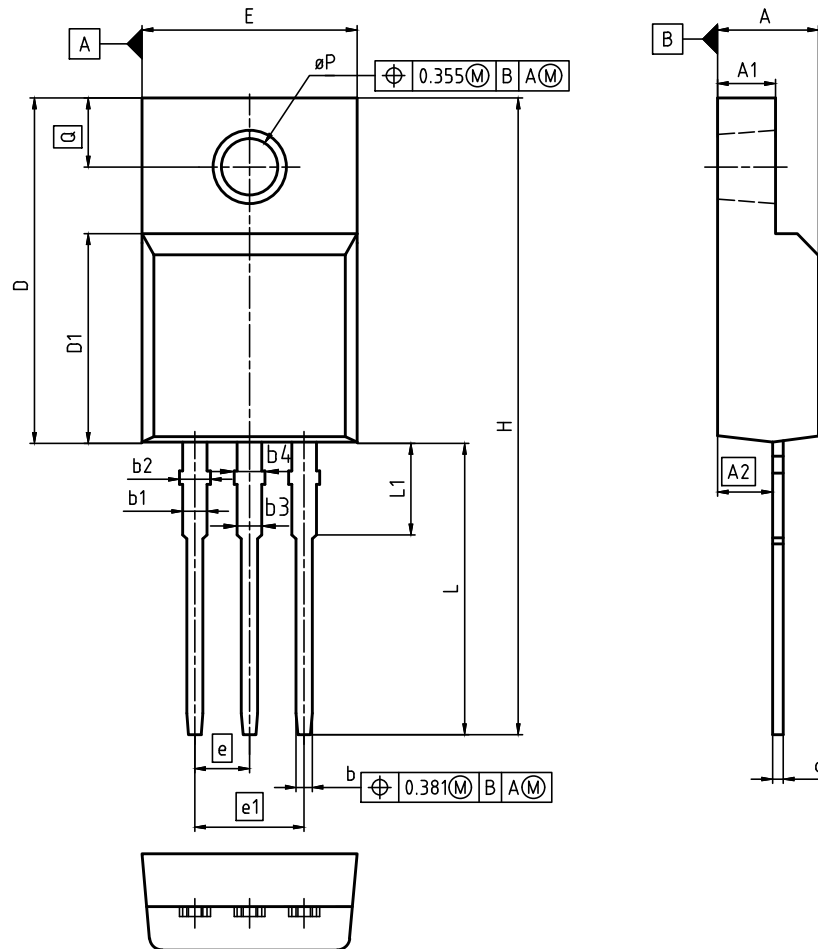


Figure 2 Outline PG-TO 220, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

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Figure 3 Outline PG-TO 220 FullPAK, dimensions in mm/inches

8 Appendix A

Table 12 Related Links

- IFX CoolMOS Webpage: www.infineon.com
- IFX Design Tools: www.infineon.com

Revision History

IPx60R190E6

Revision: 2015-02-09, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2011-06-08	Release of final data sheet
2.1	2011-09-14	-
2.2	2014-07-15	Package update and table reference correction
2.3	2015-02-09	PG-TO220 FullPAK package outline update (creation:2014-12-02)

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