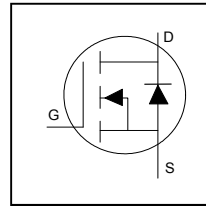


HEXFET® Power MOSFET

Application

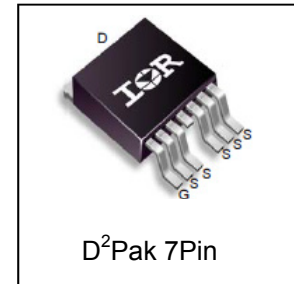
- Motion Control Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- Hard Switched and High Frequency Circuits



V_{DSS}	150V
R_{DS(on)} typ.	11.7mΩ
	14.7mΩ
I_D	86A

Benefits

- Low R_{dson} Reduces Losses
- Low Gate Charge Improves the Switching Performance
- Improved Diode Recovery Improves Switching & EMI Performance
- 30V Gate Voltage Rating Improves Robustness
- Fully Characterized Avalanche SOA



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFS4321-7PPbF	D ² Pak-7Pin	Tube	50	IRFS4321-7PPbF
		Tape and Reel Left	800	IRFS4321TRL7PP

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	86	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	61	
I _{DM}	Pulsed Drain Current ①	343	
P _D @ T _C = 25°C	Maximum Power Dissipation	350	W
	Linear Derating Factor	2.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	120	mJ
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ④	—	0.43*	°C/W
R _{θJA}	Junction-to-Ambient	—	40	

* R_{θJC} (end of life) for D2Pak and TO-262 = 0.65°C/W. This is the maximum measured value after 1000 temperature cycles from -55 to 150°C and is accounted for by the physical wear out of the die attach medium.

Notes ① through ④ are on page 2

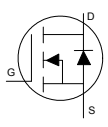
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	150	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	150	—	mV/°C	Reference to 25°C, I _D = 1mA ①
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	11.7	14.7	mΩ	V _{GS} = 10V, I _D = 34A ③
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 150V, V _{GS} = 0V
		—	—	1.0	mA	V _{DS} = 150V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V _{GS} = -20V
R _{G(int)}	Internal Gate Resistance	—	0.8	—	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

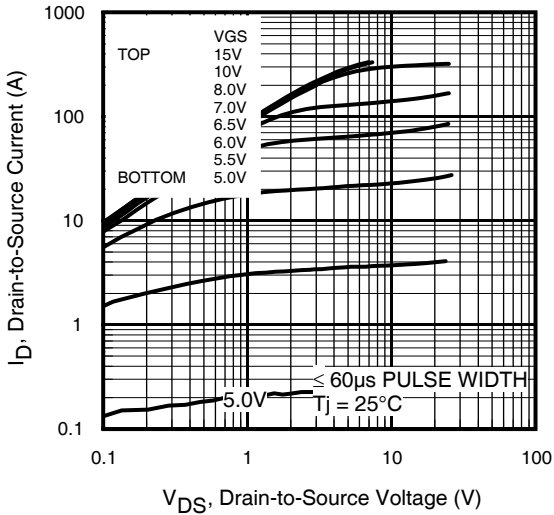
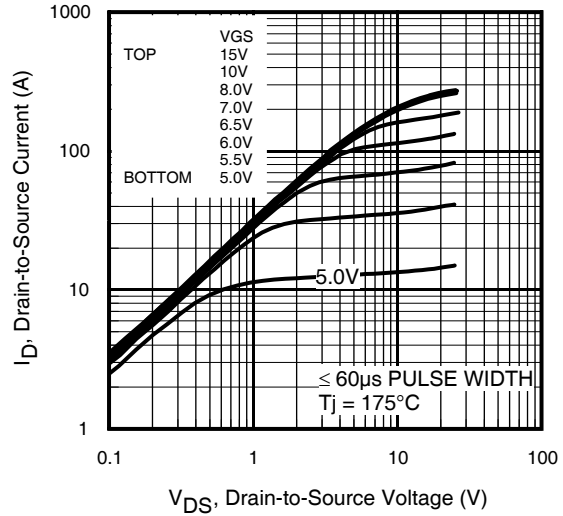
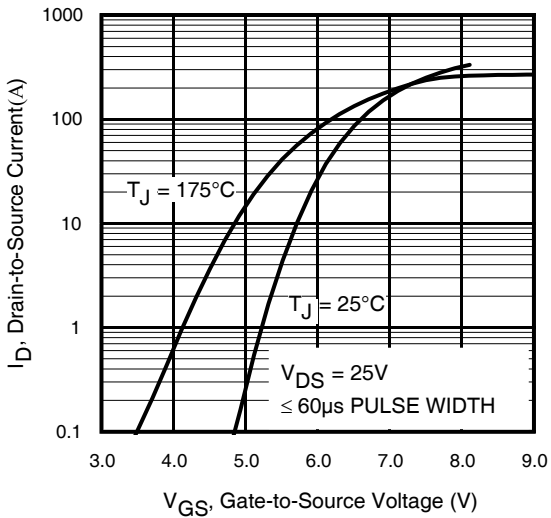
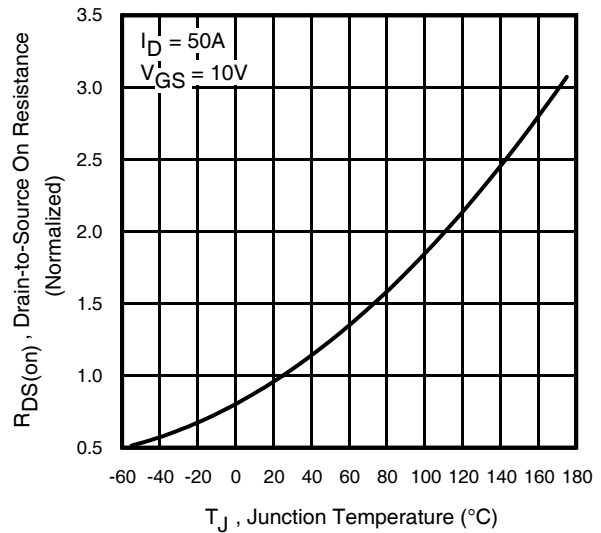
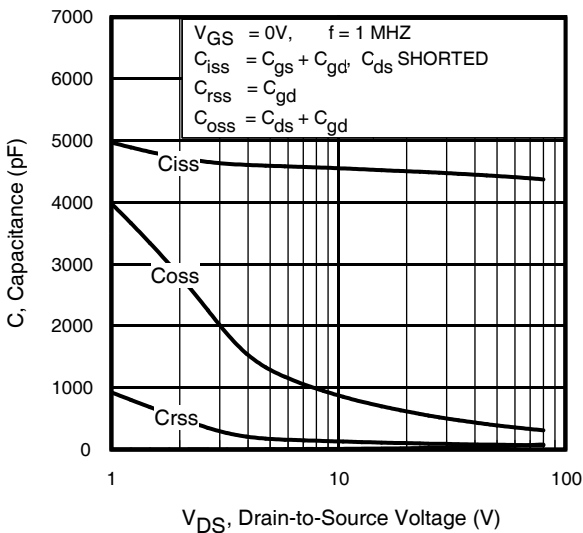
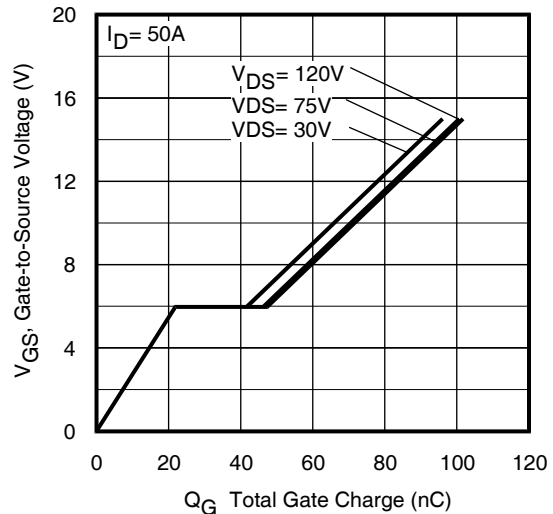
g _{fs}	Forward Transconductance	130	—	—	S	V _{DS} = 25V, I _D = 50A
Q _g	Total Gate Charge	—	71	110	nC	I _D = 50A
Q _{gs}	Gate-to-Source Charge	—	24			V _{DS} = 75V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	21			V _{GS} = 10V ③
t _{d(on)}	Turn-On Delay Time	—	18	—	ns	V _{DD} = 98V
t _r	Rise Time	—	60	—		I _D = 50A
t _{d(off)}	Turn-Off Delay Time	—	25	—		R _G = 2.5Ω
t _f	Fall Time	—	35	—		V _{GS} = 10V ③
C _{iss}	Input Capacitance	—	4460	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	390	—		V _{DS} = 50V
C _{rss}	Reverse Transfer Capacitance	—	82	—		f = 1.0MHz

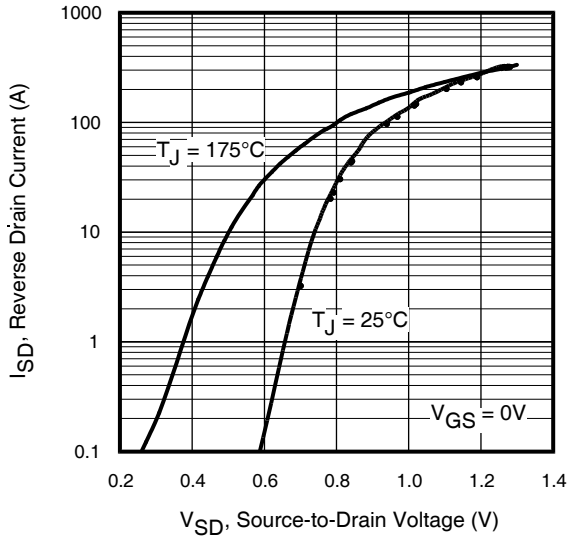
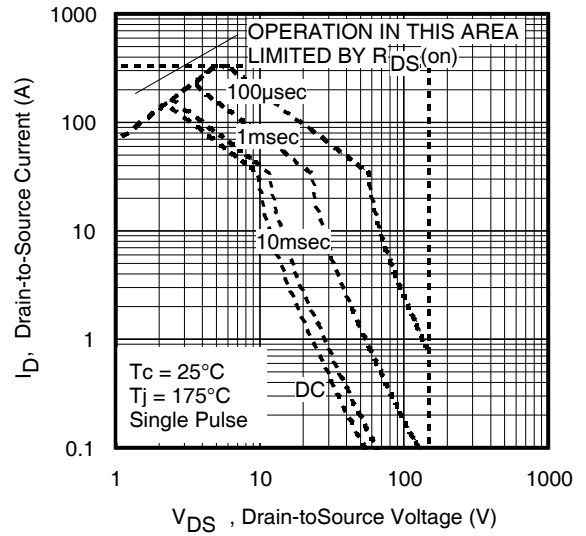
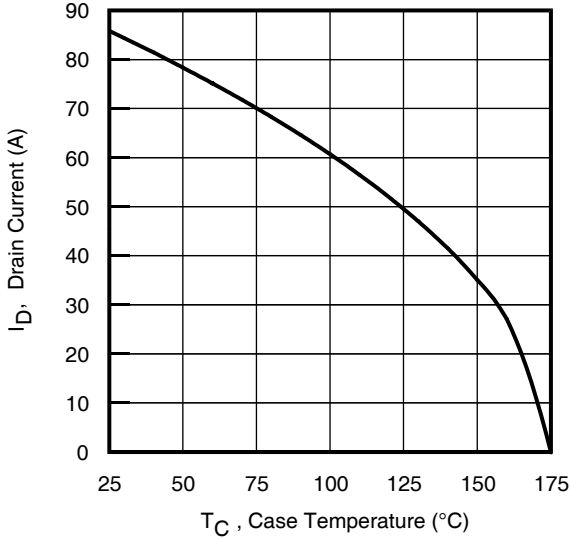
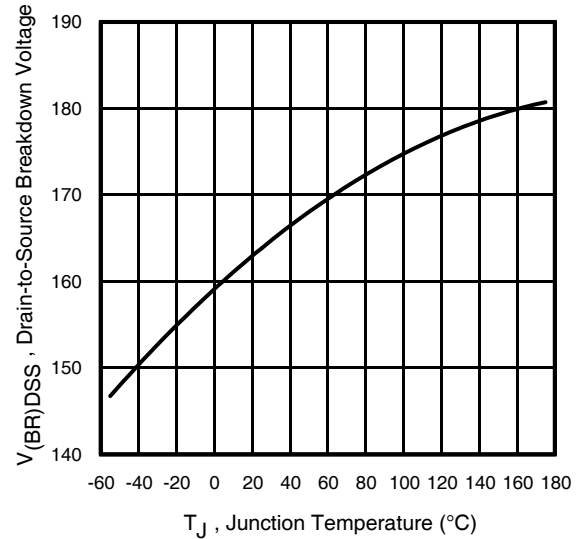
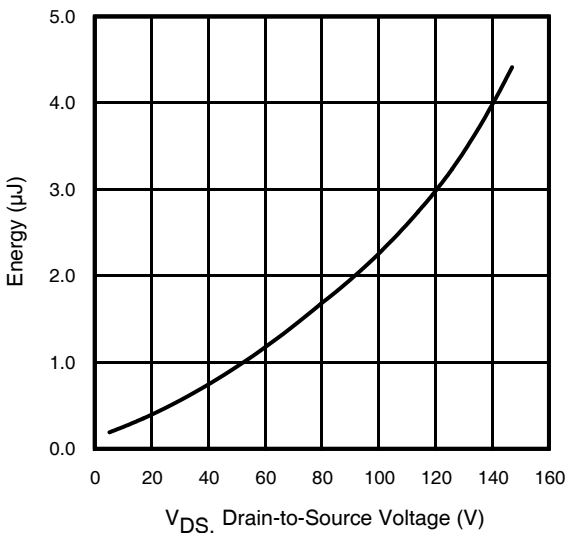
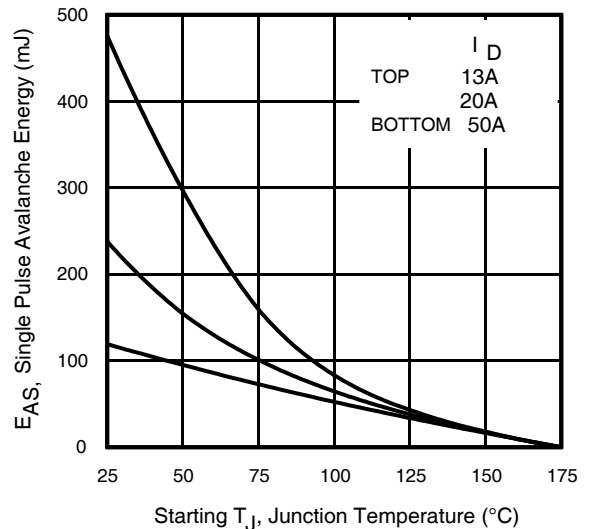
Diode Characteristics

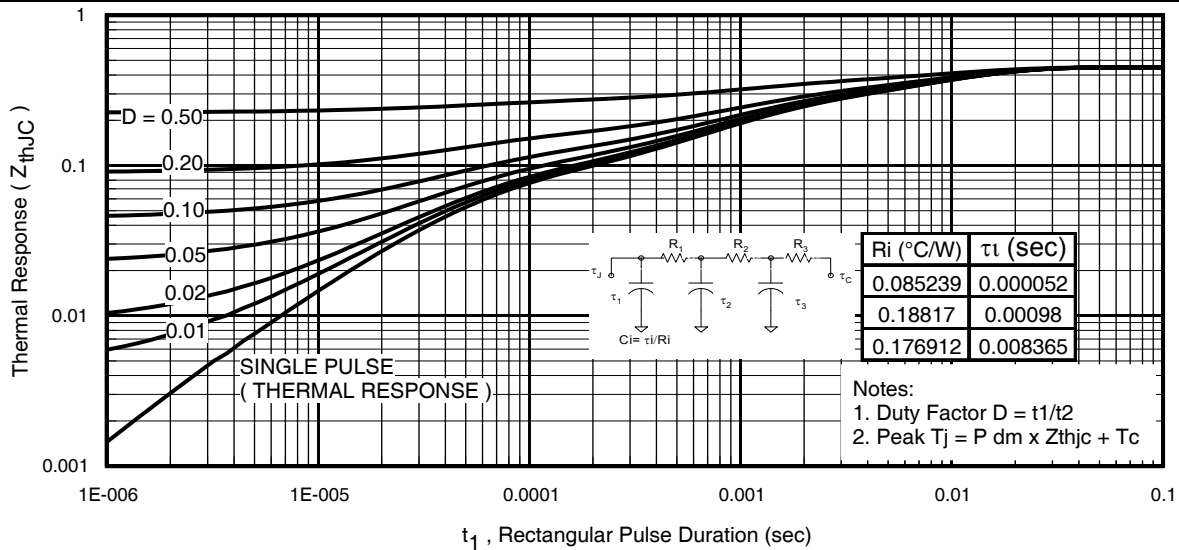
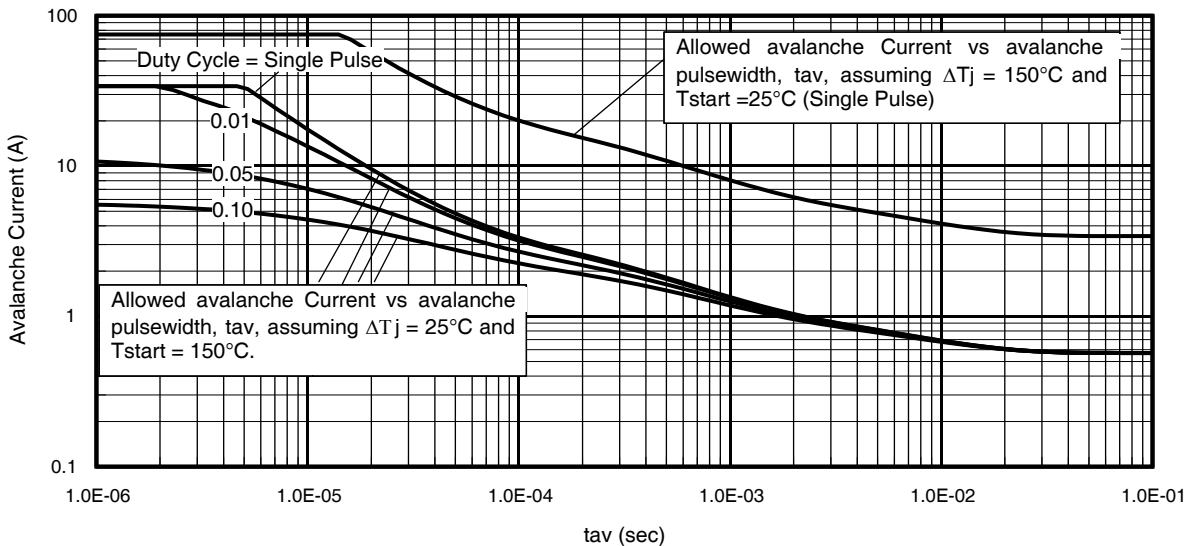
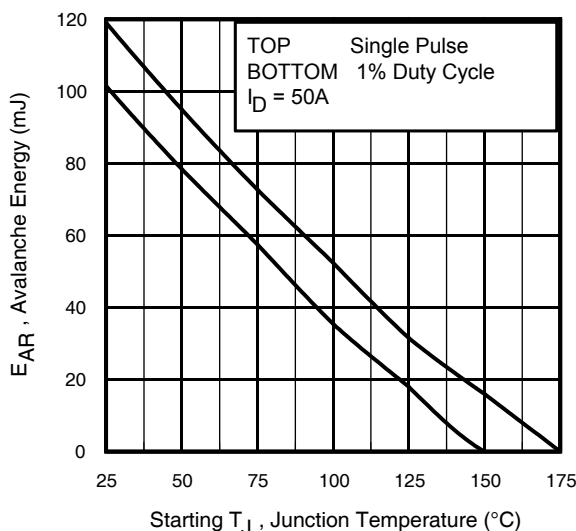
	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	86	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	343		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 50A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	89	130	ns	I _F = 50A, V _{DD} = 128V
Q _{rr}	Reverse Recovery Charge	—	300	450	nC	
I _R RM	Reverse Recovery Current	—	6.5	—	A	

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.096mH, R_G = 25Ω, I_{AS} = 50A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ R_θ is measured at T_J approximately 90°C


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig 11. Typical C_{oss} Stored Energy

Fig 12. Maximum Avalanche Energy Vs. Drain Current


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulse width

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

 t_{av} = Average time in avalanche.

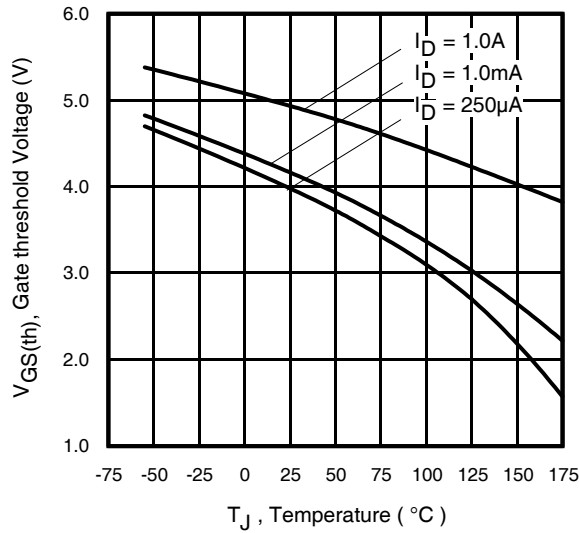
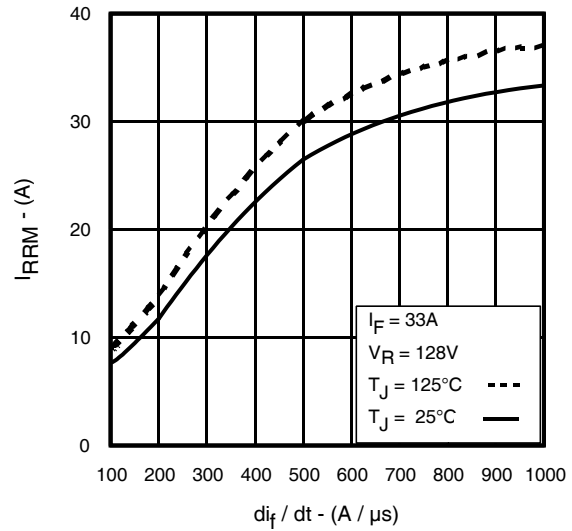
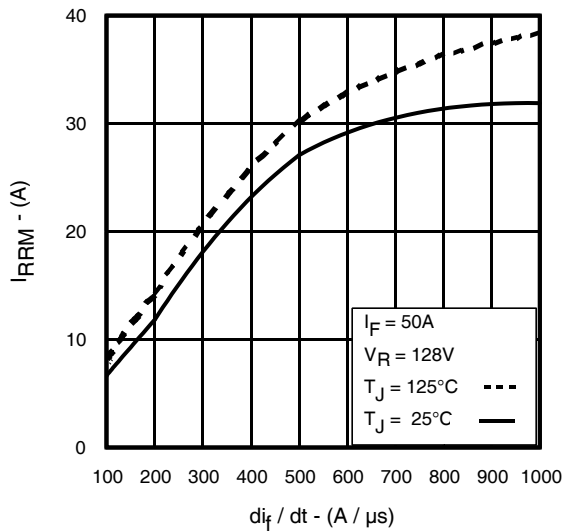
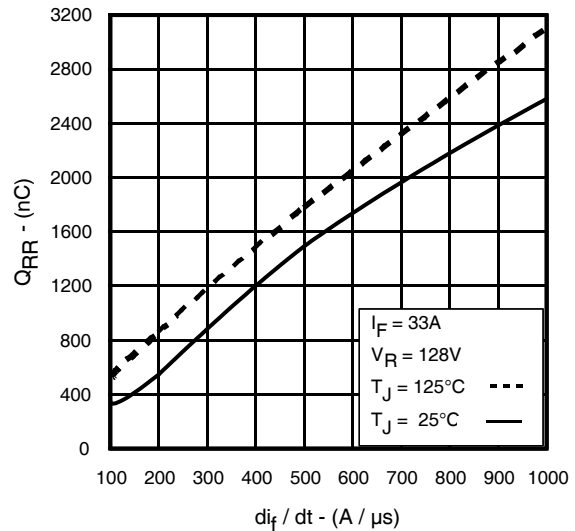
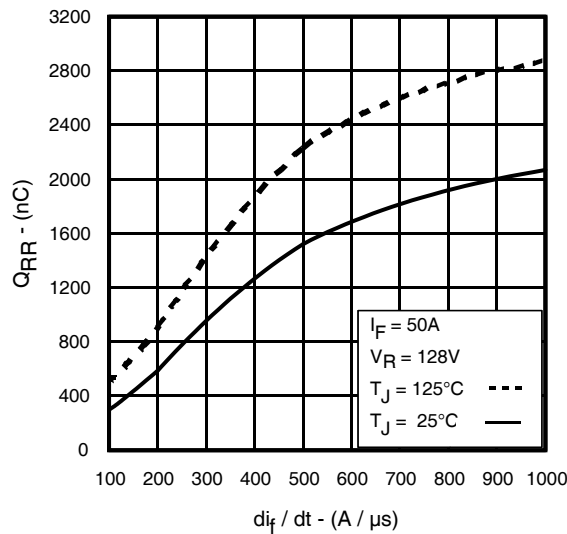
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

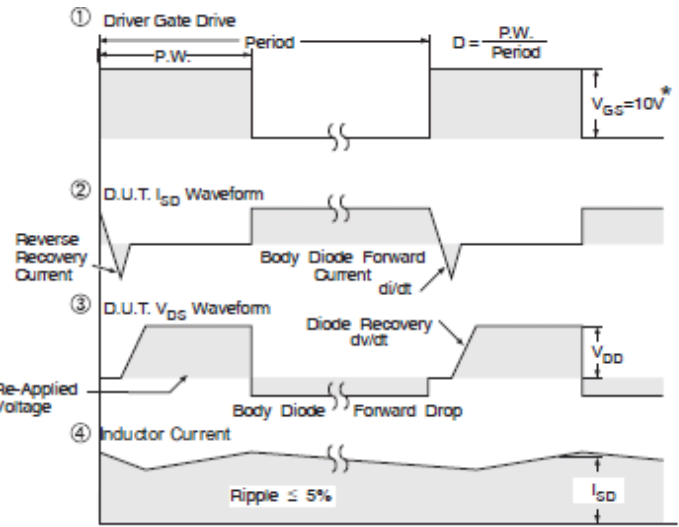
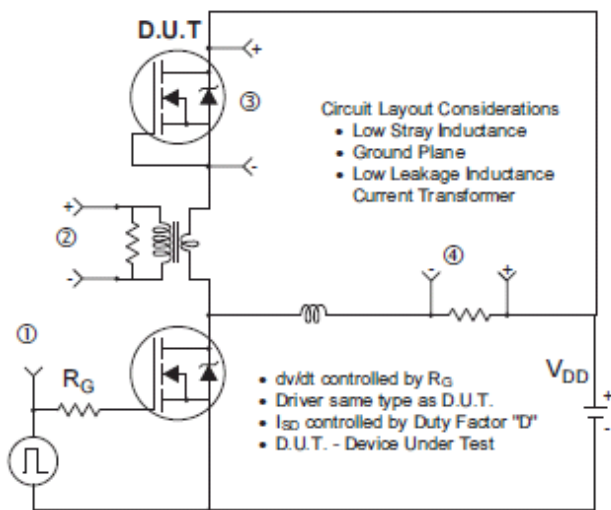
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature


Fig 16. Threshold Voltage vs. Temperature

Fig 17. Typical Recovery Current vs. di_f/dt

Fig 18. Typical Recovery Current vs. di_f/dt

Fig 19. Typical Stored Charge vs. di_f/dt

Fig 20. Typical Stored Charge vs. di_f/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET[®] Power MOSFETs

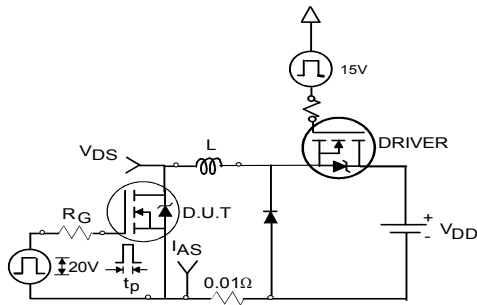


Fig 22a. Unclamped Inductive Test Circuit

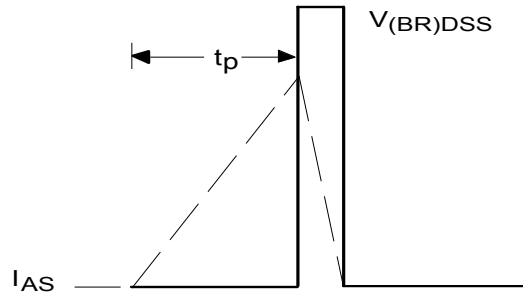


Fig 22b. Unclamped Inductive Waveforms

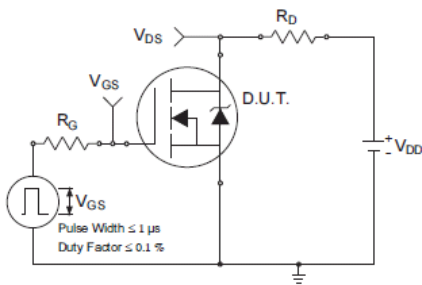


Fig 23a. Switching Time Test Circuit

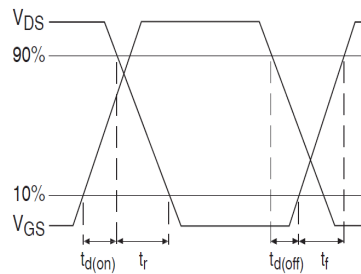


Fig 23b. Switching Time Waveforms

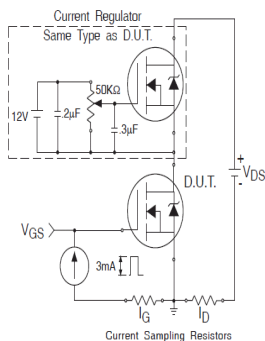


Fig 24a. Gate Charge Test Circuit

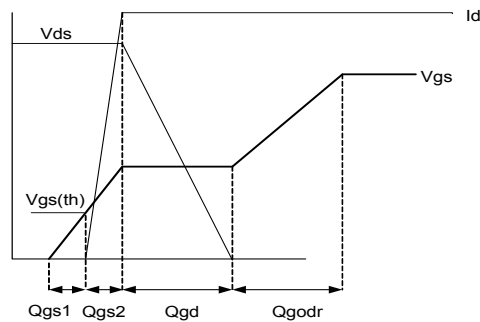
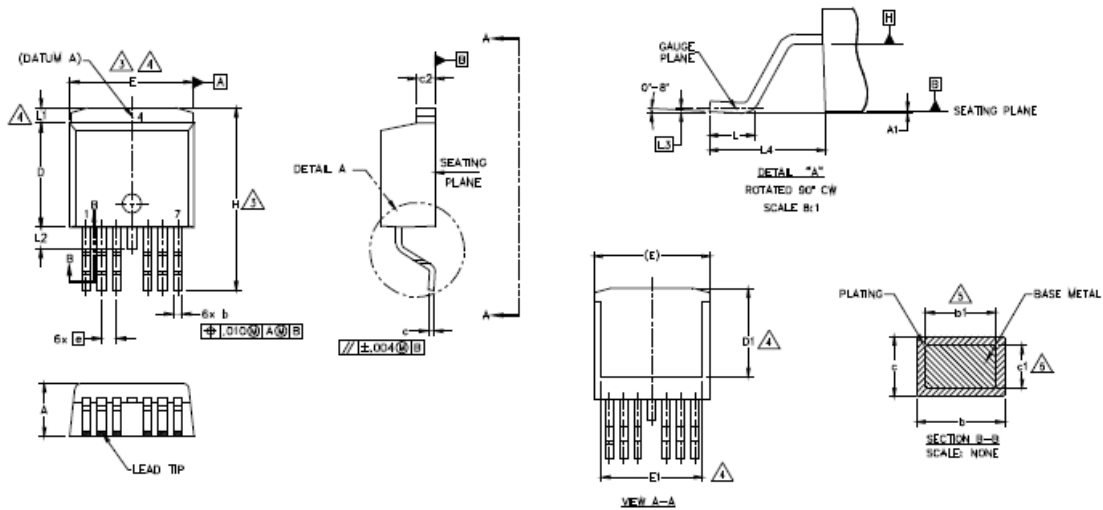


Fig 24b. Gate Charge Waveform

D²Pak-7Pin Package Outline (Dimensions are shown in millimeters (inches))


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	
E	9.65	10.67	.380	.420	
E1	6.22	—	.245	—	
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

NOTES:

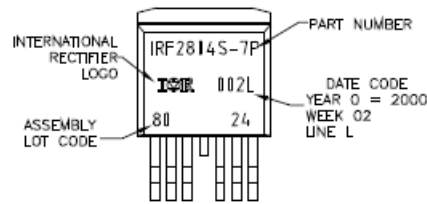
- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
- \triangle DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- \triangle THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
- \triangle DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- CONTROLLING DIMENSION: INCH.
- OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

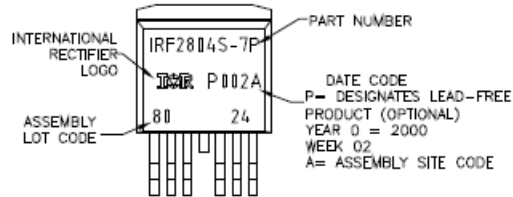
D²Pak-7Pin Part Marking Information

EXAMPLE: THIS IS AN IRF2804S-7P WITH
LOT CODE 8024
ASSEMBLED ON WW02,2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead Free"



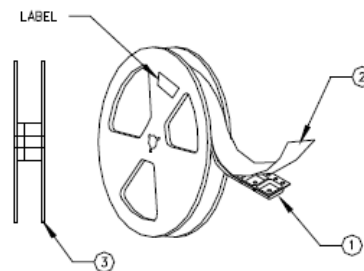
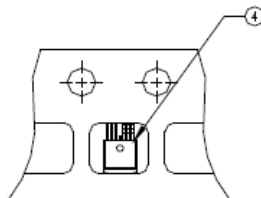
OR



D2Pak-7Pin Tape and Reel

NOTES, TAPE & REEL LABELLING:

1. TAPE AND REEL.
 - 1.1 REEL SIZE 13 INCH DIAMETER.
 - 1.2 EACH REEL CONTAINING 800 DEVICES.
 - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
 - 1.4 REEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
 - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
 - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.
2. LABELLING (REEL AND SHIPPING BAG).
 - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
 - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
 - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
 - 2.4 QUANTITY:
 - 2.5 VENDOR CODE: IR
 - 2.6 LOT CODE:
 - 2.7 DATE CODE:



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	D ² Pak-7Pin	MSL1
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

International
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[2SK1691-DL-E](#) [2SK2545\(Q,T\)](#) [D2294UK](#) [405094E](#) [423220D](#) [MCH6646-TL-E](#) [TPCC8103,L1Q\(CM](#) [367-8430-0972-503](#) [VN1206L](#)
[424134F](#) [026935X](#) [051075F](#) [SBVS138LT1G](#) [614234A](#) [715780A](#) [NTNS3166NZT5G](#) [751625C](#) [873612G](#) [IRF7380TRHR](#)
[IPS70R2K0CEAKMA1](#) [RJK60S3DPP-E0#T2](#) [RJK60S5DPK-M0#T0](#) [APT5010JVFR](#) [APT12031JFLL](#) [APT12040JVR](#) [DMN3404LQ-7](#)
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