# ISL71444M

19MHz 40V Quad Rail-to-Rail Input-Output, Low-Power Operational Amplifiers

FN8892
Rev.0.00
Jun 6, 2017

The ISL71444M features four radiation tolerant, low-power amplifiers optimized to provide maximum dynamic range. These op amps feature a unique combination of rail-to-rail operation on the input and output as well as a slew enhanced front-end that provides ultra fast slew rates positively proportional to a given step size. They also offer low-power, low-offset voltage, and low temperature drift, making it ideal for applications requiring both high DC accuracy and AC performance.

## Features

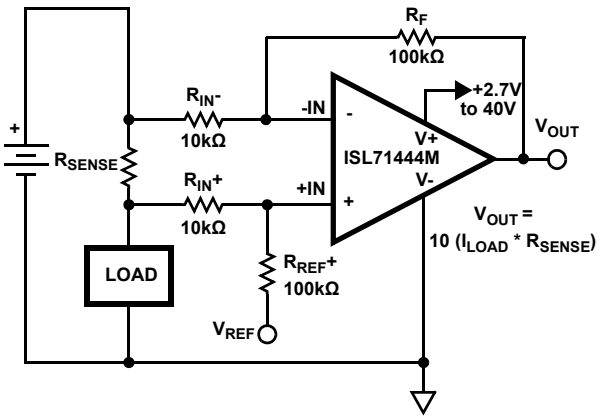
- Unity gain stable with wide gain-bandwidth product: 19MHz
- Wide single and dual supply range: 2.7V to 40V max
- Low input offset voltage: 400µV
- Low current consumption (per amplifier): 1.1mA, typ
- High large signal slew rate: 60V/µs
- Operating temperature range: -55°C to +125°C
- 14 Ld TSSOP with NiPdAu lead finish
- Characterized radiation level
  - Low Dose Rate (<10mrad(Si)): 30krad(Si)
  - Single Event Effects (LET): 43 MeV•cm$^2$/mg

## Applications

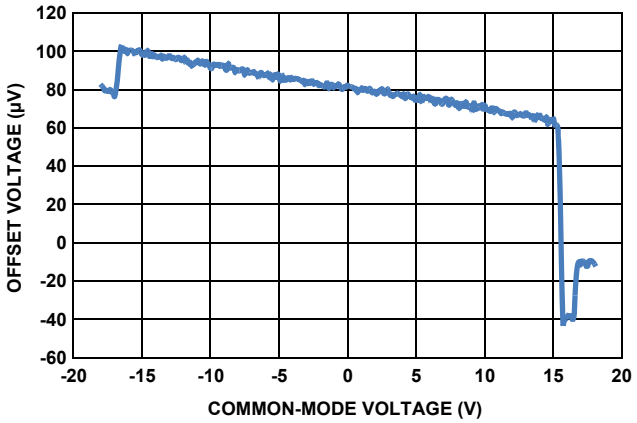
- Low Earth Orbit applications
- High altitude avionics
- Precision instruments
- Data acquisition
- Power supply control

## Related Literature

- For a full list of related documents, visit our website.
  - ISL71444M product page




**Typical Application: Single-Supply, High-Side Current Sense Amplifier**




**Offset Voltage vs Common-Mode Voltage**

# 1. Overview

## 1.1 Ordering Information

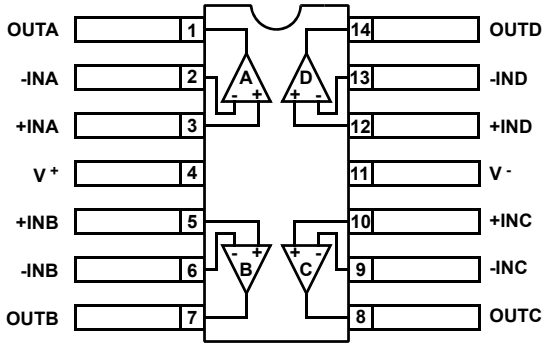
| Part Number (Notes 1, 2, 3) | Part Marking | Temp Range (°C) | Package (RoHS Compliant) | Pkg. Dwg. # |
|---|---|---|---|---|
| ISL71444MVZ | 71444 MVZ | -55 to +125 | 14 Ld TSSOP | M14.173 |
| ISL71444MEVAL1Z | Evaluation Board | | | |

Notes:

1. Add “-T” suffix for 2.5k unit or “-T7A” suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information page for the ISL71444M. For more information on MSL, see TB363.

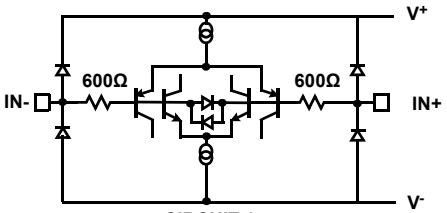
## 1.2 Pin Configuration

ISL71444M
(14 Ld TSSOP)
Top View

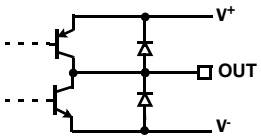


## 1.3 Pin Descriptions

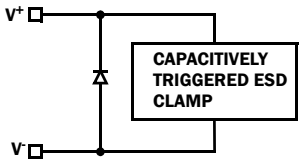
| Pin Number | Pin Name | Equivalent ESD Circuit | Description |
|---|---|---|---|
| 1 | OUTA | Circuit 2 | Amplifier A output |
| 2 | -INA | Circuit 1 | Amplifier A inverting input |
| 3 | +INA | Circuit 1 | Amplifier A non-inverting input |
| 4 | $V^+$ | Circuit 3 | Positive power supply |
| 5 | +INB | Circuit 1 | Amplifier B non-inverting input |
| 6 | -INB | Circuit 1 | Amplifier B inverting input |
| 7 | OUTB | Circuit 2 | Amplifier B output |
| 8 | OUTC | Circuit 2 | Amplifier C output |
| 9 | -INC | Circuit 1 | Amplifier C inverting input |
| 10 | +INC | Circuit 1 | Amplifier C non-inverting input |
| 11 | $V^-$ | Circuit 3 | Negative power supply |
| 12 | +IND | Circuit 1 | Amplifier D non-inverting input |
| 13 | -IND | Circuit 1 | Amplifier D inverting input |
| 14 | OUTD | Circuit 2 | Amplifier D output |



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

# 2. Specifications

## 2.1 Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Maximum Supply Voltage | | 42 | V |
| Maximum Differential Input Current | | 20 | mA |
| Maximum Differential Input Voltage | 42 or $V^-$ - 0.5 | $V^+$ +0.5 | V |
| Min/Max Input Voltage | 42 or $V^-$ - 0.5 | $V^+$ +0.5 | V |
| Max/Min Input Current for Input Voltage >$V^+$ or <$V^-$ | | ±20 | mA |
| **ESD Rating** | **Value** | | **Unit** |
| Human Body Model (Tested per JS-001-2014) | 7 | | kV |
| Machine Model (Tested per JESD22-A115C) | 400 | | V |
| Charged Device Model (Tested per JS-002-2014) | 2 | | kV |
| Latch-Up (Tested per JESD78E; Class 2, Level A), at +125°C | 100 | | mA |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

## 2.2 Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 14 Ld TSSOP Package (Notes 4, 5) | 92 | 30 |

Notes:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board. See TB379.
5. For $\theta_{JC}$, the “case temp” location is the top center.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Storage Temperature Range | -65 | +150 | °C |
| Pb-Free Reflow Profile | see TB493 | | |

## 2.3 Recommended Operation Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Ambient Operating Temperature Range | -55 | +125 | °C |
| Maximum Operating Junction Temperature | | +150 | °C |
| Single Supply Voltage | 3 ±10% | 36 ±10% | V |
| Split Rail Supply Voltage | ±1.5 ±10% | ±18 ±10% | V |

## 2.4 Electrical Specifications

### 2.4.1 $V_S$ = ±18V

$V_{CM}$ = $V_O$ = 0V, $R_L$ = Open, $T_A$ = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

| Parameter | Symbol | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = 0V | -400 | 100 | 400 | µV |
| | | $V_{CM}$ = $V^+$ to $V^-$ | **-500** | 130 | **500** | µV |
| Offset Voltage Temperature Coefficient | $TCV_{OS}$ | $V_{CM}$ = $V^+$ - 2V to $V^-$ + 2V | - | 0.5 | - | µV/°C |
| Input Offset Channel-to-Channel Match | $\Delta V_{OS}$ | $V_{CM}$ = $V^+$ | **-800** | 150 | **800** | µV |
| | | $V_{CM}$ = $V^-$ | **-800** | 170 | **800** | µV |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0V | - | 200 | **500** | nA |
| | | $V_{CM}$ = $V^+$ | - | 174 | **500** | nA |
| | | $V_{CM}$ = $V^-$ | - | 268 | **650** | nA |
| | | $V_{CM}$ = $V^+$ - 0.5V | - | 174 | **500** | nA |
| | | $V_{CM}$ = $V^-$ + 0.5V | - | 268 | **650** | nA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = $V^+$ to $V^-$ | -30 | 3 | 30 | nA |
| | | | **-50** | - | **50** | nA |
| Common-Mode Input Voltage Range | $V_{CMIR}$ | | **V-** | - | **V+** | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = $V^-$ to $V^+$ | **70** | 113 | - | dB |
| | | $V_{CM}$ = $V^+$ - 0.5V to $V^-$ + 0.5V | **80** | 113 | - | dB |
| Power Supply Rejection Ratio | PSRR | $V^-$ = -18V; $V^+$ = 0.5V to 18V<br>$V^+$ = 18V; $V^-$ = -0.5V to -18V | **83** | 130 | - | dB |
| Open-Loop Gain | $A_{VOL}$ | $R_L$ = 10kΩ to ground | **90** | 130 | - | dB |
| Output Voltage High ($V_{OUT}$ to $V^+$) | $V_{OH}$ | $R_L$ = No load | - | 25 | **160** | mV |
| | | $R_L$ = 10kΩ | - | 75 | **175** | mV |
| Output Voltage Low ($V_{OUT}$ to $V^-$) | $V_{OL}$ | $R_L$ = No load | - | 22 | **160** | mV |
| | | $R_L$ = 10kΩ | - | 65 | **175** | mV |
| Output Short-Circuit Current | $I_{SRC}$ | Sourcing; $V_{IN}$ = 0V, $V_{OUT}$ = -18V | **10** | 56 | - | mA |
| Output Short-Circuit Current | $I_{SNK}$ | Sinking; $V_{IN}$ = 0V, $V_{OUT}$ = +18V | **10** | 56 | - | mA |
| Supply Current/Amplifier | $I_S$ | Unity gain | - | 1.5 | **2.8** | mA |
| **AC Specifications** | | | | | | |
| Gain-Bandwidth Product | GBW | $A_{CL}$ = 101, $R_L$ = 10k | - | 19 | - | MHz |
| Voltage Noise Density | $e_n$ | f = 10kHz | - | 11.3 | - | nV/√Hz |
| Current Noise Density | $i_n$ | f = 10kHz | - | 0.312 | - | pA/√Hz |
| Large Signal Slew Rate | SR | $A_V$ = 1, $R_L$ = 10kΩ, $V_O$ = $10V_{P-P}$ | **60** | 180 | - | V/µs |

### 2.4.2 $V_S$ = ±2.5V

$V_{CM}$ = $V_O$ = 0V, $R_L$ = Open, $T_A$ = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C**.

| Description | Parameter | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = 0V | -400 | 100 | 400 | µV |
| | | $V_{CM}$ = $V^+$ to $V^-$ | **500** | 130 | **500** | µV |
| Offset Voltage Temperature Coefficient | $TCV_{OS}$ | $V_{CM}$ = $V^+$ - 2V to $V^-$ + 2V | - | 0.5 | - | µV/°C |
| Input Offset Channel-to-Channel Match | $\Delta V_{OS}$ | $V_{CM}$ = $V^+$ | **-800** | 150 | **800** | µV |
| | | $V_{CM}$ = $V^-$ | **-800** | 180 | **800** | µV |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0V | - | 211 | **400** | nA |
| | | $V_{CM}$ = $V^+$ | - | 157 | **400** | nA |
| | | $V_{CM}$ = $V^-$ | - | 235 | **580** | nA |
| | | $V_{CM}$ = $V^+$ - 0.5V | - | 157 | **400** | nA |
| | | $V_{CM}$ = $V^-$ + 0.5V | - | 235 | **580** | nA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = $V^+$ to $V^-$ | -30 | 3 | 30 | nA |
| | | | **-50** | - | **50** | nA |
| Common-Mode Input Voltage Range | $V_{CMIR}$ | | **V-** | - | **V+** | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM}$ = $V^-$ to $V^+$ | **70** | 95 | - | dB |
| | | $V_{CM}$ = $V^+$ - 0.5V to $V^-$ + 0.5V | **74** | 93 | - | dB |
| Power Supply Rejection Ratio | PSRR | $V^-$ = -2.5V; $V^+$ = 0.5V to 2.5V<br>$V^+$ = 2.5V; $V^-$ = -0.5V to -2.5V<br>$T_A$=25°C, 125°C | **80** | 125 | - | dB |
| | | $V^-$ = -2.5V; $V^+$ = 0.5V to 2.5V<br>$V^+$ = 2.5V; $V^-$ = -0.5V to -2.5V<br>$T_A$=-55°C | **70** | 97 | - | dB |
| Open-Loop Gain | $A_{VOL}$ | $R_L$ = 10kΩ to ground | **90** | 120 | - | dB |
| Output Voltage High ($V_{OUT}$ to $V^+$) | $V_{OH}$ | $R_L$ = No load | - | 14 | **85** | mV |
| | | $R_L$ = 10kΩ | - | 23 | **105** | mV |
| | | $R_L$ = 600Ω | - | 230 | **400** | mV |
| Output Voltage Low ($V_{OUT}$ to $V^-$) | $V_{OL}$ | $R_L$ = No load | - | 10 | **85** | mV |
| | | $R_L$ = 10kΩ | - | 18 | **105** | mV |
| | | $R_L$ = 600Ω | - | 200 | **400** | mV |
| Supply Current/Amplifier | $I_S$ | Unity gain | - | 1.1 | **2.0** | mA |
| **AC Specifications** | | | | | | |
| Gain-Bandwidth Product | GBW | $A_{CL}$ = 101, $R_L$ = 10k | - | 17 | - | MHz |
| Voltage Noise Density | $e_n$ | f = 10kHz | - | 12.3 | - | nV/√Hz |
| Current Noise Density | $i_n$ | f = 10kHz | - | 0.313 | - | pA/√Hz |
| Large Signal Slew Rate | SR | $A_V$ = 1, $R_L$ = 10kΩ, $V_O$ = $3V_{P-P}$ | - | 60 | - | V/µs |

### 2.4.3 $V_S$ = ±1.5V

$V_{CM}$ = $V_O$ = 0V, $R_L$ = Open, $T_A$ = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C**.

| DESCRIPTION | PARAMETER | TEST CONDITIONS | MIN (Note 6) | TYP | MAX (Note 6) | UNIT |
|---|---|---|---|---|---|---|
| Offset Voltage | $V_{OS}$ | $V_{CM}$ = 0V | -400 | 100 | 400 | µV |
| | | $V_{CM}$ = $V^+$ to $V^-$ | **-500** | 130 | **500** | µV |
| Input Offset Channel-to-Channel Match | $\Delta V_{OS}$ | $V_{CM}$ = $V^+$ | **-800** | 150 | **800** | µV |
| | | $V_{CM}$ = $V^-$ | **-800** | 180 | **800** | µV |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0V | - | 176 | **375** | nA |
| | | $V_{CM}$ = $V^+$ | - | 155 | **375** | nA |
| | | $V_{CM}$ = $V^-$ | - | 232 | **565** | nA |
| | | $V_{CM}$ = $V^+$ - 0.5V | - | 155 | **375** | nA |
| | | $V_{CM}$ = $V^-$ + 0.5V | - | 232 | **565** | nA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = $V^+$ to $V^-$ | -30 | 3 | 30 | nA |
| | | | **-50** | - | **50** | nA |
| Common-Mode Input Voltage Range | $V_{CMIR}$ | | **V-** | | **V+** | V |
| Output Voltage High ($V_{OUT}$ to $V^+$) | $V_{OH}$ | $R_L$ = No load | - | 19 | **50** | mV |
| | | $R_L$ = 10kΩ | - | 19 | **70** | mV |
| Output Voltage Low ($V_{OUT}$ to $V^-$) | $V_{OL}$ | $R_L$ = No load | - | 14 | **50** | mV |
| | | $R_L$ = 10kΩ | - | 14 | **70** | mV |
| Supply Current/Amplifier | $I_S$ | Unity Gain | - | 1.1 | **2.0** | mA |
| **AC Specifications** | | | | | | |
| Gain-Bandwidth Product | GBW | $A_{CL}$ = 101, $R_L$ = 10k | - | 16 | - | MHz |
| Voltage Noise Density | $e_n$ | f = 10kHz | - | 12 | - | nV/√Hz |
| Current Noise Density | $i_n$ | f = 10kHz | - | 0.312 | - | pA/√Hz |

Note:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

# 3. Typical Performance Curves

Unless otherwise specified, $V_S$ ± 18V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C.

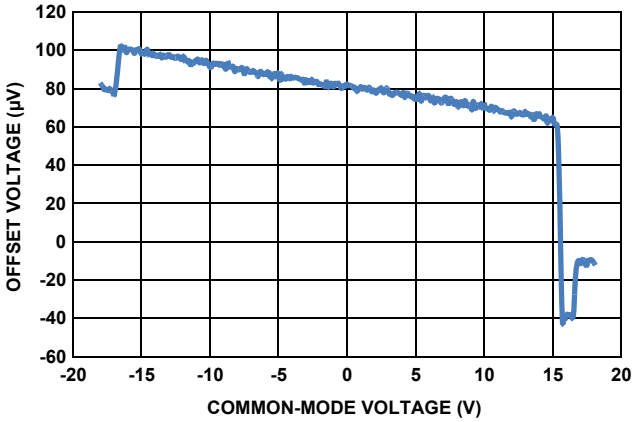



**Figure 1. Offset Voltage vs Common-Mode Voltage**

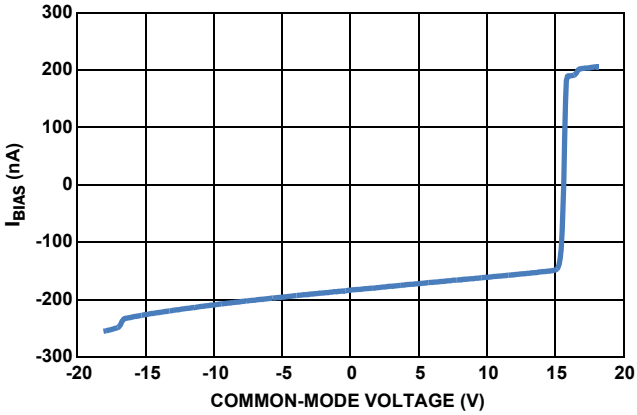



**Figure 2. $I_{BIAS}$ vs Common-Mode Voltage**

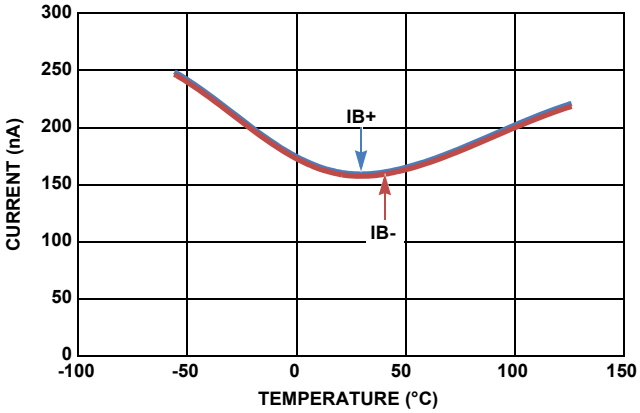



**Figure 3. $I_{BIAS}$ vs Temperature ($V_S$ = ±18V)**

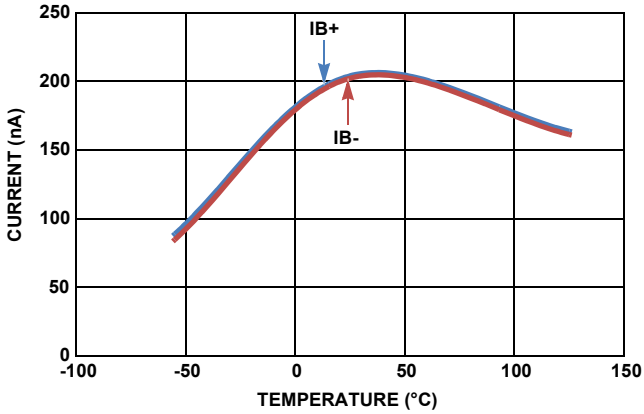



**Figure 4. $I_{BIAS}$ vs Temperature ($V_S$ = ±2.5V)**

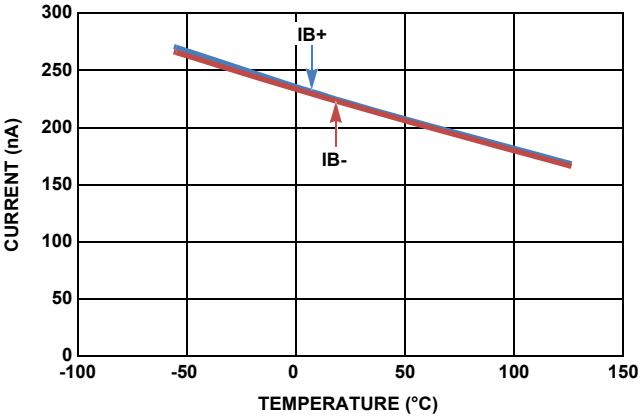



**Figure 5. $I_{BIAS}$ vs Temperature ($V_S$ = ±1.5V)**

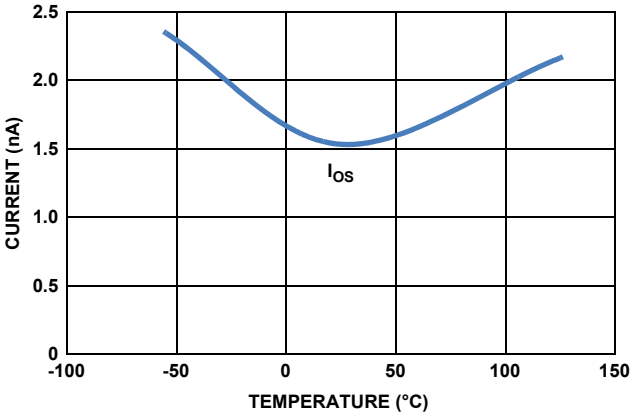



**Figure 6. $I_{OS}$ vs Temperature ($V_S$ = ±18V)**

Unless otherwise specified, $V_S$ ± 18V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C. **(Continued)**

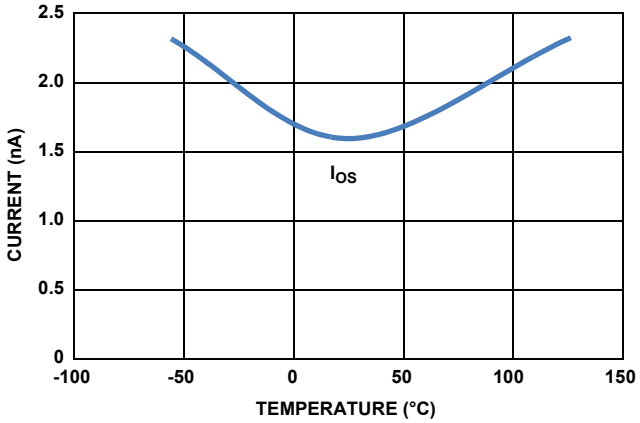



**Figure 7. $I_{OS}$ vs Temperature ($V_S$ = ±2.5V)**

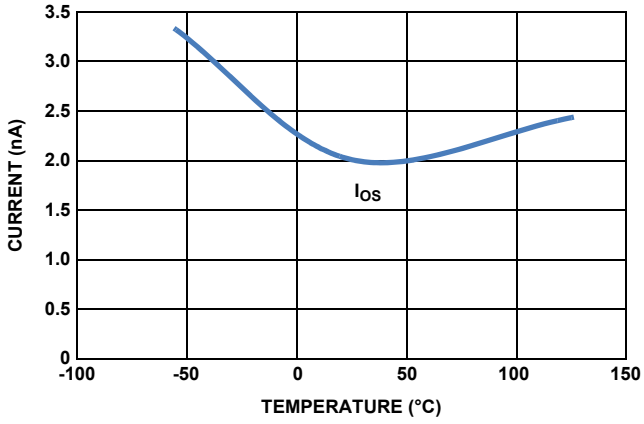



**Figure 8. $I_{OS}$ vs Temperature ($V_S$ = ±1.5V)**

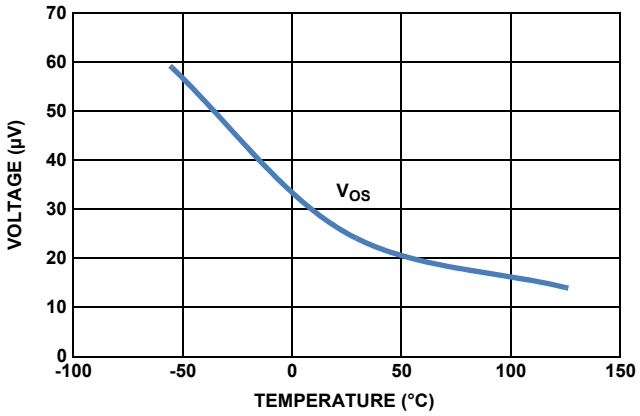



**Figure 9. $V_{OS}$ vs Temperature ($V_S$ = ±18V)**

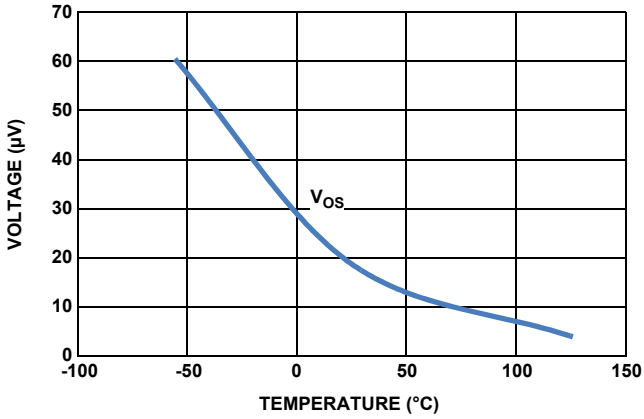



**Figure 10. $V_{OS}$ vs Temperature ($V_S$ = ±2.5V)**

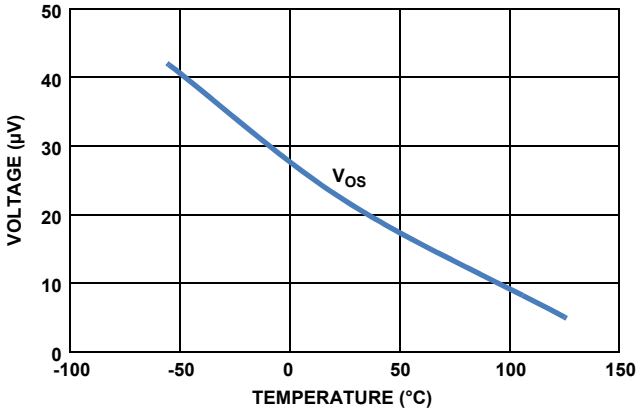



**Figure 11. $V_{OS}$ vs Temperature ($V_S$ = ±1.5V)**

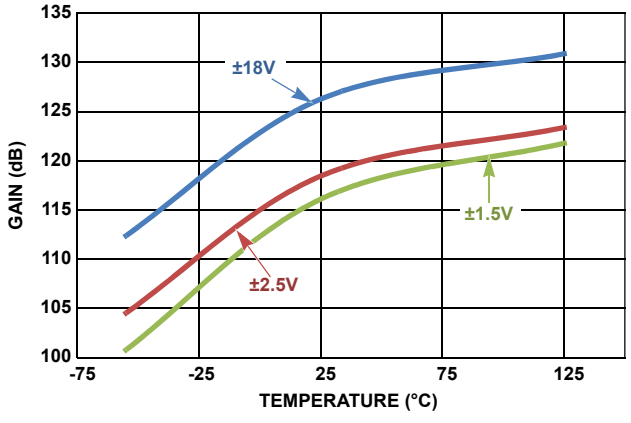



**Figure 12. $A_{VOL}$ vs Temperature vs Supply Voltage**

Unless otherwise specified, $V_S$ ± 18V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C. **(Continued)**

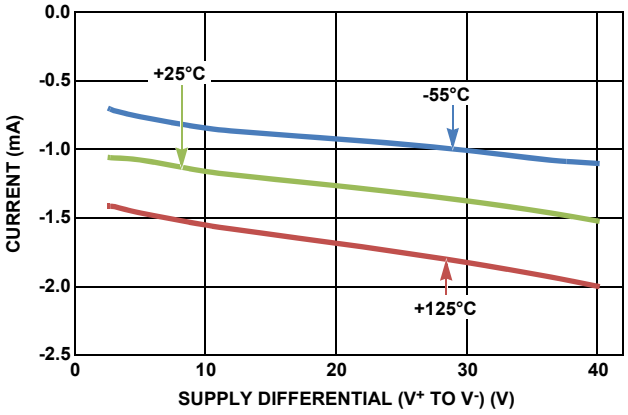



**Figure 13. Negative Supply Current vs Supply Voltage**

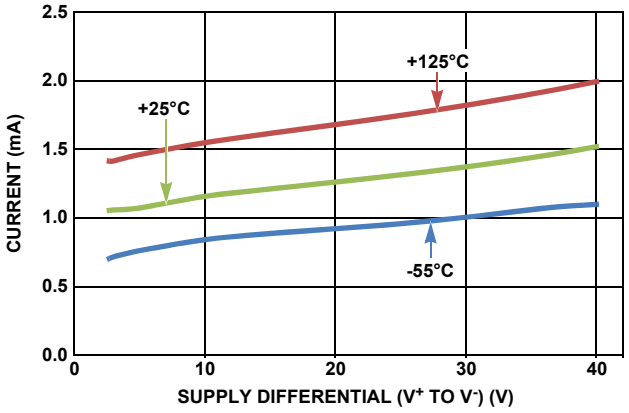



**Figure 14. Positive Supply Current vs Supply Voltage**

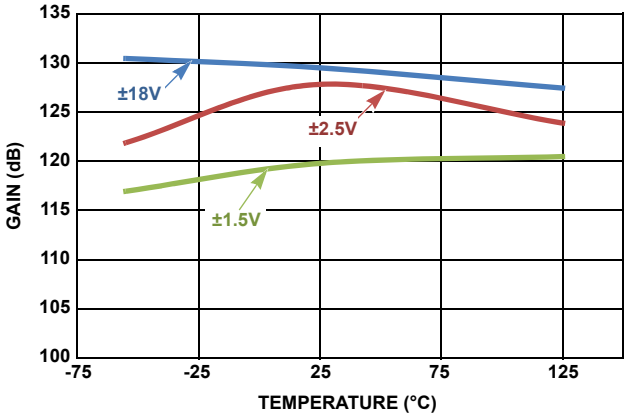



**Figure 15. PSRR+ vs Temperature vs Supply Voltage**

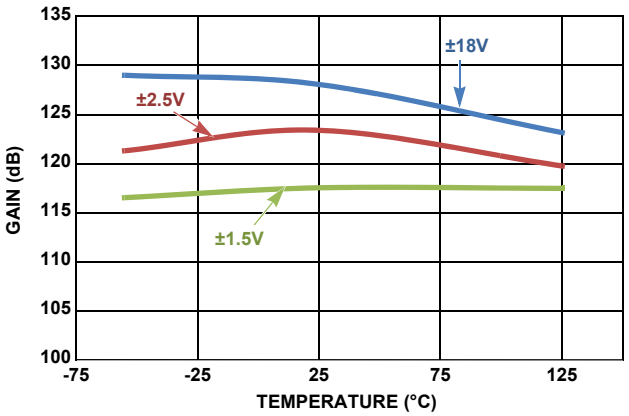



**Figure 16. PSRR- vs Temperature vs Supply Voltage**

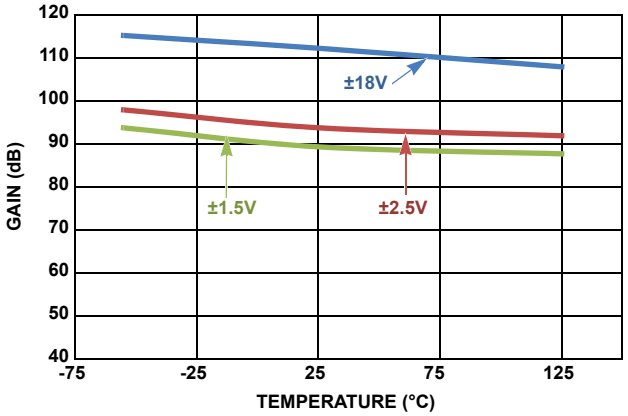



**Figure 17. CMRR vs Temperature vs Supply Voltage**

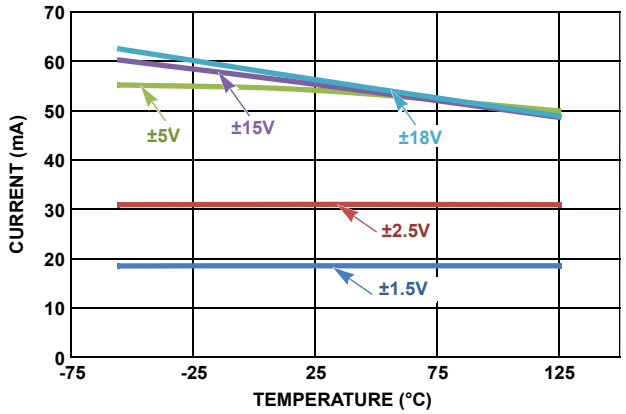



**Figure 18. Short-Circuit Current vs Temperature**

Unless otherwise specified, $V_S$ ± 18V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C. **(Continued)**

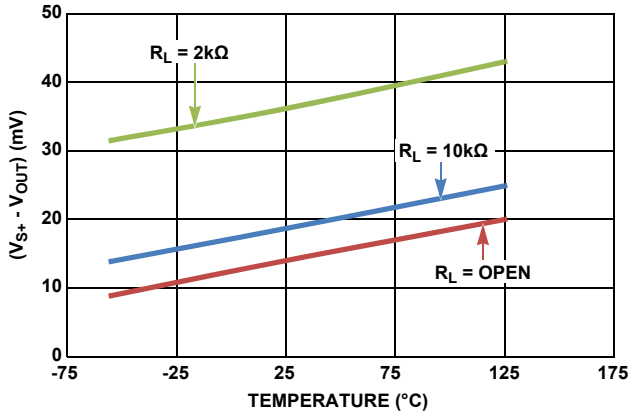



**Figure 19. ($V_S$ = ±1.5V) $V_{OH}$ vs Temperature**

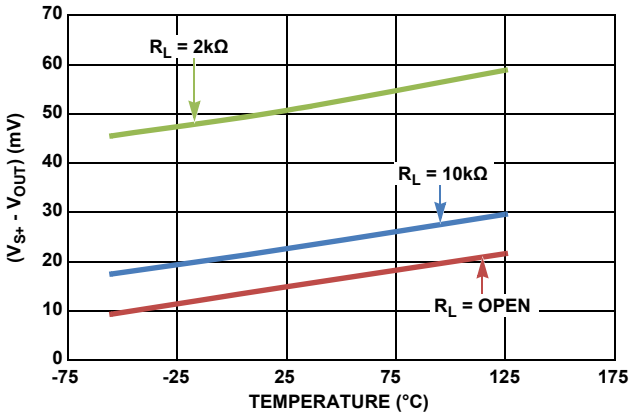



**Figure 20. ($V_S$ = ±2.5V) $V_{OH}$ vs Temperature**

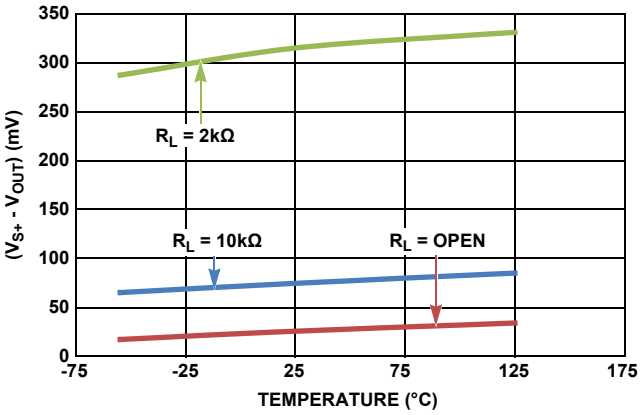



**Figure 21. ($V_S$ = ±18V) $V_{OH}$ vs Temperature**

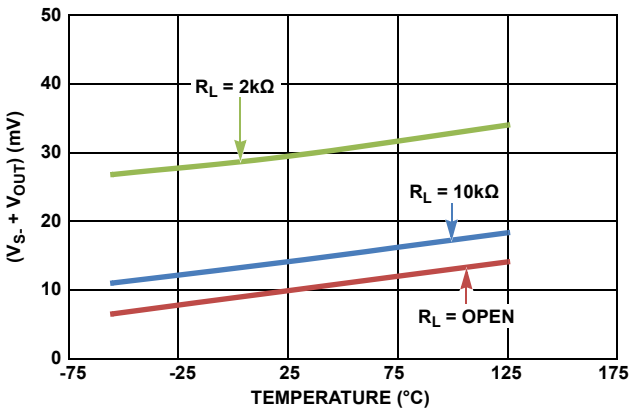



**Figure 22. ($V_S$ = ±1.5V) $V_{OL}$ vs Temperature**

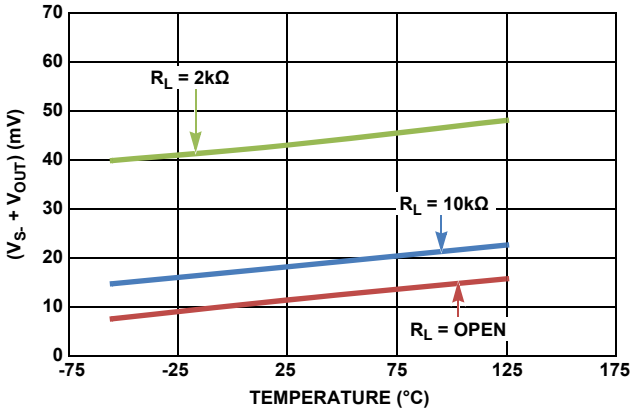



**Figure 23. ($V_S$ = ±2.5V) $V_{OL}$ vs Temperature**

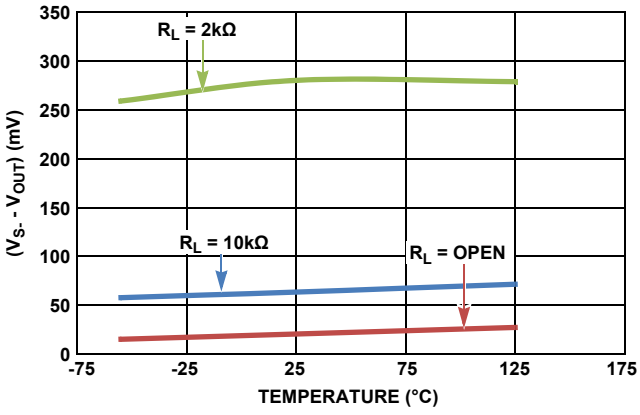



**Figure 24. ($V_S$ = ±18V) $V_{OL}$ vs Temperature**

Unless otherwise specified, $V_S$ ± 18V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C. **(Continued)**

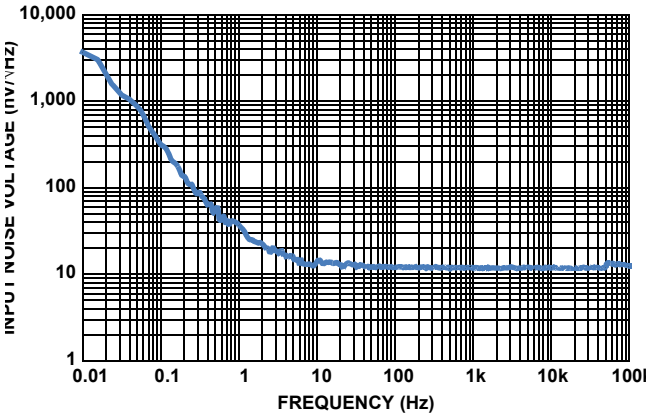



**Figure 25. Input Noise Voltage Spectral Density ($V_S$ = ±18V)**

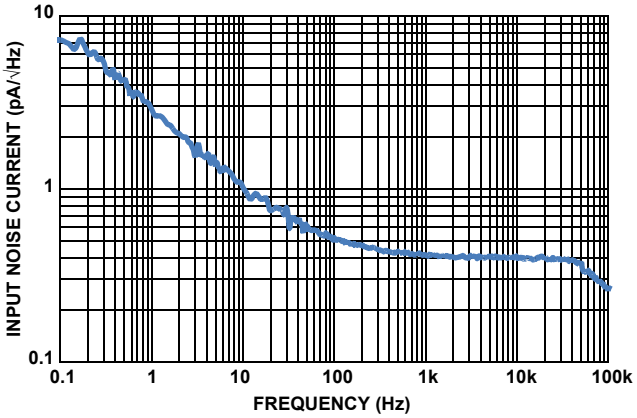



**Figure 26. Input Noise Current Spectral Density ($V_S$ = ±18V)**

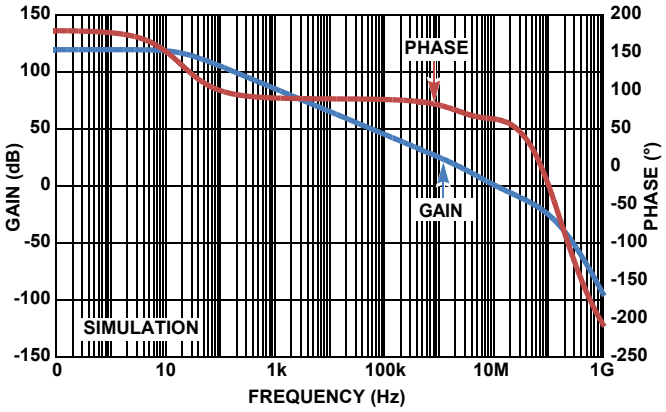



**Figure 27. Open-Loop Frequency Response ($C_L$ = 0.01pF)**

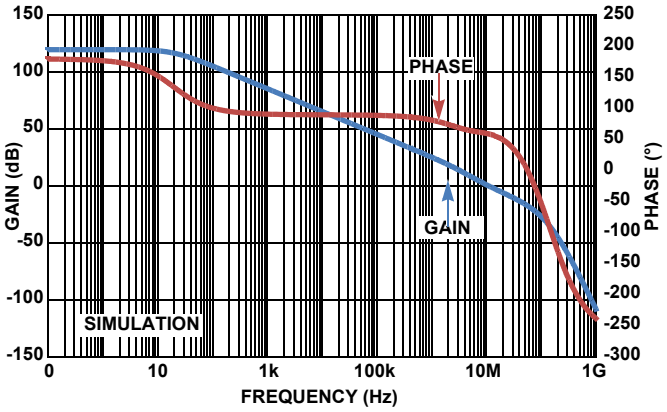



**Figure 28. Open-Loop Frequency Response ($C_L$ = 10pF)**

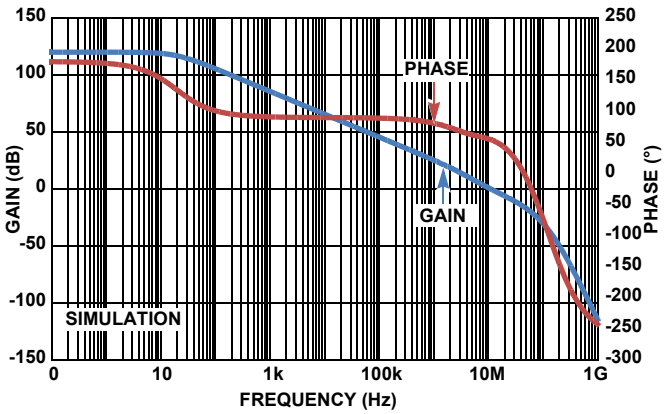



**Figure 29. Open-Loop Frequency Response ($C_L$ = 22pF)**

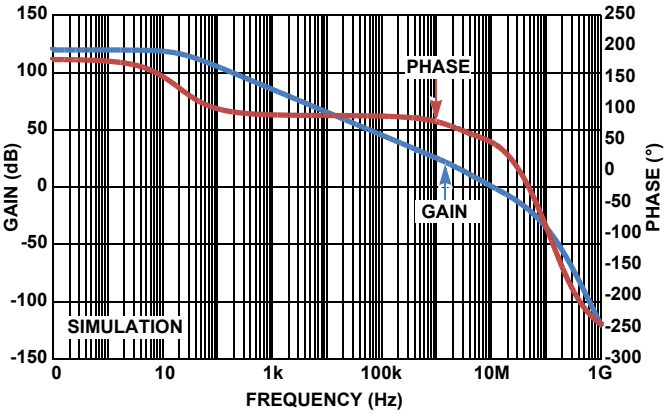



**Figure 30. Open-Loop Frequency Response ($C_L$ = 47pF)**

Unless otherwise specified, $V_S$ ± 18V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C. **(Continued)**

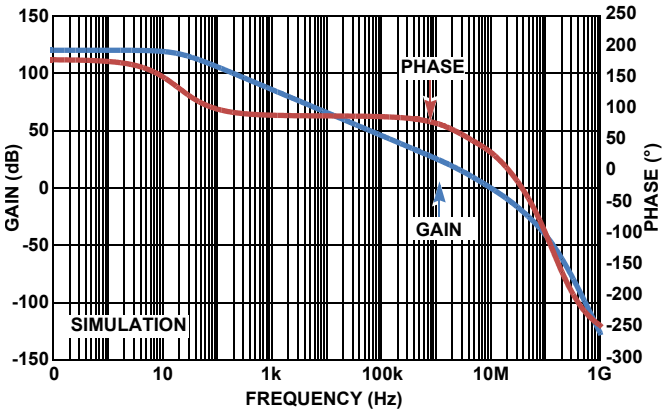



**Figure 31. Open-Loop Frequency Response ($C_L$ = 100pF)**

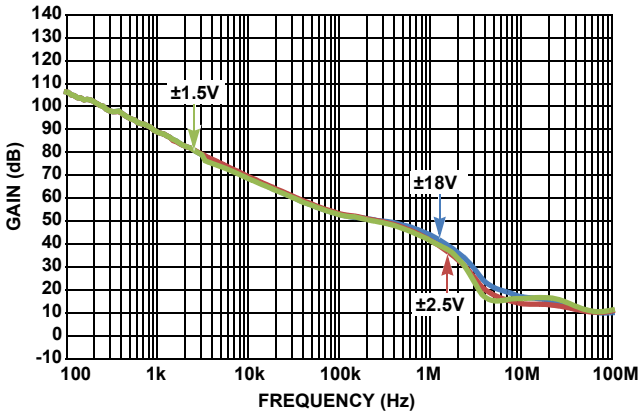



**Figure 32. CMRR vs Frequency**

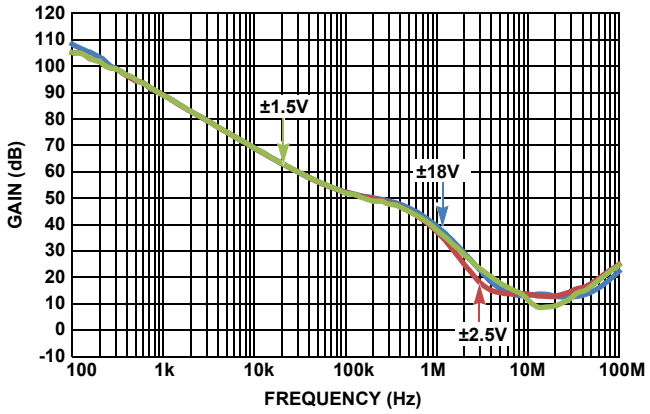



**Figure 33. PSRR vs Frequency**

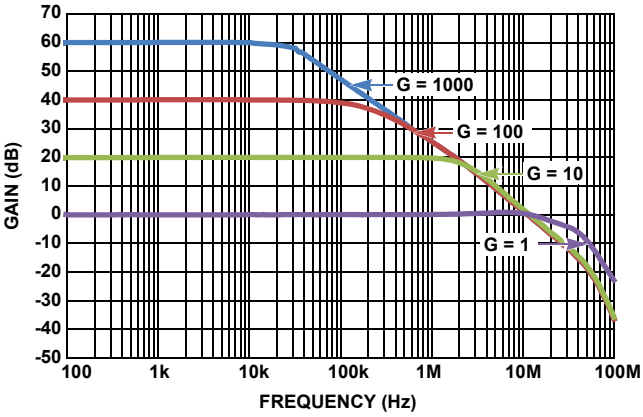



**Figure 34. Frequency Response vs Closed-Loop Gain**

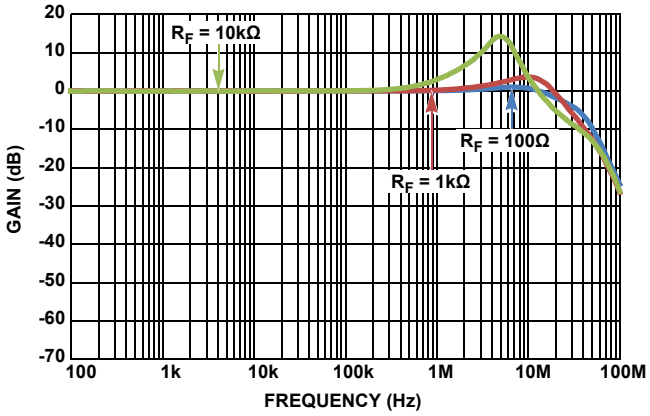



**Figure 35. Frequency Response vs Feedback Resistance ($R_F$)**

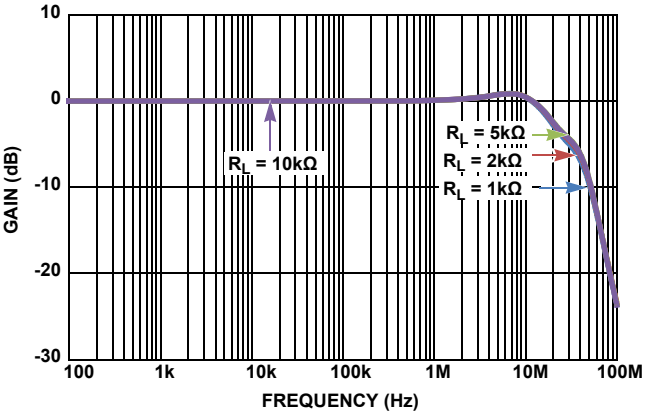



**Figure 36. Frequency Response vs Load Resistance**

Unless otherwise specified, $V_S$ ± 18V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C. **(Continued)**

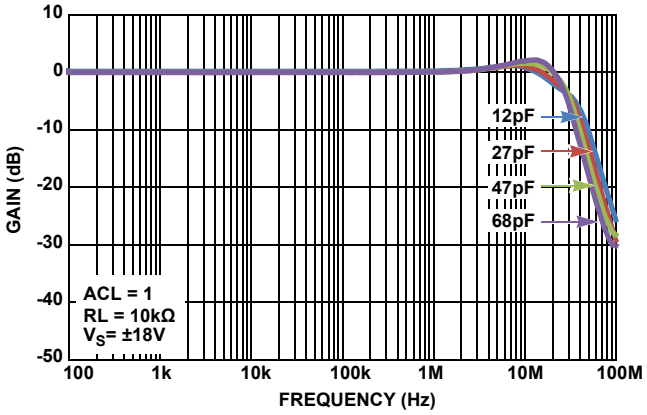



**Figure 37. Unity Gain Response vs Load Capacitance**

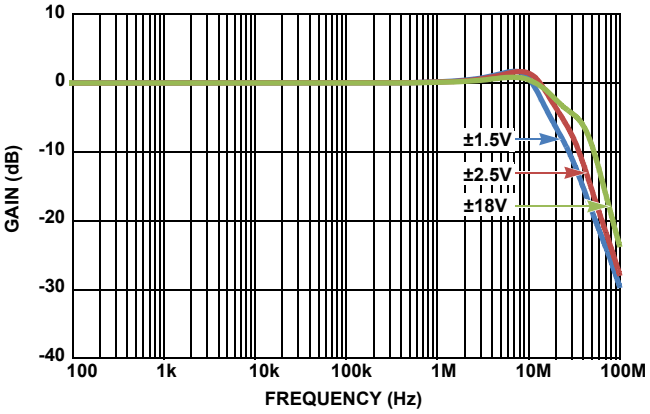



**Figure 38. Frequency Response vs Supply Voltage**

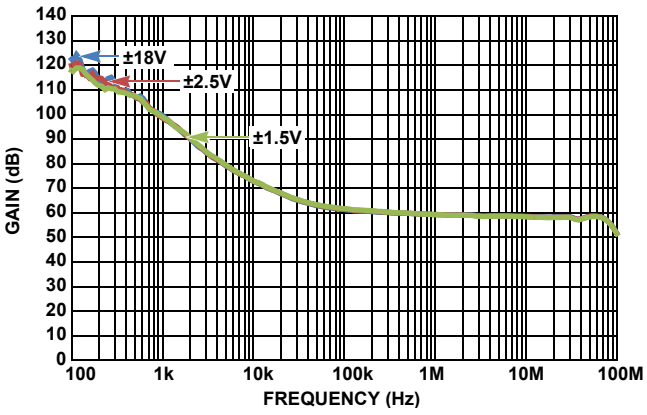



**Figure 39. Crosstalk Rejection**

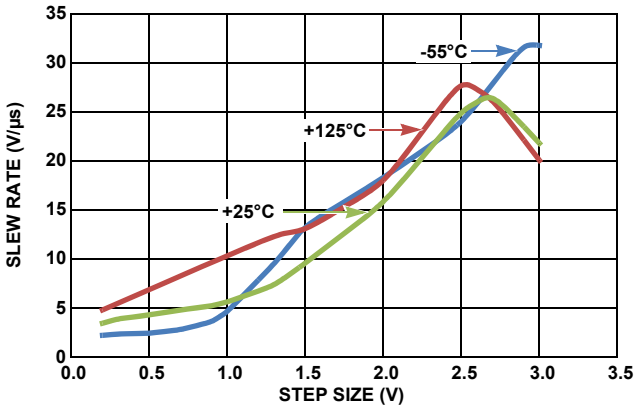



**Figure 40. Slew Rate vs Step Size vs Temperature ($V_S$ = ±1.5V)**

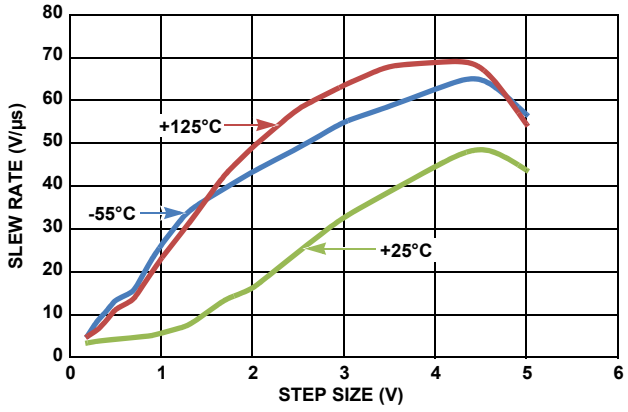



**Figure 41. Slew Rate vs Step Size vs Temperature ($V_S$ = ±2.5V)**

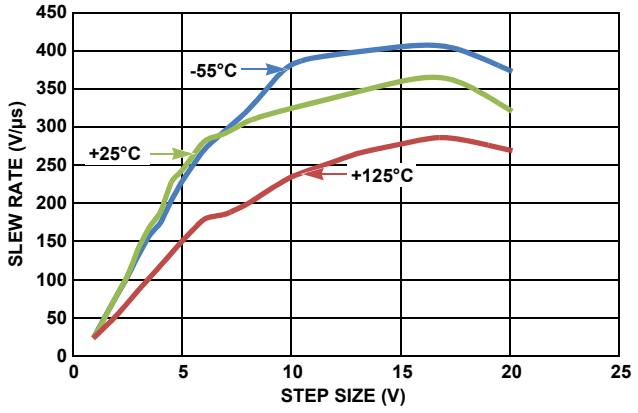



**Figure 42. Slew Rate vs Step Size vs Temperature ($V_S$ = ±18V)**

Unless otherwise specified, $V_S$ ± 18V, $V_{CM}$ = 0, $V_O$ = 0V, $T_A$ = +25°C. **(Continued)**

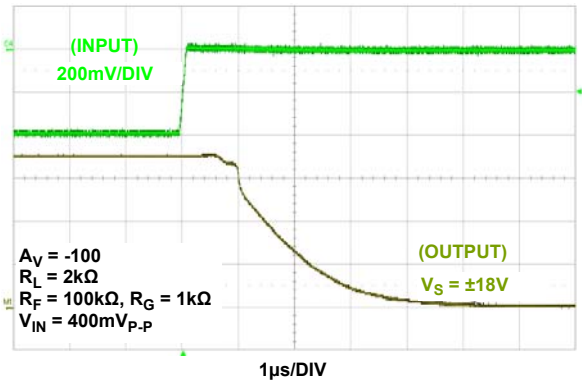



**Figure 43. Saturation Recovery ($V_S$ = ±18V)**

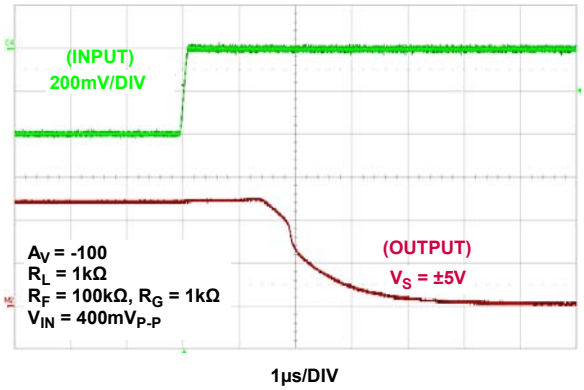



**Figure 44. Saturation Recovery ($V_S$ = ±5V)**

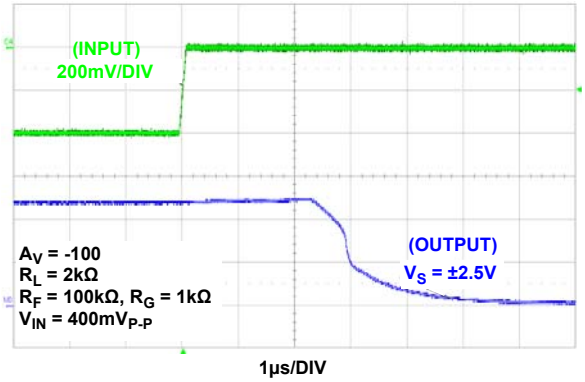



**Figure 45. Saturation Recovery ($V_S$ = ±2.5V)**

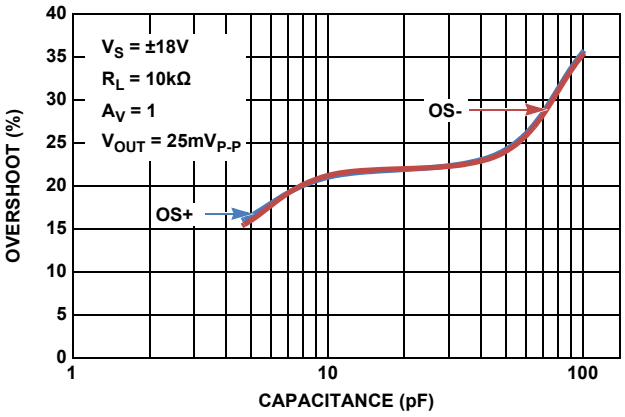



**Figure 46. Overshoot (%) vs Load Capacitance**

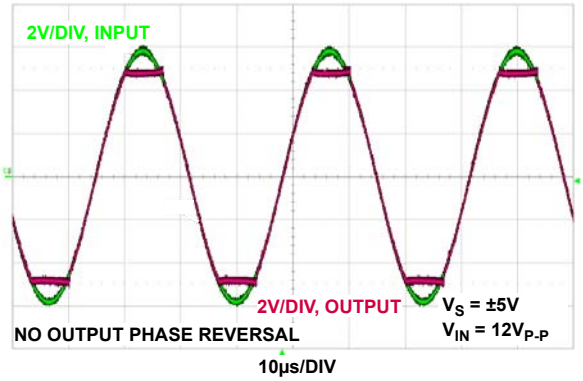



**Figure 47. Input Overdrive Response**

# 4. Applications Information

## 4.1 Functional Description

The ISL71444M contains four high-speed and low-power op amps designed to take advantage of its full dynamic input and output voltage range with rail-to-rail operation. By offering low power, low offset voltage, and low temperature drift coupled with its high bandwidth and enhanced slew rates upwards of 50V/µs, these op amps are ideal for applications requiring both high DC accuracy and AC performance. The ISL71444M is manufactured in Intersil's PR40 silicon-on-insulator process, which makes this device immune to single event latch-up and provides excellent radiation tolerance. This makes it the ideal choice for high reliability applications in harsh radiation-prone environments.

## 4.2 Operating Voltage Range

This device is designed to operate with a split supply rail from ±1.35V to ±20V or a single supply rail from 2.7V to 40V. The ISL71444M is fully characterized in production for supply rails of 5V (±2.5V) and 36V (±18V). The power supply rejection ratio is typically 120dB over the full operating voltage range. The worst case common-mode rejection ratio across temperature is within 1.5V to 2V of each rail. When VCM is inside that range, the CMRR performance is typically >110dB with a ±18V supply. The minimum CMRR performance across the -55°C to +125°C temperature range and radiation is >70dB over the full common-mode input range for power supply voltages from ±2.5V (5V) to ±18V (36V).

## 4.3 Input Performance

The slew enhanced front-end is a block that is placed in parallel with the main input stage and functions based on the input differential.

## 4.4 Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series-connected 600Ω current limiting resistors, and an anti-parallel diode pair across the inputs.

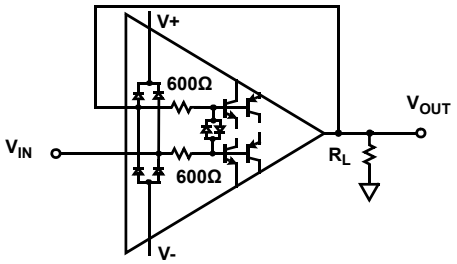



**Figure 48. Input ESD Diode Current Limiting, Unity Gain**

## 4.5 Output Short-Circuit Current Limiting

The output current limit has a worst case minimum limit of ±8mA but may reach as high as ±100mA. The op amp can withstand a short-circuit to either rail for a short duration (<1s) as long as the maximum operating junction temperature is not violated. This applies to only one amplifier at a given time. Continued use of the device in these conditions may degrade the long-term reliability of the part and is not recommended. Figure 18 on page 10 shows the typical short-circuit currents that can be expected. The ISL71444M's current limiting circuitry will automatically lower the current limit of the device if short-circuit conditions carry on for extended periods of times. This protects the device from malfunction, however, extended operation in this mode will degrade the output rail-to-rail performance by increasing the $V_{OH}/V_{OL}$ levels.

## 4.6 Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL71444M is immune to output phase reversal, even when the input voltage is 1V beyond the supplies. This is illustrated in Figure 47 on page 15.

## 4.7 Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature ($T_{JMAX}$) for all applications to determine if power supply voltages or load conditions need to be modified to remain in the safe operating area. These parameters are related using (EQ. 1):

$$T_{JMAX} = T_{AMAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package ($PD_{MAX}$)
- $PD_{MAX}$ for each amplifier can be calculated using (EQ. 2):

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- $T_{AMAX}$ = Maximum ambient temperature
- $\theta_{JA}$ = Thermal resistance of the package
- $PD_{MAX}$ = Maximum power dissipation of 1 amplifier
- $V_S$ = Total supply voltage
- $I_{qMAX}$ = Maximum quiescent supply current of 1 amplifier
- $V_{OUTMAX}$ = Maximum output voltage swing of the application

## 4.8 Unused Channel Configuration

The ISL71444M is a quad op amp. If the application does not require the use of all four op amps, the user must configure the unused channels to prevent them from oscillating. Any unused channels will oscillate if the input and output pins are floating. This results in higher than expected supply currents and possible noise injection into any of the active channels being used. The proper way to prevent oscillation is to short the output to the inverting input and ground the positive input (Figure 49).

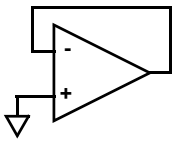



**Figure 49. Preventing Oscillations in Unused Channels**

# 5. Radiation Tolerance

The ISL71444M is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects, and Single Event Effects (SEE) has been measured, characterized, and reported in the proceeding sections. However, TID performance is not guaranteed through radiation acceptance testing nor is the characterized SEE characterized performance guaranteed.

## 5.1 Total Ionizing Dose (TID) Testing

### 5.1.1 Introduction

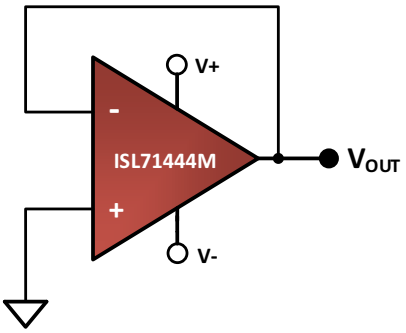
Total dose testing of the ISL71444MVZ-T proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 18 samples irradiated under bias, as shown in Table 1 on page 19, and 18 samples irradiated with all pins grounded (unbiased). Three control units were used. The bias configuration is shown in Figure 50.

Samples of the ISL71444MVZ-T were drawn from fabrication lot X7J8AB and were packaged in the production 14 Ld plastic TSSOP, Package Outline Drawing (POD) M14.173. The samples were screened to datasheet limits at room temperature only, before irradiation.

Total dose irradiations were performed using a Hopewell Designs N40 panoramic vault-type low dose rate 60Co irradiator located in the Intersil Palm Bay, Florida facility. The dose rate was 0.0089 rad(Si)/s (8.9 mrad(Si)/s). PbAl spectrum hardening filters were used to shield the test board and devices under test against low energy secondary gamma radiation.

Down-points for the testing were 0 krad(Si), 10 krad(Si), 20 krad(Si), and 30 krad(Si). Following irradiation, the samples were subjected to a high temperature biased anneal for 168 hours at +100°C.

All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each down-point. All down-point electrical testing was performed at room temperature.




**Notes:**
**V+ = +18V, V- = -18V**

**Figure 50. Irradiation Bias Configuration for the IS71444M**

### 5.1.2 Results

Table 1 summarizes the attributes data. Note, “Bin 1” indicates a device that passes all data sheet specification limits.

**Table 1. ISL71444M Total Dose Test Attributes Data**

| Dose Rate (mrad(Si)/s) | Bias | Sample Size | Down Point | Bin 1 | Rejects |
|---|---|---|---|---|---|
| 8.75 | Figure 50 | 18 | Pre-rad | 18 | |
| | | | 10krad(Si) | 18 | 0 |
| | | | 20krad(Si) | 18 | 0 |
| | | | 30krad(Si) | 18 | 0 |
| | | | Anneal | 18 | 0 |
| 8.75 | Grounded | 18 | Pre-rad | 18 | |
| | | | 10krad(Si) | 18 | 0 |
| | | | 20krad(Si) | 18 | 0 |
| | | | 30krad(Si) | 18 | 0 |
| | | | Anneal | 18 | 0 |

The plots in Figure 51 through 55 show data for key parameters at all down points. The plots show the average as a function of total dose for each of the irradiation conditions; we chose to use the average because of the relatively large sample sizes. All parts showed excellent stability over irradiation.

Table 2 on page 20 show the average of other key parameters with respect to total dose in tabular form.

### 5.1.3 Conclusion

As shown in Table 2, and the selected graphs (Figures 51 through 55), all parameters showed excellent stability over irradiation, with no observed bias sensitivity. Although, for brevity, only the ±18V results are shown; the ±2.5V and ±1.5V results were just as stable.

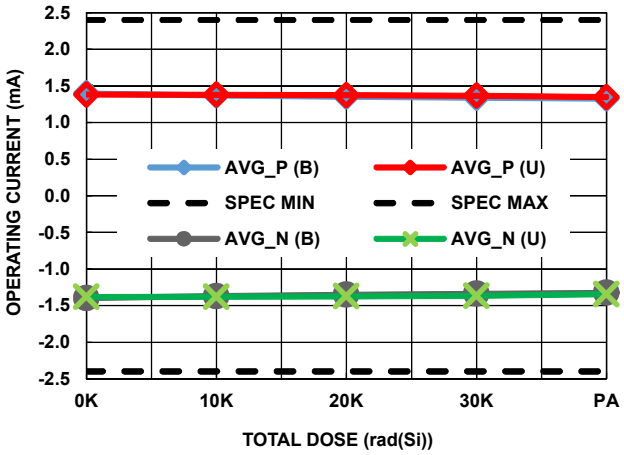



**Figure 51. Operating Supply Current vs TID $V_S$ = ±18V**

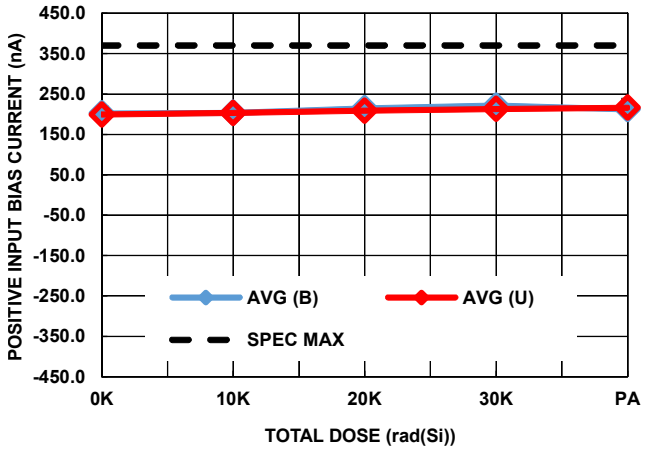



**Figure 52. Positive Input Bias Current vs TID ($V_S$ = ±18V)**

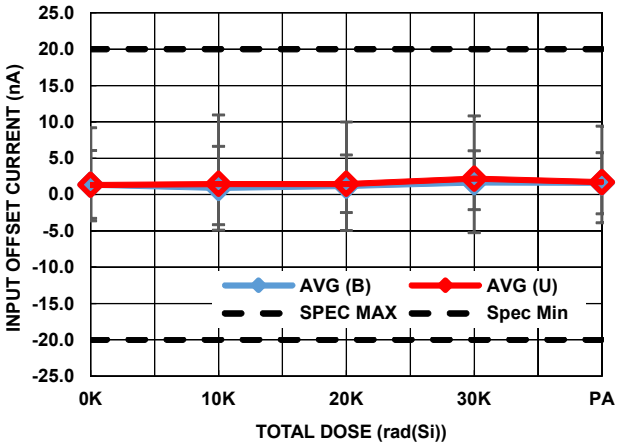



Figure 53. Input Offset Current vs TID (Vs = ±18V)

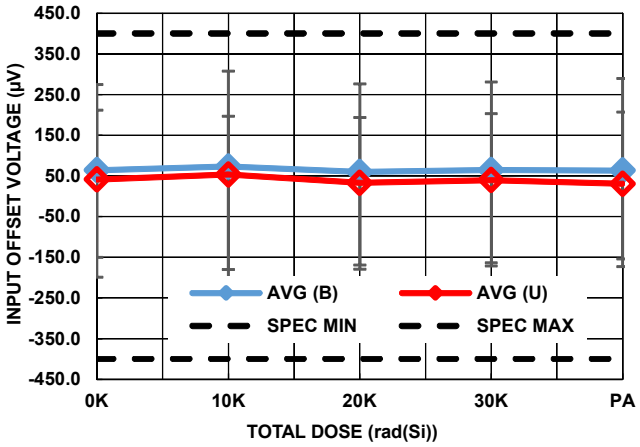



Figure 54. Input Offset Voltage vs TID (Vs = ±18V)

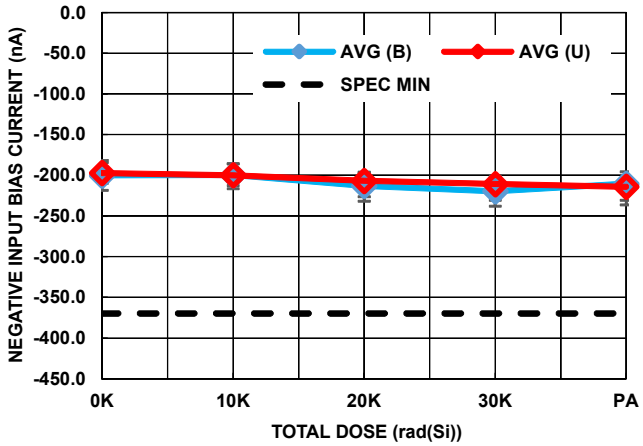



Figure 55. Negative Input Bias Current vs TID (Vs = ±18V)

Table 2. ISL71444M Response of Key Parameters vs. TID ($V_S$ = ±18V)

| Parameter | Condition | Bias | 0krad(Si) | 10krad(Si) | 20krad(Si) | 30krad(Si) | Post Anneal | Units |
|---|---|---|---|---|---|---|---|---|
| Quad Power Supply Current (Positive) $V_S$ = ±18.0V | $I_{S+}$ | Avg (Biased) | 1.40 | 1.38 | 1.35 | 1.35 | 1.33 | mA |
| | | Avg (Unbiased) | 1.38 | 1.38 | 1.38 | 1.38 | 1.35 | |
| | | Limit - | - | - | - | - | - | |
| | | Limit + | 11 | 11 | 11 | 11 | 11 | |
| Quad Power Supply Current (Negative) $V_S$ = ±18.0V | $I_{S-}$ | Avg (Biased) | -1.40 | -1.38 | -1.35 | -1.35 | -1.33 | mA |
| | | Avg (Unbiased) | -1.38 | -1.38 | -1.38 | -1.38 | -1.35 | |
| | | Limit - | -11 | -11 | -11 | -11 | -11 | |
| | | Limit + | - | - | - | - | - | |

**Table 2. ISL71444M Response of Key Parameters vs. TID ($V_S$ = ±18V) (Continued)**

| Parameter | Condition | Bias | 0krad(Si) | 10krad(Si) | 20krad(Si) | 30krad(Si) | Post Anneal | Units |
|---|---|---|---|---|---|---|---|---|
| Power Supply Current/Amplifier (Positive) $V_S$ = ±18.0V | $I_{S+}$ | Avg (Biased) | 1.40 | 1.37 | 1.35 | 1.34 | 1.33 | mA |
| | | Avg (Unbiased) | 1.38 | 1.38 | 1.37 | 1.37 | 1.35 | |
| | | Limit - | - | - | - | - | - | |
| | | Limit + | 2.40 | 2.40 | 2.40 | 2.40 | 2.40 | |
| Power Supply Current/Amplifier (Negative) $V_S$ = ±18.0V | $I_{S-}$ | Avg (Biased) | -1.40 | -1.37 | -1.35 | -1.34 | -1.33 | mA |
| | | Avg (Unbiased) | -1.38 | -1.38 | -1.37 | -1.37 | -1.35 | |
| | | Limit - | -2.40 | -2.40 | -2.40 | -2.40 | -2.40 | |
| | | Limit + | - | - | - | - | - | |
| Input Offset Voltage $V_S$ = ±18.0V $V_{CM}$ = 0V | $V_{OS}$ | Avg (Biased) | 64.25 | 73.07 | 59.85 | 64.56 | 63.30 | µV |
| | | Avg (Unbiased) | 54.14 | 69.28 | 62.96 | 68.76 | 63.93 | |
| | | Limit - | -400.00 | -400.00 | -400.00 | -400.00 | -400.00 | |
| | | Limit + | 400.00 | 400.00 | 400.00 | 400.00 | 400.00 | |
| Positive Input Bias Current $V_S$ = ±18.0V $V_{CM}$ = 0V | $I_{B+}$ | Avg (Biased) | 201.94 | 203.47 | 214.55 | 221.37 | 212.41 | nA |
| | | Avg (Unbiased) | 199.06 | 203.03 | 208.65 | 213.11 | 216.28 | |
| | | Limit - | - | - | - | - | - | |
| | | Limit + | 370.00 | 370.00 | 370.00 | 370.00 | 370.00 | |
| Negative Input Bias Current $V_S$ = ±18.0V $V_{CM}$ = 0V | $I_{B-}$ | Avg (Biased) | -200.23 | -199.89 | -213.05 | -219.70 | -210.44 | nA |
| | | Avg (Unbiased) | -197.37 | -200.14 | -206.89 | -210.92 | -214.22 | |
| | | Limit - | -370.00 | -370.00 | -370.00 | -370.00 | -370.00 | |
| | | Limit + | - | - | - | - | - | |
| Input Offset Current $V_S$ = ±18.0V $V_{CM}$ = 0V | $I_{OS}$ | Avg (Biased) | 1.34 | 0.91 | 1.18 | 1.68 | 1.62 | nA |
| | | Avg (Unbiased) | 1.33 | 1.45 | 1.46 | 2.17 | 1.70 | |
| | | Limit - | -20.00 | -20.00 | -20.00 | -20.00 | -20.00 | |
| | | Limit + | 20.00 | 20.00 | 20.00 | 20.00 | 20.00 | |
| Output Voltage High $V_S$ = ±18.0V $R_L$ = No Load | $V_{OH}$ | Avg (Biased) | 24.32 | 23.98 | 23.76 | 25.42 | 24.10 | mV |
| | | Avg (Unbiased) | 24.16 | 23.98 | 23.97 | 25.76 | 24.29 | |
| | | Limit - | - | - | - | - | - | |
| | | Limit + | 160.00 | 160.00 | 160.00 | 160.00 | 160.00 | |
| Output Voltage Low $V_S$ = ±18.0V $R_L$ = No Load | $V_{OL}$ | Avg (Biased) | 21.45 | 21.00 | 20.50 | 19.86 | 20.24 | mV |
| | | Avg (Unbiased) | 21.44 | 20.70 | 20.40 | 19.86 | 20.43 | |
| | | Limit - | - | - | - | - | - | |
| | | Limit + | 160.00 | 160.00 | 160.00 | 160.00 | 160.00 | |
| Open Loop Gain (Positive) $V_S$ = ±18.0V $R_L$ = 10kΩ | $A_{VOL+}$ | Avg (Biased) | 126.75 | 123.87 | 125.94 | 125.16 | 124.89 | dB |
| | | Avg (Unbiased) | 126.84 | 125.41 | 126.31 | 125.88 | 125.28 | |
| | | Limit - | 96.00 | 96.00 | 96.00 | 96.00 | 96.00 | |
| | | Limit + | - | - | - | - | - | |
| Open Loop Gain (Negative) $V_S$ = ±18.0V $R_L$ = 10kΩ | $A_{VOL-}$ | Avg (Biased) | 127.71 | 126.21 | 126.98 | 126.18 | 126.15 | dB |
| | | Avg (Unbiased) | 127.74 | 127.43 | 127.45 | 126.89 | 126.44 | |
| | | Limit - | 96.00 | 96.00 | 96.00 | 96.00 | 96.00 | |
| | | Limit + | - | - | - | - | - | |

**Table 2. ISL71444M Response of Key Parameters vs. TID ($V_S$ = ±18V) (Continued)**

| Parameter | Condition | Bias | 0krad(Si) | 10krad(Si) | 20krad(Si) | 30krad(Si) | Post Anneal | Units |
|---|---|---|---|---|---|---|---|---|
| Power Supply Rejection Ratio (Positive) $V_{S+}$ = +18.0V $V_{S-}$ = -0.5V to -18.0V | PSRR+ | Avg (Biased) | 107.45 | 107.91 | 107.44 | 107.36 | 106.78 | dB |
| | | Avg (Unbiased) | 106.97 | 107.15 | 107.04 | 107.23 | 106.13 | |
| | | Limit - | 88.00 | 88.00 | 88.00 | 88.00 | 88.00 | |
| | | Limit + | - | - | - | - | - | |
| Power Supply Rejection Ratio (Negative) $V_{S-}$ = -18.0V $V_{S+}$ = 0.5V to 18.0V | PSRR- | Avg (Biased) | 119.00 | 117.83 | 118.13 | 118.44 | 118.57 | dB |
| | | Avg (Unbiased) | 118.32 | 119.54 | 119.24 | 119.45 | 120.67 | |
| | | Limit - | 88.00 | 88.00 | 88.00 | 88.00 | 88.00 | |
| | | Limit + | - | - | - | - | - | |
| Common Mode Rejection Ratio $V_S$ = ±18.0V $V_{CM}$ = -18.0V to 18.0V | CMRR | Avg (Biased) | 113.56 | 114.96 | 114.37 | 113.84 | 112.61 | dB |
| | | Avg (Unbiased) | 114.19 | 113.75 | 113.81 | 113.81 | 113.23 | |
| | | Limit - | 70.00 | 70.00 | 70.00 | 70.00 | 70.00 | |
| | | Limit + | - | - | - | - | - | |
| Common Mode Rejection Ratio $V_S$ = ±18.0V $V_{CM}$ = -17.5V to 17.5V | CMRR | Avg (Biased) | 113.46 | 114.53 | 114.56 | 113.74 | 112.40 | dB |
| | | Avg (Unbiased) | 114.30 | 113.81 | 114.14 | 113.78 | 113.18 | |
| | | Limit - | 80.00 | 80.00 | 80.00 | 80.00 | 80.00 | |
| | | Limit + | - | - | - | - | - | |
| Large Signal Slew Rate (Rising) $V_S$ = ±18.0V, Gain = 1, $R_L$ = 2kΩ, $V_{OUT}$ = $10V_{P-P}$ | $SR_R$ | Avg (Biased) | 270.93 | 266.86 | 271.30 | 307.91 | 299.42 | V/µs |
| | | Avg (Unbiased) | 267.55 | 263.76 | 268.97 | 307.94 | 295.27 | |
| | | Limit - | 60.00 | 60.00 | 60.00 | 60.00 | 60.00 | |
| | | Limit + | - | - | - | - | - | |
| Large Signal Slew Rate (Falling) $V_S$ = ±18.0V, Gain = 1, $R_L$ = 2kΩ, $V_{OUT}$ = $10V_{P-P}$ | $SR_F$ | Avg (Biased) | 184.24 | 154.23 | 152.27 | 194.45 | 193.17 | V/µs |
| | | Avg (Unbiased) | 182.06 | 151.46 | 155.41 | 196.00 | 194.74 | |
| | | Limit - | 60.00 | 60.00 | 60.00 | 60.00 | 60.00 | |
| | | Limit + | - | - | - | - | - | |

## 5.2 Single Event Effects Testing

### 5.2.1 Introduction

The intense heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. The following is a summary of the SEE testing of the ISL71444M.

### 5.2.2 SEE Test Setup

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 super-conducting cyclotron, which is capable of generating a wide range of test particles with the various energy, flux, and fluence level needed for advanced radiation testing.

The test circuit is a non-inverting configuration with a gain of 10. Digital multimeters were used to monitor the supply voltage (V+/V-), output voltage ($V_{OUT}$), and supply current (I+/I-). The outputs were monitored using four LeCroy 4-channel digital oscilloscopes to capture and store the signal waveforms. Table 3 shows the scope configuration used during the testing.

**Table 3. Oscilloscope Setup for SET Testing**

| Scope | CH 1 | CH 2 | CH 3 | CH 4 | Trigger |
|---|---|---|---|---|---|
| 1 | OUTA | OUTB | OUTC | OUTD | CH1, 1% of OUTA |
| 2 | OUTA | OUTB | OUTC | OUTD | CH2, 1% of OUTB |
| 3 | OUTA | OUTB | OUTC | OUTD | CH3, 1% of OUTC |
| 4 | OUTA | OUTB | OUTC | OUTD | CH4, 1% of OUTD |

### 5.2.3 SEB/SEL Testing Results

A failure due to burnout was indicated by a permanent change to the part's supply current or output voltage after the beam was turned off. If the part's supply current or output voltage reverted back to its pre-exposure value after a power cycle, the event was deemed as latch-up. A failure for burnout was indicated by a ±4% delta (which would allow for measurement repeatability) in supply current or output voltage. The ISL71444M units did not exceed the aforementioned limits with $V_S$ = ±20V at an LET of 43MeV•cm$^2$/mg and therefore are deemed as passing. The output voltage of the amplifiers had a 0% delta pre and post exposure for all channels and all parts and thus are not shown for the sake of brevity.

**Table 4. SEB/SEL Results ($V_S$ = ±20V, LET = 43MeV•cm$^2$/mg)**

| Unit | Temp (°C) | Supply Current Pre-Exposure | | Supply Current Post-Exposure | | SEB/L |
|---|---|---|---|---|---|---|
| | | I+ (mA) | I- (mA) | I+ (mA) | I- (mA) | |
| 1 | +125 | 8.54 | 7.52 | 8.26 | 7.53 | PASS |
| 2 | +125 | 9.18 | 8.44 | 9.15 | 8.41 | PASS |
| 3 | +125 | 8.10 | 7.37 | 8.08 | 7.36 | PASS |
| 4 | +125 | 8.07 | 7.34 | 8.06 | 7.33 | PASS |

### 5.2.4 Single Event Transient Testing

Single Event Transient (SET) testing was conducted in a gain of 10 non-inverting with a 0.1V input with a supply voltage of ±1.35V and an input of 0.2V with supplies at ±15.0V.

The plots in Figure 56 through Figure 57 show the typical SET performance of the ISL71444M at LET = 43MeV•cm$^2$/mg. Fluence was run at 2x10$^6$/cm$^2$.

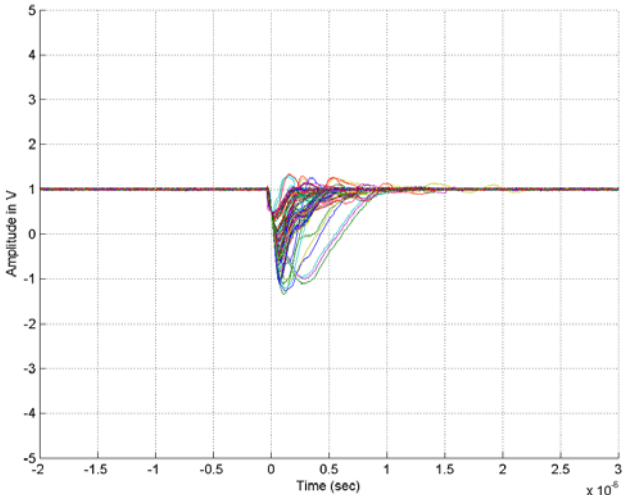



**Figure 56. SET Response with $V_S$ = ±1.35V**

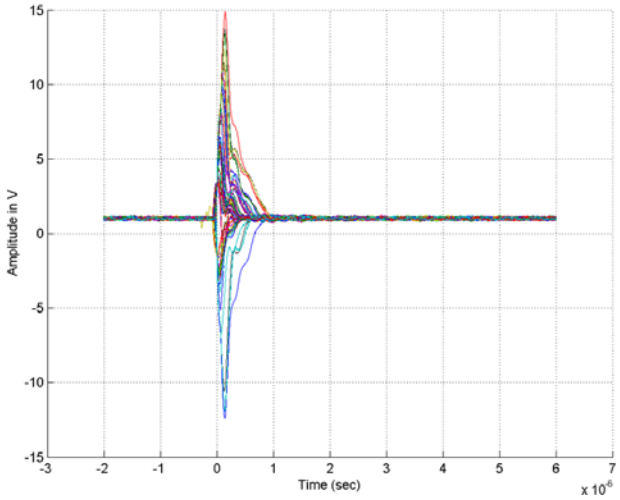



**Figure 57. SET Response with $V_S$ = ±15.0V**

With an LET = 43MeV•cm$^2$/mg, all transients lasted no longer than 1µs regardless of supply voltage. Voltage deviations were predominantly negative-going down to -1.35V with supplies at ±1.35V. With ±15V supplies, the voltage deviations were both positive up to +15V and negative down to approximately -12V.

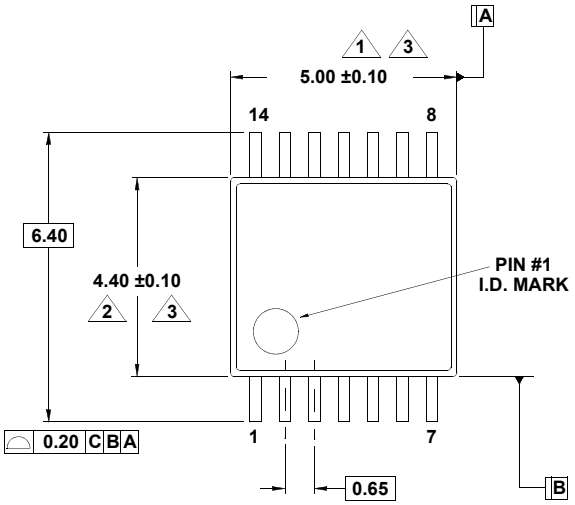
# 6. Revision History

| Rev. | Date | Description |
|---|---|---|
| 0.00 | Jun 6, 2017 | Initial release |

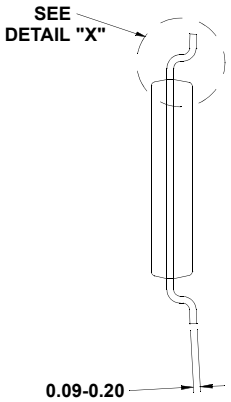
# 7. Package Outline Drawing

For the most recent package outline drawing, see M14.173.

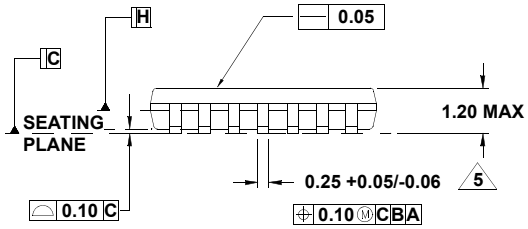
M14.173
14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 3, 10/09



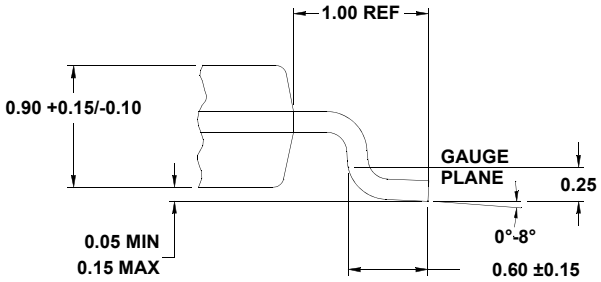

TOP VIEW



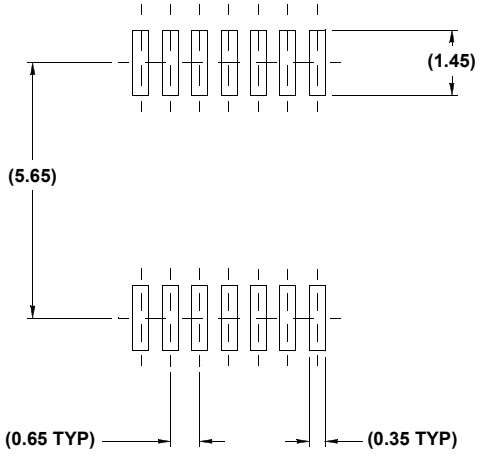

END VIEW




SIDE VIEW




DETAIL "X"




TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.

# 8. About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, please see the respective product information page found at www.intersil.com.

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