CAMERA MODULE SPECIFICATION

CUSTOMER NAME:
CUSTOMER PRODUCT NAME:
BYD PRODUCT NAME: UAR8238N

Customer Service Unit
Division VII
BYD COMPANY LIMITED

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NOTICE

This document is a general product description and maybe changed basing on customer's requirement.

Revision History

Version	Date [D/M/Y]	Notes	Writer
1.0	2014/12/14	Initial Released	WangLi

APPROVALS		
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Abbreviations

CMOS····· Complementary Metal-Oxide-Semiconductor Transistor
SVGA ····· Super Video Graphics Array (800x600)
SXGA ····· Super Extended Graphics Array (1280x1024)
SXVGA····· Super Extended Video Graphics Array (1280x960)
UXGA····· Ultra Extended Graphics Array (1600x1200)
VGA····· Video Graphics Array (640x480)
SCCB····· Serial Camera Control Bus
fps····· Frames per second
FPN····· Fixed Pattern Noise
AEC····· Auto Exposure
AGC····· Auto Exposure
AWB····· Auto Exposure
ABF····· Automatic Band Filter
ABLC····· Automatic Black-Level Calibration
TTL ·····Total Track Length
EFL····· Effective Focus Length
F/NO·····F Number
FOV····· Field Of View
CRA····· Chief Ray Angle
I^2C ····· Inter IC bus IF Interface
ISP····· Image Signal Processor
LSB····· Least Significant Bit
APE····· Application Processor Engine
bps····· bit per second
CCP····· Compact Camera Port
CCI ····· Camera Control Interface
DPCM····· Differential Pulse Code Modulation
CDS····· Correlated Double Sampling
I/O····· Input/Output

General description

Aptina's AS0260 is a 1/6-inch 2.0Mp CMOS digital image sensor with an integrated advanced camera system. This camera system features a microcontroller (MCU), a sophisticated image flow processor (IFP), MIPI and parallel output ports (only one output port can be used). The microcontroller manages all functions of the camera system and sets key operation parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 1920 x 1080 pixels with programmable timing and control circuitry. It also includes an analog signal chain with automatic offset correction, programmable gain, and a 10-bit analog-to-digital converter (ADC).

The entire system-on-a-chip (SOC) has superior low-light performance that is particularly suitable for PC camera applications. The AS0260 features Aptina's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The Aptina AS0260 can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 1080P image size at 30 frames per second (fps). It outputs JPEG compressed 8-bit data, using the parallel output port.

The AS0260 combines a 2.0Mp sensor core with an IFP to form a stand-alone solution for both image acquisition and processing. Both the sensor core and the IFP have internal registers that can be controlled by the user. In normal operation, an integrated microcontroller autonomously controls most aspects of operation. The processed image data is transmitted to the host system either through the parallel or MIPI interface. Figure 1 shows the major functional blocks of the AS0260.

Table 1. Lens Specification

Composition	3P
TTL	2.3 mm
F/NO	2.4±5%
FOV	DAGONAL：66±3°
TV-Distortion	<1%

AS0260 Sensor Specification

Features

- Superior low-light performance
- Ultra-low-power
- 1080p Full HD video at 30 fps
- Internal master clock generated by on-chip phase locked loop (PLL) oscillator
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single-die camera module
- Automatic image correction and enhancement
- Arbitrary image scaling with anti-aliasing
- Two-wire serial interface providing access to registers and microcontroller memory
- Selectable output data format: YCbCr, JPEG, MJPEG, 565RGB, 555RGB, 444RGB, processed Bayer, BT656, RAW8, RAW8+2-bit, and M420
- Parallel and 1- or 2-lane MIPI data output
- Independently configurable gamma correction
- Adaptive polynomial lens shading correction
- UVC interface support
- Perspective correction
- Multi-camera synchronization

Applications

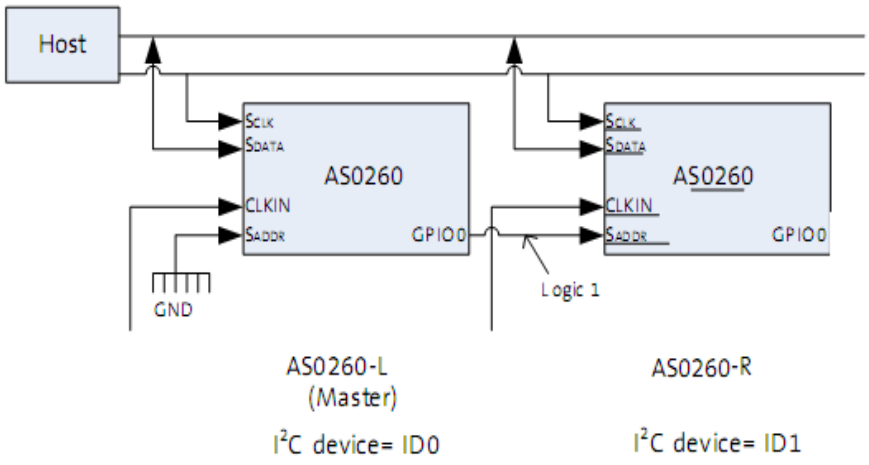
- Embedded tablet, notebook, and tethered PC cameras
- Game consoles
- Cell phones, mobile devices
- Consumer video communications

General Description

Table 1: Key Parameters

Parameter		Typical Value
Optical format		1/6-inch
Active pixels		1920 x 1080
Pixel size		1.4µm
Color filter array		RGB Bayer
Shutter type		Electronic rolling shutter (ERS)
Input clock range		6 – 54 MHz
Output pixel clock maximum		96 MHz
Output MIPI data rate maximum		768 Mb/s per lane
Frame Rate	1080p (full res)	30 fps
	720p	60 fps
	VGA	60 fps
	QVGA	120 fps
Responsivity		0.64 V/lux-sec
SNR_{MAX}		33dB
Pixel dynamic range		65dB
Supply voltage	Digital	1.7 – 1.95V
	Analog	2.5 – 3.1V
	I/O	1.7 – 1.95V or 2.5 – 3.1V
	PHY	1.7 – 1.95V
Power consumption[1]		255mW
Operating temperature, ambient		–30°C to +70° C
Chief ray angle		28°
Package options		CSP, Bare die

Auto-Sync Hardware Connections



This auto-sync mode is enabled through the following control register. When enabled the master device's GPIO/CHAIN pin and slave device's SADDR pin are used for inter-sensor communication (UDI). During the system setup phase (enumeration process) the two image sensors will be configured with unique slave addresses (typically 0xA0 and 0xA2).

Figure 2. Block Diagram

AS0260 Block Diagram

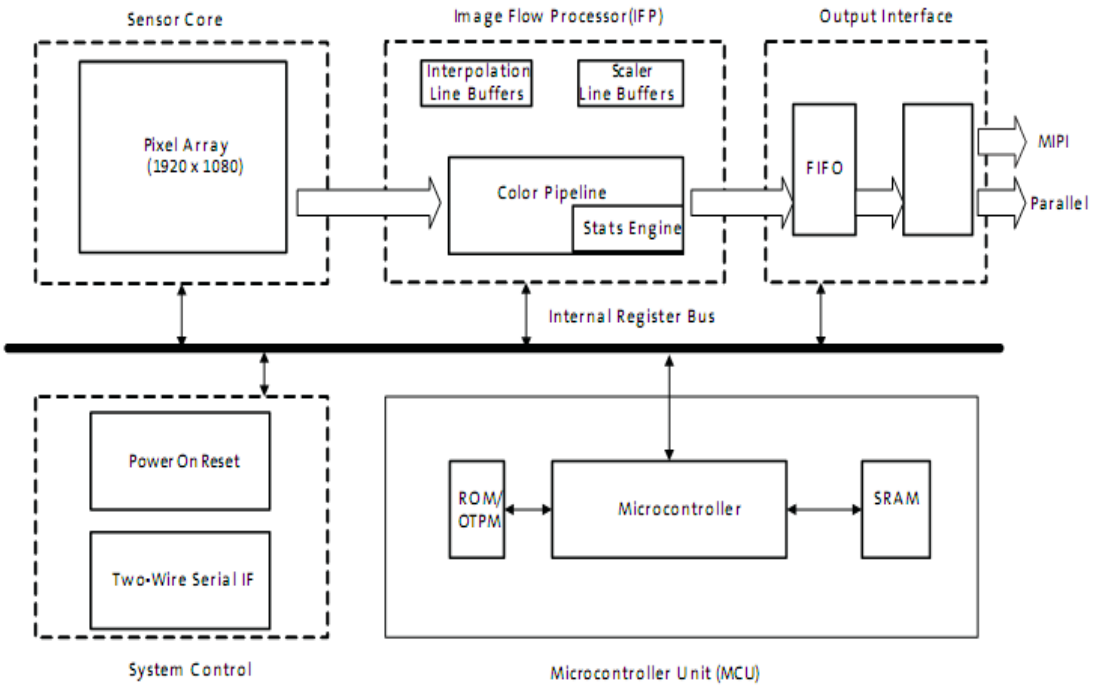
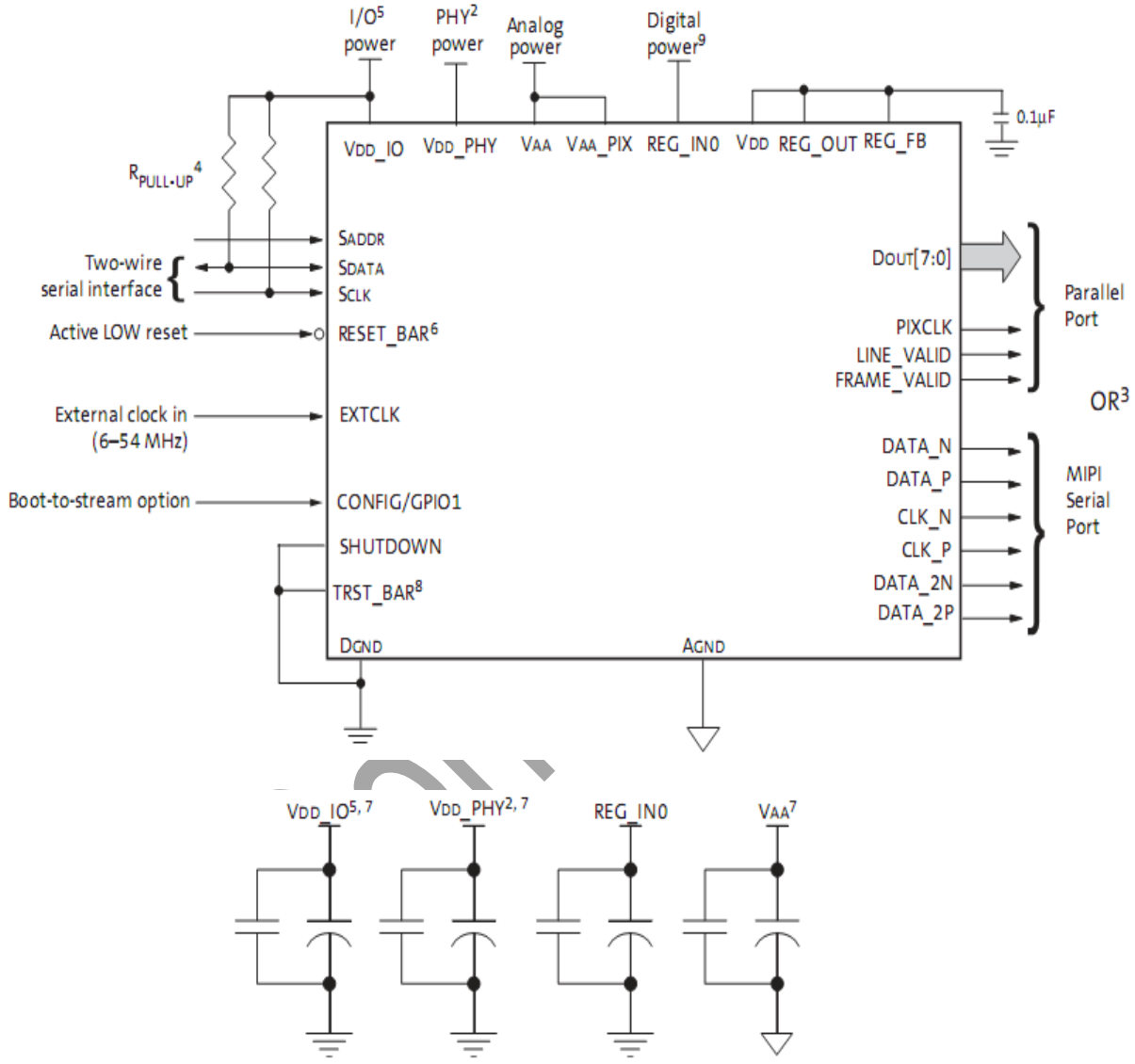
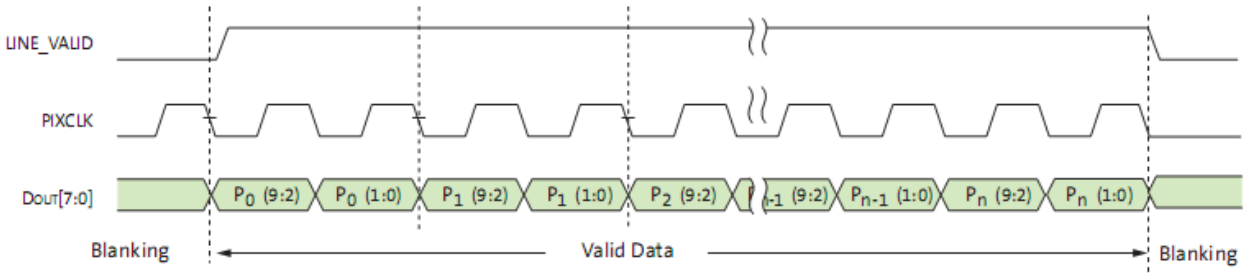


Figure 2: Typical Configuration



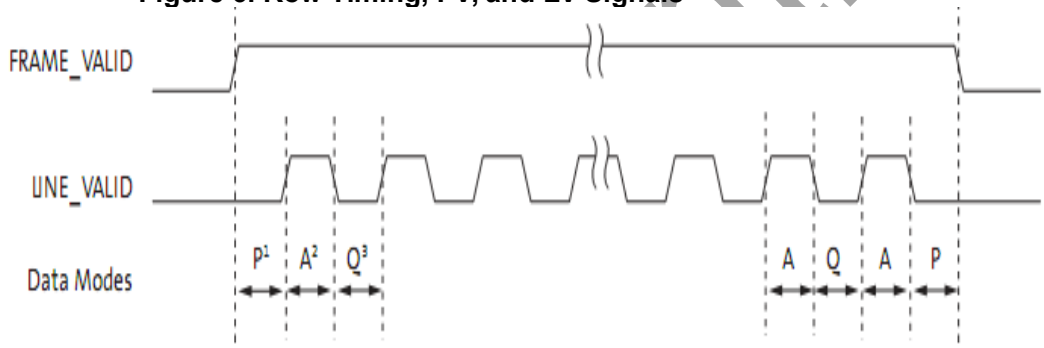
Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. If a MIPI Interface is not required, the MIPI serial port must be left floating. The VDD_PHY power signal must always be connected to the 1.8V supply.
3. Only one of the output modes (serial or parallel) can be used at any time.
4. Aptina recommends a 1.5kΩ resistor value for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.
5. All inputs must be configured with VDD_IO.
6. RESET_BAR has an internal pull-up resistor and can be left floating.
7. Aptina recommends that 0.1µF and 1µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and numbers may vary depending on layout and design considerations.
8. TRST_BAR connects to GND for normal operation.
9. Connections shown are for Revision 2 and later versions. Revision 1 of AS0260 requires VDD, REG_OUT, and REG_FB to be connected to REG_IN0.

Figure 5. Horizontal Timing YUV4:2:2



Note: Shown is 10-bit Bayer data in 8 + 2 mode.

Figure 6. Row Timing, FV, and LV Signals



Notes:
1. P: Frame start and end blanking time.
2. A: Active data time.
3. Q: Horizontal blanking time.

MIPI Port

The MIPI output implements a serial differential sub-LVDS transmitter capable of up to 1536 Mbps (768 Mbps/lane). It supports multiple formats, error checking, and custom short packets.

When the sensor is in the hardware standby system state or in the software standby system state, the MIPI signals (CLK_P, CLK_N, DATA_P, DATA_N, DATA_2P, DATA_2N) indicate ultra low power state (ULPS) corresponding to (nominal) 0V levels being driven on CLK_P, CLK_N, DATA_P, DATA_N, DATA_2P, and DATA_2N. This is equivalent to signaling code LP-00.

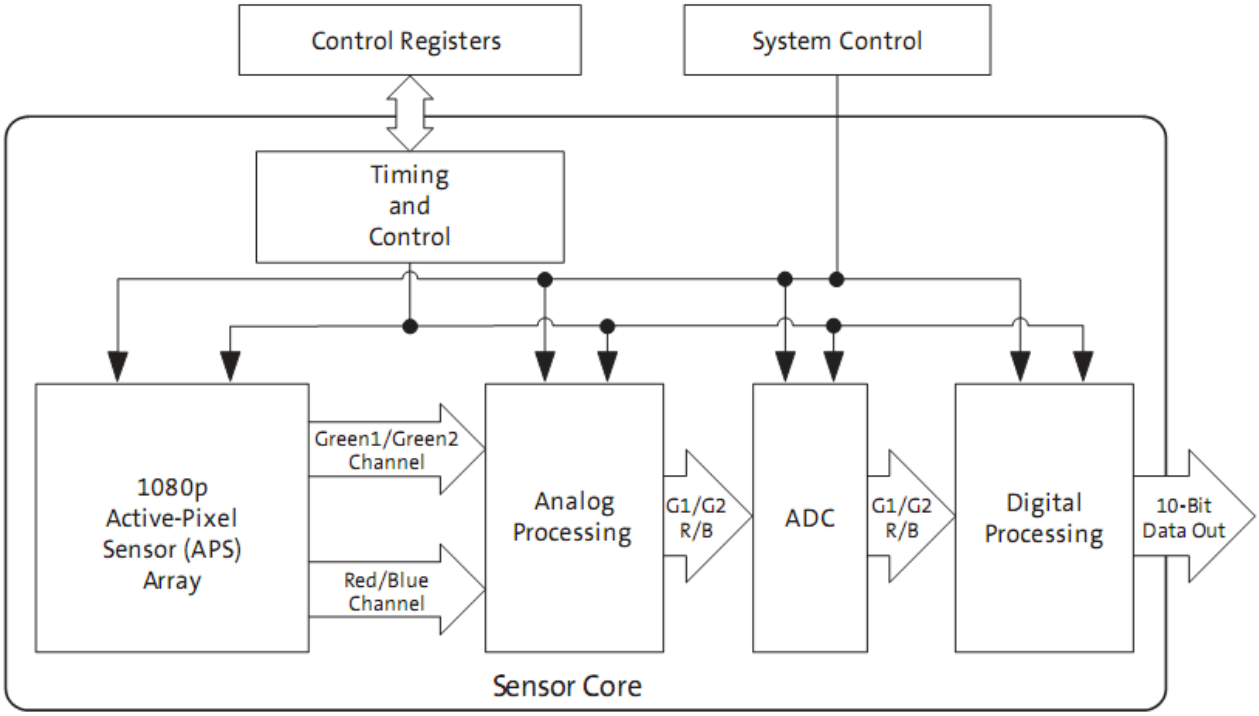
When the sensor enters the streaming system state, the interface goes through the following transitions:

1. After the PLL has locked and the bias generator for the MIPI drivers has stabilized, the MIPI interface transitions from the ULPS state to the ULPS-exit state (signaling code LP–10).
2. After a delay (TWAKEUP), the MIPI interface transitions from the ULPS-exit state to the TX-stop state (signaling code LP–11).
3. After a short period of time (the programmed integration time plus a fixed overhead), frames of pixel data start to be transmitted on the MIPI interface. Each frame of pixel data is transmitted as a number of high-speed packets. The transition from the TX-stop state to the high-speed signaling states occurs in accordance with the MIPI specifications. Between high-speed packets and between frames, the MIPI interface idles in the TX-stop state. The transition from the high-speed signaling states and the TX-stop state takes place in accordance with the MIPI specifications.
4. If the sensor is reset, any frame in progress is aborted immediately and the MIPI signals switch to indicate the ULPS.
5. If the sensor is taken out of the streaming system state and reset_register[4] = 1 (standby end-of-frame), any frame in progress is completed and the MIPI signals switch to indicate the ULPS.

If the sensor is taken out of the streaming system state and reset_register[4] = 0 (standby end-of-frame), any frame in progress is aborted as follows:

1. Any long packet in transmission is completed.
2. The end of frame short packet is transmitted.

Figure 8. Sensor Core Block Diagram



Testing

Optical testing

No	Test Item	Illumination Type	Distance	Intensity Range	Spec(2.0M)
1	Field of View	DNP Light Box(5100K)	N/A	>200Lux	>55°
2	TV-Distortion	DNP Light Box(5100K)	N/A	>200Lux	<1.5%
3	Resolution	Daylight Fluorescent (6500K)	Take the picture for full chart	250±50Lux	Centre: >800 Corners: >600
4	Shading	DNP Light Box(5100K)	Take the picture for full chart	>300Lux	>60%
5	Sensitivity	Daylight Fluorescent (6500K)	Take the picture for full chart	250±50Lux	>30db
6	Gray Scale	Daylight Fluorescent (6500K)	Take the picture for full chart	>200Lux	≥10 level
7	Focal Range	Daylight Fluorescent (6500K)	N/A	>200Lux	Non-obvious area in the target<80
8	Dark Noise	Daylight Fluorescent (6500K)	N/A	<1mLux	<10
9	Color Rendition	Daylight Fluorescent (6500K)	Take the picture for full chart	>200Lux	ΔE < 25
10	Inside Picture	Daylight Fluorescent (6500K)	40CM	>200Lux	N/A

Table 8. Optical testing

Environment testing

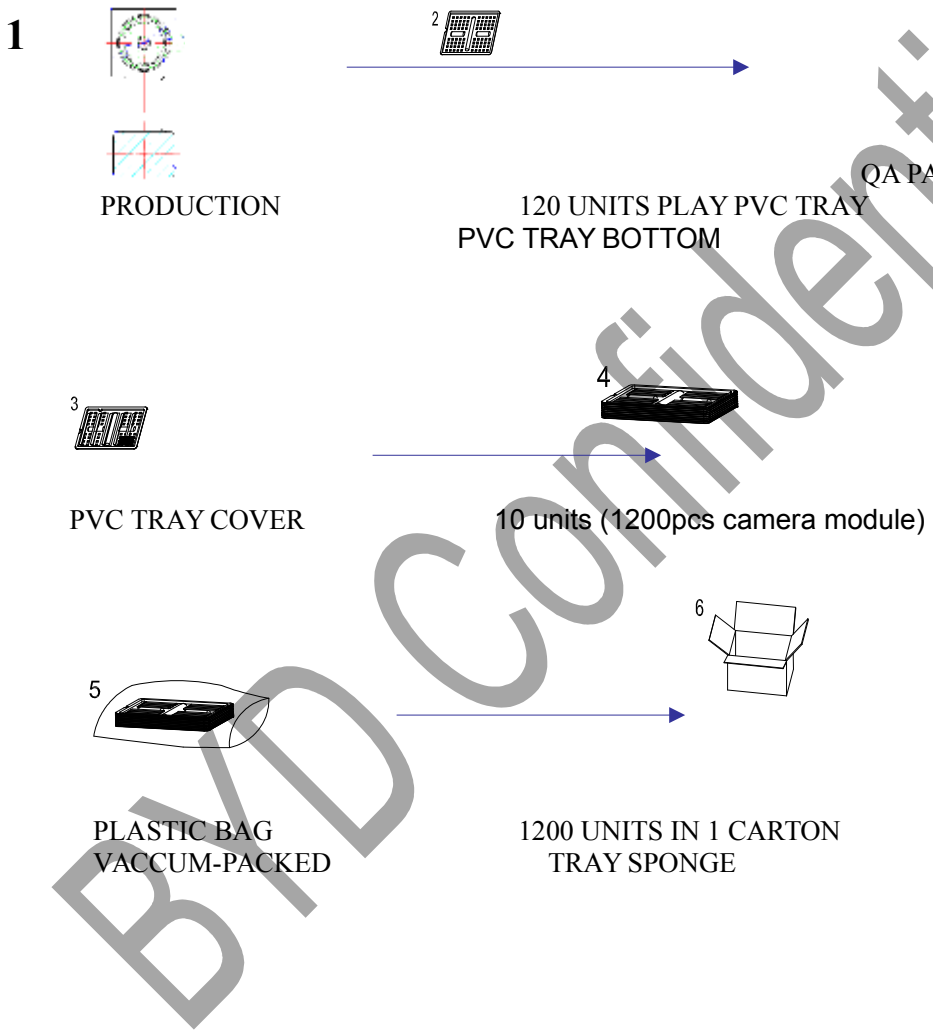
Table 10. Environment testing

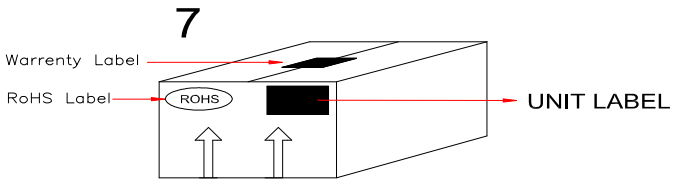
No	Test Item	Test Conditions	Judge standard
1	High Temp & Damp test	Temp.: 60°C ± 2°C Damp: 90% ± 3%RH Test duration: 48h	No image distort and good color rendition. Not to be dewy
2	Low Temperature storage	Temp.: －30°C ± 3°C Test duration: 48h	No image distort and good color rendition.
3	High Temperature storage	Temp.: 80°C ± 3°C Test duration: 48h	No image distort and good color rendition.
4	ESD(Electrostatic Discharge)	HBM:100pF/1500ohm; MM:200pF,2000V/10kv 3 times	No image distort and good color rendition.
5	Thermal Shock Test	Temp.: 80°C ± 3°C Temp.: －30°C ± 3°C 3min,24cycle	No image distort and good color rendition.
6	Vibration (Package State)	Frequency range: 5－200 Hz amplitude: 0.75mm 1 hour for each position. Test all 3 axes (X, Y, Z)	No image distort, good color rendition , no white、black、colorful dot.
7	Drop test Free fall (Package State)	Surface (floor) : Concrete or steel Number of drops: 10 Positions: Random Height: 120cm	No image distort, good color rendition , no white、black、colorful dot.
7	Drop test Free fall (Phone State)	Number of drops: 12 Positions: Random Height: 120cm	No image distort, good color rendition , no white、black、colorful dot.

Appendix 1: Packaging

The package must prevent damage to the components during transport and must be suitable for electrostatic-sensitive devices. The single camera modules shall be delivered in a reusable tray of antistatic plastic material. Several cameras shall be packed in one tray. The tray has separate holders for each camera-module.

Example:





Warranty label, ROHS label,和 UNIT label.

TRAY SPECIFICATION:
Material: black antistatic PS
Resistance: <1010 Ω
Dimension:260 (W) x 180 (D) x 11 (H) mm (Top tray and bottom tray assembly)
Capacity: 120 units (120pcs camera module)

ESD SHIELDING BAG SPECIFICATION:
Resistance: 107~1010 Ω
Dimension:430 (W) x 380 (D) x 0.075 (T) mm
Capacity : 10 units (1200pcs camera module)

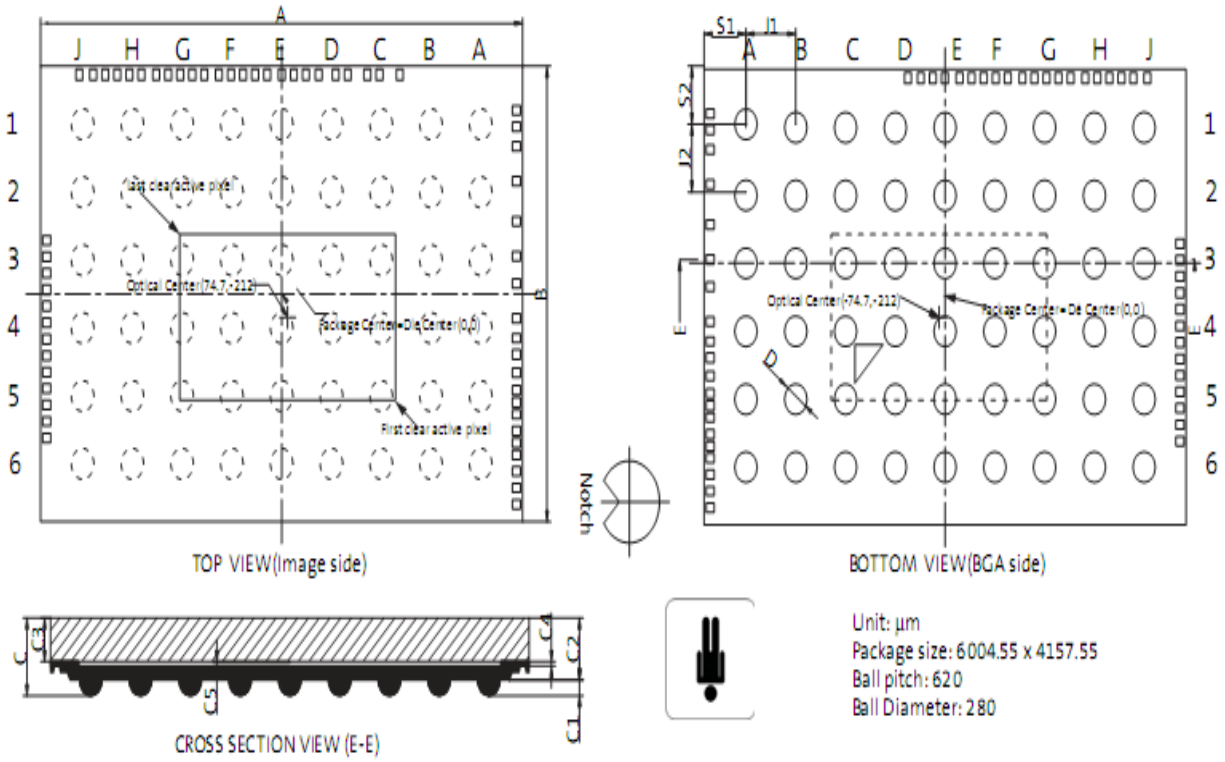
CARTON SPECIFICAITON:
Dimension:276 (W) x 198 (D) x 113 (H) mm

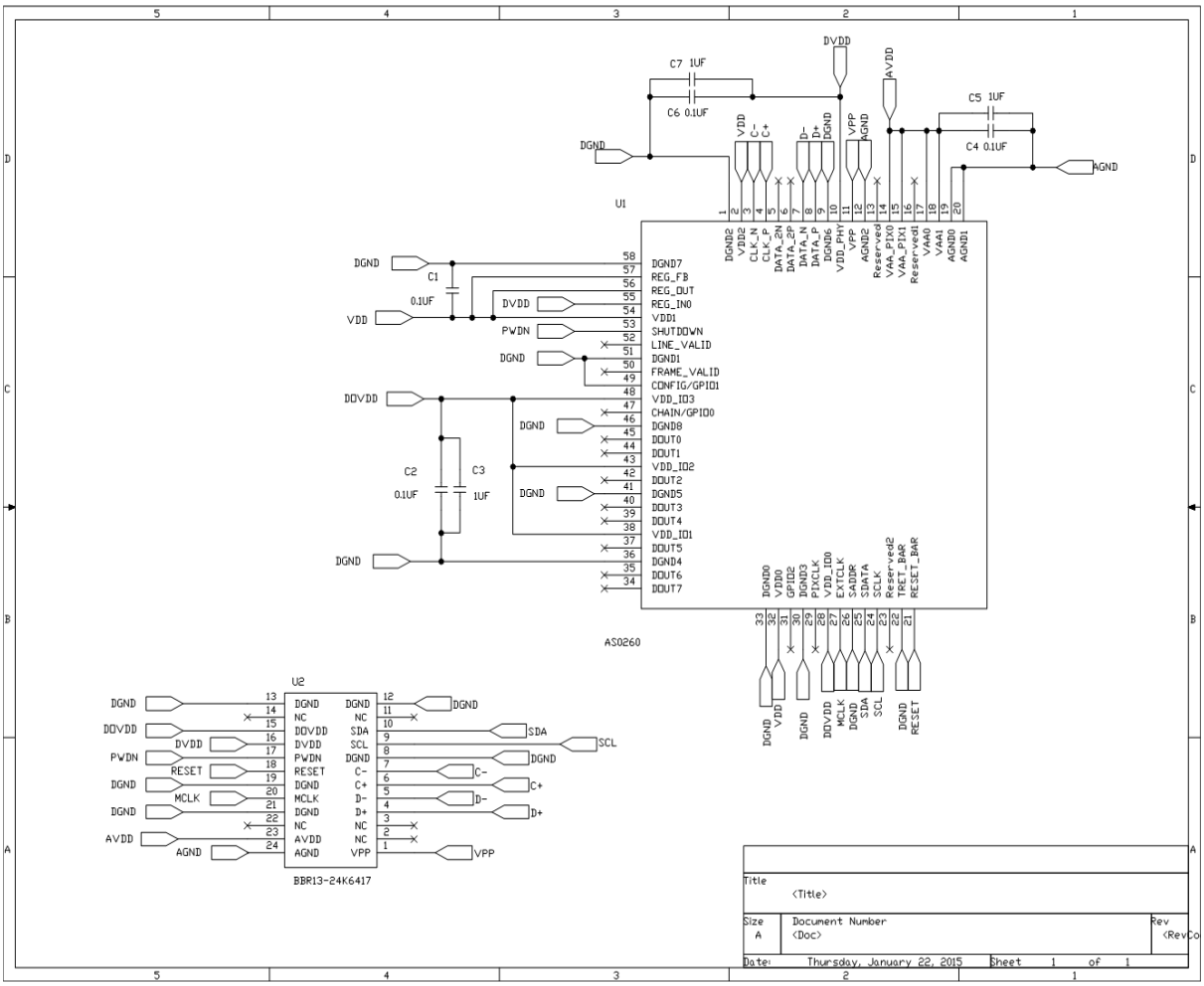
PAPER SHEET SPECIFICAITON:
Capacity : 1 units (1200pcs camera module)
Dimension:270 (W) x 192 (D) x 2.5 (T) mm

Appendix 2: Engineering Drawing

Appendix 3: Sensor datasheet

Figure 43: CSP Mechanical Drawing




C7 1UF
C6 0.1UF
C5 1UF
C4 0.1UF
C1
0.1UF
C2
0.1UF
C3
1UF
DVDD
AVDD
DGND
VDD
AGND
VPP
PWDN
DOVDD
U1
AS0260
U2
BBR13-24K6417
SDA
SCL
MCLK
RESET
C-
C+
D-
D+
Title
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