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April 1st, 2010 Renesas Electronics Corporation

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DATA SHEET



MOS FIELD EFFECT TRANSISTOR μ**PA2750GR**

PACKAGE DRAWING (Unit: mm)

2

3

4

; Source 1

Gate 1 7, 8; Drain 1

Source 2

Gate 2

6.0 ±0.3

4.4

0.8

□ 0.10

5, 6; Drain 2

← 0.5 ±0.2

ÅННĔ

F

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d

0.12 M

1.27 0.78 Max. 0.40 +0.10

5.37 Max

C

SWITCHING **N-CHANNEL POWER MOS FET**

DESCRIPTION

The µPA2750GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management application of notebook computers.

FEATURES

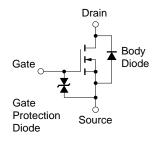
- Dual chip type
- · Low on-state resistance $RDS(on)1 = 15.5 \text{ m}\Omega \text{ MAX.}$ (VGS = 10 V, ID = 4.5 A) $R_{DS(on)2} = 21.0 \text{ m}\Omega \text{ MAX.}$ (VGS = 4.5 V, ID = 4.5 A) $R_{DS(on)3} = 23.9 \text{ m}\Omega \text{ MAX.}$ (Vgs = 4.0 V, ID = 4.5 A)
- Low Ciss: Ciss = 1040 pF TYP. (VDS = 10 V, VGS = 0 V)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION PACKAGE PART NUMBER μPA2750GR Power SOP8

ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vos = 0 V)	VDSS	30	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC)	D(DC)	±9.0	А
Drain Current (pulse) Note1	D(pulse)	±36	А
Total Power Dissipation (1 unit) Note2	Р⊤	1.7	W
Total Power Dissipation (2 unit) Note2	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	–55 to +150	°C
Single Avalanche Current Note3	AS	9.0	А
Single Avalanche Energy ^{Note3}	Eas	8.1	mJ

EQUIVALENT CIRCUIT (1/2 circuit)



Notes 1. PW \leq 10 μ s, Duty cycle \leq 1%

- 2. TA = 25°C, Mounted on ceramic substrate of 2000 mm² x 2.2 mm
- 3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V
- **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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90%

90%

tf

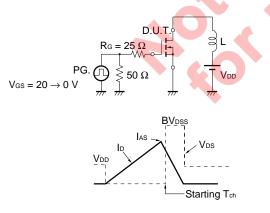
10%

td(off)

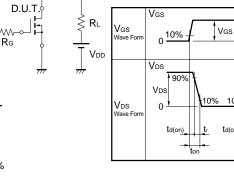
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	Vds = 30 V, Vgs = 0 V			10	μA
Gate Leakage Current	lgss	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA
Gate Cut-off Voltage	VGS(off)	Vds = 10 V, Id = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	Vds = 10 V, Id = 4.5 A	5	11		S
Drain to Source On-state Resistance	RDS(on)1	$V_{GS} = 10 \text{ V}, \text{ ID} = 4.5 \text{ A}$		12.5	15.5	mΩ
	RDS(on)2	Vgs = 4.5 V, Id = 4.5 A		16.0	21.0	mΩ
	RDS(on)3	$V_{GS} = 4.0 \text{ V}, \text{ I}_{D} = 4.5 \text{ A}$		17.9	23.9	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		1040		pF
Output Capacitance	Coss	V _{GS} = 0 V		390		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		130		pF
Turn-on Delay Time	td(on)	Vdd = 15 V, Id = 4.5 A		13		ns
Rise Time	tr	V _{GS} = 10 V		10		ns
Turn-off Delay Time	$t_{d(off)}$	R _G = 10 Ω	S	43		ns
Fall Time	tr			9		ns
Total Gate Charge	Q _G	Vpd = 24 V		21		nC
Gate to Source Charge	QGS	V _{GS} = 10 V		3.3		nC
Gate to Drain Charge	Qgd	Ib = 9.0 A		5.1		nC
Body Diode Forward Voltage	VF(S-D)	I⊧ = 9.0 A, V₀s = 0 V		0.84		V
Reverse Recovery Time	trr	IF = 9.0 A, Vgs = 0 V		34		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ µs		34		nC

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$, All terminals are connected.)

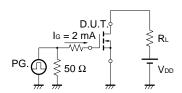
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



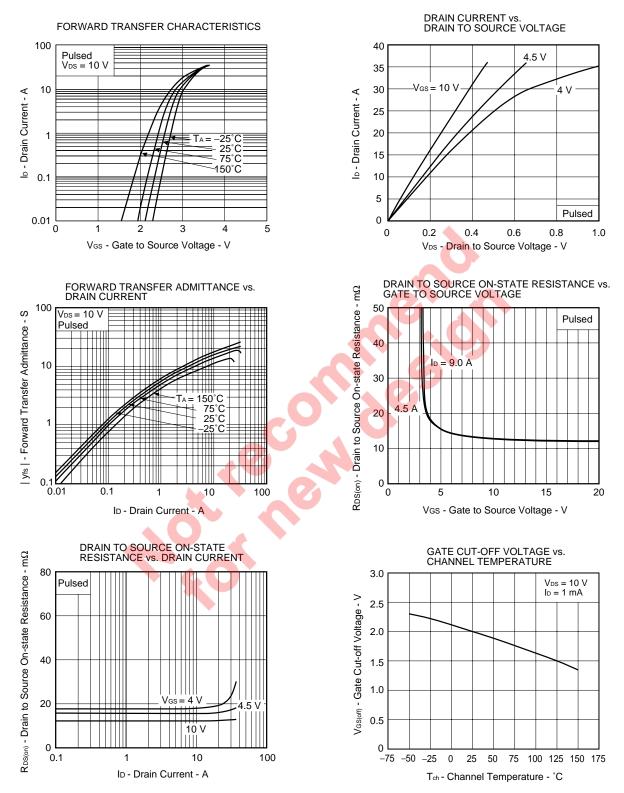
PG

τ

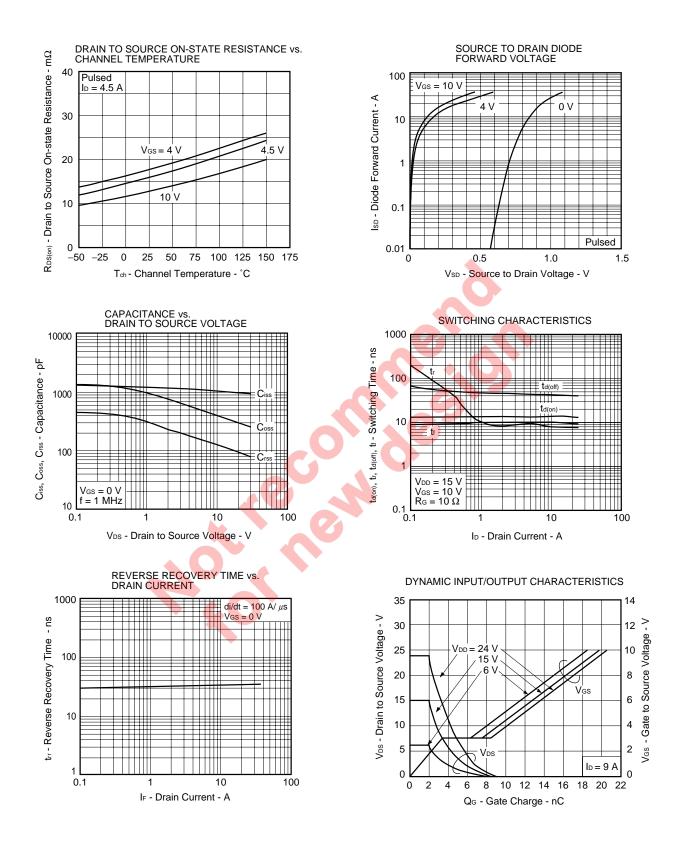
 $\begin{array}{l} \tau = 1 \; \mu s \\ \text{Duty Cycle} \leq 1\% \end{array}$

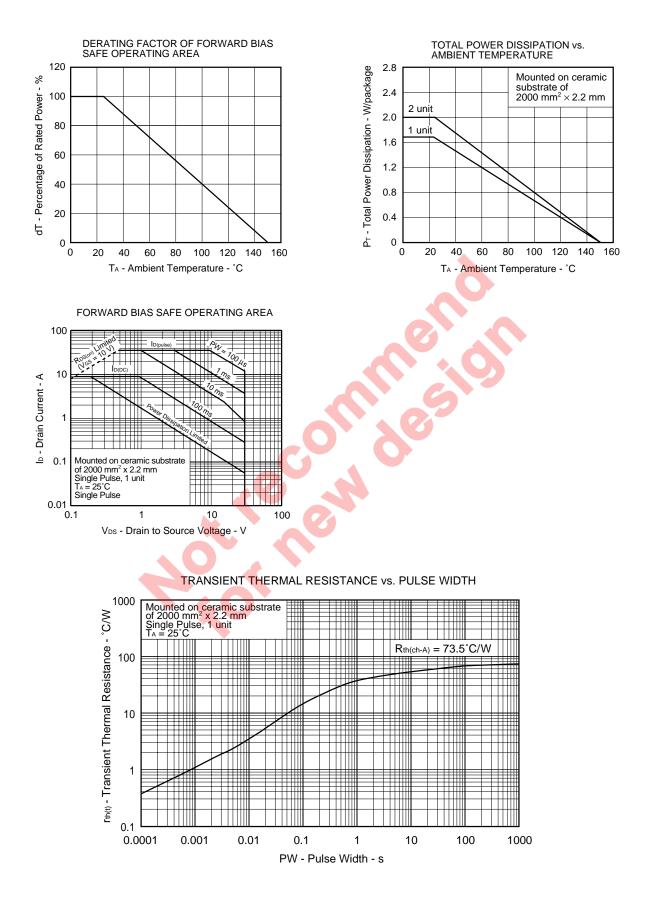
Vgs

0

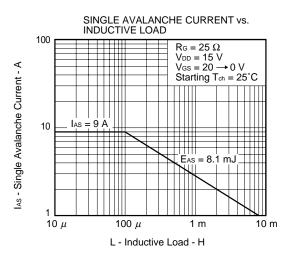


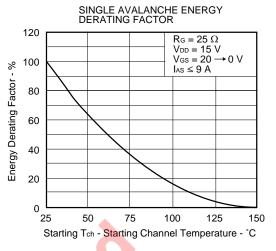
TYPICAL CHARACTERISTICS (TA = 25°C)





Data Sheet G15780EJ1V0DS





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