



# Quad 8-Bit CMOS D/A Converter with Internal 10 V Reference

## DAC-8426

### 1.1 Scope.

This specification covers the detail requirement for a quad 8-bit CMOS digital-to-analog converter with output voltage amplifiers and internal 10 V voltage reference. The internal latches provide direct interface for most microprocessors. The DAC-8426 operates with either a dual or single power supply.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace specification control drawings.

### 1.2 Part Number.

The complete part numbers per Table 1 of this specification is as follows:

Device	Part Number	Package
-1	DAC-8426AR/883	R

### 1.2.3 Case Outline.

Letter	Case Outline (Lead Finish per MIL-M-38510)
R	20-Lead Ceramic Dual-in-Line Package (Cerdip)

### 1.3 Absolute Maximum Ratings. ( $T_A = +25^\circ\text{C}$ unless otherwise noted)

$V_{DD}$ to AGND or DGND	-0.3 V, +17 V
$V_{SS}$ to AGND or DGND	-7 V, $V_{DD}$
$V_{DD}$ to $V_{SS}$	-0.3 V, +24 V
AGND to DGND	-0.3 V, +5 V
Digital Input Voltage to DGND	-0.3 V, $V_{DD}$
$V_{REFOUT}$ to AGND	-0.3 V, $V_{DD}$
$V_{OUT}$ to AGND	$V_{SS}$ , $V_{DD}$
Power Dissipation to +75°C	500 mW
Derate above 75°C by	6.4 mW/°C
Operating Temperature Range	-55°C to +125°C
Junction Temperature Range ( $T_J$ )	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 60 sec)	+300°C

### 1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC}$	$7^\circ\text{C/W}$
$\theta_{JA}$	$70^\circ\text{C/W max}$

# DAC-8426—SPECIFICATIONS

Table 1.

Test	Symbol	Device Types	Limits		Group A Subgroups	Conditions <sup>1</sup>	Units
			Min	Max			
Resolution	N	All	8		1, 2, 3	T <sub>A</sub> = +25°C, -55°C & +125°C	Bits
Total Unadjusted Error	TUE	All	-1	±1	1, 2, 3	Includes Reference <sup>2</sup> T <sub>A</sub> = +25°C, -55°C & +125°C	LSB
			-2	±2	1, 2, 3		
Relative Accuracy	INL	All	-1	±1/2	1, 2, 3	T <sub>A</sub> = +25°C, -55°C & +125°C	LSB
			-2	±1	1, 2, 3		
Differential Nonlinearity	DNL	All		±1	1, 2, 3	Note 3; T <sub>A</sub> = +25°C, -55°C & +125°C	LSB
Zero Scale Error	V <sub>ZSE</sub>	All		20	1, 2, 3	V <sub>SS</sub> = -5 V; T <sub>A</sub> = +25°C, -55°C & +125°C	mV
Reference Output Voltage	V <sub>REFOUT</sub>	All	-1	9.96	1, 2, 3	No Load; T <sub>A</sub> = +25°C, -55°C & +125°C	V
			-2	9.92			
Reference Load Regulation	LD <sub>REG</sub>	All		0.1	1, 2, 3	ΔI <sub>L</sub> = 10 mA; T <sub>A</sub> = +25°C, -55°C & +125°C	%/mA
Reference Line Regulation	LN <sub>REG</sub>	All		0.04	1, 2, 3	ΔV <sub>DD</sub> = ±10%; T <sub>A</sub> = +25°C, -55°C & +125°C	%/mA
Reference Output Current	I <sub>REFOUT</sub>	All	5		1, 2, 3	ΔV <sub>REFOUT</sub> < 40 mV; T <sub>A</sub> = +25°C, -55°C & +125°C	mA
Logic Input "0"	V <sub>INL</sub>	All		0.8	1, 2, 3	T <sub>A</sub> = +25°C, -55°C & +125°C	V
Logic Input "1"	V <sub>INH</sub>	All	2.4		1, 2, 3	T <sub>A</sub> = +25°C, -55°C & +125°C	V
Logic Input Current	I <sub>IN</sub>	All		10	1, 2, 3	V <sub>IN</sub> = 0 V or V <sub>DD</sub> ; T <sub>A</sub> = +25°C, -55°C & +125°C	μA
Positive Supply Current <sup>3</sup>	I <sub>DD</sub>	All		14	1, 2, 3	T <sub>A</sub> = +25°C, -55°C & +125°C	mA
Negative Supply Current <sup>3</sup>	I <sub>SS</sub>	All		10	1, 2, 3	Dual Supply, V <sub>SS</sub> = -5 V; T <sub>A</sub> = +25°C, -55°C & +125°C	mA
Power Supply Sensitivity	PSS	All		0.01	1, 2, 3	ΔV <sub>DD</sub> = ±10%; T <sub>A</sub> = +25°C, -55°C & +125°C	%/%
Output Source Current	I <sub>OUT</sub>	All	10		1, 2, 3	Digital Inputs All Ones; T <sub>A</sub> = +25°C, -55°C & +125°C	mA
Output Sink Current	I <sub>OUT-</sub>	All	0.35		1, 2, 3	Digital Inputs All Zeros	mA
V <sub>OUT</sub> Settling Time (Positive or Negative)	t <sub>S</sub>	All		5	9	T <sub>O</sub> ±1/2 LSB; T <sub>A</sub> = +25°C	μs
Address to Write Setup Time	t <sub>AS</sub>	All	0		9, 10, 11	T <sub>A</sub> = +25°C, -55°C & +125°C	ns
Address to Write Hold Time	t <sub>AH</sub>	All	0		9, 10, 11	T <sub>A</sub> = +25°C, -55°C & +125°C	ns
Data Valid to Write Setup Time	t <sub>DS</sub>	All	70		9, 10, 11	T <sub>A</sub> = +25°C, -55°C & +125°C	ns
Data Valid to Write Hold Time	t <sub>DH</sub>	All	10		9, 10, 11	T <sub>A</sub> = +25°C, -55°C & +125°C	ns
Write Pulse Width	t <sub>WR</sub>	All	50		9, 10, 11	T <sub>A</sub> = +25°C, -55°C & +125°C	ns
Minimum Load Resistance	R <sub>L(MIN)</sub>	All	2		1, 2, 3	Digital Inputs All Ones; T <sub>A</sub> = +25°C, -55°C & +125°C	kΩ
V <sub>OUT</sub> Slew Rate	SR	All	2.5		7	T <sub>A</sub> = +25°C	V/μs

NOTES

<sup>1</sup>V<sub>DD</sub> = +15 V ± 10%, AGND = 0 V, DGND = 0 V, V<sub>SS</sub> = 0 V unless otherwise specified.

<sup>2</sup>Includes full-scale error, relative accuracy, and zero code error.

<sup>3</sup>Digital inputs V<sub>IN</sub> = V<sub>INL</sub> or V<sub>INH</sub>; V<sub>OUT</sub> and V<sub>REFOUT</sub> unloaded.

**Table 2. Electrical Test Requirements for Class B Devices**

MIL-STD-883 Test Requirements	Subgroups (See Table 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1,* 2, 3
Group A Test Requirements	1, 2, 3, 7, 9, 10, 11

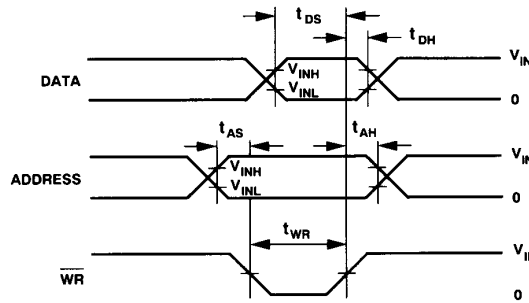
**NOTE**

\*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

**Table 3. Control Table**

Logic Control			DAC-8426
WR	A1	A0	Operation
H	X	X	No Operation Device Not Selected
L	L	L	DAC A Transparent
$\overline{L}$	L	L	DAC A Latched
L	L	H	DAC B Transparent
$\overline{L}$	L	H	DAC B Latched
L	H	L	DAC C Transparent
$\overline{L}$	H	L	DAC C Latched
L	H	H	DAC D Transparent
$\overline{L}$	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care.



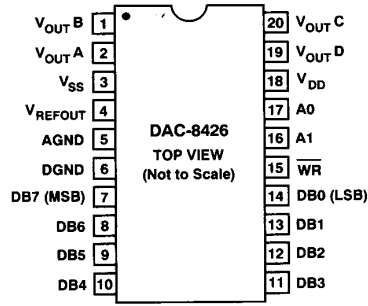
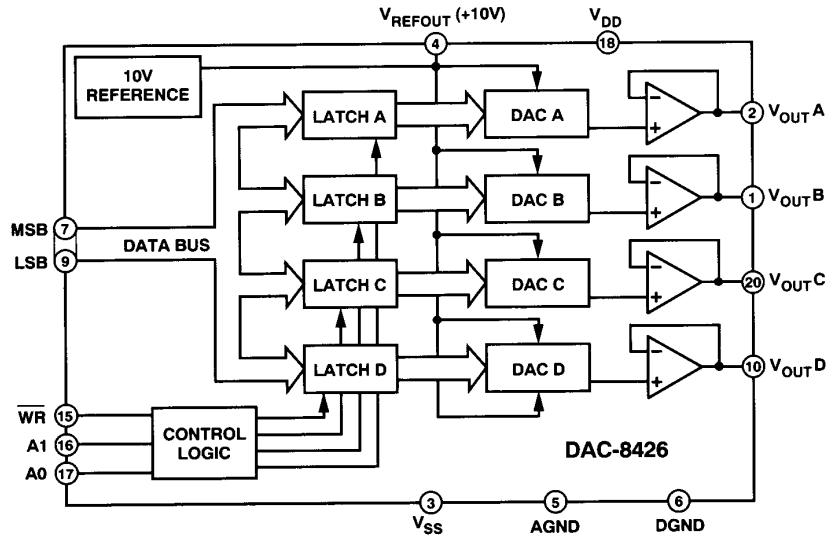
**NOTES:**

1. ALL INPUT SIGNAL RISE AND FALL TIMES ARE MEASURED FROM THE 10% TO 90% OF V<sub>DD</sub> (t<sub>r</sub> = t<sub>f</sub> = 20ns OVER THE V<sub>DD</sub> RANGE)
2. TIMING REFERENCE LEVEL IS FROM  $\frac{V_{INH} + V_{INL}}{2}$
3. V<sub>IN</sub> = 5V

*Write Timing Diagram*

# DAC-8426

## 3.2.1 Functional Block Diagram and Terminal Assignments.

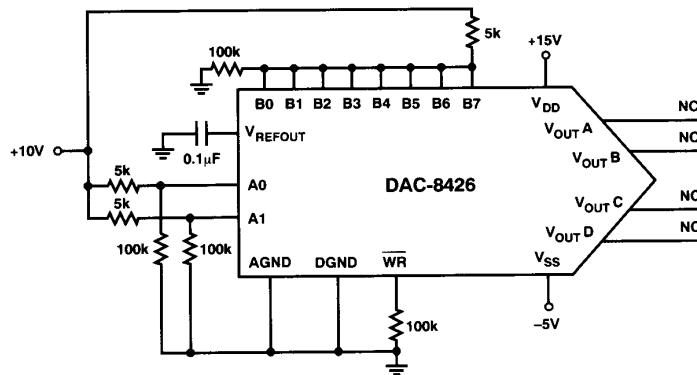


## 3.2.4 Microcircuit Technology Group.

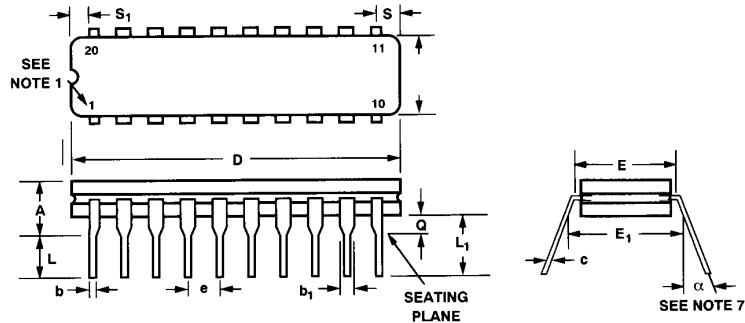
This microcircuit is covered by technology group 80.

## 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



20-Lead Ceramic DIP  
(R Suffix)



20-Lead Ceramic DIP  
(R Suffix)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	
b <sub>1</sub>	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E <sub>1</sub>	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	
L <sub>1</sub>	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	6
S <sub>1</sub>	0.005		0.13		6
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b<sub>1</sub> may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100" (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Leads center when α is 0°. E<sub>1</sub> shall be measured at the centerline of the leads.



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