

Display Elektronik GmbH

DATA SHEET

STANDARD OLED/PLED

DEP 128064J - Y



Product Specification

Version : 01

22.08.2008

C O N T E N T S

1. Numbering System
2. General Specification
3. Absolute Maximum Ratings
4. Electrical Characteristics
5. Optical Characteristics
6. Block Diagram
7. Interface Pin Function
8. Timing Characteristics
9. Power ON / OFF Sequence & Application Circuit
10. Display Control Instruction
11. Reliability
12. Appendix

1. Numbering System

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128×64	dots
Module dimension (L*W*H)	41.9*28.0*1.6(MAX)	mm
View area	38.45*20.21	mm
Active area	36.45*18.21	mm
Dot size	0.255(W)×0.255(H)	mm
Dot pitch	0.285(W)×0.285 (H)	mm

(2) Controller IC: SSD1325 Controller

(3) Temperature Range

Operating	-40 ~ +70°C
Storage	-40 ~ +85°C

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	°C
Storage Temperature	TST	-40	—	+85	°C
Input Voltage (VDD)	VDD	-0.3	—	3.5	V
Supply Voltage (Vcc)	Vcc	8	—	16	V
Humidity	—	—	—	85	%
Operating lift time	—	—	40000(*)	—	Hrs

*:60cd/m² light on

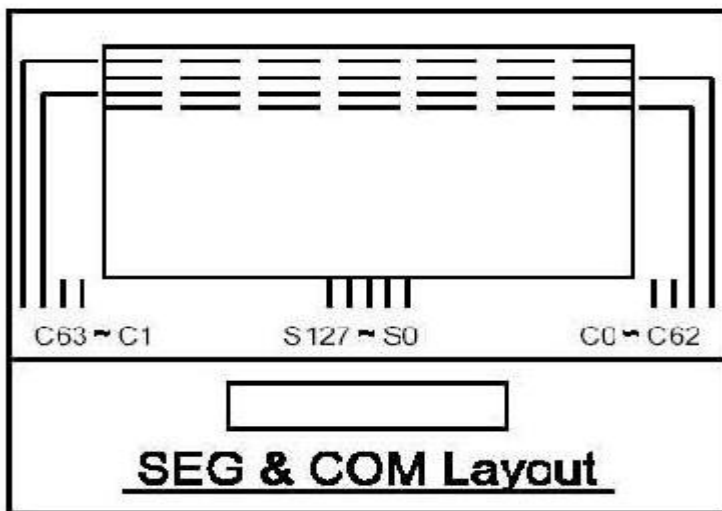
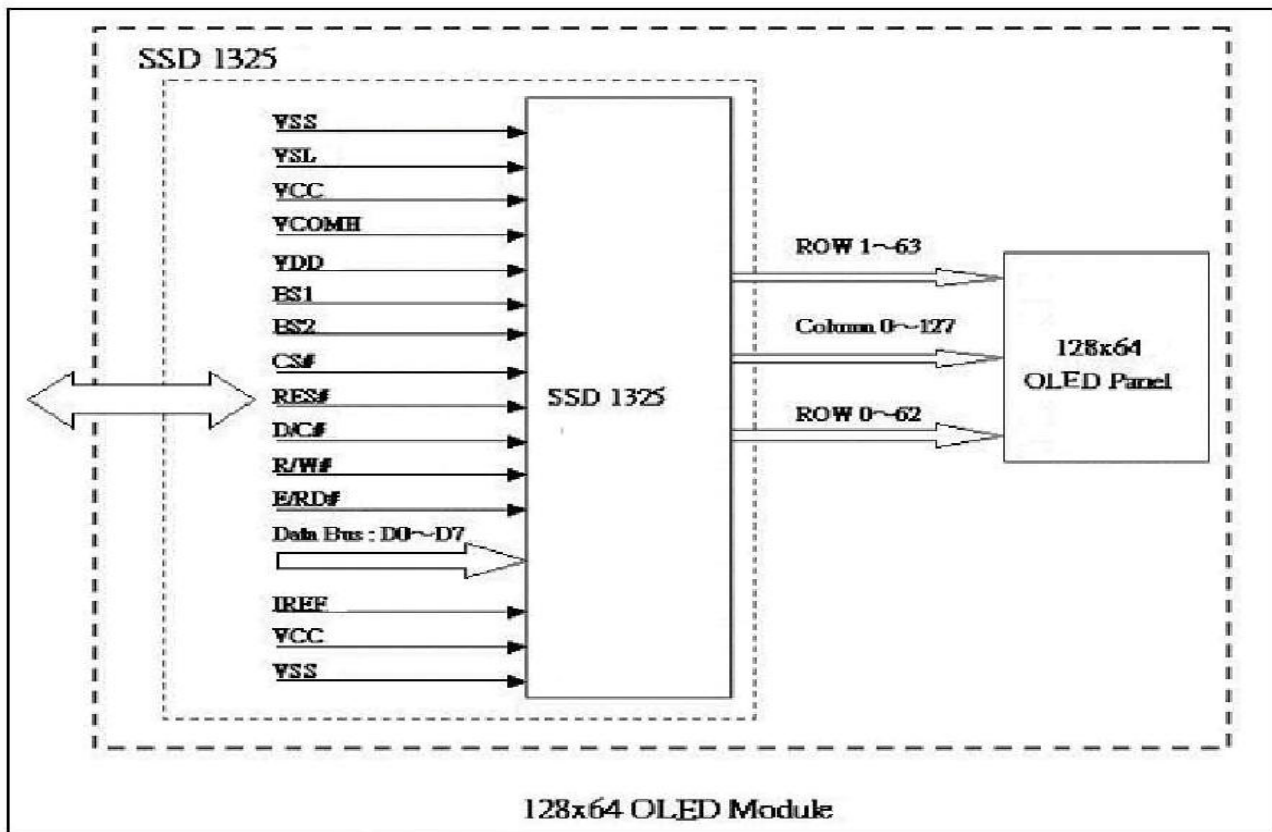
4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V _{DD} -V _{SS}	—	2.4	2.7	3.5	V
Supply Voltage For Panel	V _{CC} -V _{SS}	—	13.5	14	14.5	V
Input High Vol	V _{IH}	—	0.8V _{DD}	—	V _{DD}	V
Input Low Vol	V _{IL}	—	0	—	0.2V _{DD}	V
Output High Vol	V _{OH}	—	0.9V _{DD}	—	V _{DD}	V
Output Low Vol.	V _{OL}	—	0	—	0.1V _{DD}	V
Supply Current	I _{DD}	—	—	18	20	mA

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	160	—	—	deg
Dark Room contrast	2000:1	—	—	—
Response Time	—	10	—	us

6. Block Diagram



7. Interface Pin Function

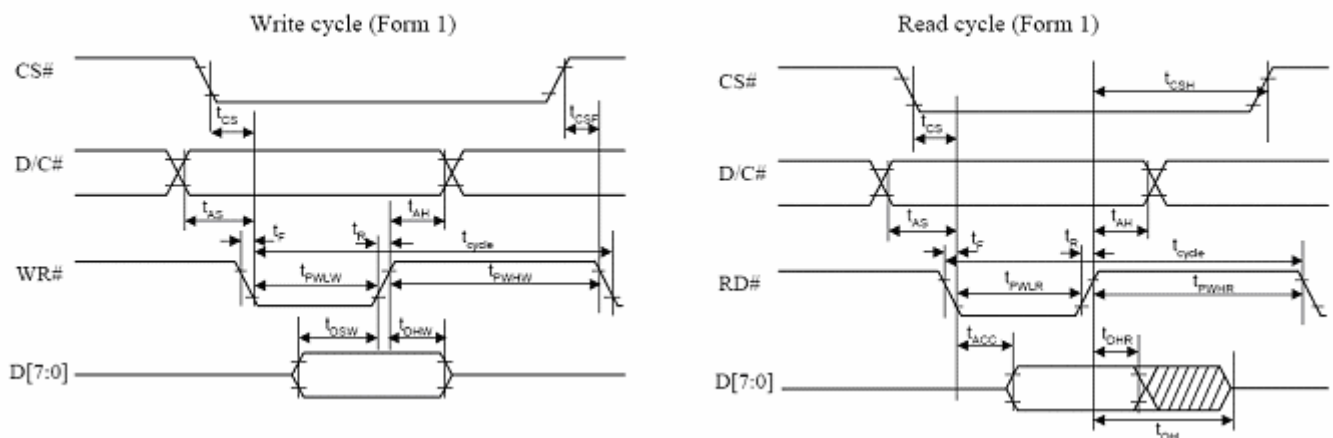
Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	VSL	—	This pin is the output pin for the voltage output low level for SEG signals. This pin can be kept NC or connected with a capacitor to VSS for stability.
3	Vcc	—	Positive OLED high voltage power supply
4	VCOMH	—	The COM voltage reference pin, this pin should be connected to ground through a capacitor
5	VDD	H/L	Voltage power supply for logic
6	BS1	H/L	Interface select pin
7	BS2	H/L	Interface select pin
8	CS#	H/L	Chip select pin. The driver IC will be selected When CS pin is active low.
9	RES#	H/L	Hardware reset signal
10	D/C#	H/L	This is data/command control pin, H: Data input ,L: Command input .
11	R/W#	H/L	Write strobe signal and reads data at the low level
12	E(RD)	H/L	Read strobe signal and reads data at the low level
13	DB0	H/L	Data bus line
14	DB1	H/L	Data bus line
15	DB2	H/L	Data bus line
16	DB3	H/L	Data bus line
17	DB4	H/L	Data bus line
18	DB5	H/L	Data bus line
19	DB6	H/L	Data bus line
20	DB7	H/L	Data bus line
21	IREF	—	The current reference input pin, this pin should be connected to ground through a resistor.
22	Vcc	—	Positive OLED high voltage power supply
23	NC	—	No connection
24	Vss	—	This is ground pin

8. Timing Characteristics

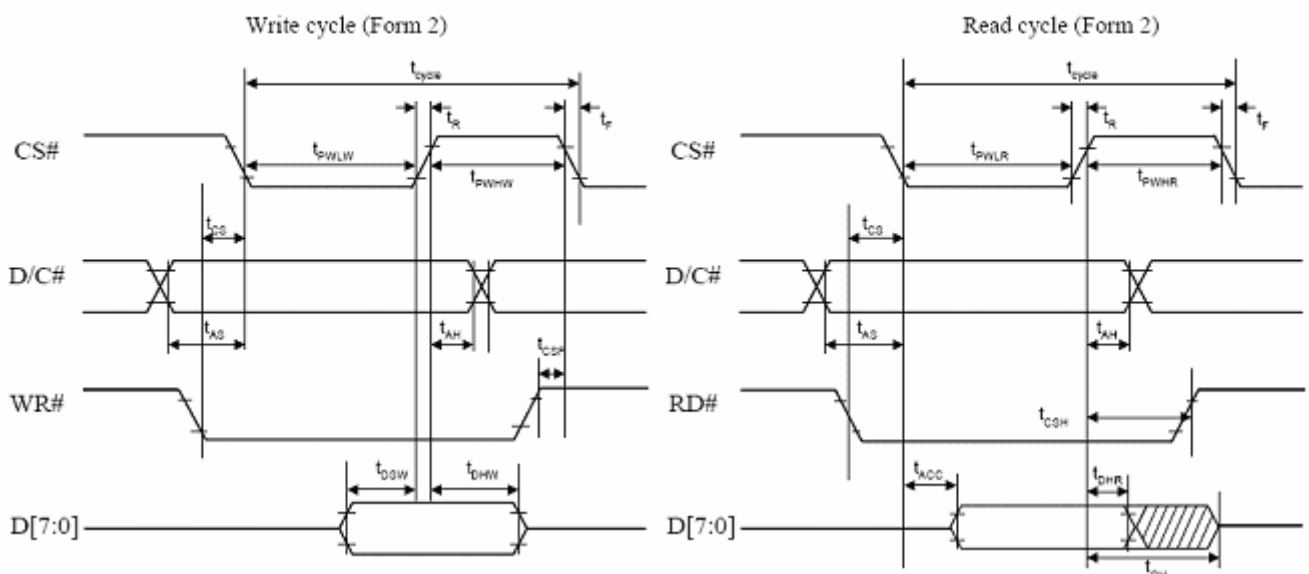
8-1.8080 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLr}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHr}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_{r}	Rise Time	-	-	15	ns
t_{f}	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics (Form 1)



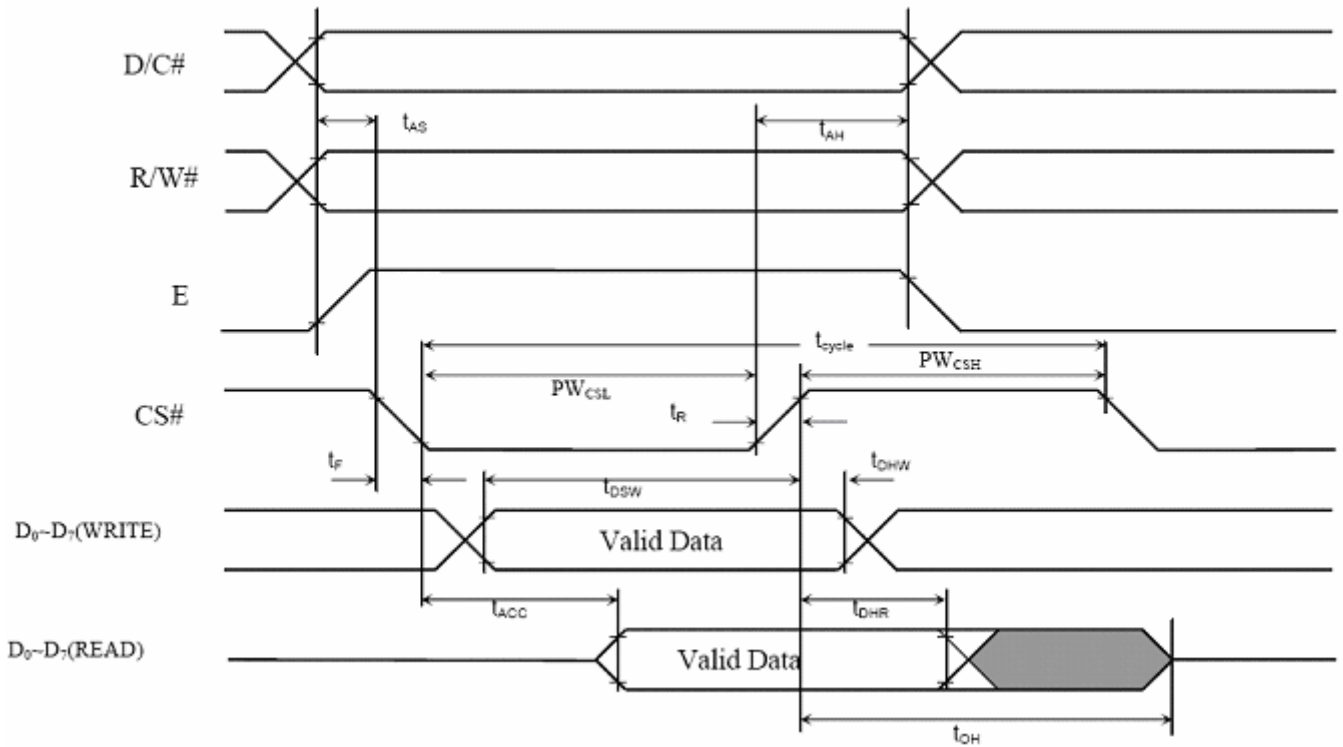
8080-series parallel interface characteristics (Form 2)



8-2.6800 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_{R}	Rise Time	-	-	15	ns
t_{F}	Fall Time	-	-	15	ns

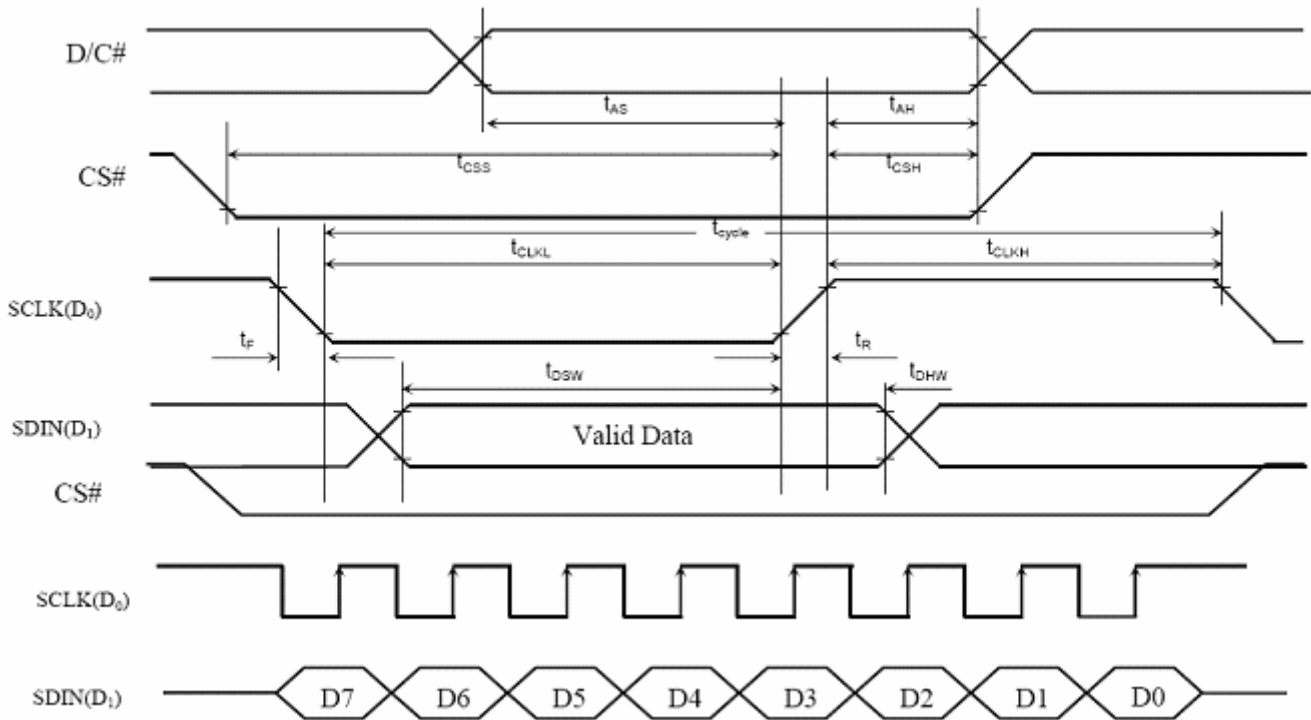
6800-series MPU Parallel Interface Characteristics



8-3.Serial Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial Interface Characteristics

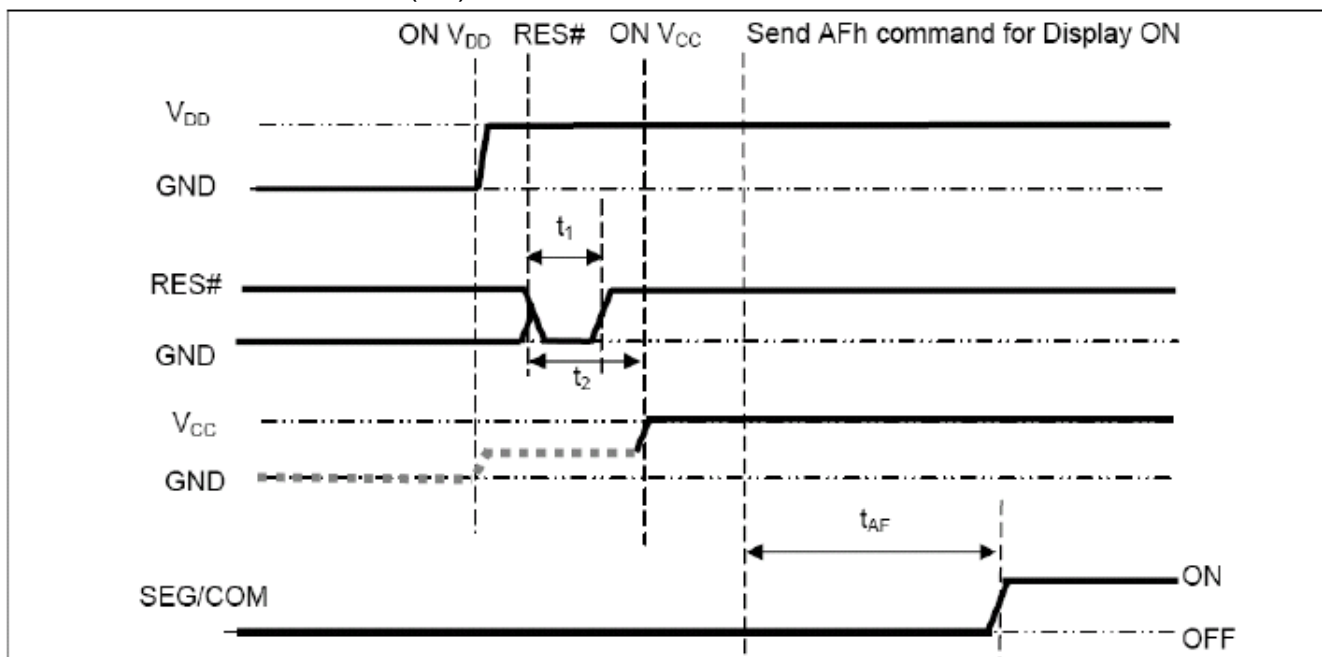


9. Power ON / OFF Sequence & Application Circuit

9.1 POWER ON / OFF SEQUENCE

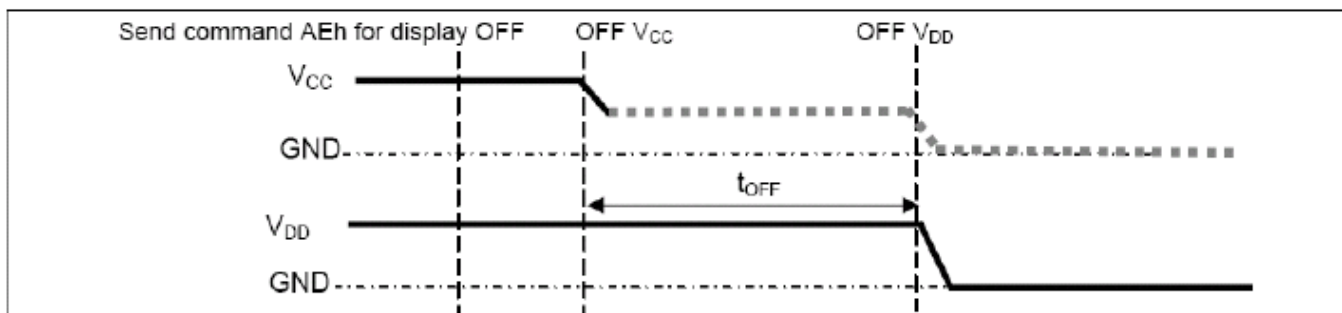
Power ON sequence:

1. Power ON V_{DD} .
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least $3\mu s$ (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least $3\mu s$ (t_2). Then Power ON V_{CC} . (1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after $100ms$ (t_{AF}).



Power OFF sequence:

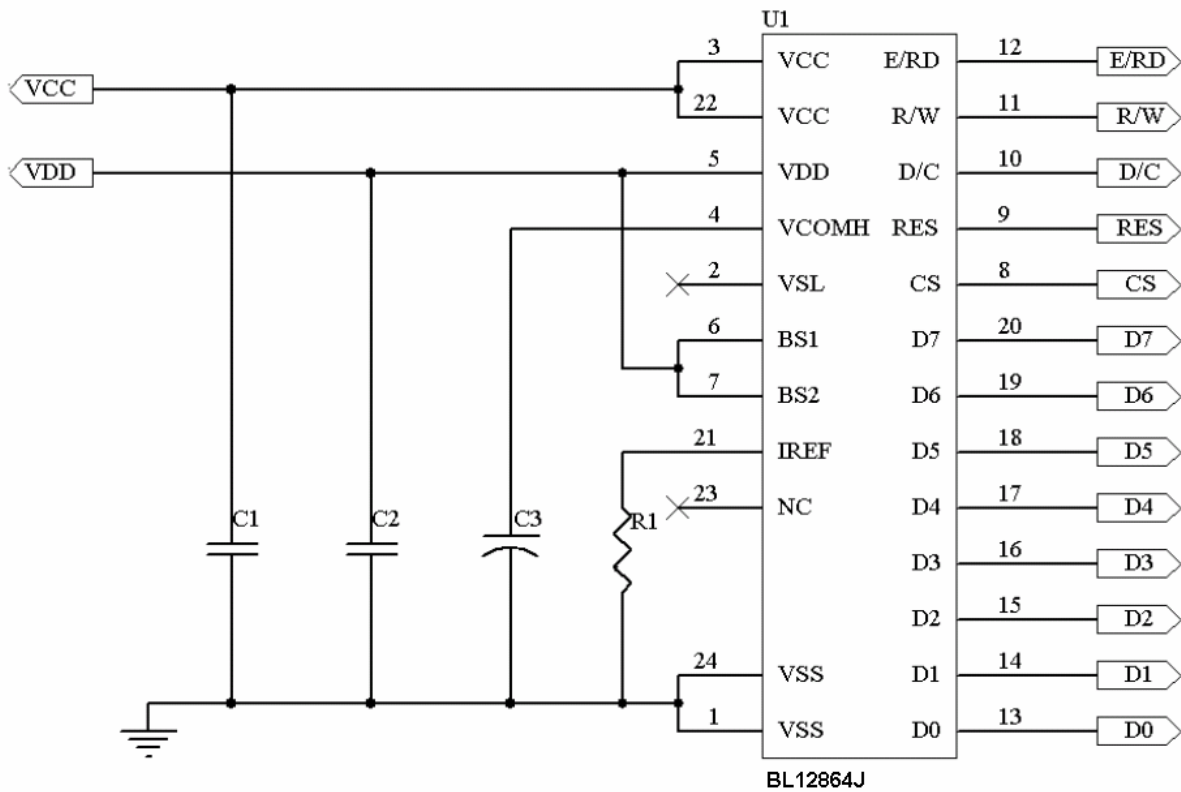
1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC} . (1), (2)
4. Wait for t_{OFF} . Power OFF V_{DD} . (where Minimum $t_{OFF}=80ms$, Typical $t_{OFF}=100ms$)



Note:

- (1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} , V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
- (2) V_{CC} should be disabled when it is OFF.

9.1 Application circuit



Recommend Components:

C1: 2.2uF/25V (0805)

C2: 1uF/16V (0603)

C3: 4.7uF/25V (TANTALUM or Solid Tantalum 4.7uF/25V/A Case (Vishay 572D))

R1: 1M ohm/1% (0805)

Note: This circuit is for 8080 interface

10. Display Control Instruction

Command Table

(D/C# = 0, R/W# (WR#) = 0, E (RD#) = 1) unless specific setting is stated

Fundamental Command Table											
D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	15 A[5:0] B[5:0]	0 * *	0 * *	0 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Column Address	Second command A[5:0] sets the column start address from 0-63, POR = 00h Third command B[5:0] sets the column end address from 0-63, RESET = 3Fh
0 0 0	75 A[6:0] B[6:0]	0 * *	1 A ₆ B ₆	1 A ₅ B ₅	1 A ₄ B ₄	0 A ₃ B ₃	1 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Row address	Second command A[6:0] sets the row start address from 0-79, RESET = 00h Third command B[6:0] sets the row end address from 0-79, RESET = 4Fh
0 0	81 A[6:0]	1 *	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Contrast Current	Double byte command to select 1 out of 128 contrast steps. Contrast increases as level increase The level is set to 40h after RESET
0	84-86	1	0	0	0	0	1	X ₁	X ₀	Set Current Range	84h = Quarter Current Range (RESET) 85h = Half Current Range 86h = Full Current Range
0 0	A0 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Re-map	A[0]=0, Disable Column Address Re-map (RESET) A[0]=1, Enable Column Address Re-map A[1]=0, Disable Nibble Re-map (RESET) A[1]=1, Enable Nibble Re-map A[2]=0, Horizontal Address Increment (RESET) A[2]=1, Vertical Address Increment A[4]=0, Disable COM Re-map disable (RESET) A[4]=1, Enable COM Re-map A[5]=0, Reserved (RESET) A[5]=1, Reserved A[6]=0, Disable COM Split Odd Even (RESET) A[6]=1, Enable COM Split Odd Even
0 0	A1 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Display Start Line	Set display RAM display start line register from 0-79 Display start line register is reset to 00h after RESET
0 0	A2 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Display Offset	Set vertical scroll by COM from 0-79 The value is reset to 00H after RESET
0	A4-A7	1	0	1	0	0	X ₂	X ₁	X ₀	Set Display Mode	A4h = Normal Display (RESET) A5h = Entire Display ON,

Fundamental Command Table											
D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
											all pixels turns ON in GS level 15 A6h = Entire Display OFF, all pixels turns OFF A7h = Inverse Display
0 0	A8 A[6:0]	1 *	0 A ₆	1 A ₅	0 A ₄	1 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX, A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX : A[6:0] = 78 represents 79MUX A[6:0] = 79 represents 80MUX
0 0	AD A[1:0]	1 *	0 *	1 *	0 *	1 *	1 *	0 1	1 A ₀	Set Master Configuration	A[0] = 0, Select external V _{CC} supply A[0] = 1, Reserved (RESET) Note (1) Bit A[0] must be set to 0b after RESET. (2) The setting will be activated after issuing Set Display ON command (AFh)
0	AE	1	0	1	0	1	1	1	0	Set Display ON	AEh = Display OFF (Sleep mode) (RESET)
0	AF	1	0	1	0	1	1	1	1	Set Display OFF	AFh = Display ON
0 0	B0 A[5:0]	1 *	0 *	1 A ₅	1 A ₄	0 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Pre-charge Compensation Enable	A[5:0] = 08h (RESET) A[5:0] = 28h, Enable pre-charge compensation
0 0 0	B1 A[3:0] A[7:4]	1 * A ₇	0 * A ₆	1 * A ₅	1 * A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLKs, RESET = 3DCLKS = 3h A[7:4] = P2, phase 2 period of 1-15 DCLKs, RESET = 5DCLKS = 5h Note (1) 0 DCLK is invalid in phase 1 & phase 2
0 0	B2 A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Set Row Period (set frame frequency)	The next command sets the number of DCLKs, K, per row between 2-158 DCLKS RESET = 37DCLKS = 25h The K value should be set as K = P1+P2+GS15 pulse width (RESET: 3+5+29DCLKS)
0 0 0	B3 A[3:0] A[7:4]	1 * A ₇	0 * A ₆	1 * A ₅	1 * A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Display Clock Divide Ratio / Oscillator Frequency	The lower nibble (A[3:0]) of the next command defines the divide ratio (D) of display clock (DCLK) Divide ratio (D)=A[3:0]+1 (A[3:0]RESET is 0001b, i.e. divide ratio (D) = 2)

Fundamental Command Table												
D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	
											The higher nibble (A[7:4]) of the next command sets the Oscillator Frequency Oscillator Frequency increases with the value of A[7:4] and vice versa Range: 0000b~1111b RESET= 0100b represents 655KHz, typical step value: 5% of previous value	
0 0	B4 A[2:0]	1 *	0 *	1 *	1 *	0 *	1 A ₂	0 A ₁	0 A ₀	Set Pre-charge Compensation Level	A[2:0] = 0 (RESET) A[2:0] = 3h, Recommended level	
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	B8 A[2:0] B[2:0] B[6:4] C[2:0] C[6:4] D[2:0] D[6:4] E[2:0] E[6:4] F[2:0] F[6:4] G[2:0] G[6:4] H[2:0] H[6:4]	1 * * * * * * * * * * * * * * * * * * *	0 * * B ₆ * * * * * * * * * * * * * * * * *	1 * * B ₅ * * * * * * * * * * * * * * * * *	1 * * B ₄ * * * * * * * * * * * * * * * * * *	1 * * * * * * * * * * * * * * * * * * *	0 * * * * * * * * * * * * * * * * * * *	0 * * * * * * * * * * * * * * * * * * *	0 A ₂ B ₂ C ₂ C ₆ D ₂ E ₂ F ₂ G ₂ H ₂	0 A ₁ B ₁ C ₁ C ₅ D ₁ E ₁ F ₁ G ₁ H ₁	0 A ₀ B ₀ C ₀ * * * * * * * * * * * * * * * * * *	Set Gray Scale Table The next eight bytes of command set the gray scale level of GS1-15 as below: A[2:0] = Gray scale level of GS1, RESET=1 B[2:0] = Gray scale level of GS2, RESET=1 B[6:4] = Gray scale level of GS3, RESET=1 C[2:0] = Gray scale level of GS4, RESET=1 C[6:4] = Gray scale level of GS5, RESET=1 D[2:0] = Gray scale level of GS6, RESET=1 D[6:4] = Gray scale level of GS7, RESET=1 E[2:0] = Gray scale level of GS8, RESET=1 E[6:4] = Gray scale level of GS9, RESET=1 F[2:0] = Gray scale level of GS10, RESET=1 F[6:4] = Gray scale level of GS11, RESET=1 G[2:0] = Gray scale level of GS12, RESET=1 G[6:4] = Gray scale level of GS13, RESET=1 H[2:0] = Gray scale level of GS14, RESET=1 H[6:4] = Gray scale level of GS15, RESET=1
0 0	BC A[7:0]	1 A ₇	0 A ₆	1 A ₅	1 A ₄	1 A ₃	1 A ₂	0 A ₁	0 A ₀	Set Precharge Voltage	Second command A[7:0] sets the precharge voltage level, A[7:0] 1xxxxxxx connects to V _{COMH} (RESET) 001xxxxx 1.0 * V _{REF} 00000000 0.51 * V _{REF} 00000001 0.52 * V _{REF} 00011111 0.84 * V _{REF}	
0 0	BE A[4:0]	1 *	0 *	1 0	1 A ₄	1 A ₃	1 A ₂	1 A ₁	0 A ₀	Set V _{COMH} Voltage	Second command A[4:0] sets the V _{COMH} voltage level , A[4:0] 00000 0.51 * V _{REF} 00001 0.52 * V _{REF} 11101 0.81 * V _{REF} (RESET) 11110 0.82 * V _{REF} 11111 0.84 * V _{REF}	
0 0	BF A[3:0]	1 *	0 *	1 *	1 *	1 A ₃	1 A ₂	1 A ₁	1 A ₀	Set Segment Low Voltage (VSL)	Second command A[3:0] sets the VSL voltage as follow: A[3:0] = 0010 kept VSL pin NC A[3:0] = 1110 (RESET) connect a capacitor between VSL pin and V _{SS}	
0	E3	1	1	1	0	0	0	0	1	1	NOP Command for No Operation	

Graphic acceleration command

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated

Graphic acceleration command										Command	Description
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0		
0	23	0	0	1	0	0	0	1	1	Graphic Acceleration Command Options	A[0] = 0b: Disable Fill rectangle A[0] = 1b: Enable Fill rectangle (RESET)
0	A[4:0]	*	*	*	A ₄	*	*	A ₁	A ₀		A[1] = 0b: Disable x-wrap(RESET) A[1] = 1b: Enable wrap around in x-direction during copying and scrolling A[4] = 0b: Disable reverse copy (RESET) A[4] = 1b: Enable reverse during copying.
0	24	0	0	1	0	0	1	0	0	Draw Rectangle	A[5:0]: Column Address of Start
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		B[6:0]: Row Address of Start
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		C[5:0]: Column Address of End
0	C[5:0]	*	*	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		D[6:0]: Row Address of End
0	D[6:0]	*	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		E[7:0]: Set Gray scale pattern
0	E[7:0]	E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		E[7:0] This byte is divided into two nibbles. The most significant 4 bits represent the gray scale level of the left pixel of each group. The least significant 4 bits represent the gray scale level of the right pixel of each group. Please refer to Figure 33 for the gray scale pattern setting examples.
											Note: (1) 0 ≤ A < C ≤ 63 (2) 0 ≤ B < D ≤ 79
0	25	0	0	1	0	0	1	0	1	Copy	A[5:0]: Column Address of Start
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		B[6:0]: Row Address of Start
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		C[5:0]: Column Address of End
0	C[5:0]	*	*	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		D[6:0]: Row Address of End
0	D[6:0]	*	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		E[5:0]: Column Address of New Start
0	E[5:0]	*	*	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		F[6:0]: Row Address of New Start
0	F[6:0]	*	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀		Note: (1) 0 ≤ A < C ≤ 63 (2) 0 ≤ B < D ≤ 79 (3) 0 ≤ E ≤ 63 (4) 0 ≤ F ≤ 79

Graphic acceleration command											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	26	0	0	1	0	0	1	1	0	Horizontal Scroll	A[5:0]: 1~63 horizontal offset in number of 2~127 column 0 no horizontal scroll
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		B[6:0]: 2~80 number of rows to be H-scrolled
0	B[6:0]	*	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		C[1:0]: scrolling time interval
0	C[1:0]	*	*	*	*	*	*	C ₁	C ₀		00b 12 frames 01b 64 frames 10b 128 frames 11b 256 frames
											Note: (1) Scrolling operates during display ON. (2) The parameters should not be changed after scrolling is activated
0	2E	0	0	1	0	1	1	1	0	Stop Moving	This command deactivates the scrolling action. Note (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Start Moving	This command activates the scrolling function according to the setting done by Horizontal Scroll command 26h. Note (1) The “wrap around in x-direction” function must be enabled before scrolling start. i.e. Bit A{1} of command 23h must be set to 1b before issuing 2F command.

Read Command Table

(D/C#=0, R/W# (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Status Register Read	D7 = 0.reserved D7 = 1.reserved D6 = 0.indicates the display is ON D6 = 1.indicated the display is OFF D5 = 0.reserved D5 = 1.reserved D4 = 0.reserved D4 = 1.reserved
--	----------------------	---

Note

(1) Patterns other than that given in Command Table are prohibited to enter to the chip as a command; Otherwise, unexpected result will occur

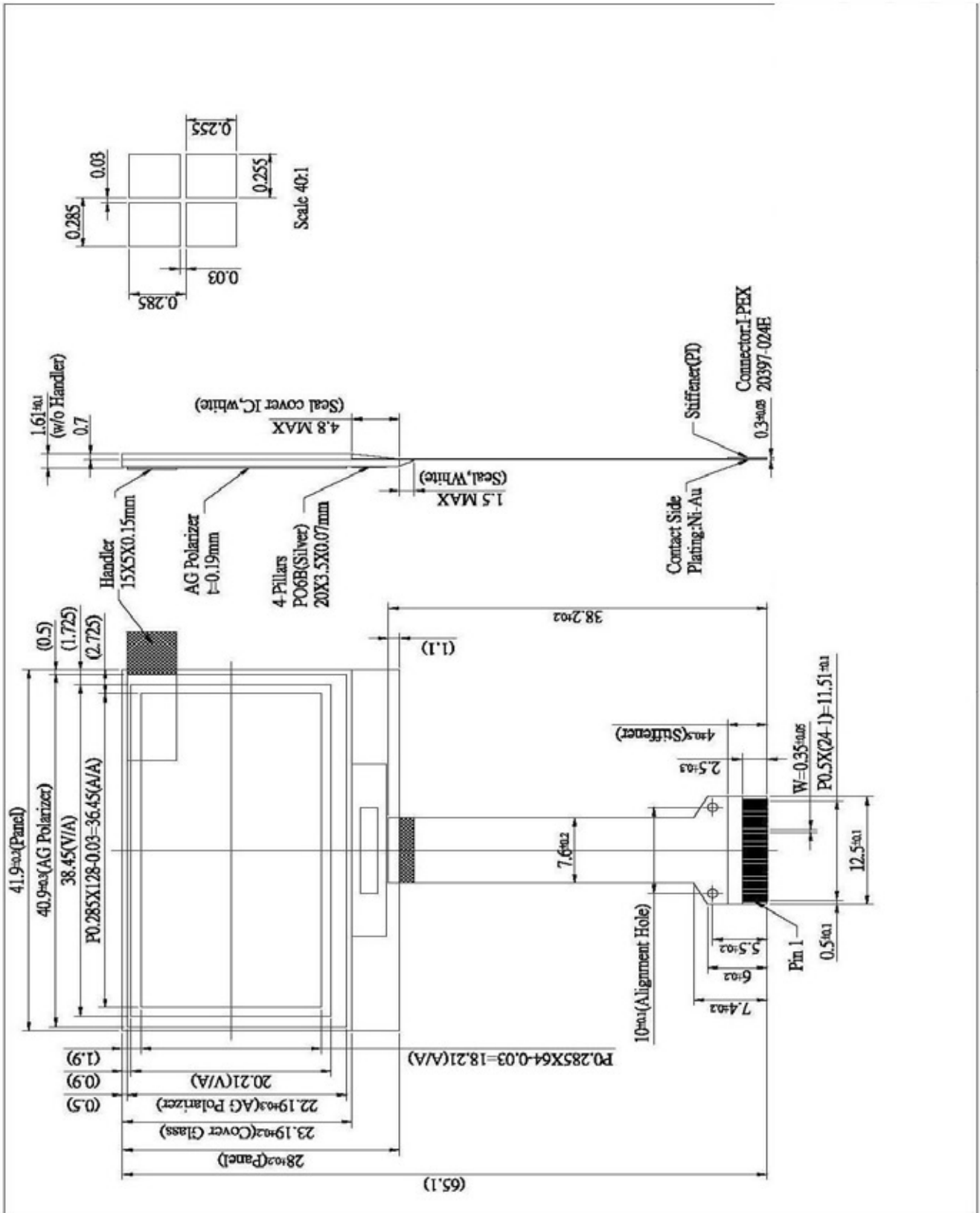
11. Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	—
2	High temp. (Operation)	70°C, 120hrs	—
3	Low temp. (Operation)	-40°C, 120hrs	—
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	—
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	—
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	—
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and faces Cycles: 1	—
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	—

12. Appendix

12.1 Drawing



X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [LED Displays & Accessories](#) category:

Click to view products by [Display Elektronik](#) manufacturer:

Other Similar products are found below :

[LTC-2721WC](#) [LTC-4624JD](#) [LTC-4627G](#) [LTC-4627WC](#) [LTD-5021AWC](#) [LTM-8522G](#) [LTP-4323P](#) [LTP-747G](#) [LTS-3361JG-06](#)
[F416SYGWA/S530-E3](#) [EADST040RA2](#) [1668](#) [HT-F196NB-5323](#) [IPD2131-27](#) [SA03-12EWA](#) [LDD-E2802RD](#) [LDD-E306MI](#) [LDQ-N514RI](#)
[LDS-A3506RD](#) [LDS-A3926RI](#) [LDT-M516RI](#) [SC03-12HDB](#) [SI-B9T151550WW](#) [SI-B9V171550WW](#) [SLC-3PF-WL](#) [1624](#) [LTC-2621JD](#)
[LTC-2623WC](#) [LTC-4624P](#) [LTC-4627JD](#) [LTD-2601E](#) [LTD-322G](#) [LTD-482PC](#) [LTP-1457AKR](#) [LTP-3784G-01](#) [LTS-313AP](#) [LTS-4812SKR-](#)
[P](#) [LTS-547AE](#) [LTS-6780P](#) [446010401-3](#) [HV-7W30-6829](#) [CA12240_MINNIE-WWW-MTG-ASSY](#) [DA43-11GWA](#) [LDD-A516RI-17](#) [LDD-](#)
[E305RI](#) [LDQ-M513RI](#) [LDQ-M5204RI-SI](#) [LDQ-N3402RI](#) [LDQ-N3606RI](#) [LDT-M2804RI](#)