DEV-ADC34J22

The DEV-ADC34J22 is a four-channel, 50MSPS ADC Module designed to integrate with Altera's HSMC standard. The DEV-ADC34J22 features TI's new JESD204B compliant ADC34J22 Analog Digital Converter (ADC), with clocking conditioning using TI's LMK04828B jitter cleaner. It provides single-ended DC coupled inputs on two of the four channels through TI's THS4541 850MHz BW fully differential amplifier.
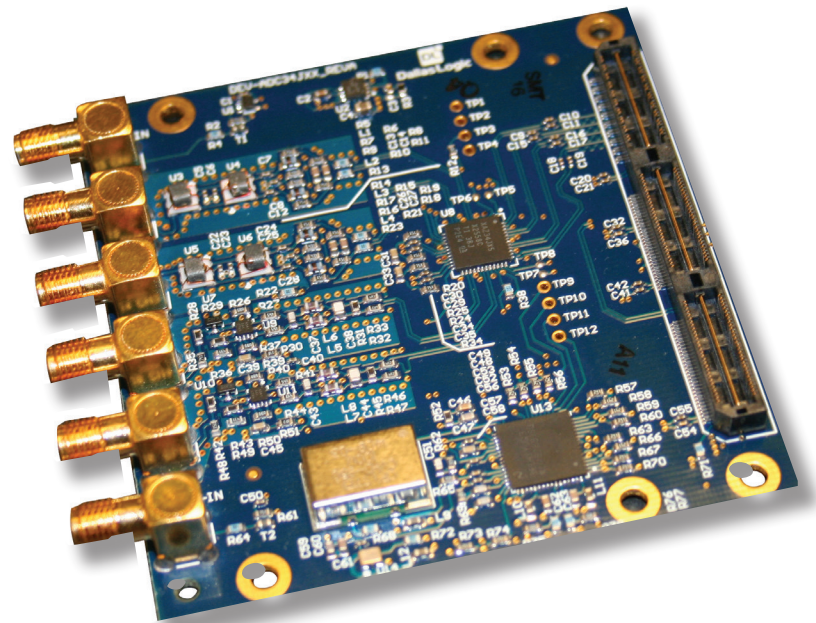
The module offers six front panel SMA connectors: 1 EXT trigger, 1 EXT clock and 4 Analog Input Channels, and an on board 10MHz TCXO for stand -alone clock generation, with a 100MHz VCXO used in conjunction with the LMK04828B for reference clock jitter cleaning. The ADC34J22 and the LMK04828B are completely configurable via Altera's Cyclone V SOC FPGA with embedded ARM Cortex A9 processors. The DEV-ADC34J22 supports a wide range of applications and offers two RF (AC coupled) channels and two Analog (DC coupled) channels.

TEXAS INSTRUMENTS   **DL Dallas Logic**

Completely configurable via Altera's Cyclone V SOC FPGA with embedded ARM Cortex A9 processors.

Board Highlights

> Quad ADC Module supporting JESD204B, Subclass 0 & 1

> Features Texas instruments New ADC34J22 JESD204B ADC

> Showcases JESD204B using Altera's Cyclone V family of FPGAs

> DC coupled capability via Texas Instruments new THS4541 Fully Differential Amplifier (FDA)

> Compatible with Arrow's SOCKIT evaluation module

> Follow up FMC module will be offered Q3'14

Order at parts.arrow.com;
Part No. DEV-ADC34J22

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Board Features

> Texas Instruments ADC34J22 Analog to Digital Converter

> 4 channel, 12bit, 50 MSPS, JESD204B compliant ADC module

> Two RF AC coupled input channels

> Two Analog DC coupled input channels

> External clock input

> External trigger input

> On board TI LMK04828B Dual Loop

> Clock Jitter Cleaner Reference oscillator - 10MHz. TCXO

> 1st Loop VCO - 100MHz. VCXO

> HSMC connector for interfacing with Altera FPGA development boards Supports up to four JESD204B lanes

> JESD204B Sub-class 0 & 1 compatible

> SPI control interfaces for both the ADC34J22 and LMK04828B devices

> Reference design available for Arrow's SOCkit development board

> VHDL design files including MTI's JESD core instantiation

> Module is configured at power-up by the SOC's ARM processor

AC Coupled RF Front End

RF Front End Features:

> Transformer coupled single ended to differential conversion

> Available on Channels 1 & 2

> RF Front End Specifications: Input range +/- 1.0V (2V p-p)

> 0.5 - 200 MHz input bandwidth

Applications Include:

> IF Software Defined Radio (SDR)
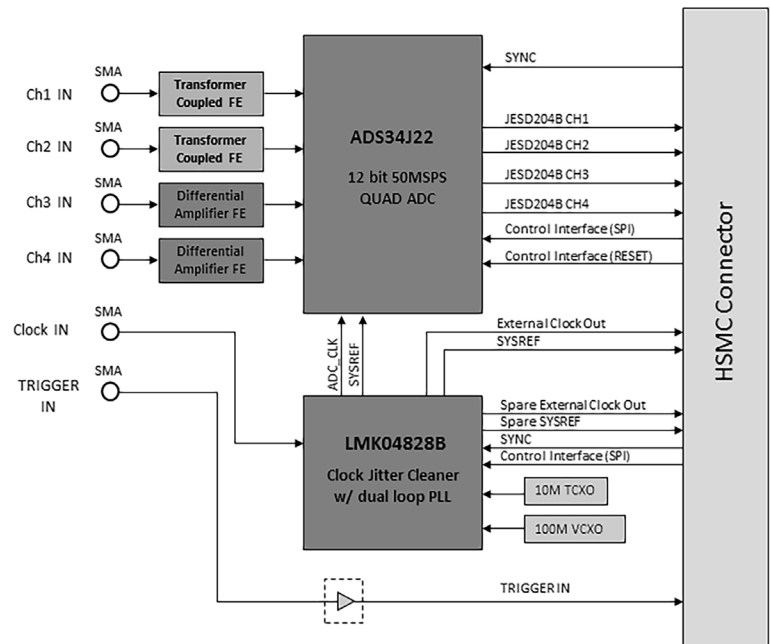
> Instrumentation

> Radar

> Portable Test Equipment

Two Analog DC Coupled Input Channels

Analog Front End Features:

> Single Ended to Differential Amplifier with G=2 V/V Available on Channels 3 & 4

> Analog Front End Specifications:

> Input range +/- 0.5 V i.e. 1 Vp-p

> DC - 15 MHz input bandwidth

Applications Include:

> Baseband Software Defined Radio (SDR)

> Instrumentation

> Medical Imaging

In Person

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