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Renesas Electronics Corporation

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User's Manual

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H8/38076R Group

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer
H8 Family/H8/300H Super Low Power Series

H8/38076RF
H8/38076R
H8/38075R
H8/38074R
H8/38073R

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are in their open states, intermediate levels are induced by noise in the vicinity, a
through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughc
chip and a low level is input on the reset pin. During the period where the states
undefined, the register settings and the output state of each pin are also undefine
your system so that it does not malfunction because of processing while it is in t
undefined state. For those products which have a reset function, reset the LSI im
after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test re
may have been be allocated to these addresses. Do not access these registers; the
operation is not guaranteed if they are accessed.

manual.

5. Contents
6. Overview
7. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

   The configuration of the functional description of each module differs according to th
   module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Eac
includes notes in relation to the descriptions given, and usage notes are given, as required
final part of each section.

8. List of Registers
9. Electrical Characteristics
10. Appendix
11. Index

Objective: This manual was written to explain the hardware functions and electrica characteristics of the H8/38076R Group to the target users.
Refer to the H8/300H Series Software Manual for a detailed description instruction set.

Notes on reading this manual:

- In order to understand the overall functions of the chip
  Read the manual according to the contents. This manual can be roughly categorized on the CPU, system control functions, peripheral functions, and electrical characteris
- In order to understand the details of the CPU's functions
  Read the H8/300H Series Software Manual.
- In order to understand the details of a register when its name is known
  Read the index that is the final part of the manual to find the page number of the ent register. The addresses, bits, and initial values of the registers are summarized in sec List of Registers.

Example: Register name: The following notation is used for cases when the s similar function, e.g. serial communication interfac implemented on more than one channel:
XXX_N (XXX is the register name and N is the ch number)

Bit order: The MSB is on the left and the LSB is on the right.

5. When the on-chip debugging emulator is used, address breaks can be set as either ava
the user or for use by the on-chip debugging emulator. If address breaks are set as bei
by the on-chip debugging emulator, the address break control registers must not be ac
6. When the on-chip debugging emulator is used, $\overline{\text{NMI}}$ is an input pin, P16 and P36 are i
pins, and P37 is an output pin.
7. When on-board programming/erasing is performed in boot mode, the SCI3 (P41/RXD
P42/TXD) is used.
8. When using the on-chip debugging emulator, set the FROMCKSTP bit in clock halt r
to 1.

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H8/38076R Group manuals:

Document Title	Docume
H8/38076R Group Hardware Manual	This man
H8/300H Series Software Manual	REJ09B0

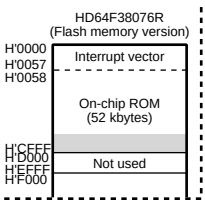
User's manuals for development tools:

Document Title	Docume
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual	REJ10B0
H8S, H8/300 Series Simulator/Debugger User's Manual	ADE-702
H8S, H8/300 Series High-performance Embedded Workshop 3 Tutorial	REJ10B0
H8S, H8/300 Series High-performance Embedded Workshop 3 User's Manual	REJ10B0

1.2 Internal Block Diagram Figure1.1 Internal Block Diagram of H8/38076R Group	3	Note 2 amended 2. The SCK4, SI4, SO4, and $\overline{\text{NMI}}$ pins are not available on-chip.
1.4 Pin Functions Table 1.4 Pin Functions	19	Table amended

		Pin No.					
Type	Symbol	FP-80A, TFP-80C	TLP-85V	Pad No.*1	Pad No.*2	I/O	Functions
16-bit timer pulse unit (TPU)	TIOCA1	80	A3	81	80	I/O	Pins for the TGR1A input or output compare PWM output.
	TIOCB1	1	B1	1	1	Input	Pins for the TGR1B input.
	TIOCA2	2	C1	2	2	I/O	Pins for the TGR2A input or output compare PWM output.
	TIOCB2	3	B2	3	3	Input	Pins for the TGR2B input.

2.1 Address Space and Memory Map Figure 2.1 Memory Map	24	Figure amended



Note amended

When the on-chip debugging emulator is used, the area H'C000 to H'CFFF and from H'F380 to H'F77F are used by the emulator and not accessible by the user.

3.2 Reset	61, 62	Replaced
3.3 Interrupts	63	Description amended … and WKP7 to WKP0) and 25 internal interrupts (for th memory version) or 24 internal … ... The interrupt controller can set interrupts other than N one of three mask levels in order to control multiple inter The interrupt priority registers A to E (IPRA to IPRE) of t interrupt controller set the interrupt mask level.
3.5.1 Notes on Stack Area Use	66	Description amended To save register values, use PUSH.W Rn (MOV.W Rn, or PUSH.L ERn (MOV.L ERn, @–SP). To restore regist use POP.W Rn (MOV.W @SP+, Rn) or POP.L ERn (MO @SP+, ERn). During interrupt exception handling or when an RTE inst executed, CCR contents are saved and restored in word
Section 4 Interrupt Controller 4.1 Features	71	Description amended • Mask levels settable with IPR An interrupt priority register (IPR) is provided for setting mask levels. Three mask levels can be set for each mod all interrupts except NMI and address break.

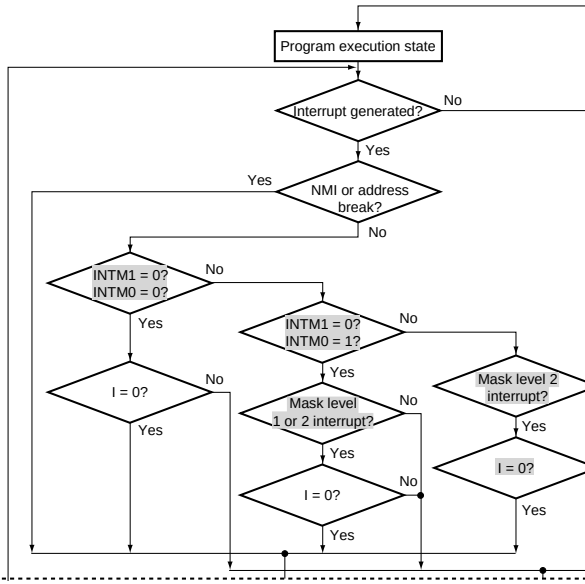
Register (INTM)		(Before) Priority level → (After) Mask level
4.4.1 External Interrupts	84	(2) WKP7 to WKP0 Interrupts ... The interrupt mask level can be set by IPR. (3) IRQ4, IRQ3, IRQ1, and IRQ0 Interrupts ... The interrupt mask level can be set by IPR. (4) IRQAEC Interrupts ... The interrupt mask level can be set by IPR.
4.4.2 Internal Interrupts	85	• The interrupt mask level can be set by IPR.
4.5 Interrupt Exception Handling Vector Table		Description amended ... The lower the vector number, the higher the priority. priority within a module is fixed. Mask levels for Interru than NMI and address break can be modified by IPR.

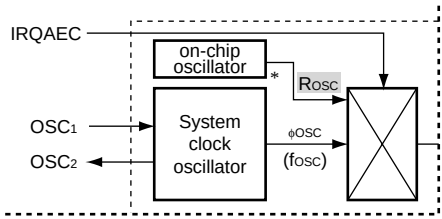
• When the I bit is cleared to 0, the INTM1 bit is cleared and the INTM0 bit is set to 1, interrupt requests with ma are held pending.

• When the I bit, INTM1 bit, and INTM0 bit are all cleare all interrupt requests are accepted.

3. If contention occurs between interrupts that are not he pending by the INTM1 and INTM0 bits in the INTM regis the I bit in CCR, the interrupt with the highest priority as table 4.2 is selected, regardless of the IPR setting.

Figure 4.2 Flowchart of Procedure Up to Interrupt Acceptance	89	Figure amended



Response Times (States)		Note 1 amended 1. One state for internal interrupts and two states for ex interrupts.
4.7.2 Instructions that Disable Interrupts	94	Description amended When an interrupt request is generated, an interrupt is sent to the CPU after the interrupt controller has deterr mask level.
Section 5 Clock Pulse Generators Figure 5.1 Block Diagram of Clock Pulse Generators (Masked ROM Version) (2)	96	Figure amended 
5.2 System Clock Generator Figure 5.2 Typical Connection to Crystal Resonator	99	Figure amended **Frequency** | **Manufacturer** | **Product Type** | **C_1, C_2 Recommendation Val** 4.19 MHz | Kyocera Kinseki Corporation | HC-491U-S | 22 pF ±20%
5.2.4 On-Chip Oscillator Selection Method (Supported only by the Masked ROM Version)	100	Description amended ... The setting takes effect when the rest is cleared. Wh chip oscillator is selected, ...

kHz/38.4-kHz Crystal Resonator		R_s = 35 kΩ (max.)
	102	Description added Notes on Use of Subclock Generator Circuit The drive capacity of the subclock generator circuit is lim order to reduce current consumption when operating in t subclock mode. As a result, there may not be sufficient a margin to accommodate some resonators. Be sure to se resonator with an equivalent series resistance (R_s) corre to that shown in figure 5.6.
5.3.3 External Clock Input Method	103	Title amended
5.4.1 Prescaler S		Description amended The output from prescaler S is shared by the on-chip pe modules. In active (medium-speed) mode and sle (medium-speed) mode,
5.5.3 Definition of Oscillation Stabilization Wait Time	106, 107	Replaced
5.5.6 Note on Using Power-On Reset Circuit	108	Description amended The LSI's internal power-on reset circuit can be adjusted connecting an external capacitor to the $\overline{\text{RES}}$ pin. Adjust capacitance of the external capacitor to ensure sufficien oscillation stabilization time before reset clearing. For de section 21, Power-On Reset Circuit.

4	NESEL	1	R/W	Noise Elimination Sampling Frequency Se The subclock pulse generator generates th signal (ϕ_w) and the system clock pulse gen generates the oscillator clock (ϕ_{OSC}). This b sampling frequency of ϕ_{OSC} when ϕ_w is sam ϕ_{OSC} = 2 to 10 MHz, clear this bit to 0. Set it internal oscillator is used. 0: Sampling rate is ϕ_{OSC}/16. 1: Sampling rate is ϕ_{OSC}/4.
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	Select the operating clock frequency in sul subsleep modes. The values of SA1 and S change if they are written to in subactive m 00: ϕ_w/8 01: ϕ_w/4 1X: ϕ_w/2

6.1.3 Clock Halt Registers 1 and 2 (CKSTPR1 and CKSTPR2) — 113

Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	S4CKSTP*1 *4	1	R/W*1	SCI4 Module Standby SCI4 enters standby mode when this bit is
3	—	1	R/W	Reserved This readable/writable bit is reserved.
2	TFCKSTP	1	R/W	Timer F Module Standby Timer F enters standby mode when this b 0.
1	FROMCKSTP*1 *4	1	R/W*1	Flash Memory Module Standby Flash memory enters standby mode when cleared to 0.

mode						mode (direct transition)		
	0	1	0	*	1	Active (medium-speed) mode (direct transition)	—	—

Table 6.3 Internal State in Each Operating Mode

120

Note amended

Function		Watch Mode	Subactive Mode	Subsleep Mode	Standby Mode
Peripheral modules	RTC	Functioning/ retained*9	Functioning/ retained*9	Functioning/ retained*9	Functioning/ retained*9
	Asynchronous event counter	Functioning*6	Functioning	Functioning	Functioning*6
	Timer F	Functioning/ retained*7	Functioning/retained*7	Functioning/ retained*7	Retained
	TPU	Retained	Retained	Retained	Retained
	WDT	Functioning*8/ retained	Functioning*8/ retained	Functioning*8/ retained	Functioning*8/ retained
	SCI3/IrDA	Reset	Functioning/ retained*2	Functioning/ retained*2	Reset

Notes:

6. Only incrementing of the external event timer by ECL overflow interrupts operate.

7. Functioning if ϕw/4 is selected as an internal clock. H retained otherwise.

8. Functioning if the on-chip oscillator is selected.

9. Functioning if the internal time keeping time-base fun selected and retained if the interval timer is selected.

		transition takes place and a transition is made instead watch mode. Note: If a direct transition is attempted while the I bit in set to 1, the device remains in sleep or watch mode, a recovery is not possible.
6.3.1 Direct Transition from Active (High-Speed) Mode to Active (Medium-Speed) Mode	125	Description amended Example: When $\phi_{osc}/8$ is selected as the CPU operating clock follow Direct transition time = (2 + 1) × tosc + 14 × 8tosc = 115t
6.3.2 Direct Transition from Active (High-Speed) Mode to Subactive Mode	126	Description amended Example: When $\phi_w/8$ is selected as the CPU operating clock following t Direct transition time = (2 + 1) × 1tosc + 14 × 1tsubcyc = 3tos
6.3.3 Direct Transition from Active (Medium-Speed) Mode to Active (High-Speed) Mode		Description amended Example: When $\phi_{osc}/8$ is selected as the CPU operating clock befo Direct transition time = (2 + 1) × 8tosc + 14 × tosc = 38t
6.3.4 Direct Transition from Active (Medium-Speed) Mode to Subactive Mode	127	Description amended Example: When ϕosc/8 is selected as the CPU operating clock before tran Direct transition time = (2 + 1) × 8tosc + 14 × 1tsubcyc = 24tos
6.3.5 Direct Transition from Subactive Mode to Active (High-Speed) Mode		Description amended Example: When ϕw/8 is selected as the CPU operating clock before transiti time = 8192 states Direct transition time = (2 + 1) × 8tw + (8192 + 14) × tosc = 24tw
6.3.6 Direct Transition from Subactive Mode to Active (Medium-Speed) Mode	128	Description amended Example: When ϕw/8 is selected as the CPU operating clock before transiti selected as the CPU operating clock following transition, and the 8,192 states Direct transition time = (2 + 1) × 8tw + (8192 + 14) × 8tosc = 24tw + 65648tosc

9.1.3 Pin Functions 161 Description amended

• P15/TIOCB2 pin

TPU Channel 2 Setting	Next table (1)	Next table (2)	Next table (3)		
PCR15	—	0	1	0	
Pin Function	—	P15 input pin	P15 output pin	P15 input pin	P
				TIOCB2 inpu	

Note: * When the MD1 and MD0 bits are set to B'00 and the IOB3 bit to 1, the pin fu becomes the TIOCB2 input pin.
Clear PCR15 to 0 when using TIOCB2 as an input pin.

TPU Channel 2 Setting	(2)	(3)	(1)	
MD1, MD0	B'00			B'10, B'01, B
IOB3 to IOB0	B'0000	B'1xxx	B'0001 to B'0111	B'xxxx
CCLR1, CCLR0	B'xx			
Output Function	—		Setting prohibited	

[Legend] x: Don't care.

	B'1xxx	B'0101 to B'0111			
CCLR1, CCLR0	—	—	—	—	Other th B'01
Output Function	—	Output compare output	—	PWM mode 1* output	PWM mode output

[Legend] x: Don't care.

Note: * The output of the TIOCB2 pin is disabled.

163 • P13/TIOCB1/TCLKB pin

TPU Channel 1 Setting	Next table (1)	Next table (2)		Next tab	
PCR13	—	0	1	0	
Pin Function	—	P13 input pin	P13 output pin	P13 input pin	
				TIOCB1 inp	
		TCLKB input pin*			

Note: * When the TPSC2 to TPSC0 bits in TCR_1 or TCR_2 are set to B'101, the becomes the TCLKB input pin.
Clear PCR13 to 0 when using TCLKB as an input pin.

TPU Channel 1 Setting	(2)	(3)	(1)	
MD1, MD0	B'00			B'10, B'01,
IOB3 to IOB0	B'0000	B'1xxx	B'0001 to B'0111	B'xxxx
CCLR1, CCLR0	B'xx			
Output Function	—	Setting prohibited		

[Legend] x: Don't care.

164 • P12/TIOCA1/TCLKA pin

Notes: 1. When the MD1 and MD0 bits are set to B'00 and the IOA3 bit to 1, the pin becomes the TIOCA1 input pin.
Clear PCR12 to 0 when using TIOCA1 as an input pin.

2. When the TPSC2 to TPSC0 bits in TCR_1 or TCR_2 are set to B'100, the becomes the TCLKA input pin.
Clear PCR12 to 0 when using TCLKA as an input pin.

from the TXD32 output pin.

• P31/RXD32/SDA pin

The pin function is switched as shown below according to the combination of the P
PCR3, ICE bit in ICCR1, and RE bit in SCR32.

ICE	0			
RE	0		1	
PCR31	0	1	x	
Pin Function	P31 input pin	P31 output pin	RXD32 output pin	SD

[Legend] x: Don't care.

• P30/SCK32/TMOW pin

The pin function is switched as shown below according to the combination of the TM
in PMR3, PCR30 bit in PCR3, CKE 1 and CKE 0 bits in SCR32, and COM b

TMOW	0					
CKE 1	0				1	
CKE 0	0			1	x	
COM	0		1	x	x	
PCR30	0	1	x		x	
Pin Function	P30 input pin	P30 output pin	SCK32 output pin		SCK32 input pin	TMOW p

[Legend] x: Don't care.

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	175	• P40/SCK31/TMIF pin

TMIF	0						
CKE1	0				1		
CKE0	0			1	0	1	
COM	0		1	x	x	x	
PCR40	0	1	x		x	x	
Pin Function	P40 input pin	P40 output pin	SCK31 output pin		SCK31 input pin	Setting prohibited	TMI

[Legend] x: Don't care.

9.8.4 Pin Functions	190	Description amended

• P92/$\overline{\text{IRQ4}}$ pin

IRQ4	0		1	
PCR92	0	1	0	
Pin Function	P92 input pin	P92 output pin	$\overline{\text{IRQ4}}$ input pin	

9.9.3 Pin Functions	192, 193	Replaced
9.10.3 Pin Functions	197	Description amended

• PB2/AN2/$\overline{\text{IRQ3}}$ pin

IRQ3	0		1
CH3 to CH0	Other than B'0110	B'0110	x
Pin Function	PB2 input pin	AN2 input pin	$\overline{\text{IRQ3}}$ input p

[Legend] x: Don't care.

• PB1/AN1/$\overline{\text{IRQ1}}$ pin

IRQ1	0		1
CH3 to CH0	Other than B'0101	B'0101	x
Pin Function	PB1 input pin	AN1 input pin	$\overline{\text{IRQ1}}$ input p

[Legend] x: Don't care.

9.12.1 How to Handle Unused Pin	200	Description amended • If an unused pin is an output pin, it is recommended to in one of the following ways: — Set the output of the unused pin to high and pull it up with an external resistor of approximately 100 kΩ. — Set the output of the unused pin to low and pull it dow GND with an external resistor of approximately 100 kΩ.
10.3.5 RTC Control Register 1 (RTCCR1)	206	Table amended

Bit	Bit Name	Initial Value	R/W	Description
3	—	0	R/W*	Reserved
2 to 0	—	All 0	—	Reserved These bits are always read as 0.

Note: * Only 0 can be written to this bit.

10.3.7 Clock Source Select Register (RTCCSR)	208	Description amended ... A free running counter controls start/stop of counter o by the RUN bit in RTCCR1. When a clock other than φw selected, ...

Bit	Bit Name	Initial Value	R/W	Description
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: φ/8 ..... Free running counter oper
1	RCS1	0	R/W	0001: φ/32 ..... Free running counter oper
0	RCS0	0	R/W	0010: φ/128 ..... Free running counter ope
				0011: φ/256 ..... Free running counter ope
				0100: φ/512 ..... Free running counter ope
				0101: φ/2048 ..... Free running counter ope
				0110: φ/4096 ..... Free running counter ope
				0111: φ/8192 ..... Free running counter ope
				1000: φw/4 ..... RTC operation Settings other than the above are prohibited.

		If an OCRFL write and compare match signal generati simultaneously, the compare match signal is invalid. H compare match signal may or may not be generated w written data and the counter value match. ...
	227	Description amended (2) TCFL, OCRFL If an OCRFL write and compare match signal generatio simultaneously, the compare match signal is invalid. H compare match signal may or may not be generated w written data and the counter value match. ...
11.6.3 Flag Clearing	227	Description amended For ST of (1) formula, please substitute the longest nu execution states in used instruction.
Section 12 16-Bit Timer Pulse Unit (TPU) 12.1 Features	231	Description amended A maximum 2-phase PWM output is possible in combi synchronous operation
Table 12.1 TPU Functions	232	Table amended

Item		Channel 1	Channel 2
I/O pin		TIOCA1	TIOCA2
Input pin		TIOCB1	TIOCB2
Counter clear function		TGR compare match or input capture	TGR compare matc capture
Compare match output	0 output	O	—
	1 output	O	—
	Toggle output	O	—

Pins

Table 12.2 Pin Configuration

Channel	Symbol	I/O	Function
1	TIOCA1	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOCB1	Input	TGRB_1 input capture input
2	TIOCA2	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOCB2	Input	TGRB_2 input capture input

12.3.3 Timer I/O Control Register (TIOR) — 239

Table 12.7 TIOR_1 (Channel 1)

Table amended

Bit 7 IOB3	Bit 6 IOB2	Bit 5 IOB1	Bit 4 IOB0	Description: TGRB_1 Function	Description: TIOCB1 Pin Function
0	0	0	0	Output compare register	Output disabled
			1		Setting prohibited
		1	0		
			1		
	1	0	0		
			1		
		1	0		
			1		

Table 12.8 TIOR_2 (Channel 2) — 240

Table amended

Bit 7 IOB3	Bit 6 IOB2	Bit 5 IOB1	Bit 4 IOB0	Description: TGRB_2 Function	Description: TIOCB2 Pin Function
0	0	0	0	Output compare register	Output disabled
			1		Setting prohibited
		1	0		
			1		
	1	0	0		
			1		
		1	0		
			1		

Functions

(2) Waveform Output by Compare Match

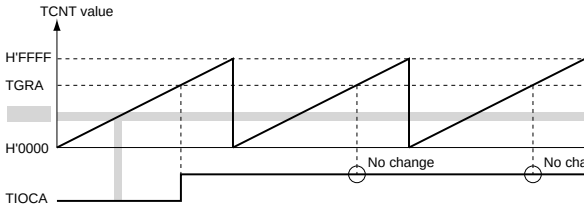
Figure 12.9 shows an example of 1 output.

… and settings have been made such that 1 is output b compare match A . ...

Figure 12.9 Example of 1 Output Operation

253

Figure title and figure amended



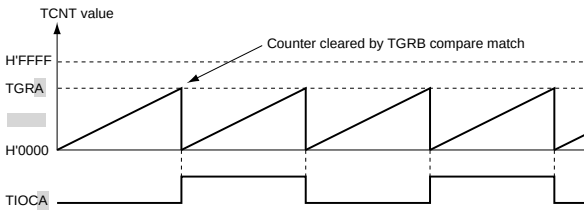
253

Description amended

In this example, TCNT has been designated as a perio counter (with counter clearing on compare match A), a have been made such that the output is toggled by compare match A .

Figure 12.10 Example of Toggle Output Operation

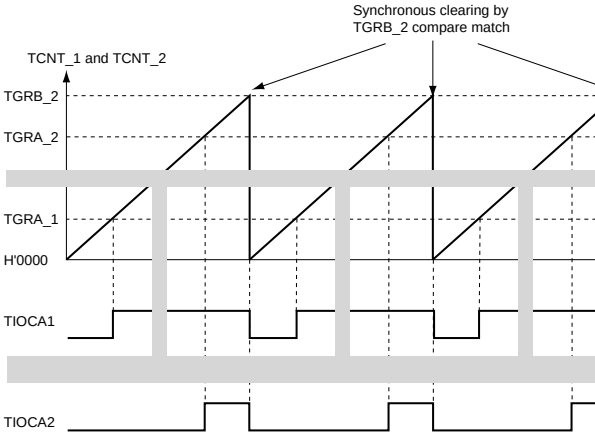
Figure amended



as the TGRB output value.

… TGRB_2 compare match is set as the TCNT clearing
and 0 is set for the initial output value and 1 for the outp
of the other TGR registers (TGRA_1, TGRB_1, and TGR
outputting a 2-phase PWM waveform.

In this case, the value set in TGRB_2 is used as the cyc

Figure 12.19 Example of PWM Mode Operation (2)	262	Figure amended 
13.3.1 Event Counter PWM Compare Register (ECPWCR)	281	Description added Always read or write to this register in word size.
13.3.2 Event Counter PWM Data Register (ECPWDR)	282	Description added Always read or write to this register in word size.

13.3.1 Event Counter L (ECL)

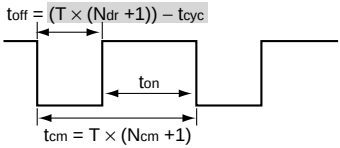
Table amended

Bit	Bit Name	Initial Value	R/W	Description
7	ECL7	0	R	Either the external asynchronous event AE
6	ECL6	0	R	φ/4, or φ/8 can be selected as the input clo
5	ECL5	0	R	ECL can be cleared to H'00 by clearing CR
4	ECL4	0	R	to 0.
3	ECL3	0	R	
2	ECL2	0	R	
1	ECL1	0	R	
0	ECL0	0	R	

13.4.4 Event Counter PWM Operation 290

Figure 13.4 Event Counter Operation Waveform

Figure amended



t_{on}: Clock input enable ti
t_{off}: Clock input disable ti
t_{cm}: One conversion peri
T: ECPWM input clock
N_{dr}: Value of ECPWDR
Fixed low when N_{dr} =
N_{cm}: Value of ECPWCR
t_{cyc}: System cock (φ) cycl

Table 13.2 Examples of Event Counter PWM Operation 291

Table amended

Clock Source Selection	Clock Source Cycle (T)*	ECPWCR Value (Ncm)	ECPWDR Value (Ndr)	toff = T × (Ndr + 1)	tcm = T × (Ncm + 1)	t
φ/2	0.5 µs	H'7A11	H'16E3	2.92975 ms	15.625 ms	1
φ/4	1 µs	D'31249	D'5859	5.85975 ms	31.25 ms	2
φ/8	2 µs			11.71975 ms	62.5 ms	5
φ/16	4 µs			23.43975 ms	125.0 ms	1
φ/32	8 µs			46.87975 ms	250.0 ms	2
φ/64	16 µs			93.75975 ms	500.0 ms	4

Active (medium-speed), sleep (medium-speed)	(ϕ_{osc}/8)	2 · f_{osc}
	(ϕ_{osc}/16)	f_{osc}
	(ϕ_{osc}/32)	1/2 · f_{osc}
	(ϕ_{osc}/64)	1/4 · f_{osc}

294 Description added

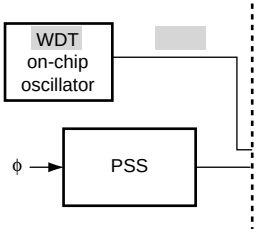
7. If the flash version is used with the IRQAEC pin fixed level, simply switching to a mask ROM version will resul on-chip oscillator being used.

14.1 Features — 295

… or the WDT on-chip oscillator can be selected as timer-counter clock.

Figure 14.1 Block Diagram of Watchdog Timer — 296

Figure amended



14.2.1 Timer Control/Status Register WD1 (TCSRWD1) — 298

Note * added

Bit	Bit Name	Initial Value	R/W	Description
2	WDON	0	R/W	Watchdog Timer On*
				TCWD starts counting up when the WDON b 1 and halts when the WDON bit is cleared to

Note: * When transitioning to the watch mode or standby mode while the main internal o selected (CKS3 = 1) using timer mode register WD (TMWD), make sure to clear 0 to halt operation of TCWD.

14.3.1 Watchdog Timer Mode	302	Description amended … The internal reset signal is output for a period of 256 cycles. …
Figure 14.2 Example of Watchdog Timer Operation		Figure amended (Before) 512ϕ_{OSC} clock cycles → (After) 256ϕ_{OSC} clock cy
14.3.2 Interval Timer Mode Figure 14.3 Interval Timer Mode Operation	303	Figure amended (Before) WT/$\overline{IT}$ = 0 → (After) WT/$\overline{IT}$ = 1 TME = 1
Section 15 Serial Communication Interface 3 (SCI3, IrDA)	305	Description amended The serial communication interface 3 (SCI3) can handl asynchronous and clocked synchronous serial commu or an Asynchronous Communication Interface Adapter The SCI3_1 can transmit and receive IrDA ...
15.3.5 Serial Mode Register (SMR)	312	Table amended

Bit	Bit Name	Initial Value	R/W	Description
2	MP	0	R/W	5-Bit Communication When this bit is set to 1, the 5-bit commun format is enabled. When writing 1 to this b write 1 to bit 5 (RE) at the same time. In a must be written to bit 3 (MPIE) in the seria register (SCR) before writing 1 to this bit.

enabled only, when φw/2 is selected for the
operating clock.

For the relationship between the bit rate reg
and the baud rate, see section 15.3.8, Bit Ra
Register (BRR). n is the decimal representa
value of n in BRR (see section 15.3.8, Bit Ra
Register (BRR)).

15.3.6 Serial Control Register (SCR)	315	Table amended

Bit	Bit Name	Initial Value	R/W	Description
3	MPIE	0	R/W	Reserved

15.3.7 Serial Status Register (SSR)	318	Table amended

Bit	Bit Name	Initial Value	R/W	Description
1	MPBR	0	R	Reserved This bit is read-only and reserved. It cannot to.
0	MPBT	0	R/W	Reserved The write value should always be 0.

N: BRR setting for baud rate generator ($0 \leq N \leq 255$)

OSC: ϕ_{osc} value (Hz)

n: Baud rate generator input clock number (n = 0, 2, or 3)
(The relation between n and the clock is shown in table 15.3)

Table 15.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (1)

320

Table amended

Bit Rate	32.8kHz			38.4kHz			2MHz			2.05	
(bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N
110	—	—	—	—	—	—	2	35	–1.36	2	3
150	—	—	—	0	3	0.00	2	25	0.16	2	2
200	—	—	—	0	2	0.00	2	19	–2.34	3	4
250	—	1	2.50	—	—	—	0	249	0.00	3	3
300	—	—	—	0	1	0.00	0	207	0.16	0	2
600	—	—	—	0	0	0.00	0	103	0.16	0	1
1200	—	—	—	—	—	—	0	51	0.16	0	5
2400	—	—	—	—	—	—	0	25	0.16	0	2

Table 15.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (2)

321

Table amended

Bit Rate	2.4576MHz			3MHz			3.6864MHz				
(bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N
110	3	10	–0.83	2	52	0.50	2	64	0.70	2	7
150	3	7	0.00	2	38	0.16	3	11	0.00	2	5
200	3	5	0.00	2	28	1.02	3	8	0.00	2	3
250	2	18	1.05	2	22	1.90	2	28	–0.69	2	3
300	3	3	0.00	3	4	–2.34	3	5	0.00	2	2
600	3	1	0.00	0	155	0.16	3	2	0.00	0	2

Table 15.5 Maximum Bit Rate for Each Frequency (Asynchronous Mode) — 324 — Table amended

OSC (MHz)	Maximum Bit Rate (bit/s)	Setting n	Setting N
0.0328	512.5	0	0
0.0384	600	0	0
2	62500	0	0

Table 15.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (1) — 325 — Table amended

ϕ	32.8 kHz			38.4 kHz			2 MH		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	E
200	0	20	–2.38	0	23	0.00	2	155	0
250	0	15	2.50	0	18	1.05	2	124	0
300	0	13	–2.38	0	15	0.00	2	103	0
500	0	7	2.50	—	—	—	2	62	–
1k	0	3	2.50	—	—	—	2	30	0

Table 15.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode) (2) — 326 — Table and note amended

ϕ	4 MHz			8 MHz			10 M		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	E
10k	0	99	0.00	0	199	0.00	2	15	–

Note: * Continuous transmission/reception is not possible.

The value set in BRR is given by the following formula:

Active (medium-speed/high-speed) or sleep (medium-speed/high-speed)

$$N = \frac{OSC}{4 \times 2^{2n} \times B} - 1$$

Subactive or subsleep

$$N = \frac{OSC}{8 \times 2^{2n} \times B} - 1$$

B: Bit rate (bit/s)

N: BRR setting for baud rate generator ($0 \le N \le 255$)

OSC: ϕ_{osc} value (Hz)

n: Baud rate generator input clock number (n = 0, 2, or 3)
(The relation between n and the clock is shown in table 15.7.)

				Selects whether the polarity of output data of the TXD31 pin is inverted or not. 0: Output data of TXD31 pin is not inverted. 1: Output data of TXD31 pin is inverted.
0	SCINV0	0	R/W	RXD31 Pin Input Data Inversion Switch Selects whether the polarity of input data of the R pin is inverted or not. 0: Input data of RXD31 pin is not inverted. 1: Input data of RXD31 pin is inverted.

15.4.1 Clock

Table 15.8 Data Transfer Formats (Asynchronous Mode)

332

Table amended

SMR				Serial Data Transfer Format and Frame Length
CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11
0	0	1	0	Setting prohibited
0	0	1	1	Setting prohibited
1	0	1	0	Setting prohibited
1	0	1	1	Setting prohibited

Table 15.9 SMR Settings and Corresponding Data Transfer Formats

333

Table amended

SMR						Data Transfer Format		
Bit 7 COM	Bit 6 CHR	Bit 2 MP	Bit 5 PE	Bit 3 STOP	Mode	Data Length	Parity Bit	Sto Len
0	0	1	0	0	Asynchronous mode	Setting prohibited		
				1				
			1	0		5-bit data	No	1 b
				1				2 b
	1		0	0		Setting prohibited		
				1				
			1	0		5-bit data	Yes	1 b
				1				2 b

15.4.2 SCI3 Initialization

Figure 15.4 Sample SCI3 Initialization Flowchart

335

Figure amended

[4] Wait at least one bit interval, then set the TE bit or R SCR to 1. Setting bits TE and RE enables the TXD31 (and RXD31 (RXD32) pins to be used. Also set the RIE TEIE bits,

15.6 Multiprocessor Communication Function	—	Deleted
15.6.1 Transmission	348	Description amended ... a high-level pulse width of at least 1.41 µs to 1.6 µs c specified.
Figure 15.16 IrDA Transmission and Reception	349	Figure amended (Before) ... 3/16 bit cycle → (After) ... 3/16 bit rate
15.6.2 Reception	349	Description amended If a pulse has a high-level width of less than 1.41 µs, ...
15.8.2 Mark State and Break Sending	354	Description amended Regardless of the value of TE, when the SPCR31 (SPC in SPCR is cleared to 0, the TXD31 (TXD32) pin is used I/O port whose direction (input or output) and level are determined by PCR and PDR. This can be used to set t TXD31 (TXD32) pin to mark state (high level) or send a during serial data transmission. To maintain the commu line at mark state (1) until SPCR31 (SPCR32) in SPCR 1, set both PCR and PDR to 1. As SPCR31 (SPCR32) i is cleared to 0 at this point, the TXD31 (TXD32) pin bec I/O port, and 1 is output from the TXD31 (TXD32) pin. T break during serial transmission, first set PCR to 1 and and then clear SPCR31 (SPCR32) and TE to 0. If TE is to 0 immediately after SPCR31 (SPCR32) is cleared to transmitter is initialized regardless of the current transm state after TE is cleared, and when SPCR31 (SPCR32) cleared to 0 the TXD31 (TXD32) pin becomes an I/O po is output from it.

Register (ADRR)		Always read this register in word size.
18.7 Usage Notes	396	Description amended If a large capacitance is provided externally as a countermeasure, the input load essentially comprises c internal input resistance of 10 kΩ, and the signal sourc impedance can be ignored.
18.7.3 Additional Usage Notes	397	Title amended
19.3.1 LCD Port Control Register (LPCR) Table 19.2 Duty Cycle and Common Function Selection	402	Table amended

Bit 7: DTS1	Bit 6: DTS0	Bit 5: CMX	Duty Cycle	Common Drivers	Notes*
0	0	0	Static	COM1	Leave COM4, COM3, and COM2 i state
		1		COM4 to COM1	COM4, COM3, and COM2 output t waveform as COM1
	1	0	1/2 duty	COM2 to COM1	Leave COM4 and COM3 in open d
		1		COM4 to COM1	COM4 outputs the same waveform COM2 outputs the same waveform
1	0	0	1/3 duty	COM3 to COM1	Leave COM4 in open drain state
		1		COM4 to COM1	Leave COM4 in open drain state
	1	0	1/4 duty	COM4 to COM1	—
		1			

Note: * If SGS3 to SGS0 are set to B'0000, the power supply voltage level of PA0 to PA3 and COM4 is Vcc. If the setting of SGS3 to SGS0 is other than B'0000, the power supply v PA0 to PA3 and COM1 to COM4 is the LCD drive power supply voltage level.

19.3.2 LCD Control Register (LCR) Table 19.4 Frame Frequency Selection	403	Note 3 amended 3. This is the frame frequency in active (medium-speed mode when ϕ_{OSC} = 2 MHz.

V2 voltage = (A + B + C) × 2/3

V3 voltage = (A + B + C) / 3

After monitoring voltage A, set B and C so the
voltage is 3 V.

19.3.5 BGR Control Register (BGRMR)	409	Description amended

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	—	All 0	R/W	Reserved This bit is always read as 0, and only 0 can b it.

19.4.3 3-V Constant-Voltage Power Supply Circuit	417	Note 4 added

4. Initially, the step-up circuit output voltage differs amor individual devices due to production variation. Therefore sure to adjust the settings of the LCD trimming register (individually for each device.

19.5 Usage Notes	420	Added
19.5.1 Pin Processing when No LCD Controller/Driver Is Used		
19.5.2 Pin Processing when No 3 V Constant Voltage Circuit Is Used		

21.2.1 Power-On Reset Circuit	460	Description amended If the $\overline{RES}$ pin rising time is t, the capacitance ($C_{\overline{RES}}$) co to the $\overline{RES}$ pin can be computed using the formula belo information about the on-chip resistor (Rp), see section Electrical Characteristics. The power supply rising time not exceed half the $\overline{RES}$ rising time (t). The $\overline{RES}$ rising should also equal or exceed the oscillation stabilization
23.1 Register Addresses (Address Order)	472	Table amended

Register Name	Abbre-viation	Bit No.	Address	Module Name	Da Bu W
Event counter H	ECH	8	H'FF96	AEC*[1]	8/
Event counter L	ECL	8	H'FF97	AEC*[1]	8/

473

Register Name	Abbre-viation	Bit No.	Address	Module Name	Da Bu W
8-bit timer counter FH	TCFH	8	H'FFB8	Timer F	8/
8-bit timer counter FL	TCFL	8	H'FFB9	Timer F	8/
Output compare register FH	OCRFH	8	H'FFBA	Timer F	8/
Output compare register FL	OCRFL	8	H'FFBB	Timer F	8/

23.2 Register Bits — 477 — Table amended

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPRA	IPRA7	IPRA6	IPRA5	IPRA4	IPRA3	IPRA2	IPRA1	IPRA

479

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SMR3_2	COM	CHR	PE	PM	STOP	MP	CKS1	CKS(
BRR3_2	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR(
SCR3_2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE(
TDR3_2	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR(
SSR3_2	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPB
RDR3_2	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR(

TSR_1_	Initialized	—	—	—	—	—	—	
TCNT_1	Initialized	—	—	—	—	—	—	
TGRA_1	Initialized	—	—	—	—	—	—	
TGRB_1	Initialized	—	—	—	—	—	—	
TCR_2	Initialized	—	—	—	—	—	—	T
TMDR_2	Initialized	—	—	—	—	—	—	
TIOR_2	Initialized	—	—	—	—	—	—	
TIER_2	Initialized	—	—	—	—	—	—	
TSR_2	Initialized	—	—	—	—	—	—	
TCNT_2	Initialized	—	—	—	—	—	—	
TGRA_2	Initialized	—	—	—	—	—	—	
TGRB_2	Initialized	—	—	—	—	—	—	

Register Abbreviation	Reset	Active	Sleep	Watch	Subactive	Subsleep	Standby	M
RTCFLG	—	—	—	—	—	—	—	R
RSECDR	—	—	—	—	—	—	—	
RMINDR	—	—	—	—	—	—	—	
RHRDR	—	—	—	—	—	—	—	
RWKDR	—	—	—	—	—	—	—	
RTCCR1	—	—	—	—	—	—	—	
RTCCR2	—	—	—	—	—	—	—	

Range

24.2.2 DC Characteristics

Table 24.2 DC Characteristics

491

Table amended

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Un
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$*3, $\overline{WKP0}$ to $\overline{WKP7}$, $\overline{IRQ4}$, AEVL, AEVH, TMIF, $\overline{ADTRG}$, SCK32, SCK31, SCK4		0.9V_{CC}	—	V_{CC} + 0.3	V
		$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$		0.9V_{CC}	—	AV_{CC} + 0.3	

24.2.3 AC Characteristics

Table 24.3 Control Signal Timing

497

Table amended

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Un
Oscillation stabilization time	t_{rc}	OSC1, OSC2	Crystal resonator (V_{CC} = 2.7 to 3.6 V)	—	0.8	2.0	ms
			Crystal resonator (V_{CC} = 2.2 to 3.6 V)	—	1.2	3	
			Ceramic resonator (V_{CC} = 2.2 to 3.6 V)	—	20	45	µs
			Ceramic resonator (other than above)	—	80	—	
			Other than above	—	—	50	ms
		×1, ×2	V_{CC} = 2.2 to 3.6 V	—	—	2.0	s
			Other than above	—	4	—	

Table 24.5 I^2C Bus Interface Timing

500

Condition amended

V_{CC} = 1.8 V to 3.6 V, AV_{CC}= 1.8 V to 3.6 V, V_{SS} = 0.0 V,
to +75°C, unless otherwise specified.

Reset Circuit Characteristics

Table 24.8 Power-On Reset Circuit Characteristics

Item	Symbol	Test Condition	Values Min.	Typ.	Max.	Unit
Reset voltage	V_rst		0.7Vcc	0.8Vcc	0.9Vcc	V
Power supply rise time	t_vtr		The Vcc rise time should be shorter than half th $\overline{RES}$ rise time.			
Reset count time	t_out		0.8	—	8.0	µs
Count start time	t_cr		Adjustable by the value of the external capacito of the $\overline{RES}$ pin.			
On-chip pull-up resistance	Rp	Vcc = 3.0 V	60	100	—	kΩ

24.2.8 Flash Memory Characteristics —Preliminary—	504	Condition A amended
Table 24.10 Flash Memory Characteristics		AV_{CC} = 2.7 V to 3.6 V, DV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, ...
		Condition B amended
		AV_{CC} = 1.8 V to 3.6 V, DV_{CC} = 2.2 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, ...
24.4.1 Power Supply Voltage and Operating Range	508	Note 1 amended
(2) Power Supply Voltage and Operating Frequency Range		... the minimum operating frequency (ϕ) is 2 MHz
24.4.2 DC Characteristics	510	Table amended

Table 24.12 DC Characteristics

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{NMI}$, $\overline{WKP0}$ to $\overline{WKP7}$, $\overline{IRQ4}$, AEVL, AEVH, TMIF, $\overline{ADTRG}$, SCK32, SCK31		0.9V_{CC}	—	V_{CC} + 0.3	V
		$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$		0.9V_{CC}	—	AV_{CC} + 0.3	

24.4.3 AC Characteristics

516 Conditions and table amended

Table 24.13 Control Signal Timing

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit
System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	2.0	—	10.0	MHz
			V_{CC} = 1.8 to 3.6 V	2.0	—	4.2	
On-chip oscillator oscillation frequency	R_{OSC}		When on-chip oscillator is selected V_{CC} = 2.7 to 3.6 V	1.0	—	10.0	
			When on-chip oscillator is selected V_{CC} = 1.8 to 2.7 V	0.5	—	4.2	
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	100	—	500 (1000)	ns
			V_{CC} = 1.8 to 3.6 V	238	—	500 (1000)	
On-chip oscillator clock (ϕ_{OSC}) cycle time	t_{ROSC}		When on-chip oscillator is selected V_{CC} = 2.7 to 3.6 V	100	—	1000	
			When on-chip oscillator is selected V_{CC} = 1.8 to 2.7 V	238	—	2000	

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Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit
Oscillation stabilization time	t_{rc}	OSC1, OSC2	Crystal resonator V_{CC} = 2.7 to 3.6 V	—	0.8	2.0	ms
			Crystal resonator V_{CC} = 2.2 to 3.6 V	—	1.2	3.0	
			Ceramic resonator V_{CC} = 2.2 to 3.6 V	—	20	45	µs
			Ceramic resonator Other than above	—	80	—	
			Other than above	—	—	50	ms
			When on-chip oscillator is selected	—	—	100	µs
		X1, X2	V_{CC} = 2.2 to 3.6 V	—	—	2.0	s
			Other than above	—	4	—	

Converter Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, u
otherwise specified.

Table 24.16 A/D Converter Characteristics

522

Item	Symbol	Applicable Pins	Test Condition	Values Min.	Typ.	Max.	Unit
Conversion time			AV_{cc} = 2.7 V to 3.6 V V_{cc} = 2.7 V to 3.6 V	6.2	—	124	µs
			AV_{cc} = 2.0 V to 3.6 V V_{cc} = 2.0 V to 3.6 V	14.7	—	124	
			Other than above	31	—	124	

24.4.6 Power-On Reset Circuit Characteristics

Table 24.18 Power-On Reset Circuit Characteristics

524

Table amended

Item	Symbol	Test Condition	Values Min.	Typ.	Max.	Unit
Reset voltage	V_rst		0.7Vcc	0.8Vcc	0.9Vcc	V
Power supply rise time	t_vtr		The Vcc rise time should be shorter than half the $\overline{RES}$ rise time.			
Reset count time	t_out		0.8	—	4.0	µs
Count start time	t_cr		Adjustable by the value of the external capacitor of the $\overline{RES}$ pin.			
On-chip pull-up resistance	Rp	Vcc = 3.0 V	60	100	—	kΩ

24.4.7 Watchdog Timer Characteristics

Table 24.19 Watchdog Timer Characteristics

525

Table amended

(Before) On-chip oscillator overflow time

(After) WDT on-chip oscillator overflow time

24.7 Recommended Resonators

Table 24.20 Recommended Crystal Resonators

529

Table amended

Frequency (MHz)	Manufacturer	Product Type
4.194	Kyocera Kinseki Corporation	HC-491U-S
10	Kyocera Kinseki Corporation	HC-491U-S

RENESAS

C. Product Code Lineup	581	Table amended

Product Classification				Product Code	Model Marking	Pack (Pac
H8/38076R Group	H8/38076R	Flash memory version	Wide-range specifications			
				HD64F38076RH10W	F38076H10	80 p
				HD64F38076RW10W	F38076W10	80 p
				HD64F38076RLP10WV	F38076RLP10WV	80 p (TLP

Section 2 CPU

Section 3 Exception Handling

Section 4 Interrupt Controller

Section 12 16-Bit Timer Pulse Unit (TPU)

Section 13 Asynchronous Event Counter (AEC)

Section 14 Watchdog Timer

Section 15 Serial Communication Interface 3 (SCI3, IrDA)

Section 16 Serial Communication Interface 4 (SCI4)

Section 17 14-Bit PWM

Section 18 A/D Converter

Section 20 I^2C Bus Interface 2 (IIC2)

Appendix

Section 22 Address Break

Section 24 Electrical Characteristics

RTC (can be used as a free-running counter)

Asynchronous event counter (AEC)

LCD controller/driver

Timer F

16-bit timer pulse unit (TPU)

14-bit PWM

Watchdog timer

SCI (Asynchronous or clocked synchronous serial communication interface)

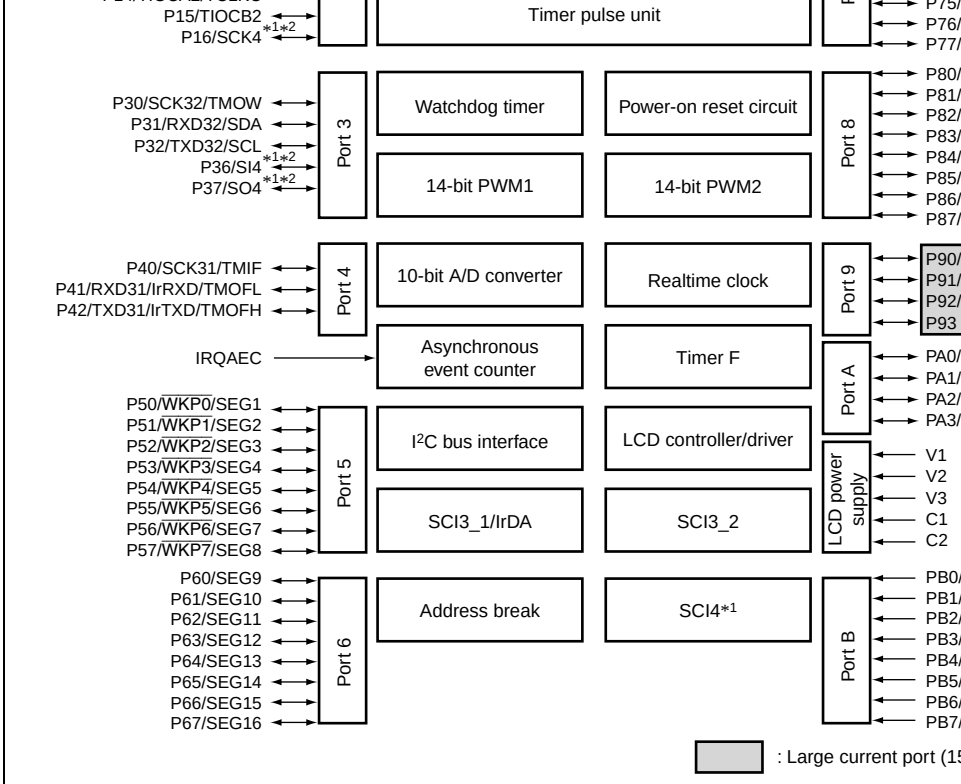
I^2C bus interface (conforms to the I^2C bus interface format that is advocated by Phili
Electronics)

10-bit A/D converter

* 4-kbyte area of 52-kbyte ROM is used for the on-chip debugging emulator. Wh
on-chip debugging emulator is not used, 52-kbyte area is available.

- General I/O ports
  I/O pins: 55 I/O pins, including 4 large current ports (I_{OL} = 15 mA, @V_{OL} = 1.0 V)
  Input-only pins: 8 input pins
- Supports various power-down states
- Compact package

Package	Code	Old Code	Body Size	Pin Pitch	Rer
QFP-80	PRQP0080JB-A	FP-80A	14 × 14 mm	0.65 mm	
TQFP-80	PTQP0080KC-A	TFP-80C	12 × 12 mm	0.5 mm	
P-TFLGA-85	PTLG0085JA-A	TLP-85V	7 × 7 mm	0.65 mm	



Notes: 1. The SCI4 pins, such as SCK4, SI4, and SO4, are supported only by the F-ZTAT version
2. The SCK4, SI4, SO4, and $\overline{\text{NMI}}$ pins are not available when the on-chip emulator debugg is used. These pins are not available as ports.
3. Supported only by the masked ROM version.

Figure 1.1 Internal Block Diagram of H8/38076R Group

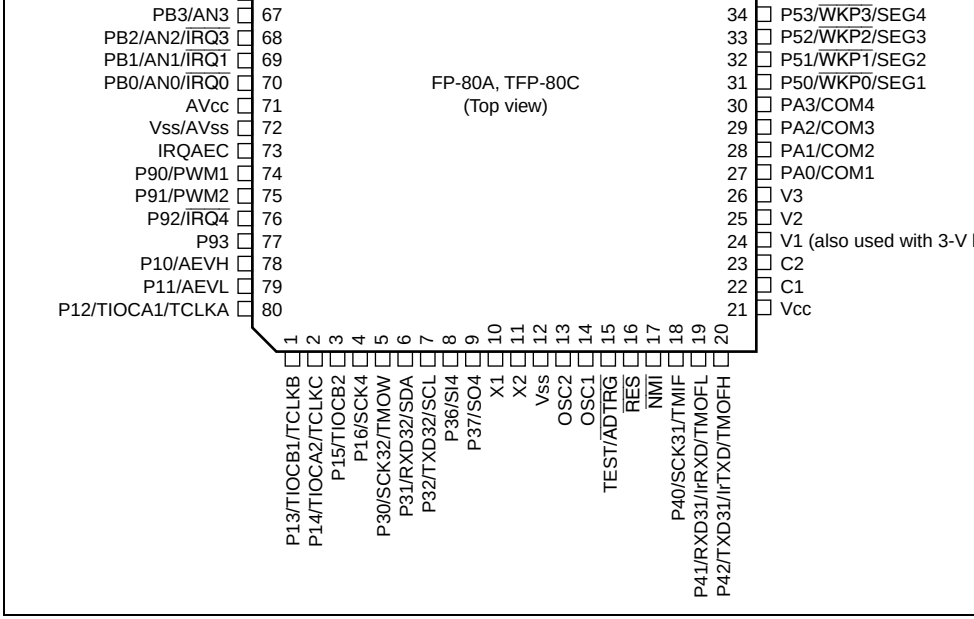
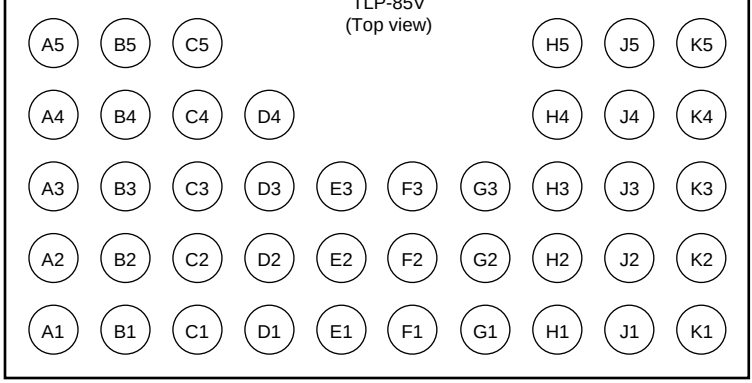


Figure 1.2 Pin Assignment of H8/38076R Group (FP-80A, TFP-80C)



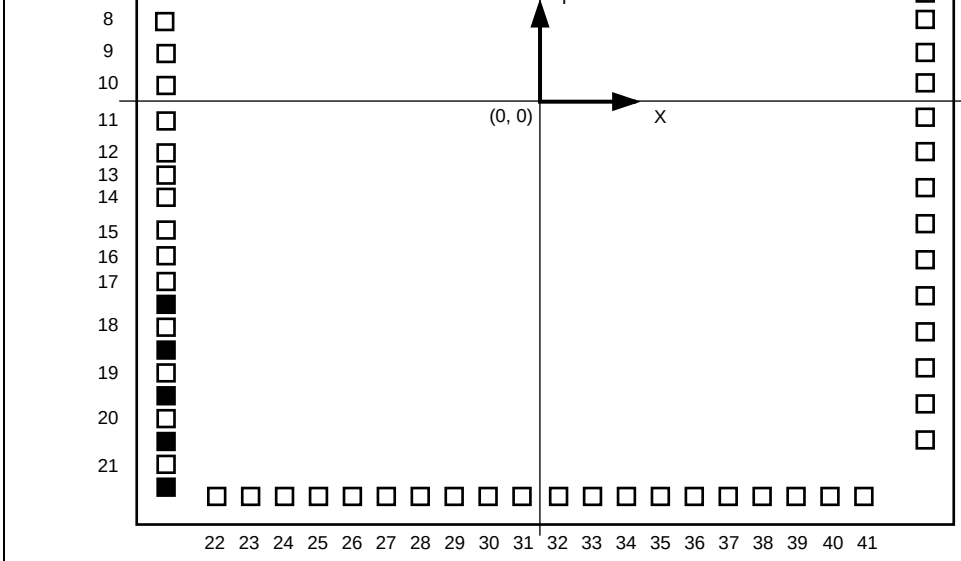
Note: For details on pin correspondence, refer to table 1.1.

Figure 1.3 Pin Assignment of H8/38076R Group (TLP-85V)

P32/TXD32/SCL	D2
P36/SI4	E1
P37/SO4	E3
X1	F2
X2	E2
Vss	F3
OSC2	G3
OSC1	F1
TEST/$\overline{\text{ADTRG}}$	G2
$\overline{\text{RES}}$	H2
$\overline{\text{NMI}}$	G1
P40/SCK31/TMIF	H3
P41/RXD31/IrRXD/TMOFL	J1
P42/TXD31/IrTXD/TMOFH	H1
NC	K1
Vcc	K2
C1	K3
C2	J2
V1	J3
V2	K4
V3	H4
PA0/COM1	J4
PA1/COM2	K5

P55/WKP5/SEG6	J8
P56/$\overline{\text{WKP6}}$/SEG7	K7
P57/$\overline{\text{WKP7}}$/SEG8	H8
P60/SEG9	K9
P61/SEG10	K8
NC	K10
P62/SEG11	J10
P63/SEG12	H10
P64/SEG13	J9
P65/SEG14	H9
P66/SEG15	G10
P67/SEG16	G8
P70/SEG17	G9
P71/SEG18	F10
P72/SEG19	F8
P73/SEG20	E9
P74/SEG21	F9
P75/SEG22	E8
P76/SEG23	D8
P77/SEG24	E10
P80/SEG25	D9
P81/SEG26	C9
P82/SEG27	D10
P83/SEG28	C8

PB5/AN5	A7
PB4/AN4	C7
PB3/AN3	B7
PB2/AN2/$\overline{\text{IRQ3}}$	A6
PB1/AN1/$\overline{\text{IRQ1}}$	C6
PB0/AN0/$\overline{\text{IRQ0}}$	B5
Avcc	B6
Vss/Avss	C5
IRQAEC	C4
P90/PWM1	A5
P91/PWM2	B4
P92/$\overline{\text{IRQ4}}$	B3
P93	A4
P10/AEVH	C3
P11/AEVL	A2
P12/TIOCA1/TCLKA	A3
NC	A1
NC	D4



Product model name	Model name on chip
HCD64F38076R	HD64F38076R

Chip size: 4.73mm × 4.73mm
Voltage level on the back of the chip: G
■ : NC pad

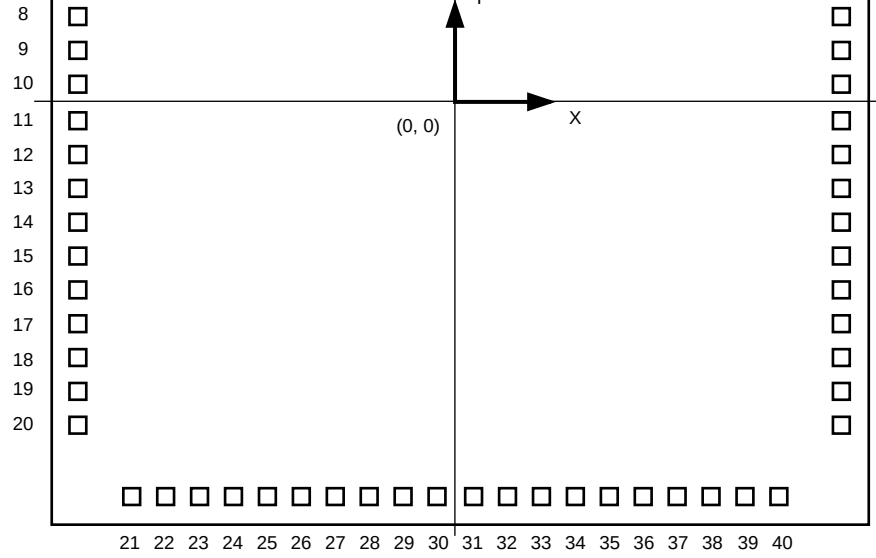
Figure 1.4 Pad Assignment of HCD64F38076R (Top View)

7	P32/TXD32/SCL	–2223	732
8	P36/SI4	–2223	523
9	P37/SO4	–2223	314
10	X1	–2223	105
11	X2	–2223	–105
12	AVss	–2223	–314
13	Vss	–2223	–418
14	OSC2	–2223	–523
15	OSC1	–2223	–732
16	TEST/$\overline{\text{ADTRG}}$	–2223	–941
17	$\overline{\text{RES}}$	–2223	–1150
18	$\overline{\text{NMI}}$	–2223	–1360
19	P40/SCK31/TMIF	–2223	–1569
20	P41/RXD31/IrRXD/TMOFL	–2223	–1778
21	P42/TXD31/IrTXD/TMOFH	–2223	–1987
22	Vcc	–1987	–2223
23	C1	–1775	–2223
24	C2	–1569	–2223
25	V1	–1360	–2223
26	V2	–1150	–2223
27	V3	–941	–2223
28	PA0/COM1	–732	–2223
29	PA1/COM2	–523	–2223

37	P55/WKP5/SEG6	1150	–2223
38	P56/$\overline{\text{WKP6}}$/SEG7	1360	–2223
39	P57/$\overline{\text{WKP7}}$/SEG8	1569	–2223
40	P60/SEG9	1778	–2223
41	P61/SEG10	1987	–2223
42	P62/SEG11	2223	–1987
43	P63/SEG12	2223	–1778
44	P64/SEG13	2223	–1569
45	P65/SEG14	2223	–1360
46	P66/SEG15	2223	–1150
47	P67/SEG16	2223	–941
48	P70/SEG17	2223	–732
49	P71/SEG18	2223	–523
50	P72/SEG19	2223	–314
51	P73/SEG20	2223	–105
52	P74/SEG21	2223	105
53	P75/SEG22	2223	314
54	P76/SEG23	2223	523
55	P77/SEG24	2223	660
56	P80/SEG25	2223	941
57	P81/SEG26	2223	1222
58	P82/SEG27	2223	1360
59	P83/SEG28	2223	1569
60	P84/SEG29	2223	1778

68	PB3/AN3	732	2223
69	PB2/AN2/$\overline{\text{IRQ3}}$	523	2223
70	PB1/AN1/$\overline{\text{IRQ1}}$	314	2223
71	PB0/AN0/$\overline{\text{IRQ0}}$	105	2223
72	AVcc	–105	2223
73	Vss/AVss	–314	2223
74	IRQAEC	–523	2223
75	P90/PWM1	–732	2223
76	P91/PWM2	–941	2223
77	P92/$\overline{\text{IRQ4}}$	–1150	2223
78	P93	–1360	2223
79	P10/AEVH	–1569	2223
80	P11/AEVL	–1778	2223
81	P12/TIOCA1/TCLKA	–1987	2223

Note: The power supply (Vss) pads in pad numbers 12 and 13 must not be open but con
When the TEST pad in pad number 16 is not used as the $\overline{\text{ADTRG}}$ pin, it must be c
to the Vss voltage level. If not, this LSI does not operate correctly.
When the TEST pad is used as the $\overline{\text{ADTRG}}$ pin, the function should be changed to
$\overline{\text{ADTRG}}$ pin at Vss voltage level during a reset in advance.



Product model name	Model name on chip
HCD64338076R	HD64338076R

Chip size: 3.60 mm × 3.69 mm
Voltage level on the back of the chip: G

Figure 1.5 Pad Assignment of HCD64338076R (Top View)

7	P32/TXD32/SCL	–1683	547
8	P36	–1683	391
9	P37	–1683	234
10	X1	–1683	97
11	X2	–1683	–29
12	VSS	–1683	–234
13	OSC2	–1683	–391
14	OSC1	–1683	–575
15	TEST/$\overline{\text{ADTRG}}$	–1683	–703
16	$\overline{\text{RES}}$	–1683	–859
17	$\overline{\text{NMI}}$	–1683	–1016
18	P40/SCK31/TMIF	–1683	–1172
19	P41/RXD31/IrRXD/TMOFL	–1683	–1328
20	P42/TXD31/IrTXD/TMOFH	–1683	–1484
21	VCC	–1448	–1728
22	C1	–1208	–1728
23	C2	–1085	–1728
24	V1	–963	–1728
25	V2	–841	–1728
26	V3	–689	–1728
27	PA0/COM1	–536	–1728
28	PA1/COM2	–384	–1728
29	PA2/COM3	–231	–1728

37	P56/WKP6/SEG7	994	–1728
38	P57/$\overline{\text{WKP7}}$/SEG8	1146	–1728
39	P60/SEG9	1298	–1728
40	P61/SEG10	1448	–1728
41	P62/SEG11	1683	–1484
42	P63/SEG12	1683	–1328
43	P64/SEG13	1683	–1159
44	P65/SEG14	1683	–1016
45	P66/SEG15	1683	–859
46	P67/SEG16	1683	–703
47	P70/SEG17	1683	–547
48	P71/SEG18	1683	–391
49	P72/SEG19	1683	–234
50	P73/SEG20	1683	–78
51	P74/SEG21	1683	78
52	P75/SEG22	1683	234
53	P76/SEG23	1683	391
54	P77/SEG24	1683	547
55	P80/SEG25	1683	703
56	P81/SEG26	1683	859
57	P82/SEG27	1683	1016
58	P83/SEG28	1683	1172
59	P84/SEG29	1683	1328
60	P85/SEG30	1683	1484

68	PB2/AN2/IRQ3	384	1728
69	PB1/AN1/$\overline{\text{IRQ1}}$	231	1728
70	PB0/AN0/$\overline{\text{IRQ0}}$	79	1728
71	AVCC	–79	1728
72	VSS/AVSS	–231	1728
73	IRQAEC	–384	1728
74	P90/PWM1	–536	1728
75	P91/PWM2	–689	1728
76	P92/$\overline{\text{IRQ4}}$	–841	1728
77	P93	–994	1728
78	P10/AEVH	–1146	1728
79	P11/AEVL	–1298	1728
80	P12/TIOCA1/TCLKA	–1448	1728

Note: The power supply (Vss) pads in pad number 12 must not be open but connected. V
TEST pad in pad number 15 is not used as the $\overline{\text{ADTRG}}$ pin, it must be connected t
voltage level. If not, this LSI does not operate correctly.

When the TEST pad is used as the $\overline{\text{ADTRG}}$ pin, the function should be changed to
$\overline{\text{ADTRG}}$ pin at Vss voltage level during a reset in advance.

	AVcc	71	B6	72	71	Input	Analog power supply pins fo converter. When the A/D co not used, connect this pin to system power supply.
	AVss	72 (= Vss)	C5 (= Vss)	73	72	Input	Ground pins for the A/D con Connect this pin to the syste supply (0 V).
	V1 to V3	24 to 26	J3, K4, H4	25 to 27	24 to 26	Input	Power supply pins for the LC controller/driver.
	C1	22	K3	23	22	Input	Capacitance pins for steppin LCD drive power supply.
	C2	23	J2	24	23	Input	
Clock pins	OSC1	14	F1	15	14	Input	These pins connect with cry ceramic resonator for the sy or can be used to input an e clock. See section 5, Clock Pulse for a typical connection.
	OSC2	13	G3	14	13	Output	
	X1	10	F2	10	10	Input	These pins connect with a 3 38.4-kHz crystal resonator f subclock. See section 5, Clo Generators, for a typical cor
	X2	11	E2	11	11	Output	

							see section 18.4.2, Externa Input Timing.
Interrupt pins	$\overline{\text{NMI}}$	17	G1	18	17	Input	NMI interrupt request pins. Non-maskable interrupt requ pin.
	$\overline{\text{IRQ0}}$	70	B5	71	70	Input	External interrupt request in
	$\overline{\text{IRQ1}}$	69	C6	70	69	Input	Can select the rising or fallin
	$\overline{\text{IRQ3}}$	68	A6	69	68	Input	
	$\overline{\text{IRQ4}}$	76	B3	77	76	Input	
	IRQAEC	73	C4	74	73	Input	Interrupt input pins for the asynchronous event counte This pin enables the asynch event input. In the masked R version, this pin controls turn the on-chip oscillator during
	$\overline{\text{WKP0}}$ to $\overline{\text{WKP7}}$	31 to 38	J5, H6, H7, K6, J7, J8, K7, H8	32 to 39	31 to 38	Input	Wakeup interrupt request in Can select the rising or fallin

	TIOCB2	3	B2	3	3	Input	Pins for the TGR2B input c input.
	TCLKA	80	A3	81	80	Input	External clock input pins.
	TCLKB	1	B1	1	1	Input	
	TCLKC	2	C1	2	2	Input	
Timer F	TMIF	18	H3	19	18	Input	Event input pins for input t F counter.
	TMOFL	19	J1	20	19	Output	Output pins for waveforms by the timer FL output com function.
	TMOFH	20	H1	21	20	Output	Output pins for waveforms by the timer FH output com function.
Asynch-ronous event counter (AEC)	AEVL	79	A2	80	79	Input	Event input pins for input t asynchronous event count
	AEVH	78	C3	79	78	Input	
RTC	TMOW	5	D1	5	5	Output	Divided clock output pins f
14-bit PWM	PWM1	74	A5	75	74	Output	Output pins for waveforms by the 14-bit PWM in PWM 1 and 2.
	PWM2	75	B4	76	75	Output	

							or on-chip emulator debugg this pin is not available.
Serial commu-nication interface 3 (SCI3)	SCK31	18	H3	19	18	I/O	SCI3_1 clock I/O pins.
	RXD31/ IrRXD	19	J1	20	19	Input	SCI3_1 data input pins or da pins for the IrDA format.
	TXD31/ IrTXD	20	H1	21	20	Output	SCI3_1 data output pins or output pins for the IrDA form
	SCK32	5	D1	5	5	I/O	SCI3_2 clock I/O pins.
	RXD32	6	D3	6	6	Input	SCI3_2 data input pins.
	TXD32	7	D2	7	7	Output	SCI3_2 data output pins.
A/D converter	AN0 to AN2	70 to 68	B5, C6, A6	71 to 69	70 to 68	Input	Analog data input pins for th converter.
	AN3 to AN7*[4]	67 to 63	B7, C7, A7, B8, B9	68 to 64	67 to 63	Input	
	$\overline{\text{ADTRG}}$	15	G2	16	15	Input	External trigger input pins fo converter.
I^2C bus interface 2 (IIC2)	SDA	6	D3	6	6	I/O	IIC data I/O pins.
	SCL	7	D2	7	7	I/O	IIC clock I/O pins.

			H9, G8				
	SEG17 to SEG24	47 to 54	G9, F10, F8, E9, F9, E8, D8, E10	48 to 55	47 to 54	Output	
	SEG25 to SEG32	55 to 62	D9, C9, D10, C8, B10, C10, A9, A8	56 to 63	55 to 62	Output	
I/O ports	P10 to P12	78 to 80	C3, A2, A3	79 to 81	78 to 80	I/O	7-bit I/O pins. Input or outp designated for each bit by the port control register 1 (
	P13 to P16	1 to 4	B1, C1, B2, C2	1 to 4	1 to 4		
	P30 to P32, P36, P37	5 to 9	D1, D3, D2, E1, E3	5 to 9	5 to 9	I/O	5-bit I/O pins. Input or outp designated for each bit by the port control register 3 (
	P40 to P42	18 to 20	H3, J1, H1	19 to 21	18 to 20	I/O	3-bit I/O pins. Input or outp designated for each bit by the port control register 4 (
	P50 to P57	31 to 38	J5, H6, H7, K6, J7, J8, K7, H8	32 to 39	31 to 38	I/O	8-bit I/O pins. Input or outp designated for each bit by the port control register 5 (
	P60 to P67	39 to 46	K9, K8, J10, H10, J9, H9, G10, G8	40 to 47	39 to 46	I/O	8-bit I/O pins. Input or outp designated for each bit by the port control register 6 (

P90 to P93	74 to 77	A5, B4, B3, A4	75 to 78	74 to 77	I/O	4-bit I/O pins. Input or outpu designated for each bit by m the port control register 9 (P
PA0 to PA3	27 to 30	J4, K5, H5, J6	28 to 31	27 to 30	I/O	4-bit I/O pins. Input or outpu designated for each bit by m the port control register A (P
PB0 to PB7	70 to 63	B5, C6, A6, B7, C7, A7, B8, B9	71 to 64	70 to 63	Input	8-bit input-only pins

Notes: 1. Pad no. for the flash memory version.
2. Pad no. for the masked ROM version.

- General-register architecture

  Sixteen 16-bit general registers also usable as sixteen 8-bit registers and eight 16-bit or eight 32-bit registers
- Sixty-two basic instructions

  8/16/32-bit data transfer and arithmetic and logic instructions

  Multiply and divide instructions

  Powerful bit-manipulation instructions
- Eight addressing modes

  Register direct [Rn]

  Register indirect [@ERn]

  Register indirect with displacement [@(d:16,ERn) or @(d:24,ERn)]

  Register indirect with post-increment or pre-decrement [@ERn+ or @–ERn]

  Absolute address [@aa:8, @aa:16, @aa:24]

  Immediate [#xx:8, #xx:16, or #xx:32]

  Program-counter relative [@(d:8,PC) or @(d:16,PC)]

  Memory indirect [@@aa:8]
- 64-kbyte address space
- High-speed operation

  All frequently-used instructions execute in one or two states

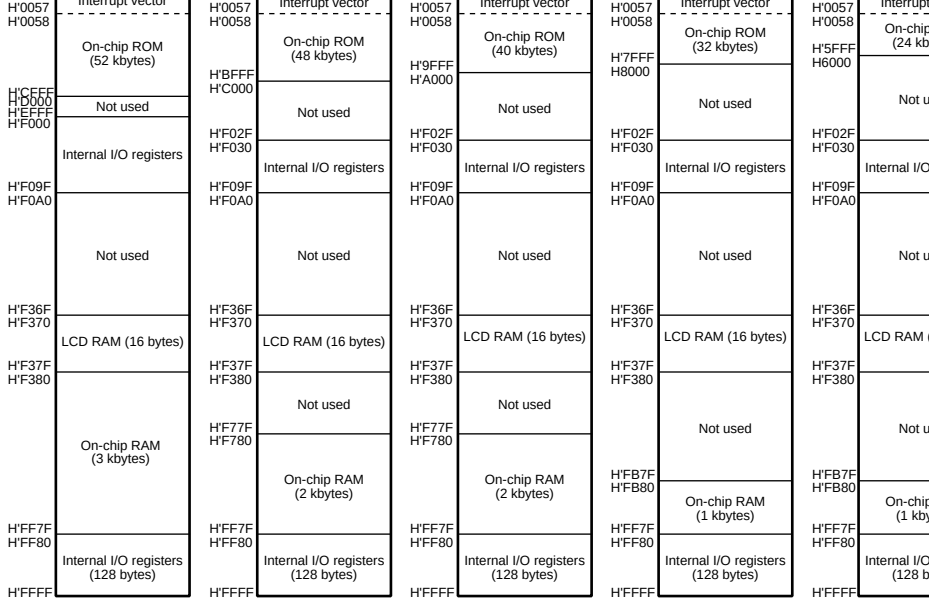
  8/16/32-bit register-register add/subtract : 2 state

  8 × 8-bit register-register multiply : 14 states

  16 ÷ 8-bit register-register divide : 14 states

  16 × 16-bit register-register multiply : 22 states

  32 ÷ 16-bit register-register divide : 22 states



Note: When the on-chip debugging emulator is used, the areas from H'C000 to H'CFFF and from H'F380 to H'F used by the emulator and not accessible by the user.

Figure 2.1 Memory Map

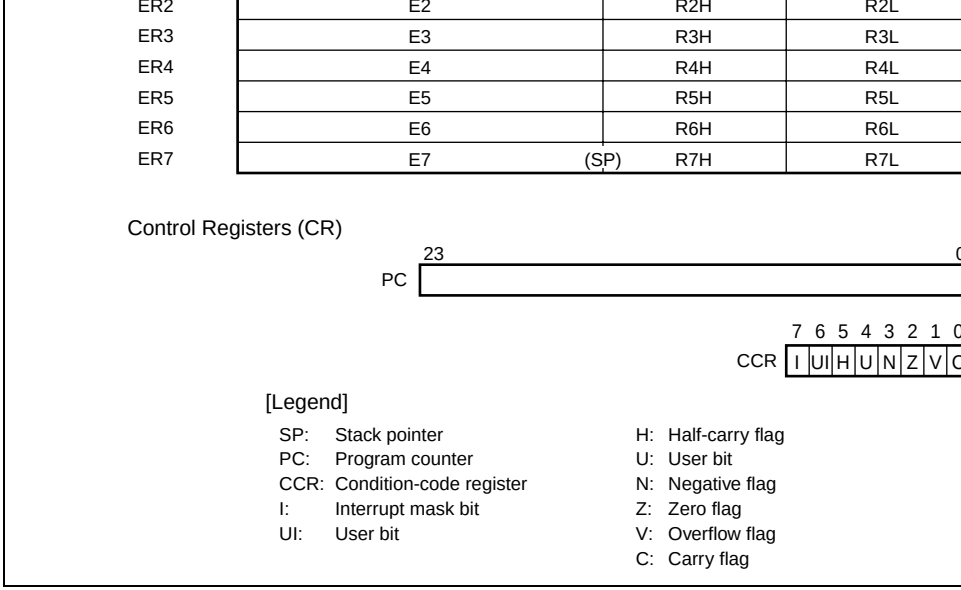


Figure 2.2 CPU Registers

The R registers divide into 8-bit registers designated by the letters RH (R0H to R7H) and
to R7L). These registers are functionally equivalent, providing a maximum of sixteen 8-b
registers.

The usage of each register can be selected independently.

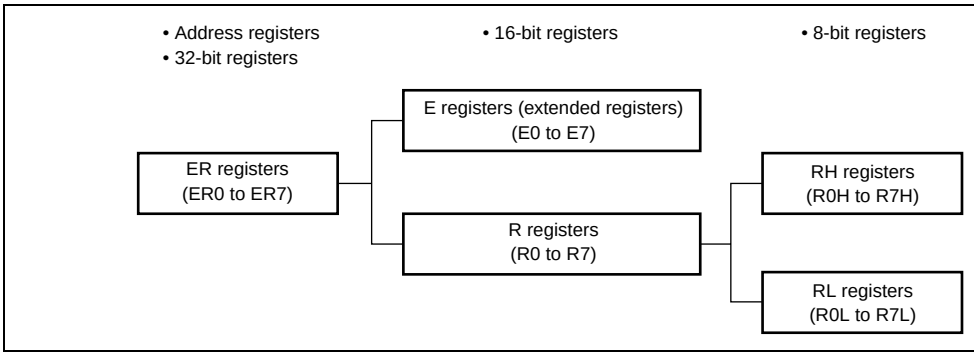


Figure 2.3 Usage of General Registers

General register ER7 has the function of the stack pointer (SP) in addition to its general-r
function, and is used implicitly in exception handling and subroutine calls. Figure 2.4 sho
relationship between the stack pointer and the stack area.

Figure 2.4 Relationship between Stack Pointer and Stack Area

2.2.2 Program Counter (PC)

This 24-bit counter indicates the address of the next instruction the CPU will execute. T
of all CPU instructions is 2 bytes (one word), so the least significant PC bit is ignored. (
instruction is fetched, the least significant PC bit is regarded as 0). The PC is initialized
start address is loaded by the vector address generated during reset exception-handling s

2.2.3 Condition-Code Register (CCR)

This 8-bit register contains internal CPU status information, including an interrupt mask
half-carry (H), negative (N), zero (Z), overflow (V), and carry (C) flags. The I bit is initi
by reset exception-handling sequence, but other bits are not initialized.

Some instructions leave flag bits unchanged. Operations can be performed on the CCR b
LDC, STC, ANDC, ORC, and XORC instructions. The N, Z, V, and C flags are used as
conditions for conditional branch (Bcc) instructions.

For the action of each instruction on the flag bits, see Appendix A.1, Instruction List.

				When the ADD.B, ADDX.B, SUB.B, SUBX.B, C or NEG.B instruction is executed, this flag is se there is a carry or borrow at bit 3, and cleared t otherwise. When the ADD.W, SUB.W, CMP.W NEG.W instruction is executed, the H flag is se there is a carry or borrow at bit 11, and cleared otherwise. When the ADD.L, SUB.L, CMP.L, o instruction is executed, the H flag is set to 1 if t carry or borrow at bit 27, and cleared to 0 othe
4	U	Undefined	R/W	User Bit Can be written and read by software using the STC, ANDC, ORC, and XORC instructions.
3	N	Undefined	R/W	Negative Flag Stores the value of the most significant bit of d sign bit.
2	Z	Undefined	R/W	Zero Flag Set to 1 to indicate zero data, and cleared to 0 indicate non-zero data.
1	V	Undefined	R/W	Overflow Flag Set to 1 when an arithmetic overflow occurs, a cleared to 0 at other times.
0	C	Undefined	R/W	Carry Flag Set to 1 when a carry occurs, and cleared to 0 otherwise. Used by: • Add instructions, to indicate a carry • Subtract instructions, to indicate a borrow • Shift and rotate instructions, to indicate a c The carry flag is also used as a bit accumulato manipulation instructions.

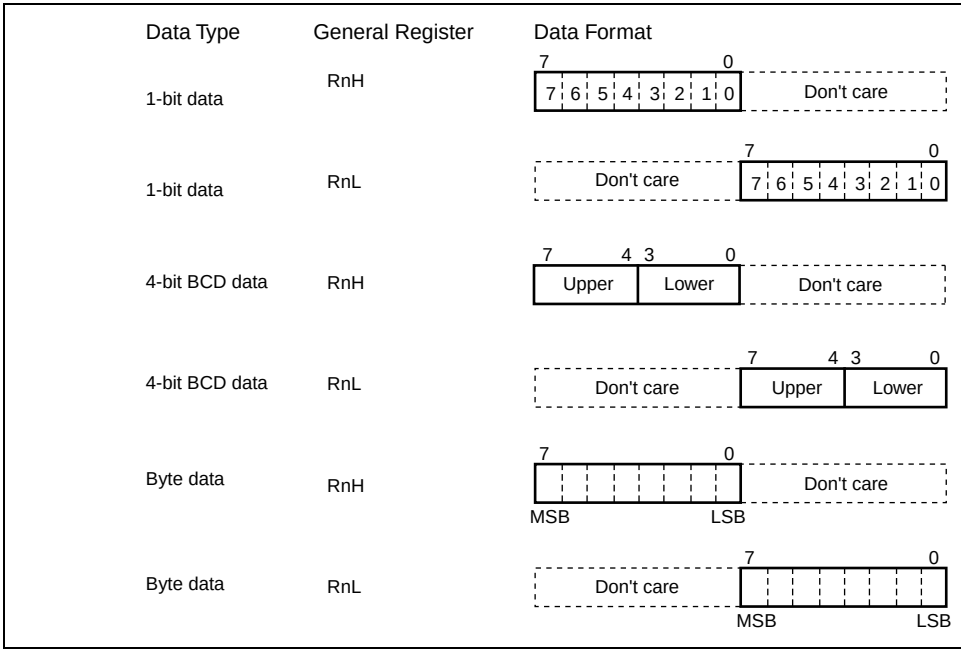
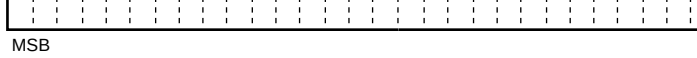


Figure 2.5 General Register Data Formats (1)



[Legend]

ERn: General register ER
En: General register E
Rn: General register R
RnH: General register RH
RnL: General register RL
MSB: Most significant bit
LSB: Least significant bit

Figure 2.5 General Register Data Formats (2)

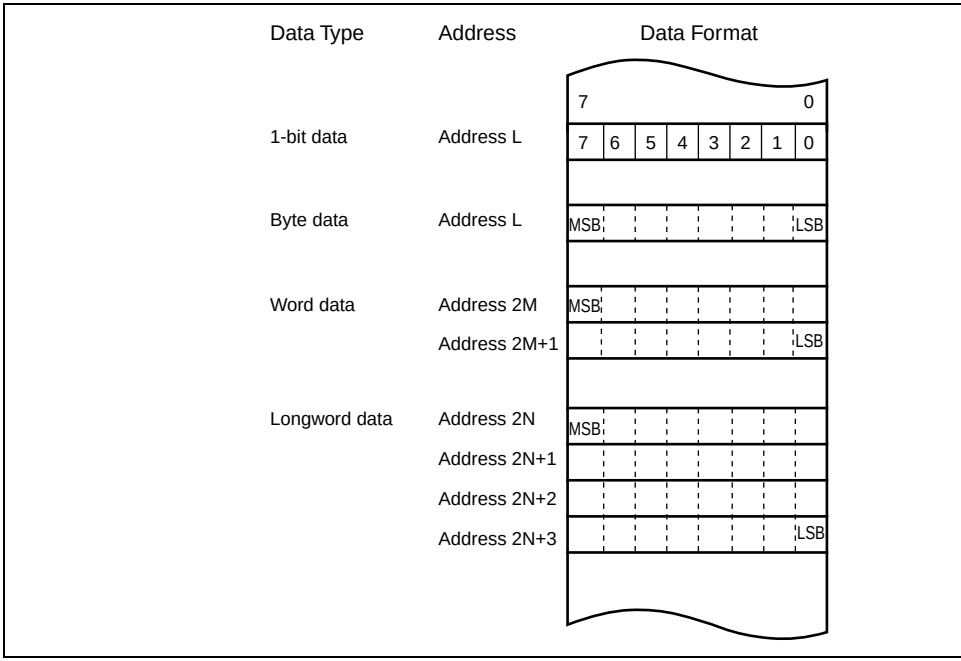


Figure 2.6 Memory Data Formats

Rd	General register (destination)*
Rs	General register (source)*
Rn	General register*
ERn	General register (32-bit register or address register)
(EAd)	Destination operand
(EAs)	Source operand
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical XOR
→	Move
¬	NOT (logical complement)

MOVFPE	B	(EAs) → Rd Cannot be used in this LSI.
MOVTPE	B	Rs → (EAs) Cannot be used in this LSI.
POP	W/L	@SP+ → Rn Pops a general register from the stack. POP.W Rn is identical @SP+, Rn. POP.L ERn is identical to MOV.L @SP+, ERn.
PUSH	W/L	Rn → @–SP Pushes a general register onto the stack. PUSH.W Rn is ident MOV.W Rn, @–SP. PUSH.L ERn is identical to MOV.L ERn, @

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

DEC		Increments or decrements a general register by 1 or 2. (Byte op can be incremented or decremented by 1 only.)
ADDS SUBS	L	Rd ± 1 → Rd, Rd ± 2 → Rd, Rd ± 4 → Rd Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit
DAA DAS	B	Rd (decimal adjust) → Rd Decimal-adjusts an addition or subtraction result in a general re referring to the CCR to produce 4-bit BCD data.
MULXU	B/W	Rd × Rs → Rd Performs unsigned multiplication on data in two general register 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
MULXS	B/W	Rd × Rs → Rd Performs signed multiplication on data in two general registers: bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
DIVXU	B/W	Rd ÷ Rs → Rd Performs unsigned division on data in two general registers: eitl bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 16-bit quotient and 16-bit remainder.

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

		general register.
EXTU	W/L	Rd (zero extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the bits of a 32-bit register to longword size, by padding with zeros left.
EXTS	W/L	Rd (sign extension) → Rd Extends the lower 8 bits of a 16-bit register to word size, or the bits of a 32-bit register to longword size, by extending the sign

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

NOT	B/W/L	¬ (Rd) → (Rd) Takes the one's complement (logical complement) of general re contents.

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

Table 2.5 Shift Instructions

Instruction	Size*	Function
SHAL SHAR	B/W/L	Rd (shift) → Rd Performs an arithmetic shift on general register contents.
SHLL SHLR	B/W/L	Rd (shift) → Rd Performs a logical shift on general register contents.
ROTL ROTR	B/W/L	Rd (rotate) → Rd Rotates general register contents.
ROTXL ROTXR	B/W/L	Rd (rotate) → Rd Rotates general register contents through the carry flag.

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

		Inverts a specified bit in a general register or memory operand number is specified by 3-bit immediate data or the lower three general register.
BTST	B	¬ (<bit-No.> of <EAd>) → Z Tests a specified bit in a general register or memory operand a clears the Z flag accordingly. The bit number is specified by 3- immediate data or the lower three bits of a general register.
BAND	B	C ∧ (<bit-No.> of <EAd>) → C ANDs the carry flag with a specified bit in a general register or operand and stores the result in the carry flag.
BIAND	B	C ∧ ¬ (<bit-No.> of <EAd>) → C ANDs the carry flag with the inverse of a specified bit in a gene register or memory operand and stores the result in the carry f The bit number is specified by 3-bit immediate data.
BOR	B	C ∨ (<bit-No.> of <EAd>) → C ORs the carry flag with a specified bit in a general register or n operand and stores the result in the carry flag.
BIOR	B	C ∨ ¬ (<bit-No.> of <EAd>) → C ORs the carry flag with the inverse of a specified bit in a gener or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C XORs the carry flag with a specified bit in a general register or operand and stores the result in the carry flag.
BIXOR	B	C ⊕ ¬ (<bit-No.> of <EAd>) → C XORs the carry flag with the inverse of a specified bit in a gene register or memory operand and stores the result in the carry f The bit number is specified by 3-bit immediate data.

BIST	B	¬ C → (<bit-No.> of <EAd>) Transfers the inverse of the carry flag value to a specified bit in register or memory operand. The bit number is specified by 3-bit immediate data.

Note: * Refers to the operand size.
B: Byte

BCC(BHS)	Carry clear (high or same)	C = 0
BCS(BLO)	Carry set (low)	C = 1
BNE	Not equal	Z = 0
BEQ	Equal	Z = 1
BVC	Overflow clear	V = 0
BVS	Overflow set	V = 1
BPL	Plus	N = 0
BMI	Minus	N = 1
BGE	Greater or equal	N ⊕ V = 0
BLT	Less than	N ⊕ V = 1
BGT	Greater than	Z∨(N ⊕ V) = 0
BLE	Less or equal	Z∨(N ⊕ V) = 1

JMP	—	Branches unconditionally to a specified address.
BSR	—	Branches to a subroutine at a specified address.
JSR	—	Branches to a subroutine at a specified address.
RTS	—	Returns from a subroutine

Note: * Bcc is the general name for conditional branch instructions.

		word access.
ANDC	B	CCR ∧ #IMM → CCR Logically ANDs the CCR with immediate data.
ORC	B	CCR ∨ #IMM → CCR Logically ORs the CCR with immediate data.
XORC	B	CCR ⊕ #IMM → CCR Logically XORs the CCR with immediate data.
NOP	—	PC + 2 → PC Only increments the program counter.

Note: * Refers to the operand size.
B: Byte
W: Word

else next;

Transfers a data block. Starting from the address set in ER5, t
data for the number of bytes set in R4L or R4 to the address lo
in ER6.

Execution of the next instruction begins as soon as the transfe
completed.

on the operand. The operation field always includes the first four bits of the instruction. S
instructions have two operation fields.

(2) Register Field

Specifies a general register. Address registers are specified by 3 bits, and data registers by
4 bits. Some instructions have two register fields. Some have no register field.

(3) Effective Address Extension

8, 16, or 32 bits specifying immediate data, an absolute address, or a displacement. A24-b
address or displacement is treated as a 32-bit data in which the first 8 bits are 0 (H'00).

(4) Condition Field

Specifies the branching condition of Bcc instructions.

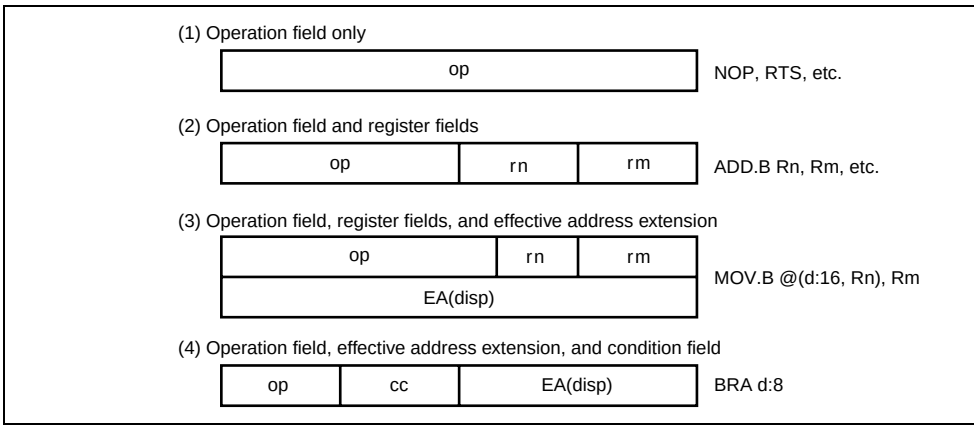


Figure 2.7 Instruction Formats

Arithmetic and logic instructions can use the register direct and immediate modes. Data
instructions can use all addressing modes except program-counter relative and memory
Bit-manipulation instructions use register direct, register indirect, or the absolute addres
(@aa:8) to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST ins
or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.10 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:24,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @–ERn
5	Absolute address	@aa:8/@aa:16/@aa:24
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

(1) Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register contain
operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and
can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

- Register indirect with post-increment—@ERn+

  The register field of the instruction code specifies an address register (ERn) the lower
  of which contains the address of a memory operand. After the operand is accessed, 1,
  added to the address register contents (32 bits) and the sum is stored in the address reg
  The value added is 1 for byte access, 2 for word access, or 4 for longword access. For
  or longword access, the register value should be even.
- Register indirect with pre-decrement—@-ERn

  The value 1, 2, or 4 is subtracted from an address register (ERn) specified by the regis
  in the instruction code, and the lower 24 bits of the result is the address of a memory o
  The result is also stored in the address register. The value subtracted is 1 for byte acce
  word access, or 4 for longword access. For the word or longword access, the register v
  should be even.

(5) Absolute Address—@aa:8, @aa:16, @aa:24

The instruction code contains the absolute address of a memory operand. The absolute ad
may be 8 bits long (@aa:8), 16 bits long (@aa:16), 24 bits long (@aa:24)

For an 8-bit absolute address, the upper 16 bits are all assumed to be 1 (H'FFFF). For a 16
absolute address the upper 8 bits are a sign extension. A 24-bit absolute address can acces
entire address space.

The access ranges of absolute addresses for this LSI are those shown in table 2.11, becaus
upper 8 bits are ignored.

operand.

The ADDS, SUBS, INC, and DEC instructions contain immediate data implicitly. Some manipulation instructions contain 3-bit immediate data in the instruction code, specifyin number.

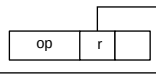
(7) Program-Counter Relative—@(d:8, PC) or @(d:16, PC)

This mode is used in the BSR instruction. An 8-bit or 16-bit displacement contained in t instruction is sign-extended and added to the 24-bit PC contents to generate a branch ad PC value to which the displacement is added is the address of the first byte of the next in so the possible branching range is –126 to +128 bytes (–63 to +64 words) or –32766 to + bytes (–16383 to +16384 words) from the branch instruction. The resulting value should even number.

(8) Memory Indirect—@@aa:8

This mode can be used by the JMP and JSR instructions. The instruction code contains a absolute address specifying a memory operand. This memory operand contains a branch The memory operand is accessed in words, generating a 16-bit branch address. Figure 2 how to specify branch address for in memory indirect mode. The upper bits of the absolu are all assumed to be 0, so the address range is 0 to 255 (H'0000 to H'00FF).

Note that the first part of the address range is also the exception vector area.

<table>
<tr>
<td></td>
<td> 
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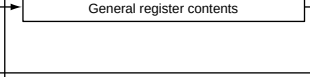
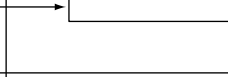
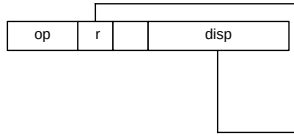
<td> 
</td>
<td>  </td>
</tr>
<tr>
<td>3</td>
<td>Register indirect with displacement
@(d:16,ERn) or @(d:24,ERn)
 
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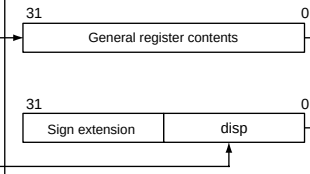
<td> 
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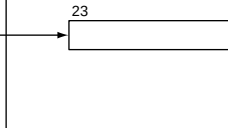
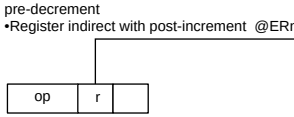
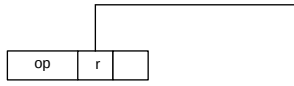
<td> 
</td>
</tr>
<tr>
<td>4</td>
<td>Register indirect with post-increment or
pre-decrement
•Register indirect with post-increment @ERn+
 

•Register indirect with pre-decrement @-ERn
 
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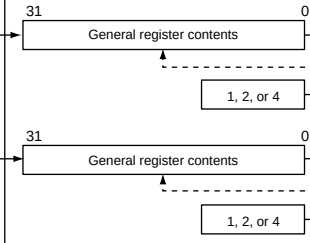
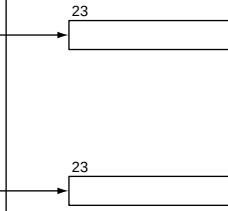
<td> 

The value to be added or subtracted is 1 when the operand is byte size, 2 for word size, and 4 for longword size.</td>
<td> 
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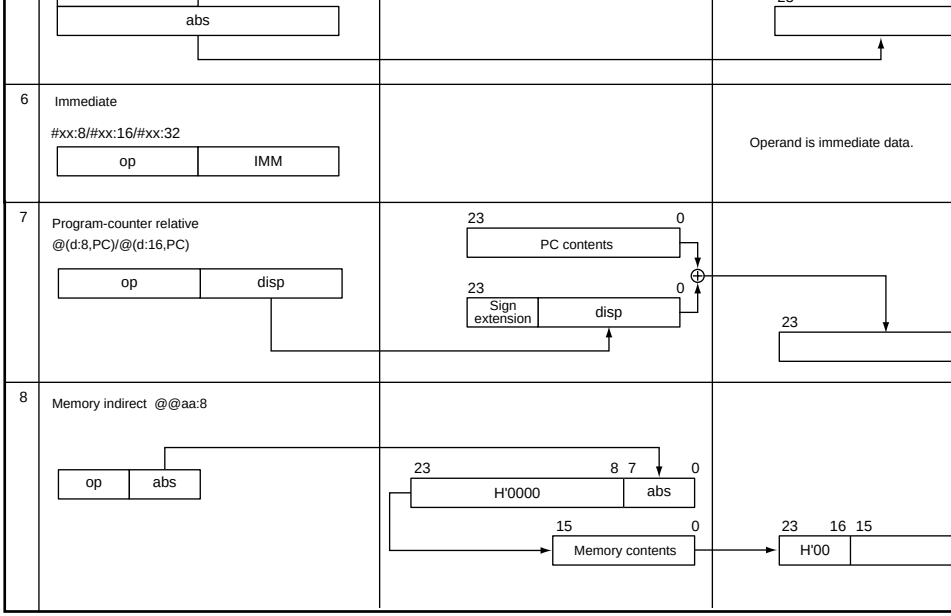


[Legend]
r, rm,rn : Register field
op : Operation field
disp : Displacement
IMM : Immediate data
abs : Absolute address

in byte or word size. Figure 2.9 shows the on-chip memory access cycle.

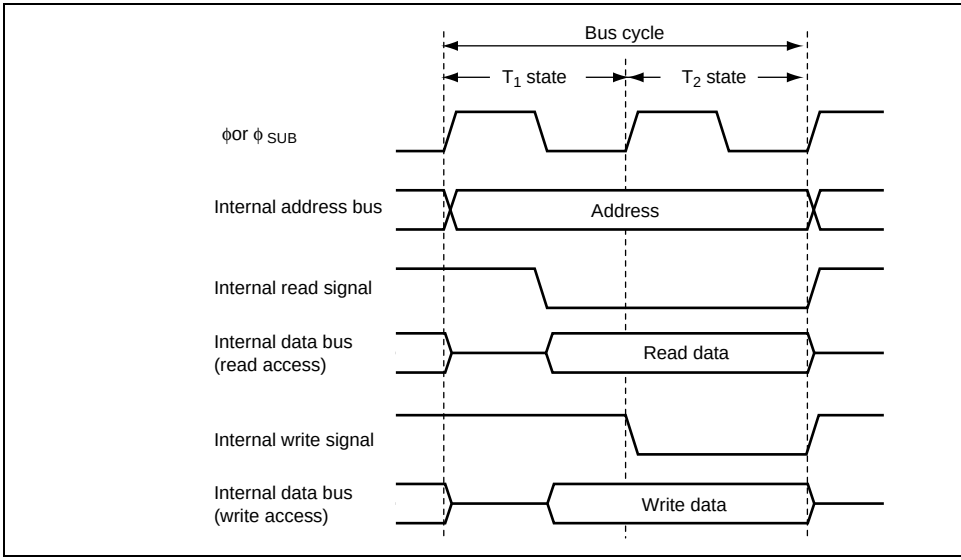


Figure 2.9 On-Chip Memory Access Cycle

module.

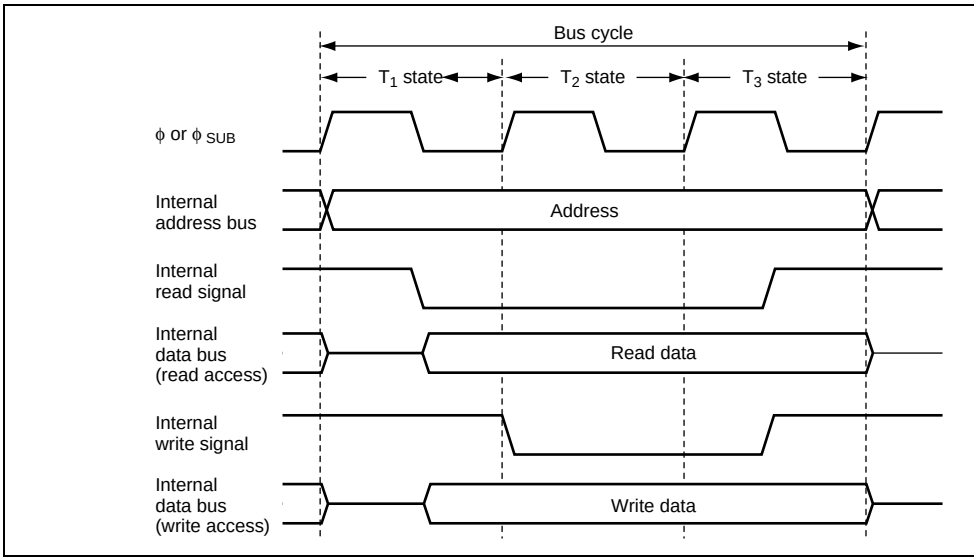


Figure 2.10 On-Chip Peripheral Module Access Cycle (3-State Access)

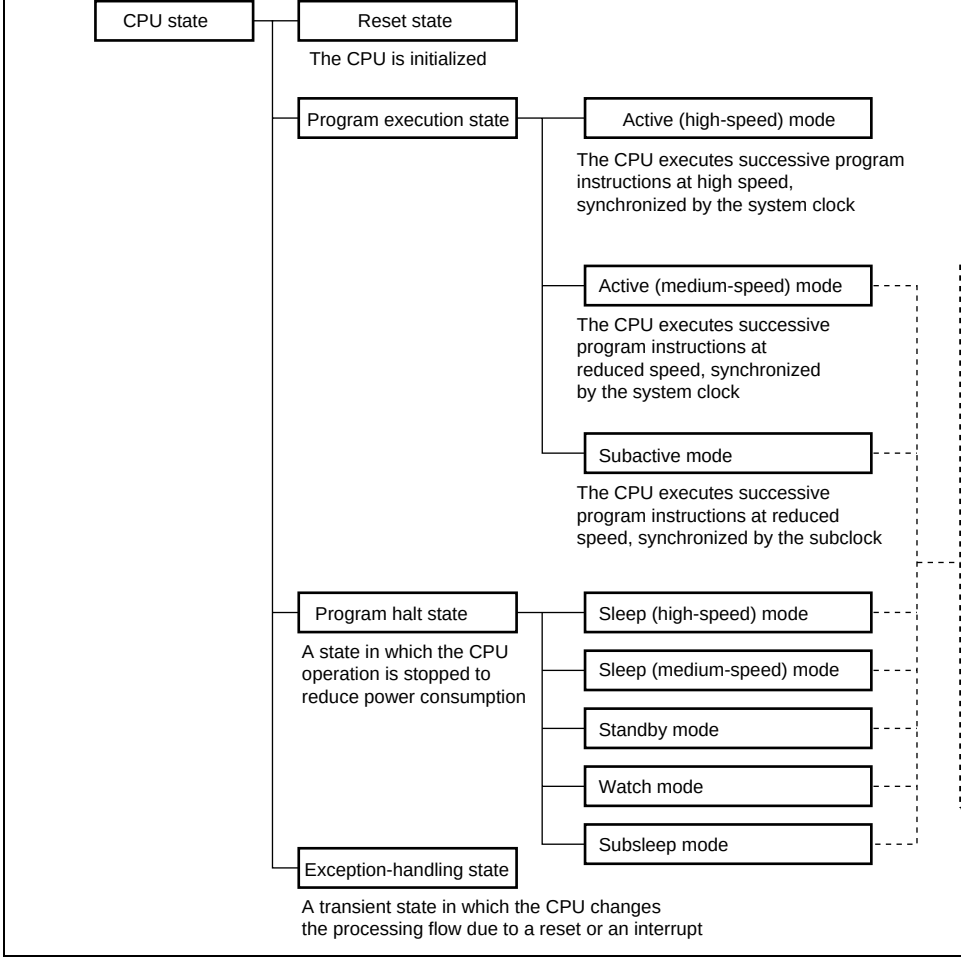


Figure 2.11 CPU Operating States

Figure 2.12 State Transitions

2.8 Usage Notes

2.8.1 Notes on Data Access to Empty Areas

The address space of this LSI includes empty areas in addition to the ROM, RAM, and on
I/O registers areas available to the user. When data is transferred from CPU to empty area
transferred data will be lost. This action may also cause the CPU to malfunction. When d
transferred from an empty area to CPU, the contents of the data cannot be guaranteed.

2.8.2 EEPMOV Instruction

EEPMOV is a block-transfer instruction and transfers the byte size of data indicated by R
which starts from the address indicated by R5, to the address indicated by R6. Set R4L an
that the end address of the destination address (value of R6 + R4L) does not exceed H'FF
value of R6 must not change from H'FFFF to H'0000 during execution).

Example 1: Bit manipulation for the timer load register and timer counter

Figure 2.13 shows an example of a timer in which two timer registers are assigned to the address. When a bit-manipulation instruction accesses the timer load register and timer c a reloadable timer, since these two registers share the same address, the following opera place.

1. Data is read in byte units.
2. The CPU sets or resets the bit to be manipulated with the bit-manipulation instructio
3. The written data is written again in byte units to the timer load register.

The timer is counting, so the value read is not necessarily the same as the value in the ti register. As a result, bits other than the intended bit in the timer counter may be modifie modified value may be written to the timer load register.

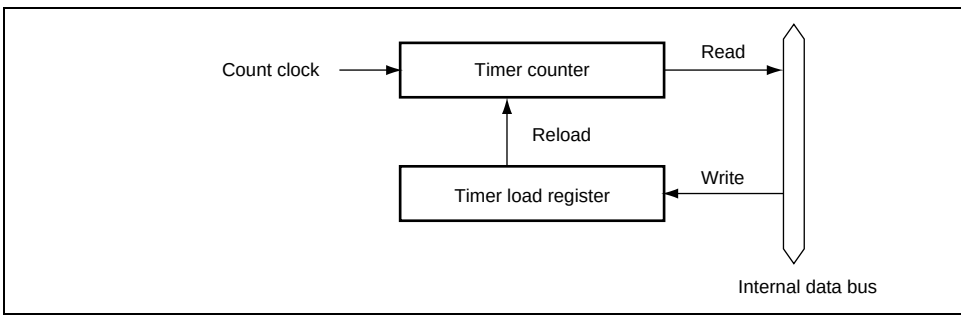


Figure 2.13 Example of Timer Configuration with Two Registers Allocated to Address

PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0

- BSET instruction executed instruction

```
BSET    #0,     @PDR5
```

The BSET instruction is executed for port 5.

- After executing BSET instruction

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**
Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	0	1	0	0	0	0	0

- Description on operation

1. When the BSET instruction is executed, first the CPU reads port 5.
   Since P57 and P56 are input pins, the CPU reads the pin states (low-level and high-le
   input).
   P55 to P50 are output pins, so the CPU reads the value in PDR5. In this example PDR
   value of H'80, but the value read by the CPU is H'40.
2. Next, the CPU sets bit 0 of the read data to 1, changing the PDR5 data to H'41.

	P57	P56	P55	P54	P53	P52	P51
Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0
RAM0	1	0	0	0	0	0	0

- BSET instruction executed

```
BSET    #0,    @RAM0
```

The BSET instruction is executed designating the work area (RAM0).

- After executing BSET instruction

```
MOV.B   @RAM0, R0L
MOV.B   R0L,  @PDR5
```

The work area (RAM0) value is written to PDR5

	P57	P56	P55	P54	P53	P52	P51
Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0
RAM0	1	0	0	0	0	0	0

Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0

- BCLR instruction executed

```
BCLR   #0,    @PCR5
```

The BCLR instruction is executed for PCR5.

- After executing BCLR instruction

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**
Input/output	Output	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	1	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0

- Description on operation

1. When the BCLR instruction is executed, first the CPU reads PCR5. Since PCR5 is a v register, the CPU reads a value of H'FF, even though the PCR5 value is actually H'3F
2. Next, the CPU clears bit 0 in the read data to 0, changing the data to H'FE.
3. Finally, H'FE is written to PCR5 and BCLR instruction execution ends.

   As a result of this operation, bit 0 in PCR5 becomes 0, making P50 an input port. Hov bits 7 and 6 in PCR5 change to 1, so that P57 and P56 change from input pins to outp To prevent this problem, store a copy of the PDR5 data in a work area in memory and manipulate data of the bit in the work area, then write this data to PDR5.

PDR5	1	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1

- BCLR instruction executed

```
BCLR    #0,     @RAM0
```

The BCLR instructions executed for the PCR5 w
(RAM0).

- After executing BCLR instruction

```
MOV.B   @RAM0, R0L
MOV.B   R0L,  @PCR5
```

The work area (RAM0) value is written to PCR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**
Input/output	Input	Input	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1
PDR5	1	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1

External interrupts other than NMI and internal interrupts other than address break a
by the I bit in CCR, and kept masked while the I bit is set to 1. Exception handling s
the current instruction or exception handling ends, if an interrupt request has been is

system use			
Reserved for system use	Break interrupts (mode transition)	2	H'0004 to H'0005
External interrupt	NMI	3	H'0006 to H'0007
Reserved for system use	Break conditions satisfied	4	H'0008 to H'0009
Address break	Break conditions satisfied	5	H'000A to H'000B
External interrupts	IRQ0	6	H'000C to H'000D
	IRQ1	7	H'000E to H'000F
	IRQAEC	8	H'0010 to H'0011
	IRQ3	9	H'0012 to H'0013
	IRQ4	10	H'0014 to H'0015
	WKP0	11	H'0016 to H'0017
	WKP1	12	H'0018 to H'0019
	WKP2	13	H'001A to H'001B
	WKP3	14	H'001C to H'001D
	WKP4	15	H'001E to H'001F
	WKP5	16	H'0020 to H'0021
	WKP6	17	H'0022 to H'0023
	WKP7	18	H'0024 to H'0025
Internal interrupts*	—	19 to 43	H'0026 to H'0056

Note: * For details on the vector table of internal interrupts, refer to section 4.5, Interru Exception Handling Vector Table.

	For details, see section 21, Power-On Reset Circuit.
Watchdog timer	Counter overflow For details, see section 14, Watchdog Timer.

3.2.1 Reset Exception Handling

When a reset source occurs, all processing halts and the LSI enters the reset state. A rese initializes the internal state of the CPU and the registers of on-chip peripheral modules.

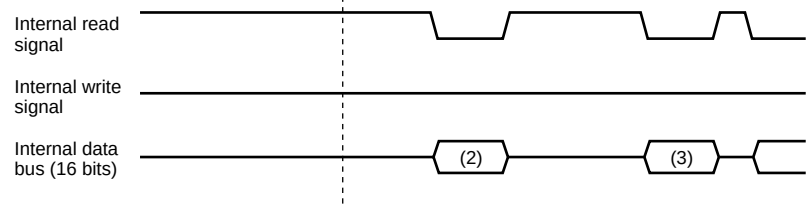
To ensure that this LSI is reset using the $\overline{\text{RES}}$ pin, proceed as follows.

- At power-on, or if the system clock pulse generator is stopped
  Hold the $\overline{\text{RES}}$ pin low until the operation of the clock pulse generator stabilizes.
- If the system clock pulse generator is running
  Hold the $\overline{\text{RES}}$ pin for the duration of the t_{REL} state specified in the electrical character

When a reset source is generated, reset exception handling starts and the LSI performs t following operations.

1. The internal state of the CPU and the registers of the on-chip peripheral modules are and the I bit in CCR is set to 1.
2. The reset exception handling vector address (H'0000 and H'0001) is read and transfe PC, and then program execution starts from the address indicated by the PC.

The reset exception handling sequence triggered by the $\overline{\text{RES}}$ pin is shown in figure 3.1.



(1) Reset exception handling vector address (H'0000)
(2) Program start address
(3) Initial program instruction

Figure 3.1 Reset Exception Handling Sequence

3.2.2 Interrupt Immediately after Reset

Immediately after a reset, if an interrupt is accepted before the stack pointer (SP) is initial and CCR will not be pushed onto the stack correctly, resulting in program runaway. To p this, immediately after reset exception handling all interrupts are masked. For this reason initial program instruction is always executed immediately after a reset. This instruction s initialize the stack pointer (e.g. MOV.L #xx: 32, SP).

NMI is an interrupt with the highest priority and accepted at all times. Interrupts are con
the interrupt controller. The interrupt controller can set interrupts other than NMI to one
mask levels in order to control multiple interrupts. The interrupt priority registers A to E
IPRE) of the interrupt controller set the interrupt mask level.

For details on interrupts, see section 4, Interrupt Controller.

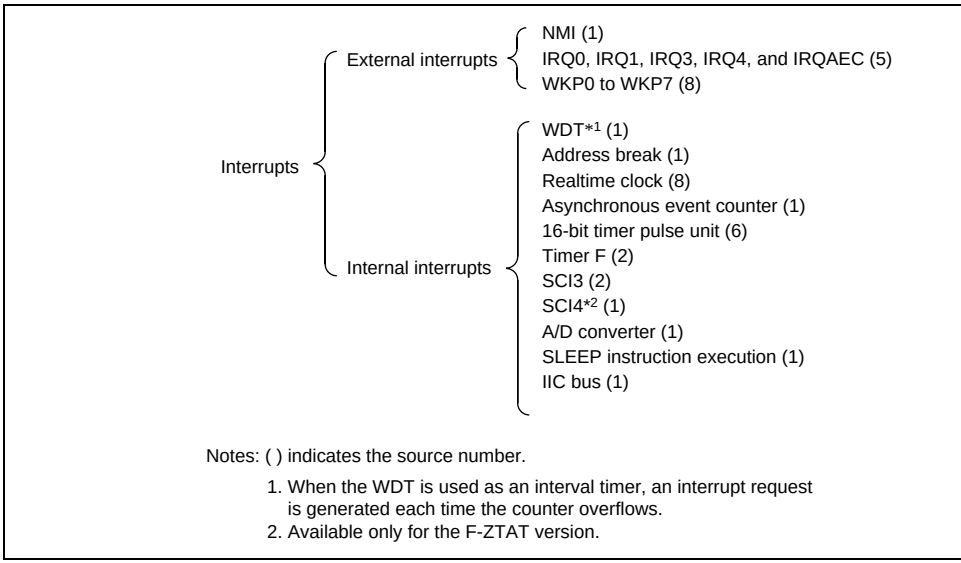
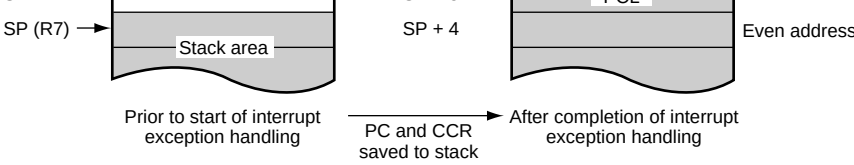


Figure 3.2 Interrupt Sources and their Numbers



[Legend]
PCH: Upper 8 bits of program counter (PC)
PCL: Lower 8 bits of program counter (PC)
CCR: Condition code register
SP: Stack pointer

Notes: 1. PC shows the address of the first instruction to be executed upon return from the interrupt handling routine.
2. Register contents must always be saved and restored by word length, starting from an even-numbered address.
* Ignored when returning from the interrupt handling routine.

Figure 3.3 Stack Status after Exception Handling

Instruction fetch	4
Internal processing	4

Note: * Excluding EEPMOV instruction.

Setting an odd address in SP may cause a program to crash. An example is shown in figu

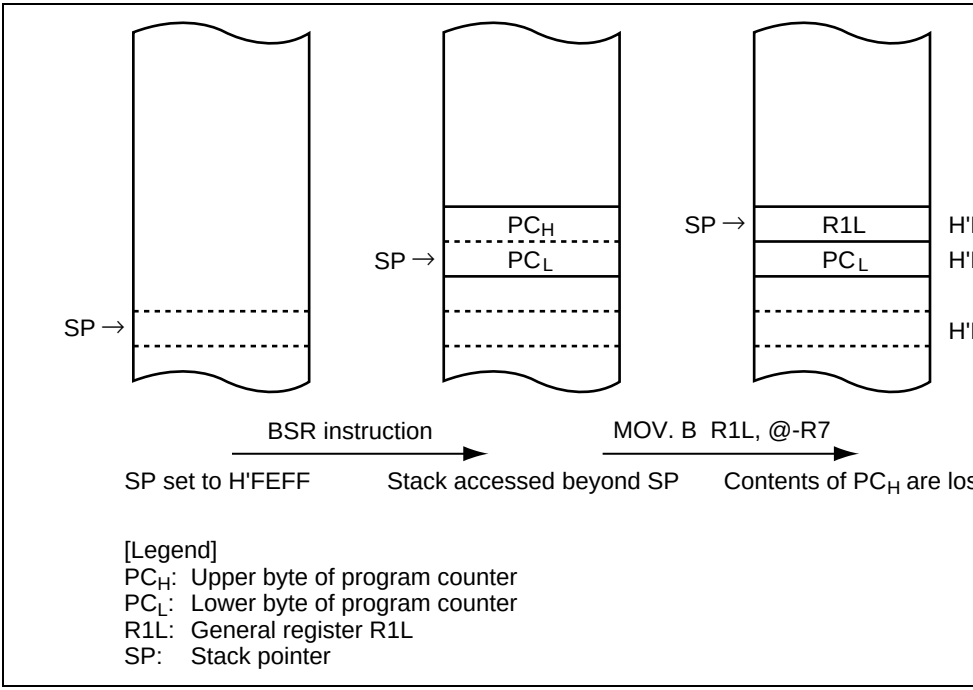


Figure 3.4 Operation when Odd Address is Set in SP

During interrupt exception handling or when an RTE instruction is executed, CCR conten saved and restored in word size. Both the upper and lower bytes of word data are saved to stack; on return, the even address contents are restored to CCR while the odd address con ignored.

request flag may be set to 1, even if a valid edge has not arrived on the selected IRQAEC
IECPWM (PWM output for the AEC). Therefore, be sure to clear the interrupt request f
after switching the pin function.

Table 3.4 shows the conditions under which interrupt request flags are set to 1 in this wa

	IRREC2	When an edge as designated by the AIEGS1 and AIEGS0 bits in A detected because the values of the IRQAEC pin and of IECPWM a switching are different (e.g., when the rising edge has been selecte the ECPWME bit in AEGSR is changed from 1 to 0 while the IRQA low and IECPWM is 1).
	IRRI1	When the IRQ1 bit in PMRB is changed from 0 to 1 while the $\overline{\text{IRQ1}}$ low and the IEG1 bit in IEGR is 0. When the IRQ1 bit in PMRB is changed from 1 to 0 while the $\overline{\text{IRQ1}}$ low and the IEG1 bit in IEGR is 1.
	IRRI0	When the IRQ0 bit in PMRB is changed from 0 to 1 while the $\overline{\text{IRQ0}}$ low and the IEG0 bit in IEGR is 0. When the IRQ0 bit in PMRB is changed from 1 to 0 while the $\overline{\text{IRQ0}}$ low and the IEG0 bit in IEGR is 1.
IWPR	IWPF7	When the WKP7 bit in PMR5 is changed from 0 to 1 while the $\overline{\text{WK}}$ low.
	IWPF6	When the WKP6 bit in PMR5 is changed from 0 to 1 while the $\overline{\text{WK}}$ low.
	IWPF5	When the WKP5 bit in PMR5 is changed from 0 to 1 while the $\overline{\text{WK}}$ low.
	IWPF4	When the WKP4 bit in PMR5 is changed from 0 to 1 while the $\overline{\text{WK}}$ low.
	IWPF3	When the WKP3 bit in PMR5 is changed from 0 to 1 while the $\overline{\text{WK}}$ low.
	IWPF2	When the WKP2 bit in PMR5 is changed from 0 to 1 while the $\overline{\text{WK}}$ low.
	IWPF1	When the WKP1 bit in PMR5 is changed from 0 to 1 while the $\overline{\text{WK}}$ low.
	IWPF0	When the WKP0 bit in PMR5 is changed from 0 to 1 while the $\overline{\text{WK}}$ low.

However, the procedure in figure 3.5 is recommended because IECPWM is an internal s
determining its value is complicated.

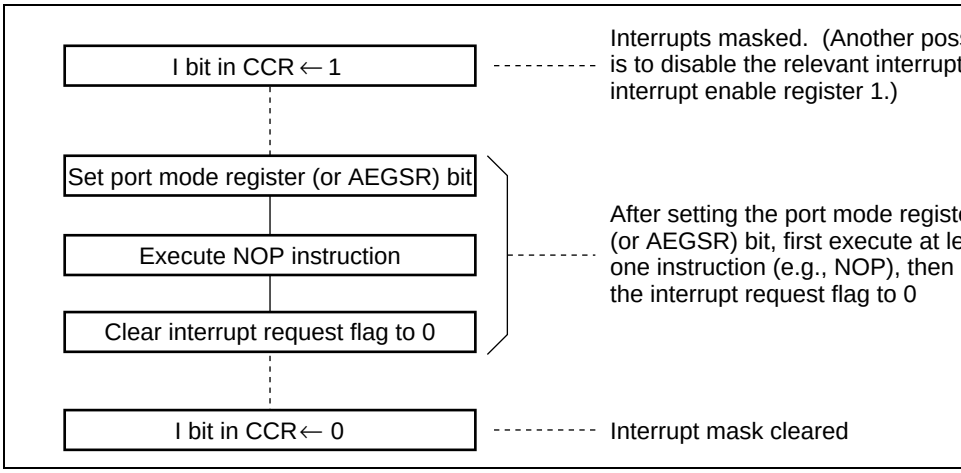


**Figure 3.5 Port Mode Register (or AEGSR) Setting and Interrupt Request I
Clearing Procedure**

```
BCLR  #1,  @IRR1:8

MOV.B R1L, @IRR1:8 (set the value of R1L to B'11111101)
```

(2) Example of a malfunction

When flags are cleared with multiple instructions, other flags might be cleared during exe
the instructions, even though they are currently set, and this will cause a malfunction.

Here is an example in which IRRI0 is cleared and disabled in the process of clearing IRR
in IRR1).

```
MOV.B @IRR1:8,R1L ......... IRRI0 = 0 at this time

AND.B #B'11111101,R1L ..... Here, IRRI0 = 1

MOV.B R1L,@IRR1:8 ......... IRRI0 is cleared to 0
```

In the above example, it is assumed that an IRQ0 interrupt is generated while the AND.B
instruction is executing.

The IRQ0 interrupt is disabled because, although the original objective is clearing IRRI1,
also cleared.

- Interrupts can be enabled or disabled in three levels by the INTM1 and INTM0 bits i interrupt mask register (INTM).
- Fourteen external interrupts

  NMI is the highest-priority interrupt, and is accepted at all times. Rising or falling ed sensing can be selected for NMI. Rising or falling edge sensing can be selected for I IRQ1, IRQ3, IRQ4, and WKP0 to WKP7. Rising, falling, or both edge sensing can b for IRQAEC.

A block diagram of the interrupt controller is shown in figure 4.1.

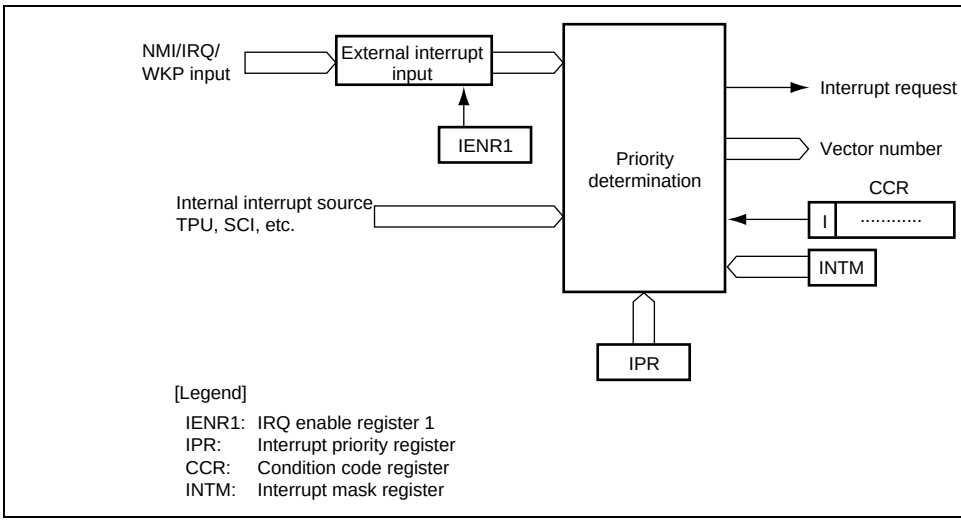


Figure 4.1 Block Diagram of Interrupt Controller

$\overline{\text{IRQ4}}$	Input	Maskable external interrupt pins Rising or falling edge can be selected
$\overline{\text{IRQ3}}$	Input	
$\overline{\text{IRQ1}}$	Input	
$\overline{\text{IRQ0}}$	Input	
$\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$	Input	Maskable external interrupt pins Accepted at a rising or falling edge

4.3 Register Descriptions

The interrupt controller has the following registers.

- Interrupt edge select register (IEGR)
- Wakeup edge select register (WEGR)
- Interrupt enable register 1 (IENR1)
- Interrupt enable register 2 (IENR2)
- Interrupt request register 1 (IRR1)
- Interrupt request register 2 (IRR2)
- Wakeup interrupt request register (IWPR)
- Interrupt priority register A (IPRA)
- Interrupt priority register B (IPRB)
- Interrupt priority register C (IPRC)
- Interrupt priority register D (IPRD)
- Interrupt priority register E (IPRE)
- Interrupt mask register (INTM)

6	TMIFEG	0	R/W	TMIF Edge Select 0: Detects a falling edge of the TMIF pin inpu 1: Detects a rising edge of the TMIF pin inpu
5	ADTRGNEG	0	R/W	$\overline{\text{ADTRG}}$ Edge Select 0: Detects a falling edge of the $\overline{\text{ADTRG}}$ pin in 1: Detects a rising edge of the $\overline{\text{ADTRG}}$ pin in
4	IEG4	0	R/W	IRQ4 Edge Select 0: Detects a falling edge of the $\overline{\text{IRQ4}}$ pin inpu 1: Detects a rising edge of the $\overline{\text{IRQ4}}$ pin inpu
3	IEG3	0	R/W	IRQ3 Edge Select 0: Detects a falling edge of the $\overline{\text{IRQ3}}$ pin inpu 1: Detects a rising edge of the $\overline{\text{IRQ3}}$ pin inpu
2	—	—	—	Reserved
1	IEG1	0	R/W	IRQ1 Edge Select 0: Detects a falling edge of the $\overline{\text{IRQ1}}$ pin inpu 1: Detects a rising edge of the $\overline{\text{IRQ1}}$ pin inpu
0	IEG0	0	R/W	IRQ0 Edge Select 0: Detects a falling edge of the $\overline{\text{IRQ0}}$ pin inpu 1: Detects a rising edge of the $\overline{\text{IRQ0}}$ pin inpu

				0: Detects a falling edge of the $\overline{\text{WKP6}}$ pin input
				1: Detects a rising edge of the $\overline{\text{WKP6}}$ pin input
5	WKEGS5	0	R/W	WKP5 Edge Select
				0: Detects a falling edge of the $\overline{\text{WKP5}}$ pin input
				1: Detects a rising edge of the $\overline{\text{WKP5}}$ pin input
4	WKEGS4	0	R/W	WKP4 Edge Select
				0: Detects a falling edge of the $\overline{\text{WKP4}}$ pin input
				1: Detects a rising edge of the $\overline{\text{WKP4}}$ pin input
3	WKEGS3	0	R/W	WKP3 Edge Select
				0: Detects a falling edge of the $\overline{\text{WKP3}}$ pin input
				1: Detects a rising edge of the $\overline{\text{WKP3}}$ pin input
2	WKEGS2	0	R/W	WKP2 Edge Select
				0: Detects a falling edge of the $\overline{\text{WKP2}}$ pin input
				1: Detects a rising edge of the $\overline{\text{WKP2}}$ pin input
1	WKEGS1	0	R/W	WKP1 Edge Select
				0: Detects a falling edge of the $\overline{\text{WKP1}}$ pin input
				1: Detects a rising edge of the $\overline{\text{WKP1}}$ pin input
0	WKEGS0	0	R/W	WKP0 Edge Select
				0: Detects a falling edge of the $\overline{\text{WKP0}}$ pin input
				1: Detects a rising edge of the $\overline{\text{WKP0}}$ pin input

				This bit is always read as 1.
5	IENWP	0	R/W	Wakeup Interrupt Request Enable The WKP7 to WKP0 interrupt requests are en when this bit is set to 1.
4	IEN4	0	R/W	IRQ4 Interrupt Request Enable The IRQ4 interrupt request is enabled when t set to 1.
3	IEN3	0	R/W	IRQ3 Interrupt Request Enable The IRQ3 interrupt request is enabled when t set to 1.
2	IENEC2	0	R/W	IRQAEC Interrupt Request Enable The IRQAEC interrupt request is enabled whe is set to 1.
1	IEN1	0	R/W	IRQ1 Interrupt Request Enable The IRQ1 interrupt request is enabled when t set to 1.
0	IEN0	0	R/W	IRQ0 Interrupt Request Enable The IRQ0 interrupt request is enabled when t set to 1.

6	IENAD	0	R/W	A/D Converter Interrupt Request Enable The A/D converter interrupt request is enabled this bit is set to 1.
5	—	0	R/W	Reserved This bit is read/write enable reserved bit.
4	—	1	R/W	Reserved This bit is always read as 1.
3	IENTFH	0	R/W	Timer FH Interrupt Request Enable The timer FH interrupt request is enabled when is set to 1.
2	IENTFL	0	R/W	Timer FL Interrupt Request Enable The timer FL interrupt request is enabled when is set to 1.
1	—	1	R/W	Reserved This bit is always read as 1.
0	IENEC	0	R/W	Asynchronous Event Counter Interrupt Reques The asynchronous event counter interrupt requ enabled when this bit is set to 1.

				When the IRQ4 pin is set as the interrupt inpu the specified edge is detected [Clearing condition] When 0 is written to this bit
3	IRRI3	0	R/(W)*	IRQ3 Interrupt Request Flag [Setting condition] When the IRQ3 pin is set as the interrupt inpu the specified edge is detected [Clearing condition] When 0 is written to this bit
2	IRREC2	0	R/(W)*	IRQAEC Interrupt Request Flag [Setting condition] When the IRQAEC pin is set as the interrupt i and the specified edge is detected [Clearing condition] When 0 is written to this bit
1	IRRI1	0	R/(W)*	IRQ1 Interrupt Request Flag [Setting condition] When the IRQ1 pin is set as the interrupt inpu the specified edge is detected [Clearing condition] When 0 is written to this bit

4.3.6 Interrupt Request Register 2 (IRR2)

IRR2 indicates the interrupt request status of the direct transition, A/D converter, timer F, asynchronous event counter.

Bit	Bit Name	Initial Value	R/W	Description
7	IRRDT	0	R/(W)*	Direct Transition Interrupt Request Flag [Setting condition] When the SLEEP instruction is executed and d transition is made while the DTON bit in SYSC to 1 [Clearing condition] When 0 is written to this bit
6	IRRAD	0	R/(W)*	A/D Converter Interrupt Request Flag [Setting condition] When A/D conversion ends [Clearing condition] When 0 is written to this bit
5	—	0	R	Reserved This bit is always read as 0.
4	—	1	R/W	Reserved This bit is always read as 1.

				[Clearing condition] When 0 is written to this bit
1	—	1	R/W	Reserved This bit is always read as 1.
0	IRREC	0	R/(W)*	Asynchronous Event Counter Interrupt Reque [Setting condition] When the asynchronous event counter overfl [Clearing condition] When 0 is written to this bit

Note: * Only a write of 0 for flag clearing is possible.

				[Clearing condition]
				When 0 is written to this bit
6	IWPF6	0	R/W	WKP6 Interrupt Request Flag
				[Setting condition]
				When the $\overline{\text{WKP6}}$ pin is set as the interrupt inpu the specified edge is detected
				[Clearing condition]
				When 0 is written to this bit
5	IWPF5	0	R/W	WKP5 Interrupt Request Flag
				[Setting condition]
				When the $\overline{\text{WKP5}}$ pin is set as the interrupt inpu the specified edge is detected
				[Clearing condition]
				When 0 is written to this bit
4	IWPF4	0	R/W	WKP4 Interrupt Request Flag
				[Setting condition]
				When the $\overline{\text{WKP4}}$ pin is set as the interrupt inpu the specified edge is detected
				[Clearing condition]
				When 0 is written to this bit
3	IWPF3	0	R/W	WKP3 Interrupt Request Flag
				[Setting condition]
				When the $\overline{\text{WKP3}}$ pin is set as the interrupt inpu the specified edge is detected
				[Clearing condition]
				When 0 is written to this bit

				When the $\overline{\text{WKP1}}$ pin is set as the interrupt inp the specified edge is detected [Clearing condition] When 0 is written to this bit
0	IWPF0	0	R/W	WKP0 Interrupt Request Flag [Setting condition] When the $\overline{\text{WKP0}}$ pin is set as the interrupt inp the specified edge is detected [Clearing condition] When 0 is written to this bit

6	IPRn6	0	R/W	source. 00: Mask level 0 (Lowest) 01: Mask level 1 1*: Mask level 2 (Highest)
5	IPRn5	0	R/W	Set the mask level of the corresponding interru
4	IPRn4	0	R/W	source. 00: Mask level 0 (Lowest) 01: Mask level 1 1*: Mask level 2 (Highest)
3	IPRn3	0	R/W	Set the mask level of the corresponding interru
2	IPRn2	0	R/W	source. 00: Mask level 0 (Lowest) 01: Mask level 1 1*: Mask level 2 (Highest)
1	IPRn1	0	R/W	Set the mask level of the corresponding interru
0	IPRn0	0	R/W	source. 00: Mask level 0 (Lowest) 01: Mask level 1 1*: Mask level 2 (Highest)

[Legend] *: Don't care.
n = A to E

0	INTM0	0	R/W	1*: Mask an interrupt with mask level 1 or les 01: Mask an interrupt with mask level 0 00: Accept all interrupts

[Legend] *: Don't care.

4.4 Interrupt Sources

4.4.1 External Interrupts

There are 14 external interrupts: NMI, WKP7 to WKP0, IRQ4, IRQ3, IRQAEC, IRQ1,

(1) NMI Interrupt

NMI is the highest-priority interrupt, and is always accepted by the CPU regardless of th
the I bit in CCR. The NMIEG bit in IEGR can be used to select whether an interrupt is r
at a rising edge or a falling edge on the NMI pin.

(2) WKP7 to WKP0 Interrupts

WKP7 to WKP0 interrupts are requested by the rising or falling edge input signals at the
$\overline{\text{WKP0}}$ pins.

When the rising or falling edge is input while the $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$ pin functions are sele
PMR5, the corresponding bit in IWPR is set to 1 and an interrupt request is generated.

Clearing the IENWP bit in IENR1 to 0 disables the wakeup interrupt request to be accep
Setting the I bit in CCR to 1 masks all interrupts.

selected by PMRB and PMR9, the corresponding bit in IRR1 is set to 1 and an interrupt r
generated.

Clearing the IEN4, IEN3, IEN1, and IEN0 bits in IENR1 to 0 disables the interrupt reque
accepted. Setting the I bit in CCR to 1 masks all interrupts.

The interrupt mask level can be set by IPR.

(4) IRQAEC Interrupts

An IRQAEC interrupt is requested by an input signal at the IRQAEC pin or IECPWM (P
output for the AEC). When the IRQAEC pin is used as an external interrupt pin, clear the
ECPWME bit in AEGSR to 0.

Using the AIEGS1 and AIEGS0 bits in AEGSR, it is possible to select whether an interru
generated by a rising edge, falling edge, or both edges.

When the IENEC2 bit in IENR1 is set to 1 and the specified edge is input, the correspond
IRR1 is set to 1 and an interrupt request is generated.

When exception handling for the IRQAEC interrupt is accepted, the I bit in CCR is set to

The interrupt mask level can be set by IPR.

4.5 Interrupt Exception Handling Vector Table

Table 4.2 shows interrupt exception handling sources, vector addresses, and interrupt pr
The lower the vector number, the higher the priority. The priority within a module is fix
levels for interrupts other than NMI and address break can be modified by IPR.

	IRQ3	9	H'0012	IPRA1, IPRA0
	IRQ4	10	H'0014	
	WKP0	11	H'0016	IPRB7, IPRB6
	WKP1	12	H'0018	
	WKP2	13	H'001A	
	WKP3	14	H'001C	
	WKP4	15	H'001E	
	WKP5	16	H'0020	
	WKP6	17	H'0022	
	WKP7	18	H'0024	
RTC	0.25-second overflow	19	H'0026	IPRB5, IPRB4
	0.5-second overflow	20	H'0028	
	Second periodic overflow	21	H'002A	
	Minute periodic overflow	22	H'002C	
	Hour periodic overflow	23	H'002E	
	Day-of-week periodic overflow	24	H'0030	
	Week periodic overflow	25	H'0032	
	Free-running overflow	26	H'0034	

	capture/compare match)			
	TG2B (TG2B input capture/compare match)	33	H'0042	
	TCI2V (overflow 2)	34	H'0044	
Timer F	Timer FL compare match Timer FL overflow	35	H'0046	IPRC3, IPRC2
	Timer FH compare match Timer FH overflow	36	H'0048	
SCI4*	Receive data full/transmit data empty Transmit end/receive error	37	H'004A	IPRC1, IPRC0
SCI3_1	Transmit completion/transmit data empty Receive data full/overrun error Framing error/parity error	38	H'004C	IPRD7, IPRD6
SCI3_2	Transmit completion/transmit data empty Receive data full/overrun error Framing error/parity error	39	H'004E	IPRD5, IPRD4
IIC	Transmit data empty/transmit end Receive data full/overrun error NACK detection Arbitration/overrun error	40	H'0050	IPRD3, IPRD2
10-bit A/D	A/D conversion end	42	H'0054	IPRE7, IPRE6
(SLEEP instruction execution)	Direct transition	43	H'0056	IPRE5, IPRE4

Note: * Supported only by the F-ZTAT version.

Four-level interrupt masking is controlled according to the combination of the I bit in CC
INTM1 and INTM0 bits in INTM.

Table 4.3 Interrupt Control States

CCR	INTM		
I	**INTM1**	**INTM0**	**States**
1	*	*	All interrupts other than NMI and address break are mas
0	1	*	Interrupts with mask level 1 or less are masked.
	0	1	Interrupts with mask level 0 are masked.
	0	0	All interrupts are accepted.

[Legend]*: Don't care.

1. If an interrupt source whose enable bit is set to 1 occurs, an interrupt request is sent to interrupt controller.
2. The following control operations are performed by referencing the INTM1 and INTM INTM and the I bit in CCR.
   - When the I bit is set to 1, the interrupt request is held pending.
   - When the I bit is cleared to 0 and the INTM1 bit is set to 1, interrupts with mask l below are held pending.
   - When the I bit is cleared to 0, the INTM1 bit is cleared to 0, and the INTM0 bit is interrupt requests with mask level 0 are held pending.
   - When the I bit, INTM1 bit, and INTM0 bit are all cleared to 0, all interrupt reques accepted.
3. If contention occurs between interrupts that are not held pending by the INTM1 and I bits in the INTM register and the I bit in CCR, the interrupt with the highest priority a in table 4.2 is selected, regardless of the IPR setting.

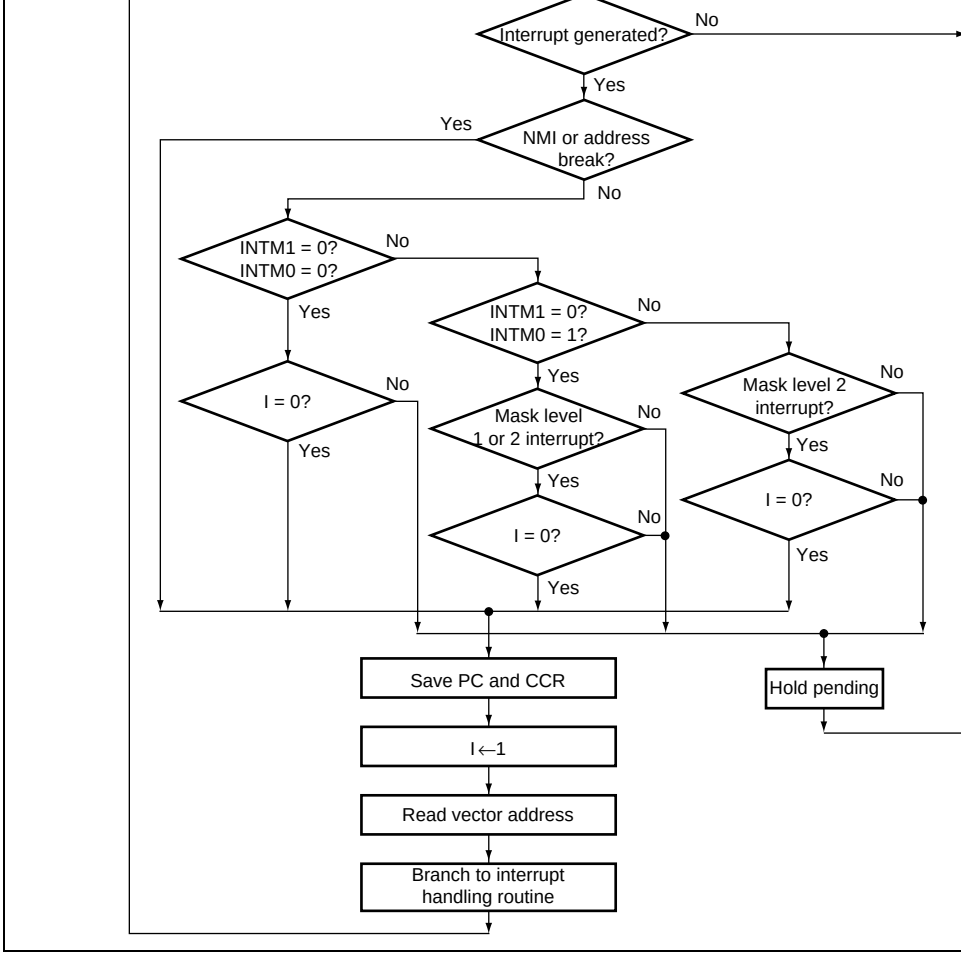


Figure 4.2 Flowchart of Procedure Up to Interrupt Acceptance

Figure 4.3 Interrupt Exception Handling Sequence

3	PC, CCR stack	4
4	Vector fetch	4
5	Instruction fetch*[2]	4
6	Internal processing*[3]	4
	Total	19 to 41

Notes: 1. One state for internal interrupts and two states for external interrupts.
2. Prefetch after interrupt acceptance and interrupt handling routine prefetch.
3. Internal processing after interrupt acceptance and internal processing after vec

will be executed for the higher-priority interrupt, and the lower-priority interrupt will be
The same also applies when an interrupt source flag is cleared to 0.

Figure 4.4 shows an example in which the TGIEA bit in TIER of the 16-bit timer pulse
is cleared to 0.

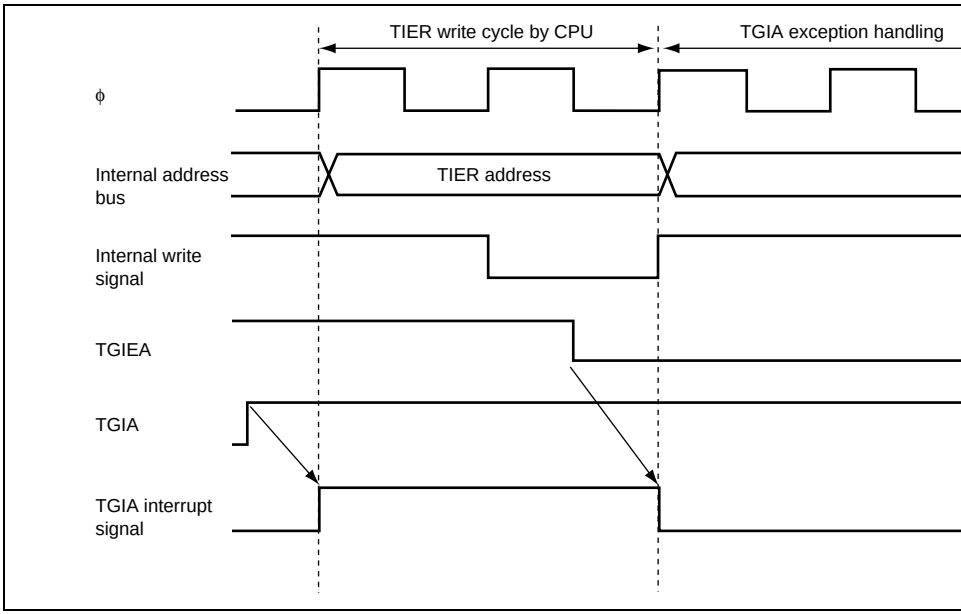


Figure 4.4 Contention between Interrupt Generation and Disabling

The above contention will not occur if an enable bit or interrupt source flag is cleared to
the interrupt is masked.

Interrupt operation differs between the EEPMOV.B instruction and the EEPMOV.W inst

With the EEPMOV.B instruction, an interrupt request (including NMI) issued during tran not accepted until the transfer is completed.

With the EEPMOV.W instruction, even if an interrupt request other than the NMI is issue transfer, the interrupt is not accepted until the transfer is completed. If the NMI interrupt issued, NMI exception handling starts at a break in the transfer cycle. The PC value saved stack in this case is the address of the next instruction.

Therefore, if an NMI interrupt is generated during execution of an EEPMOV.W instructio following coding should be used.

```
L1: EEPMOV.W
    MOV.W     R4,R4
    BNE       L1
```

4.7.4 IENR Clearing

When an interrupt request is disabled by clearing the interrupt enable register or when the request register is cleared, the interrupt request should be masked (I bit = 1). If the above is executed while the I bit is 0 and contention between the instruction execution and the in request generation occurs, exception handling, which corresponds to the interrupt request generated after instruction execution of the above operation is completed, is executed.

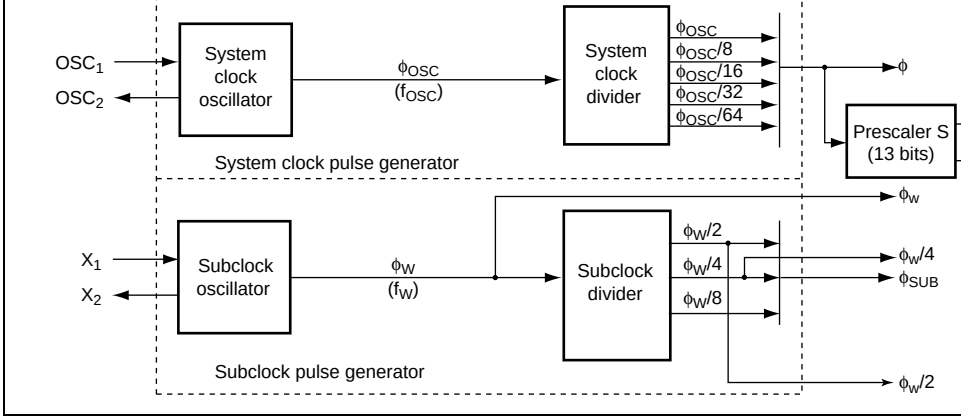
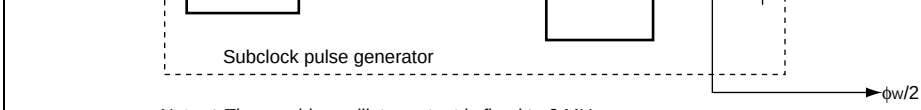


Figure 5.1 Block Diagram of Clock Pulse Generators (Flash Memory Versio



Note: * The on-chip oscillator output is fixed to 3 MHz.

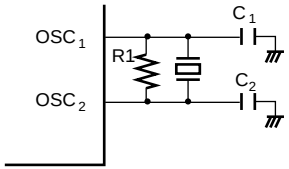
Figure 5.1 Block Diagram of Clock Pulse Generators (Masked ROM Version)

The basic clock signals that drive the CPU and on-chip peripheral modules are ϕ and ϕ_{SUB} system clock is divided by prescaler S to become a clock signal from $\phi/8192$ to $\phi/2$. Both system clock and subclock signals are provided to the on-chip peripheral modules.

Since the on-chip oscillator is available for the masked ROM version, the reference clock selected to be output from the on-chip oscillator or system clock oscillator by the input le IRQAEC pin.

Bit	Bit Name	Value	R/W	Description
7	32KSTOP	0	R/W	Subclock Oscillator Operation Control 0: Subclock oscillator operates 1: Subclock oscillator stops
6	—	0	R/W	Reserved This bit is readable/writable.
5 to 0	—	All 0	—	Reserved These bits cannot be modified.

2	IRQAECF		R	IRQAEC flag This bit indicates the IRQAEC pin input level se resets. 0: IRQAEC pin set to GND during resets 1: IRQAEC pin set to Vcc during resets
1	OSCF	—	R	OSC flag This bit indicates the oscillator operating with th clock pulse generator. 0: System clock oscillator operating (on-chip os stopped) 1: On-chip oscillator operating (system clock os stopped)
0	—	0	R/W	Reserved Never write 1 to this bit, as it can cause the LSI malfunction.



R1 = 1 MΩ ±20%

Note: Consult with the crystal resonator manufacturer to determine the circuit constants.

Frequency	Manufacturer	Product Type	C_1, C_2 Recommendation
4.19 MHz	Kyocera Kinseki Corporation	HC-491U-S	22 pF ±20%

Figure 5.2 Typical Connection to Crystal Resonator

	Co., Ltd.	CSTLS4M19G56-B0	47pF (on-chip)

Figure 5.3 Typical Connection to Ceramic Resonator

5.2.3 External Clock Input Method

Connect an external clock signal to pin OSC1, and leave pin OSC2 open. Figure 5.4 show typical connection. The duty cycle of the external clock signal must be 45 to 55%.

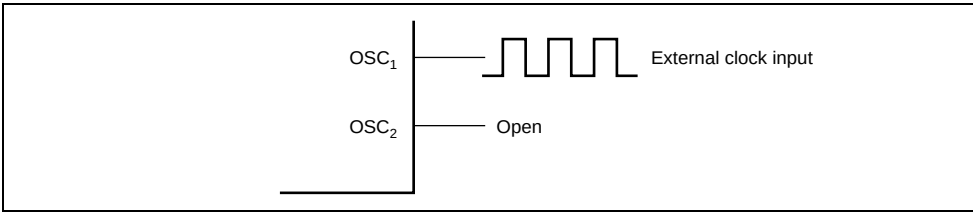


Figure 5.4 Example of External Clock Input

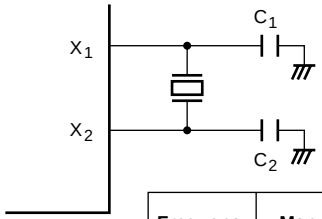
5.2.4 On-Chip Oscillator Selection Method (Supported only by the Masked ROM Version)

The on-chip oscillator is selected by the input level of the IRQAEC pin during a reset. Th selection method of the system clock oscillator and the on-chip oscillator is listed in table input level of the IRQAEC pin during a reset* should be fixed either to Vcc or GND, dep on the oscillator type to be selected. The setting takes effect when the rest is cleared. Whe chip oscillator is selected, to connect a resonator to OSC1 or OSC2 is not necessary. In th the OSC1 pin should be fixed to Vcc or GND.

Note: * This reset represents an external reset or power-on reset, but not a reset by the watchdog timer.

Clock pulses can be supplied to the subclock generator by connecting a 32.768-kHz or 3
crystal resonator, as shown in figure 5.5. Notes described in section 5.5.2, Notes on Boa
also apply to this connection.

The 32KSTOP bit in the SUB32CR register can stop the subclock oscillator with the sub
oscillator program. To stop the subclock oscillator, set the SUB32CR register in active m
When restoring from the subclock stopped condition, use the subclock after the oscillati
stabilization time has elapsed, as the same as for the power supply.



Note: Consult with the crystal resonator manufacturer to determine the circuit constants.

Frequency	Manufacturer	Products Name	C_1, C_2 Recommendation Value	Equivalent S Resistan
38.4 kHz	Epson Toyocom	C-4-TYPE	7 pF	30 kΩ m
32.768 kHz	Epson Toyocom	C-001R	7 pF	35 kΩ m

Figure 5.5 Typical Connection to 32.768-kHz/38.4-kHz Crystal Resonato

Figure 5.6 shows the equivalent circuit of the crystal resonator.

Notes on Use of Subclock Generator Circuit

The drive capacity of the subclock generator circuit is limited in order to reduce current consumption when operating in the subclock mode. As a result, there may not be sufficie additional margin to accommodate some resonators. Be sure to select a resonator with an equivalent series resistance (R_S) corresponding to that shown in figure 5.6.

5.3.2 Pin Connection when not Using Subclock

When the subclock is not used, connect the X_1 pin to GND and leave the X_2 pin open, as s figure 5.7.

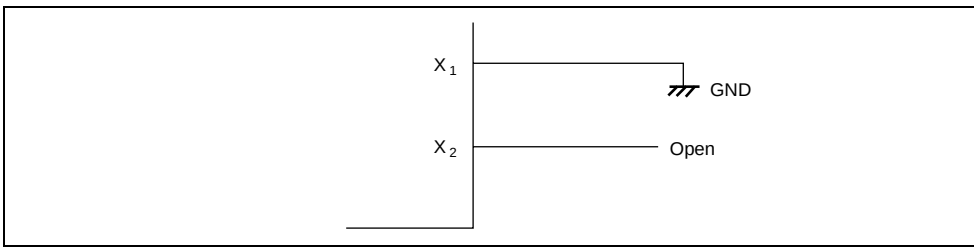


Figure 5.7 Pin Connection when not Using Subclock

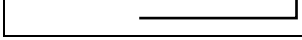


Figure 5.8 Pin Connection when Inputting External Clock

Frequency	Subclock (ϕw)
Duty	45% to 55%

5.4 Prescalers

This LSI is equipped with an on-chip prescaler (prescaler S).

Prescaler S is a 13-bit counter using the system clock (ϕ) as its input clock. Its prescaled
provide internal clock signals for on-chip peripheral modules.

5.4.1 Prescaler S

Prescaler S is a 13-bit counter using the system clock (ϕ) as its input clock. A divided ou
used as an internal clock of an on-chip peripheral module. Prescaler S is initialized to H
reset, and starts counting up on exit from the reset state. In standby mode, watch mode,
mode, and subsleep mode, the system clock pulse generator stops. Prescaler S also stops
initialized to H'0000. The CPU cannot read from or write to prescaler S.

The output from prescaler S is shared by the on-chip peripheral modules. In active (med
speed) mode and sleep (medium-speed) mode, the clock input to prescaler S is determin
division ratio designated by the MA1 and MA0 bits in SYSCR2.

resonator arrangement.

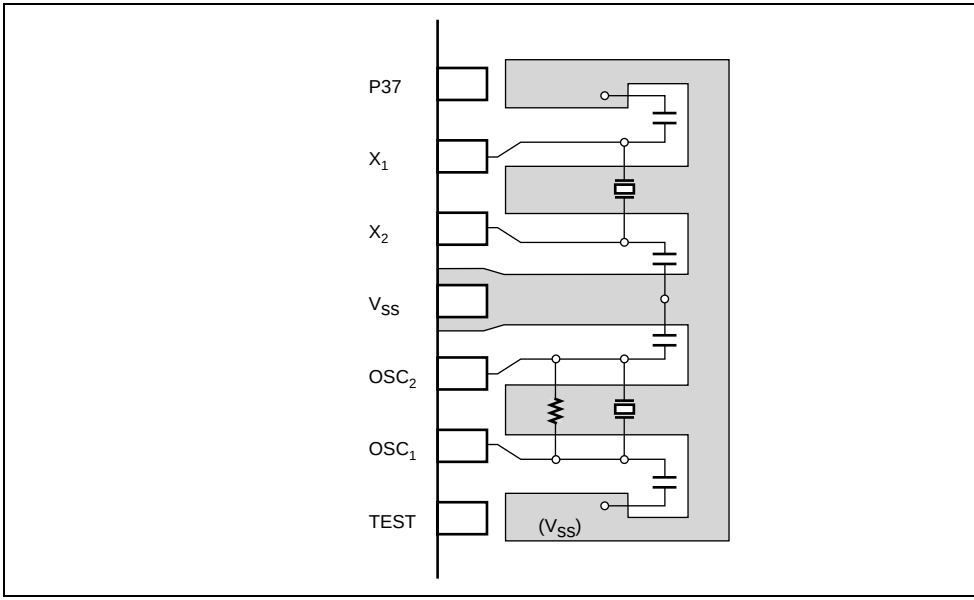
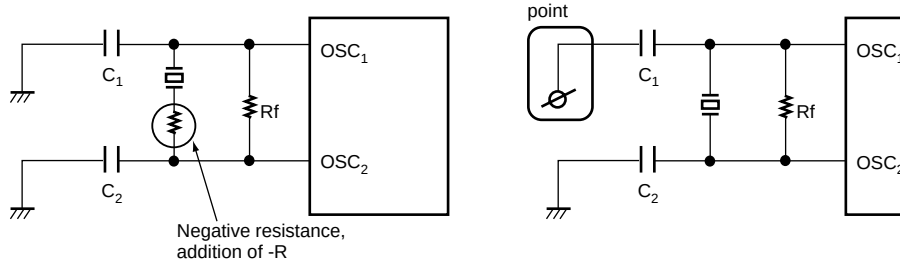
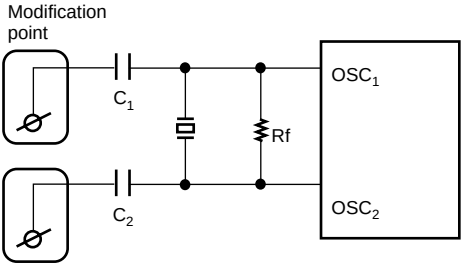


Figure 5.9 Example of Crystal and Ceramic Resonator Arrangement

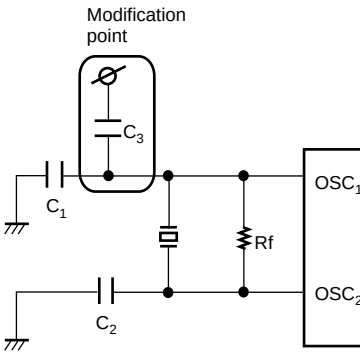


(1) Negative Resistance Measuring Circuit

(2) Oscillator Circuit Modification Suggest



(3) Oscillator Circuit Modification Suggestion 2



(4) Oscillator Circuit Modification Suggestio

Figure 5.10 Negative Resistance Measurement and Circuit Modification Sugg

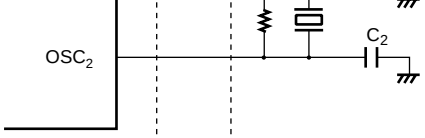


Figure 5.11 Example of Incorrect Board Design

Note: When a crystal resonator or ceramic resonator is connected, consult with the crys resonator and ceramic resonator manufacturers to determine the circuit constants the constants differ according to the resonator, stray capacitance of the mounting and so on.

5.5.3 Definition of Oscillation Stabilization Wait Time

Figure 5.12 shows the oscillation waveform (OSC2), system clock (ϕ), and microcomput operating mode when a transition is made from standby mode, watch mode, or subactive active (high-speed/medium-speed) mode, with an resonator connected to the system cloc oscillator.

As shown in figure 5.12, when a transition is made from a mode in which the system cloc oscillator is halted to active (high-speed/medium-speed) mode, the sum of the following t (oscillation start time and wait time) is required.

(1) Oscillation Start Time

The time from the point at which the system clock oscillator oscillation waveform starts t when an interrupt is generated, until generation of the system clock starts.

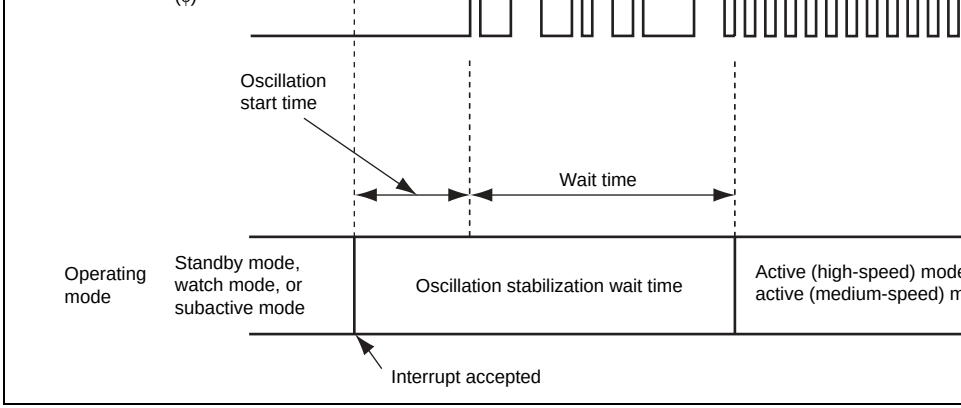


Figure 5.12 Oscillation Stabilization Wait Time

The required the oscillation stabilization time is the same as the “oscillation stabilizatio
at power-on specified in the AC characteristics. Set STS2 to STS0 in SYSCR1 so that th
is equal to or greater than t_{RC}.

If a resonator is connected to the system clock oscillator, it is important to carefully eva
characteristics of the actual circuitry mounted on the board when a transition is made fr
mode, watch mode, or subactive mode to active (high-speed/medium-speed) mode. Set a
that will allow sufficient increase in the oscillation amplitude of OSC1 and OSC2. The o
start time will differ depending on the mounted circuitry constants and stray capacitance
Therefore, consult with the manufacturer of the resonator when setting the oscillation st
wait time.

the power supply potential. In this state, the oscillation waveform may be disrupted, leadi
unstable system clock and incorrect operation of the microcomputer.

If incorrect operation occurs, change the setting of the standby timer select bits 2 to 0 (ST
STS0) (bits 6 to 4 in the system control register 1 (SYSCR1)) to give a longer wait time.

For example, if incorrect operation occurs with a wait time setting of 1,024 states, check
operation with a wait time setting of 2,048 states or more.

If the same kind of incorrect operation occurs after a reset as after a state transition, hold
pin low for a longer period.

5.5.6 Note on Using Power-On Reset Circuit

The LSI's internal power-on reset circuit can be adjusted by connecting an external capac
the $\overline{\text{RES}}$ pin. Adjust the capacitance of the external capacitor to ensure sufficient oscillati
stabilization time before reset clearing. For details, see section 21, Power-On Reset Circu

- Subactive mode

  The CPU and all on-chip peripheral modules are operable on the subclock. The subc
  frequency can be selected from ϕw/2, ϕw/4, and ϕw/8.
- Sleep (high-speed) mode

  The CPU halts. On-chip peripheral modules are operable on the system clock.
- Sleep (medium-speed) mode

  The CPU halts. On-chip peripheral modules are operable on the system clock. The sy
  clock frequency can be selected from ϕosc/8, ϕosc/16, ϕosc/32, and ϕosc/64.
- Subsleep mode

  The CPU halts. The on-chip peripheral modules are operable on the subclock. The su
  frequency can be selected from ϕw/2, ϕw/4, and ϕw/8.
- Watch mode

  The CPU halts. The on-chip peripheral modules are operable on the subclock.
- Standby mode

  The CPU and all on-chip peripheral modules halt.
- Module standby function

  Independent of the above modes, power consumption can be reduced by halting on-c
  peripheral modules that are not used in module units.

Note: In this manual, active (high-speed) mode and active (medium-speed) mode are c
called active mode.

SYSCR1 controls the power-down modes, as well as SYSCR2.

Bit	Bit Name	Initial Value	R/W	Description
7	SSBY	0	R/W	Software Standby Selects the mode to transit after the execution SLEEP instruction. 0: A transition is made to sleep mode or subsle 1: A transition is made to standby mode or wat For details, see table 6.2.
6	STS2	0	R/W	Standby Timer Select 2 to 0 Designate the time the CPU and peripheral mo wait for stable clock operation after exiting from mode, subactive mode, subsleep mode, or wat to active mode or sleep mode due to an interru designation should be made according to the o frequency so that the waiting time is at least eq oscillation stabilization time. The relationship b the specified value and the number of wait stat shown in table 6.1. When an external clock is to be used, the minir value (STS2 = 1, STS1 = 0, STS0 = 1) is recon If the internal oscillator is used, the settings CT STS = 1, and STS0 = 0 are recommended. If the setting other than the recommended valu made, operation may start before the end of th time.
5	STS1	0	R/W	
4	STS0	0	R/W	

0	MA0	1	R/W	Select the operating clock frequency in active speed) mode and sleep (medium-speed) mod MA1 and MA0 bits should be written to in acti speed) mode or subactive mode. 00: ϕOSC/8 01: ϕOSC/16 10: ϕOSC/32 11: ϕOSC/64

Table 6.1 Operating Frequency and Waiting Time

Bit				Operating Frequency		
STS2	**STS1**	**STS0**	**Waiting Time**	**2 MHz**	**4.19 MHz**	**10**
0	0	0	8,192 states	4.1	1.953	0.
		1	16,384 states	8.2	3.907	1.
	1	0	1,024 states	0.512	0.244	0.
		1	2,048 states	1.024	0.488	0.
1	0	0	4,096 states	2.048	0.977	0.
		1	2 states (external clock input)	0.001	0.0005	0.
	1	0	8 states	0.004	0.0019	0.
		1	16 states	0.008	0.0038	0.

Note: Time unit is ms.
When an external clock is input, bits STS2 to STS0 should be set as external cloc mode before mode transition is executed. When an external clock is not used, the should not be set as external clock input mode.

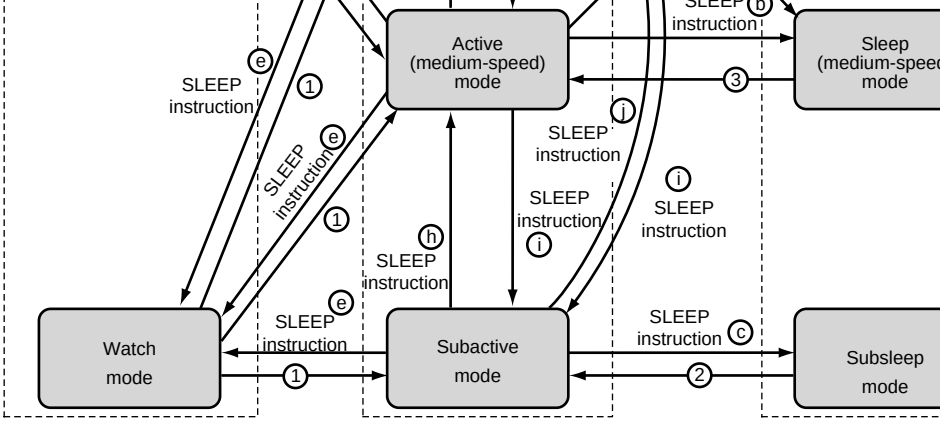
				generates the oscillator clock (ϕ_{OSC}). This bit sel sampling frequency of ϕ_{OSC} when ϕ_w is sampled ϕ_{OSC} = 2 to 10 MHz, clear this bit to 0. Set it to 1 internal oscillator is used. 0: Sampling rate is ϕ_{OSC}/16. 1: Sampling rate is ϕ_{OSC}/4.
3	DTON	0	R/W	Direct Transfer on Flag Selects the mode to which the transition is mad the SLEEP instruction is executed with bits SSI TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2. For details, see table 6.2.
2	MSON	0	R/W	Medium Speed on Flag After standby, watch, or sleep mode is cleared, selects active (high-speed) or active (medium-s mode. 0: Operation in active (high-speed) mode 1: Operation in active (medium-speed) mode
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	Select the operating clock frequency in subacti subsleep modes. The values of SA1 and SA0 c change if they are written to in subactive mode 00: ϕ_w/8 01: ϕ_w/4 1X: ϕ_w/2

[Legend] X: Don't care.

6	S31CKSTP	1	R/W	SCI3 Module Standby*[2] SCI31 enters standby mode when this bit is c 0.
5	S32CKSTP	1	R/W	SCI3 Module Standby*[2] SCI32 enters standby mode when this bit is c 0.*[1]
4	ADCKSTP	1	R/W	A/D Converter Module Standby A/D converter enters standby mode when thi cleared to 0.
3	—	1	R/W	Reserved This readable/writable bit is reserved.
2	TFCKSTP	1	R/W	Timer F Module Standby Timer F enters standby mode when this bit is 0.
1	FROMCKSTP*[1] *[4]	1	R/W*[1]	Flash Memory Module Standby Flash memory enters standby mode when thi cleared to 0.
0	RTCCKSTP	1	R/W	RTC Module Standby RTC enters standby mode when this bit is cle

				The IIC2 enters standby mode when this bit is 0.
4	PW2CKSTP	1	R/W	PWM2 Module Standby The PWM2 enters standby mode when this bit to 0.
3	AECCKSTP	1	R/W	Asynchronous Event Counter Module Standby The asynchronous event counter enters standb when this bit is cleared to 0.
2	WDCKSTP	1	R/W*[3]	Watchdog Timer Module Standby The watchdog timer enters standby mode when is cleared to 0.
1	PW1CKSTP	1	R/W	PWM1 Module Standby The PWM1 enters standby mode when this bit to 0.
0	LDCKSTP	1	R/W	LCD Module Standby The LCD controller/driver enters standby mode this bit is cleared to 0.

Notes: 1. This is a reserved bit which is not readable/writable in the masked ROM versio
2. When the SCI module standby is set, all registers in the SCI3 enter the reset s
3. This bit is valid when the WDON bit in TCSRW is 0. If this bit is cleared to 0 wh WDON bit is set to 1 (while the watchdog timer is operating), this bit is cleared However, the watchdog timer does not enter module standby mode and contin operating. When the watchdog timer stops operating and the WDON bit is clea by software, this bit is valid and the watchdog timer enters module standby mo
4. This bit should be set to 1 when the on-chip debugger is used.



Mode Transition Conditions (1)

	LSON	MSON	SSBY	TMA3	DTON
ⓐ	0	0	0	*	0
ⓑ	0	1	0	*	0
ⓒ	1	*	0	1	0
ⓓ	0	*	1	0	0
ⓔ	*	*	1	1	0
ⓕ	0	0	0	*	1
ⓖ	0	1	0	*	1
ⓗ	0	1	1	1	1
ⓘ	1	*	1	1	1
ⓙ	0	0	1	1	1

* Don't care

Mode Transition Conditions (2)

	Interrupt Sources
①	RTC, timer F, IRQ0 interrupt, AEC, WKP7 to WKP0 interrupts
②	RTC, timer F, TPU, SCI3 interrupt, IRQ4 IRQ1, IRQ0, IRQAEC interrupts, WKP7 interrupts, AEC
③	All interrupts
④	IRQ1, IRQ0, WKP7 to WKP0 interrupts, AEC

Note: A transition between different modes cannot be made to occur simply because an interrupt request is generated. Make sure to enable interrupt requests.

Figure 6.1 Mode Transition Diagram

					(medium-speed) mode	(medium-speed) mode	
0	0	1	0	0	Standby mode	Active (high-speed) mode	d
0	1	1	0	0	Standby mode	Active (medium-speed) mode	d
0	0	1	1	0	Watch mode	Active (high-speed) mode	e
0	1	1	1	0	Watch mode	Active (medium-speed) mode	e
1	*	1	1	0	Watch mode	Subactive mode	e
0	0	0	*	1	Active (high-speed) mode (direct transition)	—	—
0	1	0	*	1	Active (medium-speed) mode (direct transition)	—	g
1	*	1	1	1	Subactive mode (direct transition)	—	i

					mode		
0	0	1	0	0	Standby mode	Active (high-speed) mode	d
0	1	1	0	0	Standby mode	Active (medium-speed) mode	d
0	0	1	1	0	Watch mode	Active (high-speed) mode	e
0	1	1	1	0	Watch mode	Active (medium-speed) mode	e
1	1	1	1	0	Watch mode	Subactive mode	e
0	0	0	*	1	Active (high-speed) mode (direct transition)	—	f
0	1	0	*	1	Active (medium-speed) mode (direct transition)	—	—
1	*	1	1	1	Subactive mode (direct transition)	—	i

					speed) mode		
1	*	1	1	0	Watch mode	Subactive mode	e
0	0	1	1	1	Active (high-speed) mode (direct transition)	—	j
0	1	1	1	1	Active (medium-speed) mode (direct transition)	—	h
1	*	1	1	1	Subactive mode (direct transition)	—	—

[Legend] *: Don't care.

	IRQ1					Retained[1]		
	IRQ3							
	IRQ4							
	IRQAEC							
	WKP7 to WKP0					Functioning		
Peripheral modules	RTC	Functioning	Functioning	Functioning	Functioning	Functioning/ retained*[9]	Functioning/ retained*[9]	Functioning/ retained*[9]
	Asynchronous event counter					Functioning*[6]	Functioning	Functioning
	Timer F					Functioning/ retained*[7]	Functioning/r etained*[7]	Functioning/ retained*[7]
	TPU					Retained	Retained	Retained
	WDT					Functioning*[8]/ retained	Functioning*[8]/ retained	Functioning*[8]/ retained
	SCI3/IrDA					Reset	Functioning/ retained*[2]	Functioning/ retained*[2]
	IIC2					Retained	Retained	Retained
	PWM					Retained	Retained	Retained
	A/D converter					Retained	Retained	Retained
	LCD					Functioning/ retained*[3]	Functioning/ retained*[3]	Functioning/ retained*[3]

Notes: 1. Register contents are retained. Output is the high-impedance state.
2. Functioning if $\phi_w/2$ is selected as an internal clock, or halted and retained othe
3. Functioning if ϕw, $\phi w/2$, or $\phi w/4$ is selected as a clock to be used. Halted and r otherwise.
4. Functioning if the timekeeping time-base function is selected.
5. An external interrupt request is ignored. Contents of the interrupt request regis not affected.
6. Only incrementing of the external event timer by ECL/ECH and overflow interru operate.
7. Functioning if $\phi w/4$ is selected as an internal clock. Halted and retained otherw
8. Functioning if the on-chip oscillator is selected.
9. Functioning if the internal time keeping time-base function is selected and reta interval timer is selected.

mode to active (medium-speed) mode.

When the $\overline{\text{RES}}$ pin goes low, the CPU goes into the reset state and sleep mode is cleared interrupt request signal is synchronous with the system clock, the maximum time of 2/ϕ delayed from the point at which an interrupt request signal occurs until the interrupt exc handling is started.

Furthermore, it sometimes operates with half state early timing at the time of transition t (medium-speed) mode.

6.2.2 Standby Mode

In standby mode, the system clock oscillator stops, so the CPU and on-chip peripheral m stop functioning when the WDT disables the on-chip oscillator operation. However, as l rated voltage is supplied, the contents of CPU registers, on-chip RAM, and some on-chi peripheral module registers are retained. On-chip RAM contents will be retained as long voltage set by the RAM data retention voltage is provided. The I/O ports go to the high- state.

Standby mode is cleared by an interrupt. When an interrupt is requested, the system cloc generator starts. After the time set in bits STS2 to STS0 in SYSCR1 has elapsed, standb cleared and interrupt exception handling starts. After standby mode is cleared, a transitio to active (high-speed) or active (medium-speed) mode according to the MSON bit in SY Standby mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is di the interrupt enable bit.

When the $\overline{\text{RES}}$ pin goes low, the system clock oscillator starts. Since system clock signa supplied to the entire chip as soon as the system clock oscillator starts functioning, the $\overline{\text{R}}$ must be kept low until the system clock oscillator output stabilizes (except when the pow

Watch mode is cleared by an interrupt. When an interrupt is requested, watch mode is cle
interrupt exception handling starts. When watch mode is cleared by an interrupt, a transiti
made to active (high-speed) mode, active (medium-speed) mode, or subactive mode depe
the settings of the LSON bit in SYSCR1 and the MSON bit in SYSCR2. When the transit
made to active mode, after the time set in bits STS2 to STS0 in SYSCR1 has elapsed, int
exception handling starts. Watch mode is not cleared if the I bit in CCR is set to 1 or the r
interrupt is disabled by the interrupt enable register.

When the $\overline{\text{RES}}$ pin goes low, the system clock pulse generator starts. Since system clock
are supplied to the entire chip as soon as the system clock pulse generator starts functioni
$\overline{\text{RES}}$ pin must be kept low until the pulse generator output stabilizes. After the pulse gene
output has stabilized, the CPU starts reset exception handling if the $\overline{\text{RES}}$ pin is driven hig

6.2.4 Subsleep Mode

In subsleep mode, the CPU operation stops but on-chip peripheral modules other than the
converter and PWM function. As long as a required voltage is applied, the contents of CP
registers, the on-chip RAM, and some registers of the on-chip peripheral modules are reta
ports keep the same states as before the transition.

Subsleep mode is cleared by an interrupt. When an interrupt is requested, subsleep mode
and interrupt exception handling starts. After subsleep mode is cleared, a transition is ma
subactive mode. Subsleep mode is not cleared if the I bit in CCR is set to 1 or the request
interrupt is disabled by the interrupt enable register.

When the $\overline{\text{RES}}$ pin goes low, the system clock pulse generator starts. Since system clock
are supplied to the entire chip as soon as the system clock pulse generator starts functioni
$\overline{\text{RES}}$ pin must be kept low until the pulse generator output stabilizes. After the pulse gene
output has stabilized, the CPU starts reset exception handling if the $\overline{\text{RES}}$ pin is driven hig

When the $\overline{\text{RES}}$ pin goes low, the system clock pulse generator starts. Since system clock
are supplied to the entire chip as soon as the system clock pulse generator starts function
$\overline{\text{RES}}$ pin must be kept low until the pulse generator output stabilizes. After the pulse gen
output has stabilized, the CPU starts reset exception handling if the $\overline{\text{RES}}$ pin is driven hi

The operating frequency of subactive mode is selected from $\phi_w/2$, $\phi_w/4$, and $\phi_w/8$ by the
SA0 bits in SYSCR2.

6.2.6 Active (Medium-Speed) Mode

In active (medium-speed) mode, the system clock oscillator, subclock oscillator, CPU, a
chip peripheral module function.

Active (medium-speed) mode is cleared by the SLEEP instruction. When active (mediu
mode is cleared, a transition to standby mode is made depending on the combination of
SSBY, LSON, and TMA3 in SYSCR1, a transition to watch mode is made depending o
combination of bits SSBY and TMA3 in SYSCR1, or a transition to sleep mode is made
depending on the combination of bits SSBY and LSON in SYSCR1. Moreover, a transit
active (high-speed) mode or subactive mode is made by a direct transition. Active (medi
mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled in
interrupt enable register. When the $\overline{\text{RES}}$ pin goes low, the CPU goes into the reset state
(medium-sleep) mode is cleared.

Furthermore, it sometimes operates with half state early timing at the time of transition t
(medium-speed) mode.

In active (medium-speed) mode, the on-chip peripheral modules function at the clock fr
set by the MA1 and MA0 bits in SYSCR1.

Note: If a direct transition is attempted while the I bit in CCR is set to 1, the device ent
sleep or watch mode, and recovery is not possible.

(1) Direct transfer from active (high-speed) mode to active (medium-speed) mode

When a SLEEP instruction is executed in active (high-speed) mode while the SSBY and
bits in SYSCR1 are cleared to 0 and the MSON and DTON bits in SYSCR2 are set to 1,
transition is made to active (medium-speed) mode via sleep mode.

(2) Direct transfer from active (medium-speed) mode to active (high-speed) mode

When a SLEEP instruction is executed in active (medium-speed) mode while the SSBY
LSON bits in SYSCR1 are cleared to 0, the MSON bit in SYSCR2 is cleared to 0, and the
bit in SYSCR2 is set to 1, a transition is made to active (high-speed) mode via sleep mod

(3) Direct transfer from active (high-speed) mode to subactive mode

When a SLEEP instruction is executed in active (high-speed) mode while the SSBY, TM
LSON bits in SYSCR1 are set to 1 and the DTON bit in SYSCR2 is set to 1, a transition
to subactive mode via watch mode.

(4) Direct transfer from subactive mode to active (high-speed) mode

When a SLEEP instruction is executed in subactive mode while the SSBY and TMA3 bit
SYSCR1 are set to 1, the LSON bit in SYSCR1 is cleared to 0, the MSON bit in SYSCR
cleared to 0, and the DTON bit in SYSCR2 is set to 1, a transition is made directly to acti
speed) mode via watch mode after the waiting time set in bits STS2 to STS0 in SYSCR1
elapsed.

after the waiting time set in bits STS2 to STS0 in STCR1 has elapsed.

6.3.1 Direct Transition from Active (High-Speed) Mode to Active (Medium-Spe

The time from the start of SLEEP instruction execution to the end of interrupt exception (the direct transition time) is calculated by equation (1).

Direct transition time = {(Number of SLEEP instruction execution states) + (Number of processing states)} × (tcyc before transition) + (Number of inte exception handling execution states) × (tcyc after transition)

……

Example: When $\phi_{OSC}/8$ is selected as the CPU operating clock following transitio

Direct transition time = (2 + 1) × tosc + 14 × 8tosc = 115tosc

[Legend]
tosc: OSC clock cycle time
tcyc: System clock (ϕ) cycle time

Direct transition time = (2 + 1) × 1tosc + 14 × 1tsubcyc = 3tosc + 14tsu

[Legend]
tosc: OSC clock cycle time
tsubcyc: Subclock (ϕ_{SUB}) cycle time

6.3.3 Direct Transition from Active (Medium-Speed) Mode to Active (High-Spee

The time from the start of SLEEP instruction execution to the end of interrupt exception h
(the direct transition time) is calculated by equation (3).

Direct transition time = {(Number of SLEEP instruction execution states) + (Number of i
processing states)} × (tcyc before transition) + (Number of interr
exception handling execution states) × (tcyc after transition)
……

Example: When ϕ_{OSC}/8 is selected as the CPU operating clock before transition

Direct transition time = (2 + 1) × 8tosc + 14 × tosc = 38tosc

[Legend]
tosc: OSC clock cycle time
tcyc: System clock (ϕ) cycle time

Direct transition time = (2 + 1) × 8tosc + 14 × 1tsubcyc = 24tosc + 14

[Legend]
tosc: OSC clock cycle time
tsubcyc: Subclock (ϕ_{SUB}) cycle time

6.3.5 Direct Transition from Subactive Mode to Active (High-Speed) Mode

The time from the start of SLEEP instruction execution to the end of interrupt exception (the direct transition time) is calculated by equation (5).

Direct transition time = {(Number of SLEEP instruction execution states) + (Number of processing states)} × (tsubcyc before transition) + {(Wait time STS2 to STS0) + (Number of interrupt exception handling exec states)} × (tcyc after transition)

.....

Example: When ϕw/8 is selected as the CPU operating clock before transition ar time = 8192 states

Direct transition time = (2 + 1) × 8tw + (8192 + 14) × tosc = 24tw + 8

[Legend]
tosc: OSC clock cycle time
tw: Watch clock cycle time
tcyc: System clock (ϕ) cycle time
tsubcyc: Subclock (ϕ_{SUB}) cycle time

Example: When ϕw/8 is selected as the CPU operating clock before transition, ϕ_O
selected as the CPU operating clock following transition, and the wait t
8,192 states

Direct transition time = (2 + 1) × 8tw + (8192 + 14) × 8tosc
= 24tw + 65648tosc

[Legend]
tosc: OSC clock cycle time
tw: Watch clock cycle time
tcyc: System clock (ϕ) cycle time
tsubcyc: Subclock (ϕ_{SUB}) cycle time

6.3.7 Notes on External Input Signal Changes before/after Direct Transition

(1) Direct transition from active (high-speed) mode to subactive mode

Since the mode transition is performed via watch mode, see section 6.5.2, Notes on Exter
Signal Changes before/after Standby Mode.

(2) Direct transition from active (medium-speed) mode to subactive mode

Since the mode transition is performed via watch mode, see section 6.5.2, Notes on Exter
Signal Changes before/after Standby Mode.

(3) Direct transition from subactive mode to active (high-speed) mode

Since the mode transition is performed via watch mode, see section 6.5.2, Notes on Exter
Signal Changes before/after Standby Mode.

6.1.3, Clock Halt Registers 1 and 2 (CKSTPR1 and CKSTPR2).)

6.5 Usage Notes

6.5.1 Standby Mode Transition and Pin States

When a SLEEP instruction is executed in active (high-speed) mode or active (medium-s
mode while the SSBY and TMA3 bits in SYSCR1 are set to 1 and the LSON bit in SYS
cleared to 0, a transition is made to standby mode. At the same time, pins go to the high-
impedance state (except pins for which the pull-up MOS is designated as on). Figure 6.2
the timing in this case.

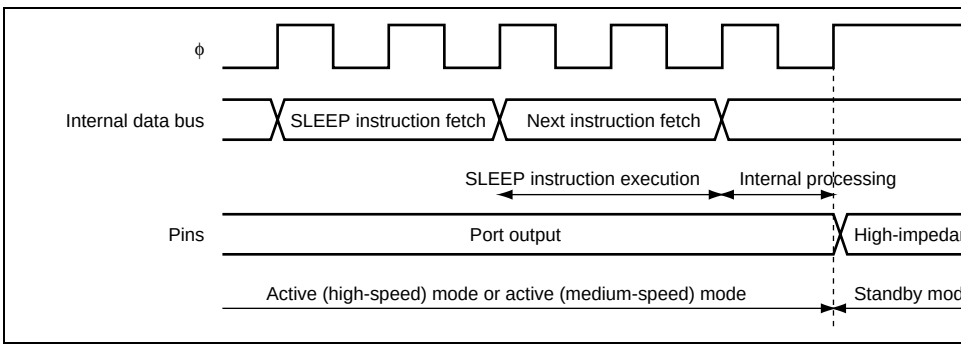


Figure 6.2 Standby Mode Transition and Pin States

(2) When External Input Signals cannot be Captured because Internal Clock Stop

The case of falling edge capture is shown in figure 6.3.

As shown in the case marked "Capture not possible," when an external input signal falls immediately after a transition to active mode or subactive mode, after oscillation is starte interrupt via a different signal, the external input signal cannot be captured if the high-lev at that point is less than 2 t_{cyc} or 2 t_{subcyc}.

(3) Recommended Timing of External Input Signals

To ensure dependable capture of an external input signal, high- and low-level signal widt least 2 t_{cyc} or 2 t_{subcyc} are necessary before a transition is made to standby mode or watch m shown in "Capture possible: case 1."

External input signal capture is also possible with the timing shown in "Capture possible: and "Capture possible: case 3," in which a 2 t_{cyc} or 2 t_{subcyc} level width is secured.

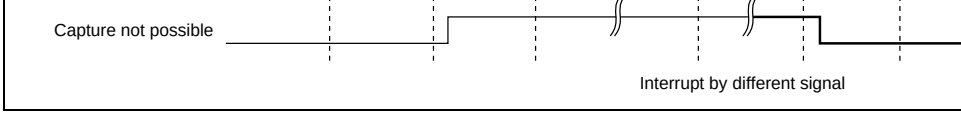


Figure 6.3 External Input Signal Capture when Signal Changes before/after Stan or Watch Mode

(4) Input Pins to which these Notes Apply

$\overline{\text{IRQ4}}$, $\overline{\text{IRQ3}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$, $\overline{\text{WKP7}}$ to $\overline{\text{WKP0}}$, IRQAEC, TMIF, $\overline{\text{ADTRG}}$, TIOCA1, TIOC TIOCA2 and TIOCB2.

- On-board programming

  On-board programming/erasing can be done in boot mode, in which the boot progra into the chip is started to erase or program of the entire flash memory. In normal us mode, individual blocks can be erased or programmed.

- Programmer mode

  Flash memory can be programmed/erased in programmer mode using a PROM prog as well as in on-board programming mode.

- Automatic bit rate adjustment

  For data transfer in boot mode, this LSI's bit rate can be automatically adjusted to m transfer bit rate of the host.

- Programming/erasing protection

  Sets software protection against flash memory programming/erasing.

- Power-down mode

  Operation of the power supply circuit can be partly halted in subactive mode. As a r memory can be read with low power consumption.

- Module standby mode

  Use of module standby mode enables this module to be placed in standby mode inde when not used. (For details, refer to section 6.4, Module Standby Function.) When t debugging emulator is used, the bit 1 (FROMCKSTP) in clock stop register 1 (CKS should be set to 1.

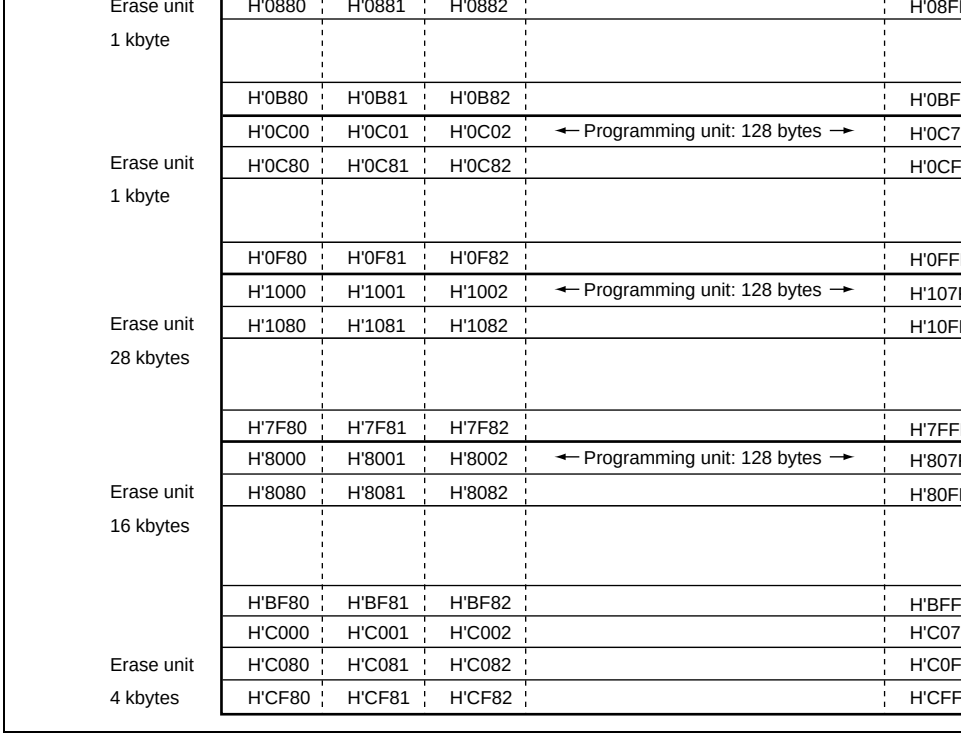


Figure 7.1 Flash Memory Block Configuration

7.2.1 Flash Memory Control Register 1 (FLMCR1)

FLMCR1 is a register that makes the flash memory change to program mode, program-ve mode, erase mode, or erase-verify mode. For details on register setting, refer to section 7. Memory Programming/Erasing.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0.
6	SWE	0	R/W	Software Write Enable When this bit is set to 1, flash memory programming/erasing is enabled. When this bi cleared to 0, other FLMCR1 register bits and a bits cannot be set.
5	ESU	0	R/W	Erase Setup When this bit is set to 1, the flash memory cha the erase setup state. When it is cleared to 0, setup state is cancelled. Set this bit to 1 before the E bit to 1 in FLMCR1.
4	PSU	0	R/W	Program Setup When this bit is set to 1, the flash memory cha the program setup state. When it is cleared to program setup state is cancelled. Set this bit t before setting the P bit in FLMCR1.
3	EV	0	R/W	Erase-Verify When this bit is set to 1, the flash memory cha erase-verify mode. When it is cleared to 0, era mode is cancelled.

				When this bit is set to 1 while SWE=1 and PS flash memory changes to program mode. Wh cleared to 0, program mode is cancelled.

7.2.2 Flash Memory Control Register 2 (FLMCR2)

FLMCR2 is a register that displays the state of flash memory programming/erasing. FL read-only register, and should not be written to.

Bit	Bit Name	Initial Value	R/W	Description
7	FLER	0	R	Flash Memory Error Indicates that an error has occurred during ar on flash memory (programming or erasing). V FLER is set to 1, flash memory goes to the er protection state. See section 7.5.3, Error Protection, for details
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

6	EB6	0	R/W	When this bit is set to 1, 4 kbytes of H'C000 to will be erased.
5	EB5	0	R/W	When this bit is set to 1, 16 kbytes of H'8000 to will be erased.
4	EB4	0	R/W	When this bit is set to 1, 28 kbytes of H'1000 to will be erased.
3	EB3	0	R/W	When this bit is set to 1, 1 kbyte of H'0C00 to H will be erased.
2	EB2	0	R/W	When this bit is set to 1, 1 kbyte of H'0800 to H will be erased.
1	EB1	0	R/W	When this bit is set to 1, 1 kbyte of H'0400 to H will be erased.
0	EB0	0	R/W	When this bit is set to 1, 1 kbyte of H'0000 to H will be erased.

				When this bit is 0 and a transition is made to s mode, the flash memory enters the power-do When this bit is 1, the flash memory remains i normal mode even after a transition is made t subactive mode.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

7.2.5 Flash Memory Enable Register (FENR)

Bit 7 (FLSHE) in FENR enables or disables the CPU access to the flash memory contro FLMCR1, FLMCR2, EBR1, and FLPWCR.

Bit	Bit Name	Initial Value	R/W	Description
7	FLSHE	0	R/W	Flash Memory Control Register Enable Flash memory control registers can be acces this bit is set to 1. Flash memory control regis cannot be accessed when this bit is set to 0.
6 to 0	—	All 0	—	Reserved These bits are always read as 0.

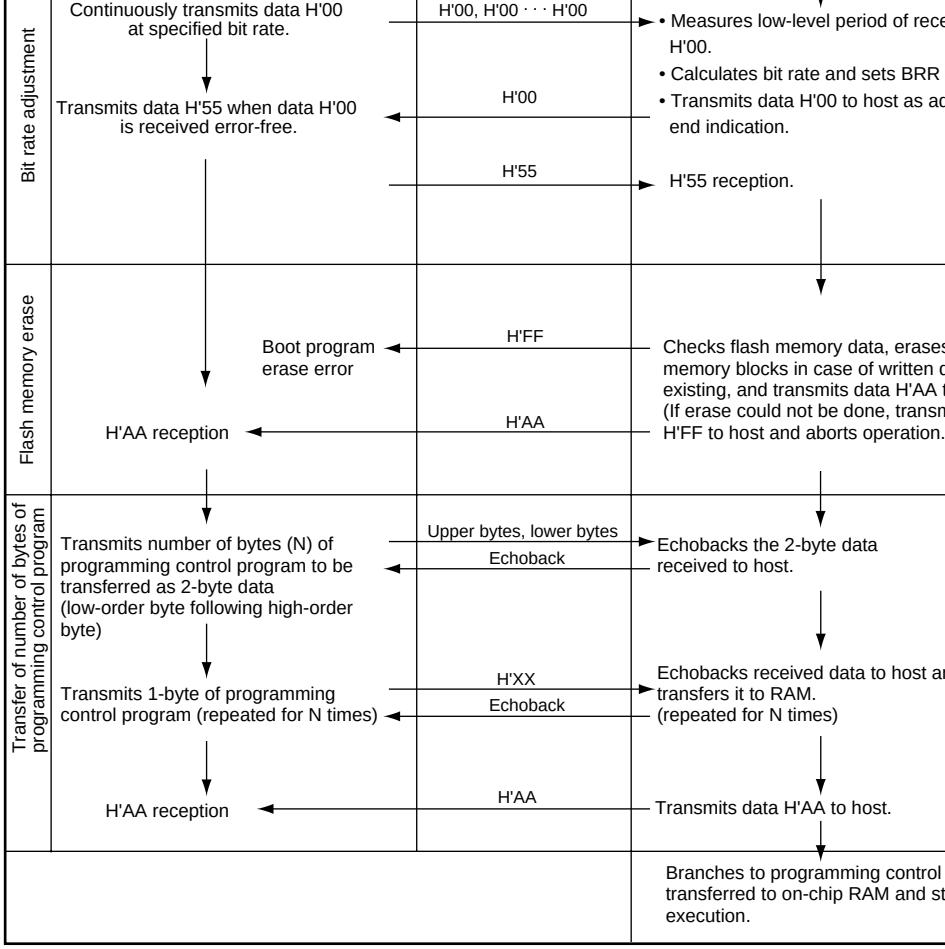
via SCI3 (channel 2). After erasing the entire flash memory, the programming control pr
executed. This can be used for programming initial values in the on-board state or for a f
return when programming/erasing can no longer be done in user program mode. In user p
mode, individual blocks can be erased and programmed by branching to the user program
control program prepared by the user.

Table 7.1 Setting Programming Modes

TEST	$\overline{\text{NMI}}$	P36	PB0	PB1	PB2	LSI State after Reset End
0	1	X	X	X	X	User Mode
0	0	1	X	X	X	Boot Mode
1	X	X	0	0	0	Programmer Mode

[Legend] X: Don't care.

3. When the boot program is initiated, the chip measures the low-level period of asynch SCI communication data (H'00) transmitted continuously from the host. The chip the calculates the bit rate of transmission from the host, and adjusts the SCI3 bit rate to m of the host. The reset should end with the RXD pin high. The RXD and TXD pins sh pulled up on the board if necessary. After the reset is complete, it takes approximatel states before the chip is ready to measure the low-level period.
4. After matching the bit rates, the chip transmits one H'00 byte to the host to indicate t completion of bit rate adjustment. The host should confirm that this adjustment end i (H'00) has been received normally, and transmit one H'55 byte to the chip. If recepti not be performed normally, initiate boot mode again by a reset. Depending on the ho transfer bit rate and system clock frequency of this LSI, there will be a discrepancy b the bit rates of the host and the chip. To operate the SCI properly, set the host's trans and system clock frequency of this LSI within the ranges listed in table 7.3.
5. In boot mode, a part of the on-chip RAM area is used by the boot program. The area H'FEEF is the area to which the programming control program is transferred from th The boot program area cannot be used until the execution state in boot mode switche programming control program.
6. Before branching to the programming control program, the chip terminates transfer o by SCI3 (by clearing the RE and TE bits in SCR to 0), however the adjusted bit rate remains set in BRR. Therefore, the programming control program can still use it for program data or verify data with the host. The TXD pin is high (PCR42 = 1, P42 = 1 contents of the CPU general registers are undefined immediately after branching to t programming control program. These registers must be initialized at the beginning o programming control program, as the stack pointer (SP), in particular, is used implic subroutine calls, etc.
7. Boot mode can be cleared by a reset. End the reset after driving the reset pin low, wa least 20 states, and then setting the $\overline{\text{NMI}}$ pin. Boot mode is also cleared when a WDT occurs.


Bit rate adjustment
Continuously transmits data H'00 at specified bit rate.
H'00, H'00 · · · H'00
• Measures low-level period of rece
H'00.
• Calculates bit rate and sets BRR
H'00
• Transmits data H'00 to host as ac
end indication.
Transmits data H'55 when data H'00 is received error-free.
H'55
H'55 reception.
Flash memory erase
H'FF
Boot program erase error
Checks flash memory data, erases
memory blocks in case of written d
existing, and transmits data H'AA t
(If erase could not be done, transm
H'FF to host and aborts operation.
H'AA
H'AA reception
Transfer of number of bytes of programming control program
Upper bytes, lower bytes
Transmits number of bytes (N) of programming control program to be transferred as 2-byte data (low-order byte following high-order byte)
Echoback
Echobacks the 2-byte data received to host.
H'XX
Echobacks received data to host an
transfers it to RAM.
Transmits 1-byte of programming control program (repeated for N times)
Echoback
(repeated for N times)
H'AA
H'AA reception
Transmits data H'AA to host.
Branches to programming control
transferred to on-chip RAM and st
execution.

On-board programming/erasing of an individual flash memory block can also be perform
program mode by branching to a user program/erase control program. The user must set
conditions and provide on-board means of supplying programming data. The flash mem
contain the user program/erase control program or a program that provides the user prog
control program from external memory. As the flash memory itself cannot be read durin
programming/erasing, transfer the user program/erase control program to on-chip RAM,
mode. Figure 7.2 shows a sample procedure for programming/erasing in user program m
Prepare a user program/erase control program in accordance with the description in sect
Flash Memory Programming/Erasing.

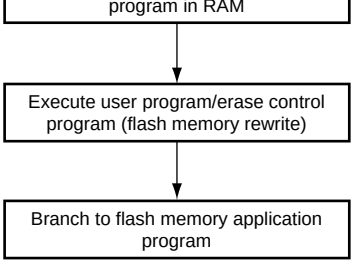
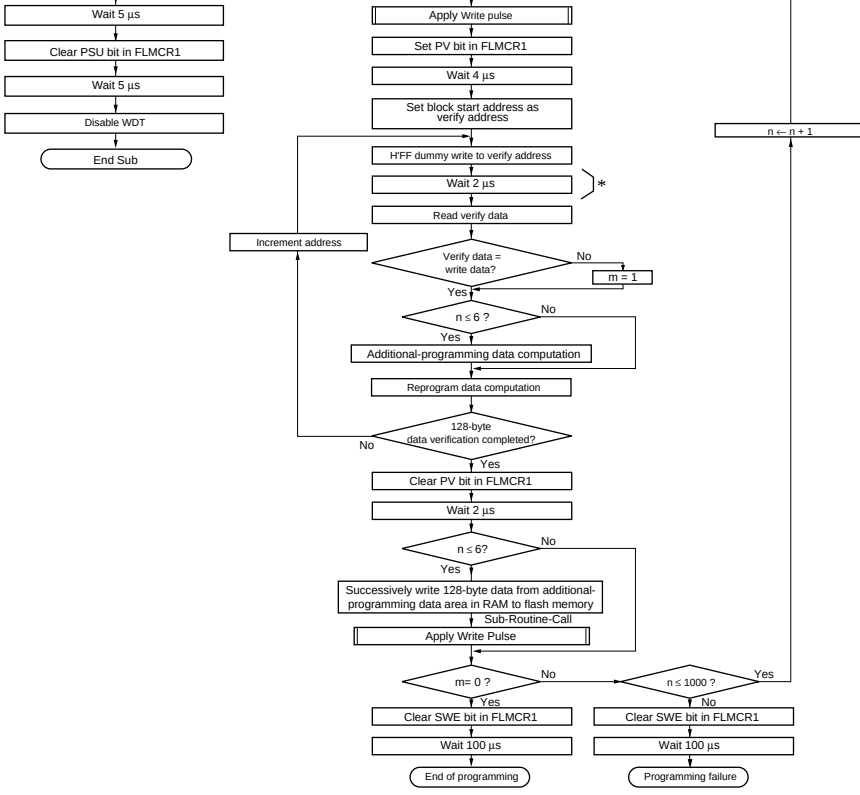


Figure 7.2 Programming/Erasing Flowchart Example in User Program Mo

7.4.1 Program/Program-Verify

When writing data or programs to the flash memory, the program/program-verify flowch in figure 7.3 should be followed. Performing programming operations according to this will enable data or programs to be written to the flash memory without subjecting the ch voltage stress or sacrificing program data reliability.

1. Programming must be done to an empty address. Do not reprogram an address to wh programming has already been performed.
2. Programming should be carried out 128 bytes at a time. A 128-byte data transfer mu performed even if writing fewer than 128 bytes. In this case, H'FF data must be writ extra addresses.
3. Prepare the following data storage areas in RAM: A 128-byte programming data are byte reprogramming data area, and a 128-byte additional-programming data area. Pe reprogramming data computation according to table 7.4, and additional programmin computation according to table 7.5.
4. Consecutively transfer 128 bytes of data in byte units from the reprogramming data a additional-programming data area to the flash memory. The program address and 12 data are latched in the flash memory. The lower 8 bits of the start address in the flas destination area must be H'00 or H'80.
5. The time during which the P bit is set to 1 is the programming time. Table 7.6 show allowable programming times.
6. The watchdog timer (WDT) is set to prevent overprogramming due to program runa An overflow cycle of approximately 6.6 ms is allowed.
7. For a dummy write to a verify address, write 1-byte data H'FF to an address whose bits are B'00. Verify data can be read in words or in longwords from the address to dummy write was performed.



Note: *The RTS instruction must not be used during the following 1. and 2. periods.
1. A period between 128-byte data programming to flash memory and the P bit clearing
2. A period between dummy writing of H'FF to a verify address and verify data reading

Figure 7.3 Program/Program-Verify Flowchart

Reprogram Data	Verify Data	Additional-Program Data	Comments
0	0	0	Additional-program
0	1	1	No additional progr
1	0	1	No additional progr
1	1	1	No additional progr

Table 7.6 Programming Time

n (Number of Writes)	Programming Time	In Additional Programming	Comments
1 to 6	30	10	
7 to 1,000	200	—	

Note: Time shown in µs.

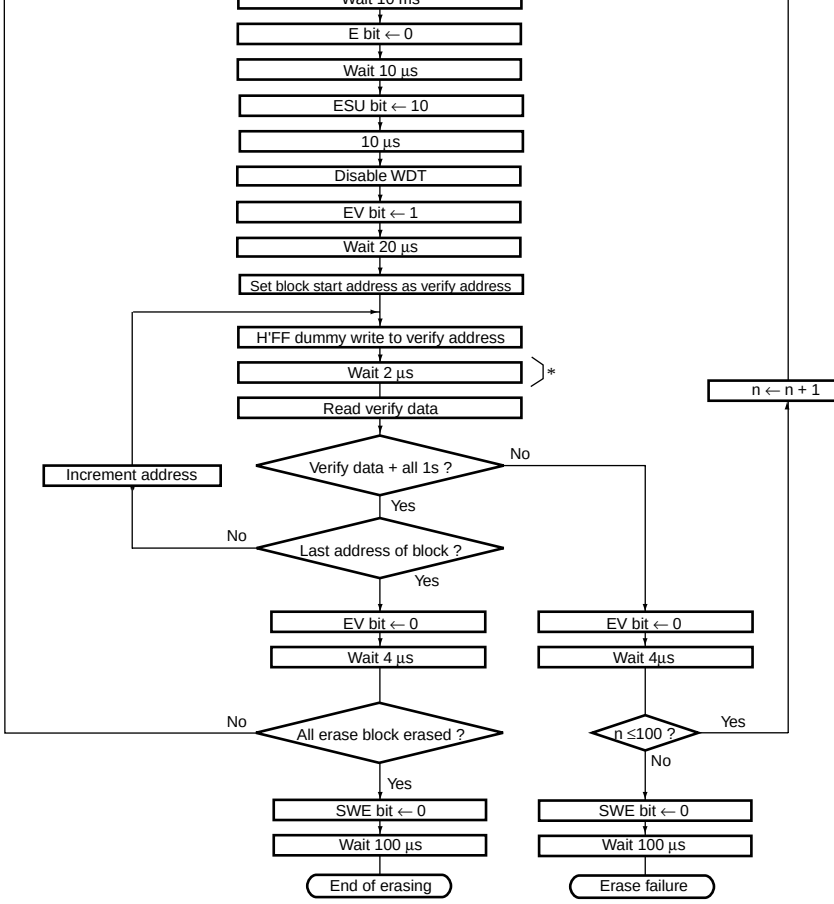
overflow cycle of approximately 19.8 ms is allowed.

5. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lo bits are B'00. Verify data can be read in longwords from the address to which a dumm was performed.
6. If the read data is not erased successfully, set erase mode again, and repeat the erase/e verify sequence as before. The maximum number of repetitions of the erase/erase-ver sequence is 100.

7.4.3 Interrupt Handling when Programming/Erasing Flash Memory

All interrupts, including the NMI interrupt, are disabled while flash memory is being prog or erased, or while the boot program is executing, for the following three reasons:

1. Interrupt during programming/erasing may cause a violation of the programming or e algorithm, with the result that normal operation cannot be assured.
2. If interrupt exception handling starts before the vector address is written or during programming/erasing, a correct vector cannot be fetched and the CPU malfunctions.
3. If an interrupt occurs during boot program execution, normal boot mode sequence can carried out.



Note: * The RTS instruction must not be used during a period between dummy writing of H'FF to a verify address and verify dat

Figure 7.4 Erase/Erase-Verify Flowchart

and erase block register 1 (EBR1) are initialized. In a reset via the RES pin, the reset stat
entered unless the $\overline{\text{RES}}$ pin is held low until oscillation stabilizes after powering on. In th
a reset during operation, hold the $\overline{\text{RES}}$ pin low for the $\overline{\text{RES}}$ pulse width specified in the A
Characteristics section.

7.5.2 Software Protection

Software protection can be implemented against programming/erasing of all flash memor
by clearing the SWE bit in FLMCR1. When software protection is in effect, setting the P
in FLMCR1 does not cause a transition to program mode or erase mode. By setting the e
block register 1 (EBR1), erase protection can be set for individual blocks. When EBR1 is
H'00, erase protection is set for all blocks.

7.5.3 Error Protection

In error protection, an error is detected when CPU runaway occurs during flash memory
programming/erasing, or operation is not performed in accordance with the program/eras
algorithm, and the program/erase operation is forcibly aborted. Aborting the program/era
operation prevents damage to the flash memory due to overprogramming or overerasing.

When the following errors are detected during programming/erasing of flash memory, the
bit in FLMCR2 is set to 1, and the error protection state is entered.

- When the flash memory of the relevant address area is read during programming/eras
  (including vector read and instruction fetch)
- Immediately after exception handling excluding a reset during programming/erasing
- When a SLEEP instruction is executed during programming/erasing

7.7 Power-Down States for Flash Memory

In user mode, the flash memory will operate in either of the following states:

- Normal operating mode
  The flash memory can be read and written to at high speed.
- Power-down operating mode
  The power supply circuit of flash memory can be partly halted. As a result, flash me
  be read with low power consumption.
- Standby mode
  All flash memory circuits are halted.

Table 7.7 shows the correspondence between the operating modes of this LSI and the fl
memory. In subactive mode, the flash memory can be set to operate in power-down mo
PDWND bit in FLPWCR. When the flash memory returns to its normal operating state
power-down mode or standby mode, a period to stabilize operation of the power supply
that were stopped is needed. When the flash memory returns to its normal operating stat
STS2 to STS0 in SYSCR1 must be set to provide a wait time of at least 20 µs, even whe
external clock is being used.

7.8 Notes on Setting Module Standby Mode

When the flash memory is set to enter module standby mode, the system clock supply is s to the module, the function is stopped, and the state is the same as that in standby mode. A program operation is stopped in the flash memory. Therefore operation program should b transferred to the RAM and the program should run in the RAM. Then the flash memory be set to enter module standby mode.

Even if an interrupt source occurs while the interrupt is enabled in module standby mode, runaway may occur because the vector cannot be fetched.

Before the flash memory is set to enter module standby mode, the corresponding bit in th interrupt enable register should be cleared to 0 and the I bit in CCR should be set to 1. Th the flash memory enters module standby mode, NMI and address break interrupt requests not be generated. Figure 7.5 shows a module standby mode setting.

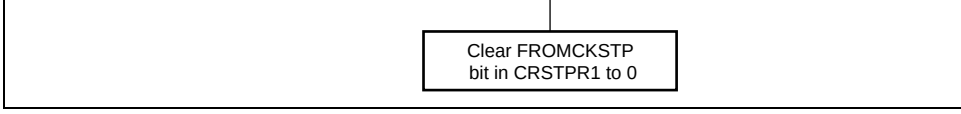


Figure 7.5 Module Standby Mode Setting

H8/38073R	1 kbyte	H'FB80 to H'FF7F

For details on the execution of bit manipulation instructions to the port data register (PD
section 2.8.3, Bit-Manipulation Instruction.

For details on block diagrams for each port, see Appendix B.1, I/O Port Block Diagrams

9.1 Port 1

Port 1 is an I/O port also functioning as an SCI4 I/O pin, TPU I/O pin, and asynchronou
counter input pin. Figure 9.1 shows its pin configuration.

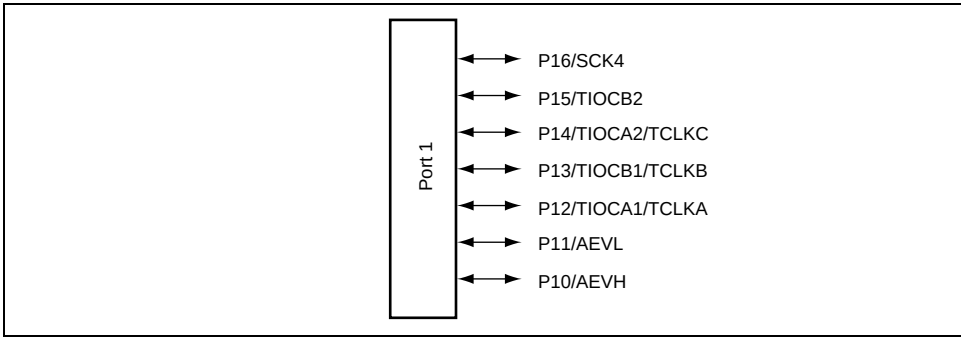


Figure 9.1 Port 1 Pin Configuration

Port 1 has the following registers.

- Port data register 1 (PDR1)
- Port control register 1 (PCR1)
- Port pull-up control register 1 (PUCR1)
- Port mode register 1 (PMR1)

3	P13	0	R/W	be modified.
2	P12	0	R/W	
1	P11	0	R/W	
0	P10	0	R/W	

9.1.2 Port Control Register 1 (PCR1)

PCR1 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 1.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Setting a PCR1 bit to 1 makes the correspondi
6	PCR16	0	W	(P16 to P10) an output pin, while clearing the b
5	PCR15	0	W	makes the pin an input pin. The settings in PCR
4	PCR14	0	W	PDR1 are valid when the corresponding pin is designated as a general I/O pin.
3	PCR13	0	W	PCR1 is a write-only register. These bits are al
2	PCR12	0	W	read as 1.
1	PCR11	0	W	Bit 7 is reserved. This bit cannot be modified.
0	PCR10	0	W	

3	PUCR13	0	R/W	be modified.
2	PUCR12	0	R/W	
1	PUCR11	0	R/W	
0	PUCR10	0	R/W	

9.1.4 Port Mode Register 1 (PMR1)

PMR1 controls the selection of functions for port 1 pins.

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 1	—	Reserved These bits are always read as 1 and cannot b
1	AEVL	0	R/W	P11/AEVL Pin Function Switch Selects whether pin P11/AEVL is used as P11 AEVL. 0: P11 I/O pin 1: AEVL input pin
0	AEVH	0	R/W	P10/AEVH Pin Function Switch Selects whether pin P10/AEVH is used as P1 AEVH. 0: P10 I/O pin 1: AEVH input pin

PCR16	0	1	x	x
Pin Function	P16 input pin	P16 output pin	SCK4 input pin*[2]	SCK4 out

[Legend] x: Don't care.

Notes: 1. Supported only by the F-ZTAT™ version.

2. Only port function is available for the masked ROM version.

Note: * When the MD1 and MD0 bits are set to B'00 and the IOB3 bit to 1, the pin fun becomes the TIOCB2 input pin.
Clear PCR15 to 0 when using TIOCB2 as an input pin.

TPU Channel 2 Setting	(2)	(3)	(1)	
MD1, MD0	B'00			B'10, B'01, B'1
IOB3 to IOB0	B'0000	B'1xxx	B'0001 to B'0111	B'xxxx
CCLR1, CCLR0	B'xx			
Output Function	—		Setting prohibited	

[Legend] x: Don't care.

	TCLKC input pin*

Notes: 1. When the MD1 and MD0 bits are set to B'00 and the IOA3 bit to 1, the pin func
becomes the TIOCA2 input pin.
Clear PCR14 to 0 when using TIOCA2 as an input pin.

2. When the TPSC2 to TPSC0 bits in TCR_2 are set to B'110, the pin function be
the TCLKC input pin.
Clear PCR14 to 0 when using TCLKC as an input pin.

TPU Channel 2 Setting	(2)	(1)	(2)	(1)	(1)
MD1, MD0	B'00		B'1x	B'10	B'11
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than
CCLR1, CCLR0	—	—	—	—	Other than B'01
Output Function	—	Output compare output	—	PWM mode 1* output	PWM mode 2 output

[Legend] x: Don't care.

Note: * The output of the TIOCB2 pin is disabled.

				TIOCB1 input
		TCLKB input pin*		

Note: * When the TPSC2 to TPSC0 bits in TCR_1 or TCR_2 are set to B'101, the pin becomes the TCLKB input pin.
Clear PCR13 to 0 when using TCLKB as an input pin.

TPU Channel 1 Setting	(2)	(3)	(1)	
MD1, MD0	B'00			B'10, B'01, B'1
IOB3 to IOB0	B'0000	B'1xxx	B'0001 to B'0111	B'xxxx
CCLR1, CCLR0	B'xx			
Output Function	—	Setting prohibited		

[Legend] x: Don't care.

	TIOCA1 input pin	
	TCLKA input pin*[2]	

Notes: 1. When the MD1 and MD0 bits are set to B'00 and the IOA3 bit to 1, the pin func
becomes the TIOCA1 input pin.
Clear PCR12 to 0 when using TIOCA1 as an input pin.

2. When the TPSC2 to TPSC0 bits in TCR_1 or TCR_2 are set to B'100, the pin
becomes the TCLKA input pin.
Clear PCR12 to 0 when using TCLKA as an input pin.

TPU Channel 1 Setting	(2)	(1)	(2)	(1)	(1)	
MD1, MD0	B'00		B'1x	B'10	B'11	
IOA3 to IOA0	B'0000 B'0100 B'1xxx	B'0001 to B'0011 B'0101 to B'0111	B'xx00	Other than B'xx00	Other than B	
CCLR1, CCLR0	—	—	—	—	Other than B'10	
Output Function	—	Output compare output	—	PWM mode 1* output	PWM mode 2 output	

[Legend] x: Don't care.

Note: * The output of the TIOCB1 pin is disabled.

The pin function is switched as shown below according to the combination of the AE
PMR1 and PCR10 bit in PCR.

AEVH	0		1
PCR10	0	1	x
Pin Function	P10 input pin	P10 output pin	AEVH input pin

[Legend] x: Don't care.

9.1.6 Input Pull-Up MOS

Port 1 has an on-chip input pull-up MOS function that can be controlled by software. W
PCR1 bit is cleared to 0, setting the corresponding PUCR1 bit to 1 turns on the input pul
for that pin. The input pull-up MOS function is in the off state after a reset.

(n = 6 t

PCR1n	0		1
PUCR1n	0	1	x
Input Pull-Up MOS	Off	On	Off

[Legend] x: Don't care.

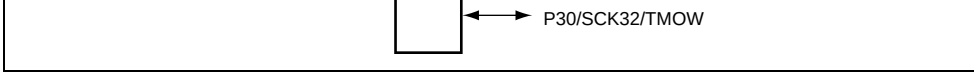


Figure 9.2 Port 3 Pin Configuration

Port 3 has the following registers.

- Port data register 3 (PDR3)
- Port control register 3 (PCR3)
- Port pull-up control register 3 (PUCR3)
- Port mode register 3 (PMR3)

9.2.1 Port Data Register 3 (PDR3)

PDR3 is a register that stores data of port 3.

Bit	Bit Name	Initial Value	R/W	Description
7	P37	0	R/W	If port 3 is read while PCR3 bits are set to 1, th
6	P36	0	R/W	stored in PDR3 are read, regardless of the actu
5	—	1	—	states. If port 3 is read while PCR3 bits are clea
4	—	1	—	the pin states are read.
3	—	1	—	Bits 5 to 3 are reserved. These bits are always and cannot be modified.
2	P32	0	R/W	
1	P31	0	R/W	
0	P30	0	R/W	

3	—	1	—	PCR3 is a write-only register. These bits are a read as 1.
2	PCR32	0	W	
1	PCR31	0	W	Bits 5 to 3 are reserved. These bits cannot be
0	PCR30	0	W	

9.2.3 Port Pull-Up Control Register 3 (PUCR3)

PUCR3 controls the pull-up MOS of the port 3 pins in bit units.

Bit	Bit Name	Initial Value	R/W	Description
7	PUCR37	0	R/W	When a PCR3 bit is cleared to 0, setting the
6	PUCR36	0	R/W	corresponding PUCR3 bit to 1 turns on the pu for the corresponding pin, while clearing the b
5	—	1	—	turns off the pull-up MOS.
4	—	1	—	Bits 5 to 1 are reserved. These bits are always
3	—	1	—	and cannot be modified.
2	—	1	—	
1	—	1	—	
0	PUCR30	0	R/W	

P30/SCK32 or as TMOW.

0: P30/SCK32 I/O pin

1: TMOW output pin

9.2.5 Pin Functions

The relationship between the register settings and the port functions is shown below.

- P37/SO4 pin

  The pin function is switched as shown below according to the combination of the TE SCR4 and PCR37 bit in PCR3.

TE*[1]	0*[1]		1*[1]
PCR37	0	1	x
Pin Function	P37 input pin	P37 output pin	SO4 output pin*[2]

[Legend] x: Don't care.

Notes: 1. Supported only by the F-ZTAT™ version.

2. Only port function is available for the masked ROM version.

- P32/TXD32/SCL pin

  The pin function is switched as shown below according to the combination of the PC
  PCR3, ICE bit in ICRR1, TE bit in SCR32, and SPC32 bit in SPCR.

ICE	0			
SPC32	0		1	
TE	x		x	
PCR32	0	1	x	
Pin Function	P32 input pin	P32 output pin	TXD32 output pin*	SCL

[Legend] x: Don't care.

Note: * If SPC32 is set to 1 and TE is cleared to 0, the mark state is entered and 1 is from the TXD32 output pin.

- P31/RXD32/SDA pin

  The pin function is switched as shown below according to the combination of the PC
  PCR3, ICE bit in ICCR1, and RE bit in SCR32.

ICE	0			
RE	0		1	
PCR31	0	1	x	
Pin Function	P31 input pin	P31 output pin	RXD32 output pin	SDA

[Legend] x: Don't care.

	pin	output pin	pin	pin	p

[Legend] x: Don't care.

9.2.6 Input Pull-Up MOS

Port 3 has an on-chip input pull-up MOS function that can be controlled by software. Wh
PCR3 bit is cleared to 0, setting the corresponding PUCR3 bit to 1 turns on the input pull
for that pin. The input pull-up MOS function is in the off state after a reset.

(n = 7, 6

PCR3n	0		1
PUCR3n	0	1	x
Input Pull-Up MOS	Off	On	Off

[Legend] x: Don't care.

Figure 9.3 Port 4 Pin Configuration

Port 4 has the following registers.

- Port data register 4 (PDR4)
- Port control register 4 (PCR4)
- Port mode register 4 (PMR4)

9.3.1 Port Data Register 4 (PDR4)

PDR4 is a register that stores data of port 4.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 1	—	Reserved These bits are always read as 1 and cannot b
2	P42	0	R/W	If port 4 is read while PCR4 bits are set to 1, t
1	P41	0	R/W	stored in PDR4 are read, regardless of the ac states. If port 4 is read while PCR4 bits are cl
0	P40	0	R/W	the pin states are read.

0	PCR40	0	W	when the corresponding pin is designated as a I/O pin. PCR4 is a write-only register. These bits are al read as 1.

				as P42 or TXD31/IrTXD, or as TMOFH. 0: P42 I/O pin or TXD31/IrTXD output pin 1: TMOFH output pin
1	TMOFL	0	R/W	P41/RXD31/IrRXD/TMOFL Pin Function Switc Selects whether pin P41/RXD31/IrRXD/TMOF as P41 or RXD31/IrRXD, or as TMOFL. 0: P41 I/O pin or RXD31/IrRXD input pin 1: TMOFL output pin
0	TMIF	0	R/W	P40/SCK31/TMIF Pin Function Switch Selects whether pin P40/SCK31/TMIF is used P40/SCK31 or as TMIF. 0: P40/SCK31 I/O pin 1: TMIF output pin

TE	x		x		
IrE	x		0	1	
PCR42	0	1	x	x	
Pin Function	P42 input pin	P42 output pin	TXD31 output pin*	IrTXD output pin*	T ou

[Legend] x: Don't care.

Note: * If SPC31 is set to 1 and TE is cleared to 0, the mark state is entered, 1 is outp the TXD32 output pin, and 0 is output from the IrTXD pin.

- P41/RXD31/IrRXD/TMOFL pin

  The pin function is switched as shown below according to the combination of the TM in PMR4, PCR41 bit in PCR4, IrE bit in IrCR, and RE bit in SCR3.

TMOFL	0				
RE	0		1		
IrE	x		0	1	
PCR41	0	1	x	x	
Pin Function	P41 input pin	P41 output pin	RXD31 input pin	IrRXD input pin	TM outp

[Legend] x: Don't care.

	pin	pin	output pin	input pin	prohibited	

[Legend] x: Don't care.

9.4 Port 5

Port 5 is an I/O port also functioning as a wakeup interrupt input pin and LCD segment
Figure 9.4 shows its pin configuration.

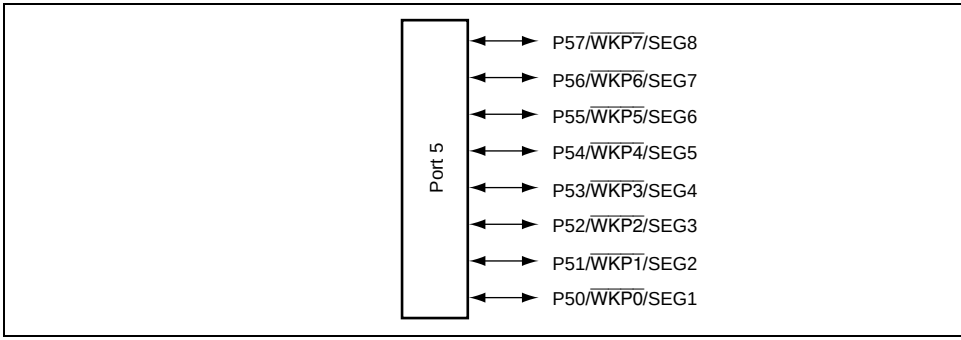


Figure 9.4 Port 5 Pin Configuration

Port 5 has the following registers.

- Port data register 5 (PDR5)
- Port control register 5 (PCR5)
- Port pull-up control register 5 (PUCR5)
- Port mode register 5 (PMR5)

2	P52	0	R/W	
1	P51	0	R/W	
0	P50	0	R/W	

9.4.2 Port Control Register 5 (PCR5)

PCR5 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 5.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR57	0	W	Setting a PCR5 bit to 1 makes the correspondi
6	PCR56	0	W	output pin, while clearing the bit to 0 makes the
5	PCR55	0	W	input pin. The settings in PCR5 and in PDR5 a
4	PCR54	0	W	when the corresponding pin is designated as a I/O pin.
3	PCR53	0	W	PCR5 is a write-only register. These bits are al
2	PCR52	0	W	read as 1.
1	PCR51	0	W	
0	PCR50	0	W	

3	PUCR53	0	R/W
2	PUCR52	0	R/W
1	PUCR51	0	R/W
0	PUCR50	0	R/W

9.4.4 Port Mode Register 5 (PMR5)

PMR5 controls the selection of functions for port 5 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	WKP7	0	R/W	P5n/$\overline{\text{WKPn}}$/SEGn+1 Pin Function Switch
6	WKP6	0	R/W	When pin P5n/$\overline{\text{WKPn}}$/SEGn+1 is not used as
5	WKP5	0	R/W	these bits select whether the pin is used as P5
4	WKP4	0	R/W	$\overline{\text{WKPn}}$.
3	WKP3	0	R/W	0: P5n I/O pin
2	WKP2	0	R/W	1: $\overline{\text{WKPn}}$ input pin
1	WKP1	0	R/W	(n = 7 to 0)
0	WKP0	0	R/W	

Note: For use as SEGn+1, see section 19.3.1, LCD Port Control Register (LPCR).

WKPn	0		1	x
PCR5n	0	1	x	x
Pin Function	P5n input pin	P5n output pin	$\overline{\text{WKPn}}$ input pin	SEGn+1 output pin

[Legend] x: Don't care.

- P53/$\overline{\text{WKP3}}$/SEG4 to P50/$\overline{\text{WKP0}}$/SEG1 pins

  The pin function is switched as shown below according to the combination of the WK
  PMR5, PCR5m bit in PCR5, and SGS3 to SGS0 bits in LPCR.

(m =

SGS3 to SGS0	Other than B'0001, B'0010, B'0011, B'0100, B'0101, B'0110, B'0111, B'1000			B'0001, B'0010, B'0011, B B'0101, B'0110, B'0111, B
WKPm	0		1	x
PCR5m	0	1	x	x
Pin Function	P5m input pin	P5m output pin	$\overline{\text{WKPm}}$ input pin	SEGm+1 output pin

[Legend] x: Don't care.

[Legend] x: Don't care.

9.5 Port 6

Port 6 is an I/O port also functioning as an LCD segment output pin. Figure 9.5 shows it configuration.

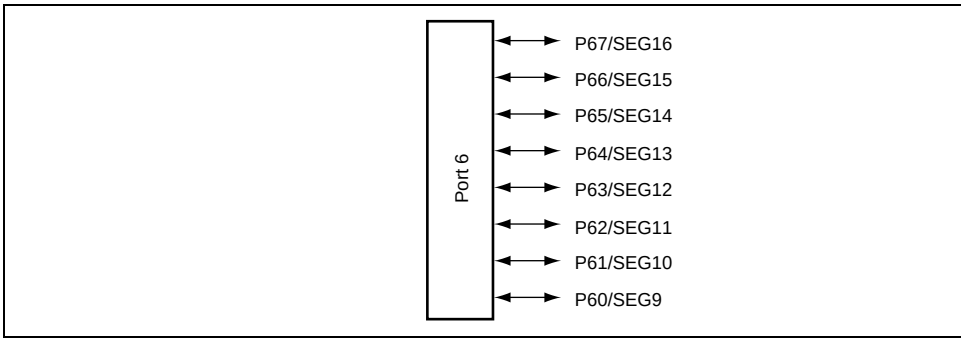


Figure 9.5 Port 6 Pin Configuration

Port 6 has the following registers.

- Port data register 6 (PDR6)
- Port control register 6 (PCR6)
- Port pull-up control register 6 (PUCR6)

3	P63	0	R/W	
2	P62	0	R/W	
1	P61	0	R/W	
0	P60	0	R/W	

9.5.2 Port Control Register 6 (PCR6)

PCR6 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 6.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR67	0	W	Setting a PCR6 bit to 1 makes the correspondi
6	PCR66	0	W	output pin, while clearing the bit to 0 makes the input pin. The settings in PCR6 and in PDR6 a
5	PCR65	0	W	when the corresponding pin is designated as a
4	PCR64	0	W	I/O pin.
3	PCR63	0	W	PCR6 is a write-only register. These bits are al
2	PCR62	0	W	read as 1.
1	PCR61	0	W	
0	PCR60	0	W	

3	PUCR63	0	R/W
2	PUCR62	0	R/W
1	PUCR61	0	R/W
0	PUCR60	0	R/W

9.5.4 Pin Functions

The relationship between the register settings and the port functions is shown below.

- P67/SEG16 to P64/SEG13 pins

  The pin function is switched as shown below according to the combination of the PC
  PCR6 and SGS3 to SGS0 bits in LPCR.

(n =

SGS3 to SGS0	Other than B'0100, B'0101, B'0110, B'0111, B'1000, B'1001, B'1010, B'1011		B'0100, B'0101, B'0110, B B'1000, B'1001, B'1010,
PCR6n	0	1	x
Pin Function	P6n input pin	P6n output pin	SEGn+9 output pi

[Legend] x: Don't care.

9.5.5 Input Pull-Up MOS

Port 6 has an on-chip input pull-up MOS function that can be controlled by software. Wh
PCR6 bit is cleared to 0, setting the corresponding PUCR6 bit to 1 turns on the input pull
for that pin. The input pull-up MOS function is in the off state after a reset.

(n = 7 t

PCR6n	0		1
PUCR6n	0	1	x
Input Pull-Up MOS	Off	On	Off

[Legend] x: Don't care.

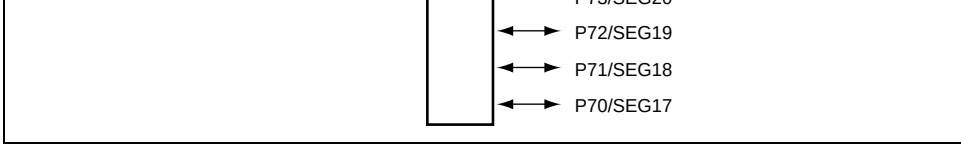


Figure 9.6 Port 7 Pin Configuration

Port 7 has the following registers.

- Port data register 7 (PDR7)
- Port control register 7 (PCR7)

9.6.1 Port Data Register 7 (PDR7)

PDR7 is a register that stores data of port 7.

Bit	Bit Name	Initial Value	R/W	Description
7	P77	0	R/W	If port 7 is read while PCR7 bits are set to 1, t
6	P76	0	R/W	stored in PDR7 are read, regardless of the ac
5	P75	0	R/W	states. If port 7 is read while PCR7 bits are cl
4	P74	0	R/W	the pin states are read.
3	P73	0	R/W	
2	P72	0	R/W	
1	P71	0	R/W	
0	P70	0	R/W	

3	PCR73	0	W	PCR7 is a write-only register. These bits are al
2	PCR72	0	W	read as 1.
1	PCR71	0	W	
0	PCR70	0	W	

9.6.3 Pin Functions

The relationship between the register settings and the port functions is shown below.

- P77/SEG24 to P74/SEG21 pins

  The pin function is switched as shown below according to the combination of the PCR
  PCR7 and SGS3 to SGS0 bits in LPCR.

(n =

SGS3 to SGS0	Other than B'0110, B'0111, B'1000, B'1001, B'1010, B'1011, B'1100, B'1101		B'0110, B'0111, B'1000, B'1 B'1010, B'1011, B'1100, B'1
PCR7n	0	1	x
Pin Function	P7n input pin	P7n output pin	SEGn+17 output pi

[Legend] x: Don't care.

9.7 Port 8

Port 8 is an I/O port also functioning as an LCD segment output pin. Figure 9.7 shows it
configuration.

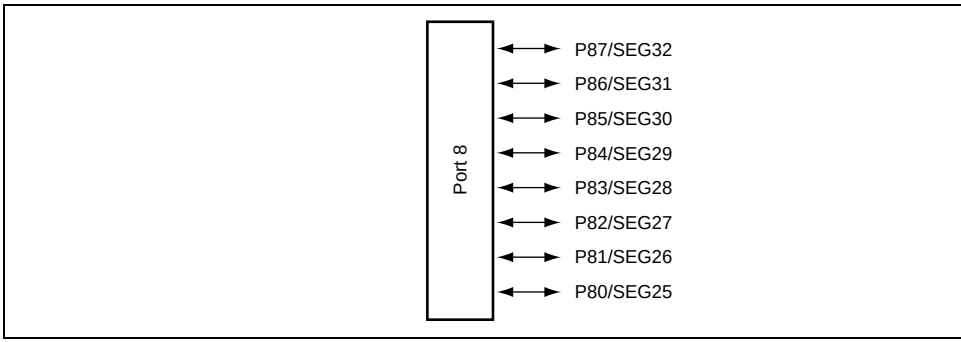


Figure 9.7 Port 8 Pin Configuration

Port 8 has the following registers.

- Port data register 8 (PDR8)
- Port control register 8 (PCR8)

3	P83	0	R/W	
2	P82	0	R/W	
1	P81	0	R/W	
0	P80	0	R/W	

9.7.2 Port Control Register 8 (PCR8)

PCR8 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 8.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR87	0	W	Setting a PCR8 bit to 1 makes the correspondi
6	PCR86	0	W	(P87 to P80) an output pin, while clearing the b
5	PCR85	0	W	makes the pin an input pin. The settings in PCR
4	PCR84	0	W	PDR8 are valid when the corresponding pin is designated as a general I/O pin.
3	PCR83	0	W	PCR8 is a write-only register. These bits are al
2	PCR82	0	W	read as 1.
1	PCR81	0	W	
0	PCR80	0	W	

PCR8n	0	1	x
Pin Function	P8n input pin	P8n output pin	SEGn+25 output pi

[Legend] x: Don't care.

- P83/SEG28 to P80/SEG25 pins

  The pin function is switched as shown below according to the combination of the PC
  in PCR8 and SGS3 to SGS0 bits in LPCR.

(m =

SGS3 to SGS0	Other than B'0111, B'1000, B'1001, B'1010, B'1011, B'1100, B'1101, B'1110		B'0111, B'1000, B'1001, B B'1011, B'1100, B'1101,
PCR8m	0	1	x
Pin Function	P8m input pin	P8m output pin	SEGm+25 output p

[Legend] x: Don't care.

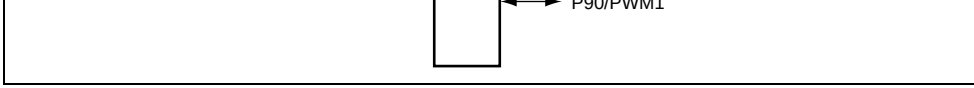


Figure 9.8 Port 9 Pin Configuration

Port 9 has the following registers.

- Port data register 9 (PDR9)
- Port control register 9 (PCR9)
- Port mode register 9 (PMR9)

9.8.1 Port Data Register 9 (PDR9)

PDR9 is a register that stores data of port 9.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1 and cannot be
3	P93	1	R/W	If port 9 is read while PCR9 bits are set to 1, th
2	P92	1	R/W	stored in PDR9 are read, regardless of the actu
1	P91	1	R/W	states. If port 9 is read while PCR9 bits are clea
0	P90	1	R/W	the pin states are read.

1	PCR91	0	W	when the corresponding pin is designated as a
0	PCR90	0	W	I/O pin. PCR9 is a write-only register. These bits are a read as 1.

9.8.3 Port Mode Register 9 (PMR9)

PMR9 controls the selection of functions for port 9 pins.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1 and cannot b
3	—	0	R/W	Reserved Although this bit is readable/writable, 1 should written to this bit.
2	IRQ4	0	R/W	P92/$\overline{\text{IRQ4}}$ Pin Function Switch Selects whether pin P92/$\overline{\text{IRQ4}}$ is used as P92 $\overline{\text{IRQ4}}$. 0: P92 I/O pin 1: $\overline{\text{IRQ4}}$ input pin

The relationship between the register settings and the port functions is shown below.

- P93 pin

  The pin function is switched as shown below according to the PCR93 bit in PCR9.

PCR93	0	1
Pin Function	P93 input pin	P93 output pin

- P92/$\overline{\text{IRQ4}}$ pin

  The pin function is switched as shown below according to the combination of the IRQ PMR9 and PCR92 bit in PCR9.

IRQ4	0		1	
PCR92	0	1	0	1
Pin Function	P92 input pin	P92 output pin	$\overline{\text{IRQ4}}$ input pin	Sett prohi

- P91/PWM2, P90/PWM1 pins

  The pin function is switched as shown below according to the combination of the PW in PMR9 and PCR9n bit in PCR9.

(

PWMn+1	0		1
PCR9n	0	1	x
Pin Function	P9n input pin	P9n output pin	PWMn+1 output pin

[Legend] x: Don't care.

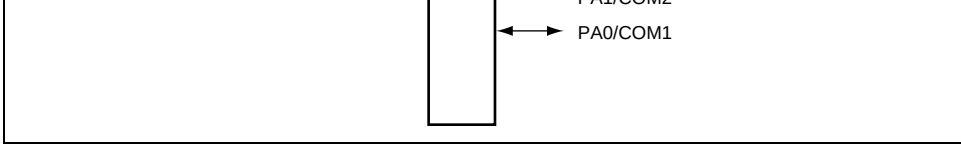


Figure 9.9 Port A Pin Configuration

Port A has the following registers.

- Port data register A (PDRA)
- Port control register A (PCRA)

9.9.1 Port Data Register A (PDRA)

PDRA is a register that stores data of port A.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1 and cannot b
3	PA3	0	R/W	If port A is read while PCRA bits are set to 1, t stored in PDRA are read, regardless of the ac states. If port A is read while PCRA bits are cl the pin states are read.
2	PA2	0	R/W	
1	PA1	0	R/W	
0	PA0	0	R/W	

1	PCRA1	0	W	when the corresponding pin is designated as a
0	PCRA0	0	W	I/O pin. PCRA is a write-only register. These bits are al read as 1.

9.9.3 Pin Functions

The relationship between the register settings and the port functions is shown below.

- PA3/COM4 pin

  The pin function depends on bit PCRA3 in PCRA and bits DTS1 and DTS0, bit CMX
  SGS3 to SGS0 in LPCR.

DTS1 to DTS0, CMX	x		Other than B'000, B'010, B'10*	B'000, B'010, B	
SGS3 to SGS0	B'0000		Other than B'0000		
PCRA3	0	1	x	0	
Pin Function	PA3 input pin*[1]	PA3 output pin*[1]	COM4 output pin	Leave open*[2]	L o

[Legend] x: Don't care.

Note: 1. The board power supply level is Vcc.
2. The board power supply level is the LCD drive power supply voltage level.

[Legend] x: Don't care.

Note: 1. The board power supply level is Vcc.
2. The board power supply level is the LCD drive power supply voltage level.

- PA1/COM2 pin

  The pin function depends on bit PCRA1 in PCRA and bits DTS1 and DTS0, bit CM
  SGS3 to SGS0 in LPCR.

DTS1 to DTS0, CMX	x		Other than B'000	B'000	
SGS3 to SGS0	B'0000		Other than B'0000		
PCRA1	0	1	x	0	
Pin Function	PA1 input pin*1	PA1 output pin*1	COM2 output pin	Leave open*2	

[Legend] x: Don't care.

Note: 1. The board power supply level is Vcc.
2. The board power supply level is the LCD drive power supply voltage level.

- PA0/COM1 pin

  The pin function depends on bit PCRA0 in PCRA and bits DTS1 and DTS0, bit CM
  SGS3 to SGS0 in LPCR.

DTS1 to DTS0, CMX	x		
SGS3 to SGS0	B'0000		Other than
PCRA0	0	1	x
Pin Function	PA0 input pin	PA0 output pin	COM1 out

[Legend] x: Don't care.

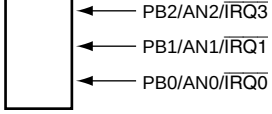


Figure 9.10 Port B Pin Configuration

Port B has the following registers.

- Port data register B (PDRB)
- Port mode register B (PMRB)

9.10.1 Port Data Register B (PDRB)

PDRB is a register that stores data of port B.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7	Undefined	R	Reading PDRB always gives the pin states. Ho
6	PB6	Undefined	R	a port B pin is selected as an analog input char
5	PB5	Undefined	R	the CH3 to CH0 bits in AMR of the A/D convert
4	PB4	Undefined	R	AIN1, that pin is read as 0 regardless of the inp
3	PB3	Undefined	R	voltage.
2	PB2	Undefined	R	
1	PB1	Undefined	R	
0	PB0	Undefined	R	

				as ADTRG. 0: TEST pin 1: $\overline{\text{ADTRG}}$ input pin For details on the setting of the $\overline{\text{ADTRG}}$ input to section 18.4.2, External Trigger Input Timin
3	—	1	—	Reserved This bit is always read as 1 and cannot be mo
2	IRQ3	0	R/W	PB2/AN2/$\overline{\text{IRQ3}}$ Pin Function Switch Selects whether pin PB2/AN2/$\overline{\text{IRQ3}}$ is used as or as $\overline{\text{IRQ3}}$. 0: PB2/AN2 input pin 1: $\overline{\text{IRQ3}}$ input pin
1	IRQ1	0	R/W	PB1/AN1/$\overline{\text{IRQ1}}$ Pin Function Switch Selects whether pin PB1/AN1/$\overline{\text{IRQ1}}$ is used as or as $\overline{\text{IRQ1}}$. 0: PB1/AN1 input pin 1: $\overline{\text{IRQ1}}$ input pin
0	IRQ0	0	R/W	PB0/AN0/$\overline{\text{IRQ0}}$ Pin Function Switch Selects whether pin PB0/AN0/$\overline{\text{IRQ0}}$ is used as or as $\overline{\text{IRQ0}}$. 0: PB0/AN0 input pin 1: $\overline{\text{IRQ0}}$ input pin

- PB6/AN6 pin

  The pin function is switched as shown below according to the CH3 to CH0 bits in AM

CH3 to CH0	Other than B'1010	B'1010
Pin Function	PB6 input pin	AN6 input pin

- PB5/AN5 pin

  The pin function is switched as shown below according to the CH3 to CH0 bits in AM

CH3 to CH0	Other than B'1001	B'1001
Pin Function	PB5 input pin	AN5 input pin

- PB4/AN4 pin

  The pin function is switched as shown below according to the CH3 to CH0 bits in AM

CH3 to CH0	Other than B'1000	B'1000
Pin Function	PB4 input pin	AN4 input pin

- PB3/AN3 pin

  The pin function is switched as shown below according to the CH3 to CH0 bits in AM

CH3 to CH0	Other than B'0111	B'0111
Pin Function	PB3 input pin	AN3 input pin

- PB1/AN1/IRQ1 pin

  The pin function is switched as shown below according to the combination of the CH
  bits in AMR and IRQ1 bit in PMRB.

IRQ1	0		1
CH3 to CH0	Other than B'0101	B'0101	x
Pin Function	PB1 input pin	AN1 input pin	$\overline{\text{IRQ1}}$ input pin

[Legend] x: Don't care.

- PB0/AN0/$\overline{\text{IRQ0}}$ pin

  The pin function is switched as shown below according to the combination of the CH
  bits in AMR and IRQ0 bit in PMRB.

IRQ0	0		1
CH3 to CH0	Other than B'0100	B'0100	x
Pin Function	PB0 input pin	AN0 input pin	$\overline{\text{IRQ0}}$ input pin

[Legend] x: Don't care.

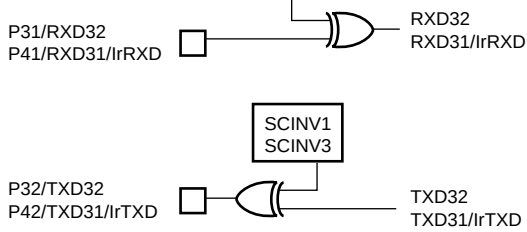


Figure 9.11 Input/Output Data Inversion Function

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved These bits are always read as 1 and cannot be
5	SPC32	0	R/W	P32/TXD32/SCL Pin Function Switch Selects whether pin P32/TXD32/SCL is used a P32/SCL or as TXD32. 0: P32/SCL I/O pin 1: TXD32 output pin* Note: * Set the TE32 bit in SCR32 after setting 1.

				pin is to be inverted or not. 0: TXD32 output data is not inverted 1: TXD32 output data is inverted
2	SCINV2	0	R/W	RXD32 Pin Input Data Inversion Switch Specifies whether the input data polarity of the pin is to be inverted or not. 0: RXD32 input data is not inverted 1: RXD32 input data is inverted
1	SCINV1	0	R/W	TXD31/IrTXD Pin Output Data Inversion Switc Specifies whether the output data polarity of t TXD31/IrTXD pin is to be inverted or not. 0: TXD31/IrTXD output data is not inverted 1: TXD31/IrTXD output data is inverted
0	SCINV0	0	R/W	RXD31/IrRXD Pin Input Data Inversion Switch Specifies whether the input data polarity of the RXD31/IrRXD pin is to be inverted or not. 0: RXD31/IrRXD input data is not inverted 1: RXD31/IrRXD input data is inverted

Note: When the serial port control register is modified, the data being input or output up point is inverted immediately after the modification, and an invalid data change is output. When modifying the serial port control register, modification must be mad in which data changes are invalidated.

— For a pin also used by the A/D converter, pull it up to AVcc. With an external resi
approximately 100 kΩ.

- If an unused pin is an output pin, it is recommended to handle it in one of the followi
  — Set the output of the unused pin to high and pull it up to Vcc with an external resis
  approximately 100 kΩ.
  — Set the output of the unused pin to low and pull it down to GND with an external
  approximately 100 kΩ.

- Reset function
- Readable/writable counter of seconds, minutes, hours, and day-of-week with BCD c
- Periodic (0.25 seconds, 0.5 seconds, one second, minute, hour, day, and week) interr
- 8-bit free running counter
- Selection of clock source
- Use of module standby mode enables this module to be placed in standby mode inde when not used. (For details, refer to section 6.4, Module Standby Function.)

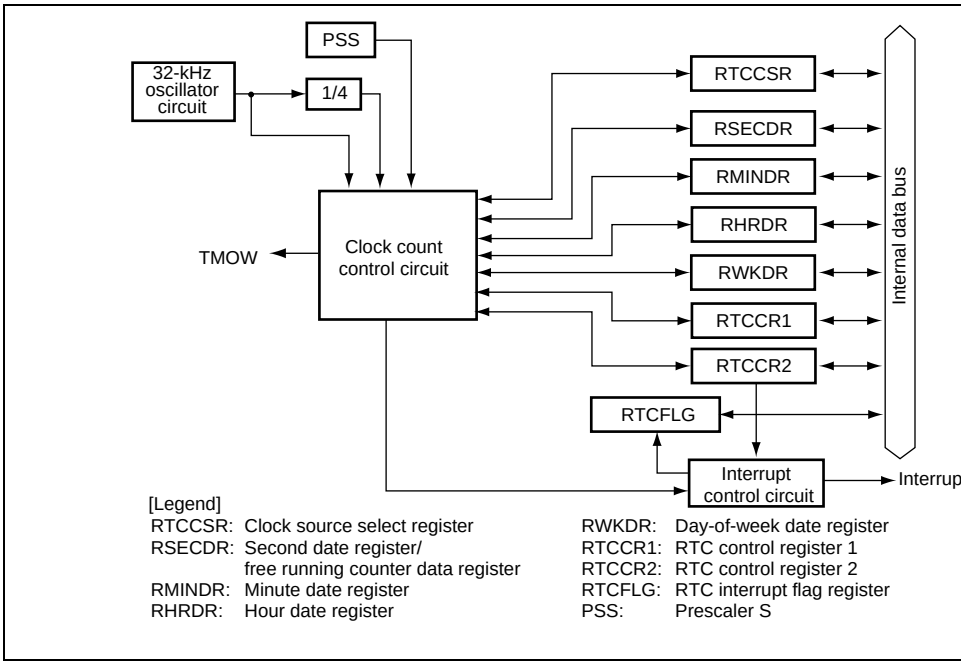


Figure 10.1 Block Diagram of RTC

The RTC has the following registers.

- Second data register/free running counter data register (RSECDR)
- Minute data register (RMINDR)
- Hour data register (RHRDR)
- Day-of-week data register (RWKDR)
- RTC control register 1 (RTCCR1)
- RTC control register 2 (RTCCR2)
- Clock source select register (RTCCSR)
- RTC Interrupt flag register (RTCFLG)

				registers. When this bit is 0, the values of secon hour, and day-of-week data registers must be a
6	SC12	—	R/W	Counting Ten's Position of Seconds
5	SC11	—	R/W	Counts on 0 to 5 for 60-second counting.
4	SC10	—	R/W	
3	SC03	—	R/W	Counting One's Position of Seconds
2	SC02	—	R/W	Counts on 0 to 9 once per second. When a carr
1	SC01	—	R/W	generated, 1 is added to the ten's position.
0	SC00	—	R/W	

10.3.2 Minute Data Register (RMINDR)

RMINDR counts the BCD-coded minute value on the carry generated once per minute b RSECDR counting. The setting range is decimal 00 to 59.

Bit	Bit Name	Initial Value	R/W	Description
7	BSY	—	R	RTC Busy This bit is set to 1 when the RTC is updating (o the values of second, minute, hour, and day-of- registers. When this bit is 0, the values of secon hour, and day-of-week data registers must be a
6	MN12	—	R/W	Counting Ten's Position of Minutes
5	MN11	—	R/W	Counts on 0 to 5 for 60-minute counting.
4	MN10	—	R/W	
3	MN03	—	R/W	Counting One's Position of Minutes
2	MN02	—	R/W	Counts on 0 to 9 once per minute. When a carr
1	MN01	—	R/W	generated, 1 is added to the ten's position.
0	MN00	—	R/W	

				registers. When this bit is 0, the values of second hour, and day-of-week data registers must be ac
6	—	0	—	Reserved This bit is always read as 0.
5	HR11	—	R/W	Counting Ten's Position of Hours
4	HR10	—	R/W	Counts on 0 to 2 for ten's position of hours.
3	HR03	—	R/W	Counting One's Position of Hours
2	HR02	—	R/W	Counts on 0 to 9 once per hour. When a carry is generated, 1 is added to the ten's position.
1	HR01	—	R/W	
0	HR00	—	R/W	

				hour, and day-of-week data registers must be a
6 to 3	—	All 0	—	Reserved These bits are always read as 0.
2	WK2	—	R/W	Day-of-Week Counting
1	WK1	—	R/W	Day-of-week is indicated with a binary code
0	WK0	—	R/W	000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday 111: Setting prohibited

6	12/24	—	R/W	Operating Mode 0: RTC operates in 12-hour mode. RHRDR coun to 11. 1: RTC operates in 24-hour mode. RHRDR coun to 23.
5	PM	—	R/W	A.m./P.m. 0: Indicates a.m. when RTC is in the 12-hour mod 1: Indicates p.m. when RTC is in the 12-hour mod
4	RST	0	R/W	Reset 0: Normal operation 1: Resets registers and control circuits except RT and this bit. Clear this bit to 0 after having beer
3	—	0	R/W*	Reserved
2 to 0	—	All 0	—	Reserved These bits are always read as 0.

Note: * Only 0 can be written to this bit.

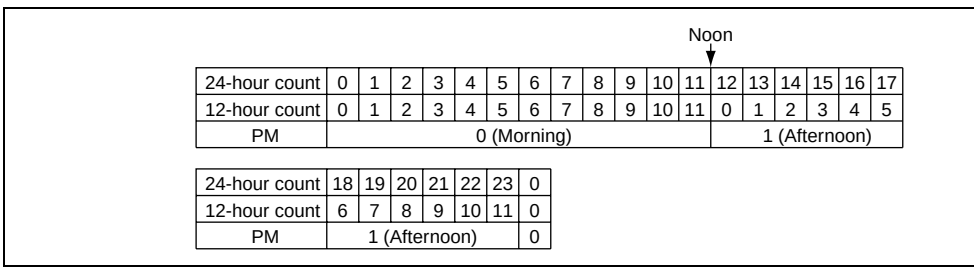


Figure 10.2 Definition of Time Expression

				0: Disables an overflow interrupt 1: Enables an overflow interrupt
6	WKIE	—	R/W	Week Periodic Interrupt Enable 0: Disables a week periodic interrupt 1: Enables a week periodic interrupt
5	DYIE	—	R/W	Day Periodic Interrupt Enable 0: Disables a day periodic interrupt 1: Enables a day periodic interrupt
4	HRIE	—	R/W	Hour Periodic Interrupt Enable 0: Disables an hour periodic interrupt 1: Enables an hour periodic interrupt
3	MNIE	—	R/W	Minute Periodic Interrupt Enable 0: Disables a minute periodic interrupt 1: Enables a minute periodic interrupt
2	1SEIE	—	R/W	One-Second Periodic Interrupt Enable 0: Disables a one-second periodic interrupt 1: Enables a one-second periodic interrupt
1	05SEIE	—	R/W	0.5-Second Periodic Interrupt Enable 0: Disables a 0.5-second periodic interrupt 1: Enables a 0.5-second periodic interrupt
0	025SEIE	—	R/W	0.25-Second Periodic Interrupt Enable 0: Disables a 0.25-second periodic interrupt 1: Enables a 0.25-second periodic interrupt

7	—	0	—	Reserved This bit is always read as 0.
6	RCS6	0	R/W	Clock Output Selection
5	RCS5	0	R/W	Select a clock output from the TMOW pin when s
4	SUB32K	0	R/W	the TMOW bit in PMR3 to 1. 000: φ/4 010: φ/8 100: φ/16 110: φ/32 xx1: φw
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: φ/8..... Free running counter opera
1	RCS1	0	R/W	0001: φ/32..... Free running counter opera
0	RCS0	0	R/W	0010: φ/128..... Free running counter opera 0011: φ/256..... Free running counter opera 0100: φ/512..... Free running counter opera 0101: φ/2048..... Free running counter opera 0110: φ/4096..... Free running counter opera 0111: φ/8192..... Free running counter opera 1000: φw/4 ..... RTC operation Settings other than the above are prohibited.

[Legend] x: Don't care.

6	WKIFG	—	R/W*	[Setting condition] When a week periodic interrupt occurs [Clearing condition] 0 is written to WKIFG when WKIFG = 1
5	DYIFG	—	R/W*	[Setting condition] When a day periodic interrupt occurs [Clearing condition] 0 is written to DYIFG when DYIFG = 1
4	HRIFG	—	R/W*	[Setting condition] When an hour periodic interrupt occurs [Clearing condition] 0 is written to HRIFG when HRIFG = 1
3	MNIFG	—	R/W*	[Setting condition] When a minute periodic interrupt occurs [Clearing condition] 0 is written to MNIFG when MNIFG = 1
2	SEIFG	—	R/W*	[Setting condition] When a one-second periodic interrupt occurs [Clearing condition] 0 is written to SEIFG when SEIFG = 1
1	05SEIFG	—	R/W*	[Setting condition] When a 0.5-second periodic interrupt occurs [Clearing condition] 0 is written to 05SEIFG when 05SEIFG = 1
0	025SEIFG	—	R/W*	[Setting condition] When a 0.25-second periodic interrupt occurs [Clearing condition] 0 is written to 025SEIFG when 025SEIFG = 1

Note: * Only 0 can be written to clear the flag.

follow this procedure.

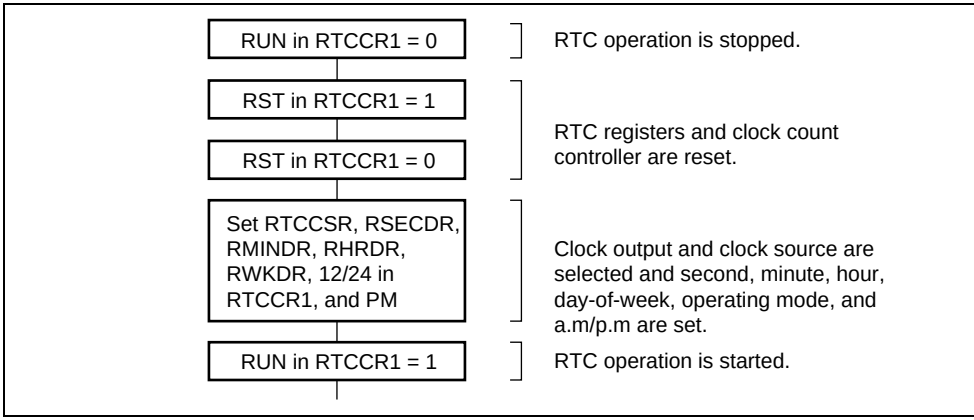


Figure 10.3 Initial Setting Procedure

bit is set to 1, the registers are updated, and the BSY bit is cleared to 0.

2. Making use of interrupts, read from the second, minute, hour, and day-of week regis the corresponding flag of RTCFLG is set to 1 and the BSY bit is confirmed to be 0.
3. Read from the second, minute, hour, and day-of week registers twice in a row, and if no change in the read data, the read data is used.

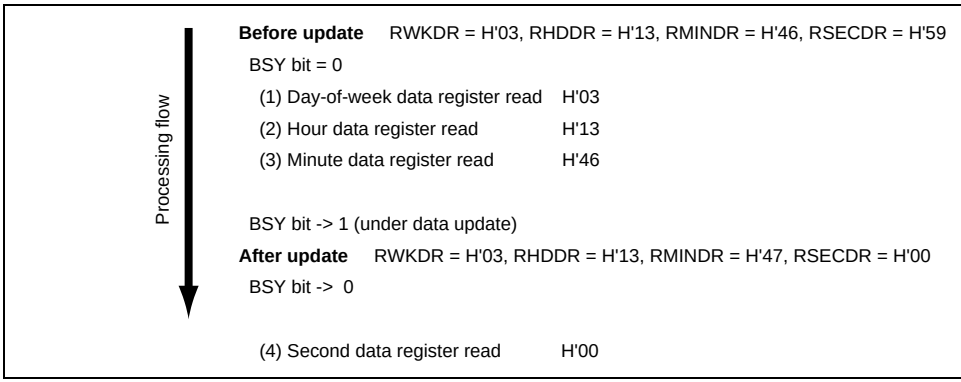


Figure 10.4 Example: Reading of Inaccurate Time Data

Table 10.2 Interrupt Sources

Interrupt Name	Interrupt Source	Interrupt En
Overflow interrupt	Occurs when the free running counter is overflown.	FOIE
Week periodic interrupt	Occurs every week when the day-of-week date register value becomes 0.	WKIE
Day periodic interrupt	Occurs every day when the day-of-week date register is counted.	DYIE
Hour periodic interrupt	Occurs every hour when the hour date register is counted.	HRIE
Minute periodic interrupt	Occurs every minute when the minute date register is counted.	MNIE
One-second periodic interrupt	Occurs every second when the one-second date register is counted.	1SEIE
0.5-second periodic interrupt	Occurs every 0.5 seconds.	05SEIE
0.25-second periodic interrupt	Occurs every 0.25 seconds.	025SEIE

a WDT overflow. As a result, its contents are undefined after power-on. Therefore, whe
RTC interrupt, always initialize the RTC register before setting IENRTC in IENR1 to 1.

- Choice of five counter input clocks
  Internal clocks (ϕ/32, ϕ/16, ϕ/4, and ϕ_w/4) or external clocks can be selected.
- Toggle output function
  Toggle output is performed to the TMOFH or TMOFL pin using a compare match si
  The initial value of toggle output can be set.
- Counter resetting by a compare match signal
- Two interrupt sources: One compare match, one overflow
- Choice of 16-bit or 8-bit mode by settings of bits CKSH2 to CKSH0 in TCRF
- Can operate in watch mode, subactive mode, and subsleep mode
  When ϕ_w/4 is selected as an internal clock, the timer F can operate in watch mode, su
  mode, and subsleep mode.
- Use of module standby mode enables this module to be placed in standby mode inde
  when not used. (For details, refer to section 6.4, Module Standby Function.)

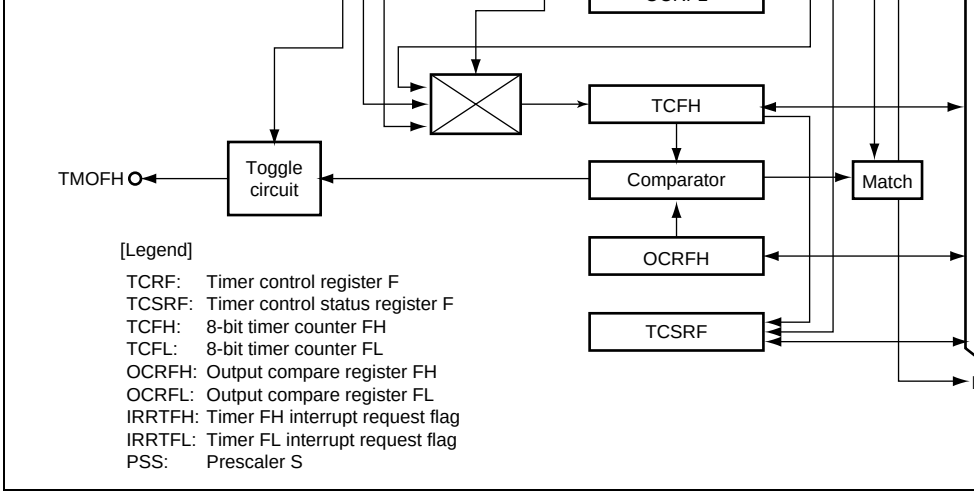


Figure 11.1 Block Diagram of Timer F

11.2 Input/Output Pins

Table 11.1 shows the input/output pins of the timer F.

Table 11.1 Pin Configuration

Name	Abbreviation	I/O	Function
Timer F event input	TMIF	Input	Event input pin to TCFL
Timer FH output	TMOFH	Output	Timer FH toggle output pin
Timer FL output	TMOFL	Output	Timer FL toggle output pin

TCF is a 16-bit read/write up-counter configured by cascaded connection of 8-bit timer
TCFH and TCFL. In addition to the use of TCF as a 16-bit counter with TCFH as the up
and TCFL as the lower 8 bits, TCFH and TCFL can also be used as independent 8-bit co

TCFH and TCFL are initialized to H'00 upon a reset.

(1) 16-Bit Mode (TCF)

When CKSH2 is cleared to 0 in TCRF, TCF operates as a 16-bit counter. The TCF inpu
selected by bits CKSL2 to CKSL0 in TCRF.

TCF can be cleared in the event of a compare match by means of CCLRH in TCSRF.

When TCF overflows from H'FFFF to H'0000, OVFH is set to 1 in TCSRF. If OVIEH i
is 1 at this time, IRRTFH is set to 1 in IRR2, and if IENTFH in IENR2 is 1, an interrupt
sent to the CPU.

(2) 8-Bit Mode (TCFH/TCFL)

When CKSH2 is set to 1 in TCRF, TCFH and TCFL operate as two independent 8-bit co
The TCFH (TCFL) input clock is selected by bits CKSH2 to CKSH0 (CKSL2 to CKSL
TCRF.

TCFH (TCFL) can be cleared in the event of a compare match by means of CCLRH (CC
TCSRF.

When TCFH (TCFL) overflows from H'FF to H'00, OVFH (OVFL) is set to 1 in TCSRF
OVIEH (OVIEL) in TCSRF is 1 at this time, IRRTFH (IRRTFL) is set to 1 in IRR2, and
IENTFH (IENTFL) in IENR2 is 1, an interrupt request is sent to the CPU.

is sent to the CPU.

Toggle output can be provided from the TMOFH pin by means of compare matches, and output level can be set by means of the TOLH bit in TCRF.

(2) 8-Bit Mode (OCRFH/OCRFL)

When CKSH2 is set to 1 in TCRF, OCRFH and OCRFL operate as two independent 8-bi registers. OCRFH contents are compared with TCFH, and OCRFL contents are with TCF the OCRFH (OCRFL) and TCFH (TCFL) values match, CMFH (CMFL) is set to 1 in TC the same time, IRRTFH (IRRTFL) is set to 1 in IRR2. If IENTFH (IENTFL) in IENR2 is time, an interrupt request is sent to the CPU.

Toggle output can be provided from the TMOFH pin (TMOFL pin) by means of compare matches, and the output level can be set by means of the TOLH (TOLL) bit in TCRF.

6	CKSH2	0	W	Clock Select H
5	CKSH1	0	W	Select the clock input to TCFH from among fo
4	CKSH0	0	W	clock sources or TCFL overflow. 000: 16-bit mode, counting on TCFL overflow 001: 16-bit mode, counting on TCFL overflow 010: 16-bit mode, counting on TCFL overflow 011: Using prohibited 100: 8-bit mode, counting on ϕ/32 101: 8-bit mode, counting on ϕ/16 110: 8-bit mode, counting on ϕ/4 111: 8-bit mode, counting on ϕ_w/4
3	TOLL	0	W	Toggle Output Level L Sets the TMOFL pin output level. 0: Low level 1: High level

				100: Internal clock: counting on ϕ/32 101: Internal clock: counting on ϕ/16 110: Internal clock: counting on ϕ/4 111: Internal clock: counting on ϕ_w/4

Note: * The TMIFEG bit in IEGR selects which edge of an external event is used for co

11.3.4 Timer Control/Status Register F (TCSRF)

TCSRF performs counter clear selection, overflow flag setting, and compare match flag s and controls enabling of overflow interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	OVFH	0	R/W*	Timer Overflow Flag H [Setting condition] When TCFH overflows from H'FF to H'00 [Clearing condition] When this bit is written to 0 after reading OVFH
6	CMFH	0	R/W*	Compare Match Flag H This is a status flag indicating that TCFH has m OCRFH. [Setting condition] When the TCFH value matches the OCRFH va [Clearing condition] When this bit is written to 0 after reading CMFH

				OCRFH match. In 16-bit mode: 0: TCF clearing by compare match is disabled 1: TCF clearing by compare match is enabled In 8-bit mode: 0: TCFH clearing by compare match is disable 1: TCFH clearing by compare match is enable
3	OVFL	0	R/W*	Timer Overflow Flag L This is a status flag indicating that TCFL has o [Setting condition] When TCFL overflows from H'FF to H'00 [Clearing condition] When this bit is written to 0 after reading OVF
2	CMFL	0	R/W*	Compare Match Flag L This is a status flag indicating that TCFL has r OCRFL. [Setting condition] When the TCFL value matches the OCRFL va [Clearing condition] When this bit is written to 0 after reading CMF

0: TCFL clearing by compare match is disabled
1: TCFL clearing by compare match is enabled

Note: * Only 0 can be written to clear the flag.

11.4 Operation

The timer F is a 16-bit counter that increments on each input clock pulse. The timer F val
constantly compared with the value set in the output compare register F, and the counter
cleared, an interrupt requested, or port output toggled, when the two values match. The ti
can also be used as two independent 8-bit timers.

11.4.1 Timer F Operation

The timer F has two operating modes, 16-bit timer mode and 8-bit timer mode. The opera
each of these modes is described below.

(1) Operation in 16-Bit Timer Mode

When the CKSH2 bit is cleared to 0 in TCRF, the timer F operates as a 16-bit timer.

Following a reset, TCF is initialized to H'0000, OCRF to H'FFFF, and TCRF and TCSRF
The counter is incremented by an input signal from an external event (TMIF pin). The TM
bit in IEGR selects which edge of an external event is used for counting.

The timer F operating clock can be selected from internal clocks or external events accor
settings of bits CKSL2 to CKSL0 in TCRF.

OCRF contents are constantly compared with TCF, and when both values match, CMFH
1 in TCSRF. If IENTFH in IENR2 is 1 at this time, an interrupt request is sent to the CPU

When the OCRFH/OCRFL and TCFH/TCFL values match, CMFH/CMFL is set to 1 in IENTFH/IENTFL in IENR2 is 1, an interrupt request is sent to the CPU, and at the same TMOFH pin/TMOFL pin output is toggled. If CCLRH/CCLRL in TCSRF is 1, TCFH/T cleared. The output level of the TMOFH pin/TMOFL pin can be set by TOLH/TOLL in

When TCFH/TCFL overflows from H'FF to H'00, OVFH/OVFL is set to 1 in TCSRF. I OVIEH/OVIEL in TCSRF and IENTFH/IENTFL in IENR2 are both 1, an interrupt requ to the CPU.

11.4.2 TCF Increment Timing

(1) Internal Clock Operation

TCF is incremented by internal clock or external event input. Bits CKSH2 to CKSH0 or CKSL0 in TCRF select one of internal clock sources (ϕ/32, ϕ/16, ϕ/4, or ϕ_W/4) created b the system clock (ϕ or ϕ_W).

(2) External Event Operation

When the CKSL2 bit in TCRF is cleared to 0, external event input is selected. The coun incremented at both rising and falling edges of external events. The TMIFEG bit in IEG which edge of an external event is used for counting. The external event pulse width req clock time longer than 2 system clocks (ϕ), or 2 subclocks (ϕ_{SUB}), depending on the oper mode. Note that an external event does not operate correctly with the lower pulse width.

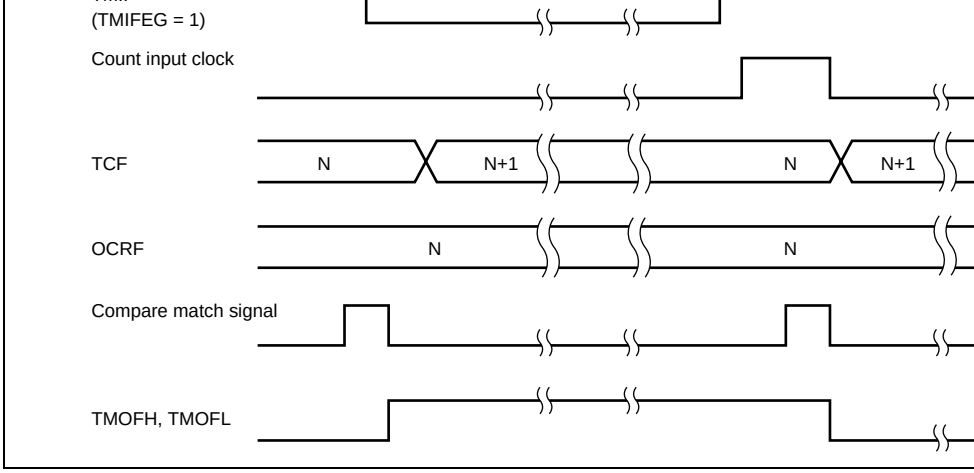


Figure 11.2 TMOFH/TMOFL Output Timing

11.4.4 TCF Clear Timing

TCF can be cleared by a compare match with OCRF.

11.4.5 Timer Overflow Flag (OVF) Set Timing

OVF is set to 1 when TCF overflows from H'FFFF to H'0000.

Table 11.2 Timer F Operating States

Operating Mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby
TCF	Reset	Functions*	Functions*	Functions/ Halted*	Functions/ Halted*	Functions/ Halted*	Halted
OCRF	Reset	Functions	Retained	Retained	Functions	Retained	Retained
TCRF	Reset	Functions	Retained	Retained	Functions	Retained	Retained
TCSRF	Reset	Functions	Retained	Retained	Functions	Retained	Retained

Note: * When ϕ_w/4 is selected as the TCF internal clock in active mode or sleep mode the system clock and internal clock are mutually asynchronous, synchronizati maintained by a synchronization circuit. This results in a maximum count cycl 1/ϕ (s). When the counter is operated in subactive mode, watch mode, or sub mode, ϕ_w /4 must be selected as the internal clock. The counter will not opera other internal clock is selected.

should be used as a port pin.

If an OCRFL write and compare match signal generation occur simultaneously, the comp
match signal is invalid. However, a compare match signal may or may not be generated v
written data and the counter value match. As the compare match signal is output in
synchronization with the TCFL clock, a compare match will not result in compare match
generation if the clock is stopped.

Compare match flag CMFH is set when all 16 bits match and a compare match signal is g
Compare match flag CMFL is set if the setting conditions for the lower 8 bits are satisfie

When TCF overflows, OVFH is set. OVFL is set if the setting conditions are satisfied wh
lower 8 bits overflow. If a TCFL write and overflow signal output occur simultaneously,
overflow signal is not output.

11.6.2 8-Bit Timer Mode

(1) TCFH, OCRFH

In toggle output, TMOFH pin output is toggled when a compare match occurs. If a TCRF
a MOV instruction and generation of the compare match signal occur simultaneously, TC
is output to the TMOFH pin as a result of the TCRF write.

If an OCRFH write and compare match signal generation occur simultaneously, the comp
match signal is invalid. However, a compare match signal may or may not be generated v
written data and the counter value match. The compare match signal is output in synchro
with the TCFH clock.

If a TCFH write and overflow signal output occur simultaneously, the overflow signal is
output.

If a TCFL write and overflow signal output occur simultaneously, the overflow signal is output.

11.6.3 Flag Clearing

When $\phi_w/4$ is selected as the internal clock, "Interrupt source generation signal" will be with ϕ_w and the signal will be outputted with ϕ_w width. And, "Overflow signal" and "Co match signal" are controlled with 2 cycles of ϕ_w signals. Those signals are output with 2 width of ϕ_w (figure 11.3)

In active (high-speed, medium-speed) mode, even if you cleared interrupt request flag d term of validity of "Interrupt source generation signal", same interrupt request flag is set figure 11.3) And, the timer overflow flag and compare match flag cannot be cleared dur term of validity of "Overflow signal" and "Compare match signal".

For interrupt request flag is set right after interrupt request is cleared, interrupt process t timer FH, timer FL interrupt might be repeated. (2 in figure 11.3) Therefore, to definitel interrupt request flag in active (high-speed, medium-speed) mode, clear should be proce the time that calculated with below (1) formula. And, to definitely clear timer overflow compare match flag, clear should be processed after read timer control status register F (after the time that calculated with below (1) formula.

For ST of (1) formula, please substitute the longest number of execution states in used i

In subactive mode, there are not limitation for interrupt request flag, timer overflow flag compare match flag clear.

2. After program process returned normal handling, clear interrupt request flags (IR IRRTFL) after more than that calculated with (1) formula.
3. After reading the timer control status register F (TCSRF), clear the timer overflo (OVFH, OVFL) and compare match flags (CMFH, CMFL).
4. Enable interrupts (set IENFH, IENFL to 1).

Method 2

1. Set interrupt handling routine time to more than time that calculated with (1) for
2. Clear interrupt request flags (IRRTFH, IRRTFL) at the end of interrupt handling
3. After read timer control status register F (TCSRF), clear timer overflow flags (C OVFL) and compare match flags (CMFH, CMFL).

All above attentions are also applied in 16-bit mode and 8-bit mode.

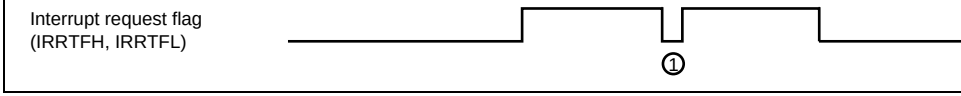


Figure 11.3 Clear Interrupt Request Flag when Interrupt Source Generation Signal is Valid

11.6.4 Timer Counter (TCF) Read/Write

When $\phi_w/4$ is selected as the internal clock in active (high-speed, medium-speed) mode, TCF is impossible. And when reading TCF, as the system clock and internal clock are m asynchronous, TCF synchronizes with synchronization circuit. This results in a maximu read value error of ±1.

When reading or writing TCF in active (high-speed, medium-speed) mode is needed, pl the internal clock except for $\phi_w/4$ before read/write is performed.

In subactive mode, even if ϕ_w /4 is selected as the internal clock, TCF can be read from to normally.

- The following operations can be set for each channel:
  Waveform output at compare match
  Input capture function
  Counter clear operation
  Multiple timer counters (TCNT) can be written to simultaneously
  Simultaneous clearing by compare match and input capture is possible
  Register synchronous input/output is possible by synchronous counter operation
  PWM output with any duty level is possible
  A maximum 2-phase PWM output is possible in combination with synchronous oper
- Operation with cascaded connection
- Fast access via internal 16-bit bus
- 6-type interrupt sources
- Register data can be transmitted automatically
- Use of module standby mode enables this module to be placed in standby mode inde
  when not used. (For details, refer to section 6.4, Module Standby Function.)

			TCLKC
General registers (TGR)		TGRA_1 TGRB_1	TGRA_2 TGRB_2
I/O pin		TIOCA1	TIOCA2
Input pin		TIOCB1	TIOCB2
Counter clear function		TGR compare match or input capture	TGR compare match or capture
Compare match output	0 output	O	—
	1 output	O	—
	Toggle output	O	—
Input capture function		O	O
Synchronous operation		O	O
PWM mode		O	O
Interrupt sources		3 sources • Compare match or input capture 1A • Compare match or input capture 1B • Overflow	3 sources • Compare match or input capture 2A • Compare match or input capture 2B • Overflow

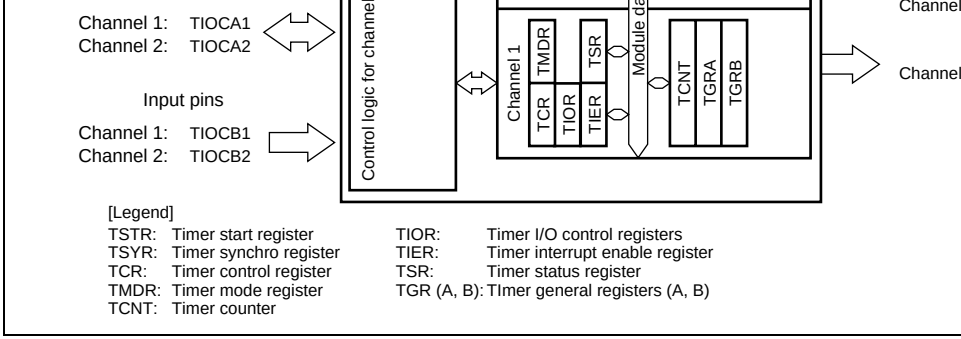


Figure 12.1 Block Diagram of TPU

12.2 Input/Output Pins

Table 12.2 Pin Configuration

Channel	Symbol	I/O	Function
Common	TCLKA	Input	External clock A input pin
	TCLKB	Input	External clock B input pin
	TCLKC	Input	External clock C input pin
1	TIOCA1	I/O	TGRA_1 input capture input/output co output/PWM output pin
	TIOCB1	Input	TGRB_1 input capture input pin
2	TIOCA2	I/O	TGRA_2 input capture input/output co output/PWM output pin
	TIOCB2	Input	TGRB_2 input capture input pin

- Timer status register_1 (TSR_1)
- Timer counter_1 (TCNT_1)
- Timer general register A_1 (TGRA_1)
- Timer general register B_1 (TGRB_1)

Channel 2:

- Timer control register_2 (TCR_2)
- Timer mode register_2 (TMDR_2)
- Timer I/O control register_2 (TIOR_2)
- Timer interrupt enable register_2 (TIER_2)
- Timer status register_2 (TSR_2)
- Timer counter_2 (TCNT_2)
- Timer general register A_2 (TGRA_2)
- Timer general register B_2 (TGRB_2)

Common:

- Timer start register (TSTR)
- Timer synchro register (TSYR)

5	CCLR0	0	R/W	These bits select the TCNT counter clearing s See table 12.3 for details.
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge. When internal clock is counted using both edges, th clock period is halved (e.g. ϕ/4 both edges = c edge). Internal clock edge selection is valid w input clock is ϕ/4 or slower. If the input clock i setting is ignored and count at a rising edge is 00: Count at rising edge 01: Count at falling edge 1X: Count at both edges [Legend] X: Don't care
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT counter clock. Th source can be selected independently for eac See tables12.4 and 12.5 for details.
0	TPSC0	0	R/W	

Table 12.4 TPSC2 to TPSC0 (Channel 1)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
1	0	0	0	Internal clock: counts on ϕ/1
			1	Internal clock: counts on ϕ/4
		1	0	Internal clock: counts on ϕ/16
			1	Internal clock: counts on ϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	Internal clock: counts on ϕ/256
			1	Counts on TCNT_2 overflow

1	0	External clock: counts on TCLKC pin input	
	1	Internal clock: counts on ϕ/1024	

12.3.2 Timer Mode Register (TMDR)

TMDR sets the operating mode for each channel. The TPU has a total of two TMDR reg
for each channel. TMDR should be set when TCNT operation is stopped.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved These bits are always read as 1 and cannot b modified.
5, 4	—	All 0	—	Reserved These bits are always read as 0 and cannot b modified.
3, 2	—	All 0	—	Reserved The write value should always be 0.
1	MD1	0	R/W	Modes 1 and 0
0	MD0	0	R/W	These bits set the timer operating mode. See table 12.6 for details.

TIOR controls TGR. The TPU has a total of two TIOR registers, one for each channel. Ca
required as TIOR is affected by the TMDR setting.

The initial output specified by TIOR is valid when the counter is stopped (the CST bit in
cleared to 0). Note also that, in PWM mode 2, the output at the point at which the counter
cleared to 0 is specified.

- TIOR_1, TIOR_2

Bit	Bit Name	Initial Value	R/W	Description
7	IOB3	All 0	R/W	I/O Control B3 to B0
6	IOB2		R/W	Specify the function of TGRB.
5	IOB1		R/W	For details, refer to tables 12.7 and 12.8.
4	IOB0		R/W	
3	IOA3	All 0	R/W	I/O Control A3 to A0
2	IOA2		R/W	Specify the function of TGRA.
1	IOA1		R/W	For details, refer to tables 12.9 and 12.10.
0	IOA0		R/W	

			1		
		1	0		
			1		
1	0	0	0	Input capture register	Capture input source is TIOCB Input capture at rising edge
			1		Capture input source is TIOCB Input capture at falling edge
		1	X		Capture input source is TIOCB Input capture at both edges
	1	X	X		Setting prohibited

[Legend]

X: Don't care

			1		
		1	0		
			1		
1	X	0	0	Input capture register	Capture input source is TIOCB2 Input capture at rising edge
			1		Capture input source is TIOCB2 Input capture at falling edge
		1	X		Capture input source is TIOCB2 Input capture at both edges

[Legend]

X: Don't care

			1		Initial output is 0
					Toggle output at compare matc
	1	0	0		Output disabled
			1		Initial output is 1
					0 output at compare match
		1	0		Initial output is 1
					1 output at compare match
			1		Initial output is 1
					Toggle output at compare matc
1	0	0	0	Input capture register	Capture input source is TIOCA1
					Input capture at rising edge
			1		Capture input source is TIOCA1
					Input capture at falling edge
		1	X		Capture input source is TIOCA1
					Input capture at both edges
	1	X	X		Setting prohibited

[Legend]

X: Don't care

			1		Initial output is 0
					Toggle output at compare matc
	1	0	0		Output disabled
			1		Initial output is 1
					0 output at compare match
		1	0		Initial output is 1
					1 output at compare match
			1		Initial output is 1
					Toggle output at compare matc
1	X	0	0	Input capture register	Capture input source is TIOCA2
					Input capture at rising edge
			1		Capture input source is TIOCA2
					Input capture at falling edge
		1	X		Capture input source is TIOCA2
					Input capture at both edges

[Legend]
X: Don't care

				This bit is always read as 1 and cannot be mo
5	—	0	—	Reserved The write value should always be 0.
4	TCIEV	0	R/W	Overflow Interrupt Enable Enables or disables interrupt requests (TCIV) TCFV flag when the TCFV flag in TSR is set t 0: Interrupt requests (TCIV) by TCFV disable 1: Interrupt requests (TCIV) by TCFV enable
3, 2	—	All 0	—	Reserved These bits are always read as 0 and cannot b modified.
1	TGIEB	0	R/W	TGR Interrupt Enable B Enables or disables interrupt requests (TGIB) TGFB bit when the TGFB bit in TSR is set to 0: Interrupt requests (TGIB) by TGFB bit disa 1: Interrupt requests (TGIB) by TGFB bit enab
0	TGIEA	0	R/W	TGR Interrupt Enable A Enables or disables interrupt requests (TGIA) TGFA bit when the TGFA bit in TSR is set to 0: Interrupt requests (TGIA) by TGFA bit disa 1: Interrupt requests (TGIA) by TGFA bit enab

				This bit is always read as 0 and cannot be modif
4	TCFV	0	R/(W)*	Overflow Flag Status flag that indicates that TCNT overflow has occurred. [Setting condition] When the TCNT value overflows (changes from to H'0000) [Clearing condition] When 0 is written to TCFV after reading TCFV =
3, 2	—	All 0	—	Reserved These bits are always read as 0 and cannot be r
1	TGFB	0	R/(W)*	Input Capture/Output Compare Flag B Status flag that indicates the occurrence of TGR capture or compare match. [Setting conditions] • When TCNT = TGRB and TGRB is functionir output compare register • When TCNT value is transferred to TGRB by capture signal and TGRB is functioning as in capture register [Clearing condition] • When 0 is written to TGFB after reading TGF

capture register

[Clearing condition]

- When 0 is written to TGFA after reading TG

Note: * Only 0 can be written to clear the flag.

12.3.6 Timer Counter (TCNT)

TCNT is a 16-bit readable/writable counter. The TPU has a total of two TCNT counters each channel.

TCNT is initialized to H'0000 by a reset or in hardware standby mode.

TCNT cannot be accessed in 8-bit units; it must always be accessed in 16-bit units.

12.3.7 Timer General Register (TGR)

TGR is a 16-bit readable/writable register, functioning as either output compare or input register. The TPU has a total of four TGR registers, two for each channel. TGR is initial H'FFFF by a reset. TGR cannot be accessed in 8-bit units; it must always be accessed in units.

2	CST2	0	R/W	Counter Start 2 and 1
1	CST1	0	R/W	These bits select operation or stoppage for TCN If 0 is written to the CST bit during operation with TIOC pin designated for output, the counter stop output compare output level of the TIOC pin is re TIOR is written to when the CST bit is cleared to pin output level will be changed to the set initial value. 0: TCNT_n count operation is stopped 1: TCNT_n performs count operation
				(r
0	—	0	—	Reserved The write value should always be 0.

1	SYNC1	0	R/W	These bits select whether operation is indepe synchronized with other channels. When synchronous operation is selected, the synchronous presetting of multiple channels, a synchronous clearing by counter clearing on a channel, are possible. To set synchronous operation, the SYNC bits set to 1. To set synchronous clearing, in addit SYNC bit, the TCNT clearing source must als means of bits CCLR1 and CCLR0 in TCR. 0: TCNT_n operates independently (TCNT p clearing is unrelated to other channels) 1: TCNT_n performs synchronous operation TCNT synchronous presetting/synchronou is possible
0	—	0	—	Reserved The write value should always be 0.

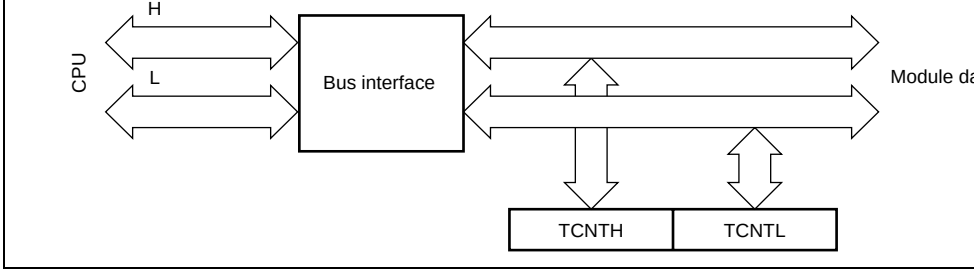


Figure 12.2 16-Bit Register Access Operation [CPU ↔ TCNT (16 Bits)]

12.4.2 8-Bit Registers

Registers other than TCNT and TGR are 8-bit. They can also be read and written to in 8-b

Examples of 8-bit register access operation are shown in figures 12.3 and 12.4.

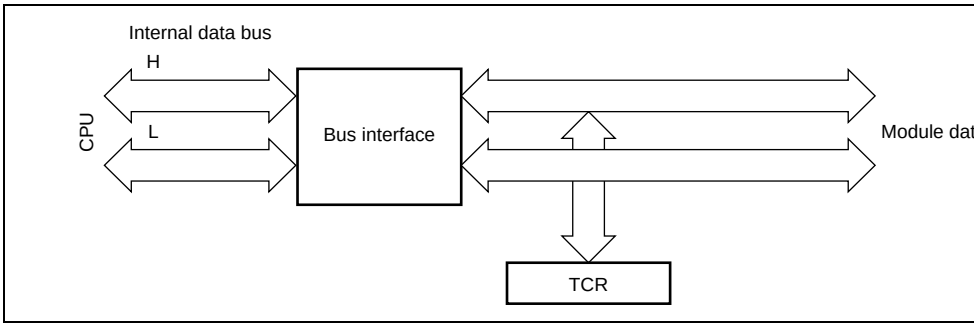


Figure 12.3 8-Bit Register Access Operation [CPU ↔ TCR (Upper 8 Bits)]

When one of bits CST1 and CST2 is set to 1 in TSTR, TCNT for the corresponding chan
begins counting. TCNT can operate as a free-running counter, periodic counter, for exam

(a) Example of Count Operation Setting Procedure

Figure 12.5 shows an example of the count operation setting procedure.

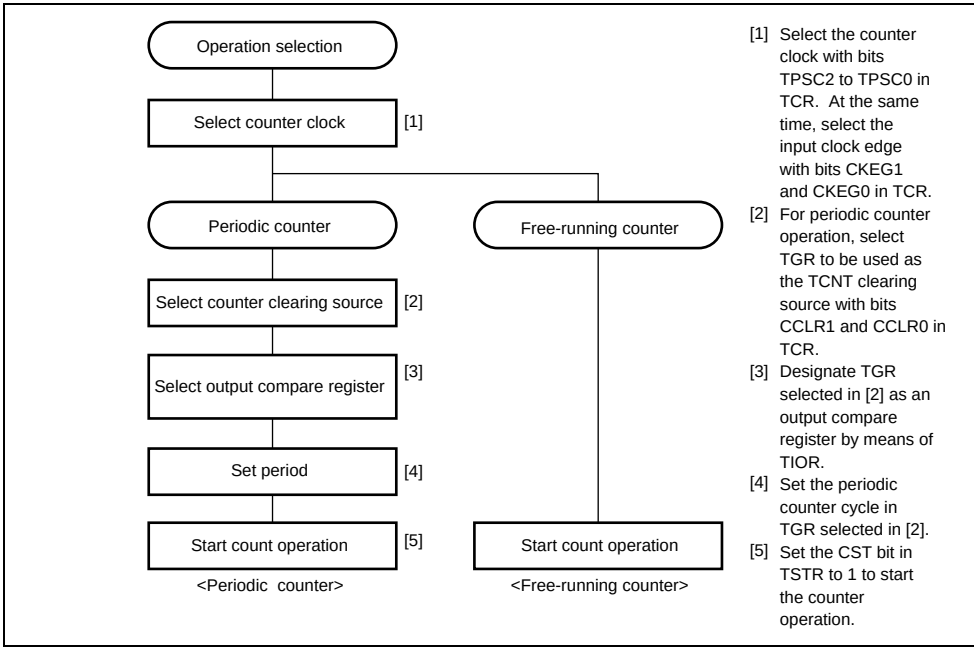


Figure 12.5 Example of Counter Operation Setting Procedure

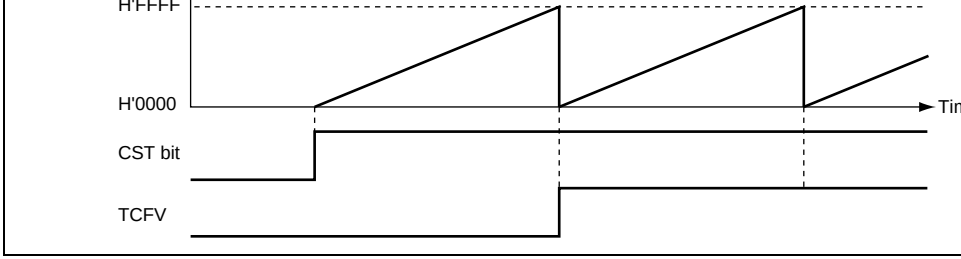


Figure 12.6 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, TCNT for the relevant ch performs periodic count operation. TGR for setting the period is designated as an output register, and counter clearing by compare match is selected by means of bits CCLR0 and in TCR. After the settings have been made, TCNT starts up-count operation as a periodi when the corresponding bit in TSTR is set to 1. When the count value matches the value the TGF bit in TSR is set to 1 and TCNT is cleared to H'0000.

If the value of the corresponding TGIE bit in TIER is 1 at this point, the TPU requests an After a compare match, TCNT starts counting up again from H'0000.

Figure 12.7 illustrates periodic counter operation.

(2) Waveform Output by Compare Match

The TPU can perform 0, 1, or toggle output from the corresponding output pin using com
match.

(a) Example of Setting Procedure for Waveform Output by Compare Match

Figure 12.8 shows an example of the setting procedure for waveform output by compare

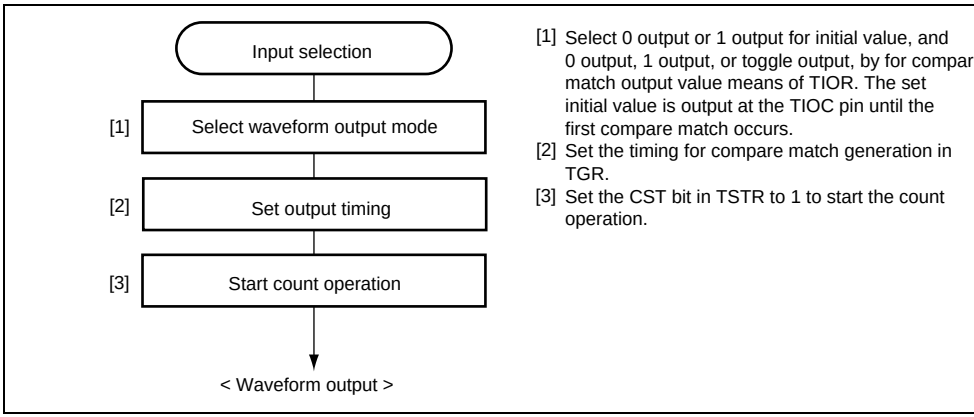


Figure 12.8 Example of Setting Procedure for Waveform Output by Compare M

(b) Examples of Waveform Output Operation

Figure 12.9 shows an example of 1 output.

In this example, TCNT has been designated as a free-running counter, and settings have b
made such that 1 is output by compare match A. When the set level and the pin level mat
pin level does not change.

Figure 12.10 shows an example of toggle output.

In this example, TCNT has been designated as a periodic counter (with counter clearing
compare match A), and settings have been made such that the output is toggled by comp
A.

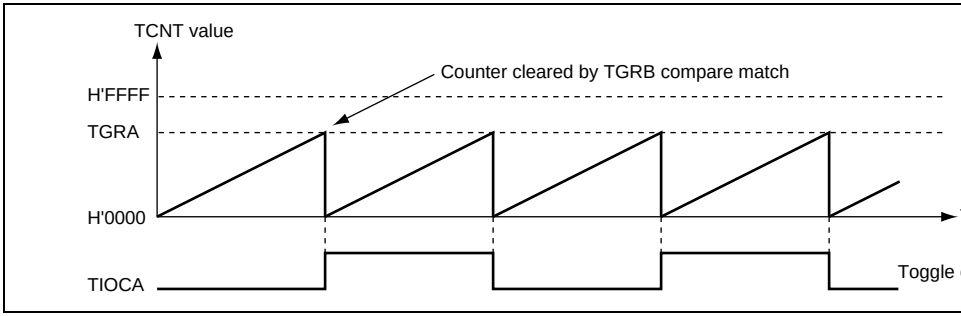


Figure 12.10 Example of Toggle Output Operation

(3) Input Capture Function

The TCNT value can be transferred to TGR on detection of the TIOC pin input edge.

Rising edge, falling edge, or both edges can be selected as the detected edge.

(a) Example of Input Capture Operation Setting Procedure

Figure 12.11 shows an example of the setting procedure for input capture operation.

(b) Example of Input Capture Operation

Figure 12.12 shows an example of input capture operation.

In this example, both rising and falling edges have been selected as the input capture inpu
the TIOCA pin, the falling edge has been selected as the input capture input edge of the T
pin, and counter clearing by TGRB input capture has been designated for TCNT.

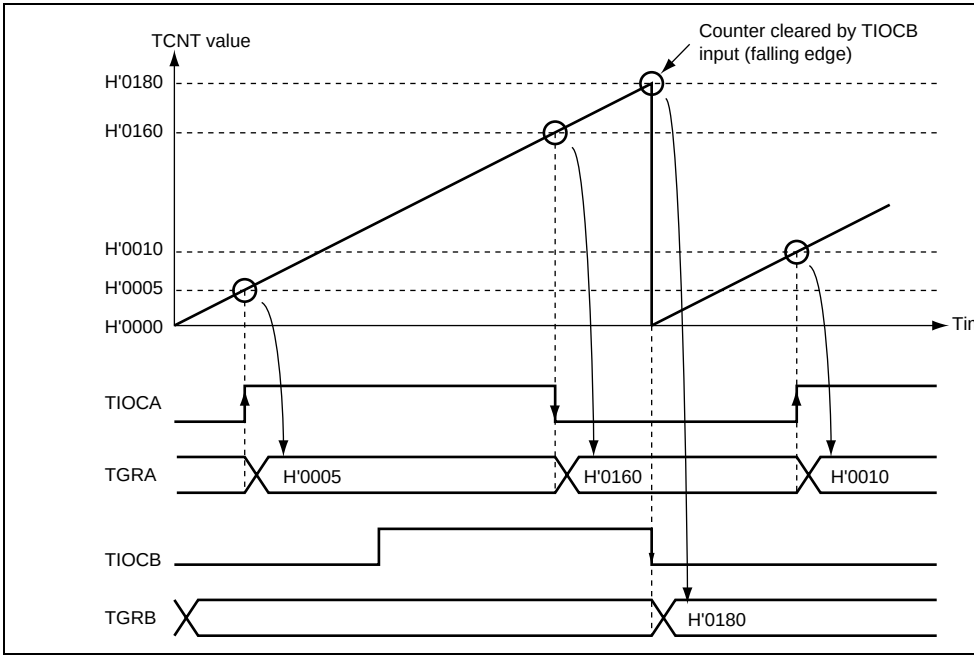
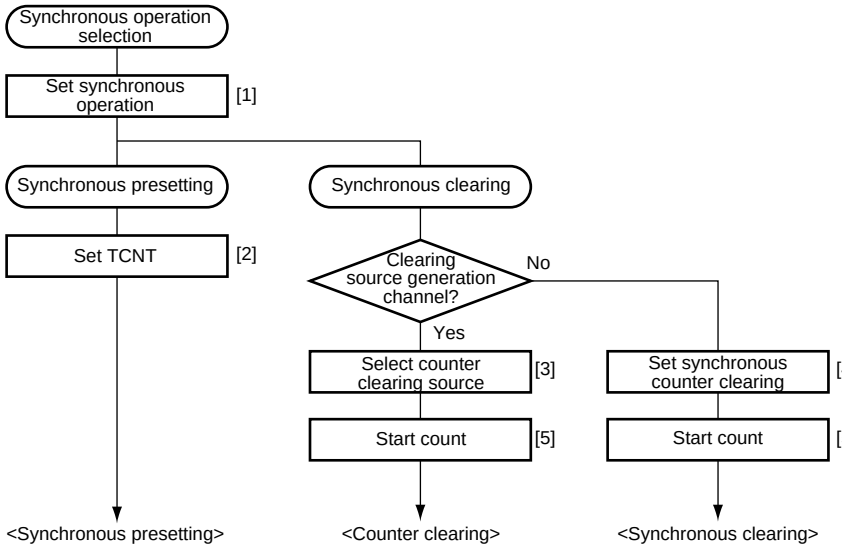


Figure 12.12 Example of Input Capture Operation

Figure 12.13 shows an example of the synchronous operation setting procedure.



[1] Set 1 to the SYNC bits in TSYR corresponding to the channels to be designated for synchronous operation.
[2] When the TCNT counter of any of the channels designated for synchronous operation is written to, the same value is simultaneously written to the other TCNT counters.
[3] Use bits CCLR1 and CCLR0 in TCR to specify TCNT clearing by input capture/output compare, etc.
[4] Use bits CCLR1 and CCLR0 in TCR to designate synchronous clearing for the counter clearing source.
[5] Set 1 to the CST bits in TSTR for the relevant channels, to start the count operation.

Figure 12.13 Example of Synchronous Operation Setting Procedure

For details on PWM modes, see section 12.5.4, PWM Modes.

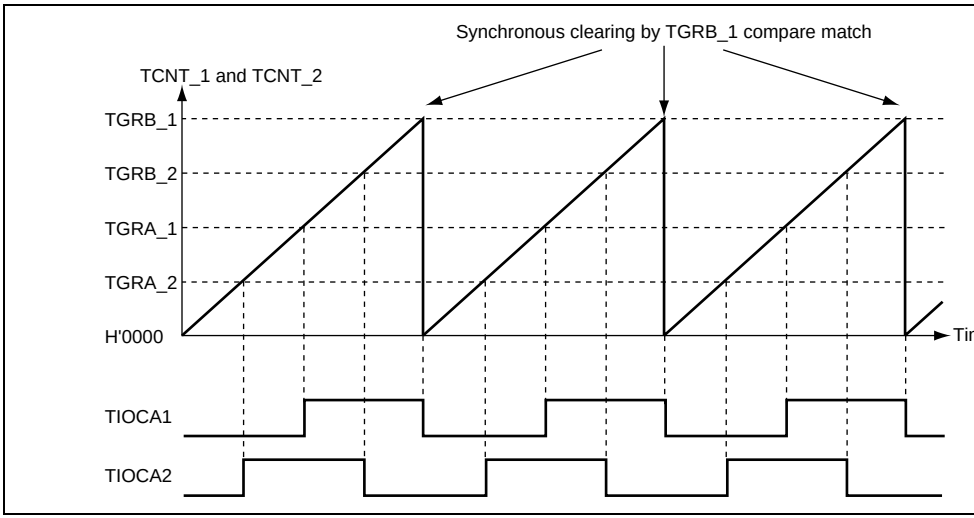


Figure 12.14 Example of Synchronous Operation

Combination	Upper 16 bits	Lower 16 bits
Channel 1 and channel 2	TCNT1	TCNT2

(1) Setting Procedure for Operation with Cascaded Connection

Figure 12.15 shows the setting procedure for cascaded connection operation.

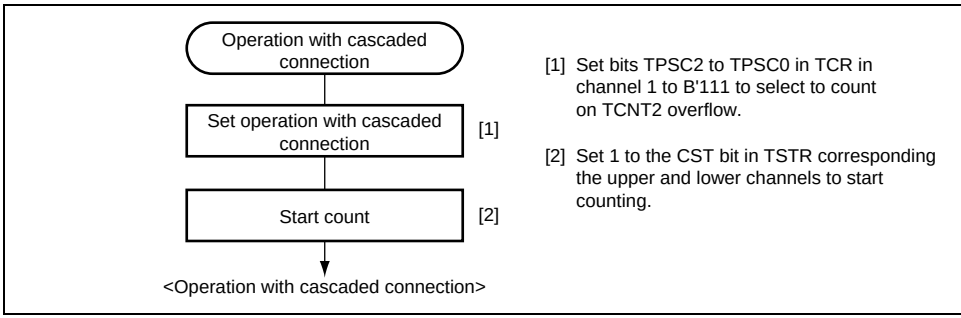


Figure 12.15 Setting Procedure for Operation with Cascaded Operation

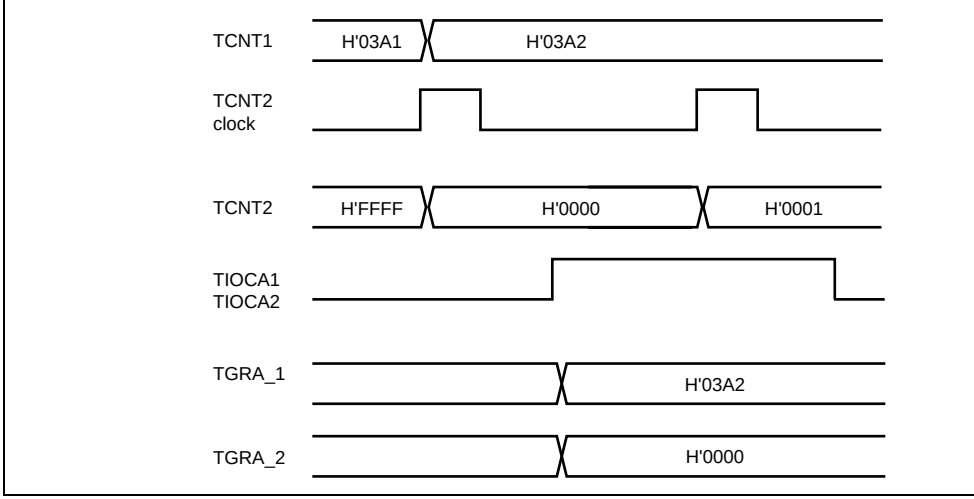


Figure 12.16 Example of Operation with Cascaded Connection

(1) PWM Mode 1

PWM output is generated from the TIOCA pin by pairing TGRA with TGRB. The level by bits IOA0 to IOA3 in TIOR is output from the TIOCA pin at compare match A, and specified by bits IOB0 to IOB3 in TIOR is output at compare match B. The initial outpu the value set in TGRA. If the set values of paired TGRs are identical, the output value d change even if a compare match occurs.

In PWM mode 1, PWM output is enabled up to 2 phases.

(2) PWM Mode 2

PWM output is generated using one TGR as the cycle register and the others as duty reg output specified in TIOR is performed by means of compare matches. Upon counter cle synchronization register compare match, the output value of each pin is the initial value TIOR. If the set values of the cycle and duty registers are identical, the output value doe change even if a compare match occurs.

In PWM mode 2, PWM output is enabled up to 2 phases.

The correspondence between PWM output pins and registers is shown in table 12.12.

(3) Example of PWM Mode Setting Procedure

Figure 12.17 shows an example of the PWM mode setting procedure.

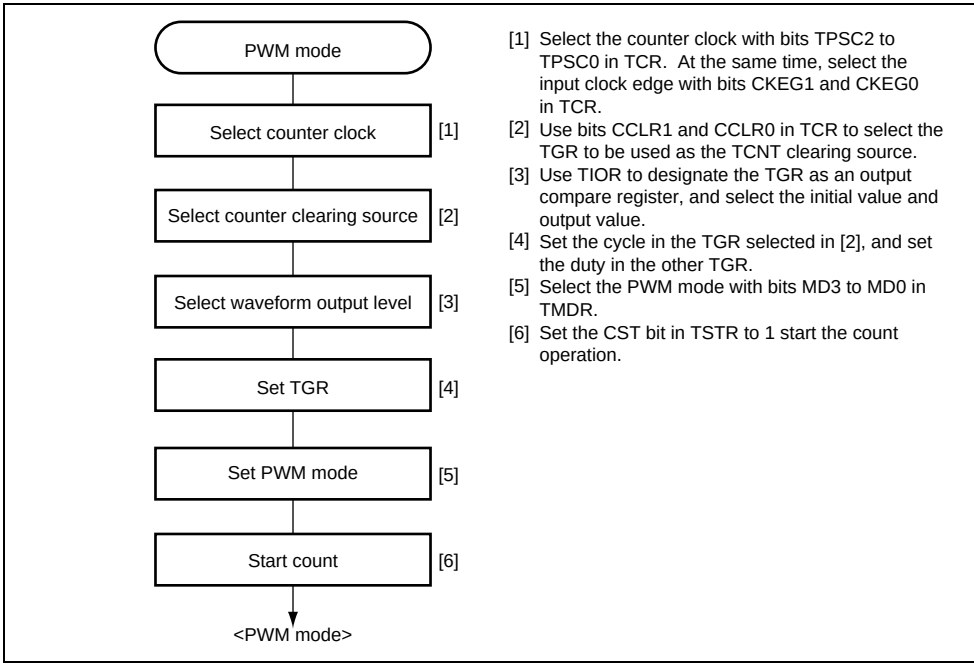


Figure 12.17 Example of PWM Mode Setting Procedure

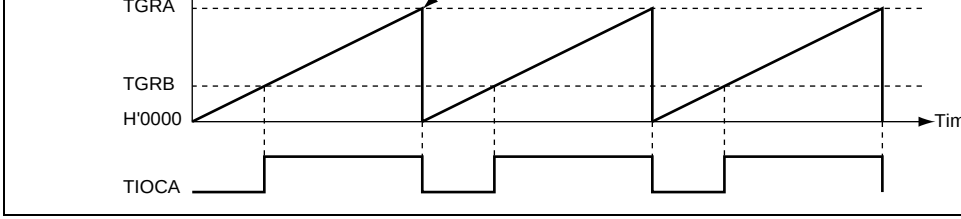


Figure 12.18 Example of PWM Mode Operation (1)

Figure 12.19 shows an example of PWM mode 2 operation. In this example, synchronou operation is designated for channels 1 and 2, TGRB_2 compare match is set as the TCN source, and 0 is set for the initial output value and 1 for the output value of the other TG (TGRA_1, TGRB_1, and TGRA_2), outputting a 2-phase PWM waveform.

In this case, the value set in TGRB_2 is used as the cycle, and the values set in the other used as the duty levels.

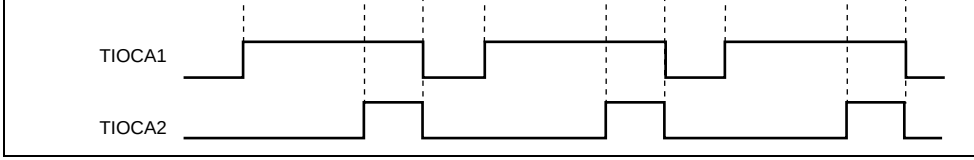


Figure 12.19 Example of PWM Mode Operation (2)

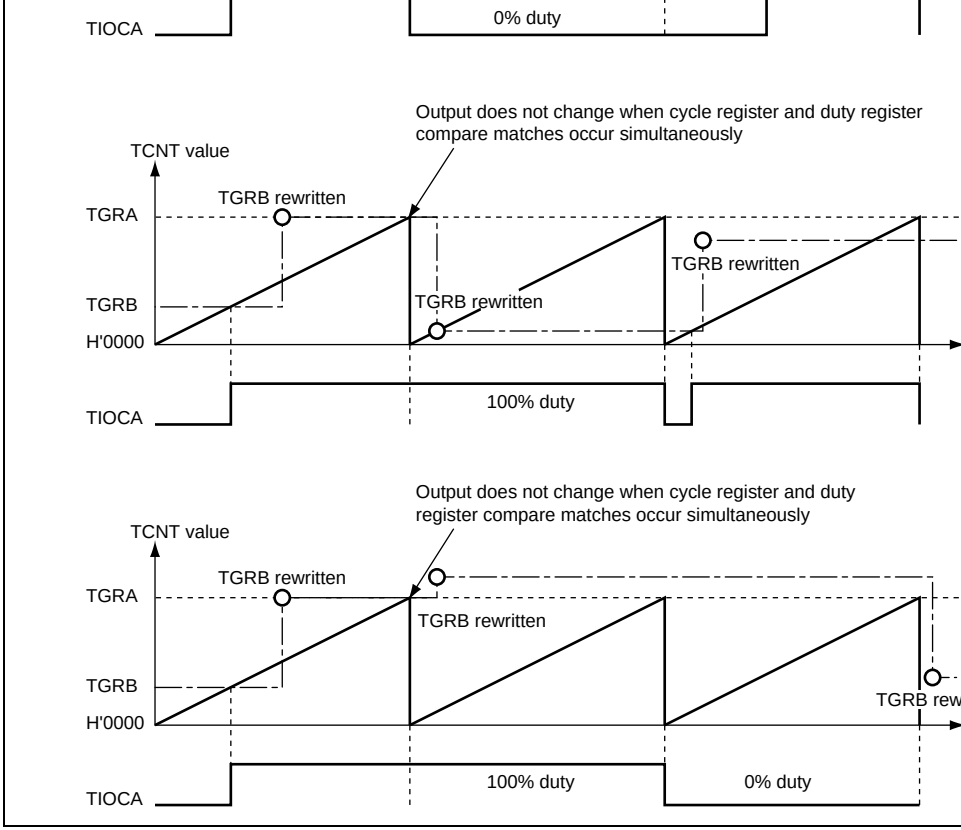


Figure 12.20 Example of PWM Mode Operation (3)

is fixed. For details, see section 4, Interrupt Controller.

Table 12.13 lists the TPU interrupt sources.

Table 12.13 TPU Interrupts

Channel	Name	Interrupt Source	Interrupt Flag	Priority
1	TGI1A	TGRA_1 input capture/compare match	TGFA_1	High
	TGI1B	TGRB_1 input capture/compare match	TGFB_1	
	TCI1V	TCNT_1 overflow	TCFV_1	
2	TGI2A	TGRA_2 input capture/compare match	TGFA_2	
	TGI2B	TGRB_2 input capture/compare match	TGFB_2	
	TCI2V	TCNT_2 overflow	TCFV_2	Low

(1) Input Capture/Compare Match Interrupt

An interrupt is requested if the TGIE bit in TIER is set to 1 when the TGF flag in TSR is by the occurrence of a TGR input capture/compare match on a particular channel. The int request is cleared by clearing the TGF flag to 0. The TPU has a total of four input capture match interrupts, two for each channel.

(2) Overflow Interrupt

An interrupt is requested if the TCIEV bit in TIER is set to 1 when the TCFV flag in TSR 1 by the occurrence of TCNT overflow on a channel. The interrupt request is cleared by c the TCFV flag to 0. The TPU has a total of two overflow interrupts, one for each channel

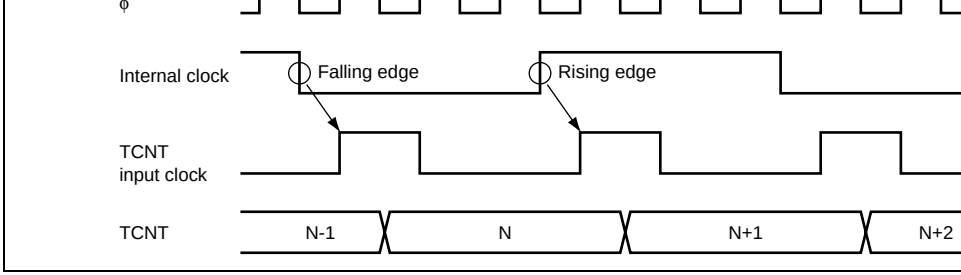


Figure 12.21 Count Timing in Internal Clock Operation

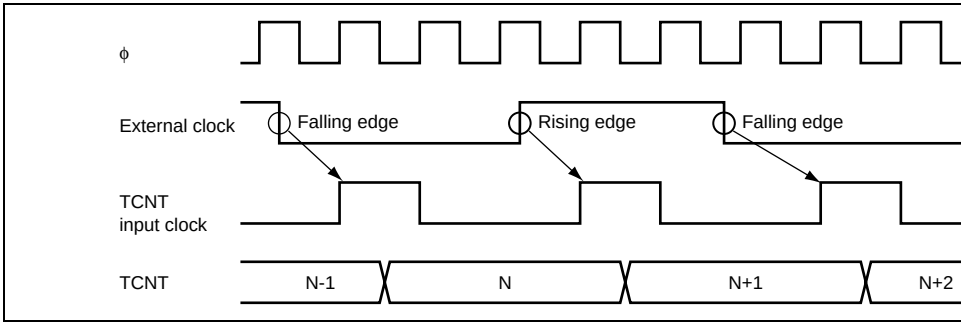


Figure 12.22 Count Timing in External Clock Operation

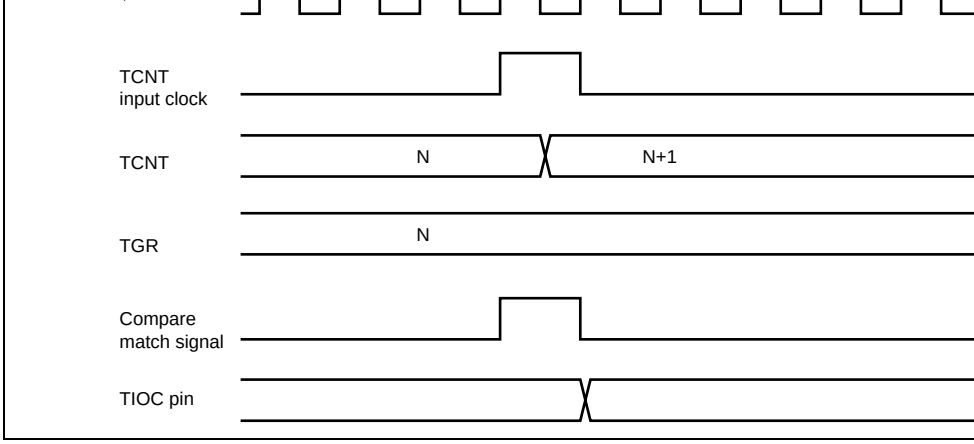


Figure 12.23 Output Compare Output Timing

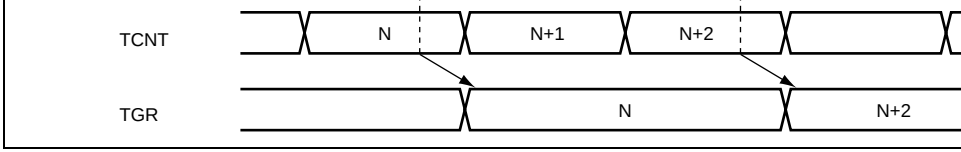


Figure 12.24 Input Capture Input Signal Timing

(4) Timing for Counter Clearing by Compare Match/Input Capture

Figure 12.25 shows the timing when counter clearing on compare match is specified, an
12.26 shows the timing when counter clearing on input capture is specified.

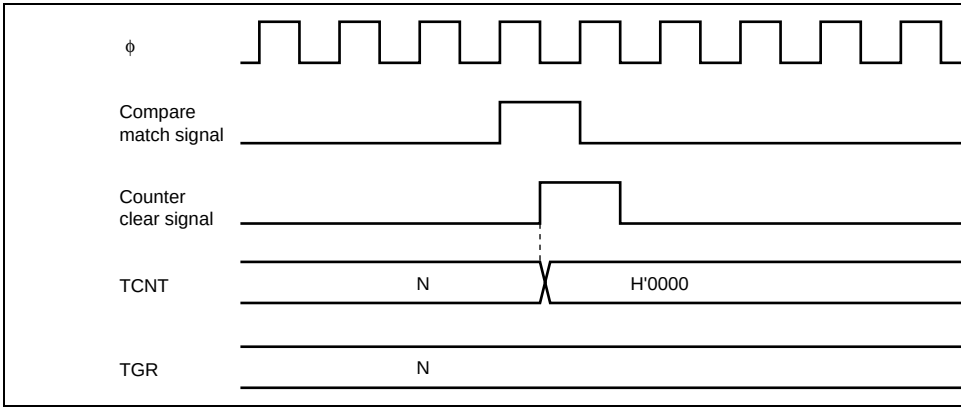


Figure 12.25 Counter Clear Timing (Compare Match)

Figure 12.26 Counter Clear Timing (Input Capture)

12.7.2 Interrupt Signal Timing

(1) TGF Flag Setting Timing in Case of Compare Match

Figure 12.27 shows the timing for setting of the TGF flag in TSR on compare match, and interrupt request signal timing.

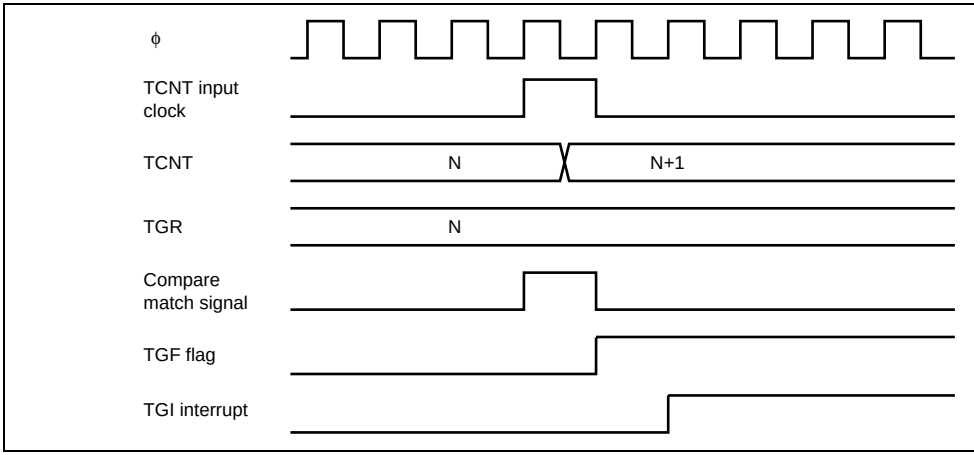


Figure 12.27 TGI Interrupt Timing (Compare Match)

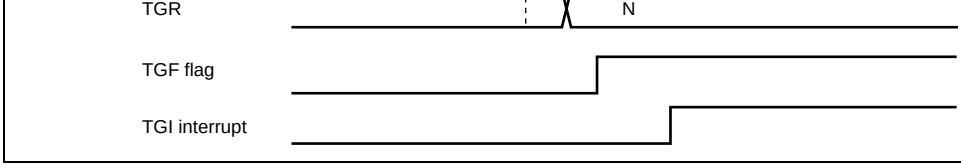


Figure 12.28 TGI Interrupt Timing (Input Capture)

(3) TCFV Flag Setting Timing

Figure 12.29 shows the timing for setting of the TCFV flag in TSR on overflow, and TC
interrupt request signal timing.

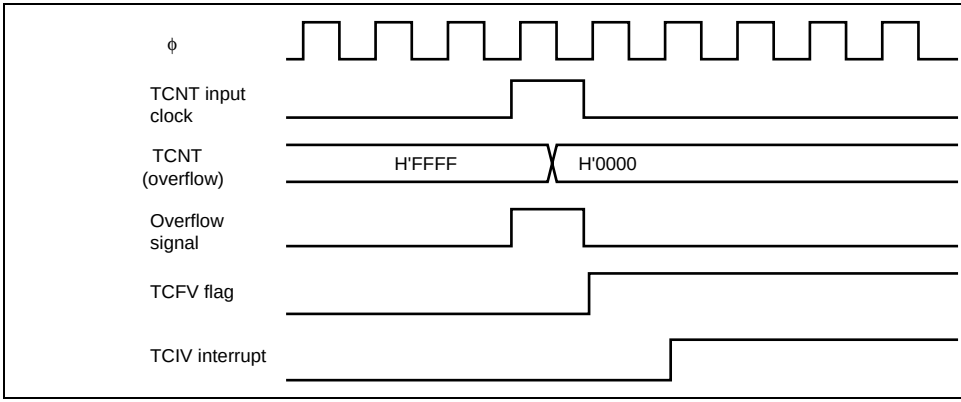


Figure 12.29 TCIV Interrupt Setting Timing

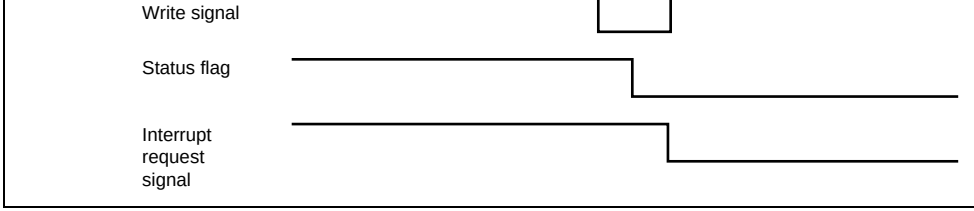


Figure 12.30 Timing for Status Flag Clearing by CPU

12.8 Usage Notes

12.8.1 Module Standby Function Setting

TPU operation can be disabled or enabled using the clock stop register. The initial setting
the TPU to operate. Register access is enabled by clearing the module standby function. F
details, refer to section 6.4, Module Standby Function.

12.8.2 Input Clock Restrictions

The input clock pulse width must be at least 1.5 states in the case of single-edge detection
least 2.5 states in the case of both-edge detection. The TPU will not operate properly at n
pulse widths.

N: TGR set value

12.8.4 Contention between TCNT Write and Clear Operation

If the counter clear signal is generated in the T2 state of a TCNT write cycle, TCNT clea
priority and the TCNT write is not performed.

Figure 12.31 shows the timing in this case.

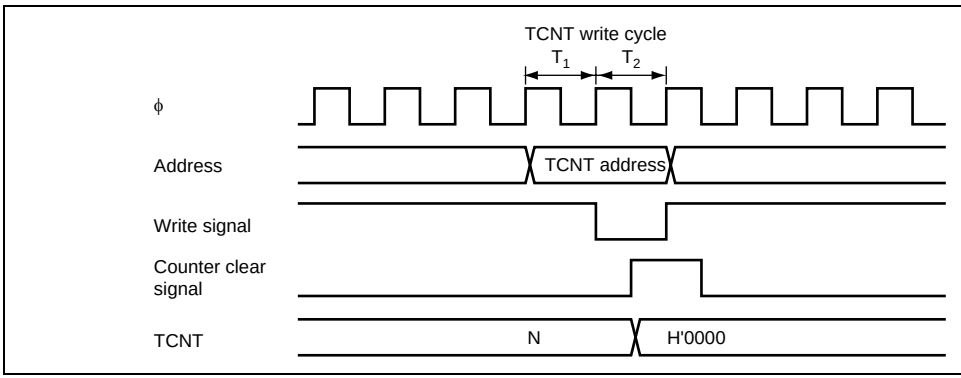


Figure 12.31 Contention between TCNT Write and Clear Operation

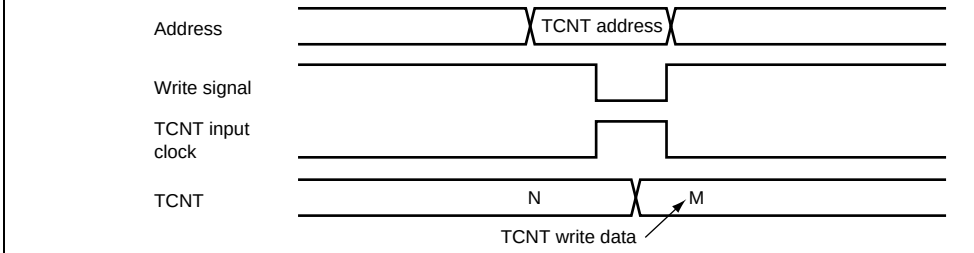


Figure 12.32 Contention between TCNT Write and Increment Operation

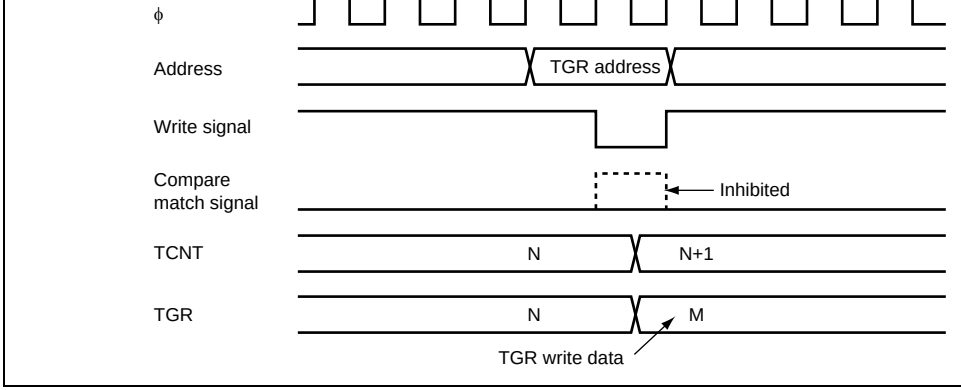


Figure 12.33 Contention between TGR Write and Compare Match

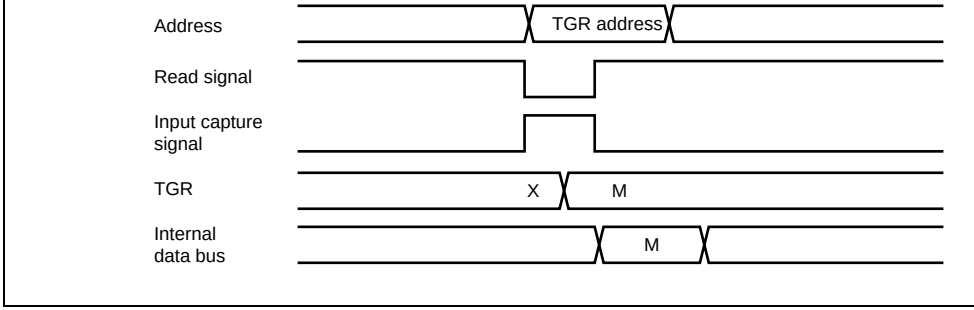


Figure 12.34 Contention between TGR Read and Input Capture

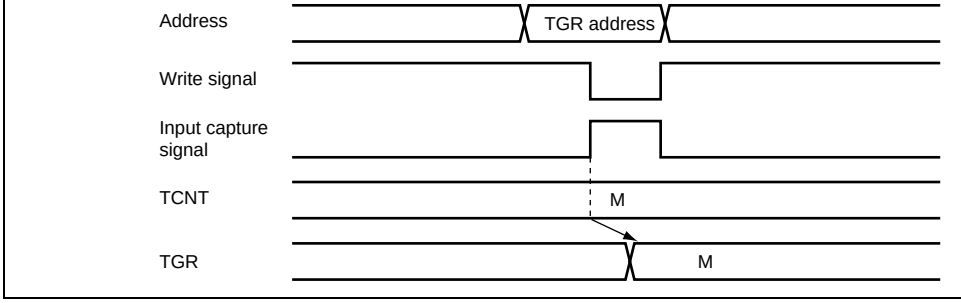


Figure 12.35 Contention between TGR Write and Input Capture

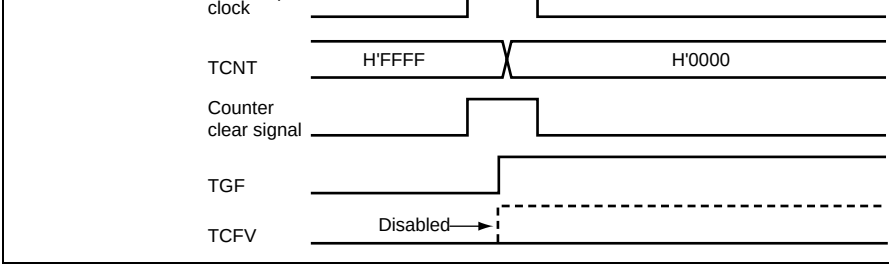


Figure 12.36 Contention between Overflow and Counter Clearing

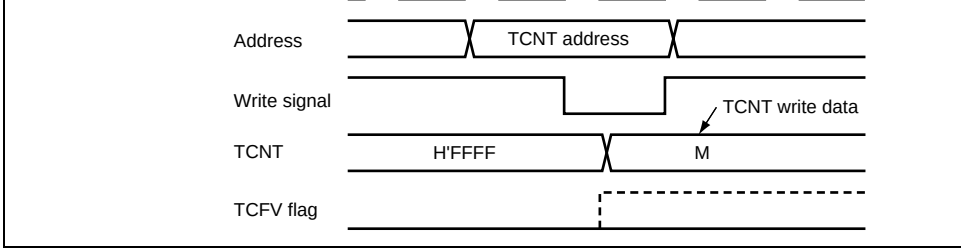


Figure 12.37 Contention between TCNT Write and Overflow

12.8.11 Multiplexing of I/O Pins

The TIOCA1 I/O pin is multiplexed with the TCLKA input pin, the TIOCB1 I/O pin wi
TCLKB input pin, and the TIOCA2 I/O pin with the TCLKC input pin. When an externa
input, compare match output should not be performed from a multiplexed pin.

12.8.12 Interrupts when Module Standby Function is Used

If the module standby function is used when an interrupt has been requested, it will not
to clear the CPU interrupt source. Interrupts should therefore be disabled before using th
standby function.

clocks (ϕ) or subclocks (ϕ_{SUB}).

- Can be used as two-channel independent 8-bit event counter or single-channel indep bit event counter.
- Event/clock input is enabled when IRQAEC goes high or event counter PWM outpu (IECPWM) goes high.
- Both edge sensing can be used for IRQAEC or event counter PWM output (IECPWM interrupts. When the asynchronous counter is not used, they can be used as independ interrupts.
- When an event counter PWM is used, event clock input enabling/disabling can be co a constant cycle.
- Selection of four clock sources

  Three internal clocks ($\phi/2$, $\phi/4$, or $\phi/8$) or external event can be selected.
- Both edge counting is possible for the AEVL and AEVH pins.
- Counter resetting and halting of the count-up function can be controlled by software
- Automatic interrupt generation on detection of an event counter overflow
- Use of module standby mode enables this module to be placed in standby mode inde when not used. (For details, refer to section 6.4, Module Standby Function.)
- The IRQAEC pin can select the on-chip oscillator and the system clock oscillator du reset, though this function does not apply to a reset by the watchdog timer. (Supporte the masked ROM version.)

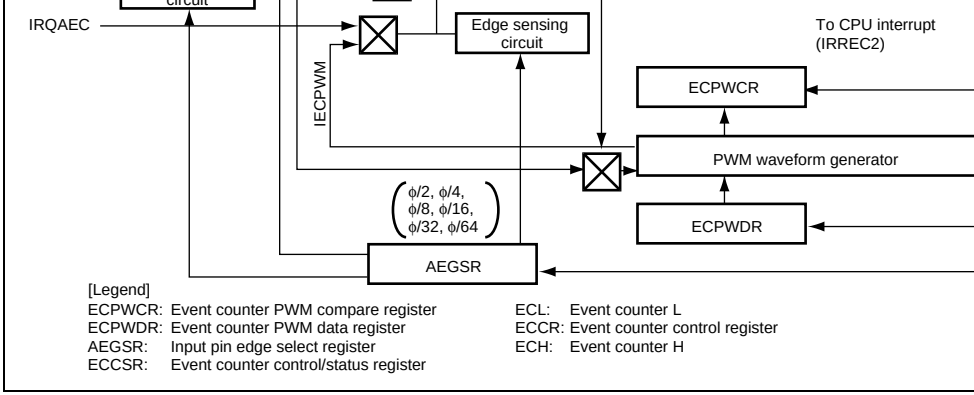


Figure 13.1 Block Diagram of Asynchronous Event Counter

13.2 Input/Output Pins

Table 13.1 shows the pin configuration of the asynchronous event counter.

Table 13.1 Pin Configuration

Name	Abbreviation	I/O	Function
Asynchronous event input H	AEVH	Input	Event input pin for input to event counte
Asynchronous event input L	AEVL	Input	Event input pin for input to event counte
Event input enable interrupt input	IRQAEC	Input	Input pin for interrupt enabling event inp Input pin to select the on-chip oscillator system clock oscillator (supported only masked ROM version)

- Event counter L (ECL)

13.3.1 Event Counter PWM Compare Register (ECPWCR)

ECPWCR sets the one conversion period of the event counter PWM waveform.

Always read or write to this register in word size.

Bit	Bit Name	Initial Value	R/W	Description
15	ECPWCR15	1	R/W	One Conversion Period of Event Counter PW Waveform When the ECPWME bit in AEGSR is 1, the ev counter PWM is operating and therefore ECP should not be modified. When changing the conversion period, the ev counter PWM must be halted by clearing the bit in AEGSR to 0 before modifying ECPWCR
14	ECPWCR14	1	R/W	
13	ECPWCR13	1	R/W	
12	ECPWCR12	1	R/W	
11	ECPWCR11	1	R/W	
10	ECPWCR10	1	R/W	
9	ECPWCR9	1	R/W	
8	ECPWCR8	1	R/W	
7	ECPWCR7	1	R/W	
6	ECPWCR6	1	R/W	
5	ECPWCR5	1	R/W	
4	ECPWCR4	1	R/W	
3	ECPWCR3	1	R/W	
2	ECPWCR2	1	R/W	
1	ECPWCR1	1	R/W	
0	ECPWCR0	1	R/W	

13	ECPWDR13	0	W	counter PWM is operating and therefore ECPW
12	ECPWDR12	0	W	should not be modified.
11	ECPWDR11	0	W	When changing the conversion cycle, the even
10	ECPWDR10	0	W	PWM must be halted by clearing the ECPWME
9	ECPWDR9	0	W	AEGSR to 0 before modifying ECPWDR.
8	ECPWDR8	0	W	
7	ECPWDR7	0	W	
6	ECPWDR6	0	W	
5	ECPWDR5	0	W	
4	ECPWDR4	0	W	
3	ECPWDR3	0	W	
2	ECPWDR2	0	W	
1	ECPWDR1	0	W	
0	ECPWDR0	0	W	

				01: Rising edge on AEVH pin is sensed 10: Both edges on AEVH pin are sensed 11: Setting prohibited
5	ALEGS1	0	R/W	AEC Edge Select L
4	ALEGS0	0	R/W	Select rising, falling, or both edge sensing for t pin. 00: Falling edge on AEVL pin is sensed 01: Rising edge on AEVL pin is sensed 10: Both edges on AEVL pin are sensed 11: Setting prohibited
3	AIEGS1	0	R/W	IRQAEC Edge Select
2	AIEGS0	0	R/W	Select rising, falling, or both edge sensing for IRQAEC pin. 00: Falling edge on IRQAEC pin is sensed 01: Rising edge on IRQAEC pin is sensed 10: Both edges on IRQAEC pin are sensed 11: Setting prohibited
1	ECPWME	0	R/W	Event Counter PWM Enable Controls operation of event counter PWM and of IRQAEC. 0: AEC PWM halted, IRQAEC selected 1: AEC PWM enabled, IRQAEC not selected
0	—	0	R/W	Reserved This bit can be read from or written to. Howev should not be set to 1.

				10: ϕ/4
				11: ϕ/8
5	ACKL1	0	R/W	AEC Clock Select L
4	ACKL0	0	R/W	Select the clock used by ECL.
				00: AEVL pin input
				01: ϕ/2
				10: ϕ/4
				11: ϕ/8
3	PWCK2	0	R/W	Event Counter PWM Clock Select
2	PWCK1	0	R/W	Select the event counter PWM clock.
1	PWCK0	0	R/W	000: ϕ/2
				001: ϕ/4
				010: ϕ/8
				011: ϕ/16
				1X0: ϕ/32
				1X1 ϕ/64
0	—	0	R/W	Reserved
				This bit can be read from or written to. Howeve should not be set to 1.

[Legend] X: Don't care.

				[Clearing condition] When this bit is written to 0 after reading OVH
6	OVL	0	R/W*	Counter Overflow L This is a status flag indicating that ECL has ov [Setting condition] When ECL overflows from H'FF to H'00 while to 1 [Clearing condition] When this bit is written to 0 after reading OVL
5	—	0	R/W	Reserved Although this bit is readable/writable, it should set to 1.
4	CH2	0	R/W	Channel Select Selects how ECH and ECL event counters are 0: ECH and ECL are used together as a single 16-bit event counter 1: ECH and ECL are used as two-channel 8-b counter
3	CUEH	0	R/W	Count-Up Enable H Enables event clock input to ECH. 0: ECH event clock input is disabled (ECH val retained) 1: ECH event clock input is enabled

				1: ECH reset is cleared and count-up function i enabled
0	CRCL	0	R/W	Counter Reset Control L Controls resetting of ECL. 0: ECL is reset 1: ECL reset is cleared and count-up function is

Note: * Only 0 can be written to clear the flag.

5	ECH5	0	R	ECH can be cleared to H'00 by clearing CRCH
4	ECH4	0	R	ESSCR to 0.
3	ECH3	0	R	
2	ECH2	0	R	
1	ECH1	0	R	
0	ECH0	0	R	

13.3.7 Event Counter L (ECL)

ECL is an 8-bit read-only up-counter that operates as an independent 8-bit event counter also operates as the upper 8-bit up-counter of a 16-bit event counter configured in comb with ECH.

Bit	Bit Name	Initial Value	R/W	Description
7	ECL7	0	R	Either the external asynchronous event AEVL
6	ECL6	0	R	$\phi/4$, or $\phi/8$ can be selected as the input clock s
5	ECL5	0	R	ECL can be cleared to H'00 by clearing CRCL to 0.
4	ECL4	0	R	
3	ECL3	0	R	
2	ECL2	0	R	
1	ECL1	0	R	
0	ECL0	0	R	

Note that the input clock is enabled when IRQAEC is high or IECPWM is high. When IR
low or IECPWM is low, the input clock is not input to the counter, which therefore does n
operate. Figure 13.2 shows the software procedure when ECH and ECL are used as a 16-
counter.

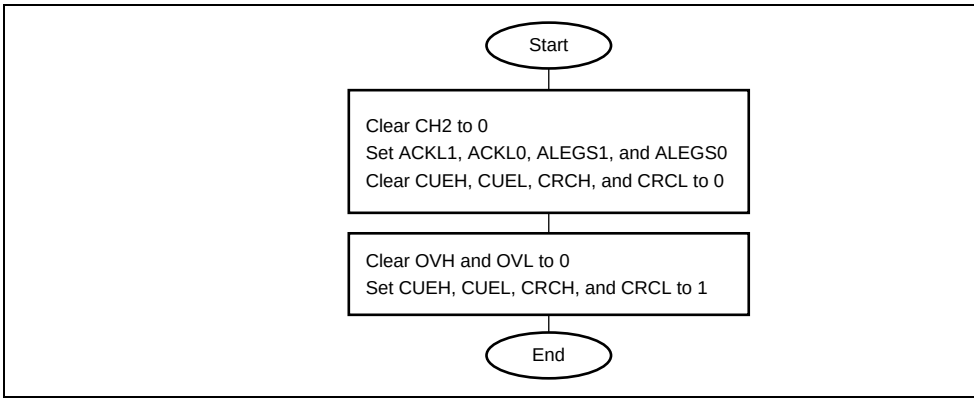


Figure 13.2 Software Procedure when Using ECH and ECL as 16-Bit Event Co

As CH2 is cleared to 0 by a reset, ECH and ECL operate as a 16-bit event counter after a
and as ACKL1 and ACKL0 are cleared to B'00, the operating clock is asynchronous even
from the AEVL pin (using falling edge sensing).

When the next clock is input after the count value reaches H'FF in both ECH and ECL, E
ECL overflow from H'FFFF to H'0000, the OVH flag is set to 1 in ECCSR, the ECH and
count values each return to H'00, and counting up is restarted. When an overflow occurs,
IRREC bit is set to 1 in IRR2. If the IENEC bit in IENR2 is 1 at this time, an interrupt re
sent to the CPU.

low or IECPWM is low, the input clock is not input to the counter, which therefore does
operate. Figure 13.3 shows the software procedure when ECH and ECL are used as 8-bi
counters.

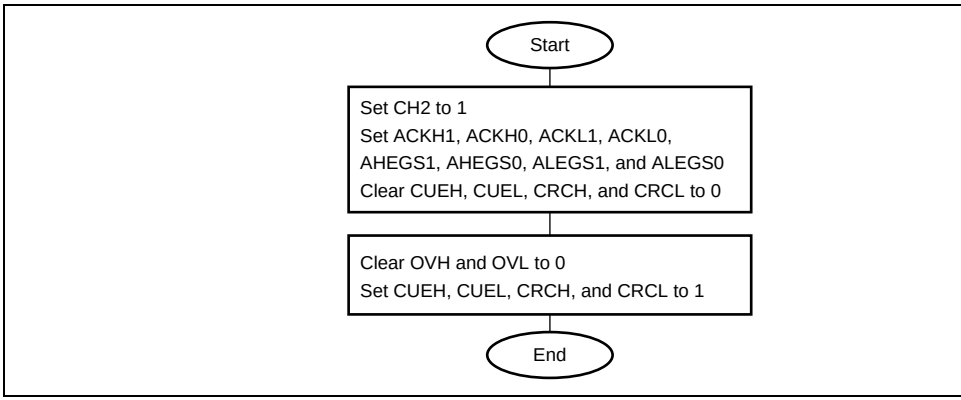


Figure 13.3 Software Procedure when Using ECH and ECL as 8-Bit Event Co

When the next clock is input after the ECH count value reaches H'FF, ECH overflows, t
flag is set to 1 in ECCSR, the ECH count value returns to H'00, and counting up is resta
Similarly, when the next clock is input after the ECL count value reaches H'FF, ECL ov
the OVL flag is set to 1 in ECCSR, the ECL count value returns to H'00, and counting u
restarted. When an overflow occurs, the IRREC bit is set to 1 in IRR2. If the IENEC bit
is 1 at this time, an interrupt request is sent to the CPU.

Rising, falling, or both edge sensing can be selected for the IRQAEC input pin with bits A
and AIAGS0 in AEGSR.

13.4.4 Event Counter PWM Operation

When the ECPWME bit in AEGSR is 1, the ECH and ECL input clocks are enabled whe
counter PWM output (IECPWM) is high. When IECPWM is low, the input clocks are no
the counters, and so ECH and ECL do not count. ECH and ECL count operations can the
controlled cyclically from outside by controlling event counter PWM. In this case, ECH a
cannot be controlled individually.

IECPWM can also operate as an interrupt source.

Interrupt enabling is controlled by IENEC2 in IENR1. When an IECPWM interrupt is ge
IRR1 interrupt request flag IRREC2 is set to 1. If IENEC2 in IENR1 is set to 1 at this tim
interrupt request is sent to the CPU.

Rising, falling, or both edge detection can be selected for IECPWM interrupt sensing wit
AIAGS1 and AIAGS0 in AEGSR.

Figure 13.4 and table 13.2 show examples of event counter PWM operation.

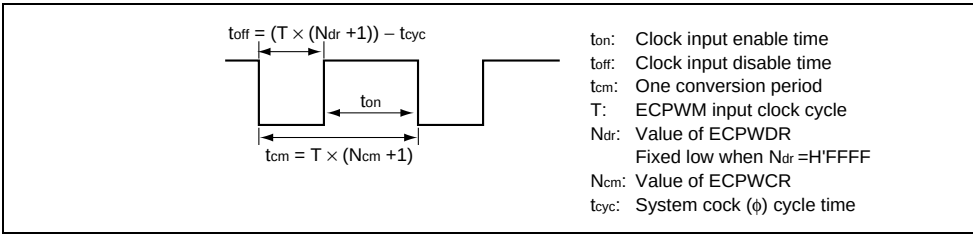


Figure 13.4 Event Counter Operation Waveform

ϕ/4	1 µs	D'31249	D'5859	5.85975 ms	31.25 ms	25.3
ϕ/8	2 µs			11.71975 ms	62.5 ms	50.7
ϕ/16	4 µs			23.43975 ms	125.0 ms	101.
ϕ/32	8 µs			46.87975 ms	250.0 ms	203.
ϕ/64	16 µs			93.75975 ms	500.0 ms	406.

Note: * toff minimum width

13.4.5 Operation of Clock Input Enable/Disable Function

The clock input to the event counter can be controlled by the IRQAEC pin when ECPW AEGSR is 0, and by the event counter PWM output, IECPWM when ECPWME in AEC As this function forcibly terminates the clock input by each signal, a maximum error of will occur depending on the IRQAEC or IECPWM timing. Figure 13.5 shows an examp operation.

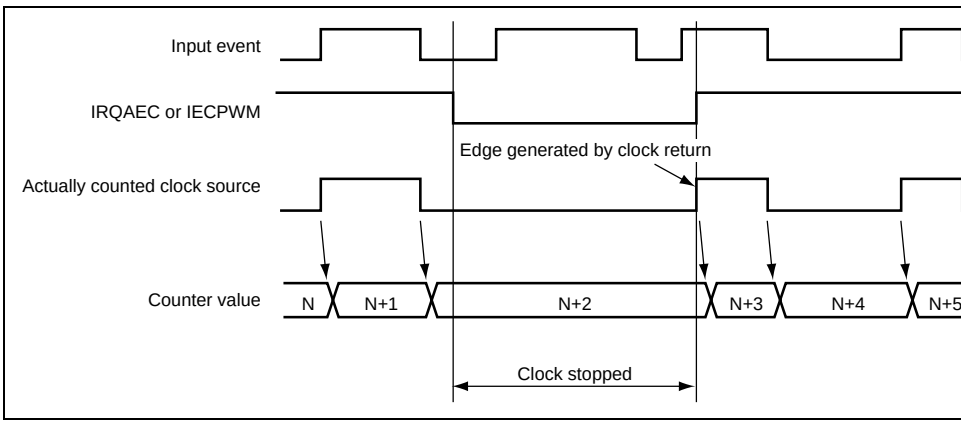


Figure 13.5 Example of Clock Control Operation

ECH	Reset	Functions	Functions	Functions*[1]*[2]	Functions*[2]	Functions*[2]	Functions*[1]*[2]
ECL	Reset	Functions	Functions	Functions*[1]*[2]	Functions[2]	Functions*[2]	Functions*[1]*[2]
IRQAEC	Reset	Functions	Functions	Retained*[3]	Functions	Functions	Retained*[3]
Event counter PWM	Reset	Functions	Functions	Retained	Retained	Retained	Retained

Notes: 1. When an asynchronous external event is input, the counter increments. Howev interrupt request is issued when the counter overflows.
2. Functions when asynchronous external events are selected; halted and retaine otherwise.
3. Clock control by IRQAEC operates, but interrupts do not.
4. As the clock is stopped in module standby mode, IRQAEC has no effect.

Table 13.4 shows a maximum clock frequency.

Table 13.4 Maximum Clock Frequency

Mode		Maximum Clock Freq Input to AEVH/AEVL
Active (high-speed), sleep (high-speed)		10 MHz
Active (medium-speed), sleep (medium-speed)	(ϕ_{osc}/8)	$2 \cdot f_{osc}$
	(ϕ_{osc}/16)	f_{osc}
	(ϕ_{osc}/32)	$1/2 \cdot f_{osc}$
	(ϕ_{osc}/64)	$1/4 \cdot f_{osc}$
Watch, subactive, subsleep, standby	(ϕ_w/2)	1000 kHz
	(ϕ_w/4)	500 kHz
ϕ_w = 32.768 kHz or 38.4 kHz	(ϕ_w/8)	250 kHz

3. When AEC uses with 16-bit mode, set CUEH in ECCSR to 1 first, set CRCH in EC second, or set both CUEH and CRCH to 1 at same time before clock input. When A operating on 16-bit mode, do not change CUEH. Otherwise, ECH will be miscounte
4. When ECPWME in AEGSR is 1, the event counter PWM is operating and therefore and ECPWDR should not be modified.

   When changing the data, clear the ECPWME bit in AEGSR to 0 (halt the event cour before modifying these registers.
5. The event counter PWM data register and event counter PWM compare register mus that event counter PWM data register < event counter PWM compare register. If the do not satisfy this condition, do not set ECPWME to 1 in AEGSR.

The WDT features are described below.

- Selectable from nine counter input clocks

  Eight internal clock sources (ϕ/64, ϕ/128, ϕ/256, ϕ/512, ϕ/1024, ϕ/2048, ϕ/4096, and or the WDT on-chip oscillator can be selected as the timer-counter clock.
- Watchdog timer mode

  If the counter overflows, this LSI is internally reset.
- Interval timer mode

  If the counter overflows, an interval timer interrupt is generated.
- Use of module standby mode enables this module to be placed in standby mode inde when not used. (For details, refer to section 6.4, Module Standby Function.)

Figure 14.1 shows a block diagram of the WDT.

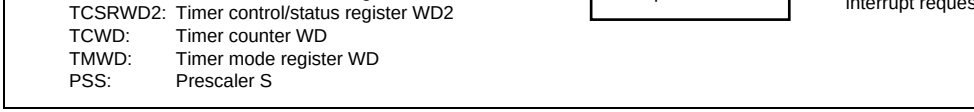


Figure 14.1 Block Diagram of Watchdog Timer

14.2 Register Descriptions

The watchdog timer has the following registers.

- Timer control/status register WD1 (TCSRWD1)
- Timer control/status register WD2 (TCSRWD2)
- Timer counter WD (TCWD)
- Timer mode register WD (TMWD)

				This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable TCWD can be written when the TCWE bit is s When writing data to this bit, the write value fo must be 0.
5	B4WI	1	R/W	Bit 4 Write Inhibit The TCSRWE bit can be written only when th value of the B4WI bit is 0. This bit is always re
4	TCSRWE	0	R/W	Timer Control/Status Register WD Write Enab The WDON and WRST bits can be written wh TCSRWE bit is set to 1. When writing data to this bit, the write value fo must be 0.
3	B2WI	1	R/W	Bit 2 Write Inhibit The WDON bit can be written only when the v of the B2WI bit is 0. This bit is always read as

				• When 0 is written to the WDON bit and 0 to B2WI bit while the TCSRWE bit is 1
1	B0WI	1	R/W	Bit 0 Write Inhibit The WRST bit can be written only when the wr of the B0WI bit is 0. This bit is always read as 1
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] When TCWD overflows and an internal reset s generated [Clearing conditions] • Reset by $\overline{\text{RES}}$ pin • When 0 is written to the WRST bit and 0 to B0WI bit while the TCSRWE bit is 1

Note: * When transitioning to the watch mode or standby mode while the main internal clo selected (CKS3 = 1) using timer mode register WD (TMWD), make sure to clear W 0 to halt operation of TCWD.

				[Setting condition] When TCWD overflows (changes from H'FF t When internal reset request generation is sel watchdog timer mode, this bit is cleared auto by the internal reset after it has been set. [Clearing condition] • When TCSRWD2 is read when OVF = 1, written to OVF*[4]
6	B5WI	1	R/(W)*[2]	Bit 5 Write Inhibit The WT/$\overline{IT}$ bit can be written only when the w of the B5WI bit is 0. This bit is always read as
5	WT/$\overline{IT}$	0	R/(W)*[3]	Timer Mode Select Selects whether the WDT is used as a watch or interval timer. 0: Watchdog timer mode 1: Interval timer mode
4	B3WI	1	R/(W)*[2]	Bit 3 Write Inhibit The IEOVF bit can be written only when the w of the B3WI bit is 0. This bit is always read as
3	IEOVF	0	R/(W)*[3]	Overflow Interrupt Enable Enables or disables an overflow interrupt requ interval timer mode. 0: Disables an overflow interrupt 1: Enables an overflow interrupt

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1.
3	CKS3	1	R/W	Clock Select 3 to 0
2	CKS2	1	R/W	Select the clock to be input to TCWD.
1	CKS1	1	R/W	1000: Internal clock: counts on φ/64
0	CKS0	1	R/W	1001: Internal clock: counts on φ/128 1010: Internal clock: counts on φ/256 1011: Internal clock: counts on φ/512 1100: Internal clock: counts on φ/1024 1101: Internal clock: counts on φ/2048 1110: Internal clock: counts on φ/4096 1111: Internal clock: counts on φ/8192 0XXX: WDT on-chip oscillator For the WDT on-chip oscillator overflow perio section 24, Electrical Characteristics. In active (medium-speed) mode or sleep (me speed) mode, the setting of B'0XXX and inter mode is disabled.

[Legend] X: Don't care.

reset signal is output for a period of 256 ϕ_{osc} clock cycles. TCWD is a writable counter, an value is set in TCWD, the count-up starts from that value. An overflow period in the rang 256 input clock cycles can therefore be set, according to the TCWD set value.

Figure 14.2 shows an example of watchdog timer operation.

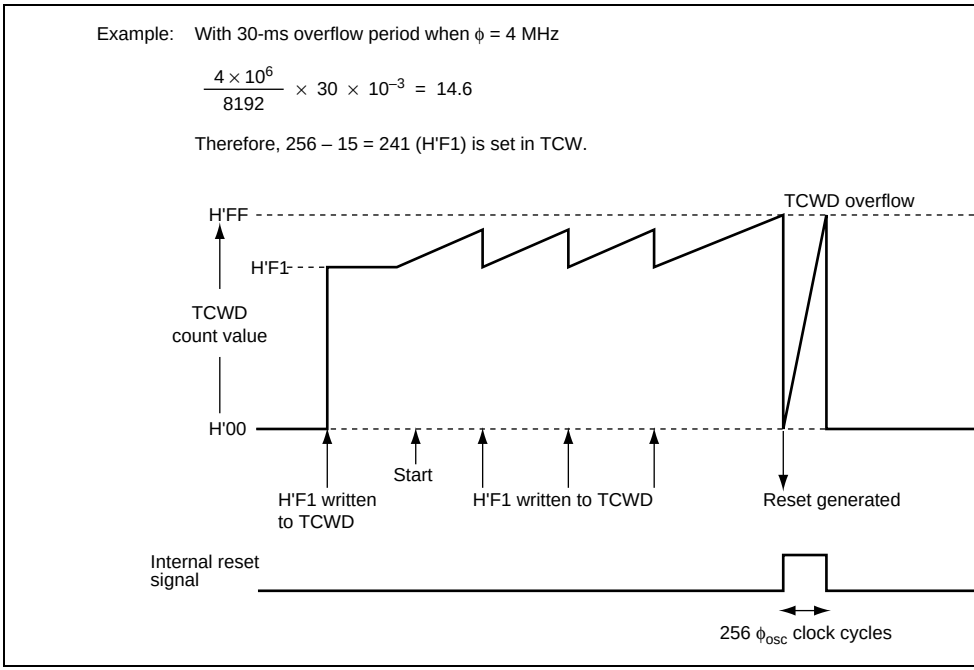


Figure 14.2 Example of Watchdog Timer Operation

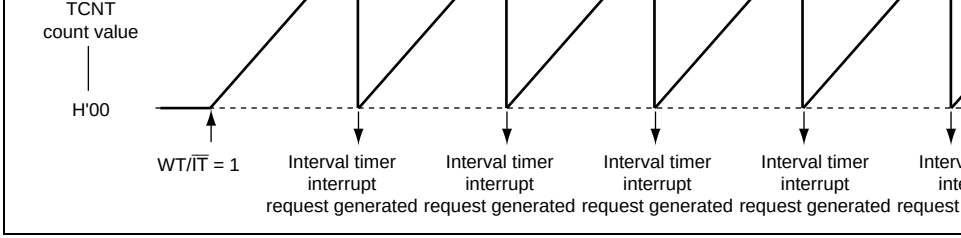


Figure 14.3 Interval Timer Mode Operation

14.3.3 Timing of Overflow Flag (OVF) Setting

Figure 14.4 shows the timing of the OVF flag setting. The OVF flag in TCSRWD2 is se
TCNT overflows. At the same time, a reset signal is output in watchdog timer mode and
interval timer interrupt is generated in interval timer mode.

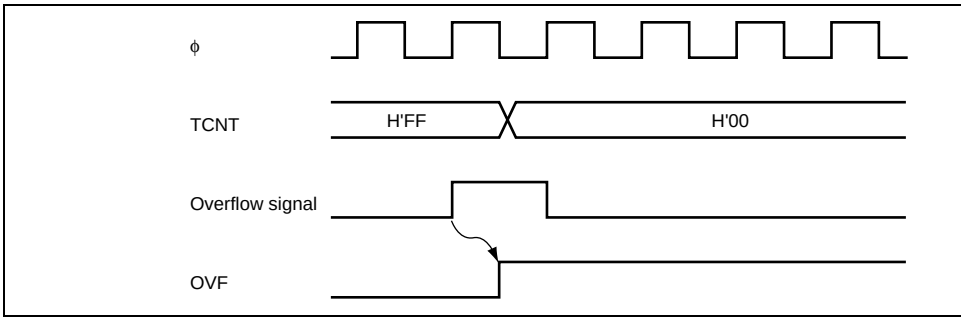


Figure 14.4 Timing of OVF Flag Setting

If the mode is switched between watchdog timer and interval timer, while the WDT is op
errors could occur in the incrementation. Software must stop the watchdog timer (by clea
WDON bit to 0) before switching the mode.

14.5.2 Module Standby Mode Control

The WDCKSTP bit in CKSTPR2 is valid when the WDON bit in the timer control/status
1 (TCSRWD1) is cleared to 0. The WDCKSTP bit can be cleared to 0 while the WDON
to 1 (while the watchdog timer is operating). However, the watchdog timer does not ente
standby mode but continues operating. When the WDON bit is cleared to 0 by software a
watchdog timer stops operating, the WDCKSTP bit is valid at the same time and the wato
timer enters module standby mode.

15.1 Features

- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability

  The transmitter and receiver are mutually independent, enabling transmission and re be executed simultaneously.

  Double-buffering is used in both the transmitter and the receiver, enabling continuou transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected
- On-chip baud rate generator, internal clock, or external clock can be selected as a tra clock source.
- Six interrupt sources

  Transmit-end, transmit-data-empty, receive-data-full, overrun error, framing error, a error.
- Use of module standby mode enables this module to be placed in standby mode inde when not used. (For details, refer to section 6.4, Module Standby Function.)

Asynchronous mode

- Data length: 7, 8, or 5 bits
- Stop bit length: 1 or 2 bits
- Parity: Even, odd, or none
- Receive error detection: Parity, overrun, and framing errors
- Break detection: Break can be detected by reading the RXD32 pin level directly in tl a framing error

Note: When using serial communication interface 3 in the masked ROM version, do n on-chip oscillator.

			TDR3_1	H'FF9B
			SSR3_1	H'FF9C
			RDR3_1	H'FF9D
			RSR3_1	—
			TSR3_1	—
			IrCR	H'FFA7
Channel 2	SCI3_2	SCK32	SMR3_2	H'FFA8
		RXD32	BRR3_2	H'FFA9
		TXD32	SCR3_2	H'FFAA
			TDR3_2	H'FFAB
			SSR3_2	H'FFAC
			RDR3_2	H'FFAD
			RSR3_2	—
			TSR3_2	—

Notes: 1. Pin names SCK3, RXD3, and TXD3 are used in the text for all channels, omitti channel designation.

2. In the text, channel description is omitted for registers and bits.

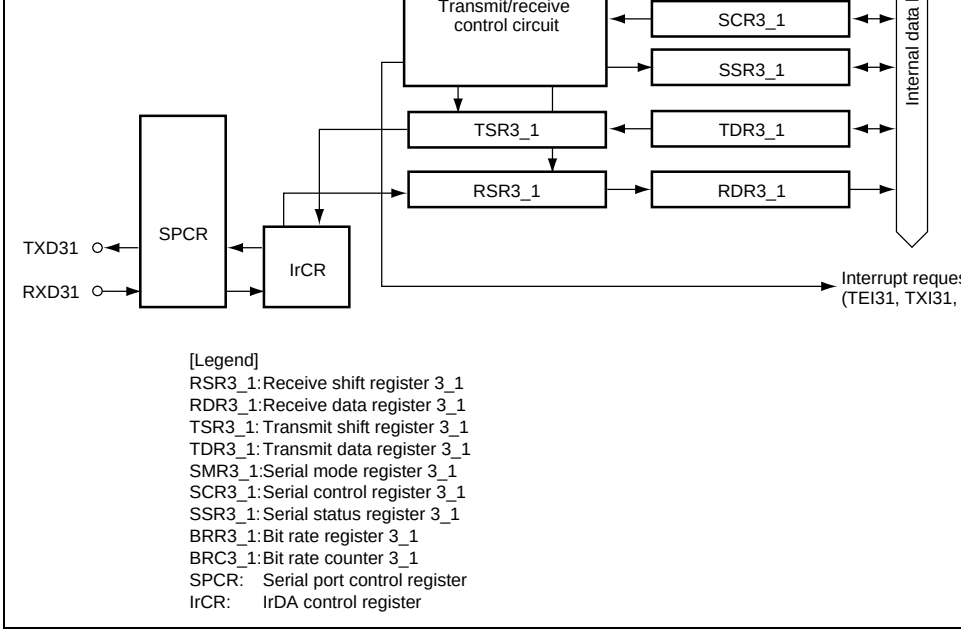
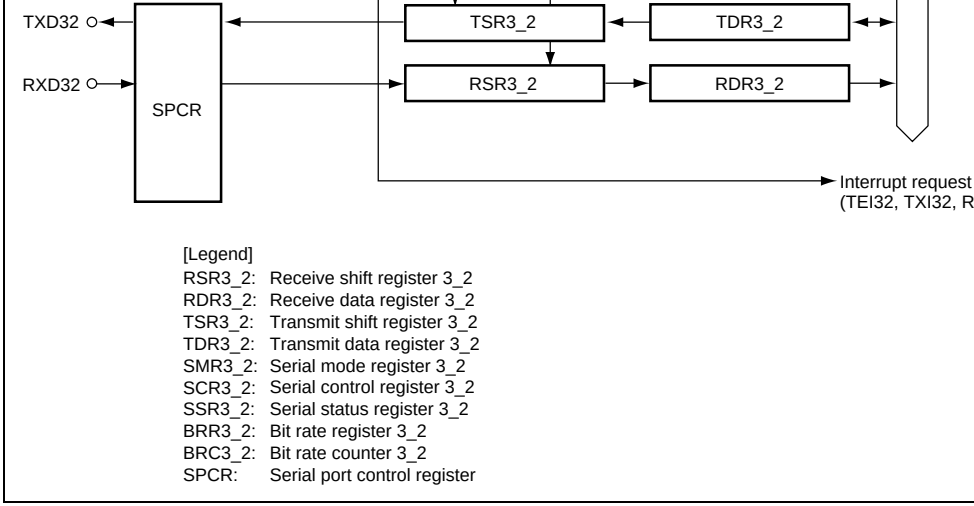


Figure 15.1 (1) Block Diagram of SCI3_1



[Legend]
RSR3_2: Receive shift register 3_2
RDR3_2: Receive data register 3_2
TSR3_2: Transmit shift register 3_2
TDR3_2: Transmit data register 3_2
SMR3_2: Serial mode register 3_2
SCR3_2: Serial control register 3_2
SSR3_2: Serial status register 3_2
BRR3_2: Bit rate register 3_2
BRC3_2: Bit rate counter 3_2
SPCR: Serial port control register

Figure 15.1 (2) Block Diagram of SCI3_2

input	RXD32		
SCI3 transmit data output	TXD31, TXD32	Output	SCI3 transmit data output

15.3 Register Descriptions

The SCI3 has the following registers for each channel.

- Receive shift register 3 (RSR3)*
- Receive data register 3 (RDR3)*
- Transmit shift register 3 (TSR3)*
- Transmit data register 3 (TDR3)*
- Serial mode register 3 (SMR3)*
- Serial control register 3 (SCR3)*
- Serial status register 3 (SSR3)*
- Bit rate register 3 (BRR3)*
- Serial port control register (SPCR)
- IrDA control register (IrCR)

Note: * These register names are abbreviated to RSR, RDR, TSR, TDR, SMR, SCR, BRR in the text.

receive-enabled. As RSR and RDR function as a double buffer in this way, continuous re
operations are possible. After confirming that the RDRF bit in SSR is set to 1, read RDR
once. RDR cannot be written to by the CPU. RDR is initialized to H'00.

RDR is initialized to H'00 by a reset or in standby mode, watch mode, or module standby

15.3.3 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the S
transfers transmit data from TDR to TSR automatically, then sends the data that starts fro
LSB to the TXD31 or TXD32 pin. Data transfer from TDR to TSR is not performed if no
been written to TDR (if the TDRE bit in SSR is set to 1). TSR cannot be directly accessed
CPU.

15.3.4 Transmit Data Register (TDR)

TDR is an 8-bit register that stores data for transmission. When the SCI3 detects that TSF
empty, it transfers the transmit data written in TDR to TSR and starts transmission. The d
buffered structure of TDR and TSR enables continuous serial transmission. If the next tra
data has already been written to TDR during transmission of one-frame data, the SCI3 tra
the written data to TSR to continue transmission. To achieve reliable serial transmission,
transmit data to TDR only once after confirming that the TDRE bit in SSR is set to 1. TD
initialized to H'FF.

TDR is initialized to H'FF by a reset or in standby mode, watch mode, or module standby

				1: Clocked synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchron mode) 0: Selects 8 or 5 bits as the data length. 1: Selects 7 or 5 bits as the data length. When 7-bit data is selected. the MSB (bit 7) i not transmitted. To select 5 bits as the data le 1 to both the PE and MP bits. The three most significant bits (bits 7, 6, and 5) in TDR are nc transmitted. In clocked synchronous mode, th length is fixed to 8 bits regardless of the CHR setting.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous When this bit is set to 1, the parity bit is adde transmit data before transmission, and the pa checked in reception. In clocked synchronous parity bit addition and checking is not perform regardless of the PE bit setting.

				an even number. When odd parity is selected, a parity bit is add transmission so that the total number of 1 bits transmit data plus the parity bit is an odd numb reception, a check is carried out to confirm tha number of 1bits in the receive data plus the pa an odd number. If parity bit addition and checking is disabled in synchronous mode and asynchronous mode, t bit setting is invalid.
3	STOP	0	R/W	Stop Bit Length (enabled only in asynchronous Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits For reception, only the first stop bit is checked, regardless of the value in the bit. If the second is 0, it is treated as the start bit of the next tran character.
2	MP	0	R/W	5-Bit Communication When this bit is set to 1, the 5-bit communicati format is enabled. When writing 1 to this bit, al write 1 to bit 5 (RE) at the same time. In additio must be written to bit 3 (MPIE) in the serial cor register (SCR) before writing 1 to this bit.

speed/high-speed) mode and sleep (medium-
speed/high-speed) mode ϕw/2 clock is set. In
mode and subsleep mode, ϕw clock is set. Th
enabled only, when ϕw/2 is selected for the C
operating clock.

For the relationship between the bit rate regis
and the baud rate, see section 15.3.8, Bit Rat
Register (BRR). n is the decimal representati
value of n in BRR (see section 15.3.8, Bit Rat
Register (BRR)).

				request is enabled. TXI (TXI32) can be release clearing the TDRE it or TI bit to 0.
6	RIE	0	R/W	Receive Interrupt Enable When this bit is set to 1, RXI and ERI interrupt are enabled. RXI (RXI32) and ERI (ERI32) can be released clearing the RDRF bit or the FER, PER, or OE flag to 0, or by clearing the RIE bit to 0.
5	TE	0	R/W	Transmit Enable When this bit is set to 1, transmission is enable this bit is 0, the TDRE bit in SSR is fixed at 1. V transmit data is written to TDR while this bit is TDRE in SSR is cleared to 0 and serial data tansmission is started. Be sure to carry out SM settings, and setting of bit SPC31 or SPC32 in to decide the transmission format before settin to 1.
4	RE	0	R/W	Receive Enable When this bit is set to 1, reception is enabled. state, serial data reception is started when a st detected in asynchronous mode or serial clock detected in clocked synchronous mode. Be sur carry out the SMR settings to decide the recep format before setting bit RE to 1. Note that the RDRF, FER, PER, and OER flag are not affected when bit RE is cleared to 0, ar their previous state

Asynchronous mode:

00: Internal baud rate generator (SCK31 or S functions as an I/O port)

01: Internal baud rate generator (Outputs a cl same frequency as the bit rate from the S SCK32 pin)

10: External clock (Inputs a clock with a frequ times the bit rate from the SCK31 or SCK

11: Reserved

Clocked synchronous mode:

00: Internal clock (SCK31 or SCK32 pin funct clock output)

01: Reserved

10: External clock (SCK31 or SCK32 pin func clock input)

11: Reserved

				[Setting conditions] • When the TE bit in SCR is 0 • When data is transferred from TDR to TSR [Clearing conditions] • When 0 is written to TDRE after reading TD • When the transmit data is written to TDR
6	RDRF	0	R/(W)*	Receive Data Register Full Indicates that the received data is stored in RD [Setting condition] • When serial reception ends normally and re data is transferred from RSR to RDR [Clearing conditions] • When 0 is written to RDRF after reading RI When data is read from RDR If an error is detected in reception, or if the RE SCR has been cleared to 0, RDR and bit RDR affected and retain their previous state. Note that if data reception is completed while b is still set to 1, an overrun error (OER) will occu the receive data will be lost.

				data it held before the overrun error occurred. received after the error is lost. Reception can continued with bit OER set to 1, and in clocke synchronous mode, transmission cannot be c either.
4	FER	0	R/(W)*	Framing Error [Setting condition] • When a framing error occurs in reception [Clearing condition] • When 0 is written to FER after reading FE When bit RE in SCR is cleared to 0, bit FER i affected and retains its previous state. Note that, in 2-stop-bit mode, only the first sto checked for a value of 1, and the second stop checked. When a framing error occurs, the re data is transferred to RDR but bit RDRF is no Reception cannot be continued with bit FER s clocked synchronous mode, neither transmiss reception is possible when bit FER is set to 1.

				still transferred to RDR, but bit RDRF is not Reception cannot be continued with bit PER 1. In clocked synchronous mode, neither transmission nor reception is possible when PER is set to 1.
2	TEND	1	R	Transmit End [Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last 1-byte serial transmit character [Clearing conditions] • When 0 is written to TDRE after readingTDR • When the transmit data is written to TDR
1	MPBR	0	R	Reserved This bit is read-only and reserved. It cannot be to.
0	MPBT	0	R/W	Reserved The write value should always be 0.

Note: * Only 0 can be written to clear the flag.

[Asynchronous Mode]

Active (medium-speed/high-speed) or sleep (medium-speed/high-speed)

$$N = \frac{OSC}{32 \times 2^{2n} \times B} - 1$$

$$\text{Error (\%)} = \frac{\text{B (bit rate obtained from n, N, } \phi\text{)} - \text{R (bit rate in left-hand column in table 15.}}{\text{R (bit rate in left-hand column in table 15.3)}}$$

Subactive or subsleep

$$N = \frac{OSC}{64 \times 2^{2n} \times B} - 1$$

[Legend] B: Bit rate (bit/s)

N: BRR setting for baud rate generator ($0 \leq N \leq 255$)

OSC: ϕ_{OSC} value (Hz)

n: Baud rate generator input clock number (n = 0, 2, or 3)

(The relation between n and the clock is shown in table 15.3)

600	—	—	—	0	0	0.00	0	103	0.16	0	108
1200	—	—	—	—	—	—	0	51	0.16	0	54
2400	—	—	—	—	—	—	0	25	0.16	0	26
4800	—	—	—	—	—	—	0	12	0.16	0	13
9600	—	—	—	—	—	—	—	—	—	0	6
19200	—	—	—	—	—	—	—	—	—	—	—
31250	—	—	—	—	—	—	0	1	0.00	—	—
38400	—	—	—	—	—	—	—	—	—	—	—

600	3	1	0.00	0	155	0.16	3	2	0.00	0	207
1200	3	0	0.00	0	77	0.16	2	5	0.00	0	103
2400	2	1	0.00	0	38	0.16	2	2	0.00	0	51
4800	2	0	0.00	0	19	–2.34	0	23	0.00	0	25
9600	0	7	0.00	0	9	–2.34	0	11	0.00	0	12
19200	0	3	0.00	0	4	–2.34	0	5	0.00	—	—
31250	—	—	—	0	2	0.00	—	—	—	0	3
38400	0	1	0.00	—	—	—	0	2	0.00	—	—

600	3	3	0.00	0	255	1.73	3	4	–2.34	3	4
1200	3	1	0.00	0	129	0.16	0	155	0.16	2	9
2400	3	0	0.00	0	64	0.16	0	77	0.16	2	4
4800	2	1	0.00	0	32	–1.36	0	38	0.16	0	39
9600	2	0	0.00	2	0	1.73	0	19	–2.34	0	19
19200	0	7	0.00	0	7	1.73	0	9	–2.34	0	9
31250	0	4	–1.70	0	4	0.00	0	5	0.00	0	5
38400	0	3	0.00	0	3	1.73	0	4	–2.34	0	4

600	3	5	0.00	2	25	0.16	3	7	0.00	2	32
1200	3	2	0.00	2	12	0.16	3	3	0.00	2	15
2400	2	5	0.00	0	103	0.16	3	1	0.00	0	129
4800	2	2	0.00	0	51	0.16	3	0	0.00	0	64
9600	0	23	0.00	0	25	0.16	2	1	0.00	0	32
19200	0	11	0.00	0	12	0.16	2	0	0.00	0	15
31250	—	—	—	0	7	0.00	0	9	–1.70	0	9
38400	0	5	0.00	—	—	—	0	7	0.00	0	7

Table 15.4 Relation between n and Clock

		SMR Setting	
n	**Clock**	**CKS1**	**CKS0**
0	ϕ	0	0
0	$\phi_w/2$*[1]/ϕ_w*[2]	0	1
2	$\phi/16$	1	0
3	$\phi/64$	1	1

Notes: 1. $\phi_w/2$ clock in active (medium-speed/high-speed) mode and sleep (medium-sp
speed) mode

2. ϕ_w clock in subactive mode and subsleep mode
In subactive or subsleep mode, the SCI3 can be operated only when CPU clo

3.6864	115200	0	0
4	125000	0	0
4.9152	153595	0	0
5	156250	0	0
6	187500	0	0
6.144	192000	0	0
7.3728	230400	0	0
8	250000	0	0
9.8304	307200	0	0
10	312500	0	0

Note: * When CKS1 = 0 and CKS0 = 1 in SMR

2.5k	—	—	—	—	—	—	0	199	0.0
5k	—	—	—	—	—	—	0	99	0.0
10k	—	—	—	—	—	—	0	49	0.0
25k	—	—	—	—	—	—	0	19	0.0
50k	—	—	—	—	—	—	0	9	0.0
100k	—	—	—	—	—	—	0	4	0.0
250k	—	—	—	—	—	—	0	1	0.0
500k	—	—	—	—	—	—	0*	0*	0.0
1M	—	—	—	—	—	—	—	—	—

Note: * Continuous transmission/reception is not possible.

2.5k	2	24	0.00	2	49	0.00	2	62	–0.7
5k	0	199	0.00	2	24	0.00	2	30	0.81
10k	0	99	0.00	0	199	0.00	2	15	–2.3
25k	0	39	0.00	0	79	0.00	0	99	0.00
50k	0	19	0.00	0	39	0.00	0	49	0.00
100k	0	9	0.00	0	19	0.00	0	24	0.00
250k	0	3	0.00	0	7	0.00	0	9	0.00
500k	0	1	0.00	0	3	0.00	0	4	0.00
1M	0*	0*	0.00*	0	1	0.00	—	—	—

Note: * Continuous transmission/reception is not possible.

The value set in BRR is given by the following formula:

Active (medium-speed/high-speed) or sleep (medium-speed/high-speed)

$$N = \frac{OSC}{4 \times 2^{2n} \times B} - 1$$

Subactive or subsleep

$$N = \frac{OSC}{8 \times 2^{2n} \times B} - 1$$

B: Bit rate (bit/s)

N: BRR setting for baud rate generator ($0 \leq N \leq 255$)

OSC: ϕ_{OSC} value (Hz)

n: Baud rate generator input clock number (n = 0, 2, or 3)
(The relation between n and the clock is shown in table 15.7.)

2. ϕ_w clock in subactive or subsleep mode
   In subactive or subsleep mode, the SCI3_1 and SCI3_2 can be operated only
   CPU clock is $\phi_w/2$.

15.3.9 Serial Port Control Register (SPCR)

SPCR selects the functions of the TXD32 and TXD31 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved
6	—	1	—	These bits are always read as 1 and cannot b modified.
5	SPC32	0	R/W	P32/TXD33 Pin Function Switch Selects whether pin P32/TXD32 is used as P3 TXD32. 0: P32 I/O pin 1: TXD32 output pin Set the TE32 bit in SCR32 after setting this bi
4	SPC31	0	R/W	P42/TXD31 Pin Function Switch Selects whether pin P42/TXD31 is used as P4 TXD31. 0: P42 I/O pin 1: TXD31 output pin Set the TE bit in SCR after setting this bit to 1

				0: Output data of RXD32 pin is not inverted. 1: Output data of RXD32 pin is inverted.
1	SCINV1	0	R/W	TXD31 Pin Output Data Inversion Switch Selects whether the polarity of output data of tl TXD31 pin is inverted or not. 0: Output data of TXD31 pin is not inverted. 1: Output data of TXD31 pin is inverted.
0	SCINV0	0	R/W	RXD31 Pin Input Data Inversion Switch Selects whether the polarity of input data of the pin is inverted or not. 0: Input data of RXD31 pin is not inverted. 1: Input data of RXD31 pin is inverted.

Note: When the serial port control register is modified, the data being input or output up t point is inverted immediately after the modification, and an invalid data change is i output. When modifying the serial port control register, modification must be made in which data changes are invalidated.

				1: TXD31/IrTXD or RXD31/IrRXD pin function IrTXD or IrRXD
6	IrCKS2	0	R/W	IrDA Clock Select
5	IrCKS1	0	R/W	If the IrDA function is enabled, these bits set t
4	IrCKS0	0	R/W	pulse width when encoding the IrTXD output 000: Bit rate × 3/16 001: ϕ/2 010: ϕ/4 011: ϕ/8 100: ϕ/16 101: Setting prohibited 11x: Setting prohibited
3 to 0	—	0	—	Reserved These bits are always read as 0 and cannot b modified.

[Legend] x: Don't care.

SMR as shown in table 15.9.

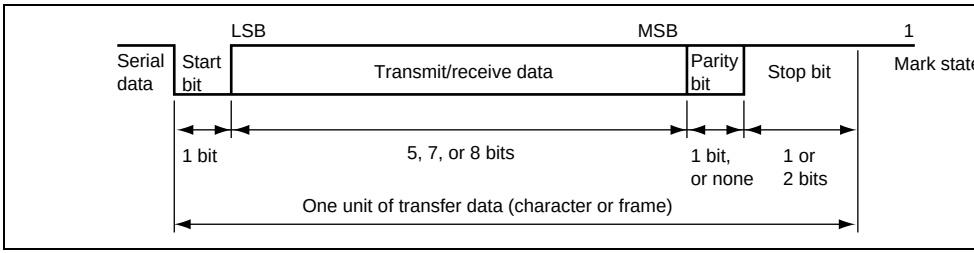


Figure 15.2 Data Format in Asynchronous Communication

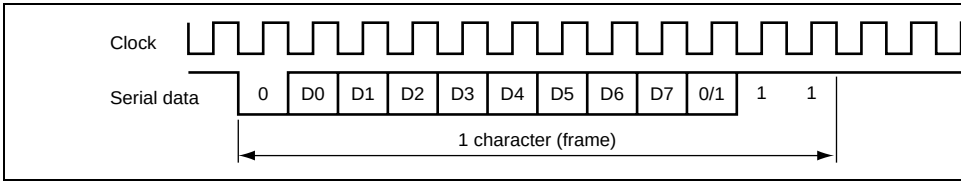


Figure 15.3 Relationship between Output Clock and Transfer Data Phas (Asynchronous Mode) (Example with 8-Bit Data, Parity, Two Stop Bits)

0	1	0	0	START 8-bit data P STOP
0	1	0	1	START 8-bit data P STOP STOP
0	1	1	0	START 5-bit data STOP
0	1	1	1	START 5-bit data STOP STOP
1	0	0	0	START 7-bit data STOP
1	0	0	1	START 7-bit data STOP STOP
1	0	1	0	Setting prohibited
1	0	1	1	Setting prohibited
1	1	0	0	START 7-bit data P STOP
1	1	0	1	START 7-bit data P STOP STOP
1	1	1	0	START 5-bit data P STOP
1	1	1	1	START 5-bit data P STOP STOP

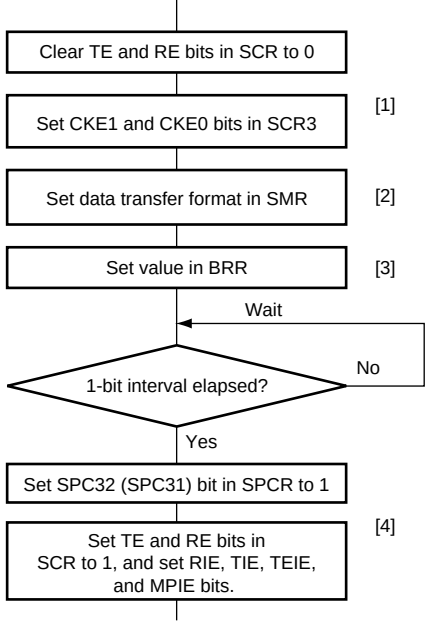
[Legend]

START: Start bit
STOP: Stop bit
P: Parity bit
MPB: Multiprocessor bit

				1			
			1	0			Yes
				1			
	0	1	0	0		Setting prohibited	
				1			
			1	0		5-bit data	No
				1			
	1		0	0		Setting prohibited	
				1			
			1	0		5-bit data	Yes
				1			
1	*	0	*	*	Clocked synchronous mode	8-bit data	No

[Legend] *: Don't care.

1	0	0	Clocked synchronous mode	Internal	Outputs serial clock
	1	0		External	Inputs serial clock
0	1	1	Reserved (Do not specify these combinations)		
1	0	1			
1	1	1			



MPIE, and bits TE and RE, to 0.

When the clock output is selected in asynchronous mode, clock is output immediately after CKE1 and CKE0 settings are made. When the clock output is selected at reception in clocked synchronous mode, clock is output immediately after CKE1, CKE0, and RE are set to 1.

[2] Set the data transfer format in SMR.

[3] Write a value corresponding to the bit rate to BRR. Not necessary if an external clock is used.

[4] Wait at least one bit interval, then set the TE bit or RE bit in SCR to 1. Setting bits TE and RE enables the TXD31 (TXD32) and RXD31 (RXD32) pins to be used. Also set the RIE, TIE, and TEIE bits, depending on whether interrupts are required. In asynchronous mode, the bits are marked at transmission and idled at reception to wait for the start bit.

Figure 15.4 Sample SCI3 Initialization Flowchart

completed.

3. The SCI3 checks the TDRE flag at the timing for sending the stop bit.
4. If the TDRE flag is 0, the data is transferred from TDR to TSR, the stop bit is sent, an serial transmission of the next frame is started.
5. If the TDRE flag is 1, the TEND flag in SSR is set to 1, the stop bit is sent, and then t state" is entered, in which 1 is output. If the TEIE bit in SCR is set to 1 at this time, a interrupt request is generated.
6. Figure 15.6 shows a sample flowchart for transmission in asynchronous mode.

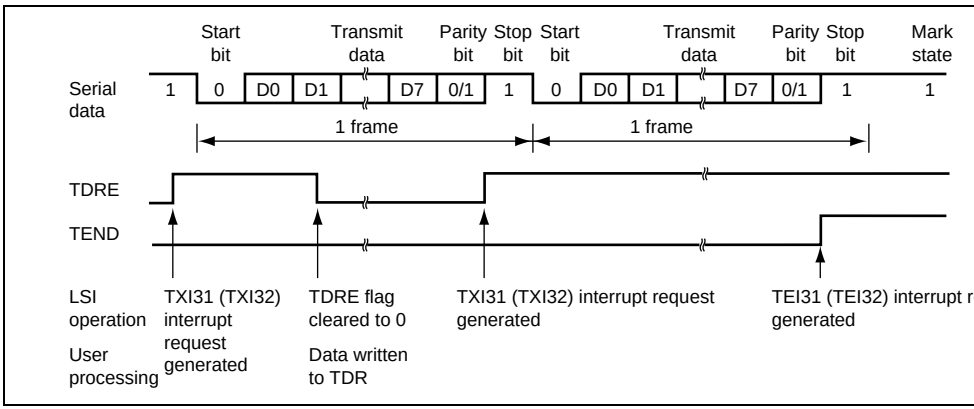
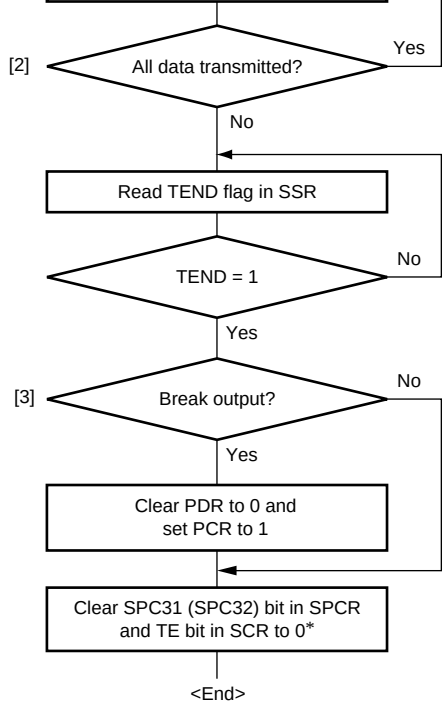


Figure 15.5 Example SCI3 Operation in Transmission in Asynchronous Mo (8-Bit Data, Parity, One Stop Bit)



then write data to TDR. When da
is written to TDR, the TDRE flag
automaticaly cleared to 0.

[3] To output a break in serial transmission, after setting PCR t and PDR to 0, clear the SPC31 (SPC32) bit in SPCR and the TE in SCR to 0.

Figure 15.6 Sample Serial Transmission Flowchart (Asynchronous Mode

- Stop bit check

  The SCI3 checks that the stop bit is 1. If two stop bits are used, only the first is check
- Status check

  The SCI3 checks that bit RDRF is set to 0, indicating that the receive data can be tran from RSR to RDR.

2. If an overrun error occurs (when reception of the next data is completed while the RD is still set to 1), the OER bit in SSR is set to 1. If the RIE bit in SCR is set to 1 at this ERI31 (ERI32) interrupt request is generated. Receive data is not transferred to RDR.
3. If a parity error is detected, the PER bit in SSR is set to 1 and receive data is transferr RDR. If the RIE bit in SCR is set to 1 at this time, an ERI31 (ERI32) interrupt reques generated.
4. If a framing error is detected (when the stop bit is 0), the FER bit in SSR is set to 1 an data is transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an ERI31 (ER interrupt request is generated.
5. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive da transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI31 (RXI32) i request is generated. Continuous reception is possible because the RXI31 (RXI32) int routine reads the receive data transferred to RDR before reception of the next receive been completed.

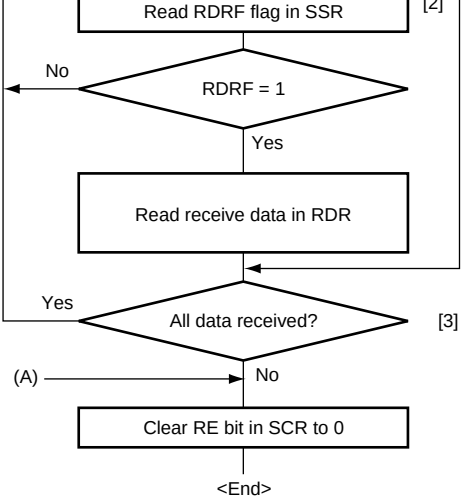
Figure 15.7 Example SCI3 Operation in Reception in Asynchronous Mod (8-Bit Data, Parity, One Stop Bit)

Table 15.11 shows the states of the SSR status flags and receive data handling when a re error is detected. If a receive error is detected, the RDRF flag retains its state before rece data. Reception cannot be resumed while a receive error flag is set to 1. Accordingly, cl OER, FER, PER, and RDRF bits to 0 before resuming reception. Figure 15.8 shows a sa flowchart for serial data reception.

Table 15.11 SSR Status Flags and Receive Data Handling

SSR Status Flag					
RDRF*	**OER**	**FER**	**PER**	**Receive Data**	**Receive Error Type**
1	1	0	0	Lost	Overrun error
0	0	1	0	Transferred to RDR	Framing error
0	0	0	1	Transferred to RDR	Parity error
1	1	1	0	Lost	Overrun error + frami
1	1	0	1	Lost	Overrun error + parity
0	0	1	1	Transferred to RDR	Framing error + parity
1	1	1	1	Lost	Overrun error + frami parity error

Note: * The RDRF flag retains the state it had before data reception. However, note t is read after an overrun error has occurred in a frame because reading of the data in the previous frame was delayed, the RDRF flag will be cleared to 0.



the error. After performing the appropriate error processing, ens that the OER, PER, and FER fla all cleared to 0. Reception cann resumed if any of these flags are 1. In the case of a framing error break can be detected by readin value of the input port correspon the RXD31 (RXD32) pin.

Figure 15.8 Sample Serial Data Reception Flowchart (Asynchronous Mode)

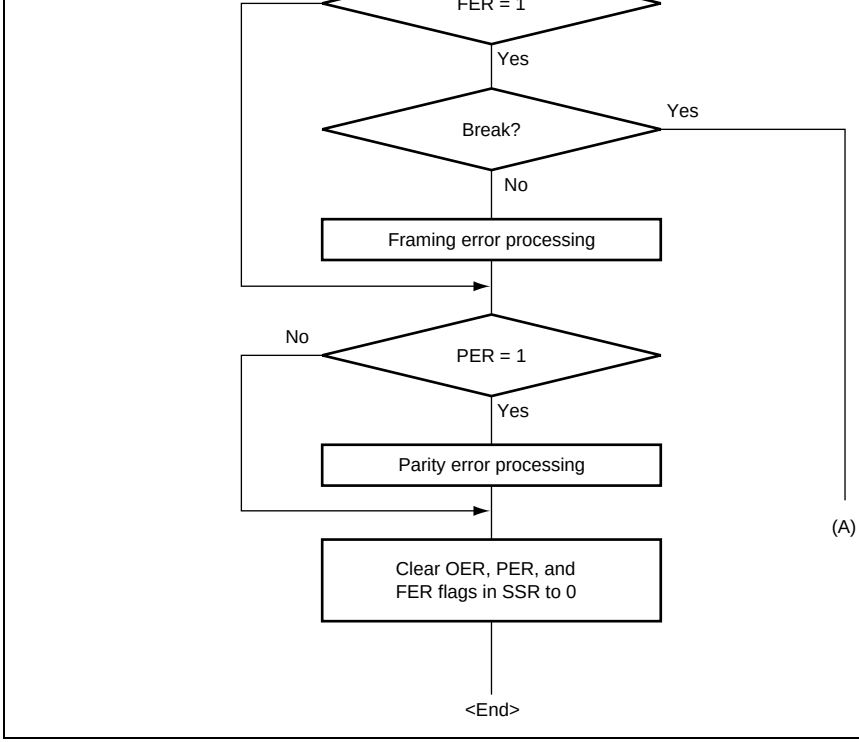


Figure 15.8 Sample Serial Data Reception Flowchart (Asynchronous Mode)

through the use of a common clock. Both the transmitter and the receiver also have a dou
buffered structure, so data can be read or written during transmission or reception, enabli
continuous data transfer.

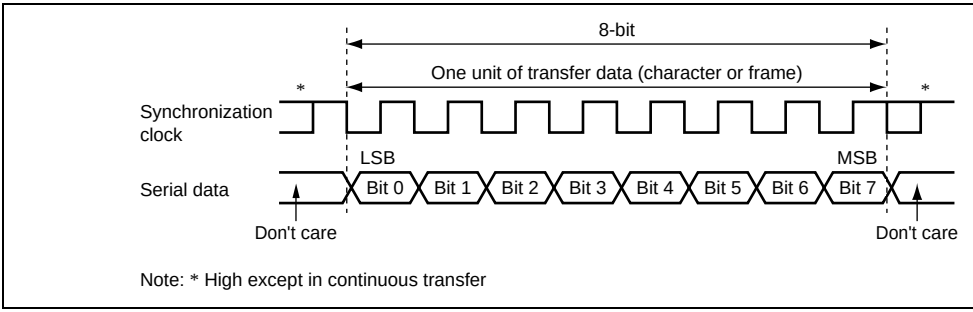


Figure 15.9 Data Format in Clocked Synchronous Communication

15.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK31 (SCK32) pin can be selected, according to the the COM bit in SMR and CKE0 and CKE1 bits in SCR. When the SCI3 is operated on an clock, the serial clock is output from the SCK31 (SCK32) pin. Eight serial clock pulses a in the transfer of one character, and when no transfer is performed the clock is fixed high

15.5.2 SCI3 Initialization

Before transmitting and receiving data, the SCI3 should be initialized as described in a sa flowchart in figure 15.4.

output clock mode has been specified, and synchronized with the input clock when t
external clock has been specified. Serial data is transmitted sequentially from the LS
from the TXD31 (TXD32) pin.

4. The SCI checks the TDRE flag at the timing for sending the MSB (bit 7).
5. If the TDRE flag is cleared to 0, data is transferred from TDR to TSR, and serial tra
of the next frame is started.
6. If the TDRE flag is set to 1, the TEND flag in SSR is set to 1, and the TDRE flag m
the output state of the last bit. If the TEIE bit in SCR is set to 1 at this time, a TEI31
is generated.
7. The SCK31 (SCK32) pin is fixed high.

Figure 15.11 shows a sample flowchart for serial data transmission. Even if the TDRE fl
cleared to 0, transmission will not start while a receive error flag (OER, FER, or PER) is
Make sure that the receive error flags are cleared to 0 before starting transmission.

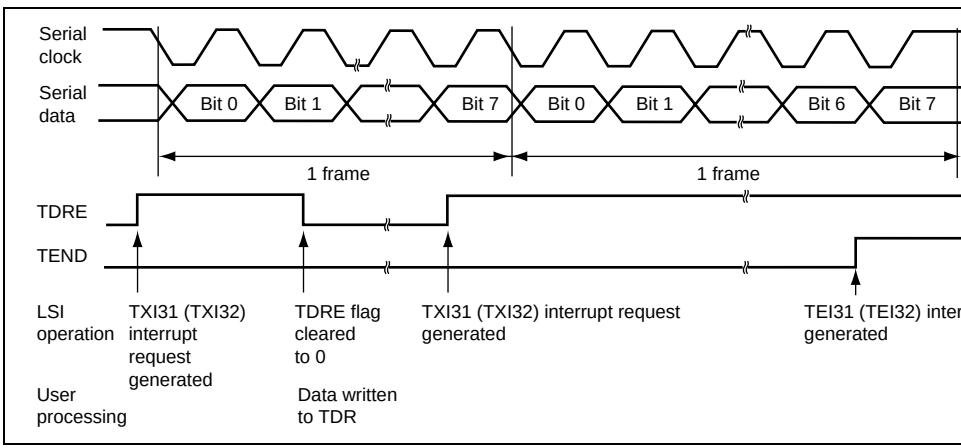
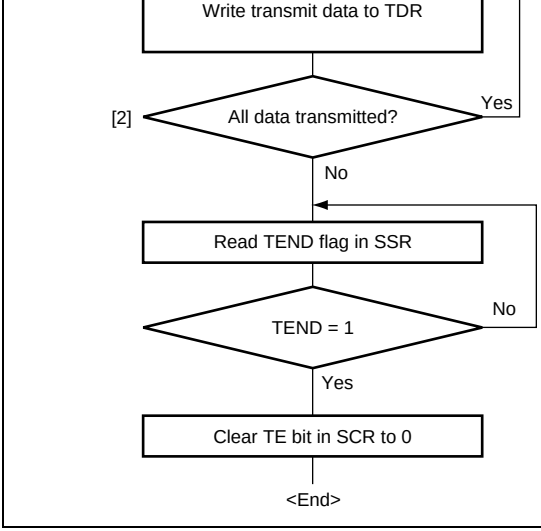


Figure 15.10 Example of SCI3 Operation in Transmission in Clocked Synchrono



When data is written to TDR, the TDRE fla
is automatically cleared to 0.

Figure 15.11 Sample Serial Transmission Flowchart (Clocked Synchronous M

time, an ERI31 (ERI32) interrupt request is generated, receive data is not transferred and the RDRF flag remains to be set to 1.

4. If reception is completed successfully, the RDRF bit in SSR is set to 1, and receive d transferred to RDR. If the RIE bit in SCR is set to 1 at this time, an RXI31 (RXI32) request is generated.

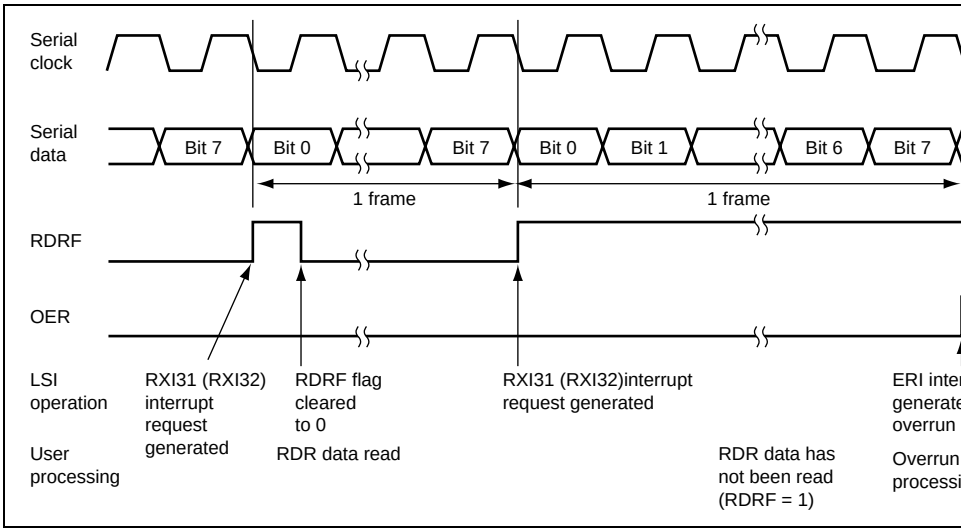
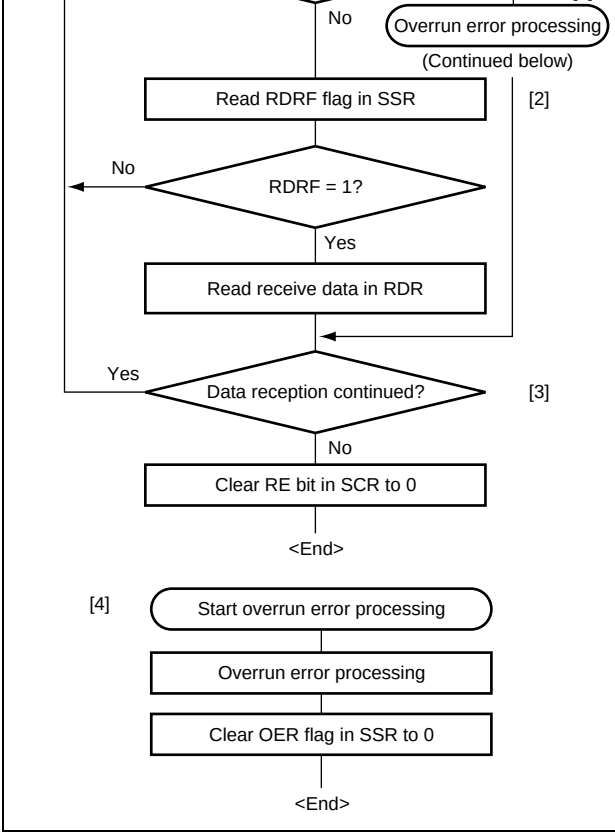


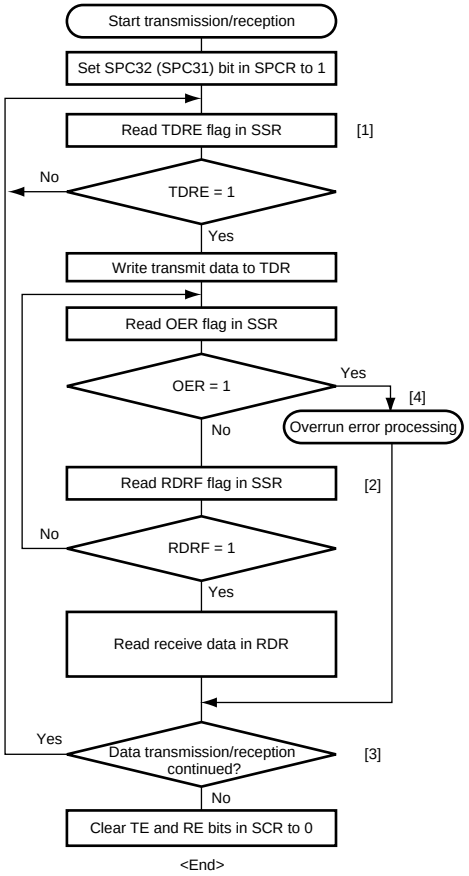
Figure 15.12 Example of SCI3 Reception Operation in Clocked Synchronous



MSB (bit 7) of the current frame is rec
reading the RDRF flag and reading R
should be finished. When data is read
RDR, the RDRF flag is automatically
cleared to 0.

[4] If an overrun error occurs, read the O
flag in SSR, and after performing the
appropriate error processing, clear th
flag to 0. Reception cannot be resum
the OER flag is set to 1.

Figure 15.13 Sample Serial Reception Flowchart (Clocked Synchronous Mod



[1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR.
When data is written to TDR, the TDRE flag is automatically cleared to 0.

[2] Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR.
When data is read from RDR, the RDRF flag is automatically cleared to 0.

[3] To continue serial transmission/ reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading RDR. Also, before the MSB (bit 7) of the current frame is transmitted, read 1 from the TDRE flag to confirm that writing is possible. Then write data to TDR.
When data is written to TDR, the TDRE flag is automatically cleared to 0. When data is read from RDR, the RDRF flag is automatically cleared to 0.

[4] If an overrun error occurs, read the OER flag in SSR, and after performing the appropriate error processing, clear the OER flag to 0. Transmission/reception cannot be resumed if the OER flag is set to 1. For overrun error processing, see figure 15.13.

Figure 15.14 Sample Flowchart of Simultaneous Serial Transmit and Receive Op (Clocked Synchronous Mode)

of 9600 bps, which can be modified as required. The IrDA interface provided by this LSI
incorporate the capability of automatic modification of the transfer rate; the transfer rate r
modified through programming.

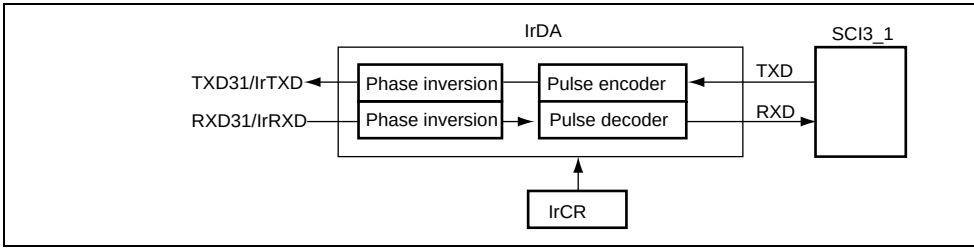


Figure 15.15 IrDA Block Diagram

15.6.1 Transmission

During transmission, the output signals from the SCI (UART frames) are converted to IR
using the IrDA interface (see figure 15.16).

For serial data of level 0, a high-level pulse having a width of 3/16 of the bit rate (1-bit in
output (initial setting). The high-level pulse can be selected using the IrCKS2 to IrCKS0
IrCR.

The high-level pulse width is defined to be 1.41 µs at minimum and (3/16 + 2.5%) × bit r
(3/16 × bit rate) +1.08 µs at maximum. For example, when the frequency of system clock
MHz, a high-level pulse width of at least 1.41 µs to 1.6 µs can be specified.

For serial data of level 1, no pulses are output.

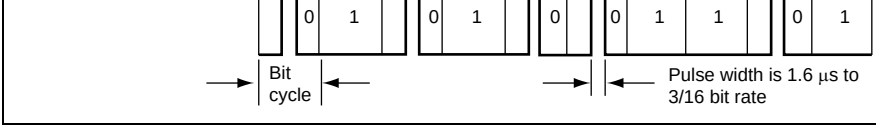


Figure 15.16 IrDA Transmission and Reception

15.6.2 Reception

During reception, IR frames are converted to UART frames using the IrDA interface be
inputting to the SCI3_1.

Data of level 0 is output each time a high-level pulse is detected and data of level 1 is ou
no pulse is detected in a bit cycle. If a pulse has a high-level width of less than 1.41 µs,
minimum width allowed, the pulse is recognized as level 0.

2	010	010	010	010
2.097152	010	010	010	010
2.4576	010	010	010	010
3	011	011	011	011
3.6864	011	011	011	011
4.9152	011	011	011	011
5	011	011	011	011
6	100	100	100	100
6.144	100	100	100	100
7.3728	100	100	100	100
8	100	100	100	100
9.8304	100	100	100	100
10	100	100	100	100

Transmission End	TEI	Setting TEND in SSR
Receive Error	ERI	Setting OER, FER, and PER in SSR

Each interrupt request can be enabled or disabled by means of bits TIE and RIE in SCR.

When the TDRE bit in SSR is set to 1, a TXI31 (TXI32) interrupt is requested. When th bit in SSR is set to 1, a TEI31 (TEI32) interrupt is requested. These two interrupts are g during transmission.

The initial value of the TDRE flag in SSR is 1. Thus, when the TIE bit in SCR is set to 1 transferring the transmit data to TDR, a TXI31 (TXI32) interrupt request is generated ev transmit data is not ready. The initial value of the TEND flag in SSR is 1. Thus, when th in SCR is set to 1 before transferring the transmit data to TDR, a TEI31 (TEI32) interrup is generated even if the transmit data has not been sent. It is possible to make use of the these interrupt requests efficiently by transferring the transmit data to TDR in the interru To prevent the generation of these interrupt requests (TXI31 and TEI31), set the enable and TEIE) that correspond to these interrupt requests to 1, after transferring the transmit TDR.

When the RDRF bit in SSR is set to 1, an RXI31 (RXI32) interrupt is requested, and if a OER, PER, and FER is set to 1, an ERI31 (ERI32) interrupt is requested. These two inte requests are generated during reception.

The SCI3 can carry out continuous reception using an RXI31 (RXI32) and continuous transmission using a TXI31 (TXI32).

These interrupts are shown in table 15.14.

(TXI32)	TIE	(on completion of the previous transmission) and the transmit data placed in TDR is transferred to TSR, bit TDRE is set to 1. If bit TIE is set to 1 at this time, a TXI31 (TXI32) is enabled and an interrupt is requested. (See figure 15.17 (b).)	routine writes the next tra data to TDR and clears b to 0. Continuous transmis be performed by repeatin above operations until the transferred to TSR has b transmitted.
TEI31 (TEI32)	TEND TEIE	When the last bit of the character in TSR is transmitted, if bit TDRE is set to 1, bit TEND is set to 1. If bit TEIE is set to 1 at this time, a TEI31 (TEI32) is enabled and an interrupt is requested. (See figure 15.17 (c).)	A TEI31 (TEI32) indicates next transmit data has no written to TDR when the the transmit character in transmitted.

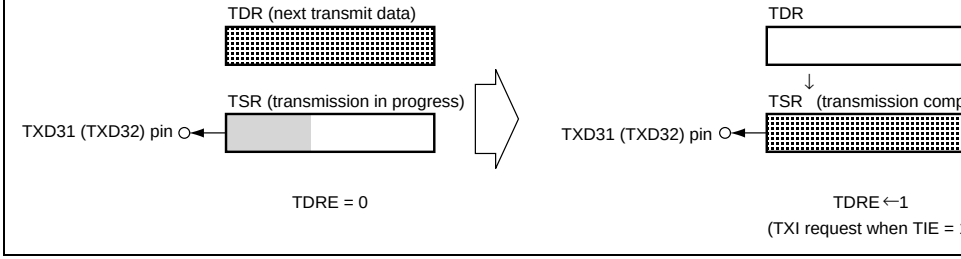


Figure 15.17 (b) TDRE Setting and TXI Interrupt

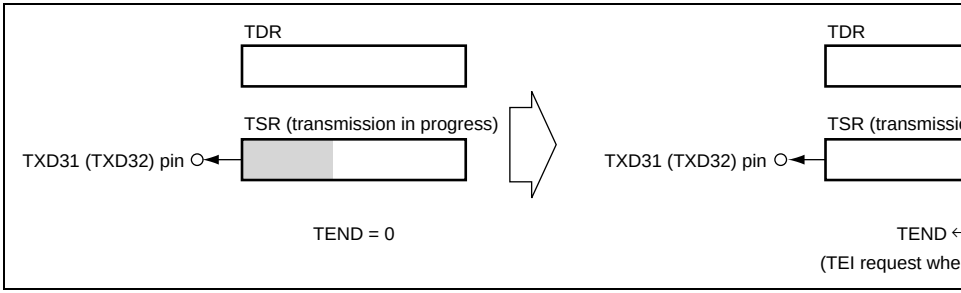


Figure 15.17 (c) TEND Setting and TEI Interrupt

Regardless of the value of TE, when the SPCR31 (SPCR32) bit in SPCR is cleared to 0, t
TXD31 (TXD32) pin is used as an I/O port whose direction (input or output) and level ar
determined by PCR and PDR. This can be used to set the TXD31 (TXD32) pin to mark s
level) or send a break during serial data transmission. To maintain the communication lin
state (1) until SPCR31 (SPCR32) in SPCR is set to 1, set both PCR and PDR to 1. As SP
(SPCR32) in SPCR is cleared to 0 at this point, the TXD31 (TXD32) pin becomes an I/O
1 is output from the TXD31 (TXD32) pin. To send a break during serial transmission, firs
PCR to 1 and PDR to 0, and then clear SPCR31 (SPCR32) and TE to 0. If TE is cleared t
immediately after SPCR31 (SPCR32) is cleared to 0, the transmitter is initialized regardl
current transmission state after TE is cleared, and when SPCR31 (SPCR32) is cleared to
TXD31 (TXD32) pin becomes an I/O port and 0 is output from it.

15.8.3 Receive Error Flags and Transmit Operations (Clocked Synchronous Mod

Transmission cannot be started when a receive error flag (OER, PER, or FER) is set to 1,
the TDRE flag is cleared to 0. Be sure to clear the receive error flags to 0 before starting
transmission. Note also that receive error flags cannot be cleared to 0 even if the RE bit is
to 0.

... Formula (1)

Where N: Ratio of bit rate to clock (N = 16)
D: Clock duty (D = 0.5 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute value of clock rate deviation

Assuming values of F (absolute value of clock rate deviation) = 0 and D (clock duty) = 0
formula (1), the reception margin can be given by the formula.

$$M = \{0.5 - 1/(2 \times 16)\} \times 100\ [\%] = 46.875\%$$

However, this is only the computed value, and a margin of 20% to 30% should be allow
system design.

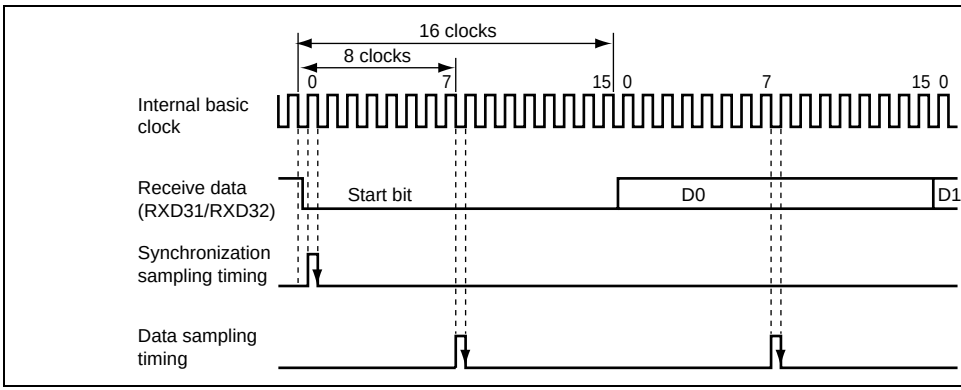


Figure 15.18 Receive Data Sampling Timing in Asynchronous Mode

CKE1 and CKE0 in SCR to 1 and 0, respectively.

In this case, bit COM in SMR should be left 1. The above prevents the SCK31 (SCK32) p being used as a general input/output pin. To avoid an intermediate level of voltage from b applied to the SCK31 (SCK32) pin, the line connected to the SCK31 (SCK32) pin should pulled up to the V_{CC} level via a resistor, or supplied with output from an external device.

(2) When SCK31 (SCK32) Function is Switched from Clock Output to General Input/Output

When stopping data transfer,

1. Issue one instruction to clear bits TE and RE to 0 and to set bits CKE1 and CKE0 in S and 0, respectively.
2. Clear bit COM in SMR to 0
3. Clear bits CKE1 and CKE0 in SCR to 0. Note that special care is also needed here to intermediate level of voltage from being applied to the SCK31 (SCK32) pin.

15.8.6 Relation between Writing to TDR and Bit TDRE

Bit TDRE in the serial status register (SSR) is a status flag that indicates that data for seri transmission has not been prepared in TDR. When data is written to TDR, bit TDRE is cl 0 automatically. When the SCI3 transfers data from TDR to TSR, bit TDRE is set to 1.

Data can be written to TDR irrespective of the state of bit TDRE, but if new data is writte TDR while bit TDRE is cleared to 0, the data previously stored in TDR will be lost if it h been transferred to TSR. Accordingly, to ensure that serial transmission is performed dep you should first check that bit TDRE is set to 1, then write the transmit data to TDR only two or more times).

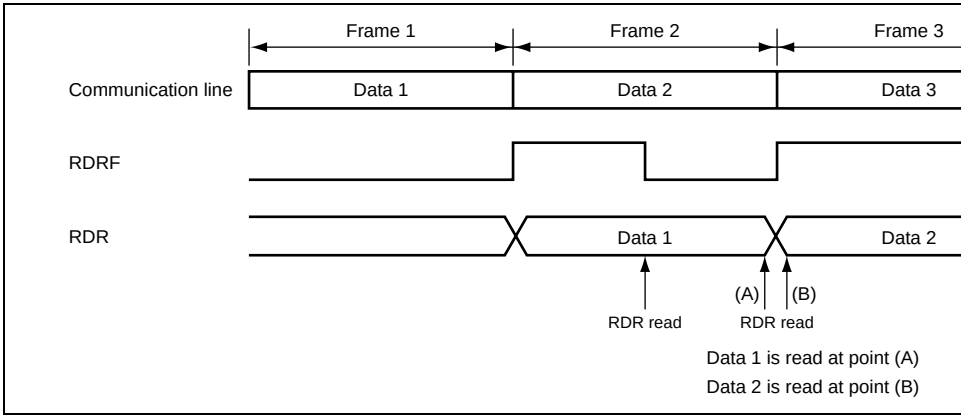


Figure 15.19 Relation between RDR Read Timing and Data

In this case, only a single RDR read operation (not two or more) should be performed af checking that bit RDRF is set to 1. If two or more reads are performed, the data read the should be transferred to RAM, etc., and the RAM contents used. Also, ensure that there sufficient margin in an RDR read operation before reception of the next frame is comple precise in terms of timing, the RDR read should be completed before bit 7 is transferred synchronous mode, or before the STOP bit is transferred in asynchronous mode.

15.8.8 Transmit and Receive Operations when Making State Transition

Make sure that transmit and receive operations have completely finished before carrying transition processing.

Version).

selected as a clock source.

- Receive error detection: Overrun errors detected
- Four interrupt sources

  Transmit-end, transmit-data-empty, receive-data-full, and overrun error
- Full-duplex communication capability

  Buffering is used in both the transmitter and the receiver, enabling continuous transm
  and continuous reception of serial data.
- When the on-chip emulator debugger etc. is not used, the SCI4 is available for the us
- Use of module standby mode enables this module to be placed in standby mode inde
  when not used. (For details, refer to section 6.4, Module Standby Function.)

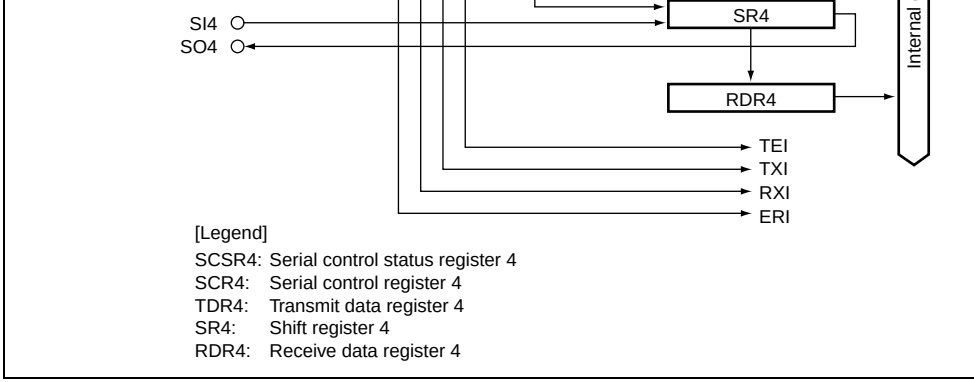


Figure 16.1 Block Diagram of SCI4

16.2 Input/Output Pins

Table 16.1 shows the SCI4 pin configuration.

Table 16.1 Pin Configuration

Pin Name	Abbreviation	I/O	Function
SCI4 clock	SCK4	I/O	SCI4 clock input/output
SCI4 data input	SI4	Input	SCI4 receive data input
SCI4 data output	SO4	Output	SCI4 transmit data output

16.3.1 Serial Control Register 4 (SCR4)

SCR4 enables or disables interrupt requests and controls SCI4 transfer operations.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable Enables or disables a transmit data empty inte (TXI) request when serial transmit data is tran from TDR4 to SR4 and the TDRE flag in SCS to 1. TXI can be cleared by clearing the TDRE SCSR4 to 0 after the flag is read as 1 or clear to 0. 0: Transmit data empty interrupt (TXI) request 1: Transmit data empty interrupt (TXI) request
6	RIE	0	R/W	Receive Interrupt Enable Enables or disables a receive data full interrup request and receive error interrupt (ERI) requ serial receive data is transferred from SR4 to the RDRF flag in SCSR4 is set to 1. RXI and be cleared by clearing the RDRF or ORER fla SCSR4 to 0 after the flag is read as 1 or clear to 0. 0: Receive data full interrupt (RXI) request an error interrupt (ERI) request disabled 1: Receive data full interrupt (RXI) request an error interrupt (ERI) request enabled

				Sets the output level of the SO4 pin. When this read, the output level of the SO4 pin is read. Th of the SO4 pin retains the value of the last bit o data after transmission is completed. However, is changed before or after transmission, the ou of the SO4 pin can be changed. When the outp of the SO4 pin is changed, the SOLP bit should cleared to 0 and the MOV instruction should be Note that this bit should not be changed during transmission because incorrect operation may [When reading] 0: The output level of the SO4 pin is low. 1: The output level of the SO4 pin is high. [When writing] 0: The output level of the SO4 pin is changed t 1: The output level of the SO4 pin is changed t
3	SOLP	1	R/W	SOL Write Protect Controls change of the output level of the SO4 to the change of the SOL bit. When the output the SO4 pin is changed, the setting of SOL = 1 SOLP = 0 or SOL = 0 and SOLP = 0 is made b MOV instruction. This bit is always read as 1. 0: When writing, the output level is changed ac to the value of the SOL pin. 1: When reading, this bit is always read as 1 ar be modified.

				1: Internal sequencer is forcibly reset
1	TE	0	R/W	Transmit Enable Enables or disables start of the SCI4 serial transmission. When this bit is cleared to 0, the flag in SCSR4 is fixed to 1. When transmit dat written to TDR4 while this bit is set to 1, the TI in SCSR4 is automatically cleared to 0 and se transmission is started. 0: Transmission disabled (SO4 pin functions a 1: Transmission enabled (SO4 pin functions a data pin)
0	RE	0	R/W	Receive Enable Enables or disables start of the SCI4 serial re Note that the RDRF and ORER flags in SCSR affected even if this bit is cleared to 0, and ret previous state. Serial data reception is started synchronous clock input is detected while this to 1 (when an external clock is selected). Whe internal clock is selected, the synchronous clo output and serial data reception is started. 0: Reception disabled (SI4 pin functions as I/O 1: Reception enabled (SI4 pin functions as rec pin)

				Indicates that data is transferred from TDR4 to the next serial transmit data can be written to T [Setting conditions] • When the TE bit in SCR4 is 0 • When data is transferred from TDR4 to SR4 data can be written to TDR4 [Clearing conditions] • When 0 is written to TDRE after reading TD • When data is written to TDR4
6	RDRF	0	R/(W)*	Receive Data Full Indicates that the receive data is stored in RDR [Setting condition] • When serial reception ends normally and re data is transferred from SR4 to RDR4 [Clearing conditions] • When 0 is written to RDRF after reading RD • When data is read from RDR4

				continued either. [Setting condition] • When the next serial reception is complete RDRF = 1 [Clearing condition] • When 0 is written to ORER after reading O
4	TEND	0	R/(W)*	Transmit End Indicates that the TDRE flag has been set to 1 transmission of the last bit of transmit data. [Setting condition] • When TDRE = 1 at transmission of the las transmit data [Clearing conditions] • When 0 is written to TEND after reading T • When data is written to TDR4 with an instr
3	CKS3	1	R/W	Clock Source Select and Pin Function
2	CKS2	0	R/W	Select the clock source to be supplied and set input/output for the SCK4 pin. The prescaler d ratio and transfer clock cycle when an internal selected are shown in table 16.2. When an ex clock is selected, the external clock cycle shou least 4/ϕ.
1	CKS1	0	R/W	
0	CKS0	0	R/W	

Note: * Only 0 can be written to clear the flag.

0	0	1	0	φ/64	12.8 µs	25.6 µs	Internal clock	SC ou
0	0	1	1	φ/32	6.4 µs	12.8 µs	Internal clock	SC ou
0	1	0	0	φ/16	3.2 µs	6.4 µs	Internal clock	SC ou
0	1	0	1	φ/8	1.6 µs	3.2 µs	Internal clock	SC ou
0	1	1	0	φ/4	0.8 µs	1.6 µs	Internal clock	SC ou
0	1	1	1	φ/2	—	0.8 µs	Internal clock	SC ou
1	0	0	0	—	—	—	I/O port (initial	
1	0	0	1	—	—	—	I/O port	
1	0	1	0	—	—	—	I/O port	
1	0	1	1	—	—	—	I/O port	
1	1	0	0	—	—	—	I/O port	
1	1	0	1	—	—	—	I/O port	
1	1	1	0	—	—	—	I/O port	
1	1	1	1	—	—	—	External clock	SC pi

RDR4 is an 8-bit register that stores receive data. When the SCI4 has received one byte
data, it transfers the received serial data from SR4 to RDR4, where it is stored. Then rec
operation is completed. After this, SR4 is receive-enabled. RDR4 cannot be written to b
RDR4 is initialized to H'00.

16.3.5 Shift Register 4 (SR4)

SR4 is a register that receives or transmits serial data. SR4 cannot be directly read from
to by the CPU.

The eight internal clocks or an external clock can be selected as a transfer clock. When th external clock is selected, the SCK4 pin is a clock input pin. When the internal clock is se the SCK4 pin is a synchronous clock output pin. The synchronous clock is output eight pu 1-character transmission or reception. While neither transmission nor reception is being performed, the signal is fixed high.

When the internal clock or external clock is not selected according to the combination of CKS3 to CKS0 bits in SCSR4, the SCK4 pin functions as an I/O port.

16.4.2 Data Transfer Format

Figure 16.2 shows the SCI4 transfer format.

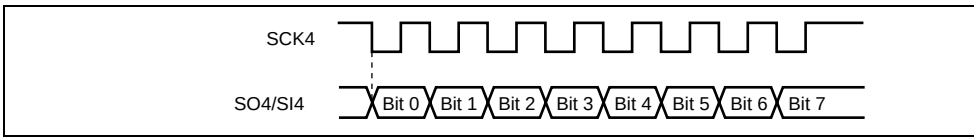


Figure 16.2 Data Transfer Format

In clocked synchronous communication, data on the communication line is output from th edge to the next falling edge of the synchronous clock. The data is guaranteed to be settle rising edge of the synchronous clock. One character starts with the LSB and ends with the After transmitting the MSB, the communication line retains the MSB level.

The SCI4 latches data at the rising edge of the synchronous clock on reception. The data format is fixed to 8-bit data. While transmission is stopped, the output level on the SO4 p changed by the SOL setting in SCR4.

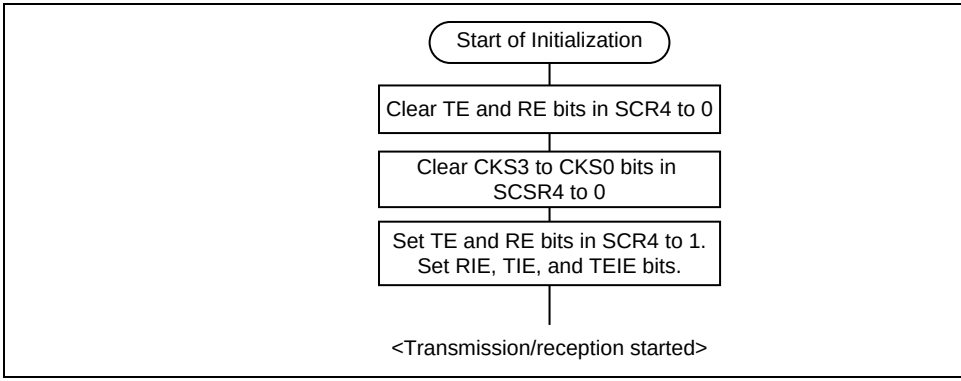
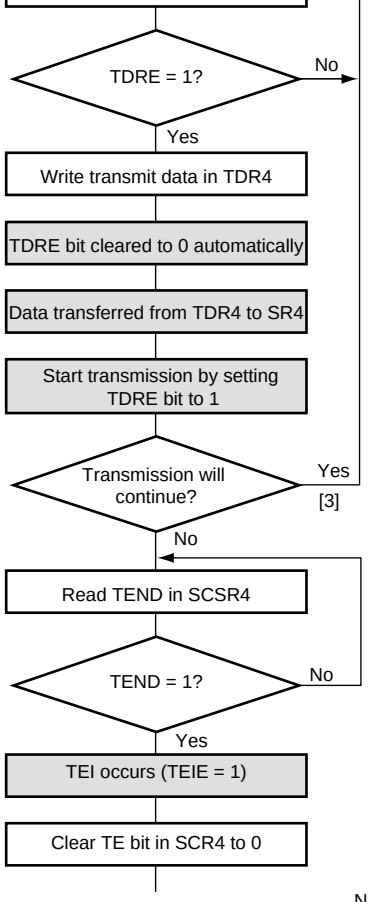


Figure 16.3 Flowchart Example of SCI4 Initialization



data transmission.

[3] To consecutively transmit data, read TDRE = 1 to confirm that TDR4 is ready. After that, write data in TDR4. Writing data in TDR4 clears the TDRE bit to 0 automatically.

Note: Hatching area indicates SCI internal operation.

Figure 16.4 Flowchart Example of Data Transmission

after transmitting the MSB (bit 7). At this time, when the TEIE bit in SCR4 is set to
generated.

5. After the transmission, the output level on pin SCK4 is fixed high.

Note: Transmission cannot be performed when the error flag (ORER) which indicates
reception status is set to 1. Before transmission, confirm that the ORER flag is c
0.

Figure 16.5 shows the example of transmission operation.

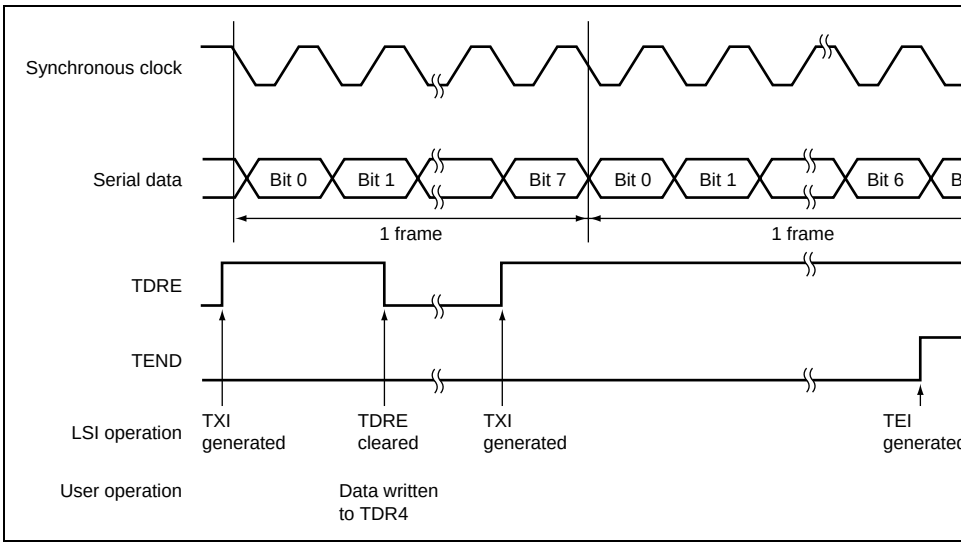
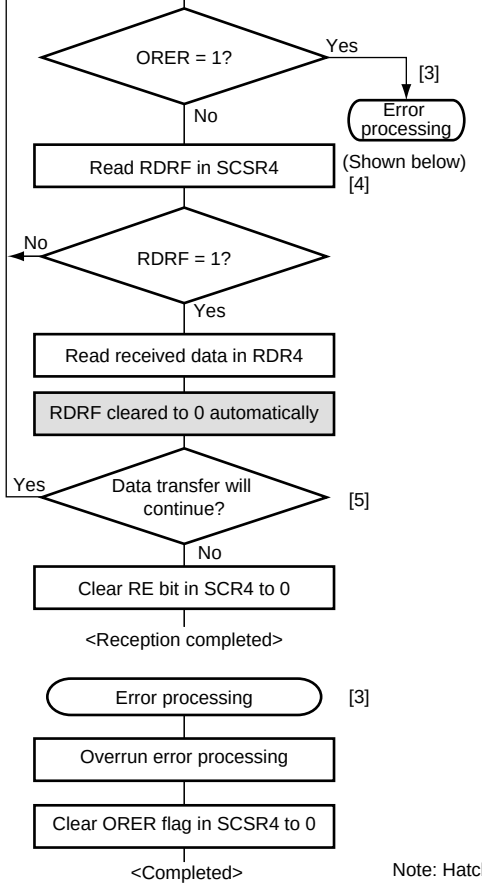


Figure 16.5 Transmit Operation Example



[4] After reading SCSR4 and confirming RDRF read the receive data in RDR4. The RDRF is automatically cleared to 0. Changes in th RDRF flag from 0 to 1 can be notified by ar interrupt.

[5] To consecutively receive data, reading the flag and RDR4 must be completed before receiving the MSB (bit 7) of the current fran

Note: Hatching area indicates SCI internal operation.

Figure 16.6 Flowchart Example of Data Reception

generated.

5. An overrun error is detected when the next data reception is completed with the RDF SCSR4 set to 1. The received data is not transferred from SR4 to RDR4.

Note: Reception cannot be performed when the error flag is set to 1. Before reception, that the ORER and RDRF flags are cleared to 0.

Figure 16.7 shows an operation example of reception.

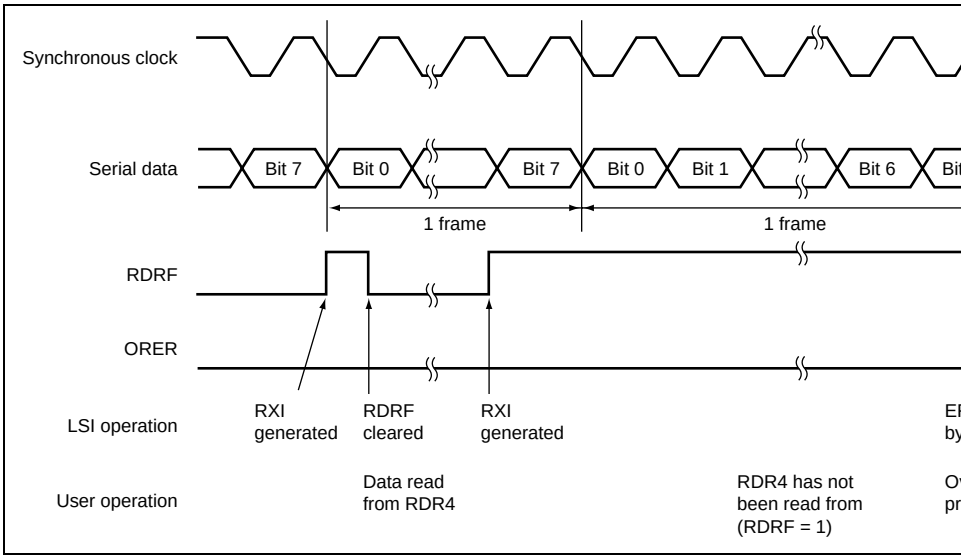
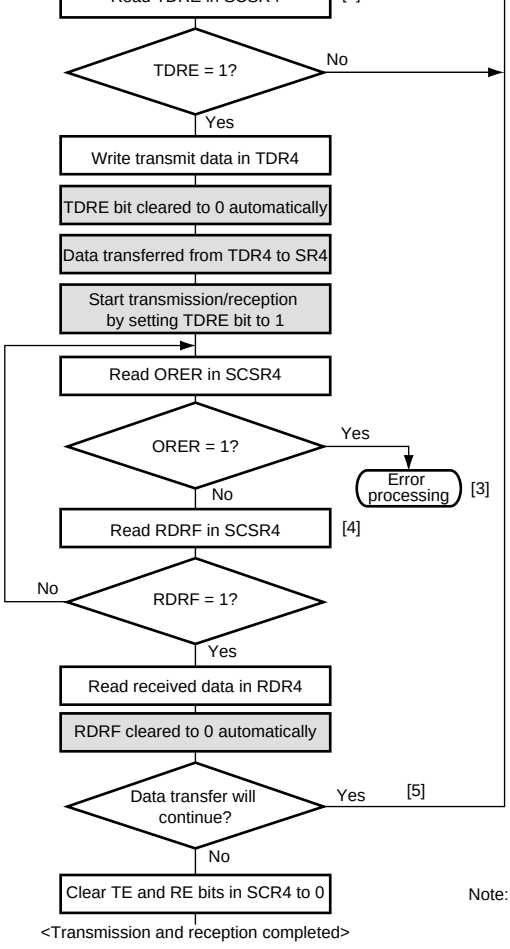


Figure 16.7 Receive Operation Example



cally. At this time, the clock is output to start data transfer.

[3] When a reception error occurs, read the ORE flag in SCSR4 and then clear the ORER flag to 0 after executing the error processing. Wh the ORER flag is set to 1, both transmission and reception cannot be restarted.

[4] After reading SCSR4 and confirming RDRF = read receive data in RDR4 and clear the RDR flag to 0. An RXI interrupt can also be used t confirm that the RDRF flag value has been c from 0 to 1.

[5] To consecutively transmit and receive data, t following operation must be completed: readi the RDRF flag and reading RDR4 before rec the MSB (bit 7) of the current frame: confirmi that TDR4 is ready for writing by reading TDR = 1 before transmitting the MSB (bit 7) and w data to TDR4 to clear the TDRE flag to 0.

Note: Hatching area indicates SCI internal operation.

Figure 16.8 Flowchart Example of Simultaneous Transmission and Recepti

Table 16.3 lists the descriptions of the interrupt sources.

Table 16.3 SCI4 Interrupt Sources

Abbreviation	Condition	Interrupt Source
RXI	RIE = 1	Receive data full (RDRF)
TXI	TIE = 1	Transmit data empty (TDRE)
TEI	TEIE = 1	Transmit end (TEND)
ERI	RIE = 1	Receive error (ORER)

The interrupt requests can be enabled/disabled by the TIE and RIE bits in SCR4.

When the TDRE flag in SCSR4 is set to 1, a TXI is generated. When the TEND bit in S set to 1, a TEI is generated. These two interrupt requests are generated during transmissi

The TDRE flag in SCSR4 is initialized to 1. Therefore, if a TXI request is enabled by se TIE bit in SCR4 to 1 before transmit data is transferred to TDR4, a TXI is generated eve transmit data is not ready.

If transmit data is transferred to TDR4 in the interrupt handling routine, these interrupt r can be effectively used.

To avoid the occurrence of the interrupt requests (TXI and TEI), clear the corresponding enable bits (TIE and TEIE) to 0 after transmit data is transferred to TDR4.

When the RDRF bit in SCSR4 is set to 1, an RXI is generated. When the ORER flag is s ERI is generated. These two interrupt requests are generated during reception.

Data is written to TDR4 regardless of the TDRE flag value. However, if data is written to
with TDRE = 0, the previous data is lost unless the previous data has been transferred to S
Accordingly, to ensure transmission, writing transmit data to TDR4 must be performed o
confirming that the TDRE flag has been set to 1. (Do not write more than once.)

16.6.2 Receive Error Flag and Transmission

While the receive error flag (ORER) is set to 1, transmission cannot be started even if the
flag is cleared to 0. To start transmission, the ORER flag must be cleared to 0.

Note that the ORER flag cannot be cleared to 0 even if the RE bit is cleared to 0.

16.6.3 Relationship between Reading RDR4 and RDRF

The SCI4 always checks the RDRF flag status during reception. When the RDRF flag is c
0 at the end of a frame, the reception is completed without error. When the RDRF flag is
it indicates that an overrun has occurred.

Since reading RDR4 clears the RDRF flag to 0 automatically, if RDR4 is read twice or m
data is read with the RDRF flag cleared to 0. In this case, when the timing of the read ope
matches that of the data reception of the next frame, the read data may be the next frame
Figure 16.9 shows this operation.

Figure 16.9 Relationship between Reading RDR4 and RDRF

In this case, RDR4 must be read only once after confirming RDRF = 1. If reading RDR4 more, store the read data in the RAM, and use the stored data. In addition, there should l margin from the timing of reading RDR4 to completion of the next frame reception. (Re RDR4 should be completed before the bit 7 transfer.)

16.6.4 SCK4 Output Waveform when Internal Clock of ϕ/2 is Selected

When the internal clock of ϕ/2 is selected by the CKS3 to CKS0 bits in SCSR4 and cont transmission or reception is performed, one pulse of high period is lengthened after eigh the clock has been output as shown in figure 16.10.

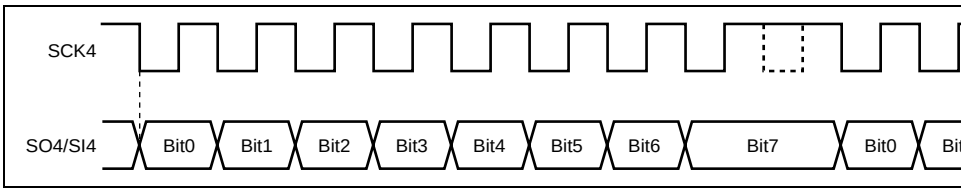


Figure 16.10 Transfer Format when Internal Clock of ϕ/2 is Selected

A conversion period of 131,072/ϕ with a minimum modulation width of 8/ϕ, a conve
period of 65,536/ϕ with a minimum modulation width of 4/ϕ, a conversion period of
with a minimum modulation width of 2/ϕ, or a conversion period of 16,384/ϕ with a
modulation width of 1/ϕ, can be selected.

- Pulse division method for less ripple
- Use of module standby mode enables this module to be placed in standby mode inde
when not used. (For details, refer to section 6.4, Module Standby Function.)
- The standard PWM or pulse-division type PWM can be selected by software.

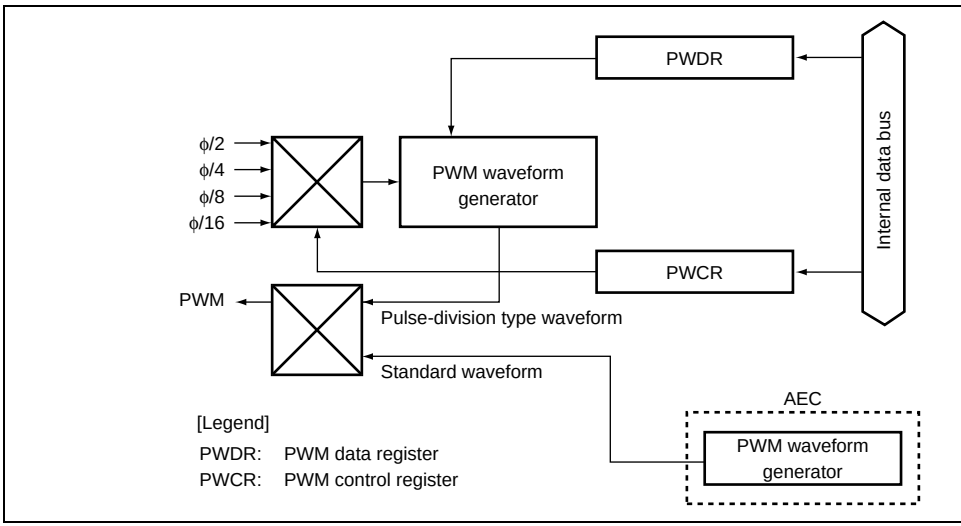


Figure 17.1 Block Diagram of 14-Bit PWM

17.3 Register Descriptions

The 14-bit PWM has the following registers.

- PWM1 control register (PWCR1)
- PWM1 data register (PWDR1)
- PWM2 control register (PWCR2)
- PWM2 data register (PWDR2)

17.3.1 PWM Control Register (PWCR)

PWCR selects the input clocks and selects whether the standard PWM or pulse-division t
PWM is used.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 1	—	Reserved These bits are always read as 1 and cannot be modified.
2	PWCRm2	0	W	PWM Output Waveform Select Selects whether the standard PWM waveform division type PWM waveform is output. 0: Pulse-division type PWM waveform is output 1: Standard PWM waveform is output

10: The input clock is $\phi/8$ ($t\phi^* = 8/\phi$)

— A conversion period is 65,536/ϕ, with a modulation width of 4/ϕ

11: The input clock is $\phi/16$ ($t\phi^* = 16/\phi$)

— A conversion period is 131,072/ϕ, with minimum modulation width of 8/ϕ

Note: * $t\phi$: Period of PWM clock input
m = 2 or 1

17.3.2 PWM Data Register (PWDR)

PWDR is a 14-bit write-only register. PWDR indicates high level width in one PWM wa cycle when the pulse-division type PWM is selected.

When data is written to the lower 14 bits of PWDR, the contents are latched in the PWM waveform generator and the PWM waveform generation data is updated.

The initial value of PWDR is 0, and it is always read as H'FFFF.

Always write to this register in word size.

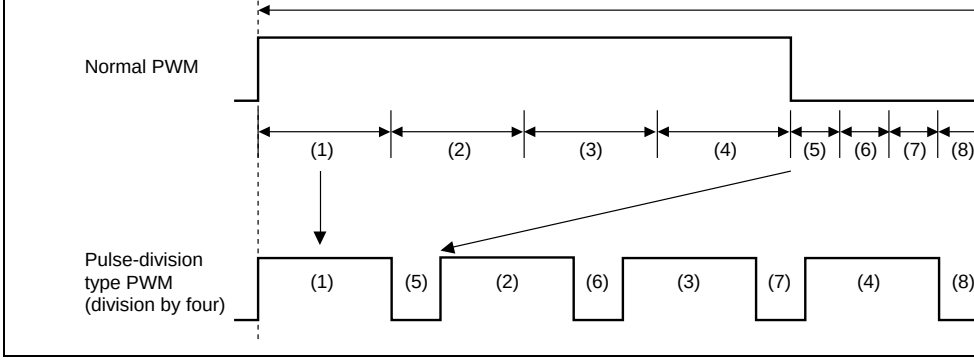


Figure 17.2 Example of Pulse-Division Type PWM Using Division by Four

17.4.2 Pulse-Division Type PWM Setting Method

When using the pulse-division type PWM, set the registers in this sequence:

1. Set the PWM1 or PWM2 bit in PMR9 (corresponding to the PWM channel used) to 1 the P90/PWM1 or P91/PWM2 pin to function as a PWM pin.
2. Set PWCR to define one conversion period.
3. Set the output waveform data in PWDR. When the data is written to PWDR, the cont latched in the PWM waveform generator, and the PWM waveform generation data is

17.4.3 Pulse-Div ision Type PWM Operating

One conversion period consists of 64 pulses, as shown in figure 17.3. The total high-level during this period (T_H) corresponds to the data in PWDR. Table 17.2 shows this relation.

Table 17.2 Correspondence Between PWCR, PWRD, and Output Waveform

PWCRm Setting Value		One Conversion	T_H	$t_{fn\ (n =$
PWCRm1	PWCRm0	Period [tcyc]	[tcyc]	[tcy
0	0	16384	(PWDRm+64) * 1	256
0	1	32768	(PWDRm+64) * 2	512
1	0	65536	(PWDRm+64) * 4	1024
1	1	131072	(PWDRm+64) * 8	2048

Note: m = 2, 1

17.4.4 Setting for Standard PWM Operation

When using the standard PWM, set the registers in this sequence:

1. Set the PWM1 or PWM2 bit in PMR9 (according to the PWM channel used) to 1 to P90/PWM1 or P91/PWM2 pin to function as a PWM pin.
2. Set PWCRm2 to 1 to select the standard PWM waveform. (m = 2 or 1)
3. Set the event counter PWM in the asynchronous event counter. For the setting metho description of the event counter PWM operation in the asynchronous event counter.
4. The PWM pin outputs the PWM waveform set by the event counter.

Note: When the standard waveform is used, 16-bit counter operation, 8-bit counter ope and IRQAEC operation for the asynchronous event counter are not available bec PWM for the asynchronous event counter is used.
When the IECPWM signal of the asynchronous event counter goes high, ECH a increment. However, when the signal goes low, these counters stop. (For details section 13.4, Operation.)

* Write-enabled

17.6 Usage Notes

17.6.1 Timing of Effect on PWM Waveform After Writing to PWDR

If PWDR is rewritten during PWM waveform output, the effects on the PWM waveform follows, depending on the timing of the write operation:

(1) Write performed during low-level output.
New setting takes effect from next pulse.

(2) Write performed during low-level output.
a. Duty increased.
New setting takes effect immediately after write.
b. Duty decreased.
- High width at time of write exceeds PWDR high width after write.
High-level output for one pulse period.
- High width at time of write does not exceed PWDR high width after write.
New setting takes effect immediately after write.

- High-speed conversion: 12.4 µs per channel (at 5-MHz operation)
- Sample and hold function
- Conversion start method

  A/D conversion can be started by software and external trigger.
- Interrupt source

  An A/D conversion end interrupt request can be generated.
- Use of module standby mode enables this module to be placed in standby mode inde when not used. (For details, refer to section 6.4, Module Standby Function.)

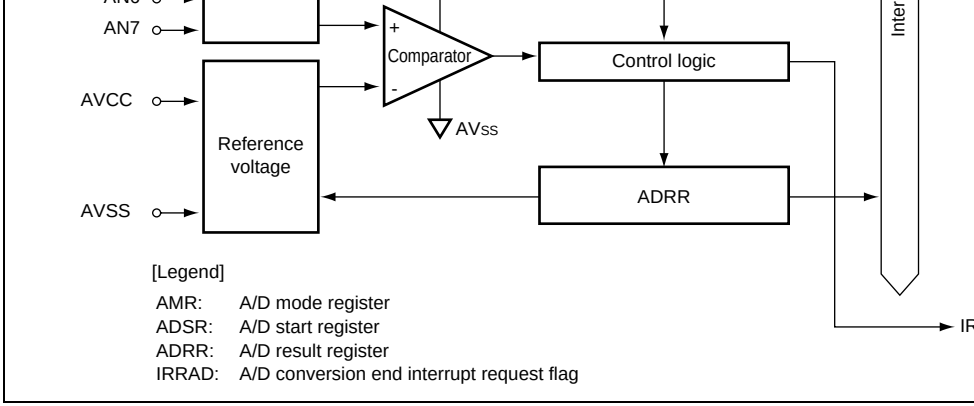


Figure 18.1 Block Diagram of A/D Converter

Analog input pin 0	AN0	Input	Analog input pins
Analog input pin 1	AN1	Input	
Analog input pin 2	AN2	Input	
Analog input pin 3	AN3	Input	
Analog input pin 4	AN4	Input	
Analog input pin 5	AN5	Input	
Analog input pin 6	AN6	Input	
Analog input pin 7	AN7	Input	
External trigger input pin	$\overline{\text{ADTRG}}$	Input	External trigger input that cont A/D conversion start.

18.3 Register Descriptions

The A/D converter has the following registers.

- A/D result register (ADRR)
- A/D mode register (AMR)
- A/D start register (ADSR)

18.3.1 A/D Result Register (ADRR)

ADRR is a 16-bit read-only register that stores the results of A/D conversion. The upper the data are stored in ADRR. ADRR can be read by the CPU at any time, but the ADRR during A/D conversion is undefined. After A/D conversion is completed, the conversion stored as 10-bit data, and this data is retained until the next conversion operation starts. value of ADRR is undefined.

Always read this register in word size.

				4))
6	TRGE	0	R/W	External Trigger Select Enables or disables the A/D conversion start by external trigger input. 0: Disables the A/D conversion start by the exte trigger input. 1: Starts A/D conversion at the rising or falling the $\overline{\text{ADTRG}}$ pin The edge of the $\overline{\text{ADTRG}}$ pin is selected by the ADTRGNEG bit in IEGR.
5	—	1	—	Reserved
4	—	1	—	These bits are always read as 1 and cannot be modified.
3	CH3	0	R/W	Channel Select 3 to 0
2	CH2	0	R/W	Select the analog input channel.
1	CH1	0	R/W	00xx: No channel selected
0	CH0	0	R/W	0100: AN0 0101: AN1 0110: AN2 0111: AN3 1000: AN4 1001: AN5 1010: AN6 1011: AN7 11xx: Using prohibited The channel selection should be made while th bit is cleared to 0.

[Legend] x: Don't care.

These bits are always read as 1 and cannot b
modified.

18.4 Operation

The A/D converter operates by successive approximation with 10-bit resolution. When c
the conversion time or analog input channel, in order to prevent incorrect operation, firs
bit ADSF to 0 in ADSR.

18.4.1 A/D Conversion

1. A/D conversion is started from the selected channel when the ADSF bit in ADSR is
   according to software.
2. When A/D conversion is completed, the result is transferred to the A/D result regist
3. On completion of conversion, the IRRAD flag in IRR2 is set to 1. If the IENAD bit
   is set to 1 at this time, an A/D conversion end interrupt request is generated.
4. The ADSF bit remains set to 1 during A/D conversion. When A/D conversion ends,
   ADSF bit is automatically cleared to 0 and the A/D converter enters the wait state.

the $\overline{\text{ADTRG}}$ pin, reset should be cleared while the 0-fixed or 1-fixed signal is
the TEST pin. Then the ADTSTCHG bit should be set to 1 after the TEST sig
fixed.

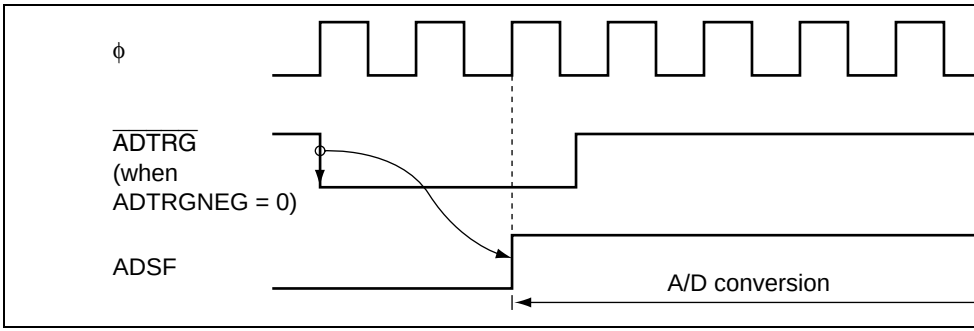


Figure 18.2 External Trigger Input Timing

18.4.3 Operating States of A/D Converter

Table 18.2 shows the operating states of the A/D converter.

Table 18.2 Operating States of A/D Converter

Operating Mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	M S
AMR	Reset	Functions	Functions	Retained	Retained	Retained	Retained	R
ADSR	Reset	Functions	Functions	Retained	Retained	Retained	Retained	R
ADRR	Retained*	Functions	Functions	Retained	Retained	Retained	Retained	R

Note: * Undefined at a power-on reset.

idle state.

3. Bit IENAD = 1, so an A/D conversion end interrupt is requested.
4. The A/D interrupt handling routine starts.
5. The A/D conversion result is read and processed.
6. The A/D interrupt handling routine ends.

If bit ADSF is set to 1 again afterward, A/D conversion starts and steps 2 through 6 take

Figures 18.4 and 18.5 show flowcharts of procedures for using the A/D converter.

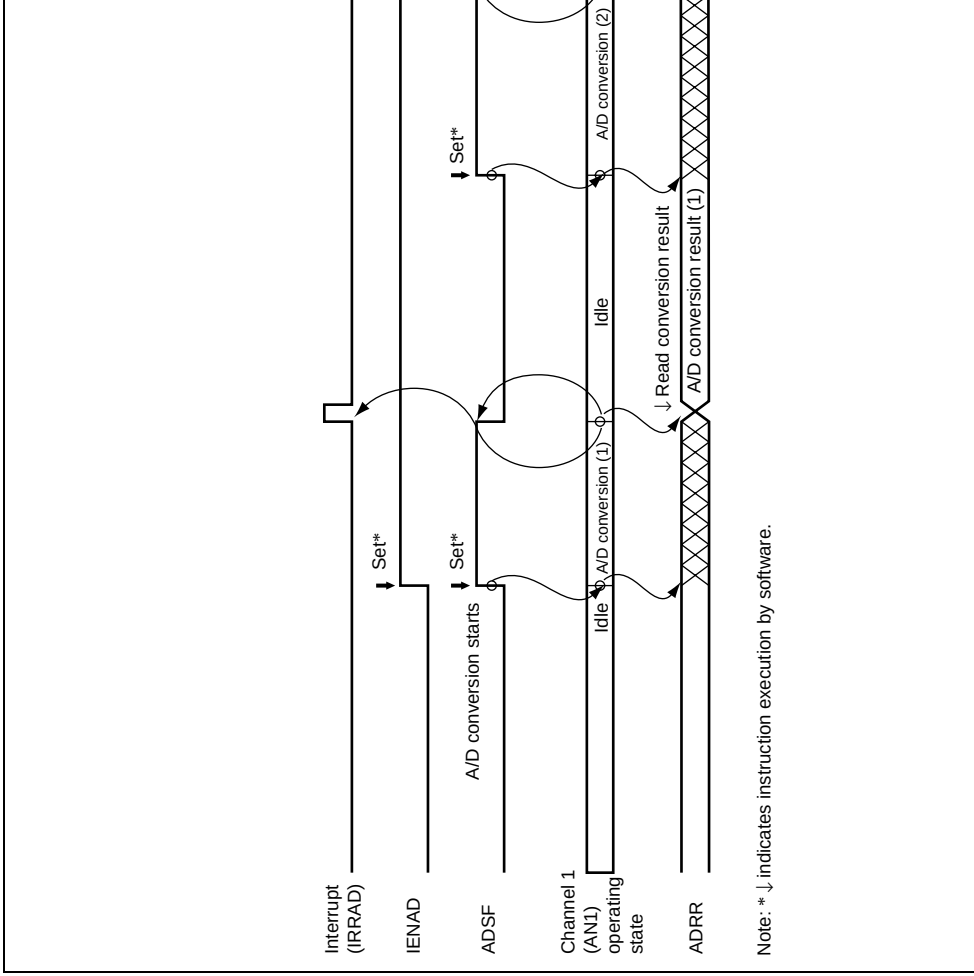


Figure 18.3 Example of A/D Conversion Operation

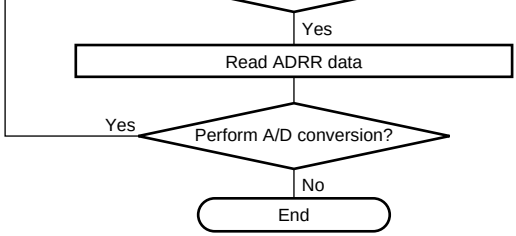


Figure 18.4 Flowchart of Procedure for Using A/D Converter (Polling by Soft

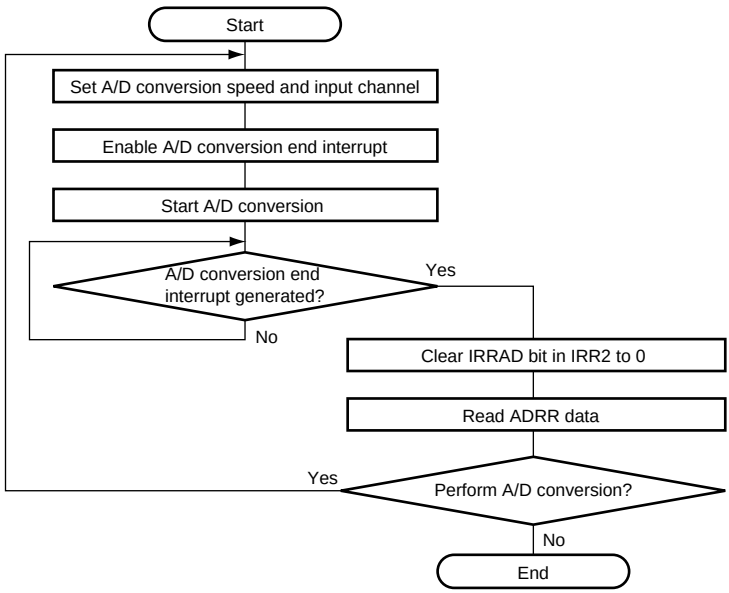


Figure 18.5 Flowchart of Procedure for Using A/D Converter (Interrupts U

when the digital output changes from the minimum voltage value 0000000000 to 000
(see figure 18.7).

- Full-scale error

  The deviation of the analog input voltage value from the ideal A/D conversion charac
  when the digital output changes from 1111111110 to 1111111111 (see figure 18.7).

- Nonlinearity error

  The error with respect to the ideal A/D conversion characteristics between zero voltag
  full-scale voltage. Does not include offset error, full-scale error, or quantization error.

- Absolute accuracy

  The deviation between the digital value and the analog input value. Includes offset er
  scale error, quantization error, and nonlinearity error.

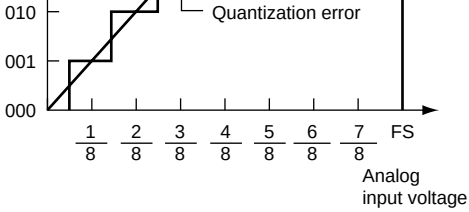


Figure 18.6 A/D Conversion Accuracy Definitions (1)

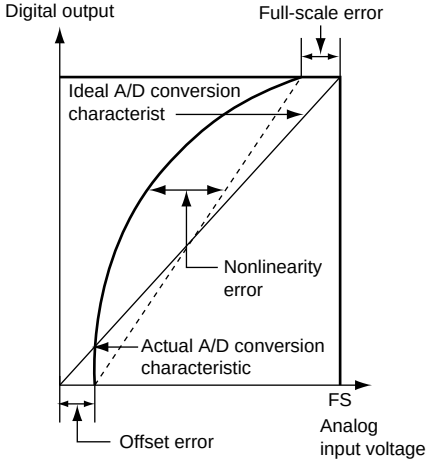


Figure 18.7 A/D Conversion Accuracy Definitions (2)

this case, it may not be possible to follow an analog signal with a large differential coeffi
(e.g., 5 mV/µs or greater) (see figure 18.8).

When converting a high-speed analog signal, a low-impedance buffer should be inserted.

18.7.2 Influences on Absolute Accuracy

Adding capacitance results in coupling with GND, and therefore noise in GND may adve
affect absolute accuracy. Be sure to make the connection to an electrically stable GND.

Care is also required to ensure that filter circuits do not interfere with digital signals or ac
antennas on the mounting board.

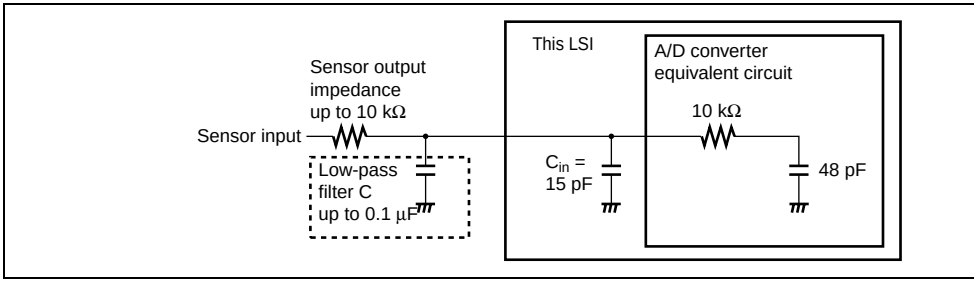
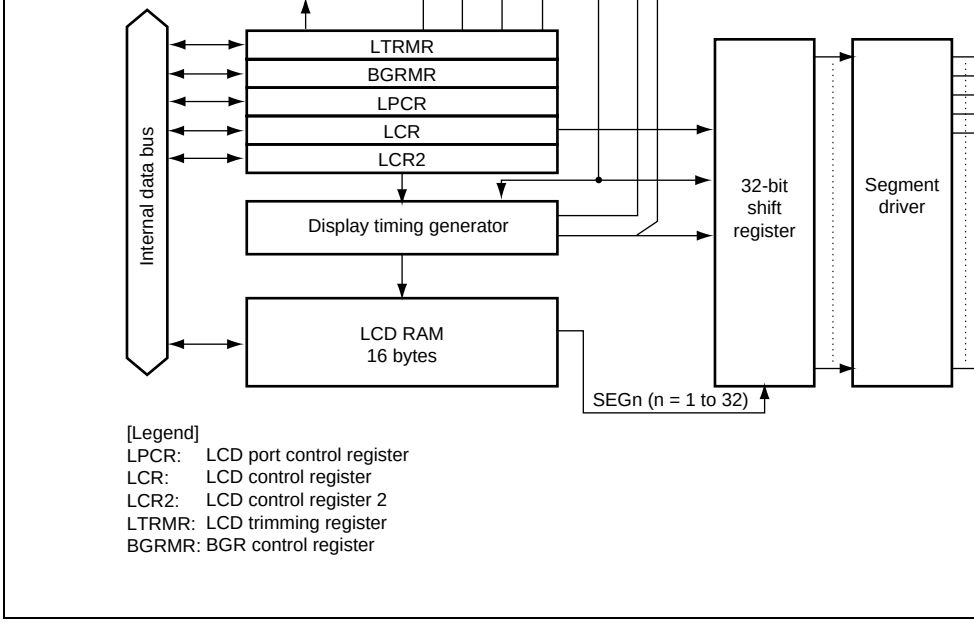


Figure 18.8 Example of Analog Input Circuit

cleared to 0 in CKSTPR1.

Static	32 SEG
1/2	32 SEG
1/3	32 SEG
1/4	32 SEG

- LCD RAM capacity
  8 bits × 16 bytes (128 bits)
- Word access to LCD RAM
- The segment output pins can be used as ports.
  SEG32 to SEG1 pins can be used as ports in groups of four.
- Common output pins not used because of the duty cycle can be used for common do
  buffering (parallel connection).
  With 1/2 duty, parallel connection of COM1 to COM2, and of COM3 to COM4, can
  In static mode, parallel connection of COM1 to COM2, COM3, and COM4 can be u
- Choice of 11 frame frequencies
- A or B waveform selectable by software
- On-chip power supply split-resistor
- Display possible in operating modes other than standby mode
- On-chip 3-V constant-voltage power supply circuit
  This power circuit can constantly supply 3 V to LCD drive power supply without us
  voltage.
- Output of the 3-V constant-voltage power supply circuit adjustable
- Use of module standby mode enables this module to be placed in standby mode inde
  when not used. (For details, refer to section 6.4, Module Standby Function.)



[Legend]
LPCR: LCD port control register
LCR: LCD control register
LCR2: LCD control register 2
LTRMR: LCD trimming register
BGRMR: BGR control register

Figure 19.1 Block Diagram of LCD Controller/Driver

pins			Pins can be used in parallel with static 1/2 duty
LCD power supply pins	V1, V2, V3	—	Used when a bypass capacitor is conn externally, and when an external powe circuit is used
LCD step-up capacitance pins	C1, C2	—	Capacitance pins for stepping up the l power supply

19.3 Register Descriptions

The LCD controller/driver has the following registers.

- LCD port control register (LPCR)
- LCD control register (LCR)
- LCD control register 2 (LCR2)
- LCD trimming register (LTRMR)
- BGR control register (BGRMR)
- LCDRAM

				increase the common drive power when not all common pins are used because of the duty se For details, see table 19.2.
4	—	—	W	Reserved Only 0 can be written to this bit.
3	SGS3	0	R/W	Segment Driver Select 3 to 0
2	SGS2	0	R/W	Select the segment drivers to be used.
1	SGS1	0	R/W	For details, see table 19.3.
0	SGS0	0	R/W	

Table 19.2 Duty Cycle and Common Function Selection

Bit 7: DTS1	Bit 6: DTS0	Bit 5: CMX	Duty Cycle	Common Drivers	Notes*
0	0	0	Static	COM1	Leave COM4, COM3, and COM2 in ope state
		1		COM4 to COM1	COM4, COM3, and COM2 output the sa waveform as COM1
	1	0	1/2 duty	COM2 to COM1	Leave COM4 and COM3 in open drain s
		1		COM4 to COM1	COM4 outputs the same waveform as C COM2 outputs the same waveform as C
1	0	0	1/3 duty	COM3 to COM1	Leave COM4 in open drain state
		1		COM4 to COM1	Leave COM4 in open drain state
	1	0	1/4 duty	COM4 to COM1	—
		1			

Note: * If SGS3 to SGS0 are set to B'0000, the power supply voltage level of PA0 to PA3 and COM COM4 is Vcc. If the setting of SGS3 to SGS0 is other than B'0000, the power supply voltage PA0 to PA3 and COM1 to COM4 is the LCD drive power supply voltage level.

		1	0	Port	Port	SEG	SEG	SEG	SEG	SEG
			1	Port	SEG	SEG	SEG	SEG	SEG	SEG
1	0	0	0	SEG	SEG	SEG	SEG	SEG	SEG	SEG
			1	SEG	SEG	SEG	SEG	SEG	SEG	SEG
		1	0	SEG	SEG	SEG	SEG	SEG	SEG	Port
			1	SEG	SEG	SEG	SEG	SEG	Port	Port
	1	0	0	SEG	SEG	SEG	SEG	Port	Port	Port
			1	SEG	SEG	SEG	Port	Port	Port	Port
		1	0	SEG	SEG	Port	Port	Port	Port	Port
			1	SEG	Port	Port	Port	Port	Port	Port

19.3.2 LCD Control Register (LCR)

LCR controls LCD drive power supply and display data, and selects the frame frequency

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	—	Reserved This bit is always read as 1 and cannot be mo
6	PSW	0	R/W	LCD Drive Power Supply Control Can be used to turn off the LCD drive power s when LCD display is not required in power-do or when an external power supply is used. Wh ACT bit is cleared to 0 or in standby mode, the drive power supply is turned off regardless of of this bit. 0: LCD drive power supply is turned off 1: LCD drive power supply is turned on

				Specifies whether the LCD RAM contents are d or blank data is displayed regardless of the LCI contents. 0: Blank data is displayed 1: LCD RAM data is displayed
3	CKS3	0	R/W	Frame Frequency Select 3 to 0
2	CKS2	0	R/W	Select the operating clock and the frame freque However, in subactive mode, watch mode, and subsleep mode, the system clock (ϕ) is halted. Therefore display operations are not performed the clocks from ϕ/2 to ϕ/256 is selected. If LCD is required in these modes, ϕ_w, ϕ_w/2, or ϕ_w/4 mu selected as the operating clock. For details, see table 19.4.
1	CKS1	0	R/W	
0	CKS0	0	R/W	

		1	ϕ/16	244 Hz	30.5 H
1	0	0	ϕ/32	122 Hz	—
		1	ϕ/64	61 Hz	—
	1	0	ϕ/128	30.5 Hz	—
		1	ϕ/256	—	—

[Legend]

X: Don't care

Notes: 1. When 1/3 duty is selected, the frame frequency is 4/3 times the value shown.

2. This is the frame frequency when ϕ_w = 32.768 kHz.

3. This is the frame frequency in active (medium-speed, ϕ_{osc}/8) mode when ϕ_{osc}

19.3.3 LCD Control Register 2 (LCR2)

LCR2 controls switching between the A waveform and B waveform, selection of the ste for the 3-V constant-voltage circuit, connection with the LCD power-supply split resisto turning on or off 3-V constant-voltage power supply.

				voltage power supply circuit. The step-up clock obtained by dividing the clock selected by the C CKS0 bits in LCR into 4 or 8. 0: Divided into 4 1: Divided into 8
5	CHG	0	R/W	Connection Control of LCD Power-Supply Split Selects whether an LCD power-supply split res disconnected or connected from or to LCD driv supply. 0: Disconnected 1: Connected
4	SUPS	0	R/W	3-V Constant-Voltage Power Supply Control Can be used to turn off the 3-V constant-voltag supply when LCD display is not required in pow mode, or when an external power supply is use the BGRSTPN bit in BGRMR is cleared to 0 or standby mode, the 3-V constant-voltage power turned off regardless of the setting of this bit. 0: 3-V constant-voltage power supply is turned 1: 3-V constant-voltage power supply is turned
3 to 0	—	—	W	Reserved Only 0 can be written to these bits.

4	TRM0	0	R/W	3 V. Following values* indicate the voltage of pin. Set this register so that the voltage on the should be 3 V. 0000: ±0 V 1000: 0.48 V 0001: -0.06 V 1001: 0.42 V 0010: -0.12 V 1010: 0.36 V 0011: -0.15 V 1011: 0.30 V 0100: -0.21 V 1100: 0.24 V 0101: -0.24 V 1101: 0.18 V 0110: -0.30 V 1110: 0.12 V 0111: -0.33 V 1111: 0.06 V
3	—	1	—	Reserved This bit is always read as 1 and cannot be mo

010: 0.18 V

011: 0.27 V

100: -0.36 V

101: -0.27 V

110: -0.18 V

111: -0.09 V

Notes: Setting Method for LCD Trimming Register (LTRMR)
Assuming the following definitions,

V1 initial state voltage: A

LTRMR register TRM3 to TRM0: B

CTRM2 to CTRM0: C

rough guidelines for the voltages after trimming are as follows:

V1 voltage = A + B + C

V2 voltage = (A + B + C) × 2/3

V3 voltage = (A + B + C) / 3

After monitoring voltage A, set B and C so the V1 voltage is 3 V.

* These are approximate values and are not guaranteed. Therefore these value
be used as reference values.

				0: Band-gap reference circuit halts 1: Band-gap reference circuit operates
6 to 3	—	All 1	—	Reserved These bits are always read as 1 and cannot b modified.
2 to 0	—	All 0	R/W	Reserved This bit is always read as 0, and only 0 can be it.

When 1/2 duty is used, interconnect pins V2 and V3 as shown in figure 19.2.

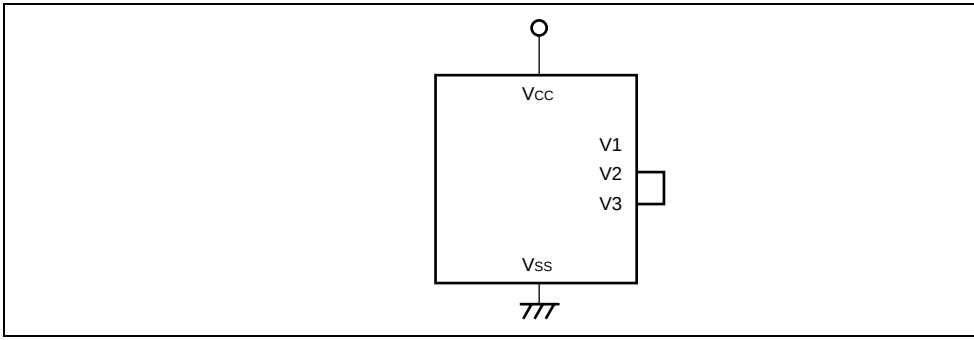


Figure 19.2 Handling of LCD Drive Power Supply when Using 1/2 Duty

(b) Large-Panel Display

As the impedance of the on-chip power supply split-resistor is large, it may not be suitabl
driving a panel which requires a current more than the current value calculated by the on-
power supply split-resistor and voltage of the LCD power supply. If the display lacks sha
when using a large panel, refer to section 19.4.5, Boosting LCD Drive Power Supply and
Adjustment. When static or 1/2 duty is selected, the common output drive capability can
increased. Set CMX to 1 when selecting the duty cycle. In this mode, with a static duty cy
COM4 to COM1 output the same waveform, and with 1/2 duty the COM1 waveform is o
from pins COM2 and COM1, and the COM2 waveform is output from pins COM4 and C

(c) LCD Drive Power Supply Setting

With this LSI, there are two ways of providing LCD power: by using the on-chip power s
circuit, or by using an external power supply circuit.

The segment drivers to be used can be selected with bits SGS3 to SGS0.

(c) Frame Frequency Selection

The frame frequency can be selected by setting bits CKS3 to CKS0. The frame frequenc
be selected in accordance with the LCD panel specification. For the clock selection meth
watch mode, subactive mode, and subsleep mode, see section 19.4.4, Operation in Powe
Modes.

(d) A or B Waveform Selection

Either the A or B waveform can be selected as the LCD waveform to be used by means
LCDAB.

(e) LCD Drive Power Supply Selection

When an external power supply circuit is used, turn the LCD drive power supply off wit
bit.

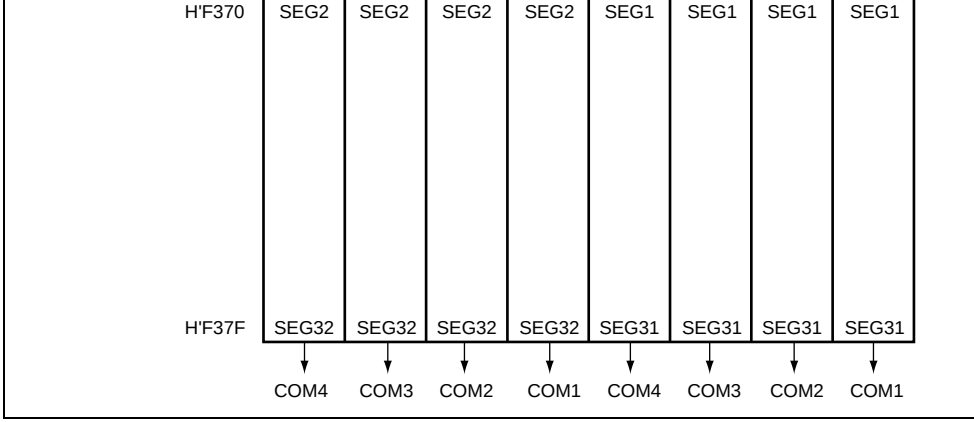


Figure 19.3 LCD RAM Map (1/4 Duty)

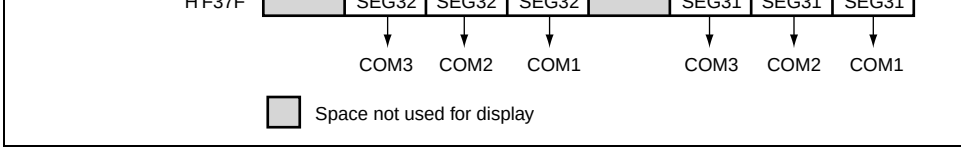


Figure 19.4 LCD RAM Map (1/3 Duty)

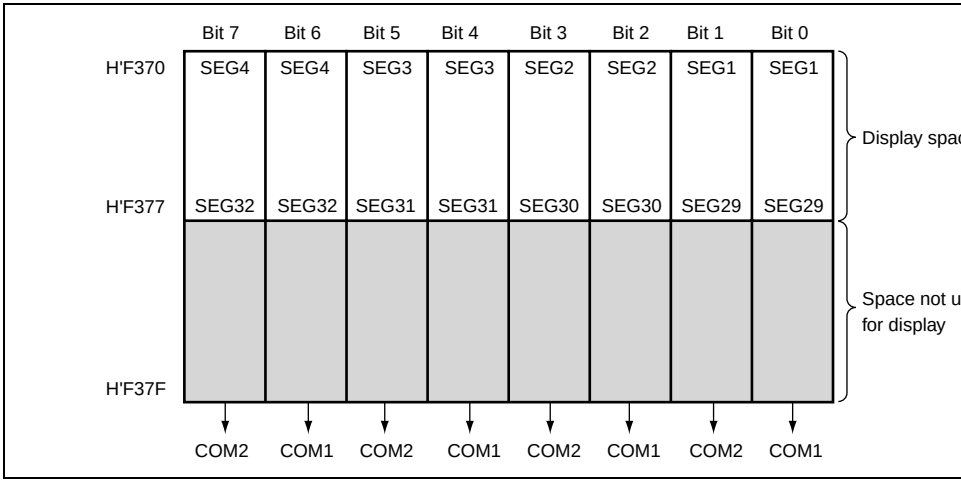


Figure 19.5 LCD RAM Map (1/2 Duty)

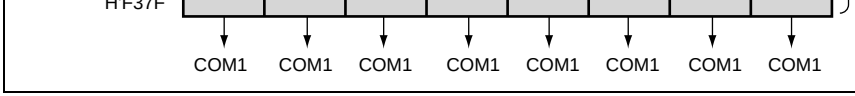


Figure 19.6 LCD RAM Map (Static Mode)

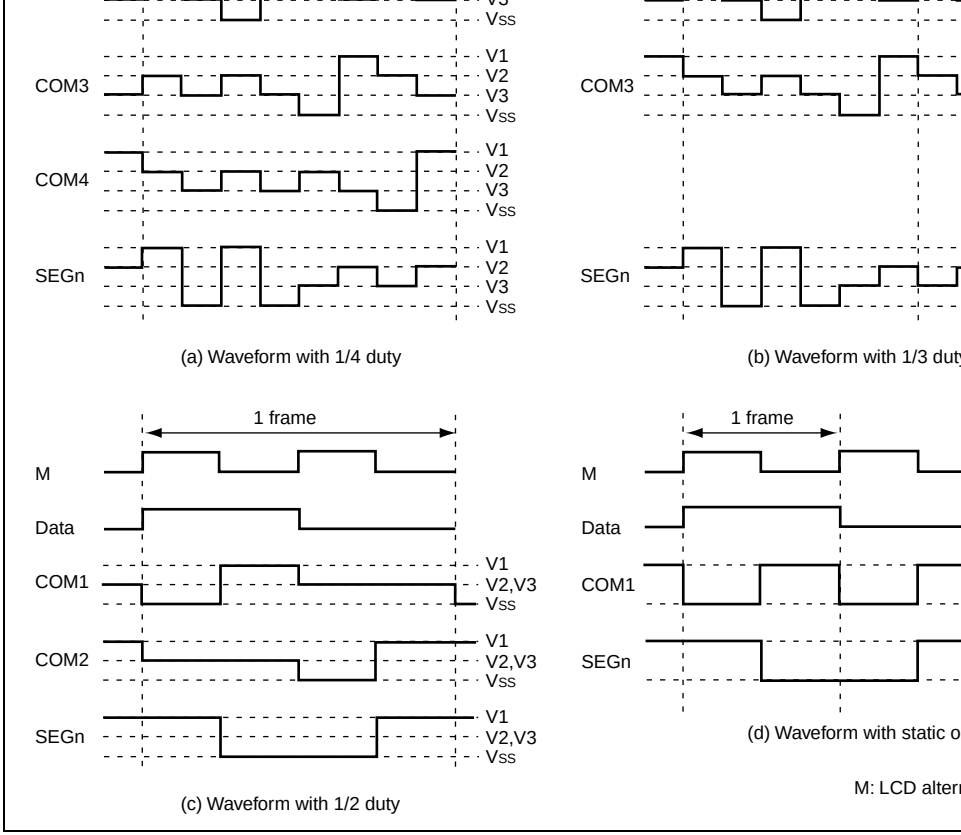


Figure 19.7 Output Waveforms for Each Duty Cycle (A Waveform)

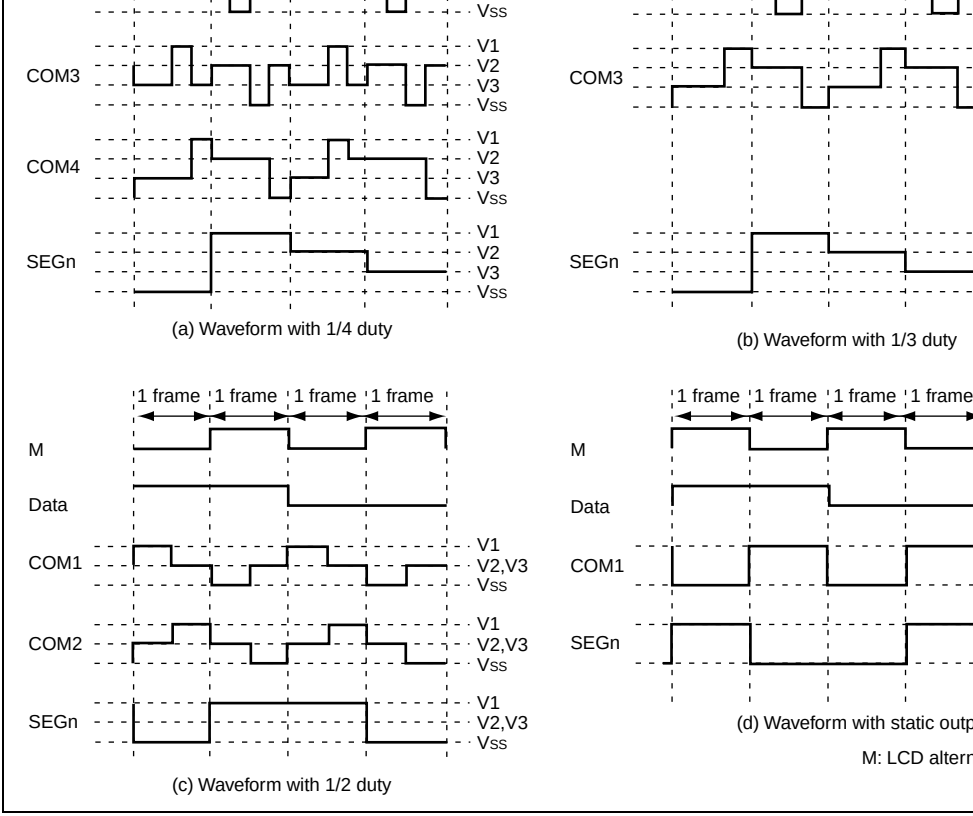


Figure 19.8 Output Waveforms for Each Duty Cycle (B Waveform)

1/3 duty	Common output	V3	V2	V1	VSS
	Segment output	V2	V3	VSS	V1
1/4 duty	Common output	V3	V2	V1	VSS
	Segment output	V2	V3	VSS	V1

M: LCD alternation signal

19.4.3 3-V Constant-Voltage Power Supply Circuit

This LSI incorporates a 3-V constant-voltage power supply circuit consisting of a band g reference circuit (BGR), a triple step-up circuit, etc. This allows the 3 V constant voltag LCD driver independently of Vcc.

Before activating a step-up circuit, LCD controller/driver operates and set the duty cycle function of the LCD driver or I/O, display data, frame frequencies, etc. Insert a capacitar µF between the C1 pin and C2 pin, and connect a capacitance of 0.1 µF to each of V1, V pins. (See figure 19.9.)

After this setting, setting the BGRSTPN bit in the BGR control register (BGRMR) to 1 the band gap reference circuit, generating 1 V constant voltage (V_{LCD3}) at the V3 pin. Fur selecting the step-up circuit clock of the LCD control register 2 (LCR2) and setting the S to 1 activates the triple step-up circuit, generating 2 V constant voltage, twice V_{LCD3}, at th and generating 3 V constant voltage, triple V_{LCD3}, at the V1 pin.

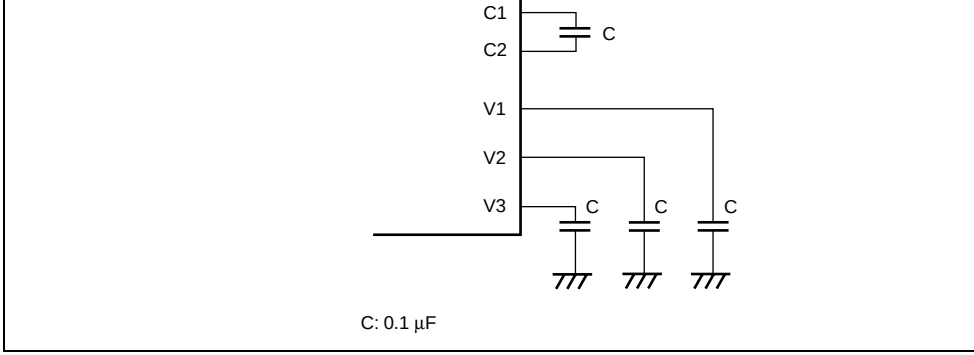


Figure 19.9 Capacitance Connection when Using 3-V Constant-Voltage Power Supply Circuit

19.4.4 Operation in Power-Down Modes

In this LSI, the LCD controller/driver can be operated even in the power-down modes. Th operating state of the LCD controller/driver in the power-down modes is summarized in t 19.6.

In subactive mode, watch mode, and subsleep mode, the system clock oscillator stops, an therefore, unless ϕ_w, $\phi_w/2$, or $\phi_w/4$ has been selected by bits CKS3 to CKS0, the clock wil supplied and display will halt. The subclock can be turned on or off by setting the 32KST the SUB32K control register (SUB32CR). When it is turned off, display will halt. Since t possibility that a direct current will be applied to the LCD panel in this case, it is essentia ensure that the subclock is turned on and ϕ_w, $\phi_w/2$, or $\phi_w/4$ is selected.

In active (medium-speed) mode, the system clock is switched, and therefore bits CKS3 to must be modified to ensure that the frame frequency does not change.

3. Display operation is performed only if ϕ_W, $\phi_W/2$, or $\phi_W/4$ is selected as the oper clock.
4. The clock supplied to the LCD stops.
5. When the 32KSTOP bit in SUB32CR is set to 1, the subclock ϕ_W halts and dis operation halts.

19.4.5 Boosting LCD Drive Power Supply and Fine Adjustment

When a large panel is driven, the on-chip power supply capacity may be insufficient. In the power supply impedance must be reduced. This can be done by connecting bypass c of around 0.1 to 0.3 µF to pins V1 to V3, as shown in figure 19.10, or by adding a split r externally. The voltage on the V1 pin can further be adjusted by connecting a variable re (VR) between the V_{CC} and V1 pins.

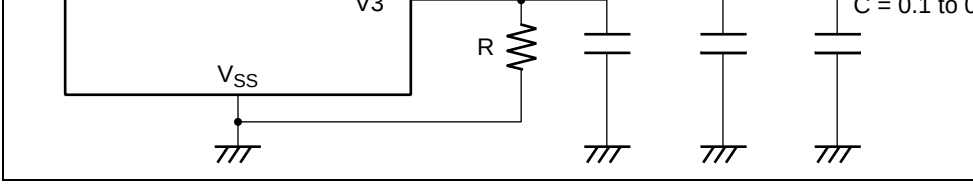


Figure 19.10 Connection of External Split Resistor

19.5 Usage Notes

19.5.1 Pin Processing when No LCD Controller/Driver Is Used

(1) V1, V2, V3

Connect to GND. In this case, CHG in LCR2 should not be changed from its initial va
(LCD power-supply split resistor disconnected).

(2) C1, C2

Leave open.

19.5.2 Pin Processing when No 3 V Constant Voltage Circuit Is Used

Leave pins C1 and C2 open.

- Continuous transmission/reception

  Since the shift register, transmit data register, and receive data register are independe each other, the continuous transmission/reception can be performed.
- Use of module standby mode enables this module to be placed in standby mode inde when not used. (For details, refer to section 6.4, Module Standby Function.)

I^2C bus format

- Start and stop conditions generated automatically in master mode
- Selection of acknowledge output levels when receiving
- Automatic loading of acknowledge bit when transmitting
- Bit synchronization/wait function

  In master mode, the state of SCL is monitored per bit, and the timing is synchronize automatically.

  If transmission/reception is not yet possible, set the SCL to low until preparations ar completed.
- Six interrupt sources

  Transmit data empty (including slave-address match), transmit end, receive data full slave-address match), arbitration lost, NACK detection, and stop condition detection
- Direct bus drive

  Two pins, SCL and SDA pins, function as CMOS outputs in normal operation (wher port/serial function is selected) and NMOS outputs when the bus drive function is se

Clocked synchronous format

- Four interrupt sources

  Transmit-data-empty, transmit-end, receive-data-full, and overrun error

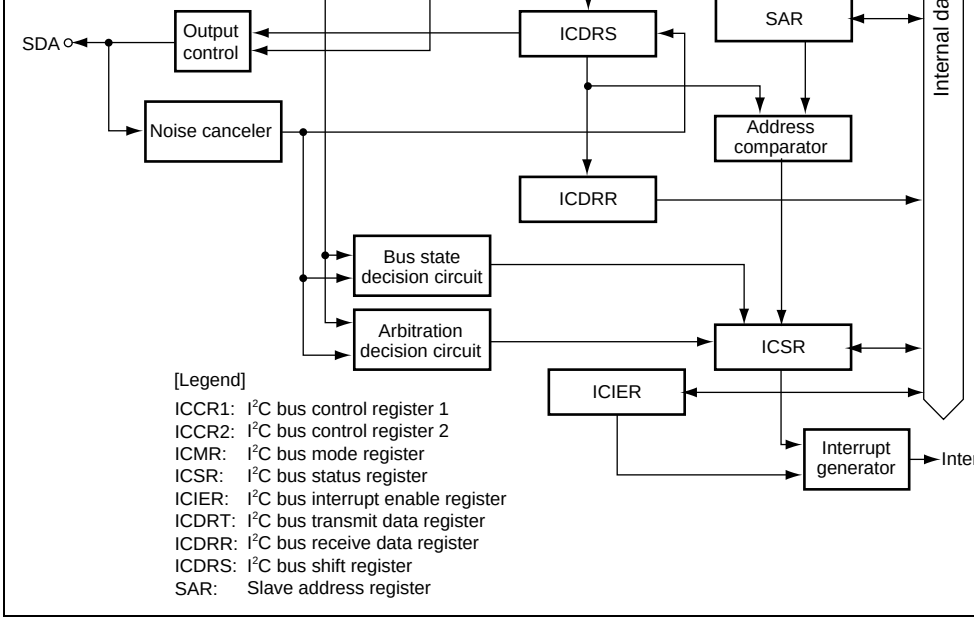


Figure 20.1 Block Diagram of I²C Bus Interface 2

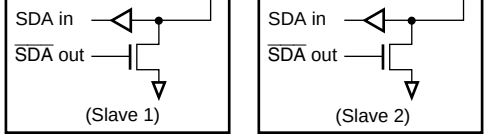


Figure 20.2 External Circuit Connections of I/O Pins

20.2 Input/Output Pins

Table 20.1 summarizes the input/output pins used by the I^2C bus interface 2.

Table 20.1 Pin Configuration

Name	Abbreviation	I/O	Function
Serial clock pin	SCL	I/O	IIC serial clock input/output
Serial data pin	SDA	I/O	IIC serial data input/output

- I²C bus transmit data register (ICDRT)
- I²C bus receive data register (ICDRR)
- I²C bus shift register (ICDRS)

20.3.1 I²C Bus Control Register 1 (ICCR1)

ICCR1 enables or disables the I²C bus interface 2, controls transmission or reception, and
master or slave mode, transmission or reception, and transfer clock frequency in master m

Bit	Bit Name	Initial Value	R/W	Description
7	ICE	0	R/W	I2C Bus Interface Enable 0: This module is halted. (SCL and SDA pins a the port/serial function.) 1: This bit is enabled for transfer operations. (S SDA pins are bus drive state.)
6	RCVD	0	R/W	Reception Disable This bit enables or disables the next operation TRS is 0 and ICDRR is read. 0: Enables next reception 1: Disables next reception

				agree with the slave address that is set to SA eighth bit is 1, TRS is automatically set to 1. overrun error occurs in master mode with the synchronous serial format, MST is cleared to slave receive mode is entered. Operating modes are described below accord MST and TRS combination. When clocked sy serial format is selected and MST is 1, clock i 00: Slave receive mode 01: Slave transmit mode 10: Master receive mode 11: Master transmit mode
3	CKS3	0	R/W	Transfer Clock Select 3 to 0 In master mode, set these bits according to th necessary transfer rate (see table 20.2, Trans In slave mode, these bits are used to secure t setup time in transmission mode. When CKS3 data setup time is 10 tcyc and when CKS3 = setup time is 20 tcyc.
2	CKS2	0	R/W	
1	CKS1	0	R/W	
0	CKS0	0	R/W	

		1	0	φ/112	17.9 kHz	44.6 kHz	89.3
			1	φ/128	15.6 kHz	39.1 kHz	78.1
1	0	0	0	φ/56	35.7 kHz	89.3 kHz	179
			1	φ/80	25.0 kHz	62.5 kHz	125
		1	0	φ/96	20.8 kHz	52.1 kHz	104
			1	φ/128	15.6 kHz	39.1 kHz	78.1
	1	0	0	φ/160	12.5 kHz	31.3 kHz	62.5
			1	φ/200	10.0 kHz	25.0 kHz	50.0
		1	0	φ/224	8.9 kHz	22.3 kHz	44.6
			1	φ/256	7.8 kHz	19.5 kHz	39.1

				format, this bit has no meaning. With the I2C format, this bit is set to 1 when the SDA level from high to low under the condition of SCL = assuming that the start condition has been iss bit is cleared to 0 when the SDA level change to high under the condition of SCL = high, ass that the stop condition has been issued. Write BBSY and 0 to SCP to issue a start condition this procedure when also re-transmitting a sta condition. Write 0 in BBSY and 0 in SCP to is condition. To issue start/stop conditions, use instruction.
6	SCP	1	R/W	Start/Stop Issue Condition Disable The SCP bit controls the issue of start/stop co master mode. To issue a start condition, write 1 in BBSY an SCP. A retransmit start condition is issued in way. To issue a stop condition, write 0 in BBS SCP. This bit is always read as 1. If 1 is writte data is not stored.
5	SDAO	1	R/W	SDA Output Value Control This bit is used with SDAOP when modifying level of SDA. This bit should not be manipulat transfer. 0: When reading, SDA pin outputs low. When writing, SDA pin is changed to outpu 1: When reading, SDA pin outputs high. When writing, SDA pin is changed to outpu (outputs high by external pull-up resistance

2	—	1	—	Reserved This bit is always read as 1, and cannot be mo
1	IICRST	0	R/W	IIC Control Part Reset This bit resets the control part except for I2C re If this bit is set to 1 when hang-up occurs beca communication failure during I2C operation, I2 part can be reset without setting ports and initia registers.
0	—	1	—	Reserved This bit is always read as 1, and cannot be mo

				Set this bit to 0 when the I2C bus format is us
6	WAIT	0	R/W	Wait Insertion Bit In master mode with the I2C bus format, this whether to insert a wait after data transfer exc acknowledge bit. When WAIT is set to 1, after the clock for the final data bit, low period is ex two transfer clocks. If WAIT is cleared to 0, da acknowledge bits are transferred consecutive wait inserted. The setting of this bit is invalid in slave mode I2C bus format or with the clocked synchrono format.
5, 4	—	All 1	—	Reserved These bits are always read as 1, and cannot modified.
3	BCWP	1	R/W	BC Write Protect This bit controls the BC2 to BC0 modifications modifying BC2 to BC0, this bit should be clea and use the MOV instruction. In clock synchro serial mode, BC should not be modified. 0: When writing, values of BC2 to BC0 are se 1: When reading, 1 is always read. When writing, settings of BC2 to BC0 are inva

the clock synchronous serial format, these bits
not be modified.

I2C Bus Format	Clock Synchronous Seri
000: 9 bits	000: 8 bits
001: 2 bits	001: 1 bits
010: 3 bits	010: 2 bits
011: 4 bits	011: 3 bits
100: 5 bits	100: 4 bits
101: 6 bits	101: 5 bits
110: 7 bits	110: 6 bits
111: 8 bits	111: 7 bits

				disabled. 1: Transmit data empty interrupt request (TXI) enabled.
6	TEIE	0	R/W	Transmit End Interrupt Enable This bit enables or disables the transmit end i (TEI) at the rising of the ninth clock while the in ICSR is 1. TEI can be canceled by clearing bit or the TEIE bit to 0. 0: Transmit end interrupt request (TEI) is disa 1: Transmit end interrupt request (TEI) is ena
5	RIE	0	R/W	Receive Interrupt Enable This bit enables or disables the receive data f interrupt request (RXI) and the overrun error i request (ERI) with the clocked synchronous fo when a receive data is transferred from ICDR ICDRR and the RDRF bit in ICSR is set to 1. be canceled by clearing the RDRF or RIE bit 0: Receive data full interrupt request (RXI) an error interrupt request (ERI) with the clocke synchronous format are disabled. 1: Receive data full interrupt request (RXI) an error interrupt request (ERI) with the clocke synchronous format are enabled.

3	STIE	0	R/W	Stop Condition Detection Interrupt Enable 0: Stop condition detection interrupt request (S disabled. 1: Stop condition detection interrupt request (S enabled.
2	ACKE	0	R/W	Acknowledge Bit Judgment Select 0: The value of the receive acknowledge bit is and continuous transfer is performed. 1: If the receive acknowledge bit is 1, continuo transfer is halted.
1	ACKBR	0	R	Receive Acknowledge In transmit mode, this bit stores the acknowled that are returned by the receive device. This bi be modified. 0: Receive acknowledge = 0 1: Receive acknowledge = 1
0	ACKBT	0	R/W	Transmit Acknowledge In receive mode, this bit specifies the bit to be the acknowledge timing. 0: 0 is sent at the acknowledge timing. 1: 1 is sent at the acknowledge timing.

				• When TRS is set • When a start condition (including re-transfer) has been issued • When transmit mode is entered from receive slave mode [Clearing conditions] • When 0 is written in TDRE after reading TDR • When data is written to ICDRT with an instru
6	TEND	0	R/W	Transmit End [Setting conditions] • When the ninth clock of SCL rises with the I^2 format while the TDRE flag is 1 • When the final bit of transmit frame is sent w clock synchronous serial format [Clearing conditions] • When 0 is written in TEND after reading TEN • When data is written to ICDRT with an instru
5	RDRF	0	R/W	Receive Data Register Full [Setting condition] • When a receive data is transferred from ICD ICDRR [Clearing conditions] • When 0 is written in RDRF after reading RDI • When ICDRR is read with an instruction

				• When a stop condition is detected after comp a frame transfer in master mode • When a stop condition is detected after the fir slave address and SAR match following a ge and detection of a start condition in slave mo [Clearing condition] • When 0 is written to STOP after reading 1
2	AL/OVE	0	R/W	Arbitration Lost Flag/Overrun Error Flag This flag indicates that arbitration was lost in mas with the I^2C bus format and that the final bit has b received while RDRF = 1 with the clocked synchr format. When two or more master devices attempt to sei bus at nearly the same time, if the I^2C bus interfa detects data differing from the data it sent, it sets to indicate that the bus has been taken by anothe [Setting conditions] • If the internal SDA and SDA pin disagree at th SCL in master transmit mode • When the SDA pin outputs high in master mo a start condition is detected • When the final bit is received with the clocked synchronous format while RDRF = 1 [Clearing condition] • When 0 is written in AL/OVE after reading AL

				receive mode. [Clearing condition] • When 0 is written in AAS after reading AAS=
0	ADZ	0	R/W	General Call Address Recognition Flag This bit is valid in I²C bus format slave receive m [Setting condition] • When the general call address is detected in receive mode [Clearing conditions] • When 0 is written in ADZ after reading ADZ=

20.3.6 Slave Address Register (SAR)

SAR selects the communication format and sets the slave address. When the chip is in s with the I²C bus format, if the upper 7 bits of SAR match the upper 7 bits of the first fra received after a start condition, the chip operates as the slave device.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	SVA6 to SVA0	All 0	R/W	Slave Address 6 to 0 These bits set a unique address in bits SVA6 differing form the addresses of other slave de connected to the I²C bus.
0	FS	0	R/W	Format Select 0: I²C bus format is selected. 1: Clocked synchronous serial format is selec

ICDRR is an 8-bit register that stores the receive data. When data of one byte is received, transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDI receive-only register, therefore the CPU cannot write to this register. The initial value of is H'FF.

20.3.9 I²C Bus Shift Register (ICDRS)

ICDRS is a register that is used to transfer/receive data. In transmission, data is transferre ICDRT to ICDRS and the data is sent from the SDA pin. In reception, data is transferred ICDRS to ICDRR after data of one byte is received. This register cannot be read directly CPU.

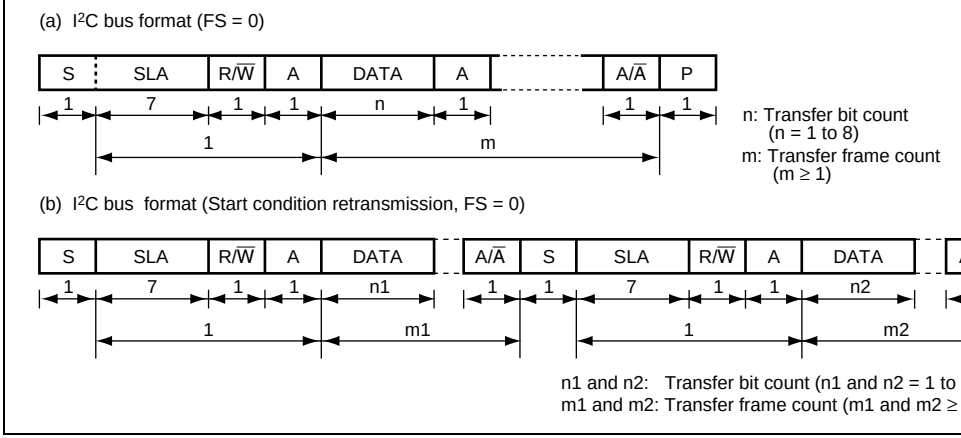


Figure 20.3 I²C Bus Formats

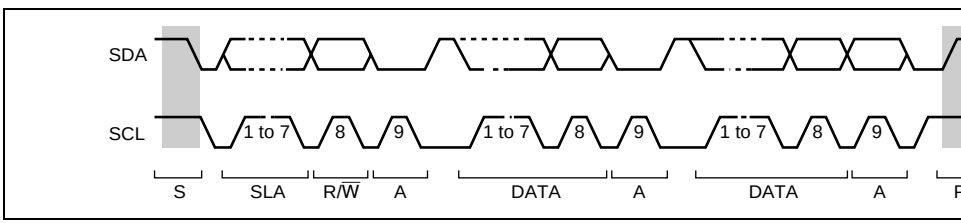


Figure 20.4 I²C Bus Timing

20.4.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and transmit data, a slave device returns an acknowledge signal. For master transmit mode operation timing, r figures 20.5 and 20.6. The transmission procedure and operations in master transmit mod described below.

1. Set the ICE bit in ICCR1 to 1. Set the MLS and WAIT bits in ICMR and the CKS3 to bits in ICCR1 to 1. (Initial setting)
2. Read the BBSY flag in ICCR2 to confirm that the bus is free. Set the MST and TRS b ICCR1 to select master transmit mode. Then, write 1 to BBSY and 0 to SCP using M instruction. (Start condition issued) This generates the start condition.
3. After confirming that TDRE in ICSR has been set, write the transmit data (the first by show the slave address and R/$\overline{W}$) to ICDRT. At this time, TDRE is automatically clea and data is transferred from ICDRT to ICDRS. TDRE is set again.
4. When transmission of one byte data is completed while TDRE is 1, TEND in ICSR is at the rise of the 9th transmit clock pulse. Read the ACKBR bit in ICIER, and confirm slave device has been selected. Then, write second byte data to ICDRT. When ACKB the slave device has not been acknowledged, so issue the stop condition. To issue the condition, write 0 to BBSY and SCP using MOV instruction. SCL is fixed low until t transmit data is prepared or the stop condition is issued.
5. The transmit data after the second byte is written to ICDRT every time TDRE is set.
6. Write the number of bytes to be transmitted to ICDRT. Wait until TEND is set (the en byte data transmission) while TDRE is 1, or wait for NACK (NACKF in ICSR = 1) fr receive device while ACKE in ICIER is 1. Then, issue the stop condition to clear TEN NACKF.
7. When the STOP bit in ICSR is set to 1, the operation returns to the slave receive mod

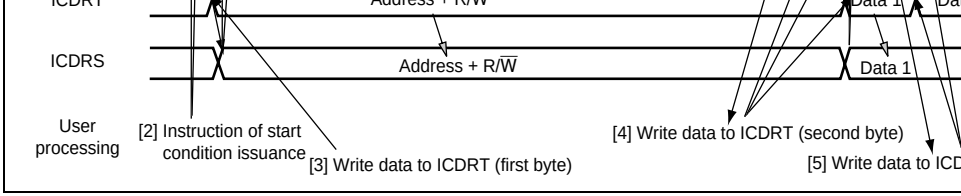


Figure 20.5 Master Transmit Mode Operation Timing (1)

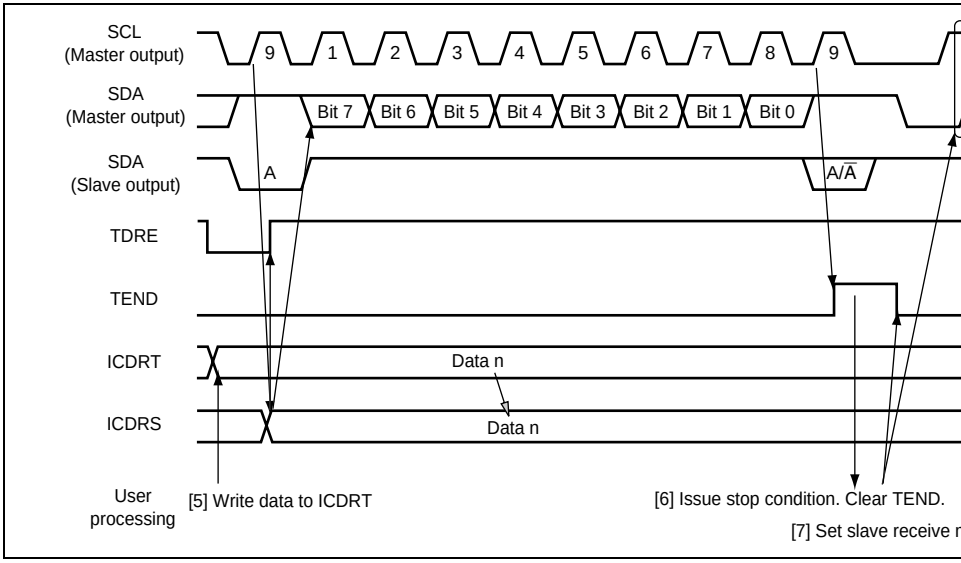


Figure 20.6 Master Transmit Mode Operation Timing (2)

2. When ICDRR is read (dummy data read), reception is started, and the receive clock is and data received, in synchronization with the internal clock. The master device outpu level specified by ACKBT in ICIER to SDA, at the 9th receive clock pulse.
3. After the reception of first frame data is completed, the RDRF bit in ICST is set to 1 a of 9th receive clock pulse. At this time, the receive data is read by reading ICDRR, an is cleared to 0.
4. The continuous reception is performed by reading ICDRR every time RDRF is set. If receive clock pulse falls after reading ICDRR by the other processing while RDRF is fixed low until ICDRR is read.
5. If next frame is the last receive data, set the RCVD bit in ICCR1 and set the ACKBT ICIER. to 1 before reading ICDRR. This enables the issuance of the stop condition af next reception.
6. When the RDRF bit is set to 1 at rise of the 9th receive clock pulse, and clearing the S in ICSR issue the stage condition.
7. When the STOP bit in ICSR is set to 1, read ICDRR. Then clear the RCVD bit to 0.
8. Clear the MST bit in ICCR1 and then, the operation returns to the slave receive mode

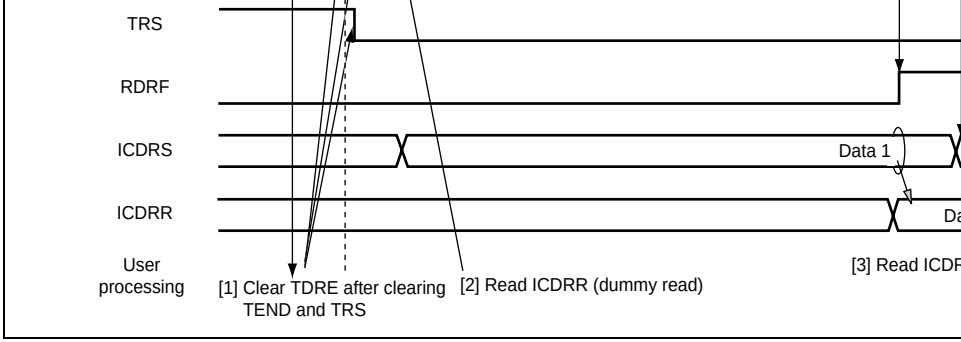


Figure 20.7 Master Receive Mode Operation Timing (1)

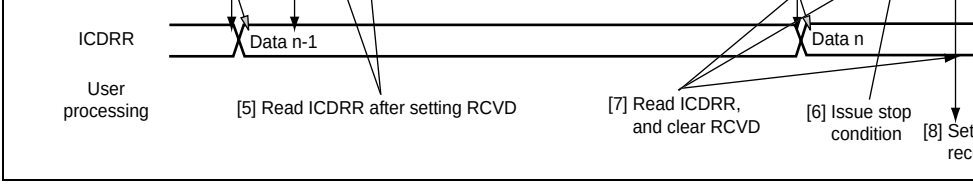


Figure 20.8 Master Receive Mode Operation Timing (2)

2. When the slave address matches in the first frame following detection of the start co
the slave device outputs the level specified by ACKBT in ICIER to SDA, at the rise
clock pulse. At this time, if the 8th bit data (R/$\overline{W}$) is 1, the TRS and ICSR bits in IC
set to 1, and the mode changes to slave transmit mode automatically. The continuou
transmission is performed by writing transmit data to ICDRT every time TDRE is se
3. If TDRE is set after writing last transmit data to ICDRT, wait until TEND in ICSR is
with TDRE = 1. When TEND is set, clear TEND.
4. Clear TRS for the end processing, and read ICDRR (dummy read). SCL is free.
5. Clear TDRE.

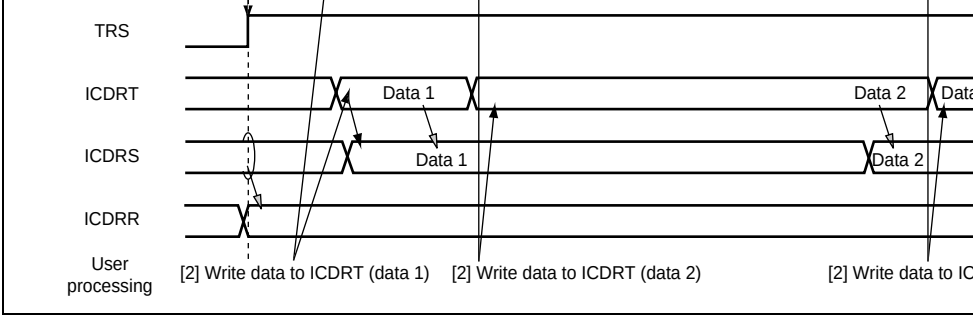


Figure 20.9 Slave Transmit Mode Operation Timing (1)

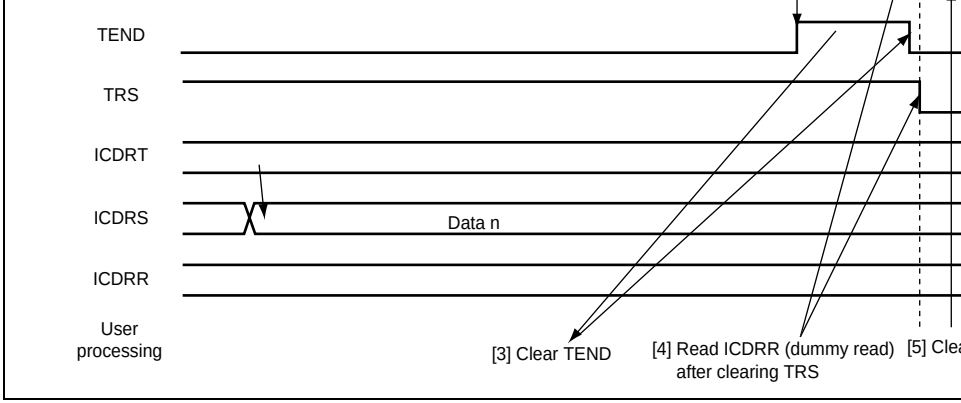


Figure 20.10 Slave Transmit Mode Operation Timing (2)

20.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and transmit data, an slave device returns an acknowledge signal. For slave receive mode operation timing, re figures 20.11 and 20.12. The reception procedure and operations in slave receive mode a described below.

1. Set the ICE bit in ICCR1 to 1. Set the MLS and WAIT bits in ICMR and the CKS3 bits in ICCR1 to 1. (Initial setting) Set the MST and TRS bits in ICCR1 to select slav mode, and wait until the slave address matches.
2. When the slave address matches in the first frame following detection of the start co the slave device outputs the level specified by ACKBT in ICIER to SDA, at the rise clock pulse. At the same time, RDRF in ICSR is set to read ICDRR (dummy read). (read data show the slave address and R/$\overline{W}$, it is not used.)

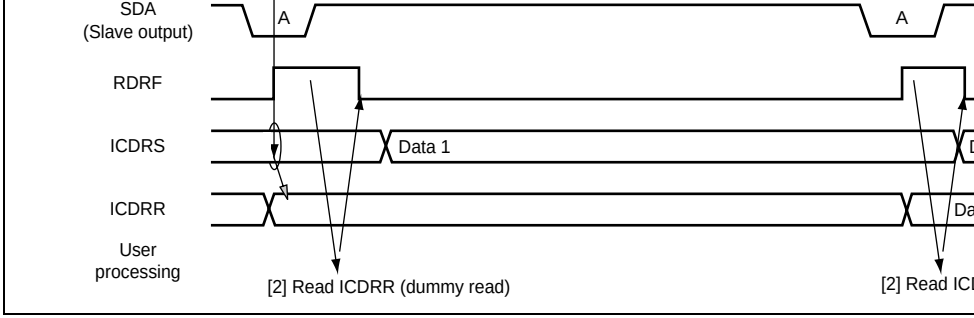


Figure 20.11 Slave Receive Mode Operation Timing (1)

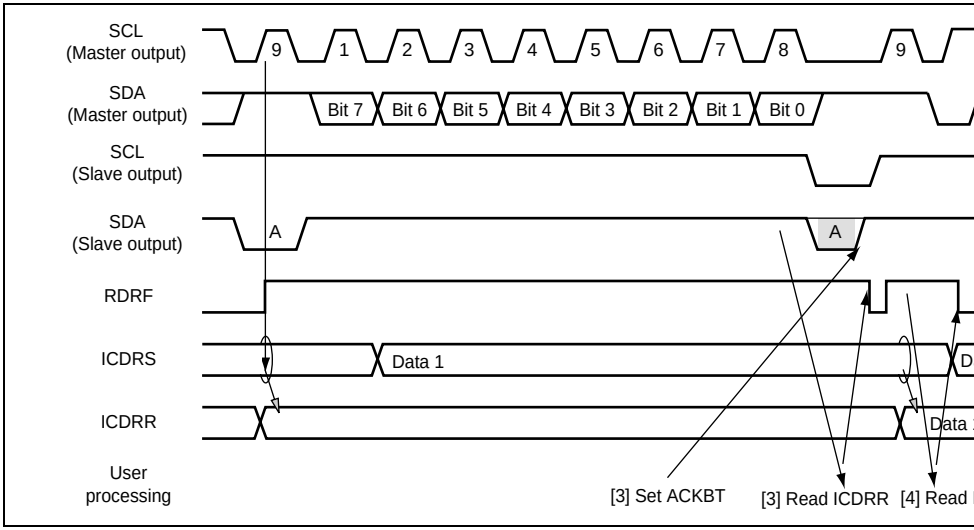


Figure 20.12 Slave Receive Mode Operation Timing (2)

of the SCL clock is guaranteed. The MLS bit in ICMR sets the order of data transfer, in MSB first or LSB first. The output level of SDA can be changed during the transfer wai SDAO bit in ICCR2.

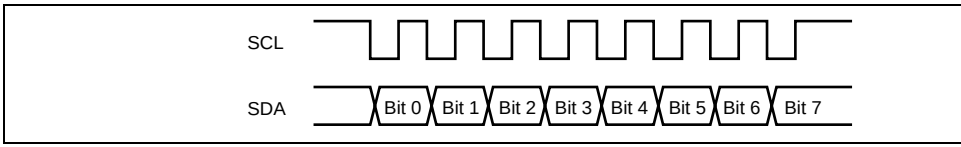


Figure 20.13 Clocked Synchronous Serial Transfer Format

transferred from ICDRT to ICDRS, and TDRE is set automatically. The continuous transmission is performed by writing data to ICDRT every time TDRE is set. When c from transmit mode to receive mode, clear TRS while TDRE is 1.

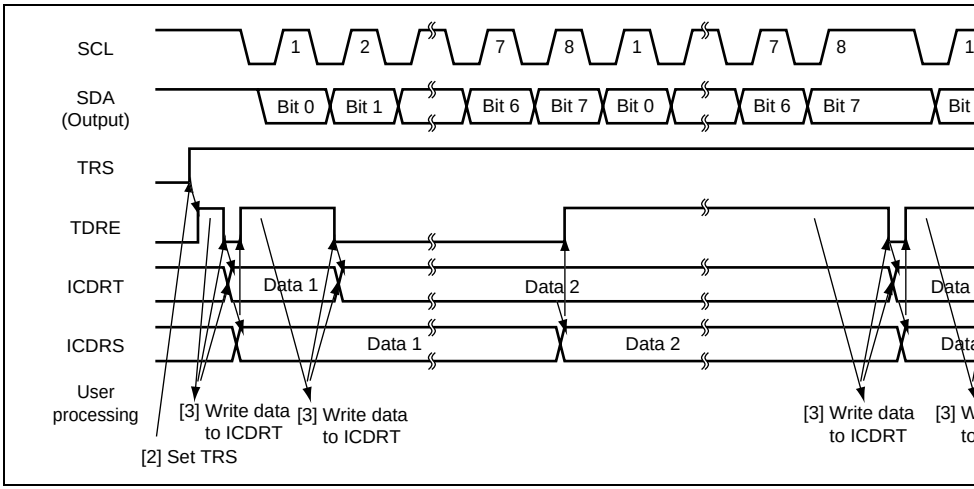


Figure 20.14 Transmit Mode Operation Timing

continually output. The continuous reception is performed by reading ICDRR every
RDRF is set. When the 8th clock is risen while RDRF is 1, the overrun is detected a
AL/OVE in ICSR is set. At this time, the previous reception data is retained in ICDR

4. To stop receiving when MST = 1, set RCVD in ICCR1 to 1, then read ICDRR. Then
fixed high after receiving the next byte data.

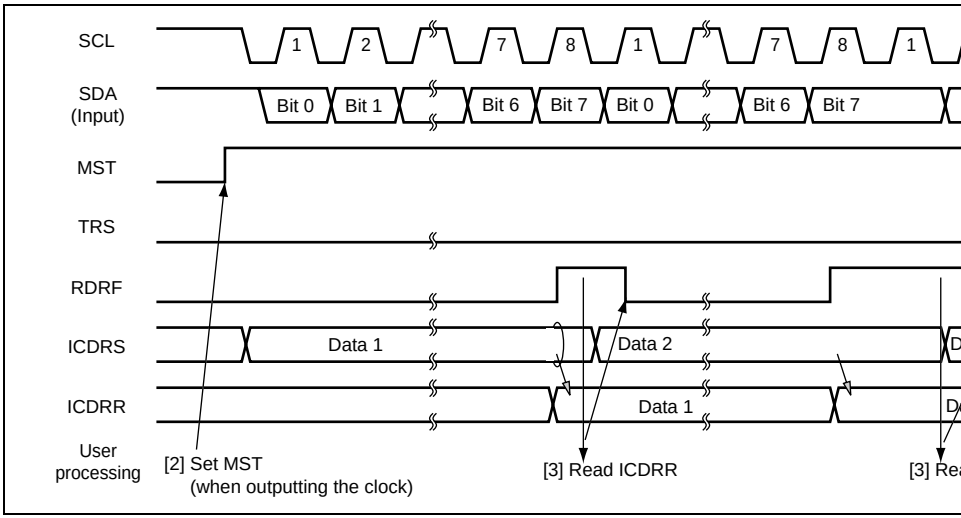


Figure 20.15 Receive Mode Operation Timing

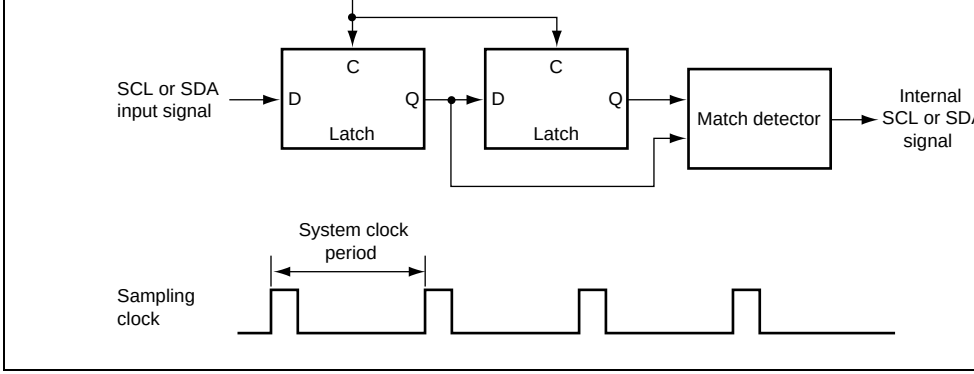


Figure 20.16 Block Diagram of Noise Conceler

20.4.8 Example of Use

Flowcharts in respective modes that use the I^2C bus interface are shown in figures 20.17 t

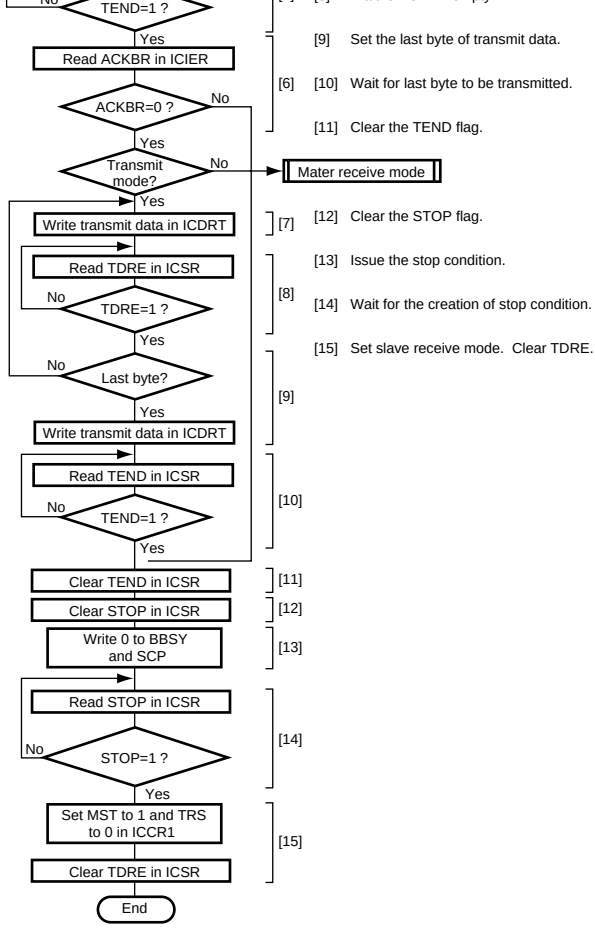
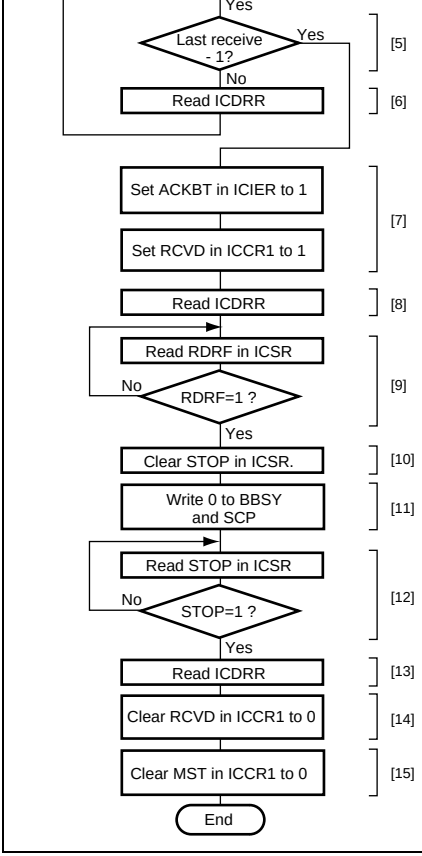


Figure 20.17 Sample Flowchart for Master Transmit Mode



[9] Wait for the last byte to be receive.

[10] Clear the STOP flag.

[11] Issue the stop condition.

[12] Wait for the creation of stop condition.

[13] Read the last byte of receive data.

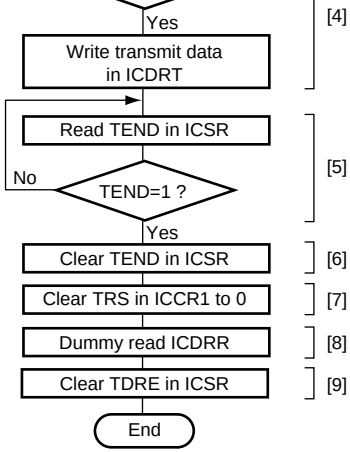
[14] Clear RCVD.

[15] Set slave receive mode.

Note: When 1 byte is received, skip steps [2] to [6] after [1] and then jum
to step [7].
In step [8], dummy-read ICDRR.

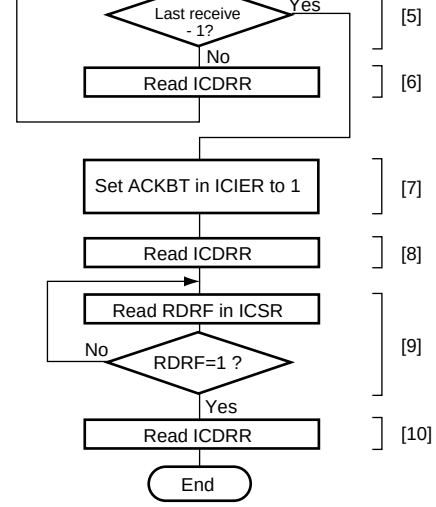
* Do not activate an interrupt during the execution of steps [1] to [3

Figure 20.18 Sample Flowchart for Master Receive Mode



[9] Clear the TDRE flag.

Figure 20.19 Sample Flowchart for Slave Transmit Mode



[8] Read the (last byte - 1) of receive data.

[9] Wait the last byte to be received.

[10] Read for the last byte of receive data.

Note: When 1 byte is received, skip steps [2] to [6] after [1] and then jump to step [7].
In step [8], dummy-read ICDRR.

Figure 20.20 Sample Flowchart for Slave Receive Mode

Transmit Data Empty	TXI	(TDRE=1) • (TIE=1)	○	○
Transmit End	TEI	(TEND=1) • (TEIE=1)	○	○
Receive Data Full	RXI	(RDRF=1) • (RIE=1)	○	○
STOP Recognition	STPI	(STOP=1) • (STIE=1)	○	×
NACK Receive	NAKI	{(NACKF=1)+(AL=1)} • (NAKIE=1)	○	×
Arbitration Lost/Overrun			○	○

When interrupt conditions described in table 20.3 are 1 and the I bit in CCR is 0, the CP executes interrupt exception processing. Interrupt sources should be cleared in the excep processing. TDRE and TEND are automatically cleared to 0 by writing the transmit data ICDRT. RDRF are automatically cleared to 0 by reading ICDRR. TDRE is set to 1 agai same time when transmit data is written to ICDRT. When TDRE is cleared to 0, then an data of one byte may be transmitted.

Figure 20.21 shows the timing of the bit synchronous circuit and table 20.4 shows the tim
SCL output changes from low to Hi-Z then SCL is monitored.

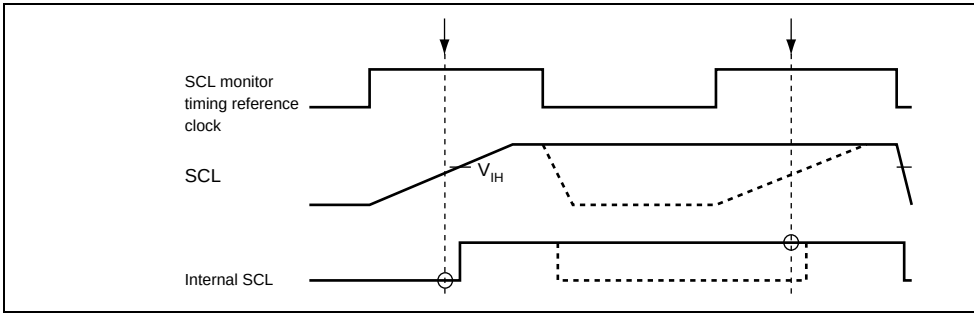


Figure 20.21 Timing of Bit Synchronous Circuit

Table 20.4 Time for Monitoring SCL

CKS3	CKS2	Time for Monitoring SCL
0	0	7.5 tcyc
	1	19.5 tcyc
1	0	17.5 tcyc
	1	41.5 tcyc

during the eighth clock.

2. The WAIT bit in the I2C bus mode register (ICMR) must be held 0.

   If the WAIT bit is set to 1, when a slave device holds the SCL signal low more than
   transfer clock cycle during the eighth clock, the high level period of the ninth clock
   shorter than a given period.

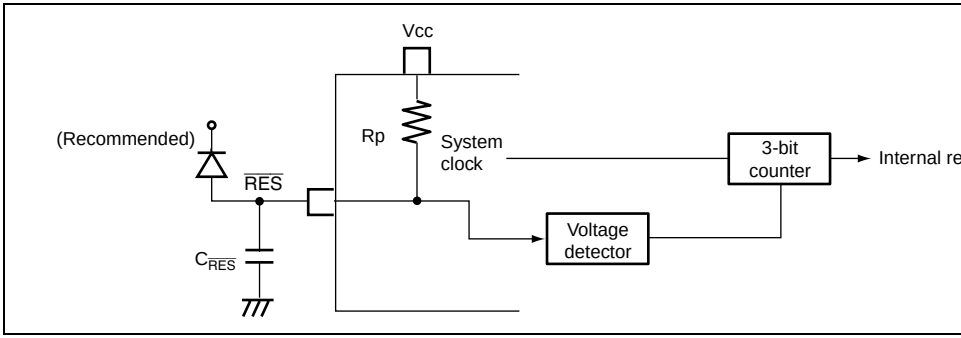


Figure 21.1 Power-On Reset Circuit

If the $\overline{\text{RES}}$ pin rising time is t, the capacitance ($C_{\overline{\text{RES}}}$) connected to the $\overline{\text{RES}}$ pin can be co
using the formula below. For information about the on-chip resistor (Rp), see section 24,
Characteristics. The power supply rising time should not exceed half the $\overline{\text{RES}}$ rising time
$\overline{\text{RES}}$ rising time (t) should also equal or exceed the oscillation stabilization time (trc).

$$C_{\overline{\text{RES}}} = \frac{t}{Rp} \quad (t > trc,\ t > t\_vtr \times 2)$$

Note: Adjust the capacitor connected to the $\overline{\text{RES}}$ pin so that t_vtr × 2 exceeds the oscill
stabilization time.

Note that the power supply voltage (Vcc) must fall below Vpor = 100 mV and rise after c
the RES pin is removed. To remove charge on the RES pin, it is recommended that the di
should be placed near Vcc. If the power supply voltage (Vcc) rises from the point above
power-on reset may not occur.

Figure 21.2 Power-On Reset Circuit Operation Timing

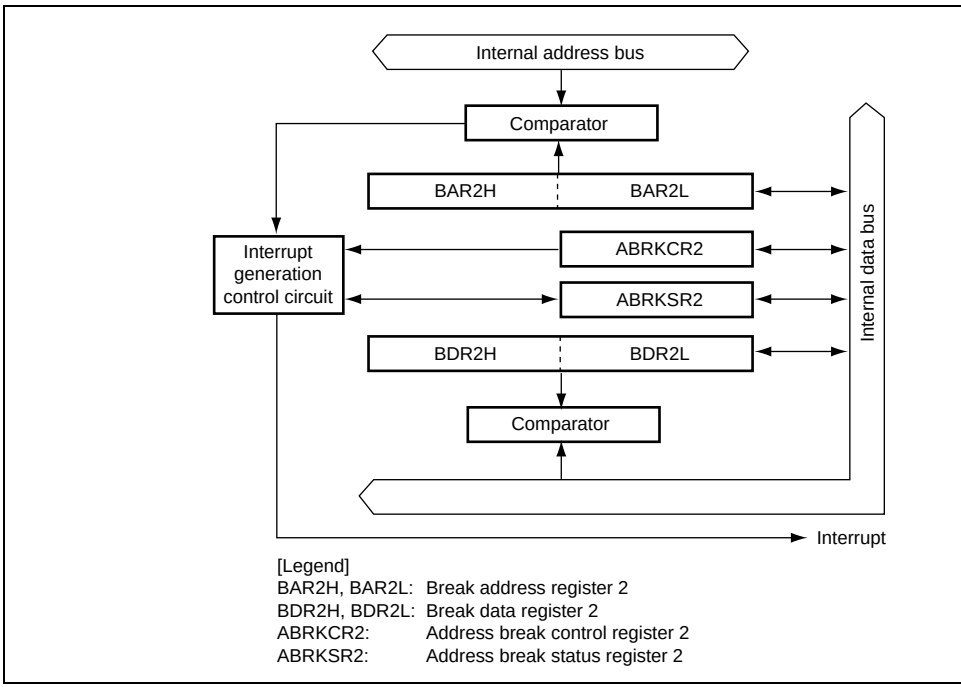


Figure 22.1 Block Diagram of Address Break

ABRKCR2 sets address break conditions.

Bit	Bit Name	Initial Value	R/W	Description
7	RTINTE2	1	R/W	RTE Interrupt Enable When this bit is 0, the interrupt immediately aft executing RTE is masked and then one instruc be executed. When this bit is 1, the interrupt is masked.
6	CSEL21	0	R/W	Condition Select 1 and 0 These bits set address break conditions. 00: Instruction execution cycle (no data compa 01: CPU data read cycle 10: CPU data write cycle 11: CPU data read/write cycle
5	CSEL20	0	R/W	
4	ACMP22	0	R/W	Address Compare Condition Select 2 to 0 These bits set the comparison condition betwe address set in BAR2 and the internal address 000: Compares 16-bit addresses 001: Compares upper 12-bit addresses 010: Compares upper 8-bit addresses 011: Compares upper 4-bit addresses 1xx: Setting prohibited
3	ACMP21	0	R/W	
2	ACMP20	0	R/W	

[Legend] x: Don't care.

When an address break is set in the data read cycle or data write cycle, the data bus used depend on the combination of the byte/word access and address. Table 22.1 shows the a data bus used. When an I/O register space with an 8-bit data bus width is accessed in wo byte access is generated twice. For details on data widths of each register, see section 23 Register Addresses (Address Order).

Table 22.1 Access and Data Bus Used

	Word Access		Byte Access	
	Even Address	**Odd Address**	**Even Address**	**Odd A**
ROM space	Upper 8 bits	Lower 8 bits	Upper 8 bits	Upper
RAM space	Upper 8 bits	Lower 8 bits	Upper 8 bits	Upper
I/O register with 8-bit data bus width	Upper 8 bits	Upper 8 bits	Upper 8 bits	Upper
I/O register with 16-bit data bus width*[1]	Upper 8 bits	Lower 8 bits	—	—
I/O register with 16-bit data bus width*[2]	Upper 8 bits	Lower 8 bits	Upper 8 bits	Upper

Notes: 1. Registers whose addresses do not range from H'FF96 and H'FF97, and H'FF H'FFBB with 16-bit data bus width.

2. Registers whose addresses range from H'FF96 and H'FF97, and H'FFB8 to H

				When 0 is written after ABIF=1 is read
6	ABIE2	0	R/W	Address Break Interrupt Enable When this bit is 1, an address break interrupt r enabled.
5 to 0	—	All 1	—	Reserved These bits are always read as 1.

22.1.3 Break Address Registers 2 (BAR2H, BAR2L)

BAR2H and BAR2L are 16-bit read/write registers that set the address for generating an break interrupt. When setting the address break condition to the instruction execution cyc first byte address of the instruction. The initial value of this register is H'FFFF.

22.1.4 Break Data Registers 2 (BDR2H, BDR2L)

BDR2H and BDR2L are 16-bit read/write registers that set the data for generating an add break interrupt. BDR2H is compared with the upper 8-bit data bus. BDR2L is compared lower 8-bit data bus. When memory or registers are accessed by byte, the upper 8-bit data used for even and odd addresses in the data transmission. Therefore, comparison data mu in BDR2H for byte access. For word access, the data bus used depends on the address. Se 22.1.1, Address Break Control Register 2 (ABRKCR2), for details. The initial value of th register is undefined.

When the address break is specified in instruction execution cycle

Register setting
- ABRKCR2 = H'80
- BAR2 = H'025A

Program

	0258	NOP
*	025A	NOP
	025C	MOV.W @H'025A,R0
	0260	NOP
	0262	NOP
	:	:

Underline indicates the address to be stacked.

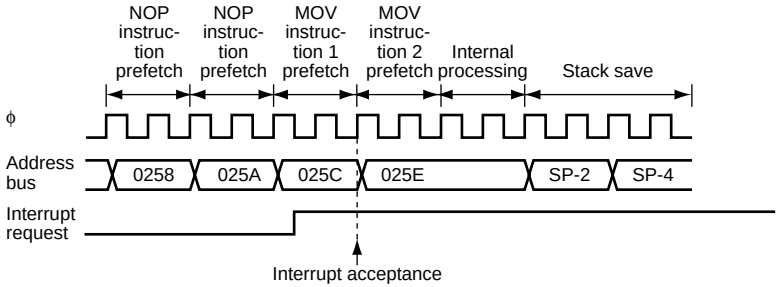


Figure 22.2 Address Break Interrupt Operation Example (1)

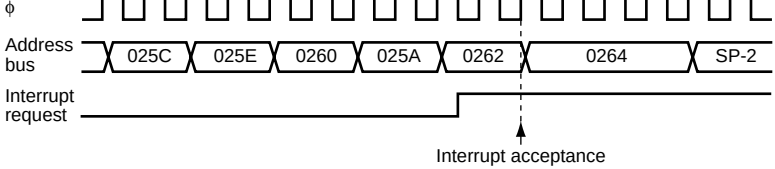


Figure 22.2 Address Break Interrupt Operation Example (2)

22.3 Operating States of Address Break

The operating states of the address break are shown in table 22.2.

Table 22.2 Operating States of Address Break

Operating Mode	Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	M S
ABRKCR2	Reset	Functions	Retained	Retained	Functions	Retained	Retained	R
ABRKSR2	Reset	Functions	Retained	Retained	Functions	Retained	Retained	R
BAR2H	Reset	Functions	Retained	Retained	Functions	Retained	Retained	R
BAR2L	Reset	Functions	Retained	Retained	Functions	Retained	Retained	R
BDR2H	Retained*	Functions	Retained	Retained	Functions	Retained	Retained	R
BDR2L	Retained*	Functions	Retained	Retained	Functions	Retained	Retained	R

Note: * Undefined at a power-on reset

- The number of access states is indicated.

2. Register bits
- Bit configurations of the registers are described in the same order as the register addr
- Reserved bits are indicated by — in the bit name column.
- When registers consist of 16 bits, bits are described from the MSB side.

3. Register states in each operating mode
- Register states are described in the same order as the register addresses.
- The register states described here are for the basic operating modes. If there is a spec
  for an on-chip peripheral module, refer to the section on that on-chip peripheral mod

Transmit data register 4	TDR4	8	H'F00E	SCI4	8
Receive data register 4	RDR4	8	H'F00F	SCI4	8
Flash memory control register 1	FLMCR1	8	H'F020	ROM	8
Flash memory control register 2	FLMCR2	8	H'F021	ROM	8
Flash memory power control register	FLPWCR	8	H'F022	ROM	8
Erase block register1	EBR1	8	H'F023	ROM	8
Flash memory enable register	FENR	8	H'F02B	ROM	8
Timer start register	TSTR	8	H'F030	TPU	8
Timer synchro register	TSYR	8	H'F031	TPU	8
Timer control register_1	TCR_1	8	H'F040	TPU_1	8
Timer mode register_1	TMDR_1	8	H'F041	TPU_1	8
Timer I/O control register_1	TIOR_1	8	H'F042	TPU_1	8
Timer interrupt enable register_1	TIER_1	8	H'F044	TPU_1	8
Timer status register_1	TSR_1	8	H'F045	TPU_1	8
Timer counter_1	TCNT_1	16	H'F046	TPU_1	16
Timer general register A_1	TGRA_1	16	H'F048	TPU_1	16
Timer general register B_1	TGRB_1	16	H'F04A	TPU_1	16
Timer control register_2	TCR_2	8	H'F050	TPU_2	8
Timer mode register_2	TMDR_2	8	H'F051	TPU_2	8
Timer I/O control register_2	TIOR_2	8	H'F052	TPU_2	8
Timer interrupt enable register_2	TIER_2	8	H'F054	TPU_2	8
Timer status register_2	TSR_2	8	H'F055	TPU_2	8
Timer counter_2	TCNT_2	16	H'F056	TPU_2	16

Day-of-week data register	RWKDR	8	H'F06B	RTC	8
RTC control register 1	RTCCR1	8	H'F06C	RTC	8
RTC control register 2	RTCCR2	8	H'F06D	RTC	8
SUB32k control register	SUB32CR	8	H'F06E	Clock pulse generator	8
Clock source select register	RTCCSR	8	H'F06F	RTC	8
I^2C bus control register 1	ICCR1	8	H'F078	IIC2	8
I^2C bus control register 2	ICCR2	8	H'F079	IIC2	8
I^2C bus mode register	ICMR	8	H'F07A	IIC2	8
I^2C bus interrupt enable register	ICIER	8	H'F07B	IIC2	8
I^2C bus status register	ICSR	8	H'F07C	IIC2	8
Slave address register	SAR	8	H'F07D	IIC2	8
I^2C bus transmit data register	ICDRT	8	H'F07E	IIC2	8
I^2C bus receive data register	ICDRR	8	H'F07F	IIC2	8
Interrupt priority register A	IPRA	8	H'F080	Interrupts	8
Interrupt priority register B	IPRB	8	H'F081	Interrupts	8
Interrupt priority register C	IPRC	8	H'F082	Interrupts	8
Interrupt priority register D	IPRD	8	H'F083	Interrupts	8
Interrupt priority register E	IPRE	8	H'F084	Interrupts	8
Address break control register 2	ABRKCR2	8	H'F096	Address break	8
Address break status register 2	ABRKSR2	8	H'F097	Address break	8

Event counter PWM compare register	ECPWCR	16	H'FF8C	AEC*[1]	16
Event counter PWM data register	ECPWDR	16	H'FF8E	AEC*[1]	16
Wakeup edge select register	WEGR	8	H'FF90	Interrupts	8
Serial port control register	SPCR	8	H'FF91	SCI3	8
Input pin edge select register	AEGSR	8	H'FF92	AEC*[1]	8
Event counter control register	ECCR	8	H'FF94	AEC*[1]	8
Event counter control/status register	ECCSR	8	H'FF95	AEC*[1]	8
Event counter H	ECH	8	H'FF96	AEC*[1]	8/16
Event counter L	ECL	8	H'FF97	AEC*[1]	8/16
Serial mode register 3_1	SMR3_1	8	H'FF98	SCI3_1	8
Bit rate register 3_1	BRR3_1	8	H'FF99	SCI3_1	8
Serial control register 3_1	SCR3_1	8	H'FF9A	SCI3_1	8
Transmit data register 3_1	TDR3_1	8	H'FF9B	SCI3_1	8
Serial status register 3_1	SSR3_1	8	H'FF9C	SCI3_1	8
Receive data register 3_1	RDR3_1	8	H'FF9D	SCI3_1	8
LCD port control register	LPCR	8	H'FFA0	LCD*[3]	8
LCD control register	LCR	8	H'FFA1	LCD*[3]	8
LCD control register 2	LCR2	8	H'FFA2	LCD*[3]	8
LCD trimming register	LTRMR	8	H'FFA3	LCD*[3]	8
BGR control register	BGRMR	8	H'FFA4	LCD*[3]	8
IrDA control register	IrCR	8	H'FFA7	IrDA	8
Serial mode register 3_2	SMR3_2	8	H'FFA8	SCI3_2	8
Bit rate register 3_2	BRR3_2	8	H'FFA9	SCI3_2	8

Timer counter WD	TCWD	8	H'FFB3	WDT*[2]	8
Timer control register F	TCRF	8	H'FFB6	Timer F	8
Timer control/status register F	TCSRF	8	H'FFB7	Timer F	8
8-bit timer counter FH	TCFH	8	H'FFB8	Timer F	8/16
8-bit timer counter FL	TCFL	8	H'FFB9	Timer F	8/16
Output compare register FH	OCRFH	8	H'FFBA	Timer F	8/16
Output compare register FL	OCRFL	8	H'FFBB	Timer F	8/16
A/D result register	ADRR	16	H'FFBC	A/D converter	16
A/D mode register	AMR	8	H'FFBE	A/D converter	8
A/D start register	ADSR	8	H'FFBF	A/D converter	8
Port mode register 1	PMR1	8	H'FFC0	I/O ports	8
Oscillator Control Register	OSCCR	8	H'FFC1	Clock pulse generator	8
Port mode register 3	PMR3	8	H'FFC2	I/O ports	8
Port mode register 4	PMR4	8	H'FFC3	I/O ports	8
Port mode register 5	PMR5	8	H'FFC4	I/O ports	8
Port mode register 9	PMR9	8	H'FFC8	I/O ports	8
Port mode register B	PMRB	8	H'FFCA	I/O ports	8
PWM2 control register	PWCR2[2]	8	H'FFCD	14-bit PWM	8
PWM2 data register	PWDR2	16	H'FFCE	14-bit PWM	16
PWM1 control register	PWCR1	8	H'FFD0	14-bit PWM	8
PWM1 data register	PWDR1	16	H'FFD2	14-bit PWM	16

Port data register 9	PDR9	8	H'FFDC	I/O ports	8
Port data register A	PDRA	8	H'FFDD	I/O ports	8
Port data register B	PDRB	8	H'FFDE	I/O ports	8
Port pull-up control register 1	PUCR1	8	H'FFE0	I/O ports	8
Port pull-up control register 3	PUCR3	8	H'FFE1	I/O ports	8
Port pull-up control register 5	PUCR5	8	H'FFE2	I/O ports	8
Port pull-up control register 6	PUCR6	8	H'FFE3	I/O ports	8
Port control register 1	PCR1	8	H'FFE4	I/O ports	8
Port control register 3	PCR3	8	H'FFE6	I/O ports	8
Port control register 4	PCR4	8	H'FFE7	I/O ports	8
Port control register 5	PCR5	8	H'FFE8	I/O ports	8
Port control register 6	PCR6	8	H'FFE9	I/O ports	8
Port control register 7	PCR7	8	H'FFEA	I/O ports	8
Port control register 8	PCR8	8	H'FFEB	I/O ports	8
Port control register 9	PCR9	8	H'FFEC	I/O ports	8
Port control register A	PCRA	8	H'FFED	I/O ports	8
System control register 1	SYSCR1	8	H'FFF0	System	8
System control register 2	SYSCR2	8	H'FFF1	System	8
IRQ edge select register	IEGR	8	H'FFF2	Interrupts	8
Interrupt enable register 1	IENR1	8	H'FFF3	Interrupts	8
Interrupt enable register 2	IENR2	8	H'FFF4	Interrupts	8
Interrupt mask register	INTM	8	H'FFF5	Interrupts	8

3. LCD: LCD controller/driver

FLMCR1	—	SWE	ESU	PSU	EV	PV	E	P
FLMCR2	FLER	—	—	—	—	—	—	—
FLPWCR	PDWND	—	—	—	—	—	—	—
EBR1	—	EB6	EB5	EB4	EB3	EB2	EB1	EB0
FENR	FLSHE	—	—	—	—	—	—	—
TSTR	—	—	—	—	—	CST2	CST1	—
TSYR	—	—	—	—	—	SYNC2	SYNC1	—
TCR_1	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
TMDR_1	—	—	—	—	—	—	MD1	MD0
TIOR_1	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
TIER_1	—	—	—	TCIEV	—	—	TGIEB	TGIEA
TSR_1_	—	—	—	TCFV	—	—	TGFB	TGFA
TCNT_1	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TGRA_1	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TGRB_1	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCR_2	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0
TMDR_2	—	—	—	—	—	—	MD1	MD0
TIOR_2	IOB3	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
TIER_2	—	—	—	TCIEV	—	—	TGIEB	TGIEA
TSR_2	—	—	—	TCFV	—	—	TGFB	TGFA

RMINDR	BSY	MN12	MN11	MN10	MN03	MN02	MN01	MN00
RHRDR	BSY	—	HR11	HR10	HR03	HR02	HR01	HR00
RWKDR	BSY	—	—	—	—	WK2	WK1	WK0
RTCCR1	RUN	12/24	PM	RST	—	—	—	—
RTCCR2	FOIE	WKIE	DYIE	HRIE	MNIE	1SEIE	05SEIE	025SEIE
SUB32CR	32KSTOP	—	—	—	—	—	—	—
RTCCSR	—	RCS6	RCS5	SUB32K	RCS3	RCS2	RCS1	RCS0
ICCR1	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
ICCR2	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—
ICMR	MLS	WAIT	—	—	BCWP	BC2	BC1	BC0
ICIER	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT
ICSR	TDRE	TEND	RDRF	NACKF	STOP	AL/OVE	AAS	ADZ
SAR	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS
ICDRT	ICDRT7	ICDRT6	ICDRT5	ICDRT4	ICDRT3	ICDRT2	ICDRT1	ICDRT0
ICDRR	ICDRR7	ICDRR6	ICDRR5	ICDRR4	ICDRR3	ICDRR2	ICDRR1	ICDRR0
IPRA	IPRA7	IPRA6	IPRA5	IPRA4	IPRA3	IPRA2	IPRA1	IPRA0
IPRB	IPRB7	IPRB6	IPRB5	IPRB4	IPRB3	IPRB2	IPRB1	IPRB0
IPRC	IPRC7	IPRC6	IPRC5	IPRC4	IPRC3	IPRC2	IPRC1	IPRC0
IPRD	IPRD7	IPRD6	IPRD5	IPRD4	IPRD3	IPRD2	IPRD1	IPRD0
IPRE	IPRE7	IPRE6	IPRE5	IPRE4	—	—	—	—

ECPWDR	ECPWDR15	ECPWDR14	ECPWDR13	ECPWDR12	ECPWDR11	ECPWDR10	ECPWDR9	ECPWDR8
	ECPWDR7	ECPWDR6	ECPWDR5	ECPWDR4	ECPWDR3	ECPWDR2	ECPWDR1	ECPWDR0
WEGR	WKEGS7	WKEGS6	WKEGS5	WKEGS4	WKEGS3	WKEGS2	WKEGS1	WKEGS0
SPCR	—	—	SPC32	SPC31	SCINV3	SCINV2	SCINV1	SCINV0
AEGSR	AHEGS1	AHEGS0	ALEGS1	ALEGS0	AIEGS1	AIEGS0	ECPWME	—
ECCR	ACKH1	ACKH0	ACKL1	ACKL0	PWCK2	PWCK1	PWCK0	—
ECCSR	OVH	OVL	—	CH2	CUEH	CUEL	CRCH	CRCL
ECH	ECH7	ECH6	ECH5	ECH4	ECH3	ECH2	ECH1	ECH0
ECL	ECL7	ECL6	ECL5	ECL4	ECL3	ECL2	ECL1	ECL0
SMR3_1	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0
BRR3_1	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0
SCR3_1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0
TDR3_1	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0
SSR3_1	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT
RDR3_1	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
LPCR	DTS1	DTS0	CMX	—	SGS3	SGS2	SGS1	SGS0
LCR	—	PSW	ACT	DISP	CKS3	CKS2	CKS1	CKS0
LCR2	LCDAB	HCKS	CHG	SUPS	—	—	—	—
LTRMR	TRM3	TRM2	TRM1	TRM0	—	CTRM2	CTRM1	CTRM0
BGRMR	BGRSTPN	—	—	—	—	BTRM2	BTRM1	BTRM0
IrCR	IrE	IrCKS2	IrCKS1	IrCKS0	—	—	—	—

TCSRWD2	OVF	B5WI	WT/$\overline{IT}$	B3WI	IEOVF	—	—	—
TCWD	TCW7	TCW6	TCW5	TCW4	TCW3	TCW2	TCW1	TCW0
TCRF	TOLH	CKSH2	CKSH1	CKSH0	TOLL	CKSL2	CKSL1	CKSL0
TCSRF	OVFH	CMFH	OVIEH	CCLRH	OVFL	CMFL	OVIEL	CCLRL
TCFH	TCFH7	TCFH6	TCFH5	TCFH4	TCFH3	TCFH2	TCFH1	TCFH0
TCFL	TCFL7	TCFL6	TCFL5	TCFL4	TCFL3	TCFL2	TCFL1	TCFL0
OCRFH	OCRFH7	OCRFH6	OCRFH5	OCRFH4	OCRFH3	OCRFH2	OCRFH1	OCRFH0
OCRFL	OCRFL7	OCRFL6	OCRFL5	OCRFL4	OCRFL3	OCRFL2	OCRFL1	OCRFL0
ADRR	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2
	ADR1	ADR0	—	—	—	—	—	—
AMR	CKS	TRGE	—	—	CH3	CH2	CH1	CH0
ADSR	ADSF	—	—	—	—	—	—	—
PMR1	—	—	—	—	—	—	AEVL	AEVH
OSCCR	—	—	—	—	—	IRQAECF	OSCF	—
PMR3	—	—	—	—	—	—	—	TMOW
PMR4	—	—	—	—	—	TMOFH	TMOFL	TMIF
PMR5	WKP7	WKP6	WKP5	WKP4	WKP3	WKP2	WKP1	WKP0
PMR9	—	—	—	—	—	IRQ4	PWM2	PWM1
PMRB	—	—	—	ADTSTCHG	—	IRQ3	IRQ1	IRQ0

PDR4	—	—	—	—	—	P42	P41	P40
PDR5	P57	P56	P55	P54	P53	P52	P51	P50
PDR6	P67	P66	P65	P64	P63	P62	P61	P60
PDR7	P77	P76	P75	P74	P73	P72	P71	P70
PDR8	P87	P86	P85	P84	P83	P82	P81	P80
PDR9	—	—	—	—	P93	P92	P91	P90
PDRA	—	—	—	—	PA3	PA2	PA1	PA0
PDRB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
PUCR1	—	PUCR16	PUCR15	PUCR14	PUCR13	PUCR12	PUCR11	PUCR10
PUCR3	PUCR37	PUCR36	—	—	—	—	—	PUCR30
PUCR5	PUCR57	PUCR56	PUCR55	PUCR54	PUCR53	PUCR52	PUCR51	PUCR50
PUCR6	PUCR67	PUCR66	PUCR65	PUCR64	PUCR63	PUCR62	PUCR61	PUCR60
PCR1	—	PCR16	PCR15	PCR14	PCR13	PCR12	PCR11	PCR10
PCR3	PCR37	PCR36	—	—	—	PCR32	PCR31	PCR30
PCR4	—	—	—	—	—	PCR42	PCR41	PCR40
PCR5	PCR57	PCR56	PCR55	PCR54	PCR53	PCR52	PCR51	PCR50
PCR6	PCR67	PCR66	PCR65	PCR64	PCR63	PCR62	PCR61	PCR60
PCR7	PCR77	PCR76	PCR75	PCR74	PCR73	PCR72	PCR71	PCR70
PCR8	PCR87	PCR86	PCR85	PCR84	PCR83	PCR82	PCR81	PCR80
PCR9	—	—	—	—	PCR93	PCR92	PCR91	PCR90
PCRA	—	—	—	—	PCRA3	PCRA2	PCRA1	PCRA0
SYSCR1	SSBY	STS2	STS1	STS0	LSON	TMA3	MA1	MA0
SYSCR2	—	—	—	NESEL	DTON	MSON	SA1	SA0

CKSTPR2	ADBCKSTP	TPUCKSTP	IICCKSTP	PW2CKSTP	AECCKSTP	WDCKSTP	PW1CKSTP	LDCKSTP

Notes: 1. AEC: Asynchronous event counter
2. WDT: Watchdog timer
3. LCD: LCD controller/driver
4. This bit is available only for the flash memory version. In the masked ROM ve
bit is reserved.

FLPWCR	Initialized	—	—	—	—	—	—	
EBR1	Initialized	—	—	—	—	—	Initialized	
FENR	Initialized	—	—	—	—	—	—	
TSTR	Initialized	—	—	—	—	—	—	TPU
TSYR	Initialized	—	—	—	—	—	—	
TCR_1	Initialized	—	—	—	—	—	—	TPU
TMDR_1	Initialized	—	—	—	—	—	—	
TIOR_1	Initialized	—	—	—	—	—	—	
TIER_1	Initialized	—	—	—	—	—	—	
TSR_1_	Initialized	—	—	—	—	—	—	
TCNT_1	Initialized	—	—	—	—	—	—	
TGRA_1	Initialized	—	—	—	—	—	—	
TGRB_1	Initialized	—	—	—	—	—	—	
TCR_2	Initialized	—	—	—	—	—	—	TPU
TMDR_2	Initialized	—	—	—	—	—	—	
TIOR_2	Initialized	—	—	—	—	—	—	
TIER_2	Initialized	—	—	—	—	—	—	
TSR_2	Initialized	—	—	—	—	—	—	
TCNT_2	Initialized	—	—	—	—	—	—	
TGRA_2	Initialized	—	—	—	—	—	—	
TGRB_2	Initialized	—	—	—	—	—	—	

								ge
RTCCSR	Initialized	—	—	—	—	—	—	RT
ICCR1	Initialized	—	—	—	—	—	—	IIC
ICCR2	Initialized	—	—	—	—	—	—	
ICMR	Initialized	—	—	—	—	—	—	
ICIER	Initialized	—	—	—	—	—	—	
ICSR	Initialized	—	—	—	—	—	—	
SAR	Initialized	—	—	—	—	—	—	
ICDRT	Initialized	—	—	—	—	—	—	
ICDRR	Initialized	—	—	—	—	—	—	
IPRA	Initialized	—	—	—	—	—	—	Int
IPRB	Initialized	—	—	—	—	—	—	
IPRC	Initialized	—	—	—	—	—	—	
IPRD	Initialized	—	—	—	—	—	—	
IPRE	Initialized	—	—	—	—	—	—	
ABRKCR2	Initialized	—	—	—	—	—	—	Ad
ABRKSR2	Initialized	—	—	—	—	—	—	
BAR2H	Initialized	—	—	—	—	—	—	
BAR2L	Initialized	—	—	—	—	—	—	
BDR2H	—	—	—	—	—	—	—	
BDR2L	—	—	—	—	—	—	—	
ECPWCR	Initialized	—	—	—	—	—	—	AE
ECPWDR	Initialized	—	—	—	—	—	—	

BRR3_1	Initialized	—	—	Initialized	—	—	Initialized	
SCR3_1	Initialized	—	—	Initialized	—	—	Initialized	
TDR3_1	Initialized	—	—	Initialized	—	—	Initialized	
SSR3_1	Initialized	—	—	Initialized	—	—	Initialized	
RDR3_1	Initialized	—	—	Initialized	—	—	Initialized	
LPCR	Initialized	—	—	—	—	—	—	LCD
LCR	Initialized	—	—	—	—	—	—	
LCR2	Initialized	—	—	—	—	—	—	
LTRMR	Initialized	—	—	—	—	—	—	
BGRMR	Initialized	—	—	—	—	—	—	
IrCR	Initialized	—	—	Initialized	—	—	Initialized	IrDA
SMR3_2	Initialized	—	—	Initialized	—	—	Initialized	SCI
BRR3_2	Initialized	—	—	Initialized	—	—	Initialized	
SCR3_2	Initialized	—	—	Initialized	—	—	Initialized	
TDR3_2	Initialized	—	—	Initialized	—	—	Initialized	
SSR3_2	Initialized	—	—	Initialized	—	—	Initialized	
RDR3_2	Initialized	—	—	Initialized	—	—	Initialized	
TMWD	Initialized	—	—	—	—	—	—	WDT
TCSRWD1	Initialized	—	—	—	—	—	—	
TCSRWD2	Initialized	—	—	—	—	—	—	
TCWD	Initialized	—	—	—	—	—	—	

ADSR	Initialized	—	—	—	—	—	—	
PMR1	Initialized	—	—	—	—	—	—	I/O
PMR3	Initialized	—	—	—	—	—	—	
PMR4	Initialized	—	—	—	—	—	—	
PMR5	Initialized	—	—	—	—	—	—	
PMR9	Initialized	—	—	—	—	—	—	
PMRB	Initialized	—	—	—	—	—	—	
PWCR2	Initialized	—	—	—	—	—	—	14
PWDR2	Initialized	—	—	—	—	—	—	
PWCR1	Initialized	—	—	—	—	—	—	
PWDR1	Initialized	—	—	—	—	—	—	
PDR1	Initialized	—	—	—	—	—	—	I/O
OSCCR	Initialized	—	—	—	—	—	—	Clo ge
PDR3	Initialized	—	—	—	—	—	—	I/O
PDR4	Initialized	—	—	—	—	—	—	
PDR5	Initialized	—	—	—	—	—	—	
PDR6	Initialized	—	—	—	—	—	—	
PDR7	Initialized	—	—	—	—	—	—	
PDR8	Initialized	—	—	—	—	—	—	
PDR9	Initialized	—	—	—	—	—	—	
PDRA	Initialized	—	—	—	—	—	—	
PDRB	Initialized	—	—	—	—	—	—	

PCR6	Initialized	—	—	—	—	—	—	
PCR7	Initialized	—	—	—	—	—	—	
PCR8	Initialized	—	—	—	—	—	—	
PCR9	Initialized	—	—	—	—	—	—	
PCRA	Initialized	—	—	—	—	—	—	
SYSCR1	Initialized	—	—	—	—	—	—	Syst
SYSCR2	Initialized	—	—	—	—	—	—	
IEGR	Initialized	—	—	—	—	—	—	Inter
IENR1	Initialized	—	—	—	—	—	—	
IENR2	Initialized	—	—	—	—	—	—	
INTM	Initialized	—	—	—	—	—	—	
IRR1	Initialized	—	—	—	—	—	—	
IRR2	Initialized	—	—	—	—	—	—	
IWPR	Initialized	—	—	—	—	—	—	
CKSTPR1	Initialized	—	—	—	—	—	—	Syst
CKSTPR2	Initialized	—	—	—	—	—	—	

Notes: — is not initialized.

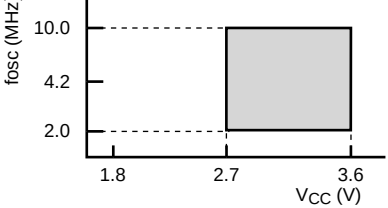
1. AEC: Asynchronous event counter
2. WDT: Watchdog timer
3. LCD: LCD controller/driver

Analog power supply voltage		AV_{CC}	–0.3 to +4.3	V
Input voltage	Other than port B	V_{in}	–0.3 to V_{CC} +0.3	V
	Port B	AV_{in}	–0.3 to AV_{CC} +0.3	V
Operating temperature		T_{opr}	–20 to +75 (regular specifications)*[2]	°C
			–40 to +85 (wide-range specifications)*[2]	
			+75 (products shipped as chips)*[3]	
Storage temperature		T_{stg}	–55 to +125	°C

Notes: 1. Permanent damage may occur to the chip if absolute maximum ratings are ex
Normal operation should be under the conditions specified in Electrical Chara
Exceeding these values can result in incorrect operation and reduced reliabili

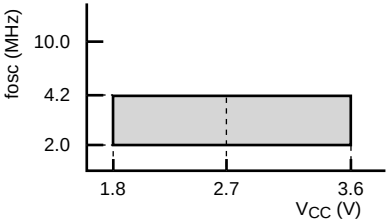
2. When the operating voltage (Vcc) for reading the flash memory is from 2.7 V
the operating temperature (Ta) for programming/erasing ranges from –20 to +
When the operating voltage (Vcc) for reading the flash memory is from 1.8 V
the operating temperature (Ta) for programming/erasing ranges from –20 to +

3. Power may be applied when the temperature is between –20 to +75°C.

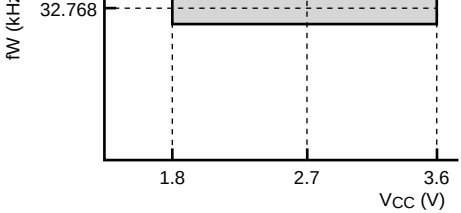


· Active (high-speed) mode
· Sleep (high-segment) mode
· Refer to no.1 in the note.

[4-MHz version]



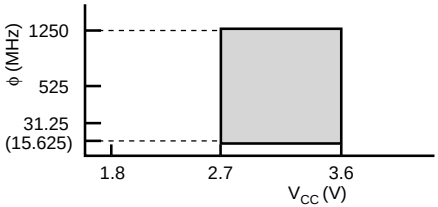
· Active (high-speed) mode
· Sleep (high-speed) mode
· Refer to no.1 in the note.



· All operating mode
· Refer to no. 2 in the note.

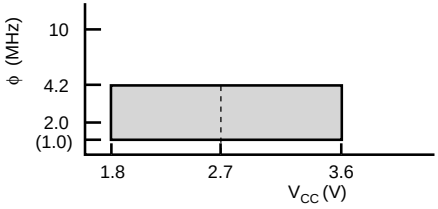
Notes: 1.The fosc values are those when a re
is used; when an external clock is u
minimum value of fosc is 2 MHz.
2. When a resonator is used, hold VC
2.2 V to 3.6 V from power-on until th
oscillation settling time has elapsed

· Refer to no.1 in the note.

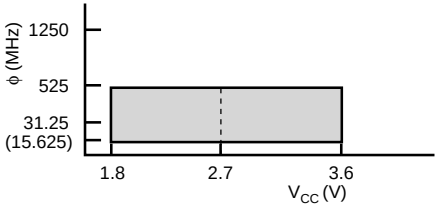


· Active (medium-speed) mode
· Sleep (medium-speed) mode (except A/D converter)
· Refer to no.2 in the note.

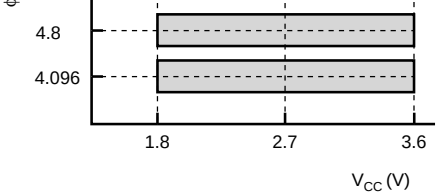
[4-MHz version]



· Active (high-speed) mode
· Sleep (high-speed) mode (except CPU)
· Refer to no.1 in the note.



· Active (medium-speed) mode
· Sleep (medium-speed) mode (except A/D converter)
· Refer to no.2 in the note.



· Subactive mode
· Subsleep mode (except CPU)
· Watch mode (except CPU)

Notes: 1. The value in parentheses is the minimu
frequency when an external clock is inp
using a resonator, the minimum operat
(φ) is 2 MHz.

2. The value in parentheses is the minimu
frequency when an external clock is inp
using a resonator, the minimum operat
(φ) is 31.25 kHz.

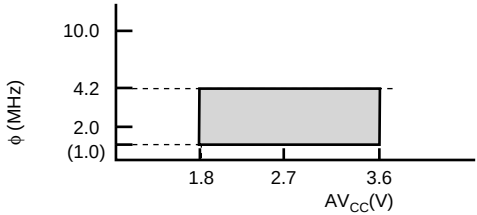
· Sleep (high-speed) mode

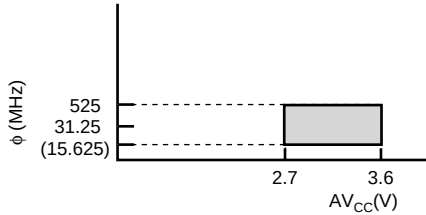
· Refer to no.1 in the note.

· Sleep (medium-speed) mode

· Refer to no.2 in the note.

[4-MHz version]





· Active (high-speed) mode

· Sleep (high-speed) mode

· Refer to no.1 in the note.

· Active (medium-speed) mode

· Sleep (medium-speed) mode

· Refer to no.2 in the note.

Notes: 1. The minimum operating frequency (ϕ) is 2 MHz when using a resonator; and 1 MHz when using an external clock.

2. The minimum operating frequency (ϕ) is 31.25 kHz when using a resonator; and 15.625 kHz when using an external clock.

voltage	to $\overline{\text{WKP7}}$, $\overline{\text{IRQ4}}$, AEVL, AEVH, TMIF, $\overline{\text{ADTRG}}$, SCK32, SCK31, SCK4				
	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ3}}$		0.9V_{cc}	—	AV_{cc} + 0.3
	RXD32, RXD31		0.8V_{cc}	—	V_{cc} + 0.3
	OSC1		0.9V_{cc}	—	V_{cc} + 0.3
	X1	V_{cc} = 2.7 to 3.6 V	0.9V_{cc}	—	V_{cc} + 0.3
	P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P93, PA0 to PA3, TCLKA, TCLKB, TCLKC, TIOCA1, TIOCA2, TIOCB1, TIOCB2, SCL, SDA		0.8V_{cc}	—	V_{cc} + 0.3
	PB0 to PB7		0.8V_{cc}	—	AV_{cc} + 0.3
	IRQAEC		0.9V_{cc}	—	V_{cc} + 0.3

		OSC1		–0.3	—	0.1V_{CC}	
		X1	V_{CC} = 2.7 to 3.6 V	–0.3	—	0.1V_{CC}	
		P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P93, PA0 to PA3, TCLKA, TCLKB, TCLKC, TIOCA1, TIOCB1, TIOCA2, TIOCB2, SCL, SDA, PB0 to PB7		–0.3	—	0.2V_{CC}	
Output high voltage	V_{OH}	P10, P16, P30 to P32, P36, P37 P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, PA0 to PA3	$-I_{OH}$ = 1.0 mA V_{CC} = 2.7 to 3.6 V	V_{CC} – 1.0	—	—	V
			$-I_{OH}$ = 0.1 mA	V_{CC} – 0.3	—	—	
		P90 to P93	I_{OH} = 1.0 mA V_{CC} = 2.7 to 3.6 V	V_{CC} – 1.0	—	—	
			I_{OH} = 0.1 mA	V_{CC} – 0.3	—	—	

			V_{CC} = 2.7 to 3.6 V				
			I_{OL} = 10 mA, V_{CC} = 2.2 to 3.6 V	—	—	0.5	
			I_{OL} = 8 mA V_{CC} = 1.8 to 3.6 V	—	—	0.5	
		SCL, SDA	V_{CC} = 2.0 to 3.6 V I_{OL} = 3.0 mA	—	—	0.4	
			V_{CC} = 1.8 to 2.0 V I_{OL} = 3.0 mA	—	—	$0.2V_{CC}$	
Input/output leakage current	$\lvert I_{IL} \rvert$	$\overline{NMI}$*[3], OSC1, X1, P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, IRQAEC, PA0 to PA3, P90 to P93	V_{IN} = 0.5 V to V_{CC} – 0.5 V	—	—	1.0	µA
		PB0 to PB7	V_{IN} = 0.5 V to AV_{CC} – 0.5 V	—	—	1.0	
Pull-up MOS current	$-I_p$	P10 to P16, P30, P36, P37, P50 to P57, P60 to P67	V_{CC} = 3.0 V, V_{IN} = 0 V	30	—	180	µA

			V_{CC} = 3.0 V, f_{OSC} = 4 MHz					g 1
			Active (high-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	6.6	10		*
	I_{OPE2}	V_{CC}	Active (medium-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{osc}/64	—	0.4	—	mA	* M g 1
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz, ϕ_{osc}/64	—	0.7	—		* M g 1
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz, ϕ_{osc}/64	—	1.1	1.8		*
Sleep mode current consumption	I_{SLEEP}	V_{CC}	V_{CC}= 1.8 V, f_{OSC}= 2 MHz	—	0.7	—	mA	* M g 1
			V_{CC}= 3.0 V, f_{OSC}= 4 MHz	—	1.7	—		* M g 1
			V_{CC}= 3.0 V, f_{OSC}= 10 MHz	—	3.5	5.0		*

mode current consumption			LCD on, 32-kHz crystal resonator ($\phi_{SUB} = \phi_w/2$)				
Watch mode current consumption	I_{WATCH}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C, 32-kHz crystal resonator, LCD not used	—	0.4	—	µA
			V_{CC} = 2.7 V, 32-kHz crystal resonator, LCD not used	—	2.0	6.0	
Standby mode current consumption	I_{STBY}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C, 32-kHz crystal resonator not used	—	0.4	—	µA
			V_{CC} = 3.0 V, Ta = 25°C, 32-kHz crystal resonator not used	—	0.6	—	
			32-kHz crystal resonator not used	—	1.0	5.0	
			V_{CC} = 3.0 V, 32KSTOP = 1	—	0.3	—	
RAM data retaining voltage	V_{RAM}	V_{CC}		1.5	—	—	V
Allowable output low current (per pin)	I_{OL}	Output pins except port 9		—	—	0.5	mA
		P90 to P93		—	—	15.0	

current (total)

Notes: 1. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator Pi
Active (high-speed) mode (I_{OPE1})	V_{cc}	Only CPU operates On-chip WDT oscillator is off	V_{cc}	Halted	System clock crystal reson
Active (medium-speed) mode (I_{OPE2})					Subclock osc Pin X1 = GN
Sleep mode	V_{cc}	Only on-chip timers operate On-chip WDT oscillator is off	V_{cc}	Halted	
Subactive mode	V_{cc}	Only CPU operates On-chip WDT oscillator is off	V_{cc}	Halted	System clock crystal reson
Subsleep mode	V_{cc}	Only on-chip timers operate, CPU stops On-chip WDT oscillator is off	V_{cc}	Halted	Subclock osc crystal reson
Watch mode	V_{cc}	Only time base operates, CPU stops On-chip WDT oscillator is off	V_{cc}	Halted	
Standby mode	V_{cc}	CPU and timers both stop On-chip WDT oscillator is off	V_{cc}	Halted	System clock crystal reson Subclock osc Pin X1 = GN (32KSTOP =

2. Excludes current in pull-up MOS transistors and output buffers.
3. Used for the determination of user mode or boot mode when the reset is releas
4. Except for the package for the TLP-85V.
5. Only for 4-MHz version.

System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	2.0	—	10.0	MHz
			V_{CC} = 1.8 to 3.6 V	2.0	—	4.2	
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	100	—	500 (1000)	ns
			V_{CC} = 1.8 to 3.6 V	238	—	500 (1000)	
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}
				—	—	64	µs
Subclock oscillation frequency	f_W	X1, X2		—	32.768 or 38.4	—	kHz
Watch clock (ϕ_W) cycle time	t_W	X1, X2		—	30.5 or 26.0	—	µs
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}			2	—	8	t_W
Instruction cycle time				2	—	—	t_{cyc} t_{subcyc}
Oscillation stabilization time	t_{rc}	OSC1, OSC2	Crystal resonator (V_{CC} = 2.7 to 3.6 V)	—	0.8	2.0	ms
			Crystal resonator (V_{CC} = 2.2 to 3.6 V)	—	1.2	3	
			Ceramic resonator (V_{CC} = 2.2 to 3.6 V)	—	20	45	µs
			Ceramic resonator (other than above)	—	80	—	
			Other than above	—	—	50	ms
		×1, ×2	V_{CC} = 2.2 to 3.6 V	—	—	2.0	s
			Other than above	—	4	—	

			V_{CC} = 1.8 to 3.6 V	95	—	—		
		X1		—	15.26 or 13.02	—	µs	
External clock F time	t_{CPr}	OSC1	V_{CC} = 2.7 to 3.6 V	—	—	10	ns	F
			V_{CC} = 1.8 to 3.6 V	—	—	24		
		X1		—	—	55.0		
External clock fall time	t_{CPf}	OSC1	V_{CC} = 2.7 to 3.6 V	—	—	10	ns	F
			V_{CC} = 1.8 to 3.6 V	—	—	24		
		X1		—	—	55.0		
$\overline{RES}$ pin low width	t_{REL}	$\overline{RES}$		10	—	—	t_{cyc}	F 2
Input pin high width	t_{IH}	$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{NMI}$, $\overline{IRQ3}$, $\overline{IRQ4}$, IRQAEC, $\overline{WKP0}$ to $\overline{WKP7}$, TMIF, $\overline{ADTRG}$		2	—	—	t_{cyc} t_{subcyc}	F
		AEVL, AEVH	V_{CC} = 2.7 to 3.6 V	50	—	—	ns	
			V_{CC} = 1.8 to 3.6 V	110	—	—		
	t_{TCKWH}	TCLKA, TCLKB, TCLKC, TIOCA1, TIOCB1, TIOCA2, TIOCB2	Single edge specified	1.5	—	—	t_{cyc}	F
			Both edges specified	2.5	—	—		

TCLKC, TIOCA1, TIOCB1, TIOCA2, TIOCB2	Single edge specified	1.5	—	—	
	Both edges specified	2.5	—	—	

Notes: 1. Selected with the SA1 and SA0 bits in the system control register 2 (SYSCR2
2. The value in parentheses is t_{OSC} (max.) when an external clock is used.
3. For details on the power-on reset characteristics, refer to table 24.8 and figur

Table 24.4 Serial Interface Timing

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise speci

Item		Symbol	Test Condition	Values Min.	Typ.	Max.	Unit
Input clock cycle	Asynchronous	t_{scyc}		4	—	—	t_{cyc} or t_{subcyc}
	Clocked synchronous			6	—	—	
Input clock pulse width		t_{SCKW}	0.4	0.4	—	0.6	t_{scyc}
Transmit data delay time (clocked synchronous)		t_{TXD}	—	—	—	1	t_{cyc} or t_{subcyc}
Receive data setup time (clocked synchronous)		t_{RXS}		238	—	—	ns
			V_{CC} = 2.7 to 3.6 V	100			
Receive data hold time (clocked synchronous)		t_{RXH}		238	—	—	ns
			V_{CC} = 2.7 to 3.6 V	100			

SCL and SDA input spike pulse removal time	t_{SP}	—	—	$1t_{cyc}$	ns
SDA input bus-free time	t_{BUF}	$5t_{cyc}$	—	—	ns
Start condition input hold time	t_{STAH}	$3t_{cyc}$	—	—	ns
Retransmission start condition input setup time	t_{STAS}	$3t_{cyc}$	—	—	ns
Setup time for stop condition input	t_{STOS}	$3t_{cyc}$	—	—	ns
Data-input setup time	t_{SDAS}	$1t_{cyc}$ + 20	—	—	ns
Data-input hold time	t_{SDAH}	0	—	—	ns
Capacitive load of SCL and SDA	Cb	0	—	400	pF
SCL and SDA output fall time	t_{Sf}	—	—	300	ns

24.2.4 A/D Converter Characteristics

Table 24.6 lists the A/D converter characteristics.

	AI_{STOP2}	AV_{CC}		—	—	5	µA
Analog input capacitance	C_{AIN}	AN0 to AN7		—	—	15.0	pF
Allowable signal source impedance	R_{AIN}			—	—	10.0	kΩ
Resolution (data length)				—	—	10	bits
Nonlinearity error			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	—	—	±3.5	LSB
			AV_{CC} = 2.0 V to 3.6 V V_{CC} = 2.0 V to 3.6 V	—	—	±5.5	
			Other than above	—	—	±7.5	
Quantization error				—	—	±0.5	LSB
Absolute accuracy			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	—	—	±4.0	LSB
			AV_{CC} = 2.0 V to 3.6 V V_{CC} = 2.0 V to 3.6 V	—	—	±6.0	
			Other than above	—	—	±8.0	
Conversion time			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	6.2	—	124	µs
			AV_{CC} = 2.0 V to 3.6 V V_{CC} = 2.0 V to 3.6 V	14.7	—	124	
			Other than above	31	—	124	

Notes: 1. Set AV_{CC} = V_{CC} when the A/D converter is not used.
2. AI_{STOP1} is the current in active and sleep modes while the A/D converter is idle
3. AI_{STOP2} is the current at a reset and in standby, watch, subactive, and subsleep while the A/D converter is idle.
4. Conversion time = 31 µs

Common driver drop voltage	V_{DC}	COM1 to COM4	I_D = 2 µA V1 = 2.7 V to 3.6 V	—	—	0.3	V
LCD power supply split-resistance	R_{LCD}		Between V1 and V_{SS}	1.5	3.0	7.0	MΩ
LCD display voltage	V_{LCD}	V1		2.2	—	3.6	V
V3 power supply voltage	V_{LCD3}	V3	Between V3 and V_{SS}	0.9	1.0	1.1	V
V2 power supply voltage	V_{LCD2}	V2	Between V2 and V_{SS}	—	2.0 (V_{LCD3} × 2)	—	V
V1 power supply voltage	V_{LCD1}	V1	Between V1 and V_{SS}	—	3.0 (V_{LCD3} × 3)	—	V
3-V constant voltage LCD power supply circuit current consumption	I_{LCD}	Vcc	Vcc = 3.0 V Booster clock: 125 kHz	—	20	—	µA

Notes: 1. The voltage drop from power supply pins V1, V2, V3, and V_{SS} to each segment
common pin.
2. When the LCD display voltage is supplied from an external power source, ensu
the following relationship is maintained: V1 ≥ V2 ≥ V3 ≥ V_{SS}.
3. The value when the LCD power supply split-resistor is separated and 3-V cons
voltage power supply circuit is driven.
4. For details on the register (BGRMR) setting range when the voltage of the V3
to 1.0 V, refer to section 19.3.5, BGR Control Register (BGRMR).
5. Includes the current consumption of the band-gap reference circuit (BGR) (ope

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Reset voltage	V_rst		0.7Vcc	0.8Vcc	0.9Vcc	V
Power supply rise time	t_vtr		The Vcc rise time should be shorter than half the $\overline{RES}$ rise time.			
Reset count time	t_out		0.8	—	8.0	µs
Count start time	t_cr		Adjustable by the value of the external capacitor of the $\overline{RES}$ pin.			
On-chip pull-up resistance	Rp	Vcc = 3.0 V	60	100	—	kΩ

24.2.7 Watchdog Timer Characteristics

Table 24.9 Watchdog Timer Characteristics

V_{CC} = 1.8 V to 3.6 V, AV_{CC} = 1.8 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V,
Ta = –20 to +75°C (regular specifications), Ta = –40 to +85°C (wide-range specification
unless otherwise specified.

		Applicable		Values				
Item	Symbol	Pins	Test Condition	Min.	Typ.	Max.	Unit	
On-chip oscillator overflow time	t_{ovf}			0.2	0.4	—	s	

wide-range specifications, products shipped as chips)

Condition B:

AV_{CC} = 1.8 V to 3.6 V, DV_{CC} = 2.2 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, V_{CC} = 1.8 V to 3.6 V (
voltage range in reading), V_{CC} = 3.0 V to 3.6 V (operating voltage range in programming/
Ta = –20 to +50°C (operating temperature range in programming/erasing: regular specifi
wide-range specifications)

Item		Symbol	Test Condition	Values Min.	Typ.	Max.
Programming time (per 128 bytes)*1*2*4		t_p		—	7	200
Erase time (per block)*1*3*6		t_E		—	100	1200
Maximum number of reprogrammings		N_{WEC}		1000*8*11	10000*9	—
				100*8*12	10000*9	—
Data retention time		t_{DRP}		10*10	—	—
Programming	Wait time after SWE bit setting*1	x		1	—	—
	Wait time after PSU bit setting*1	y		50	—	—
	Wait time after P bit setting*1*4	z1	1 ≤ n ≤ 6	28	30	32
		z2	7 ≤ n ≤ 1000	198	200	202
		z3	Additional-programming	8	10	12
	Wait time after P bit clear*1	α		5	—	—
	Wait time after PSU bit clear*1	β		5	—	—
	Wait time after PV bit setting*1	γ		4	—	—
	Wait time after dummy write*1	ε		2	—	—
	Wait time after PV bit clear*1	η		2	—	—
	Wait time after SWE bit clear*1	θ		100	—	—
	Maximum programming count*1*4*5	N		—	—	1000

Wait time after SWE bit clear	z_0	100			
Maximum erase count*[1]*[6]*[7]	N	—	—	120	

Notes:
1. Make the time settings in accordance with the program/erase algorithms.
2. The programming time for 128 bytes. (Indicates the total time for which the P flash memory control register 1 (FLMCR1) is set. The program-verify time is included.)
3. The time required to erase one block. (Indicates the total time for which the E flash memory control register 1 (FLMCR1) is set. The erase-verify time is no included.)
4. Programming time maximum value (t_P (max.)) = wait time after P bit setting (maximum number of programmings (N)
5. Set the maximum number of programmings (N) according to the actual set v z1, z2, and z3, so that it does not exceed the programming time maximum v (max.)). The wait time after P bit setting (z1, z2) should be changed as follow according to the value of the number of programmings (n).

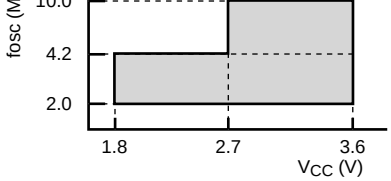
   Number of programmings (n)

   $1 \leq n \leq 6$ z1 = 30 µs

   $7 \leq n \leq 1000$ z2 = 200 µs
6. Erase time maximum value (t_E (max.)) = wait time after E bit setting (z) × ma number of erases (N)
7. Set the maximum number of erases (N) according to the actual set value of it does not exceed the erase time maximum value (t_E (max.)).
8. The minimum number of times in which all characteristics are guaranteed fo reprogramming. (The guarantee covers the range from 1 to the minimum val
9. Reference value at 25°C. (Guideline showing number of reprogrammings ov functioning will be retained under normal circumstances.)
10. Data retention characteristics within the range indicated in the specifications the minimum value for reprogrammings.
11. Applies to an operating voltage range when reading data of 2.7 to 3.6 V.
12. Applies to an operating voltage range when reading data of 1.8 to 3.6 V.

	Port B	AV_{in}	–0.3 to AV_{CC} +0.3	V
Operating temperature		T_{opr}	–20 to +75 (regular specifications)	°C
			–40 to +85 (wide-range specifications)	
			+75 (products shipped as chips)*[2]	
Storage temperature		T_{stg}	–55 to +125	°C

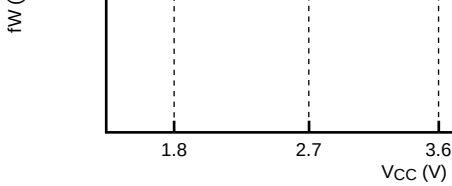
Notes: 1. Permanent damage may occur to the chip if absolute maximum ratings are exc
Normal operation should be under the conditions specified in Electrical Charac
Exceeding these values can result in incorrect operation and reduced reliability
2. Power may be applied when the temperature is between –20 and +75°C.



· Active (high-speed) mode

· Sleep (high-speed) mode

· Refer to no.1 in the note.

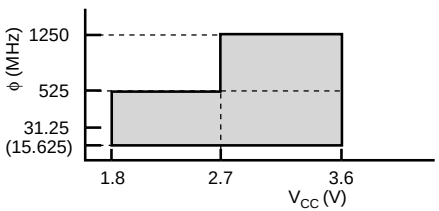


· All operating mode

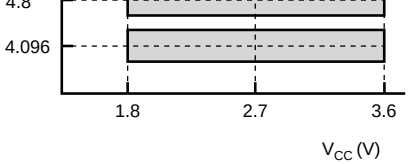
· Refer to no.2 in the note.

Notes: 1.The fosc values are those when a
is used; when an external clock is
minimum value of fosc is 1 MHz.

2. When a resonator is used, hold V
2.2 V to 3.6 V from power-on until
oscillation settling time has elapse



· Active (medium-speed) mode
· Sleep (medium-speed) mode (except A/D converter)
· Refer to no.2 in the note.



· Subactive mode
· Subsleep mode (except CPU)
· Watch mode (except CPU)

Notes: 1. The value in parentheses is the minimur frequency when an external clock is inpu using a resonator, the minimum operatin (ϕ) is 2 MHz.

2. The value in parentheses is the minimur frequency when an external clock is inpu using a resonator, the minimum operatin (ϕ) is 31.25 kHz.

Refer to no.1 in the note. Refer to no.2 in the note.

Notes: 1. The minimum operating frequency (ϕ) is 2 MHz when using a resonator; and 1 MHz when using an external clock.

2. The minimum operating frequency (ϕ) is 31.25 kHz when using a resonator; and 15.625 kHz when using an external clock.

voltage	$\overline{WKP7}$, $\overline{IRQ4}$, AEVL, AEVH, TMIF, $\overline{ADTRG}$, SCK32, SCK31			
	$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ3}$	0.9V_{cc}	—	AV_{cc} + 0.3
	RXD32, RXD31	0.8V_{cc}	—	V_{cc} + 0.3
	OSC1	0.9V_{cc}	—	V_{cc} + 0.3
	X1 (V_{cc} = 2.7 to 3.6 V)	0.9V_{cc}	—	V_{cc} + 0.3
	P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P93, PA0 to PA3, TCLKA, TCLKB, TCLKC, TIOCA1, TIOCA2, TIOCB1, TIOCB2, SCL, SDA	0.8V_{cc}	—	V_{cc} + 0.3
	PB0 to PB7	0.8V_{cc}	—	AV_{cc} + 0.3
	IRQAEC	0.9V_{cc}	—	V_{cc} + 0.3

		X1	V_{CC} = 2.7 to 3.6 V	–0.3	—	0.1V_{CC}	
		P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P93, PA0 to PA3, TCLKA, TCLKB, TCLKC, TIOCA1, TIOCB1, TIOCA2, TIOCB2, SCL, SDA, PB0 to PB7		–0.3	—	0.2V_{CC}	
Output high voltage	V_{OH}	P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, PA0 to PA3	$-I_{OH}$ = 1.0 mA V_{CC} = 2.7 to 3.6 V	V_{CC} – 1.0	—	—	V
			$-I_{OH}$ = 0.1 mA	V_{CC} – 0.3	—	—	
		P90 to P93	$-I_{OH}$ = 1.0 mA V_{CC} = 2.7 to 3.6 V	V_{CC} – 1.0	—	—	
			$-I_{OH}$ = 0.1 mA	V_{CC} – 0.3	—	—	

			V_{CC} = 2.7 to 3.6 V				
			I_{OL} = 10 mA V_{CC} = 2.2 to 3.6 V	—	—	0.5	
			I_{OL} = 8.0 mA V_{CC} = 1.8 to 3.6 V	—	—	0.5	
		SCL, SDA	V_{CC} = 2.0 to 3.6 V I_{OL} = 3.0 mA	—	—	0.4	V
			V_{CC} = 1.8 to 2.0 V I_{OL} = 3.0 mA	—	—	$0.2V_{CC}$	
Input/output leakage current	$\lvert I_{IL} \rvert$	$\overline{\text{NMI}}$, OSC1, X1, P10 to P16, P30 to P32, P36, P37, P40 to P42, P50 to P57, P60 to P67, P70 to P77, P80 to P87, IRQAEC, PA0 to PA3, P90 to P93	V_{IN} = 0.5 V to V_{CC} – 0.5 V	—	—	1.0	µA
		PB0 to PB7	V_{IN} = 0.5 V to AV_{CC} – 0.5 V	—	—	1.0	
Pull-up MOS current	$-I_p$	P10 to P16, P30, P36, P37, P50 to P57, P60 to P67	V_{CC} = 3 V, V_{IN} = 0 V	30	—	180	µA
Input capacitance*[3]	C_{IN}	All input pins except power supply pin	f = 1 MHz, V_{IN} =0 V, Ta = 25°C	—	—	15.0	pF

			V_{CC} = 3.0 V, f_{OSC} = 10 MHz				
	I_{OPE2}	V_{CC}	Active (medium-speed) mode, V_{CC} = 1.8 V, f_{OSC} = 2 MHz, ϕ_{osc}/64	—	0.2	—	mA
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 4 MHz, ϕ_{osc}/64	—	0.4	—	
			Active (medium-speed) mode, V_{CC} = 3.0 V, f_{OSC} = 10 MHz, ϕ_{osc}/64	—	0.8	1.8	
Sleep mode current consumption	I_{SLEEP}	V_{CC}	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	—	0.3	—	mA
			V_{CC} = 3.0 V, f_{OSC} = 4 MHz	—	1.2	—	
			V_{CC} = 3.0 V, f_{OSC} = 10 MHz	—	3.0	5.0	

Subsleep mode current consumption	I_{SUBSP}	V_{CC}	V_{CC} = 2.7 V, LCD on, 32-kHz crystal resonator ($\phi_{SUB} = \phi_w/2$)	—	4.5	10	µA
Watch mode current consumption	I_{WATCH}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C, 32-kHz crystal resonator, LCD not used	—	0.5	—	µA
			V_{CC} = 2.7 V, 32-kHz crystal resonator, LCD not used	—	1.6	6.0	
Standby mode current consumption	I_{STBY}	V_{CC}	V_{CC} = 1.8 V, Ta = 25°C, 32-kHz crystal resonator not used	—	0.4	—	µA
			V_{CC} = 3.0 V, Ta = 25°C, 32-kHz crystal resonator not used	—	0.6	—	
			32-kHz crystal resonator not used	—	1.0	5.0	
			V_{CC} = 3.0 V, 32KSTOP = 1	—	0.3	—	
RAM data retaining voltage	V_{RAM}	V_{CC}		1.5	—	—	V
Allowable output low current (per pin)	I_{OL}	Output pins except port 9		—	—	0.5	mA
		P90 to P93		—	—	15.0	

current (total)

Notes: 1. Pin states during current measurement.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	LCD Power Supply	Oscillator
Active (high-speed) mode (I_{OPE1})	V_{cc}	Only CPU operates On-chip WDT oscillator is off	V_{cc}	Halted	System clo crystal reso
Active (medium-speed) mode (I_{OPE2})					Subclock os Pin X1 = GI
Sleep mode	V_{cc}	Only on-chip timers operate On-chip WDT oscillator is off	V_{cc}	Halted	
Subactive mode	V_{cc}	Only CPU operates On-chip WDT oscillator is off	V_{cc}	Halted	System clo crystal reso
Subsleep mode	V_{cc}	Only on-chip timers operate, CPU stops On-chip WDT oscillator is off	V_{cc}	Halted	Subclock os crystal reso
Watch mode	V_{cc}	Only time base operates, CPU stops On-chip WDT oscillator is off TCSRWD1 (WDON) = 0	V_{cc}	Halted	
Standby mode	V_{cc}	CPU and timers both stop On-chip WDT oscillator is off TCSRWD1 (WDON) = 0	V_{cc}	Halted	System clo crystal reso Subclock os Pin X1 = GI (32KSTOP

2. Excludes current in pull-up MOS transistors and output buffers.
3. Except for the package for the TLP-85V.

System clock oscillation frequency	f_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	2.0	—	10.0	MHz	
			V_{CC} = 1.8 to 3.6 V	2.0	—	4.2		
On-chip oscillator oscillation frequency	R_{OSC}		When on-chip oscillator is selected V_{CC} = 2.7 to 3.6 V	1.0	—	10.0		*4
			When on-chip oscillator is selected V_{CC} = 1.8 to 2.7 V	0.5	—	4.2		
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC1, OSC2	V_{CC} = 2.7 to 3.6 V	100	—	500 (1000)	ns	Fi *2
			V_{CC} = 1.8 to 3.6 V	238	—	500 (1000)		
On-chip oscillator clock (ϕ_{OSC}) cycle time	t_{ROSC}		When on-chip oscillator is selected V_{CC} = 2.7 to 3.6 V	100	—	1000		*4
			When on-chip oscillator is selected V_{CC} = 1.8 to 2.7 V	238	—	2000		
System clock (ϕ) cycle time	t_{cyc}			1	—	64	t_{OSC}	
				—	—	64	µs	
Subclock oscillation frequency	f_w	X1, X2		—	32.768 or 38.4	—	kHz	Fi
Watch clock (ϕ_w) cycle time	t_w	X1, X2		—	30.5 or 26.0	—	µs	Fi
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}			2	—	8	t_w	*1
Instruction cycle time				2	—	—	t_{cyc} t_{subcyc}	

			Other than above	—	—	50	ms
			When on-chip oscillator is selected	—	—	100	µs
		X1, X2	V_{CC} = 2.2 to 3.6 V	—	—	2.0	s
			Other than above	—	4	—	
External clock high width	t_{CPH}	OSC1	V_{CC} = 2.7 to 3.6 V	40	—	—	ns
			V_{CC} = 1.8 to 3.6 V	95	—	—	
		X1		—	15.26 or 13.02	—	µs
External clock low width	t_{CPL}	OSC1	V_{CC} = 2.7 to 3.6 V	40	—	—	ns
			V_{CC} = 1.8 to 3.6 V	95	—	—	
		X1		—	15.26 or 13.02	—	µs
External clock rise time	t_{CPr}	OSC1	V_{CC} = 2.7 to 3.6 V	—	—	10	ns
			V_{CC} = 1.8 to 3.6 V	—	—	24	
		X1		—	—	55.0	ns
External clock fall time	t_{CPf}	OSC1	V_{CC} = 2.7 to 3.6 V	—	—	10	ns
			V_{CC} = 1.8 to 3.6 V	—	—	24	
		X1		—	—	55.0	ns
$\overline{RES}$ pin low width	t_{REL}	$\overline{RES}$		10	—	—	t_{cyc}

		TIOCA1, TIOCB1, TIOCA2, TIOCB2						
			Both edges specified	2.5	—	—		
Input pin low width	t_{IL}	$\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{NMI}$, $\overline{IRQ3}$, $\overline{IRQ4}$, IRQAEC, $\overline{WKP0}$ to $\overline{WKP7}$, TMIF, $\overline{ADTRG}$		2	—	—	t_{cyc} t_{subcyc}	Fi
		AEVL, AEVH	V_{CC} = 2.7 to 3.6 V	50	—	—	ns	
			V_{CC} = 1.8 to 3.6 V	110	—	—		
	t_{TCKWL}	TCLKA, TCLKB, TCLKC, TIOCA1, TIOCB1, TIOCA2, TIOCB2	Single edge specified	1.5	—	—	t_{cyc}	Fi
			Both edges specified	2.5	—	—		

Notes: 1. Selected with the SA1 and SA0 bits in the system control register 2 (SYSCR2)
2. The value in parentheses is t_{OSC} (max.) when an external clock is used.
3. For details on the power-on reset characteristics, refer to table 24.18 and figur
4. Characteristics vary due to variations in factors such as temperature, power su voltage, and production lot. When designing the system, give due consideratio actual usage conditions. For actual data on this product, please contact a Ren representative.

(clocked synchronous)	t_{TXD}					cyc	subcyc
Receive data setup time (clocked synchronous)	t_{RXS}		238	—	—	ns	Fig
		V_{cc} = 2.7 to 3.6 V	100				
Receive data hold time (clocked synchronous)	t_{RXH}		238	—	—	ns	Fig
		V_{cc} = 2.7 to 3.6 V	100				

SCL and SDA input spike pulse removal time	t_{SP}	—	—	$1t_{cyc}$	ns
SDA input bus-free time	t_{BUF}	$5t_{cyc}$	—	—	ns
Start condition input hold time	t_{STAH}	$3t_{cyc}$	—	—	ns
Retransmission start condition input setup time	t_{STAS}	$3t_{cyc}$	—	—	ns
Setup time for stop condition input	t_{STOS}	$3t_{cyc}$	—	—	ns
Data-input setup time	t_{SDAS}	$1t_{cyc}$ + 20	—	—	ns
Data-input hold time	t_{SDAH}	0	—	—	ns
Capacitive load of SCL and SDA	Cb	0	—	400	pF
SCL and SDA output fall time	t_{Sf}	—	—	300	ns

voltage							
Analog input voltage	AV_{IN}	AN0 to AN7		–0.3	—	AV_{CC} + 0.3	V
Analog power supply current	AI_{OPE}	AV_{CC}	AV_{CC} = 3.0 V	—	—	1.0	mA
	AI_{STOP1}	AV_{CC}		—	600	—	µA
	AI_{STOP2}	AV_{CC}		—	—	5	µA
Analog input capacitance	C_{AIN}	AN0 to AN7		—	—	15.0	pF
Allowable signal source impedance	R_{AIN}			—	—	10.0	kΩ
Resolution (data length)				—	—	10	bits
Nonlinearity error			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	—	—	±3.5	LSB
			AV_{CC} = 2.0 V to 3.6 V V_{CC} = 2.0 V to 3.6 V	—	—	±5.5	
			Other than above	—	—	±7.5	
Quantization error				—	—	±0.5	LSB
Absolute accuracy			AV_{CC} = 2.7 V to 3.6 V V_{CC} = 2.7 V to 3.6 V	—	—	±4.0	LSB
			AV_{CC} = 2.0 V to 3.6 V V_{CC} = 2.0 V to 3.6 V	—	—	±6.0	
			Other than above	—	—	±8.0	

while the A/D converter is idle.

4. Conversion time = 62 μs

voltage		SEG32	V1 = 2.7 V to 3.6 V					
Common driver drop voltage	V_{DC}	COM1 to COM4	I_D = 2 µA V1 = 2.7 V to 3.6 V	—	—	0.3	V	
LCD power supply split-resistance	R_{LCD}		Between V1 and V_{SS}	1.5	3.0	7.0	MΩ	
LCD display voltage	V_{LCD}	V1		2.2	—	3.6	V	
V3 power supply voltage	V_{LCD3}	V3	Between V3 and V_{SS}	0.9	1.0	1.1	V	
V2 power supply voltage	V_{LCD2}	V2	Between V2 and V_{SS}	—	2.0 (V_{LCD3} × 2)	—	V	
V1 power supply voltage	V_{LCD1}	V1	Between V1 and V_{SS}	—	3.0 (V_{LCD3} × 3)	—	V	
3-V constant voltage LCD power supply circuit current consumption	I_{LCD}	Vcc	V_{CC} = 3.0 V Booster clock: 125 kHz	—	20	—	µA	

Notes: 1. The voltage drop from power supply pins V1, V2, V3, and V_{SS} to each segmen common pin.

2. When the LCD display voltage is supplied from an external power source, ens the following relationship is maintained: V1 ≥ V2 ≥ V3 ≥ V_{SS}.

3. The value when the LCD power supply split-resistor is separated and 3-V cor voltage power supply circuit is driven.

4. For details on the register (BGRMR) setting range when the voltage of the V3 to 1.0 V, refer to section 19.3.5, BGR Control Register (BGRMR).

5. Includes the current consumption of the band-gap reference circuit (BGR) (op

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Fi
Reset voltage	V_rst		0.7Vcc	0.8Vcc	0.9Vcc	V	Fi
Power supply rise time	t_vtr		The Vcc rise time should be shorter than half the $\overline{\text{RES}}$ rise time.				
Reset count time	t_out		0.8	—	4.0	µs	
Count start time	t_cr		Adjustable by the value of the external capacitor of the $\overline{\text{RES}}$ pin.				
On-chip pull-up resistance	Rp	Vcc = 3.0 V	60	100	—	kΩ	Fi

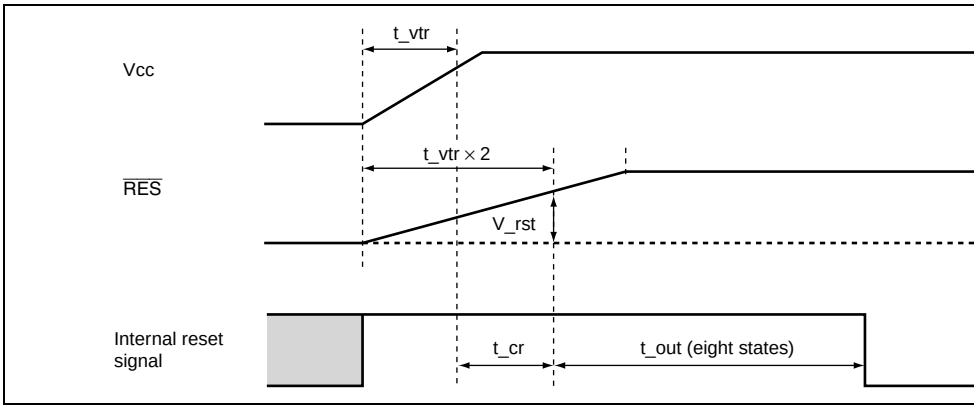


Figure 24.1 Power-On Reset Circuit Reset Timing

24.5 Operation Timing

Figures 24.2 to 24.7 show operation timings.

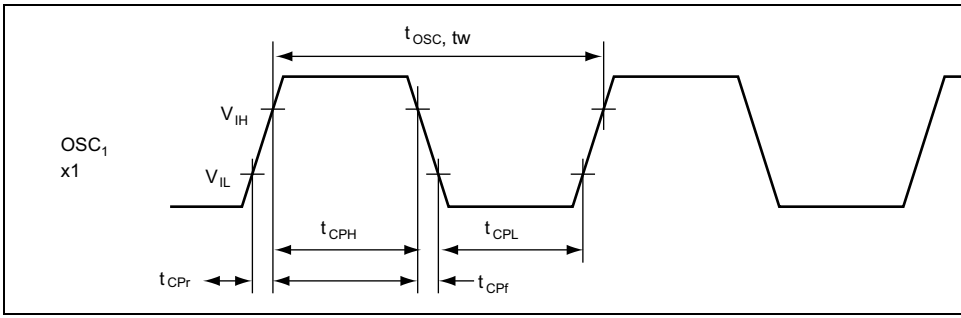


Figure 24.2 Clock Input Timing

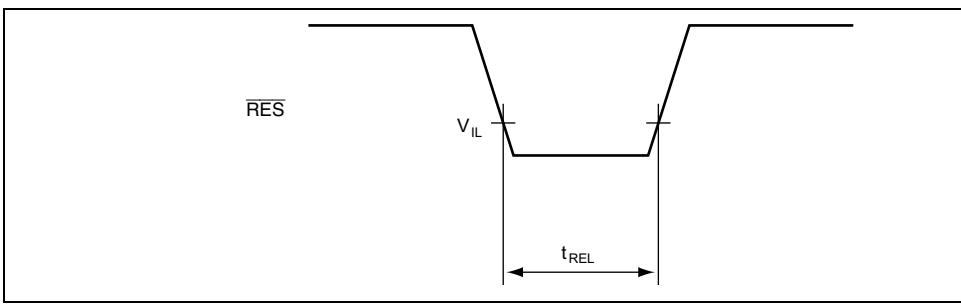


Figure 24.3 $\overline{RES}$ Low Width Timing

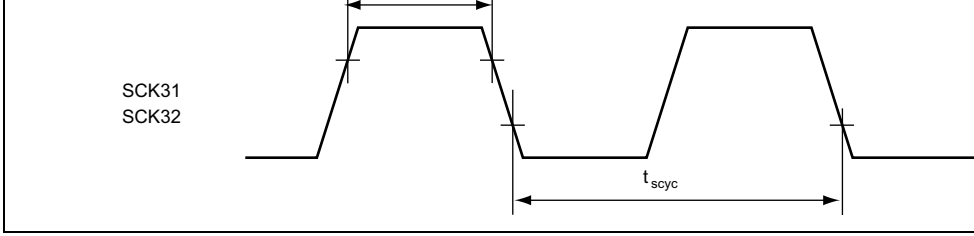
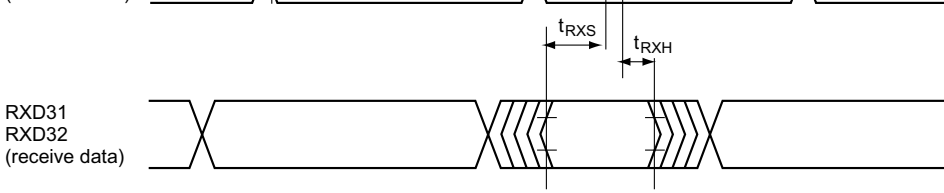


Figure 24.5 SCK3 Input Clock Timing



Note: * Output timing reference levels

Output high	V_{OH} = 1/2 Vcc + 0.2 V
Output low	V_{OL} = 0.8 V

Load conditions are shown in figure 24.9.

Figure 24.6 SCI3 Input/Output Timing in Clocked Synchronous Mode

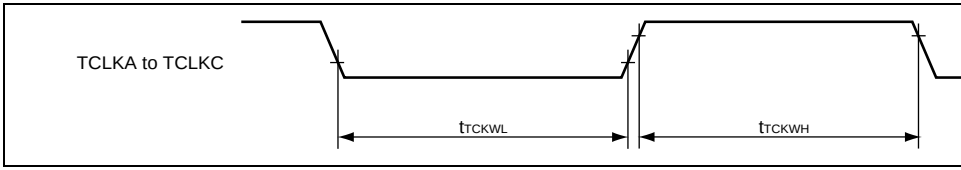


Figure 24.7 Clock Input Timing for TCLKA to TCLKC Pins

Note: * S, P, and Sr represent the following:
S: Start condition
P: Stop condition
Sr: Retransmission start condition

Figure 24.8 I²C Bus Interface Input/Output Timing

24.6 Output Load Circuit

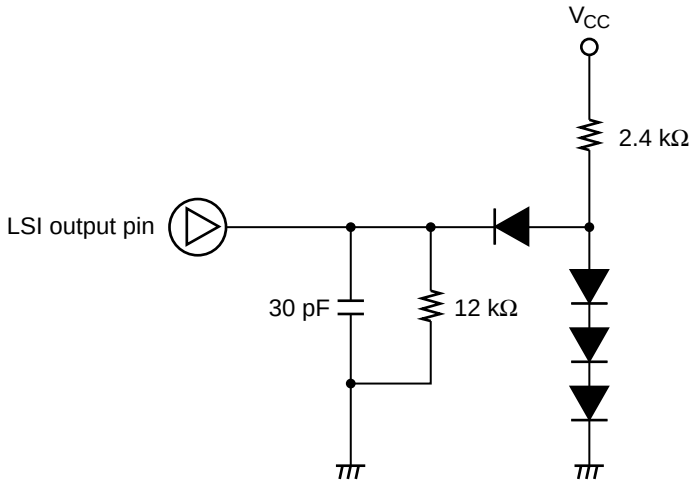


Figure 24.9 Output Load Condition

Frequency (MHz)	Manufacturer	Product Type
2	Murata Manufacturing Co., Ltd.	CSTCC2M00G53-B0
	Murata Manufacturing Co., Ltd.	CSTCC2M00G56-B0
4.194	Murata Manufacturing Co., Ltd.	CSTLS4M19G53-B0
	Murata Manufacturing Co., Ltd.	CSTLS4M19G56-B0
10	Murata Manufacturing Co., Ltd.	CSTLS10M0G53-B0
	Murata Manufacturing Co., Ltd.	CSTLS10M0G56-B0

24.8 Usage Note

The F-ZTAT and masked ROM versions satisfy the electrical characteristics shown in th
manual, but actual electrical characteristic values, operating margins, noise margins, and
properties may vary due to differences in manufacturing process, on-chip ROM, layout p
and so on.

When system evaluation testing is carried out using the F-ZTAT version, the same evalu
testing should also be conducted for the masked ROM version when changing over to th

Rs	General source register
Rn	General register
ERd	General destination register (address register or 32-bit register)
ERs	General source register (address register or 32-bit register)
ERn	General register (32-bit register)
(EAd)	Destination operand
(EAs)	Source operand
PC	Program counter
SP	Stack pointer
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
disp	Displacement
→	Transfer from the operand on the left to the operand on the right, or trans the state on the left to the state on the right
+	Addition of the operands on both sides
–	Subtraction of the operand on the right from the operand on the left
×	Multiplication of the operands on both sides
÷	Division of the operand on the left by the operand on the right
∧	Logical AND of the operands on both sides
∨	Logical OR of the operands on both sides
⊕	Logical exclusive OR of the operands on both sides

*	Undetermined (no guaranteed value)
0	Cleared to 0
1	Set to 1
—	Not affected by execution of the instruction
Δ	Varies depending on conditions, described in notes

	MOV.B @ERs, Rd	B			2						@ERs → Rd8	—	—	↕	↕	0
	MOV.B @(d:16, ERs), Rd	B				4					@(d:16, ERs) → Rd8	—	—	↕	↕	0
	MOV.B @(d:24, ERs), Rd	B				8					@(d:24, ERs) → Rd8	—	—	↕	↕	0
	MOV.B @ERs+, Rd	B					2				@ERs → Rd8 ERs32+1 → ERs32	—	—	↕	↕	0
	MOV.B @aa:8, Rd	B						2			@aa:8 → Rd8	—	—	↕	↕	0
	MOV.B @aa:16, Rd	B						4			@aa:16 → Rd8	—	—	↕	↕	0
	MOV.B @aa:24, Rd	B						6			@aa:24 → Rd8	—	—	↕	↕	0
	MOV.B Rs, @ERd	B			2						Rs8 → @ERd	—	—	↕	↕	0
	MOV.B Rs, @(d:16, ERd)	B				4					Rs8 → @(d:16, ERd)	—	—	↕	↕	0
	MOV.B Rs, @(d:24, ERd)	B				8					Rs8 → @(d:24, ERd)	—	—	↕	↕	0
	MOV.B Rs, @–ERd	B					2				ERd32–1 → ERd32 Rs8 → @ERd	—	—	↕	↕	0
	MOV.B Rs, @aa:8	B						2			Rs8 → @aa:8	—	—	↕	↕	0
	MOV.B Rs, @aa:16	B						4			Rs8 → @aa:16	—	—	↕	↕	0
	MOV.B Rs, @aa:24	B						6			Rs8 → @aa:24	—	—	↕	↕	0
	MOV.W #xx:16, Rd	W	4								#xx:16 → Rd16	—	—	↕	↕	0
	MOV.W Rs, Rd	W		2							Rs16 → Rd16	—	—	↕	↕	0
	MOV.W @ERs, Rd	W			2						@ERs → Rd16	—	—	↕	↕	0
	MOV.W @(d:16, ERs), Rd	W				4					@(d:16, ERs) → Rd16	—	—	↕	↕	0
	MOV.W @(d:24, ERs), Rd	W				8					@(d:24, ERs) → Rd16	—	—	↕	↕	0
	MOV.W @ERs+, Rd	W					2				@ERs → Rd16 ERs32+2 → @ERd32	—	—	↕	↕	0
	MOV.W @aa:16, Rd	W						4			@aa:16 → Rd16	—	—	↕	↕	0
	MOV.W @aa:24, Rd	W						6			@aa:24 → Rd16	—	—	↕	↕	0
	MOV.W Rs, @ERd	W			2						Rs16 → @ERd	—	—	↕	↕	0
	MOV.W Rs, @(d:16, ERd)	W				4					Rs16 → @(d:16, ERd)	—	—	↕	↕	0
	MOV.W Rs, @(d:24, ERd)	W				8					Rs16 → @(d:24, ERd)	—	—	↕	↕	0

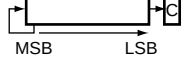
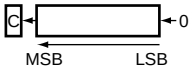
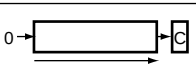
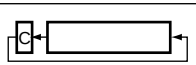
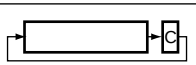
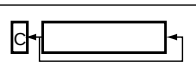
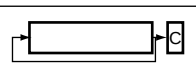
	MOV.L ERs, ERd	L			2							ERs32 → ERd32					
	MOV.L @ERs, ERd	L			4							@ERs → ERd32	—	—	↕	↕	0
	MOV.L @(d:16, ERs), ERd	L				6						@(d:16, ERs) → ERd32	—	—	↕	↕	0
	MOV.L @(d:24, ERs), ERd	L				10						@(d:24, ERs) → ERd32	—	—	↕	↕	0
	MOV.L @ERs+, ERd	L					4					@ERs → ERd32 ERs32+4 → ERs32	—	—	↕	↕	0
	MOV.L @aa:16, ERd	L						6				@aa:16 → ERd32	—	—	↕	↕	0
	MOV.L @aa:24, ERd	L						8				@aa:24 → ERd32	—	—	↕	↕	0
	MOV.L ERs, @ERd	L			4							ERs32 → @ERd	—	—	↕	↕	0
	MOV.L ERs, @(d:16, ERd)	L				6						ERs32 → @(d:16, ERd)	—	—	↕	↕	0
	MOV.L ERs, @(d:24, ERd)	L				10						ERs32 → @(d:24, ERd)	—	—	↕	↕	0
	MOV.L ERs, @–ERd	L					4					ERd32–4 → ERd32 ERs32 → @ERd	—	—	↕	↕	0
	MOV.L ERs, @aa:16	L						6				ERs32 → @aa:16	—	—	↕	↕	0
	MOV.L ERs, @aa:24	L						8				ERs32 → @aa:24	—	—	↕	↕	0
POP	POP.W Rn	W									2	@SP → Rn16 SP+2 → SP	—	—	↕	↕	0
	POP.L ERn	L									4	@SP → ERn32 SP+4 → SP	—	—	↕	↕	0
PUSH	PUSH.W Rn	W									2	SP–2 → SP Rn16 → @SP	—	—	↕	↕	0
	PUSH.L ERn	L									4	SP–4 → SP ERn32 → @SP	—	—	↕	↕	0
MOVFPE	MOVFPE @aa:16, Rd	B						4				Cannot be used in this LSI	Cannot be used in this LSI				
MOVTPE	MOVTPE Rs, @aa:16	B						4				Cannot be used in this LSI	Cannot be used in this LSI				

	ADD.L #xx:32, ERd	L	6									ERd32+#xx:32 → ERd32	—	(2)	↕	↕	↕
	ADD.L ERs, ERd	L		2								ERd32+ERs32 → ERd32	—	(2)	↕	↕	↕
ADDX	ADDX.B #xx:8, Rd	B	2									Rd8+#xx:8 +C → Rd8	—	↕	↕	(3)	↕
	ADDX.B Rs, Rd	B		2								Rd8+Rs8 +C → Rd8	—	↕	↕	(3)	↕
ADDS	ADDS.L #1, ERd	L		2								ERd32+1 → ERd32	—	—	—	—	—
	ADDS.L #2, ERd	L		2								ERd32+2 → ERd32	—	—	—	—	—
	ADDS.L #4, ERd	L		2								ERd32+4 → ERd32	—	—	—	—	—
INC	INC.B Rd	B		2								Rd8+1 → Rd8	—	—	↕	↕	↕
	INC.W #1, Rd	W		2								Rd16+1 → Rd16	—	—	↕	↕	↕
	INC.W #2, Rd	W		2								Rd16+2 → Rd16	—	—	↕	↕	↕
	INC.L #1, ERd	L		2								ERd32+1 → ERd32	—	—	↕	↕	↕
	INC.L #2, ERd	L		2								ERd32+2 → ERd32	—	—	↕	↕	↕
DAA	DAA Rd	B		2								Rd8 decimal adjust → Rd8	—	*	↕	↕	*
SUB	SUB.B Rs, Rd	B		2								Rd8–Rs8 → Rd8	—	↕	↕	↕	↕
	SUB.W #xx:16, Rd	W	4									Rd16–#xx:16 → Rd16	—	(1)	↕	↕	↕
	SUB.W Rs, Rd	W		2								Rd16–Rs16 → Rd16	—	(1)	↕	↕	↕
	SUB.L #xx:32, ERd	L	6									ERd32–#xx:32 → ERd32	—	(2)	↕	↕	↕
	SUB.L ERs, ERd	L		2								ERd32–ERs32 → ERd32	—	(2)	↕	↕	↕
SUBX	SUBX.B #xx:8, Rd	B	2									Rd8–#xx:8–C → Rd8	—	↕	↕	(3)	↕
	SUBX.B Rs, Rd	B		2								Rd8–Rs8–C → Rd8	—	↕	↕	(3)	↕
SUBS	SUBS.L #1, ERd	L		2								ERd32–1 → ERd32	—	—	—	—	—
	SUBS.L #2, ERd	L		2								ERd32–2 → ERd32	—	—	—	—	—
	SUBS.L #4, ERd	L		2								ERd32–4 → ERd32	—	—	—	—	—
DEC	DEC.B Rd	B		2								Rd8–1 → Rd8	—	—	↕	↕	↕
	DEC.W #1, Rd	W		2								Rd16–1 → Rd16	—	—	↕	↕	↕
	DEC.W #2, Rd	W		2								Rd16–2 → Rd16	—	—	↕	↕	↕

	MULXU. W Rs, ERd	W		2								Rd16 × Rs16 → ERd32 (unsigned multiplication)	—	—	—	—	—
MULXS	MULXS. B Rs, Rd	B		4								Rd8 × Rs8 → Rd16 (signed multiplication)	—	—	↕	↕	—
	MULXS. W Rs, ERd	W		4								Rd16 × Rs16 → ERd32 (signed multiplication)	—	—	↕	↕	—
DIVXU	DIVXU. B Rs, Rd	B		2								Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (unsigned division)	—	—	(6)	(7)	—
	DIVXU. W Rs, ERd	W		2								ERd32 ÷ Rs16 → ERd32 (Ed: remainder, Rd: quotient) (unsigned division)	—	—	(6)	(7)	—
DIVXS	DIVXS. B Rs, Rd	B		4								Rd16 ÷ Rs8 → Rd16 (RdH: remainder, RdL: quotient) (signed division)	—	—	(8)	(7)	—
	DIVXS. W Rs, ERd	W		4								ERd32 ÷ Rs16 → ERd32 (Ed: remainder, Rd: quotient) (signed division)	—	—	(8)	(7)	—
CMP	CMP.B #xx:8, Rd	B	2									Rd8–#xx:8	—	↕	↕	↕	↕
	CMP.B Rs, Rd	B		2								Rd8–Rs8	—	↕	↕	↕	↕
	CMP.W #xx:16, Rd	W	4									Rd16–#xx:16	—	(1)	↕	↕	↕
	CMP.W Rs, Rd	W		2								Rd16–Rs16	—	(1)	↕	↕	↕
	CMP.L #xx:32, ERd	L	6									ERd32–#xx:32	—	(2)	↕	↕	↕
	CMP.L ERs, ERd	L		2								ERd32–ERs32	—	(2)	↕	↕	↕

											of ERd32)						
EXTS	EXTS.W Rd	W		2							(<bit 7> of Rd16) → (<bits 15 to 8> of Rd16)	—	—	↕	↕	0	
	EXTS.L ERd	L		2							(<bit 15> of ERd32) → (<bits 31 to 16> of ERd32)	—	—	↕	↕	0	

	AND.L #xx:32, ERd	L	6									ERd32∧#xx:32 → ERd32	—	—	↕	↕	0
	AND.L ERs, ERd	L		4								ERd32∧ERs32 → ERd32	—	—	↕	↕	0
OR	OR.B #xx:8, Rd	B	2									Rd8∨#xx:8 → Rd8	—	—	↕	↕	0
	OR.B Rs, Rd	B		2								Rd8∨Rs8 → Rd8	—	—	↕	↕	0
	OR.W #xx:16, Rd	W	4									Rd16∨#xx:16 → Rd16	—	—	↕	↕	0
	OR.W Rs, Rd	W		2								Rd16∨Rs16 → Rd16	—	—	↕	↕	0
	OR.L #xx:32, ERd	L	6									ERd32∨#xx:32 → ERd32	—	—	↕	↕	0
	OR.L ERs, ERd	L		4								ERd32∨ERs32 → ERd32	—	—	↕	↕	0
XOR	XOR.B #xx:8, Rd	B	2									Rd8⊕#xx:8 → Rd8	—	—	↕	↕	0
	XOR.B Rs, Rd	B		2								Rd8⊕Rs8 → Rd8	—	—	↕	↕	0
	XOR.W #xx:16, Rd	W	4									Rd16⊕#xx:16 → Rd16	—	—	↕	↕	0
	XOR.W Rs, Rd	W		2								Rd16⊕Rs16 → Rd16	—	—	↕	↕	0
	XOR.L #xx:32, ERd	L	6									ERd32⊕#xx:32 → ERd32	—	—	↕	↕	0
	XOR.L ERs, ERd	L		4								ERd32⊕ERs32 → ERd32	—	—	↕	↕	0
NOT	NOT.B Rd	B		2								¬ Rd8 → Rd8	—	—	↕	↕	0
	NOT.W Rd	W		2								¬ Rd16 → Rd16	—	—	↕	↕	0
	NOT.L ERd	L		2								¬ Rd32 → Rd32	—	—	↕	↕	0

SHAR	SHAR.W Rd	W		2									—	—	↕	↕	0
	SHAR.L ERd	L		2									—	—	↕	↕	0
SHLL	SHLL.B Rd	B		2									—	—	↕	↕	0
	SHLL.W Rd	W		2									—	—	↕	↕	0
	SHLL.L ERd	L		2									—	—	↕	↕	0
SHLR	SHLR.B Rd	B		2									—	—	↕	↕	0
	SHLR.W Rd	W		2									—	—	↕	↕	0
	SHLR.L ERd	L		2									—	—	↕	↕	0
ROTXL	ROTXL.B Rd	B		2									—	—	↕	↕	0
	ROTXL.W Rd	W		2									—	—	↕	↕	0
	ROTXL.L ERd	L		2									—	—	↕	↕	0
ROTXR	ROTXR.B Rd	B		2									—	—	↕	↕	0
	ROTXR.W Rd	W		2									—	—	↕	↕	0
	ROTXR.L ERd	L		2									—	—	↕	↕	0
ROTL	ROTL.B Rd	B		2									—	—	↕	↕	0
	ROTL.W Rd	W		2									—	—	↕	↕	0
	ROTL.L ERd	L		2									—	—	↕	↕	0
ROTR	ROTR.B Rd	B		2									—	—	↕	↕	0
	ROTR.W Rd	W		2									—	—	↕	↕	0
	ROTR.L ERd	L		2									—	—	↕	↕	0

	BSET Rn, @ERd	B			4							(Rn8 of @ERd) ← 1	—	—	—	—	—
	BSET Rn, @aa:8	B						4				(Rn8 of @aa:8) ← 1	—	—	—	—	—
BCLR	BCLR #xx:3, Rd	B		2								(#xx:3 of Rd8) ← 0	—	—	—	—	—
	BCLR #xx:3, @ERd	B			4							(#xx:3 of @ERd) ← 0	—	—	—	—	—
	BCLR #xx:3, @aa:8	B						4				(#xx:3 of @aa:8) ← 0	—	—	—	—	—
	BCLR Rn, Rd	B		2								(Rn8 of Rd8) ← 0	—	—	—	—	—
	BCLR Rn, @ERd	B			4							(Rn8 of @ERd) ← 0	—	—	—	—	—
	BCLR Rn, @aa:8	B						4				(Rn8 of @aa:8) ← 0	—	—	—	—	—
BNOT	BNOT #xx:3, Rd	B		2								(#xx:3 of Rd8) ← ¬ (#xx:3 of Rd8)	—	—	—	—	—
	BNOT #xx:3, @ERd	B			4							(#xx:3 of @ERd) ← ¬ (#xx:3 of @ERd)	—	—	—	—	—
	BNOT #xx:3, @aa:8	B						4				(#xx:3 of @aa:8) ← ¬ (#xx:3 of @aa:8)	—	—	—	—	—
	BNOT Rn, Rd	B		2								(Rn8 of Rd8) ← ¬ (Rn8 of Rd8)	—	—	—	—	—
	BNOT Rn, @ERd	B			4							(Rn8 of @ERd) ← ¬ (Rn8 of @ERd)	—	—	—	—	—
	BNOT Rn, @aa:8	B						4				(Rn8 of @aa:8) ← ¬ (Rn8 of @aa:8)	—	—	—	—	—
BTST	BTST #xx:3, Rd	B		2								¬ (#xx:3 of Rd8) → Z	—	—	—	↕	—
	BTST #xx:3, @ERd	B			4							¬ (#xx:3 of @ERd) → Z	—	—	—	↕	—
	BTST #xx:3, @aa:8	B						4				¬ (#xx:3 of @aa:8) → Z	—	—	—	↕	—
	BTST Rn, Rd	B		2								¬ (Rn8 of @Rd8) → Z	—	—	—	↕	—
	BTST Rn, @ERd	B			4							¬ (Rn8 of @ERd) → Z	—	—	—	↕	—
	BTST Rn, @aa:8	B						4				¬ (Rn8 of @aa:8) → Z	—	—	—	↕	—
BLD	BLD #xx:3, Rd	B		2								(#xx:3 of Rd8) → C	—	—	—	—	—

BST	BST #xx:3, Rd	B		2								C → (#xx:3 of Rd8)	—	—	—	—	—
	BST #xx:3, @ERd	B			4							C → (#xx:3 of @ERd24)	—	—	—	—	—
	BST #xx:3, @aa:8	B						4				C → (#xx:3 of @aa:8)	—	—	—	—	—
BIST	BIST #xx:3, Rd	B		2								¬ C → (#xx:3 of Rd8)	—	—	—	—	—
	BIST #xx:3, @ERd	B			4							¬ C → (#xx:3 of @ERd24)	—	—	—	—	—
	BIST #xx:3, @aa:8	B						4				¬ C → (#xx:3 of @aa:8)	—	—	—	—	—
BAND	BAND #xx:3, Rd	B		2								C∧(#xx:3 of Rd8) → C	—	—	—	—	—
	BAND #xx:3, @ERd	B			4							C∧(#xx:3 of @ERd24) → C	—	—	—	—	—
	BAND #xx:3, @aa:8	B						4				C∧(#xx:3 of @aa:8) → C	—	—	—	—	—
BIAND	BIAND #xx:3, Rd	B		2								C∧ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—
	BIAND #xx:3, @ERd	B			4							C∧ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—
	BIAND #xx:3, @aa:8	B						4				C∧ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—
BOR	BOR #xx:3, Rd	B		2								C∨(#xx:3 of Rd8) → C	—	—	—	—	—
	BOR #xx:3, @ERd	B			4							C∨(#xx:3 of @ERd24) → C	—	—	—	—	—
	BOR #xx:3, @aa:8	B						4				C∨(#xx:3 of @aa:8) → C	—	—	—	—	—
BIOR	BIOR #xx:3, Rd	B		2								C∨ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—
	BIOR #xx:3, @ERd	B			4							C∨ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—
	BIOR #xx:3, @aa:8	B						4				C∨ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—
BXOR	BXOR #xx:3, Rd	B		2								C⊕(#xx:3 of Rd8) → C	—	—	—	—	—
	BXOR #xx:3, @ERd	B			4							C⊕(#xx:3 of @ERd24) → C	—	—	—	—	—
	BXOR #xx:3, @aa:8	B						4				C⊕(#xx:3 of @aa:8) → C	—	—	—	—	—
BIXOR	BIXOR #xx:3, Rd	B		2								C⊕ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—
	BIXOR #xx:3, @ERd	B			4							C⊕ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—
	BIXOR #xx:3, @aa:8	B						4				C⊕ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—

	BHI d:8	—							2			C∨ Z = 0	—	—	—	—	—			
	BHI d:16	—							4				—	—	—	—	—			
	BLS d:8	—							2			C∨ Z = 1	—	—	—	—	—			
	BLS d:16	—							4				—	—	—	—	—			
	BCC d:8 (BHS d:8)	—							2			C = 0	—	—	—	—	—			
	BCC d:16 (BHS d:16)	—							4				—	—	—	—	—			
	BCS d:8 (BLO d:8)	—							2			C = 1	—	—	—	—	—			
	BCS d:16 (BLO d:16)	—							4				—	—	—	—	—			
	BNE d:8	—							2			Z = 0	—	—	—	—	—			
	BNE d:16	—							4				—	—	—	—	—			
	BEQ d:8	—							2			Z = 1	—	—	—	—	—			
	BEQ d:16	—							4				—	—	—	—	—			
	BVC d:8	—							2			V = 0	—	—	—	—	—			
	BVC d:16	—							4				—	—	—	—	—			
	BVS d:8	—							2			V = 1	—	—	—	—	—			
	BVS d:16	—							4				—	—	—	—	—			
	BPL d:8	—							2			N = 0	—	—	—	—	—			
	BPL d:16	—							4				—	—	—	—	—			
	BMI d:8	—							2			N = 1	—	—	—	—	—			
	BMI d:16	—							4				—	—	—	—	—			
	BGE d:8	—							2			N⊕V = 0	—	—	—	—	—			
	BGE d:16	—							4				—	—	—	—	—			
	BLT d:8	—							2			N⊕V = 1	—	—	—	—	—			
	BLT d:16	—							4				—	—	—	—	—			
	BGT d:8	—							2			Z∨ (N⊕V) = 0	—	—	—	—	—			
	BGT d:16	—							4				—	—	—	—	—			
	BLE d:8	—							2			Z∨ (N⊕V) = 1	—	—	—	—	—			
	BLE d:16	—							4				—	—	—	—	—			

	BSR d:16	—							4			PC → @–SP PC ← PC+d:16	—	—	—	—	—
JSR	JSR @ERn	—			2							PC → @–SP PC ← ERn	—	—	—	—	—
	JSR @aa:24	—						4				PC → @–SP PC ← aa:24	—	—	—	—	—
	JSR @@aa:8	—								2		PC → @–SP PC ← @aa:8	—	—	—	—	—
RTS	RTS	—									2	PC ← @SP+	—	—	—	—	—

LDC	LDC #xx:8, CCR	B	2								#xx:8 → CCR	↕	↕	↕	↕	↕
	LDC Rs, CCR	B		2							Rs8 → CCR	↕	↕	↕	↕	↕
	LDC @ERs, CCR	W			4						@ERs → CCR	↕	↕	↕	↕	↕
	LDC @(d:16, ERs), CCR	W				6					@(d:16, ERs) → CCR	↕	↕	↕	↕	↕
	LDC @(d:24, ERs), CCR	W				10					@(d:24, ERs) → CCR	↕	↕	↕	↕	↕
	LDC @ERs+, CCR	W					4				@ERs → CCR ERs32+2 → ERs32	↕	↕	↕	↕	↕
	LDC @aa:16, CCR	W						6			@aa:16 → CCR	↕	↕	↕	↕	↕
	LDC @aa:24, CCR	W						8			@aa:24 → CCR	↕	↕	↕	↕	↕
STC	STC CCR, Rd	B		2							CCR → Rd8					
	STC CCR, @ERd	W			4						CCR → @ERd					
	STC CCR, @(d:16, ERd)	W				6					CCR → @(d:16, ERd)					
	STC CCR, @(d:24, ERd)	W				10					CCR → @(d:24, ERd)					
	STC CCR, @–ERd	W					4				ERd32–2 → ERd32 CCR → @ERd					
	STC CCR, @aa:16	W						6			CCR → @aa:16					
	STC CCR, @aa:24	W						8			CCR → @aa:24					
ANDC	ANDC #xx:8, CCR	B	2								CCR∧#xx:8 → CCR	↕	↕	↕	↕	↕
ORC	ORC #xx:8, CCR	B	2								CCR∨#xx:8 → CCR	↕	↕	↕	↕	↕
XORC	XORC #xx:8, CCR	B	2								CCR⊕#xx:8 → CCR	↕	↕	↕	↕	↕
NOP	NOP	—								2	PC ← PC+2					

												R4L–1 → R4L							
												until R4L=0							
												else next							
	EEPMOV. W	—								4		if R4 ≠ 0 then	—	—	—	—	—		
												repeat @R5 → @R6							
												R5+1 → R5							
												R6+1 → R6							
												R4–1 → R4							
												until R4=0							
												else next							

Notes: 1. The number of states in cases where the instruction code and its operands ar
in on-chip memory is shown here. For other cases, see Appendix A.3, Numbe
Execution States.

2. n is the value set in register R4L or R4.

(1) Set to 1 when a carry or borrow occurs at bit 11; otherwise cleared to 0.

(2) Set to 1 when a carry or borrow occurs at bit 27; otherwise cleared to 0.

(3) Retains its previous value when the result is zero; otherwise cleared to 0.

(4) Set to 1 when the adjustment produces a carry; otherwise retains its previous

(5) The number of states required for execution of an instruction that transfers da
synchronization with the E clock is variable.

(6) Set to 1 when the divisor is negative; otherwise cleared to 0.

(7) Set to 1 when the divisor is zero; otherwise cleared to 0.

(8) Set to 1 when the quotient is negative; otherwise cleared to 0.

Instruction code:

1st byte		2nd byte	
AH	AL	BH	BL

Instruction when most significant bit of BH i

Instruction when most significant bit of BH i

AH \ AL	0	1	2	3	4	5	6	7	8	9	A	B	C
0	NOP	Table A-2 (2)	STC	LDC	ORC	XORC	ANDC	LDC	ADD		Table A-2 (2)	Table A-2 (2)	
1	Table A-2 (2)	Table A-2 (2)	Table A-2 (2)	Table A-2 (2)	OR.B	XOR.B	AND.B	Table A-2 (2)	SUB		Table A-2 (2)	Table A-2 (2)	
2	MOV.B												
3													
4	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI	BGI
5	MULXU	DIVXU	MULXU	DIVXU	RTS	BSR	RTE		Table A-2 (2)	JMP			BSI
6	BSET	BNOT	BCLR	BTST	OR	XOR	AND	BST / BIST	MOV				
7					BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD	MOV	Table A-2 (2)	Table A-2 (2)	EEPMOV	
8	ADD												
9	ADDX												
A	CMP												
B	SUBX												
C	OR												
D	XOR												
E	AND												
F													

Instruction code:

1st byte		2nd byte	
AH	AL	BH	BL

AH AL \ BH	0	1	2	3	4	5	6	7	8	9	A	B
01	MOV				LDC/STC				SLEEP			
0A	INC								AD			
0B	ADDS					INC		INC	ADDS			
0F	DAA								MC			
10	SHLL			SHLL					SHAL			SHAL
11	SHLR			SHLR					SHAR			SHAR
12	ROTXL			ROTXL					ROTL			ROTL
13	ROTXR			ROTXR					ROTR			ROTR
17	NOT			NOT		EXTU		EXTU	NEG			NEG
1A	DEC								SU			
1B	SUBS					DEC		DEC	SUB			
1F	DAS								CM			
58	BRA	BRN	BHI	BLS	BCC	BCS	BNE	BEQ	BVC	BVS	BPL	BMI
79	MOV	ADD	CMP	SUB	OR	XOR	AND					

Instruction code:

1st byte		2nd byte		3rd byte		4th byte	
AH	AL	BH	BL	CH	CL	DH	DL

Instruction when mo
Instruction when mo

AH / ALBH / BLCH \ CL	0	1	2	3	4	5	6	7	8	9	A	B
01406										LDC / STC		LDC / STC
01C05	MULXS		MULXS									
01D05		DIVXS		DIVXS								
01F06					OR	XOR	AND					
7Cr06 *1				BTST								
7Cr07 *1				BTST	BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD				
7Dr06 *1	BSET	BNOT	BCLR					BST / BIST				
7Dr07 *1	BSET	BNOT	BCLR									
7Eaa6 *2				BTST								
7Eaa7 *2				BTST	BOR / BIOR	BXOR / BIXOR	BAND / BIAND	BLD / BILD				
7Faa6 *2	BSET	BNOT	BCLR					BST / BIST				
7Faa7 *2	BSET	BNOT	BCLR									

Notes: 1. r is the register designation field.
2. aa is the absolute address field.

BSET #0, @FF00

From table A.4:

I = L = 2, J = K = M = N= 0

From table A.3:

$S_I = 2$, $S_L = 2$

Number of states required for execution = $2 \times 2 + 2 \times 2 = 8$

When instruction is fetched from on-chip ROM, branch address is read from on-chip RO
on-chip RAM is used for stack area.

JSR @@ 30

From table A.4:

I = 2, J = K = 1, L = M = N = 0

From table A.3:

$S_I = S_J = S_K = 2$

Number of states required for execution = $2 \times 2 + 1 \times 2 + 1 \times 2 = 8$

Note: * Depends on which on-chip peripheral module is accessed. See section 23.1, F
Addresses (Address Order).

ADDS	ADDS #1/2/4, ERd	1		
ADDX	ADDX #xx:8, Rd	1		
	ADDX Rs, Rd	1		
AND	AND.B #xx:8, Rd	1		
	AND.B Rs, Rd	1		
	AND.W #xx:16, Rd	2		
	AND.W Rs, Rd	1		
	AND.L #xx:32, ERd	3		
	AND.L ERs, ERd	2		
ANDC	ANDC #xx:8, CCR	1		
BAND	BAND #xx:3, Rd	1		
	BAND #xx:3, @ERd	2		1
	BAND #xx:3, @aa:8	2		1
Bcc	BRA d:8 (BT d:8)	2		
	BRN d:8 (BF d:8)	2		
	BHI d:8	2		
	BLS d:8	2		
	BCC d:8 (BHS d:8)	2		
	BCS d:8 (BLO d:8)	2		
	BNE d:8	2		
	BEQ d:8	2		
	BVC d:8	2		
	BVS d:8	2		
	BPL d:8	2		
	BMI d:8	2		
	BGE d:8	2		

	BCS d:16(BLO d:16)	2		1
	BNE d:16	2		1
	BEQ d:16	2		1
	BVC d:16	2		1
	BVS d:16	2		1
	BPL d:16	2		1
	BMI d:16	2		1
	BGE d:16	2		1
	BLT d:16	2		1
	BGT d:16	2		1
	BLE d:16	2		1
BCLR	BCLR #xx:3, Rd	1		
	BCLR #xx:3, @ERd	2	2	
	BCLR #xx:3, @aa:8	2	2	
	BCLR Rn, Rd	1		
	BCLR Rn, @ERd	2	2	
	BCLR Rn, @aa:8	2	2	
BIAND	BIAND #xx:3, Rd	1		
	BIAND #xx:3, @ERd	2	1	
	BIAND #xx:3, @aa:8	2	1	
BILD	BILD #xx:3, Rd	1		
	BILD #xx:3, @ERd	2	1	
	BILD #xx:3, @aa:8	2	1	

	BIXOR #xx:3, @aa:8	2		1
BLD	BLD #xx:3, Rd	1		
	BLD #xx:3, @ERd	2		1
	BLD #xx:3, @aa:8	2		1
BNOT	BNOT #xx:3, Rd	1		
	BNOT #xx:3, @ERd	2		2
	BNOT #xx:3, @aa:8	2		2
	BNOT Rn, Rd	1		
	BNOT Rn, @ERd	2		2
	BNOT Rn, @aa:8	2		2
BOR	BOR #xx:3, Rd	1		
	BOR #xx:3, @ERd	2		1
	BOR #xx:3, @aa:8	2		1
BSET	BSET #xx:3, Rd	1		
	BSET #xx:3, @ERd	2		2
	BSET #xx:3, @aa:8	2		2
	BSET Rn, Rd	1		
	BSET Rn, @ERd	2		2
	BSET Rn, @aa:8	2		2
BSR	BSR d:8	2	1	
	BSR d:16	2	1	
BST	BST #xx:3, Rd	1		
	BST #xx:3, @ERd	2		2
	BST #xx:3, @aa:8	2		2

	BXOR #xx:3, @aa:8	2		1	
CMP	CMP.B #xx:8, Rd	1			
	CMP.B Rs, Rd	1			
	CMP.W #xx:16, Rd	2			
	CMP.W Rs, Rd	1			
	CMP.L #xx:32, ERd	3			
	CMP.L ERs, ERd	1			
DAA	DAA Rd	1			
DAS	DAS Rd	1			
DEC	DEC.B Rd	1			
	DEC.W #1/2, Rd	1			
	DEC.L #1/2, ERd	1			
DUVXS	DIVXS.B Rs, Rd	2			
	DIVXS.W Rs, ERd	2			
DIVXU	DIVXU.B Rs, Rd	1			
	DIVXU.W Rs, ERd	1			
EEPMOV	EEPMOV.B	2		2n+2*[1]	
	EEPMOV.W	2		2n+2*[1]	
EXTS	EXTS.W Rd	1			
	EXTS.L ERd	1			
EXTU	EXTU.W Rd	1			
	EXTU.L ERd	1			

	JSR @@aa:8	2	1	1		
LDC	LDC #xx:8, CCR	1				
	LDC Rs, CCR	1				
	LDC@ERs, CCR	2				1
	LDC@(d:16, ERs), CCR	3				1
	LDC@(d:24,ERs), CCR	5				1
	LDC@ERs+, CCR	2				1
	LDC@aa:16, CCR	3				1
	LDC@aa:24, CCR	4				1
MOV	MOV.B #xx:8, Rd	1				
	MOV.B Rs, Rd	1				
	MOV.B @ERs, Rd	1			1	
	MOV.B @(d:16, ERs), Rd	2			1	
	MOV.B @(d:24, ERs), Rd	4			1	
	MOV.B @ERs+, Rd	1			1	
	MOV.B @aa:8, Rd	1			1	
	MOV.B @aa:16, Rd	2			1	
	MOV.B @aa:24, Rd	3			1	
	MOV.B Rs, @Erd	1			1	
	MOV.B Rs, @(d:16, ERd)	2			1	
	MOV.B Rs, @(d:24, ERd)	4			1	
	MOV.B Rs, @-ERd	1			1	
	MOV.B Rs, @aa:8	1			1	

	MOV.W @aa:16, Rd	2		1	
	MOV.W @aa:24, Rd	3		1	
	MOV.W Rs, @ERd	1		1	
	MOV.W Rs, @(d:16,ERd)	2		1	
	MOV.W Rs, @(d:24,ERd)	4		1	
MOV	MOV.W Rs, @-ERd	1		1	
	MOV.W Rs, @aa:16	2		1	
	MOV.W Rs, @aa:24	3		1	
	MOV.L #xx:32, ERd	3			
	MOV.L ERs, ERd	1			
	MOV.L @ERs, ERd	2		2	
	MOV.L @(d:16,ERs), ERd	3		2	
	MOV.L @(d:24,ERs), ERd	5		2	
	MOV.L @ERs+, ERd	2		2	
	MOV.L @aa:16, ERd	3		2	
	MOV.L @aa:24, ERd	4		2	
	MOV.L ERs,@ERd	2		2	
	MOV.L ERs, @(d:16,ERd)	3		2	
	MOV.L ERs, @(d:24,ERd)	5		2	
	MOV.L ERs, @-ERd	2		2	
	MOV.L ERs, @aa:16	3		2	
	MOV.L ERs, @aa:24	4		2	
MOVFPE	MOVFPE @aa:16, Rd*[2]	2	1		
MOVTPE	MOVTPE Rs,@aa:16*[2]	2	1		

NOT	NOT.B Rd	1		
	NOT.W Rd	1		
	NOT.L ERd	1		
OR	OR.B #xx:8, Rd	1		
	OR.B Rs, Rd	1		
	OR.W #xx:16, Rd	2		
	OR.W Rs, Rd	1		
	OR.L #xx:32, ERd	3		
	OR.L ERs, ERd	2		
ORC	ORC #xx:8, CCR	1		
POP	POP.W Rn	1		1
	POP.L ERn	2		2
PUSH	PUSH.W Rn	1		1
	PUSH.L ERn	2		2
ROTL	ROTL.B Rd	1		
	ROTL.W Rd	1		
	ROTL.L ERd	1		
ROTR	ROTR.B Rd	1		
	ROTR.W Rd	1		
	ROTR.L ERd	1		
ROTXL	ROTXL.B Rd	1		
	ROTXL.W Rd	1		
	ROTXL.L ERd	1		

SHAR	SHAR.B Rd	1			
	SHAR.W Rd	1			
	SHAR.L ERd	1			
SHLL	SHLL.B Rd	1			
	SHLL.W Rd	1			
	SHLL.L ERd	1			
SHLR	SHLR.B Rd	1			
	SHLR.W Rd	1			
	SHLR.L ERd	1			
SLEEP	SLEEP	1			
STC	STC CCR, Rd	1			
	STC CCR, @ERd	2		1	
	STC CCR, @(d:16,ERd)	3		1	
	STC CCR, @(d:24,ERd)	5		1	
	STC CCR,@-ERd	2		1	
	STC CCR, @aa:16	3		1	
	STC CCR, @aa:24	4		1	
SUB	SUB.B Rs, Rd	1			
	SUB.W #xx:16, Rd	2			
	SUB.W Rs, Rd	1			
	SUB.L #xx:32, ERd	3			
	SUB.L ERs, ERd	1			
SUBS	SUBS #1/2/4, ERd	1			

XORC	XORC #xx:8, CCR	1

Notes: 1. n: Specified value in R4L. The source and destination operands are accessed
times respectively.
2. It can not be used in this LSI.

transfer instructions	POP, PUSH	—	—	—	—	—	—	—	—	—	—	—	
	MOVFPE, MOVTPE	—	—	—	—	—	—	—	—	—	—	—	
Arithmetic operations	ADD, CMP	BWL	BWL	—	—	—	—	—	—	—	—	—	
	SUB	WL	BWL	—	—	—	—	—	—	—	—	—	
	ADDX, SUBX	B	B	—	—	—	—	—	—	—	—	—	
	ADDS, SUBS	—	L	—	—	—	—	—	—	—	—	—	
	INC, DEC	—	BWL	—	—	—	—	—	—	—	—	—	
	DAA, DAS	—	B	—	—	—	—	—	—	—	—	—	
	MULXU, MULXS, DIVXU, DIVXS	—	BW	—	—	—	—	—	—	—	—	—	
	NEG	—	BWL	—	—	—	—	—	—	—	—	—	
	EXTU, EXTS	—	WL	—	—	—	—	—	—	—	—	—	
Logical operations	AND, OR, XOR	—	BWL	—	—	—	—	—	—	—	—	—	
	NOT	—	BWL	—	—	—	—	—	—	—	—	—	
Shift operations		—	BWL	—	—	—	—	—	—	—	—	—	
Bit manipulations		—	B	B	—	—	—	B	—	—	—	—	
Branching instructions	BCC, BSR	—	—	—	—	—	—	—	—	—	—	—	
	JMP, JSR	—	—	◯	—	—	—	—	—	—	◯	◯	
	RTS	—	—	—	—	—	—	—	—	◯	—	—	◯
System control instructions	RTE	—	—	—	—	—	—	—	—	—	—	—	
	SLEEP	—	—	—	—	—	—	—	—	—	—	—	
	LDC	B	B	W	W	W	W	—	W	W	—	—	
	STC	—	B	W	W	W	W	—	W	W	—	—	
	ANDC, ORC, XORC	B	—	—	—	—	—	—	—	—	—	—	
	NOP	—	—	—	—	—	—	—	—	—	—	—	
Block data transfer instructions		—	—	—	—	—	—	—	—	—	—	—	

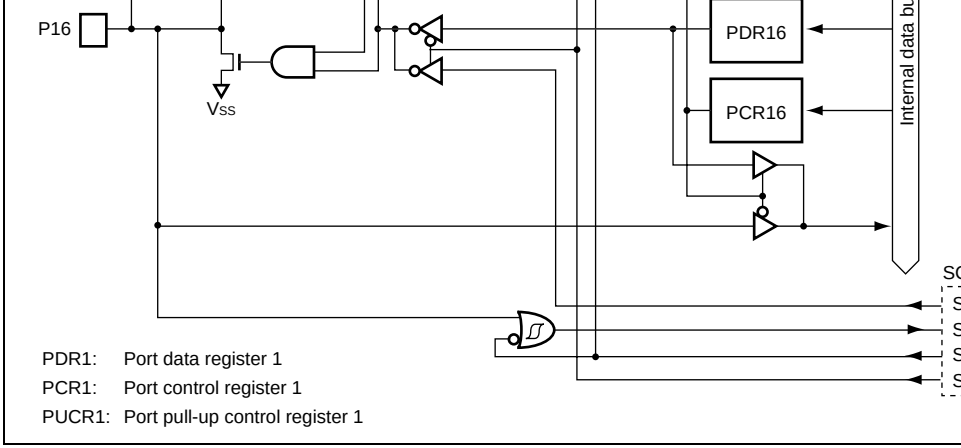


Figure B.1 (a) Port 1 Block Diagram (P16) (F-ZTAT Version)

PDR1: Port data register 1
PCR1: Port control register 1
PUCR1: Port pull-up control register 1

Figure B.1 (b) Port 1 Block Diagram (P16) (Masked ROM Version)

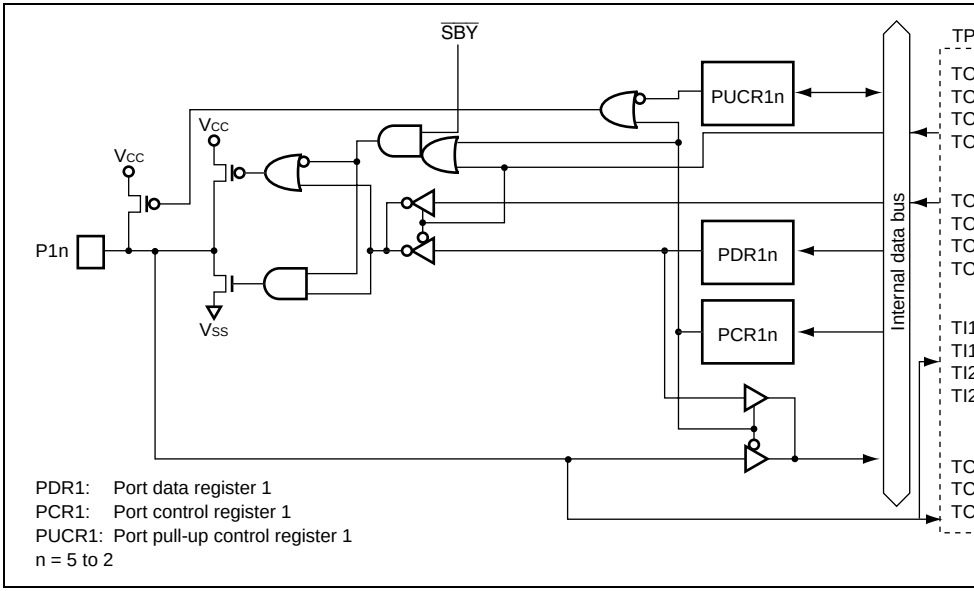
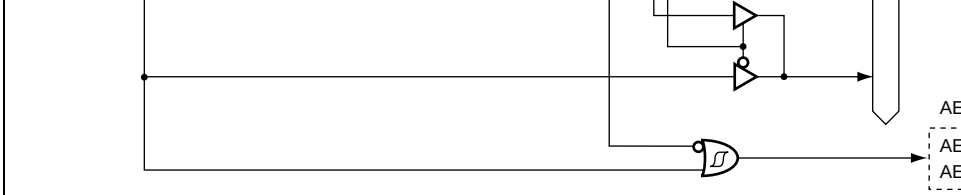
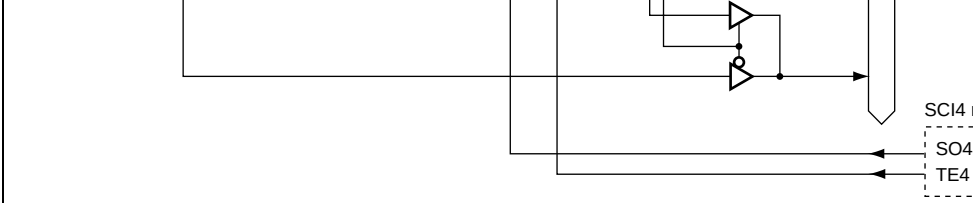


Figure B.1 (c) Port 1 Block Diagram (P15 to P12)



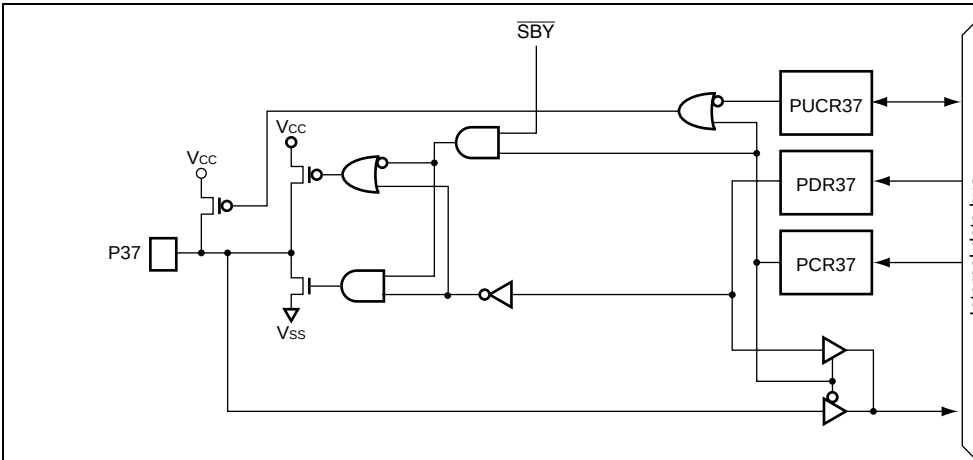
PDR1: Port data register 1
PCR1: Port control register 1
PMR1: Port mode register 1
PUCR1: Port pull-up control register 1
n = 1, 0

Figure B.1 (d) Port 1 Block Diagram (P11, P10)



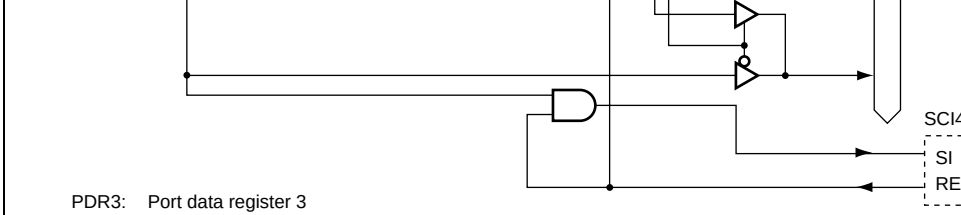
PDR3: Port data register 3
PCR3: Port control register 3
PUCR3: Port pull-up control register 3

Figure B.2 (a) Port 3 Block Diagram (P37) (F-ZTAT Version)



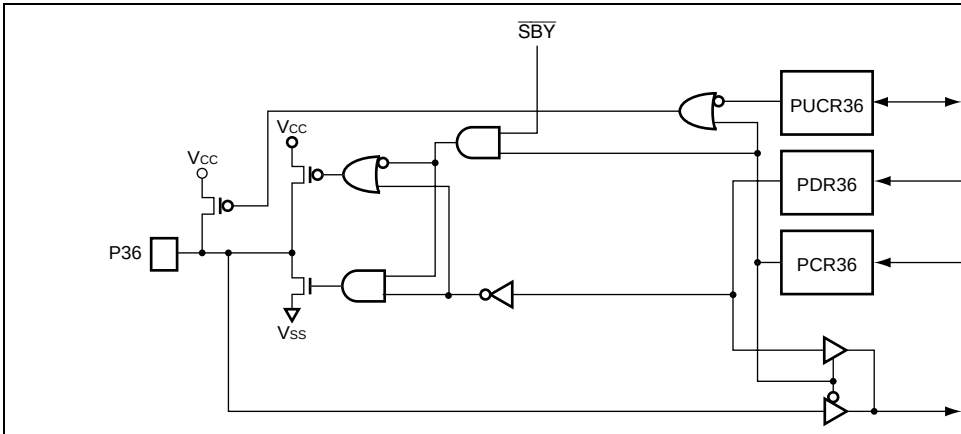
PDR3: Port data register 3
PCR3: Port control register 3
PUCR3: Port pull-up control register 3

Figure B.2 (b) Port 3 Block Diagram (P37) (Masked ROM Version)



PDR3: Port data register 3
PCR3: Port control register 3
PUCR3: Port pull-up control register 3

Figure B.2 (c) Port 3 Block Diagram (P36) (F-ZTAT Version)



PDR3: Port data register 3
PCR3: Port control register 3
PUCR3: Port pull-up control register 3

Figure B.2 (d) Port 3 Block Diagram (P36) (Masked ROM Version)

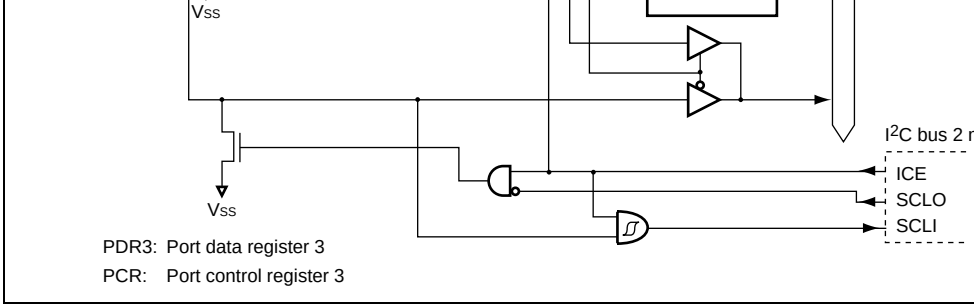


Figure B.2 (e) Port 3 Block Diagram (P32)

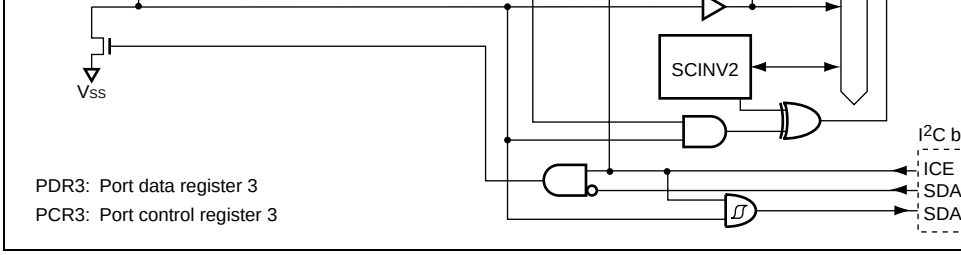
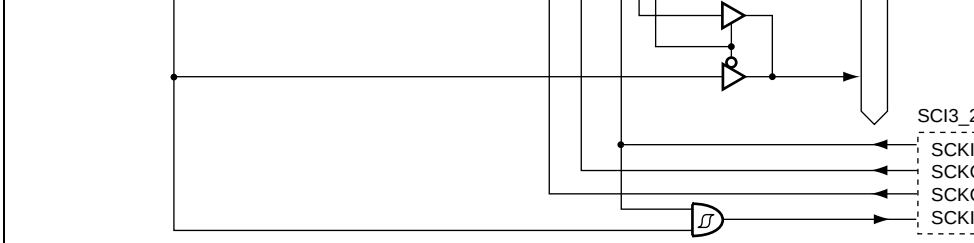
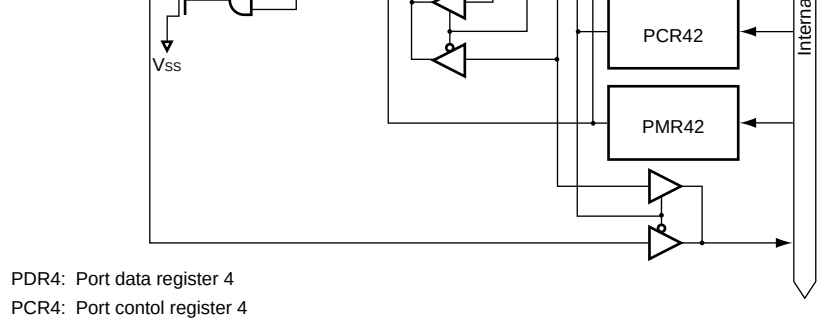


Figure B.2 (f) Port 3 Block Diagram (P31)



PDR3: Port data register 3
PCR3: Port control register 3
PMR3: Port mode register 3
PUCR3: Port pull-up control register 3

Figure B.2 (g) Port 3 Block Diagram (P30)



PDR4: Port data register 4
PCR4: Port contol register 4
PMR4: Port mode register 4

Figure B.3 (a) Port 4 Block Diagram (P42)

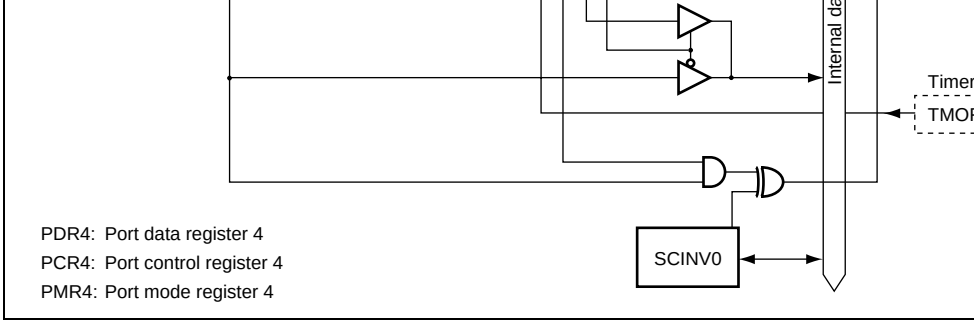
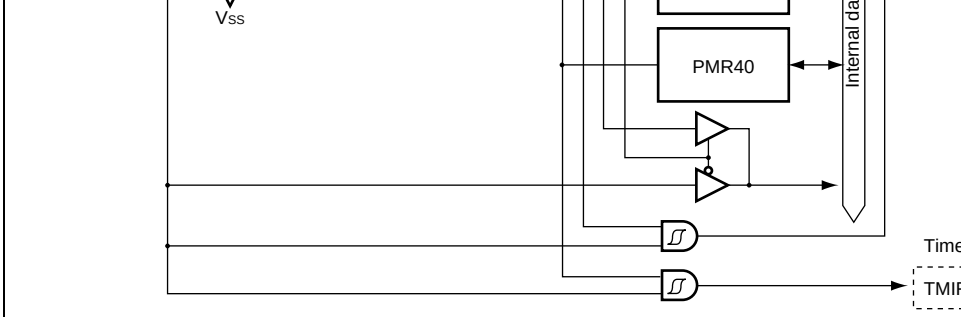
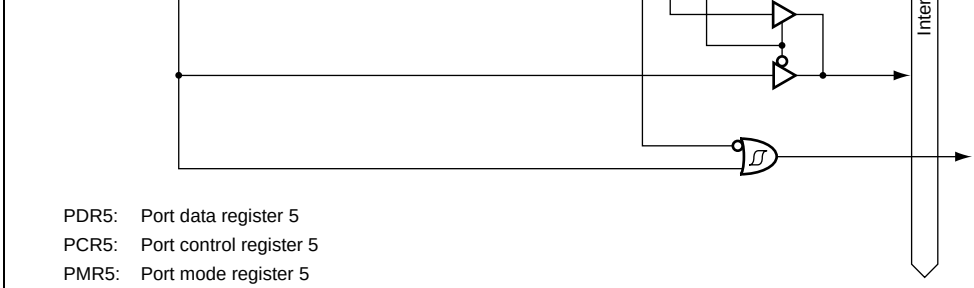


Figure B.3 (b) Port 4 Block Diagram (P41)



PDR4: Port data register 4
PCR4: Port control register 4
PMR4: Port mode register 4

Figure B.3 (c) Port 4 Block Diagram (P40)

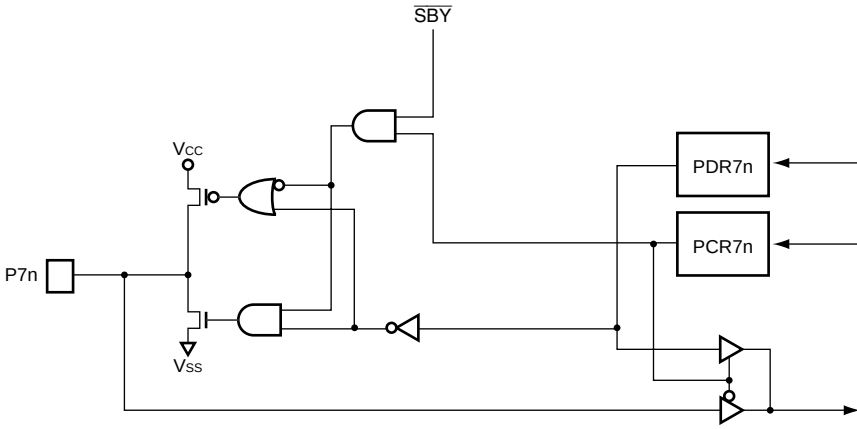


PDR5: Port data register 5
PCR5: Port control register 5
PMR5: Port mode register 5
PUCR5: Port pull-up control register 5
n = 7 to 0

Figure B.4 Port 5 Block Diagram

PDR6: Port data register 6
PCR6: Port control register 6
PUCR6: Port pull-up control register 6
n = 7 to 0

Figure B.5 Port 6 Block Diagram

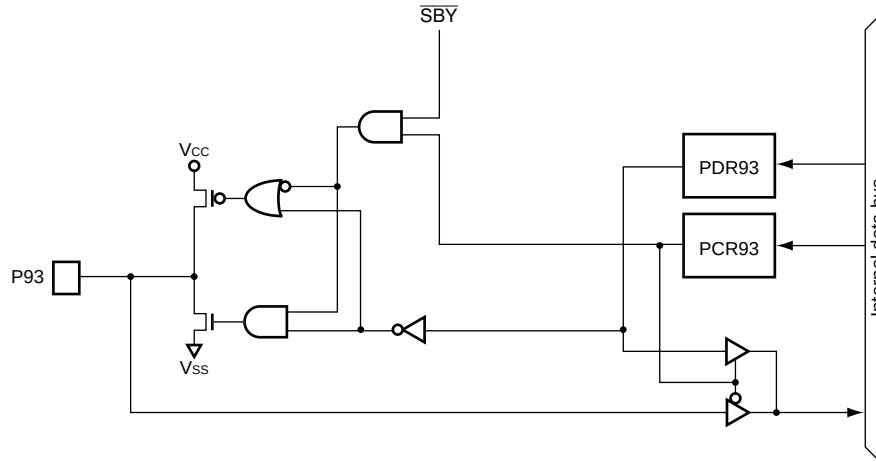


PDR7: Port data register 7
PCR7: Port control register 7
n = 7 to 0

Figure B.6 Port 7 Block Diagram

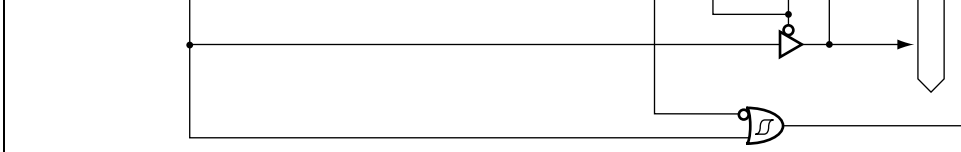
PDR8: Port data register 8
PCR8: Port control register 8
n = 7 to 0

Figure B.7 Port 8 Block Diagram



PDR9: Port data register 9
PCR9: Port control register 9

Figure B.8 (a) Port 9 Block Diagram (P93)

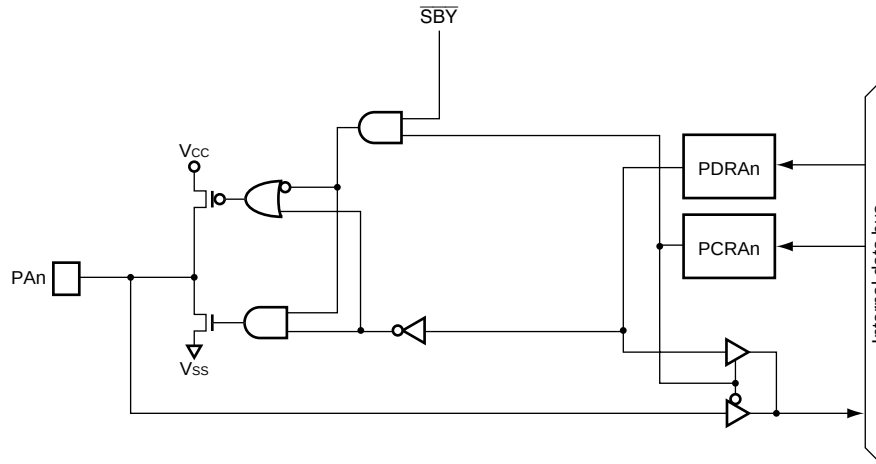


PDR9: Port data register 9
PCR9: Port control register 9
PMR9: Port mode register 9

Figure B.8 (b) Port 9 Block Diagram (P92)

PDR9: Port data register 9
PCR9: Port control register 9
PMR9: Port mode register 9
n = 1, 0

Figure B.8 (c) Port 9 Block Diagram (P91, P90)



PDRA: Port data register A
PCRA: Port control register A
n = 3 to 0

Figure B.9 Port A Block Diagram

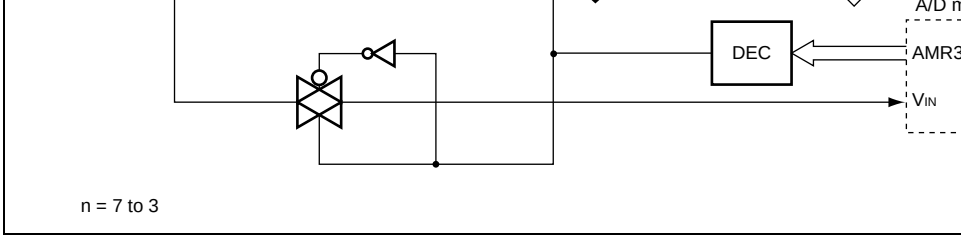


Figure B.10 (a) Port B Block Diagram (PB7 to PB3)

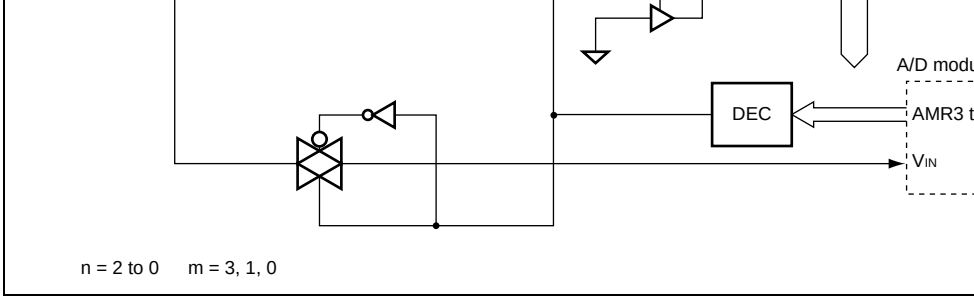


Figure B.10 (b) Port B Block Diagram (PB2 to PB0)

P57 to P50	High impedance	Retained	Retained	High impedance*	Functioning	Functioning
P67 to P60	High impedance	Retained	Retained	High impedance*	Functioning	Functioning
P77 to P70	High impedance	Retained	Retained	High impedance*	Functioning	Functioning
P87 to P80	High impedance	Retained	Retained	High impedance*	Functioning	Functioning
P93 to P90	High impedance	Retained	Retained	High impedance*	Functioning	Functioning
PA3 to PA0	High impedance	Retained	Retained	High impedance*	Functioning	Functioning
PB7 to PB5, PB4, PB3, PB2 to PB0	High impedance	High impedance	High impedance	High impedance*	High impedance	High impedance

Notes: * Registers are retained and output level is high impedance.

		HD64F38076RLP10V	F38076RLP10V	
		HCD64F38076RC4	—	Chip
		HCD64F38076RC10	—	Chip
	Wide-range specifications	HD64F38076RH10W	F38076H10	80 pin QFP
		HD64F38076RW10W	F38076W10	80 pin TQF
		HD64F38076RLP10WV	F38076RLP10WV	80 pin P-TF (TLP-85V)
Masked ROM version	Regular specifications	HD64338076RH	38076(***)H	80 pin QFP
		HD64338076RW	38076(***)W	80 pin TQF
		HD64338076RLPV	38076R(***)LPV	80 pin P-TF (TLP-85V)
		HCD64338076R	—	Chip
	Wide-range specifications	HD64338076RHW	38076(***)H	80 pin QFP
		HD64338076RWW	38076(***)W	80 pin TQF
		HD64338076RLPWV	38076R(***)LPWV	80 pin P-TF (TLP-85V)

					(TLP-85V
H8/38074R	Masked ROM version	Regular specifications	HD64338074RH	38074(***)H	80 pin QF
			HD64338074RW	38074(***)W	80 pin TQ
			HD64338074RLPV	38074R(***)LPV	80 pin P-T
					(TLP-85V
			HCD64338074R	—	Chip
		Wide-range specifications	HD64338074RHW	38074(***)H	80 pin QF
			HD64338074RWW	38074(***)W	80 pin TQ
			HD64338074RLPWV	38074R(***)LPWV	80 pin P-T
					(TLP-85V
H8/38073R	Masked ROM version	Regular specifications	HD64338073RH	38073(***)H	80 pin QF
			HD64338073RW	38073(***)W	80 pin TQ
			HD64338073RLPV	38073R(***)LPV	80 pin P-T
					(TLP-85V
			HCD64338073R	—	Chip
		Wide-range specifications	HD64338073RHW	38073(***)H	80 pin QF
			HD64338073RWW	38073(***)W	80 pin TQ
			HD64338073RLPWV	38073R(***)LPWV	80 pin P-T
					(TLP-85V

[Legend]
(***): ROM code

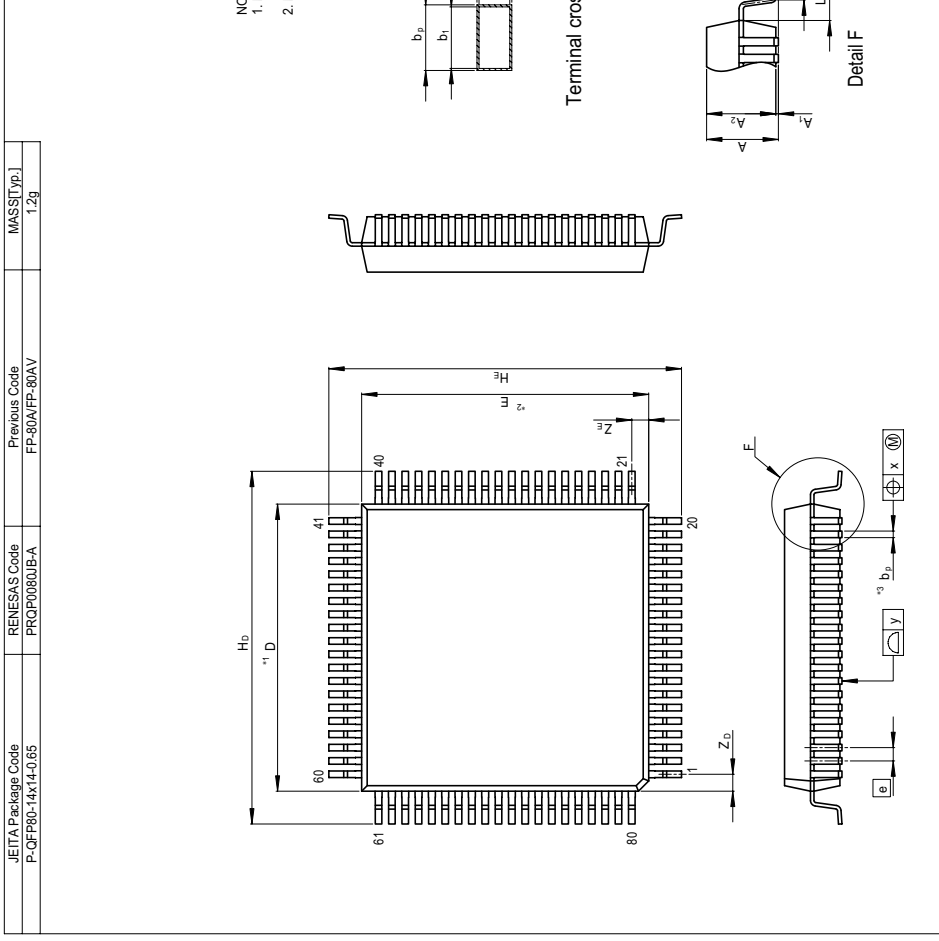


Figure D.1 Package Dimensions (FP-80A)

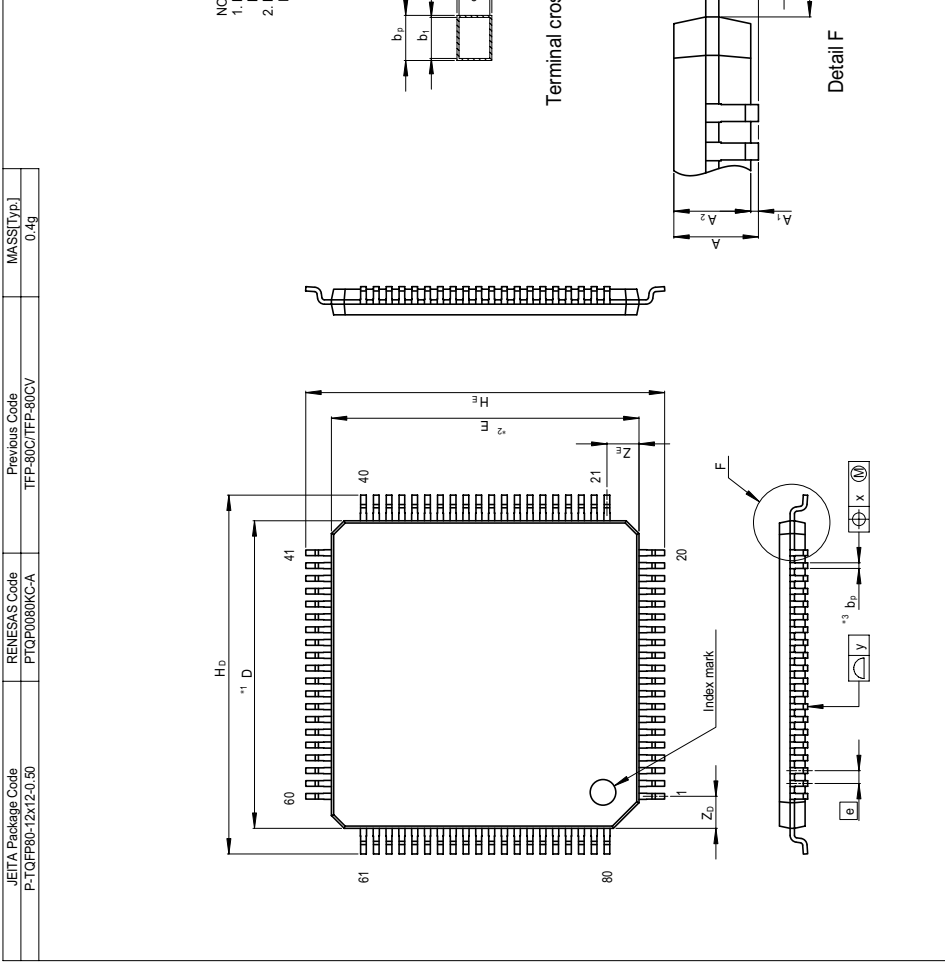
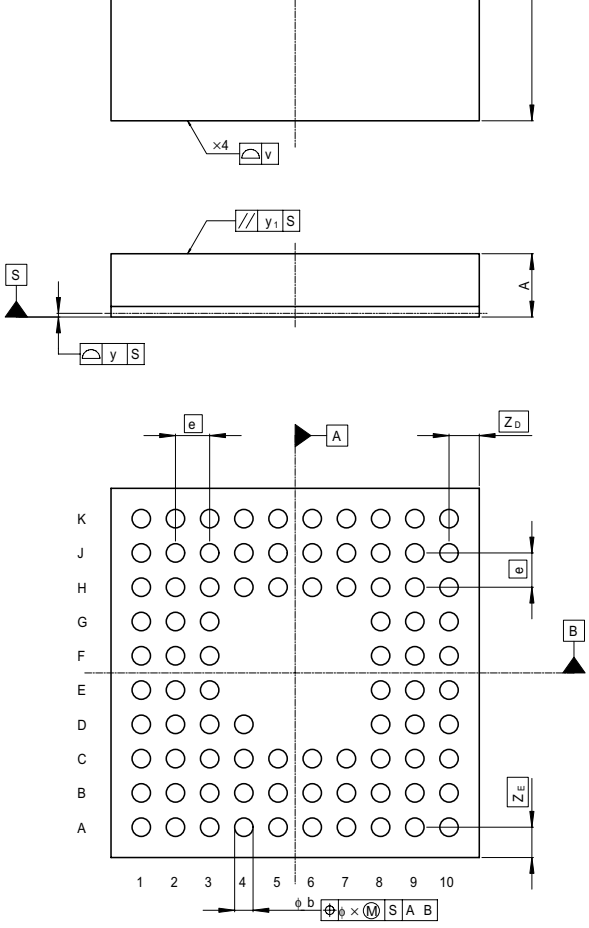
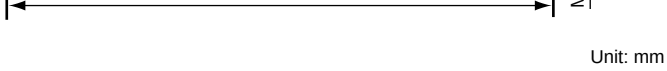


Figure D.2 Package Dimensions (TFP-80C)



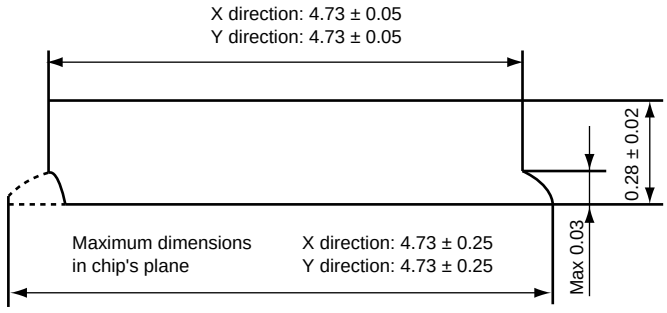
Reference Symbol	Dimension in Millimeters	
	Min	Nom
D	—	7.0
E	—	7.0
v	—	—
w	—	—
A	—	—
A_1	—	—
e	—	0.65
b	0.30	0.35
x	—	—
y	—	—
y_1	—	—
S_D	—	—
S_E	—	—
Z_D	—	0.575
Z_E	—	0.575

Figure D.3 Package Dimensions (TLP-85V)



Unit: mm

Figure E.1 Cross-Sectional View of Chip (HCD64338076R, HCD64338075R, HCD64338074R, and HCD64338073R)



Unit: mm

Figure E.2 Cross-Sectional View of Chip (HCD64F38076R)

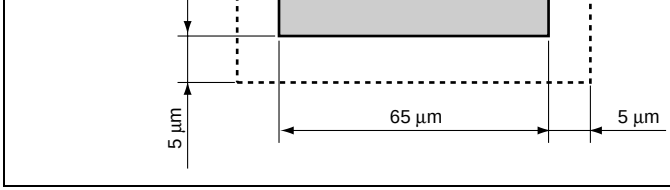


Figure F.1 Bonding Pad Form
(HCD64F38076R, HCD64338076R, HCD64338075R, HCD64338074R, and HCD64

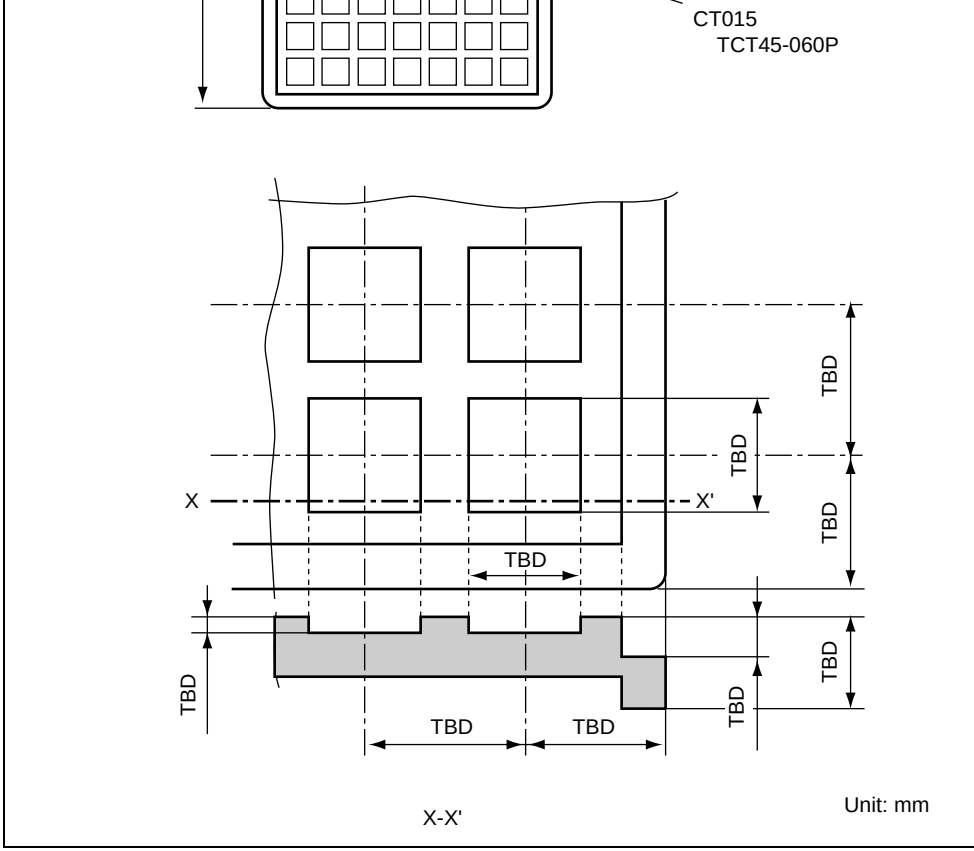


Figure G.1 Chip Tray Specifications
(HCD64338076R, HCD64338075R, HCD64338074R, and HCD64338073R)

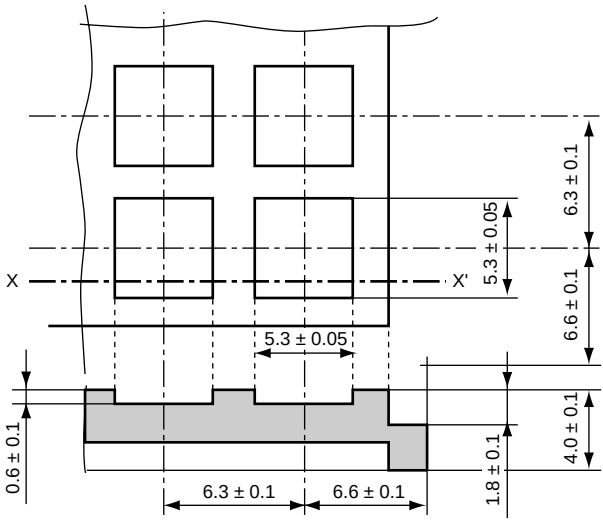


Figure G.2 Chip Tray Specifications (HCD64F38076R)

B

C

F

G

H

I

S

V

W

Renesas 16-Bit Single-Chip Microcomputer
Hardware Manual
H8/38076R Group

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