3.3V/2.5V 1:11 LVCMOS Zero Delay Clock Generator

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DATASHEET

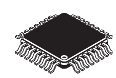
The MPC9352 is a 3.3 V or 2.5 V compatible, 1:11 PLL based clock generator targeted for high performance clock tree applications. With output frequencies up to 200 MHz and output skews lower than 200 ps, the device meets the needs of most demanding clock applications.

Features

- Configurable 11 Outputs LVCMOS PLL Clock Generator
- Fully Integrated PLL
- Wide Range of Output Clock Frequency of 16.67 MHz to 200 MHz
- Multiplication of the Input Reference Clock Frequency by 3, 2, 1, 3 ÷ 2, 2 ÷ 3, 1 ÷ 3 and 1 ÷ 2
- 2.5 V and 3.3 V LVCMOS Compatible
- Maximum Output Skew of 200 ps
- Supports Zero-Delay Applications
- Designed for High-Performance Telecom, Networking and Computing Applications
- 32-Lead LQFP Package, Pb-Free
- Ambient Temperature Range –40°C to +85°C
- For functional replacement use 8T49N285

MPC9352

LOW VOLTAGE
3.3 V/2.5 V LVCMOS 1:11
CLOCK GENERATOR



AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03

The MPC9352 is a fully 3.3 V or 2.5 V compatible PLL clock generator and clock driver. The device has the capability to generate output clock signals of 16.67 to 200 MHz from external clock sources. The internal PLL is optimized for its frequency range and does not require external lock filter components. One output of the MPC9352 has to be connected to the PLL feedback input FB_IN to close the external PLL feedback path. The output divider of this output setting determines the PLL frequency multiplication factor. This multiplication factor, F_RANGE, and the reference clock frequency must be selected to situate the VCO in its specified lock range. The frequency of the clock outputs can be configured individually for all three output banks by the FSELx pins supporting systems with different, but phase-aligned, clock frequencies.

The PLL of the MPC9352 minimizes the propagation delay, and therefore, supports zero-delay applications. All inputs and outputs are LVCMOS compatible. The outputs are optimized to drive parallel terminated 50Ω transmission lines. Alternatively, each output can drive up to two series terminated transmission lines giving the device an effective fanout of 22.

The device also supports output high-impedance disable and a PLL bypass mode for static system test and diagnosis. The MPC9352 is packaged in a 32 ld LQFP.

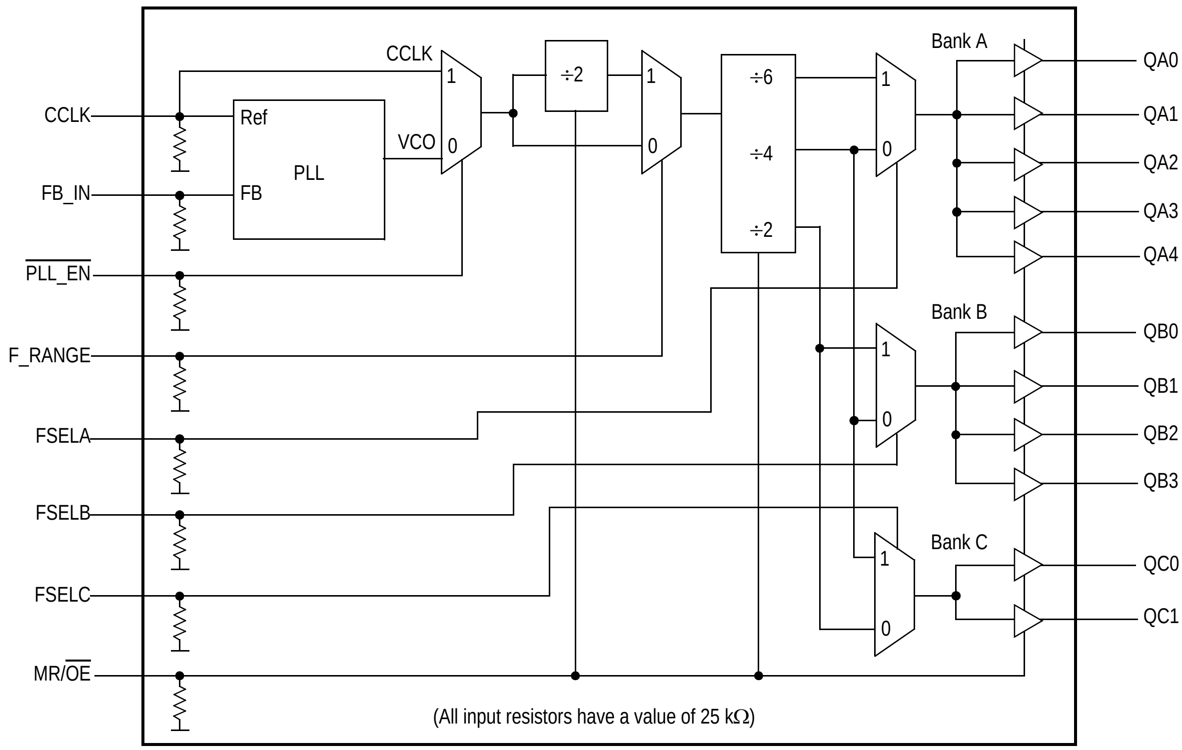
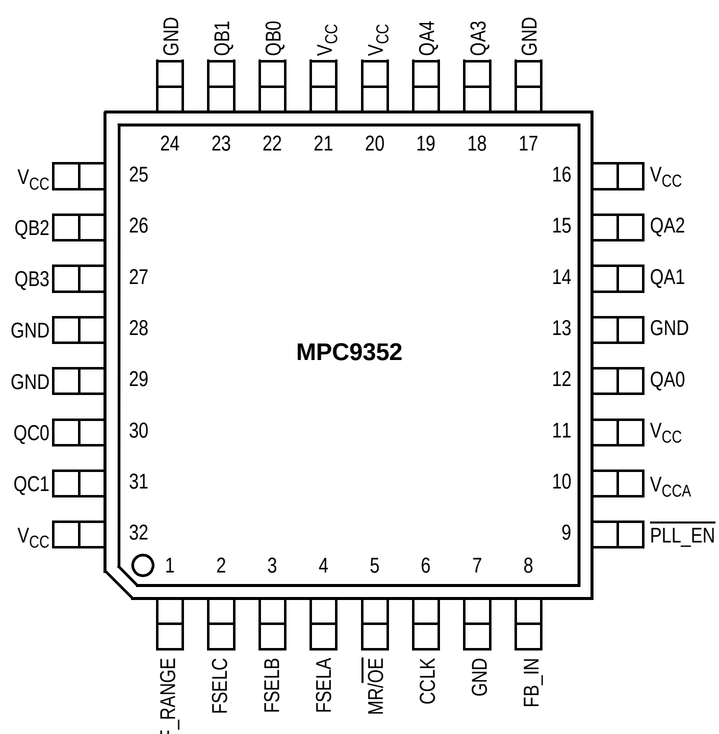


Figure 1. MPC9352 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin V_{CCA}. Please see Applications Information section for details.

Figure 2. MPC9352 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an output
F_RANGE	Input	LVCMOS	PLL frequency range select
FSELA	Input	LVCMOS	Frequency divider select for bank A outputs
FSELB	Input	LVCMOS	Frequency divider select for bank B outputs
FSELC	Input	LVCMOS	Frequency divider select for bank C outputs
$\overline{\text{PLL\_EN}}$	Input	LVCMOS	PLL enable/disable
MR/$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
QA0–4, QB0–3, QC0–1	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CCA}. Please see Applications Information section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
F_RANGE, FSELA, FSELB, and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 9 and Table 10 for supported frequency ranges and output to input frequency ratios.			
F_RANGE	0	VCO ÷ 1 (High input frequency range)	VCO ÷ 2 (Low input frequency range)
FSELA	0	Output divider ÷ 4	Output divider ÷ 6
FSELB	0	Output divider ÷ 4	Output divider ÷ 2
FSELC	0	Output divider ÷ 2	Output divider ÷ 4
MR/$\overline{\text{OE}}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset, the PLL feedback loop is open and the VCO is operating at its lowest frequency. The MPC9352 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CCLK).
$\overline{\text{PLL\_EN}}$	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC9352 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	DC Input Current		±20	mA
I_{OUT}	DC Output Current		±50	mA
T_S	Storage Temperature	–65	125	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -24 mA(1)
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output impedance		14 – 17		Ω	
I_{IN}	Input Current(2)			±200	μA	V_{IN} = V_{CC} or V_{IN} = GND
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}(3)	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

1. The MPC9352 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. Inputs have pull-down resistors affecting the input current.
3. I_{CCQ} is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40° to 85°C)(1)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode(2) ÷4 feedback ÷6 feedback ÷8 feedback ÷12 feedback Input reference frequency in PLL bypass mode(3)	50.0 33.3 25.0 16.67		100.0 66.6 50.0 33.3 250.0	MHz MHz MHz MHz MHz	
f_{VCO}	VCO lock frequency range(4)	200		400	MHz	
f_{MAX}	Output Frequency ÷2 output(5) ÷4 output ÷6 output ÷8 output ÷12 output	100 50 33.3 25 16.67		200 100 66.6 50 33.3	MHz MHz MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0 V
$t_{(\varnothing)}$	Propagation Delay CCLK to FB_IN f_{ref} > 40 MHz (static phase offset) f_{ref} < 40 MHz	–50 –200		+150 +150	ps ps	PLL locked
$t_{sk(O)}$	Output-to-output Skew(6) all outputs, any frequency within QA output bank within QB output bank within QC output bank			200 200 100 100	ps ps ps ps	
DC	Output duty cycle	47	50	53	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time			8	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter output frequencies mixed outputs are in any ÷4 and ÷6 combination all outputs same frequency			 400 250 100	 ps ps ps	
$t_{JIT(PER)}$	Period Jitter output frequencies mixed outputs are in any ÷4 and ÷6 combination all outputs same frequency			200 150 75	ps ps ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter ÷4 feedback divider RMS (1 σ)(7) ÷6 feedback divider RMS (1 σ) ÷8 feedback divider RMS (1 σ) ÷12 feedback divider RMS (1 σ)		15 20 18 – 20 25		ps ps ps ps	
BW	PLL closed loop bandwidth(8) ÷4 feedback ÷6 feedback ÷8 feedback ÷12 feedback		3.0 – 10.0 1.5 – 6.0 1.0 – 3.5 0.5 – 2.0		MHz MHz MHz MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. PLL mode requires $\overline{PLL\_EN}$=0 to enable the PLL and zero-delay operation. It is not recommended to use a ÷2 divider for feedback.
3. In PLL bypass mode, the MPC9352 divides the input reference clock.
4. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
5. See Table 9 and Table 10 for output divider configurations.
6. See Applications Information section for part-to-part skew calculation.
7. See Applications Information section for a jitter calculation for other confidence factors than 1 σ.
8. -3 dB point of PLL transfer characteristics.

Table 7. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	–0.3		0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH} = –15 mA(1)
V_{OL}	Output Low Voltage			0.6	V	I_{OL} = 15mA
Z_{OUT}	Output Impedance		17 – 20		Ω	
I_{IN}	Input Current			±200	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CCQ}(2)	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

1. The MPC9352 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines per output.
2. I_{CCQ} is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

Table 8. AC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)**(1)**

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode(2) ÷4 feedback ÷6 feedback ÷8 feedback ÷12 feedback Input reference frequency in PLL bypass mode(3)	50.0 33.3 25.0 16.67		100.0 66.6 50.0 33.3 250.0	MHz MHz MHz MHz MHz	
f_{VCO}	VCO lock frequency range(4)	200		400	MHz	
f_{MAX}	Output Frequency ÷2 output(5) ÷4 output ÷6 output ÷8 output ÷12 output	100 50 33.3 25 16.67		200 100 66.6 50 33.3	MHz MHz MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	0.8 to 2.0 V
$t_{(\varnothing)}$	Propagation Delay CCLK to FB_IN (static phase offset) f_{ref} > 40 MHz f_{ref} < 40 MHz	–50 –200		+150 +150	ps ps	PLL locked
$t_{sk(O)}$	Output-to-output Skew(6) all outputs, any frequency within QA output bank within QB output bank within QC output bank			200 200 100 100	ps ps ps ps	
DC	Output duty cycle	47	50	53	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8 V
$t_{PLZ, HZ}$	Output Disable Time			8	ns	
$t_{PZL, ZH}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter output frequencies mixed RMS (1 σ) outputs are in any ÷4 and ÷6 combination RMS (1 σ) all outputs same frequency RMS (1 σ)			 400 250 100	 ps ps ps	
$t_{JIT(PER)}$	Period Jitter output frequencies mixed RMS (1 σ) outputs are in any ÷4 and ÷6 combination RMS (1 σ) all outputs same frequency RMS (1 σ)			200 150 75	ps ps ps	

Table 8. AC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)**(1)** (Continued)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$t_{JIT(\varnothing)}$	I/O Phase Jitter	÷4 feedback divider RMS (1 σ)(7) ÷6 feedback divider RMS (1 σ) ÷8 feedback divider RMS (1 σ) ÷12 feedback divider RMS (1 σ)		15 20 18 – 20 25		ps ps ps ps	
BW	PLL closed loop bandwidth(8)	÷4 feedback ÷6 feedback ÷8 feedback ÷12 feedback		1.0 – 8.0 0.7 – 3.0 0.5 – 2.5 0.4 – 1.0		MHz MHz MHz MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. PLL mode requires PLL_EN=0 to enable the PLL and zero-delay operation. It is not recommended to use a ÷2 divider for feedback.
3. In PLL bypass mode, the MPC9352 divides the input reference clock.
4. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
5. See Table 9 and Table 10 for output divider configurations.
6. See application section for part-to-part skew calculation.
7. See application section for a jitter calculation for other confidence factors than 1 σ.
8. -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC9352

The MPC9352 supports output clock frequencies from 16.67 to 200 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 400 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:3, 3:2 as well as 2:3, 3:1 and 2:1. Table 9 and Table 10 illustrates the various output configurations and frequency ratios supported by the MPC9352. See also Figure 3 to Figure 6 for further reference. A ÷2 output divider cannot be used for feedback.

Table 9. MPC9352 Example Configuration (F_RANGE = 0)

PLL Feedback	fref(1) [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 4(2)	50-100	0	0	0	fref (50-100 MHz)	fref (50-100 MHz)	fref * 2 (100-200 MHz)
		0	0	1	fref (50-100 MHz)	fref (50-100 MHz)	fref (50-100 MHz)
		1	0	0	fref * 2÷3 (33-66 MHz)	fref (50-100 MHz)	fref * 2 (100-200 MHz)
		1	0	1	fref * 2÷3 (33-66 MHz)	fref (50-100 MHz)	fref (50-100 MHz)
VCO ÷ 6(3)	33.3-66.67	1	0	0	fref (33-66 MHz)	fref * 3÷2 (50-100 MHz)	fref * 3 (100-200 MHz)
		1	0	1	fref (33-66 MHz)	fref * 3÷2 (50-100 MHz)	fref * 3÷2 (50-100 MHz)
		1	1	0	fref (33-66 MHz)	fref * 3 (100-200 MHz)	fref * 3 (100-200 MHz)
		1	1	1	fref (33-66 MHz)	fref * 3 (100-200 MHz)	fref * 3÷2 (50-100 MHz)

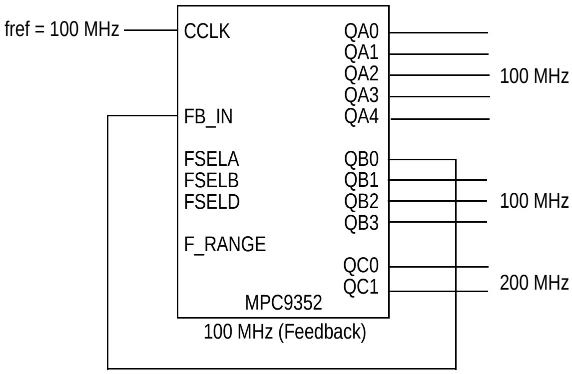
1. fref is the input clock reference frequency (CCLK).
2. QAx connected to FB_IN and FSELA=0.
3. QAx connected to FB_IN and FSELA=1.

Table 10. MPC9352 Example Configurations (F_RANGE = 1)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 8[2]	25-50	0	0	0	fref (25-50 MHz)	fref (25-50 MHz)	fref * 2 (50-100 MHz)
		0	0	1	fref (25-50 MHz)	fref (25-50 MHz)	fref (25-50 MHz)
		1	0	0	fref * 2÷3 (16-33 MHz)	fref (25-50 MHz)	fref * 2 (50-100 MHz)
		1	0	1	fref * 2÷3 (16-33 MHz)	fref (25-50 MHz)	fref (25-50 MHz)
VCO ÷ 12[3]	16.67-33.3	1	0	0	fref (16-33 MHz)	fref * 3÷2 (25-50 MHz)	fref * 3 (50-100 MHz)
		1	0	1	fref (16-33 MHz)	fref * 3÷2 (25-50 MHz)	fref * 3÷2 (25-50 MHz)
		1	1	0	fref (16-33 MHz)	fref * 3 (50-100 MHz)	fref * 3 (50-100 MHz)
		1	1	1	fref (16-33 MHz)	fref * 3 (50-100 MHz)	fref * 3÷2 (25-50 MHz)

1. fref is the input clock reference frequency (CCLK).
2. QAx connected to FB_IN and FSELA=0.
3. QAx connected to FB_IN and FSELA=1.

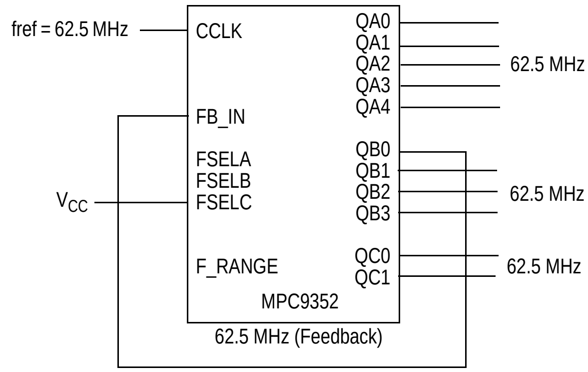
Example Configurations for the MPC9352



MPC9352 default configuration (feedback of QB0 = 100 MHz). All control pins are left open.

Frequency Range	Min	Max
Input	50 MHz	100 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	100 MHz	200 MHz

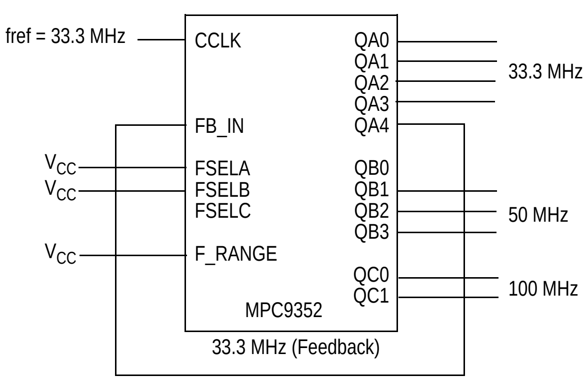
Figure 3. MPC9352 Default Configuration



MPC9352 zero-delay (feedback of QB0 = 62.5 MHz). All control pins are left open except FSELC = 1. All outputs are locked in frequency and phase to the input clock.

Frequency Range	Min	Max
Input	50 MHz	100 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	50 MHz	100 MHz

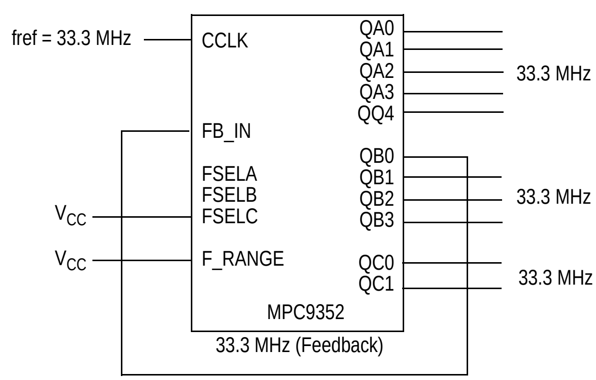
Figure 4. MPC9352 Zero Delay Buffer Configuration



MPC9352 configuration to multiply the reference frequency by 3, 3 ÷ 2 and 1. PLL feedback of QA4 = 33.3 MHz.

Frequency Range	Min	Max
Input	25 MHz	50 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	100 MHz	200 MHz

Figure 5. MPC9352 Default Configuration



MPC9352 zero-delay (feedback of QB0 = 33.3 MHz). Equivalent to Table 2 except F_RANGE = 1 enabling a lower input and output clock frequency.

Frequency Range	Min	Max
Input	25 MHz	50 MHz
QA outputs	25 MHz	50 MHz
QB outputs	25 MHz	50 MHz
QC outputs	25 MHz	50 MHz

Figure 6. MPC9352 Zero Delay Buffer Configuration 2

Power Supply Filtering

The MPC9352 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance, I/O jitter. The MPC9352 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9352. Figure 7 illustrates a typical power supply filter scheme. The MPC9352 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range; therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet, the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325 V (V_{CC} = 3.3 V or V_{CC} = 2.5 V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 7 should have a resistance of 5–15 Ω (V_{CC} = 3.3 V) or 9–10 Ω (V_{CC} = 2.5 V) to meet the voltage drop criteria.

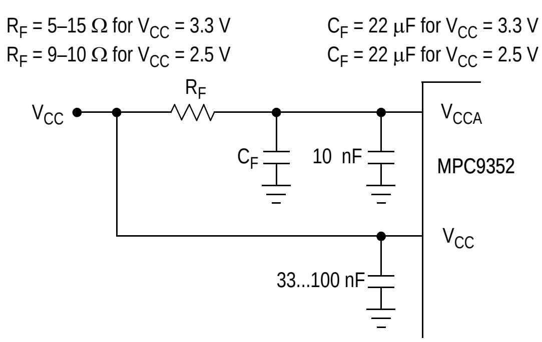


Figure 7. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics. The RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7, the filter cut-off frequency is around 3–5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive, and thus, increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9352 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9352 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9352. Designs using the MPC9352 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9352 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9352 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9352 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter.

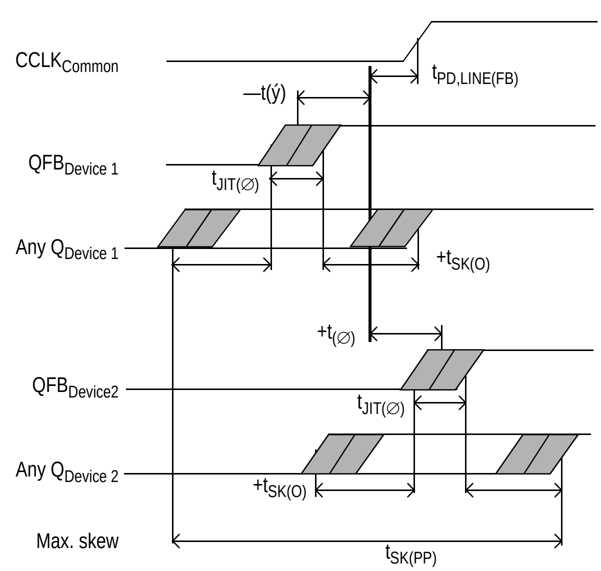


Figure 8. MPC9352 Max. Device-to-Device Skew

Due to the statistical nature of I/O jitter, a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 11.

Table 11. Confidence Factor CF

CF	Probability of clock edge within the distribution
$\pm 1\sigma$	0.68268948
$\pm 2\sigma$	0.95449988
$\pm 3\sigma$	0.99730007
$\pm 4\sigma$	0.99993663
$\pm 5\sigma$	0.99999943
$\pm 6\sigma$	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation, an I/O jitter confidence factor of 99.7% ($\pm 3\sigma$) is assumed, resulting in a worst case timing uncertainty from input to any output of –445 ps to 395 ps relative to CCLK:

$$t_{SK(PP)} = [-200ps...150ps] + [-200ps...200ps] + [(15ps \bullet -3)...(15ps \bullet 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [-445ps...395ps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 9 can be used for a more precise timing performance analysis.

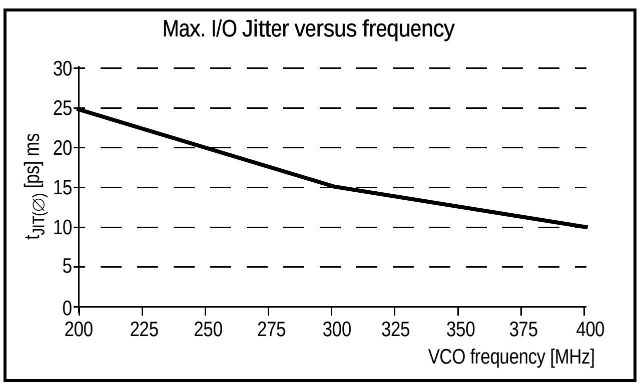


Figure 9. Max. I/O Jitter versus Frequency

Driving Transmission Lines

The MPC9352 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω, the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}\div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9352 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9352 clock driver is effectively doubled due to its capability to drive multiple lines.

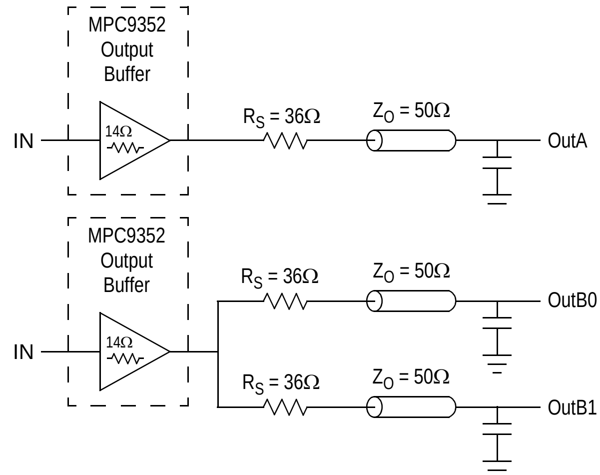


Figure 10. Single versus Dual Transmission Lines

The waveform plots in Figure 11 show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9352 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9352. The output waveform in Figure 11 shows a step in the waveform. This step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor, plus the output impedance, does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega\ ||\ 50\ \Omega$$
$$R_S = 36\ \Omega\ ||\ 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18+17+25))$$
$$= 1.31\ V$$

At the load end, the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

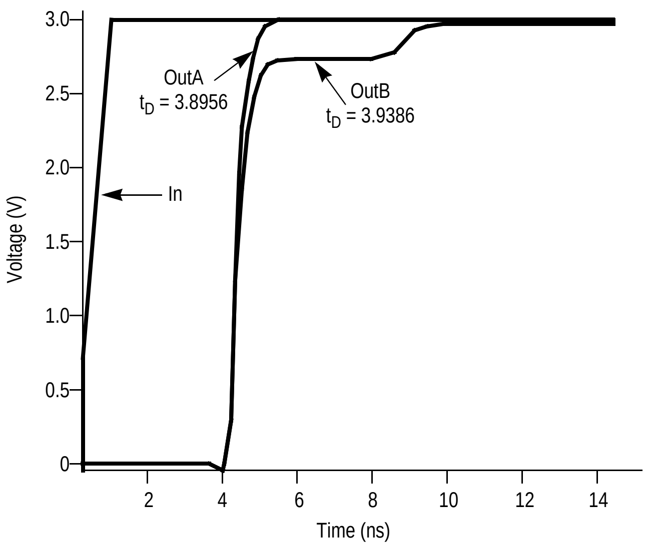
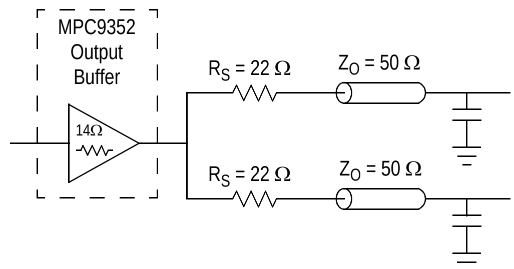


Figure 11. Single versus Dual Waveforms

Since this step is well above, the threshold region, it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 12 should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.



$$14\ \Omega + 22\ \Omega \,||\, 22\ \Omega = 50\ \Omega \,||\, 50\ \Omega$$
$$25\ \Omega = 25\ \Omega$$

Figure 12. Optimized Dual Line Termination

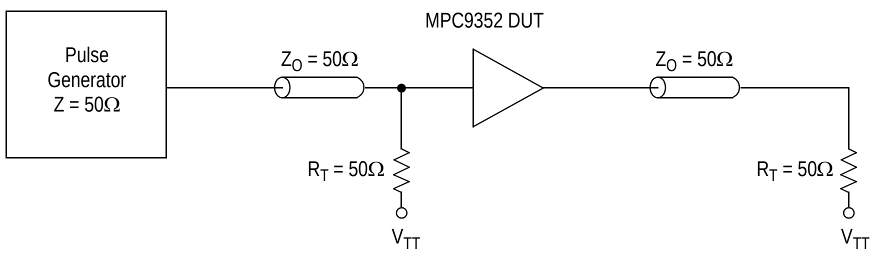
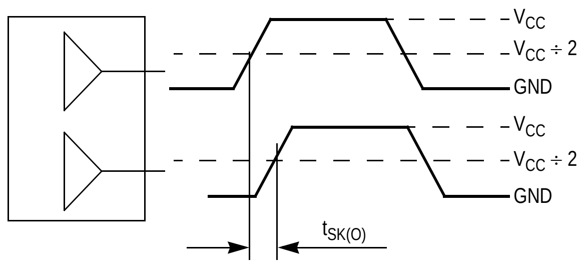


Figure 13. CCLK MPC9352 AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device.

Figure 14. Output-to-Output Skew $t_{SK(O)}$

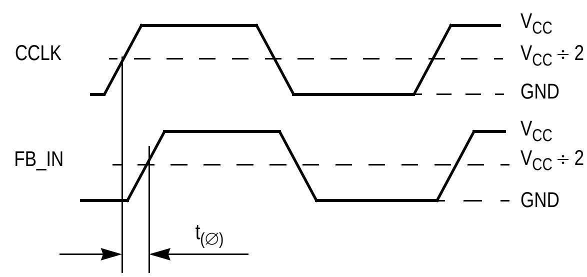
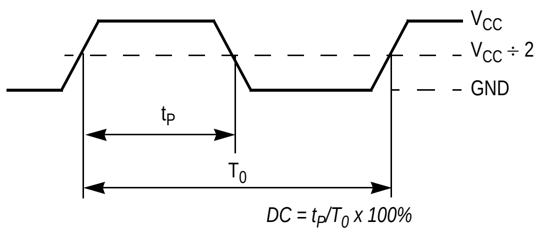
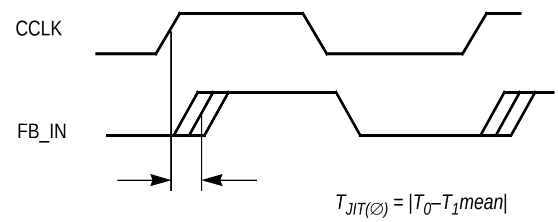


Figure 15. Propagation Delay ($t_{(\varnothing)}$, static phase offset) Test Reference



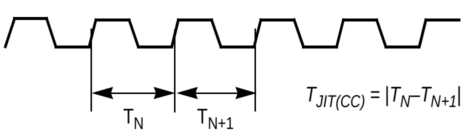
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 16. Output Duty Cycle (DC)



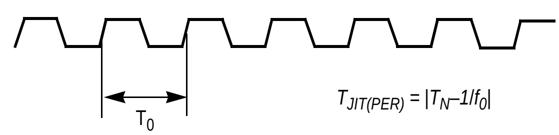
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles.

Figure 17. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

Figure 18. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles.

Figure 19. Period Jitter

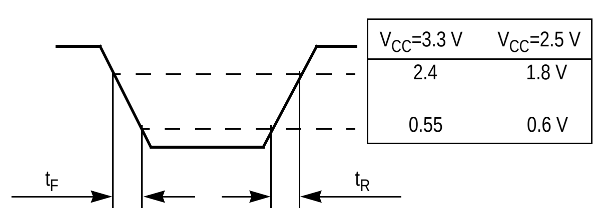
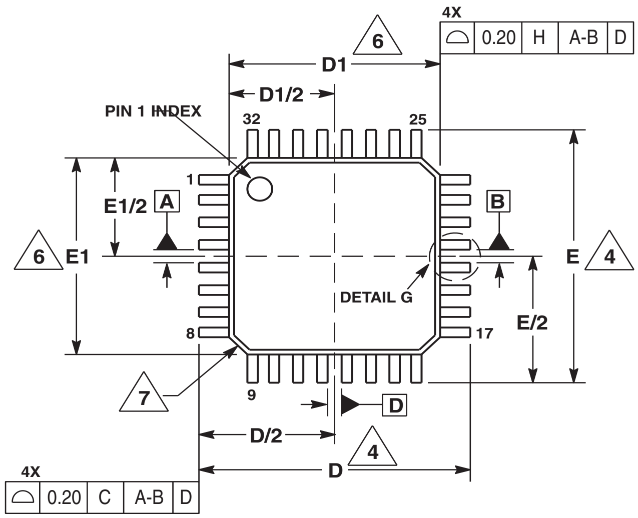
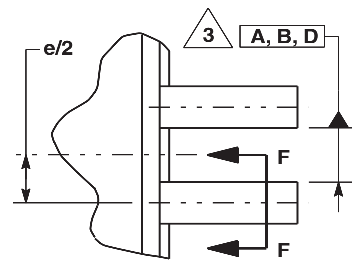


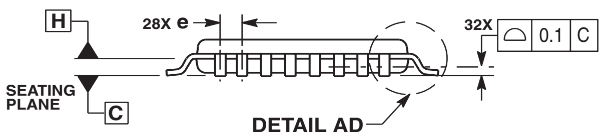
Figure 20. Output Transition Time Test Reference

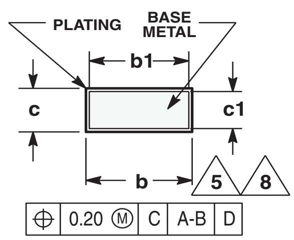
PACKAGE DIMENSIONS



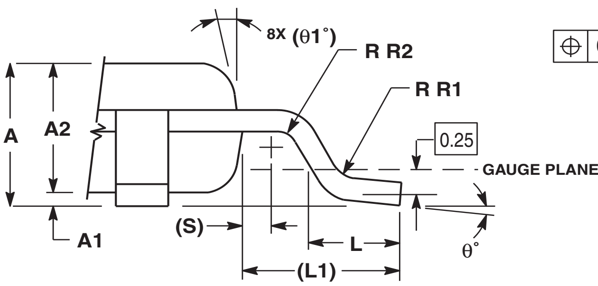


DETAIL G





SECTION F-F



DETAIL AD

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0˚	7˚
q1	12 REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

CASE 873A-03
ISSUE B

DATE 03/10/00

CASE 873A-03
ISSUE B
32-LEAD LQFP PACKAGE

Revision History

Rev.	Originator	Date	Description of Change
7	Jinzhu Li	05/30/06	Corrected Figure 2, 32-Lead Package Pinout, pin 12 from nQA0 to QA0.
8	S. Nolan	11/16/12	Removed leaded parts.
8	J Dela Torre	1/7/13	NRND – Not Recommend for New Designs. Use replacement part ICS87952.
8	J Dela Torre	1/31/13	Removed replacement part from features list.
8		3/14/16	Product Discontinuation Notice - Last time buy expires September 7, 2016. PDN N-16-02

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