Freescale Semiconductor
Technical Data

Document Number: MRF7S21080H
Rev. 1, 3/2011

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF7S21080HR3
MRF7S21080HSR3

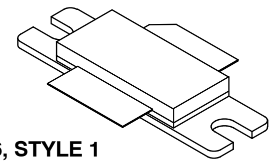
Designed for CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for TD-SCDMA and PCN-PCS/cellular radio applications.

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 800 mA, P_{out} = 22 Watts Avg., f = 2167.5 MHz, IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  Power Gain — 18 dB
  Drain Efficiency — 32%
  Device Output Signal PAR — 6.5 dB @ 0.01% Probability on CCDF
  ACPR @ 5 MHz Offset — -38 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 2140 MHz, 80 Watts CW Peak Tuned Output Power
- P_{out} @ 1 dB Compression Point ≃ 80 Watts CW

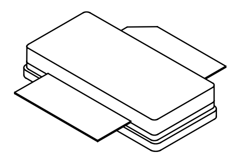
Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13 inch Reel.

2110-2170 MHz, 22 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465-06, STYLE 1
NI-780
MRF7S21080HR3



CASE 465A-06, STYLE 1
NI-780S
MRF7S21080HSR3

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 79°C, 79 W CW Case Temperature 75°C, 22 W CW	$R_{\theta JC}$	 0.60 0.65	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

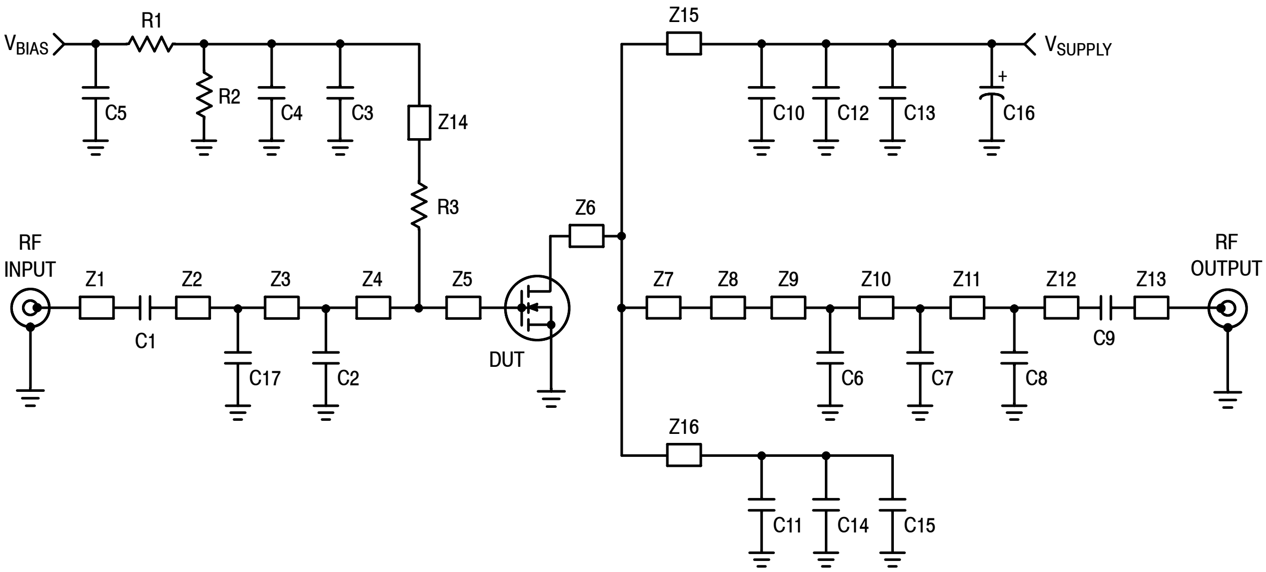
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 174 μAdc)	$V_{GS(th)}$	1.5	2	3	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 800 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (1) (V_{DD} = 28 Vdc, I_D = 800 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4	5.5	7	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.74 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
Dynamic Characteristics (2)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	0.64	—	pF
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	296	—	pF
Input Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	160	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 800 mA, P_{out} = 22 W Avg., f = 2167.5 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	16.5	18	19.5	dB
Drain Efficiency	η_D	30	32	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.7	6.5	—	dB
Adjacent Channel Power Ratio	ACPR	—	-38	-35	dBc
Input Return Loss	IRL	—	-16	-9	dB

1. V_{GG} = 2 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
2. Part internally matched both on input and output.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 800 mA, 2110-2170 MHz Bandwidth					
Video Bandwidth @ 70 W PEP P_{out} where IM3 = -30 dBc (Tone Spacing from 100 kHz to VBW) ΔIMD3 = IMD3 @ VBW frequency - IMD3 @ 100 kHz <1 dBc (both sidebands)	VBW	—	10	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 22 W Avg.	G_F	—	0.12	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P_{out} = 80 W CW	Φ	—	22.3	—	°
Average Group Delay @ P_{out} = 80 W CW, f = 2140 MHz	Delay	—	6.21	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 80 W CW, f = 2140 MHz, Six Sigma Window	ΔΦ	—	151.6	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.009	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.008	—	dB/°C



Z1	0.325″ x 0.083″ Microstrip	Z10*	0.457″ x 0.083″ Microstrip
Z2*	0.921″ x 0.083″ Microstrip	Z11*	0.118″ x 0.083″ Microstrip
Z3*	0.126″ x 0.083″ Microstrip	Z12*	0.206″ x 0.083″ Microstrip
Z4*	0.645″ x 0.083″ Microstrip	Z13	0.301″ x 0.083″ Microstrip
Z5	0.275″ x 0.669″ Microstrip	Z14*	1.220″ x 0.080″ Microstrip
Z6	0.114″ x 0.764″ Microstrip	Z15, Z16*	0.720″ x 0.080″ Microstrip
Z7	0.374″ x 0.764″ Microstrip	PCB	Taconic TLX8-0300, 0.030″, ε_r = 2.55
Z8	0.180″ x 0.524″ Microstrip		
Z9*	0.075″ x 0.083″ Microstrip		

* Variable for tuning

Figure 1. MRF7S21080HR3(HSR3) Test Circuit Schematic

Table 5. MRF7S21080HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C3, C9, C10, C11	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C2	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C4	220 nF Chip Capacitor	18125C224KAT1A	AVX
C5, C12, C13, C14, C15	10 μF, 50 V Chip Capacitors	C5750X5R1H106M	TDK
C6	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
C7, C8, C17	0.2 pF Chip Capacitors	ATC100B0R2BT500XT	ATC
C16	220 μF, 63 V Electrolytic Capacitor, Radial	222213668221	Vishay
R1, R2	2 KΩ, 1/4 W Chip Resistors	CRCW12062001FKEA	Vishay
R3	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay

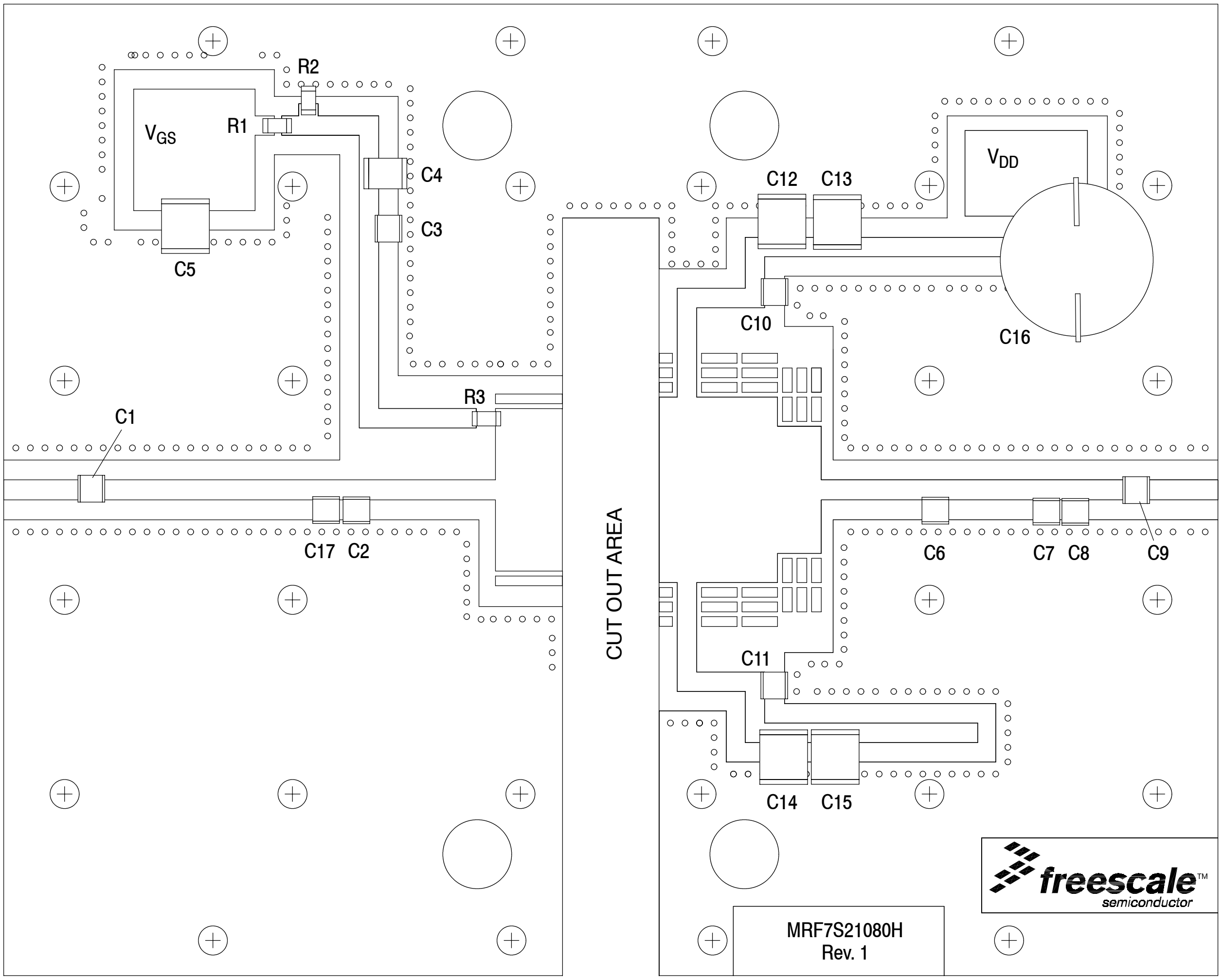


Figure 2. MRF7S21080HR3(HSR3) Test Circuit Component Layout

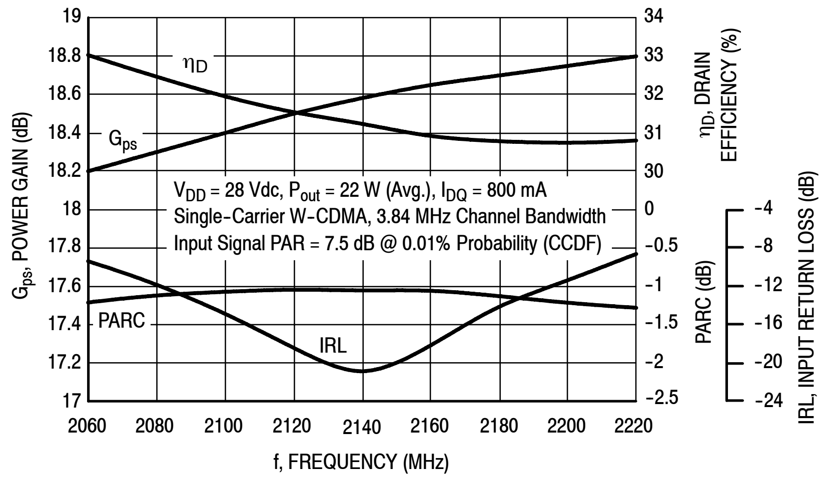


Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 22 Watts Avg.

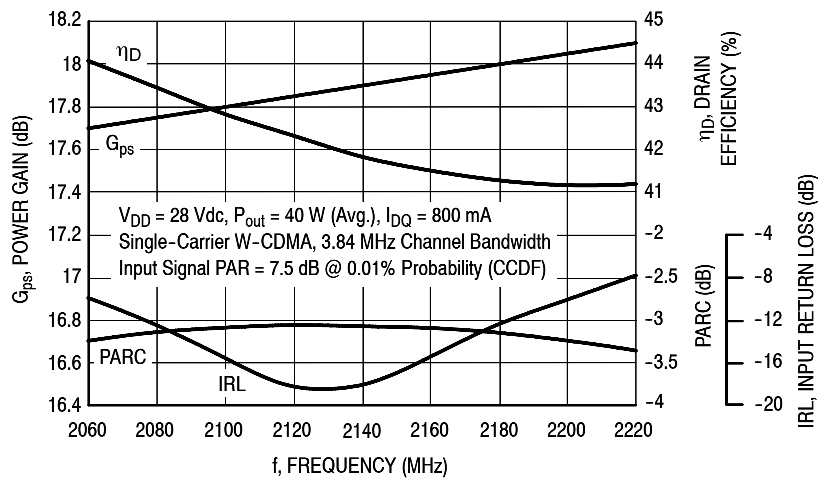


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 40 Watts Avg.

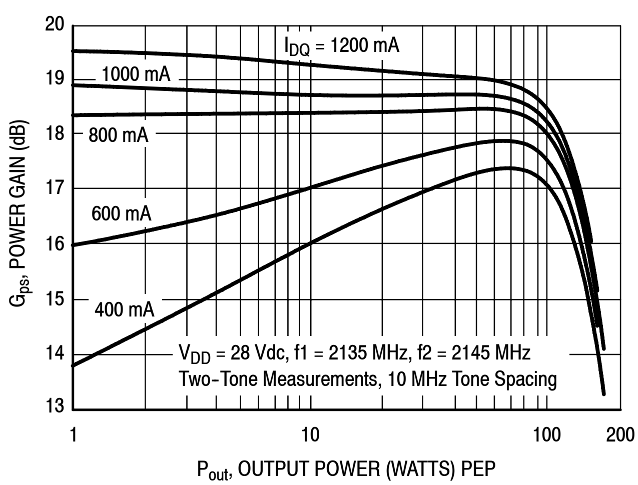


Figure 5. Two-Tone Power Gain versus Output Power

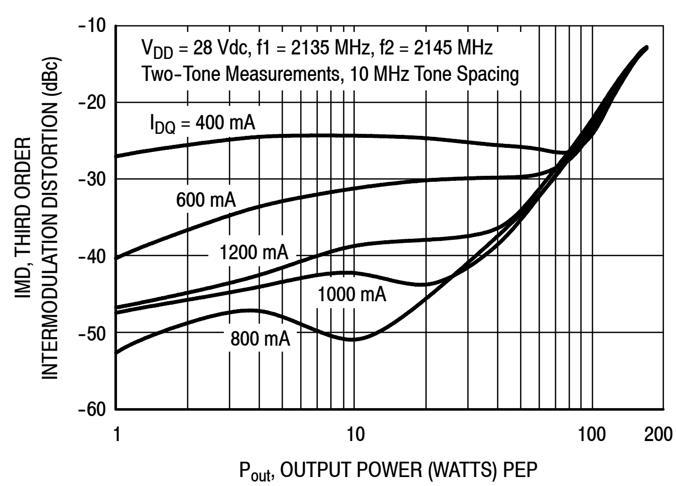


Figure 6. Third Order Intermodulation Distortion versus Output Power

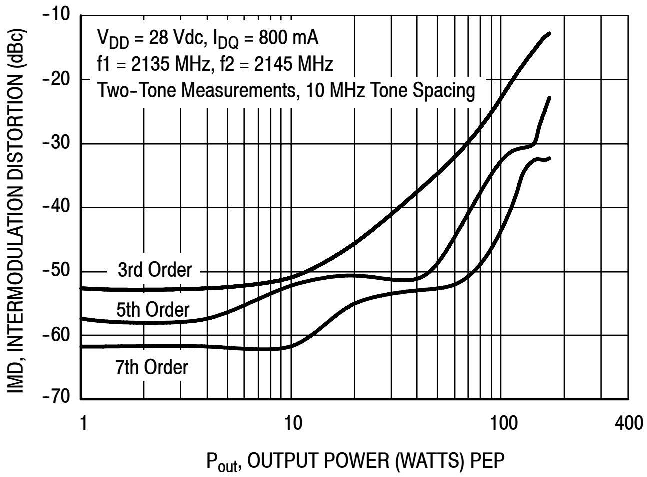


Figure 7. Intermodulation Distortion Products versus Output Power

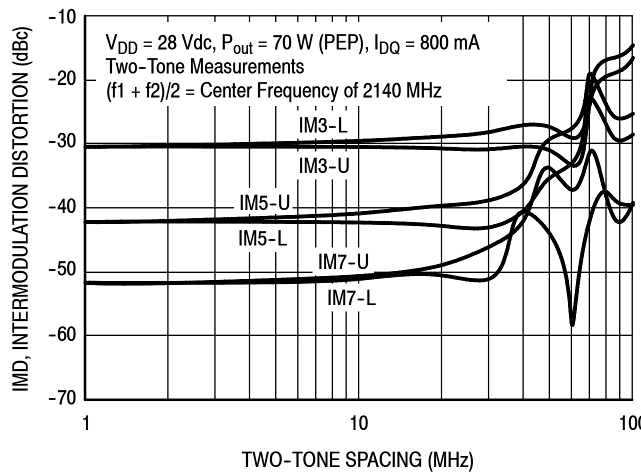


Figure 8. Intermodulation Distortion Products versus Tone Spacing

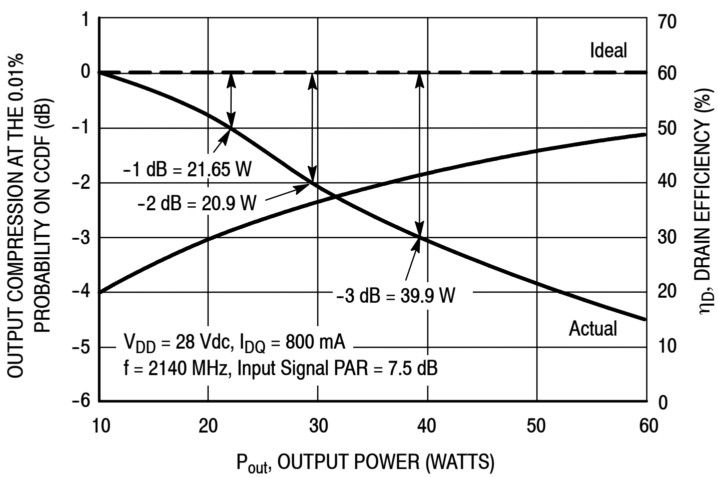


Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

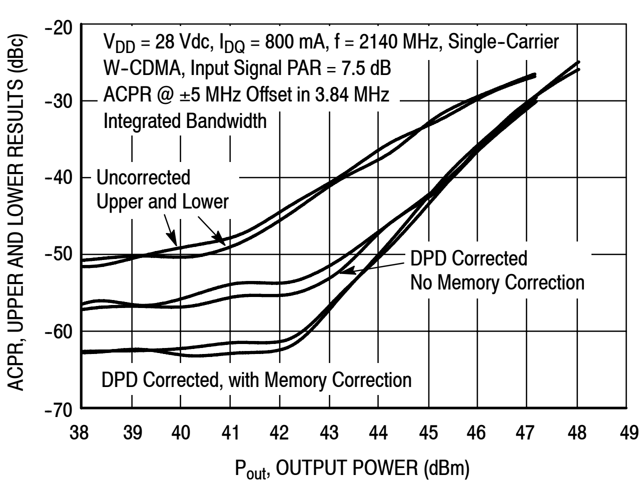


Figure 10. Digital Predistortion Correction versus ACPR and Output Power

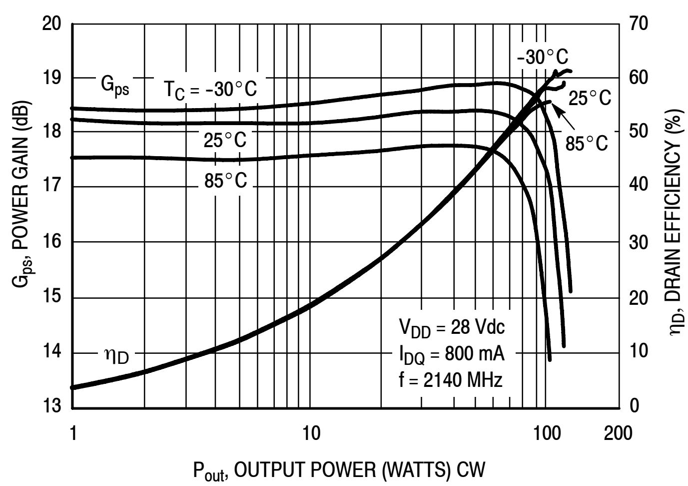


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

TYPICAL CHARACTERISTICS

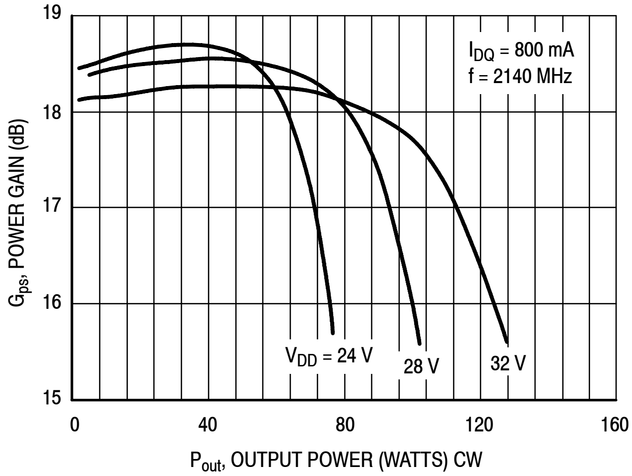


Figure 12. Power Gain versus Output Power

W-CDMA TEST SIGNAL

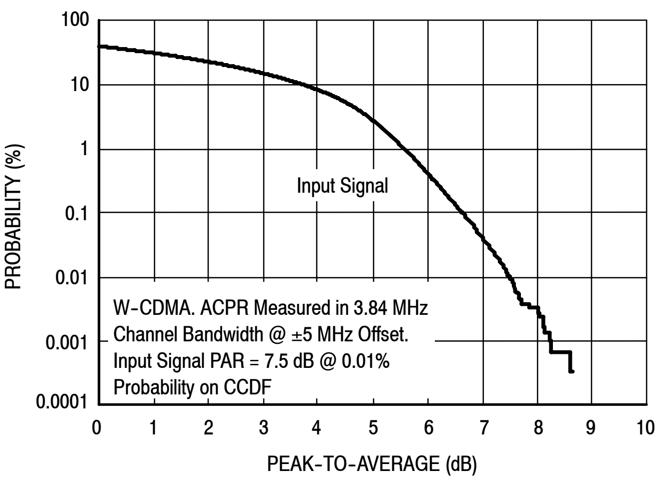


Figure 13. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

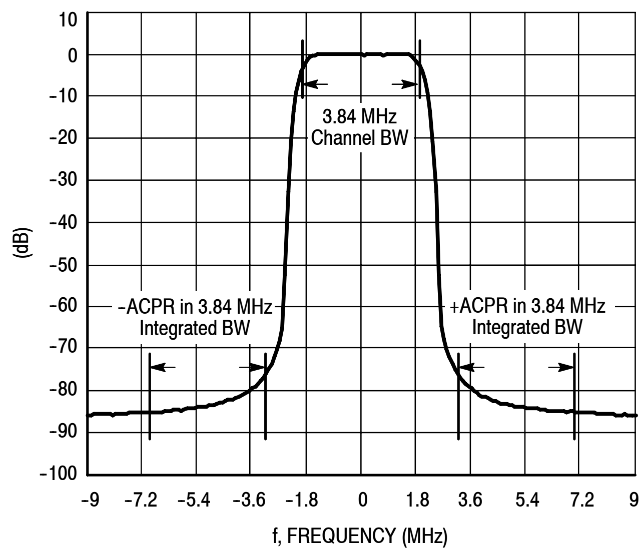
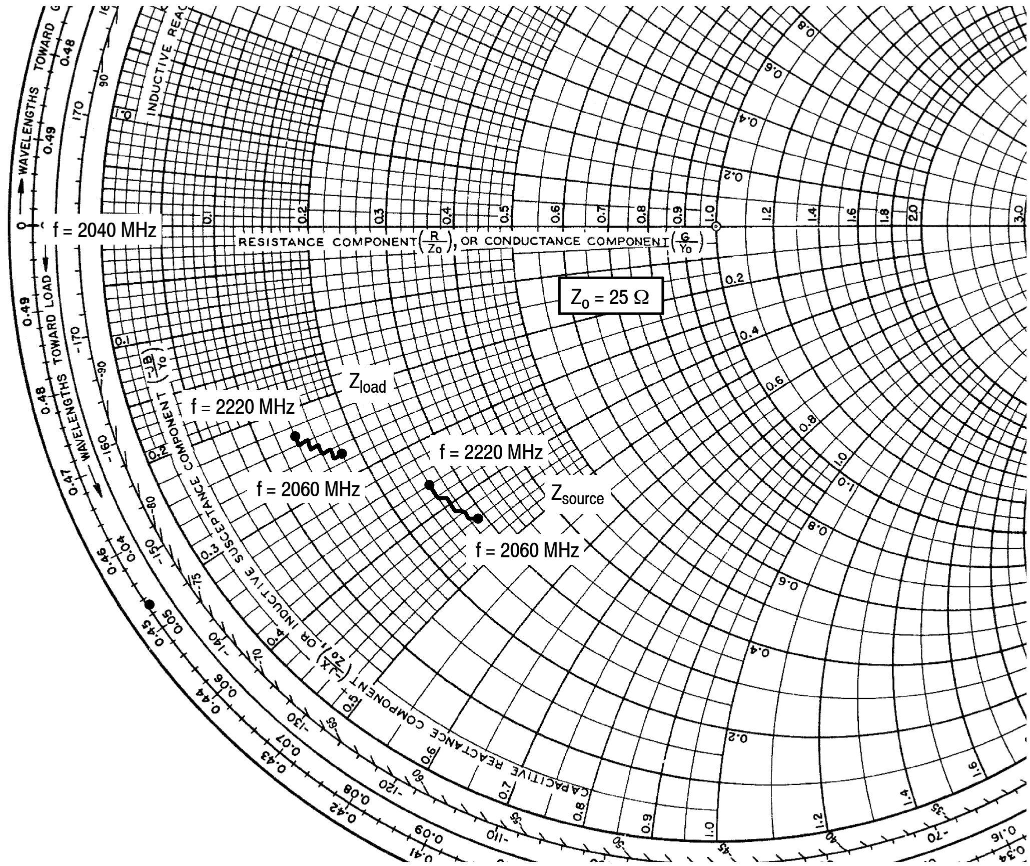


Figure 14. Single-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 800 mA, P_{out} = 22 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2060	7.16 - j11.074	4.403 - j6.809
2080	7.066 - j10.796	4.275 - j6.662
2100	6.954 - j10.526	4.147 - j6.515
2120	6.857 - j10.260	4.017 - j6.375
2140	6.745 - j9.980	3.889 - j6.233
2160	6.668 - j9.728	3.764 - j6.126
2180	6.588 - j9.462	3.642 - j6.016
2200	6.511 - j9.203	3.519 - j5.895
2220	6.403 - j8.892	3.401 - j5.774

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

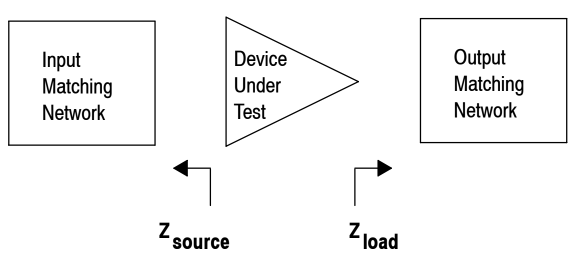
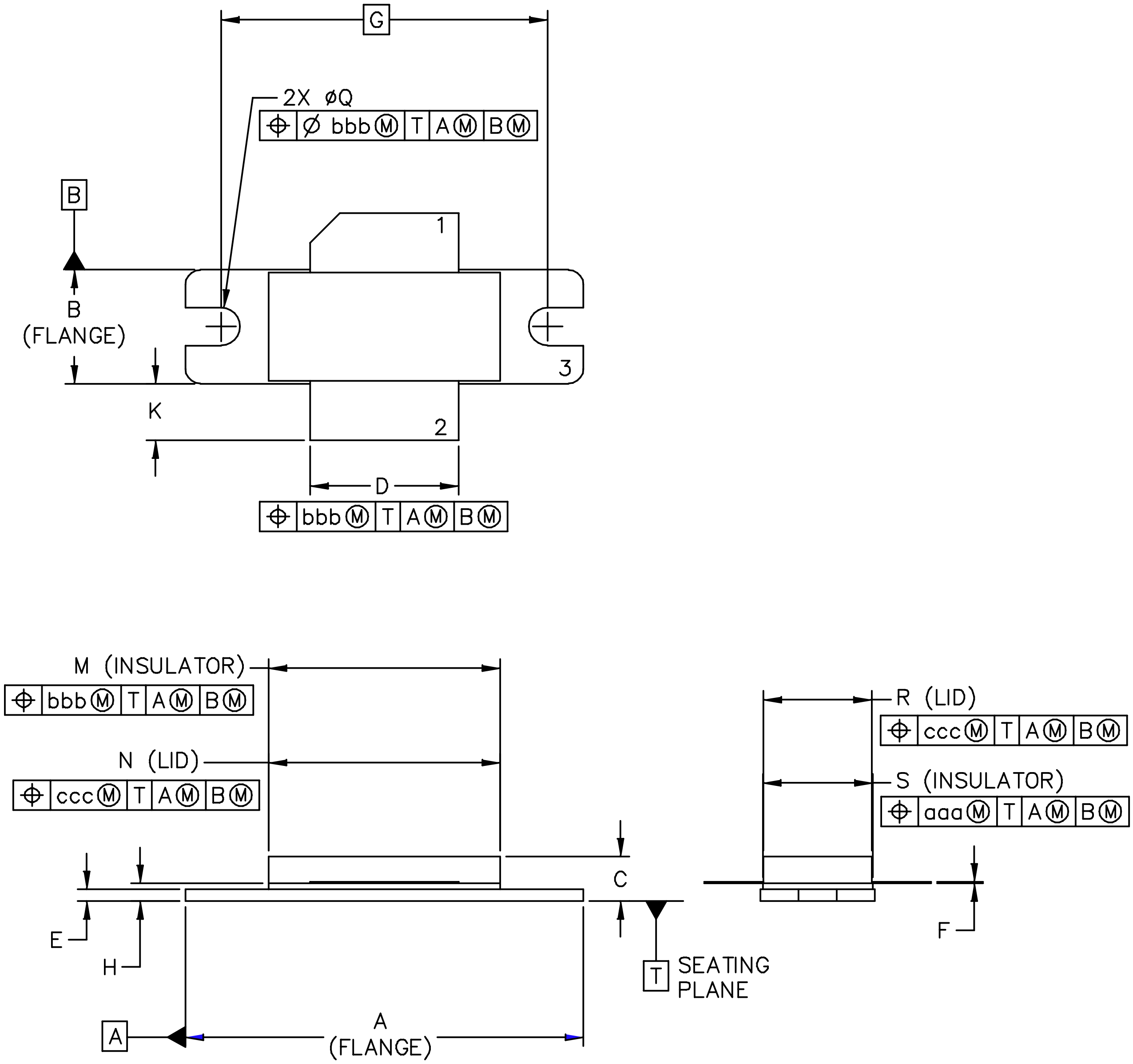


Figure 15. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M—1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX	DIM	INCH MIN		INCH MAX	MILLIMETER MIN		MILLIMETER MAX
A	1.335	–	1.345	33.91	–	34.16	R	.365	–	.375	9.27	–	9.53
B	.380	–	.390	9.65	–	9.91	S	.365	–	.375	9.27	–	9.52
C	.125	–	.170	3.18	–	4.32	aaa	–	.005	–	–	0.127	–
D	.495	–	.505	12.57	–	12.83	bbb	–	.010	–	–	0.254	–
E	.035	–	.045	0.89	–	1.14	ccc	–	.015	–	–	0.381	–
F	.003	–	.006	0.08	–	0.15	–	–	–	–	–	–	–
G	1.100 BSC			27.94 BSC			–	–	–	–	–	–	–
H	.057	–	.067	1.45	–	1.7	–	–	–	–	–	–	–
K	.170	–	.210	4.32	–	5.33	–	–	–	–	–	–	–
M	.774	–	.786	19.66	–	19.96	–	–	–	–	–	–	–
N	.772	–	.788	19.6	–	20	–	–	–	–	–	–	–
Q	ø.118	–	ø.138	ø3	–	ø3.51	–	–	–	–	–	–	–

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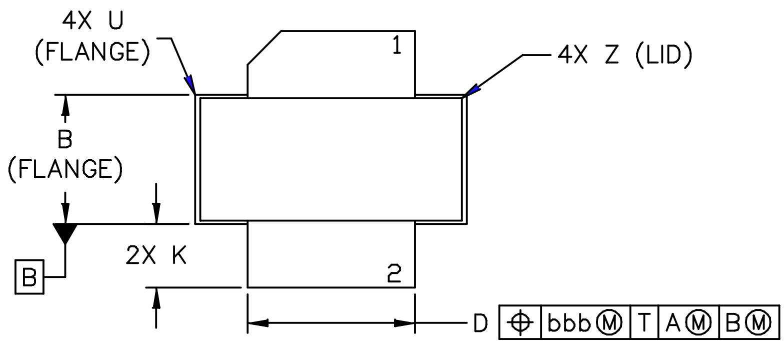

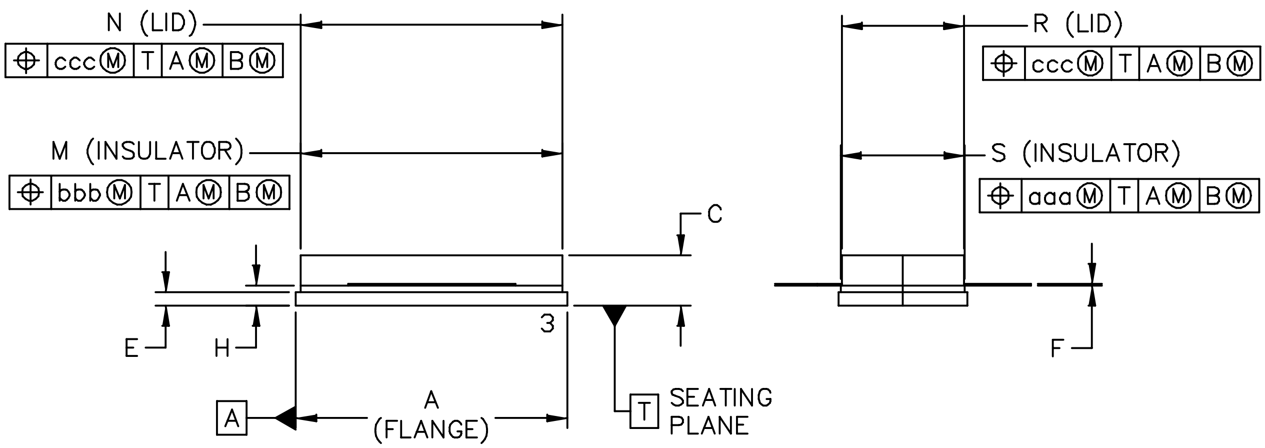

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STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

	INCH			MILLIMETER				INCH			MILLIMETER		
DIM	MIN		MAX	MIN		MAX	DIM	MIN		MAX	MIN		MAX
A	.805	–	.815	20.45	–	20.7	U	–	–	.040	–	–	1.02
B	.380	–	.390	9.65	–	9.91	Z	–	–	.030	–	–	0.76
C	.125	–	.170	3.18	–	4.32	aaa	–	.005	–	–	0.127	–
D	.495	–	.505	12.57	–	12.83	bbb	–	.010	–	–	0.254	–
E	.035	–	.045	0.89	–	1.14	ccc	–	.015	–	–	0.381	–
F	.003	–	.006	0.08	–	0.15	–	–	–	–	–	–	–
H	.057	–	.067	1.45	–	1.7	–	–	–	–	–	–	–
K	.170	–	.210	4.32	–	5.33	–	–	–	–	–	–	–
M	.774	–	.786	19.61	–	20.02	–	–	–	–	–	–	–
N	.772	–	.788	19.61	–	20.02	–	–	–	–	–	–	–
R	.365	–	.375	9.27	–	9.53	–	–	–	–	–	–	–
S	.365	–	.375	9.27	–	9.52	–	–	–	–	–	–	–

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PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2007	• Initial Release of Data Sheet
1	Mar. 2011	• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13628, p. 1, 2 • Fig. 13, MTTF versus Junction Temperature removed, p. 8. Refer to the device’s MTTF Calculator available at freescale.com/RFpower. Go to Design Resources > Software and Tools. • Fig. 14, CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal and Fig. 15, Single-Carrier W-CDMA Spectrum updated to show the undistorted input test signal, p. 8 (renumbered as Figs. 13 and 14 respectively after Fig. 13 removed) • Added Electromigration MTTF Calculator and RF High Power Model availability to Product Software, p. 14

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