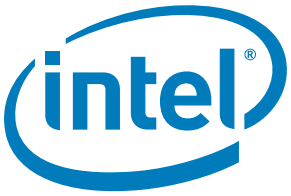


Intel® Pentium® Processor N3500-series, J2850, J2900, and Intel® Celeron® Processor N2900-series, N2800-series, J1800-series, J1900, J1750

Datasheet

November 2014

Revision 004

Document Number: 329670-004

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

Intel technologies may require enabled hardware, specific software, or services activation. Check with your system manufacturer or retailer.

All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

No computer system can be absolutely secure. Intel does not assume any liability for lost or stolen data or systems or any damages resulting from such losses.

No computer system can provide absolute security under all conditions. Intel® Trusted Execution Technology (Intel® TXT) requires a computer system with Intel® Virtualization Technology, an Intel TXT-enabled processor, chipset, BIOS, Authenticated Code Modules and an Intel TXT-compatible measured launched environment (MLE). The MLE could consist of a virtual machine monitor, an OS or an application. In addition, Intel TXT requires the system to contain a TPM v1.2, as defined by the Trusted Computing Group and specific software for some uses. For more information, see http://www.intel.com/technology/security/

Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain computer system software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

Intel® High Definition Audio (Intel® HD Audio): Requires an Intel® HD Audio enabled system. Consult your PC manufacturer for more information. Sound quality will depend on equipment and actual implementation. For more information about Intel® HD Audio, refer to http://www.intel.com/design/chipsets/hdaudio.htm

Hyper-Threading Technology requires a computer system with a processor supporting HT Technology and an HT Technology-enabled chipset, BIOS and operating system. Performance will vary depending on the specific hardware and software you use. For more information including details on which processors support HT Technology, see http://www.intel.com/info/hyperthreading.

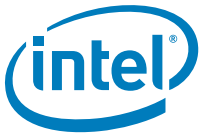
Enhanced Intel SpeedStep® Technology See the Processor Spec Finder or contact your Intel representative for more information.

64-bit computing on Intel architecture requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel® 64 architecture. Performance will vary depending on your hardware and software configurations. Consult with your system vendor for more information.

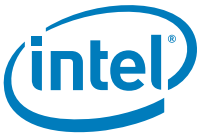
Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See www.intel.com/products/processor_number for details.

Intel, Celeron, Pentium and Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

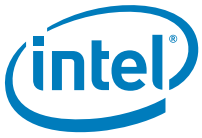
*Other names and brands may be claimed as the property of others.



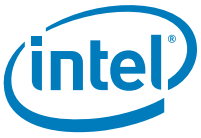
Contents

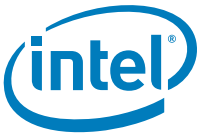


Figures



Tables

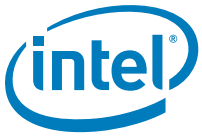




Revision History

Revision Number	Description	Revision Date
001	• Initial release	October 2013
002	• Minor edits throughout for clarity • Added Intel Pentium processor N3530 and N2930 • Added Intel Celeron processor N3830 and N2807 • Added Intel Pentium processor J2900 • Added Intel Celeron processor J1900 Chapter 1 • Updated the table details of the to include new SKUs • Updated feature overview for interfaces that are supported for Windows 8.1 Non Connected Standby Chapter 2 • Updated the table details of the GPIO Signals for GPIO_S0_SC[046], GPIO_S0_SC[047], GPIO_S0_SC[048], GPIO_S5[15], GPIO_S5[16], GPIO_S5[17] Chapter 5 • Added table note (Processor Clock Outputs) that Intel recommends 25 MHz. 19.2 MHz is not validated Chapter 6 • De-featured C6IS for all SKUs • Removed C1E power state - Updated Section 6.3.4, Processor Core C-States Description - Updated 6.3.5, Package C-States • Remove Table's note that S0ix is supported only on the Premium SKU. • Table 40, Processor Sx-States to SLP_S*#. Updated the table details of the SoC Sx-States to SLPT_S*# for PMC_PLTRST# from 0 or 1 to High or Low to match platform understanding. Chapter 7 • Updated the figure and notes of the S0 to S3 to S4/S5 (Power Down) Sequence without S0ix Chapter 8 • Table 51, Processor Thermal Specifications. Updated the table details of the Thermal Specification to include new SKUs. Added the table note to clarify the definition for (Tj) at TDP and (Tj,max). • Section 8.3, Voltage and Current Specifications. Remove VCC and VNN from Processor Power Rail DC Specifications and Max Current table. • Updated Table 53, Processor VCC and VNN Currents Chapter 10 • Updated Section 10.1 note on Thermal management support • Updated Table 91, Supported DDR3L SO-DIMM Size Chapter 13 • Updated sub-chapter VED (Video Encode/Decode) that Video encode is NOT supported on all SKUs Chapter 14 • Figure 18, xHCI and EHCI Port Mapping. Added figure note. • Section 14.6.45, USB2 Port Disable Override (USB2PDO)—Offset E4h. Updated to correctly reflect the power well. • Added Section 14.7, USB xHCI Memory Mapped I/O Registers Chapter 15 • Updated register content Chapter 25 • Updated register content	March 2014
003	• Added Intel Pentium processor N3540 • Added Intel Celeron processor N2940, N2840, and N2808 • Added Section 1.2.10.1, Low Power Engine (LPE) Audio • Added Chapter 16, Low Power Engine (LPE) for Audio (I^2S)	July 2014
004	• Added N2807 SKU to Table 53, VCC and VNN Currents	November 2014

§



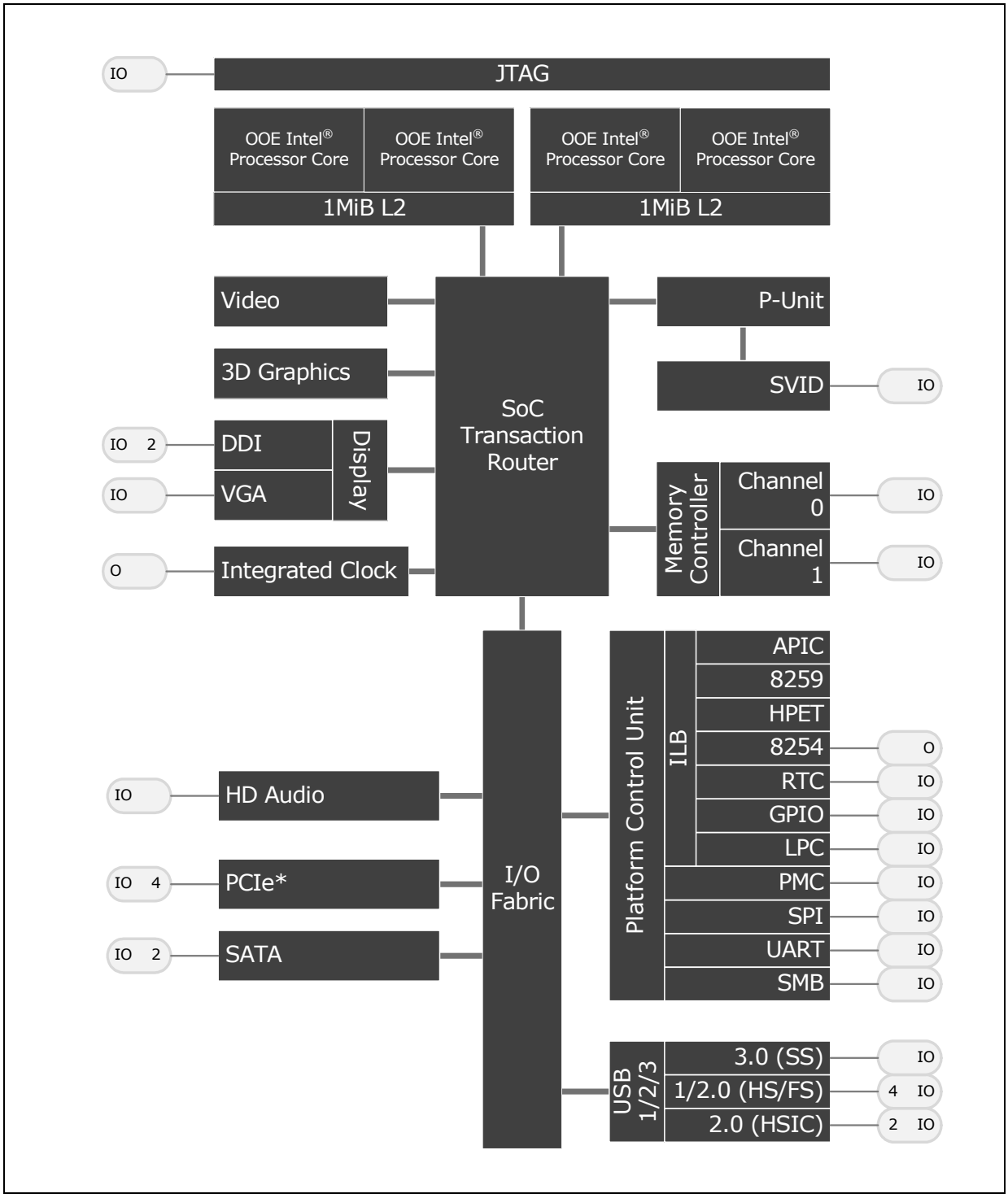
1 Introduction

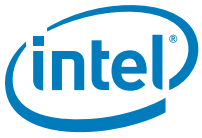
Intel® Pentium® processor N3500-series, J2850, J2900, and Intel® Celeron® processor N2900-series, N2800-series, J1800-series, J1750 are Intel Architecture (IA) processors that integrate with the next generation Intel® processor core, Graphics, Memory Controller, and I/O interfaces into a single system-on-chip solution.

The following figures show the system-level block diagram of the processor. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

Note: Intel® Pentium® processor N3500-series, J2850, J2900, and Intel® Celeron® processor N2900-series, N2800-series, J1800-series, J1750 are referred to as “processor” in this document, and the platform based on these processors is referred to as “Platform” in this document.

Figure 1. Processor Block Diagram





1.1 Terminology

Term	Description
ACPI	Advanced Configuration and Power Interface
Cold Reset	Full reset is when PWROK is de-asserted and all system rails except VCCRTC are powered down
CRT	Cathode Ray Tube
CRU	Clock Reset Unit
DP	Display Port
DTS	Digital Thermal Sensor
EIOB	Electronic In/Out Board
EMI	Electro Magnetic Interference
eDP	embedded Display Port
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. HDMI transmits all Advanced Television Systems Committee (ATSC) HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details available at http://www.hdmi.org/).
IGD	Internal Graphics Unit
Intel® TXE	Intel® Trusted Execution Engine
LCD	Liquid Crystal Display
MPEG	Moving Picture Experts Group
MSI	Message Signaled Interrupt. MSI is a transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
MSR	Model Specific Register, as the name implies, is model-specific and may change from processor model number (n) to processor model number (n+1). An MSR is accessed by setting ECX to the register number and executing either the RDMSR or WRMSR instruction. The RDMSR instruction will place the 64 bits of the MSR in the EDX: EAX register pair. The WRMSR writes the contents of the EDX: EAX register pair into the MSR.
PCIe*	PCI Express* (PCIe*) is a high-speed serial interface. The PCIe* configuration is software-compatible with the existing PCI specifications.
PWM	Pulse Width Modulation
Rank	A unit of DRAM corresponding to the set of SDRAM devices that are accessed in parallel for a given transaction. For a 64-bit wide data bus using 8-bit (x8) wide SDRAM devices, a rank would be eight devices. Multiple ranks can be added to increase capacity without widening the data bus, at the cost of additional electrical loading.
SCI	System Control Interrupt. SCI is used in the ACPI protocol.
SDRAM	Synchronous Dynamic Random Access Memory
SERR	System Error. SERR is an indication that an unrecoverable error has occurred on an I/O bus.
SMC	System Management Controller or External Controller refers to a separate system management controller that handles reset sequences, sleep state transitions, and other system management tasks.
SMI	System Management Interrupt is used to indicate any of several system conditions (such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity).
TMDS	Transition-Minimized Differential Signaling. TMDS is a serial signaling interface used in DVI and HDMI to send visual data to a display. TMDS is based on low-voltage differential signaling with 8/10b encoding for DC balancing.
VCO	Voltage Controlled Oscillator
Warm Reset	Warm reset is a reset of the Processor without removing power (internal only reset for Processors).

1.2 Feature Overview

All features subject to software availability.

Note: SIO (SPI, HSUART, PWM), and LPE interfaces are not planned to be supported by this processor on Windows*8 platform.

1.2.1 Processor Core

See Chapter 10, "Processor Core" for more details.

- Dual or Quad-core processor
- Up to four IA-compatible low-power Intel® processor cores
  - — One thread per core
- Two-wide instruction decode, out of order execution
- On-die, 32 KB 8-way L1 instruction cache and 24 KB 6-way L1 data cache per core
- On-die, 1 MB, 16-way L2 cache, shared per two cores
- 36-bit physical address, 48-bit linear address size support
- Supported C-states: C0, C1, C6, C7
- Supports Intel® Virtualization Technology (Intel® VT-x)

1.2.2 System Memory Controller

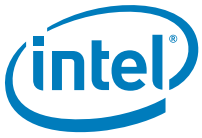
See Chapter , "System Memory Controller" for more details.

- Supports up to two channels of DDR3L
- 64 bit data bus for each channel
- Supports x8 and x16 DDR3L SDRAM device data widths
- Supports DDR3L with 1066 or 1333 MT/s data rates
  - — Total memory bandwidth supported is 8.5 GB/s (for 1066 MT/s single channel) scalable to 21.3GB/s (for 1333 MT/s dual channel)
- Supports different physical mappings of bank addresses to optimize performance
- Out-of-order request processing to increase performance
- Aggressive power management to reduce power consumption
- Proactive page closing policies to close unused pages

1.2.3 Display Controller

See Chapter 12, "Graphics, Video, and Display" for more details.

- Support 2 DDI ports to enable eDP 1.3, DP 1.1a, DVI, or HDMI 1.4a
- Support 2 panel power sequence for 2 eDP ports



- Support Audio on DP and HDMI
- Supports Intel® Display Power Saving Technology (DPST) 6.0, Panel Self Refresh (PSR) and Display Refresh Rate Switching Technology (DRRS)
- Supports one VGA port

1.2.4 Graphics and Media Engine

See Chapter 12, "Graphics, Video, and Display" for more details.

- Intel's 7th generation (Gen 7) graphics and media encode/decode engine
- VED video decoder in addition to Gen 7 Media decoder
- Supports DX*11, OpenGL 3.0 (OGL 3.0), OpenCL 1.2 (OCL 1.2), OpenGLES 2.0 (OGLES 2.0)
- GPU shader is capable of up to 8 gigaflops
- 4x anti-aliasing
- Full HW acceleration for decode of H.264, MPEG2, MVC, VC-1, VP8, MJPEG
- Full HW acceleration for encode of H.264, MPEG2, MVC
- Supports 2.0 Stereoscopic 3D Stretch
- Polyphase 8 tap scaling
- HD HQV

1.2.5 Power Management

See Chapter 6, "Power Management" for more details.

- ACPI 5.0 support
- Processor states: C0-C7
- Display device states: D0, D3
- Graphics device states: D0, D3
- System sleep states: S0, S3, S4, S5
- Dynamic I/O power reductions (disabling sense amps on input buffers, tri-stating output buffers)
- Conditional memory self-refresh during C2 (C2–C7 for select SKUs)
- Active power-down of display links
- Downloadable power management firmware

1.2.6 PCI Express*

The processor has four PCI Express* lanes and up to four PCI Express root ports, each supporting the PCI Express Base specification Rev 2.0 at a maximum of 5 Gbit/s data transfer rate. The root port configurations are flexible and can be configured to be (4) x1, (2) x2's, (1) x2 plus (2) x1's, and (1) x4.

See Chapter 18, "PCI Express* 2.0" for more details.

1.2.7 SATA

See Chapter 13, "Serial ATA (SATA)" for more details.

- Two (2) SATA Revision 2.0 ports (eSATA capable)
- Legacy IDE (including IRQ)/Native IDE/AHCI appearance to the operating system
- Partial/Slumber power management modes with wake
- Capable of 3 Gbit/s transfer rate
- Supports RunTime D3

1.2.8 USB xHCI Controller

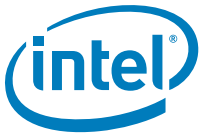
See Chapter 14, "USB Host Controller Interfaces (xHCI, EHCI)" for more details.

- Supports USB 3.0/2.0/1.1
- Implements xHCI software host controller interface
- One USB 3.0 Super Speed (SS) port
- Four ports multiplexed with EHCI controller that are High-Speed/Full-Speed (HS/FS)

1.2.9 USB 2.0 EHCI Controller

See Chapter 14, "USB Host Controller Interfaces (xHCI, EHCI)" for more details.

- Internal Rate Matching Hub to support USB 1.1 to 2.0 devices
- Four Ports multiplexed with xHCI controller
- Enhanced EHCI descriptor caching



1.2.10 Audio Controllers

1.2.10.1 Low Power Engine (LPE) Audio

LPE is a complete audio solution based on an internal audio processing engine, which includes three I^2S output ports. See Chapter 16, "Low Power Engine (LPE) for Audio (I^2S)" for Audio (I^2S)" for more details.

LPE supports:

- I^2S and DDI with dedicated DMA
- MP3, AAC, AC3/DD+, WMA9, PCM (WAV)

Note: Codecs supported depend on software and may be different.

Note: LPE is supported on selected processor SKUs.

1.2.10.2 Intel® High Definition Audio (Intel® HD Audio)

See Chapter 15, "Intel® High Definition Audio (Intel® HD Audio)" for more details.

- Four in plus four out streams (Only 3 used)
- One stream for each DDI, available for HDMI and DP
- No wake on audio (modem) support

1.2.11 Intel® Trusted Execution Engine (Intel® TXE)

The Intel TXE system contains a security engine and additional hardware security features that enable a secure and robust platform.

See Chapter 17, "Intel® Trusted Execution Engine (Intel® TXE)" for more details.

Security features include:

- Isolated execution environment for crypto operations (SKU-enabled)
- Supports secure boot – with customer programmable keys to secure code

Note: The SoC requires TXE firmware in the PCU SPI flash image to function.

1.2.12 Platform Control Unit (PCU)

The platform controller unit is a collection of HW blocks, including SMBus, UART, debug/boot SPI, and Intel legacy block (iLB), that are critical to implement a Windows* compatible platform. See Chapter 19, "Platform Controller Unit (PCU) Overview" for links to more information about each interface.

Key PCU features include:

- SMBus Host controller – supports SMBus 2.0 specification

- Universal Asynchronous Receiver/Transmitter (UART) with COM1 interface
- A Serial Peripheral Interface (SPI) for Flash only – stores boot FW and system configuration data
- Intel Legacy Block (iLB) supports legacy PC platform features
  - RTC, Interrupts, Timers, General Purpose I/Os (GPIO), and Peripheral interface (LPC for TPM) blocks.

1.2.13 Package

This processor is packaged in a Flip-Chip Ball Grid Array (FCBGA) package with 1170 solder balls with 0.593 mm (minimum) ball pitch. The package dimensions are 25 mm x 27 mm. See Chapter 9, "Package Information" for more details.

1.2.14 SKU List

The processor SKUs are listed in the following table.

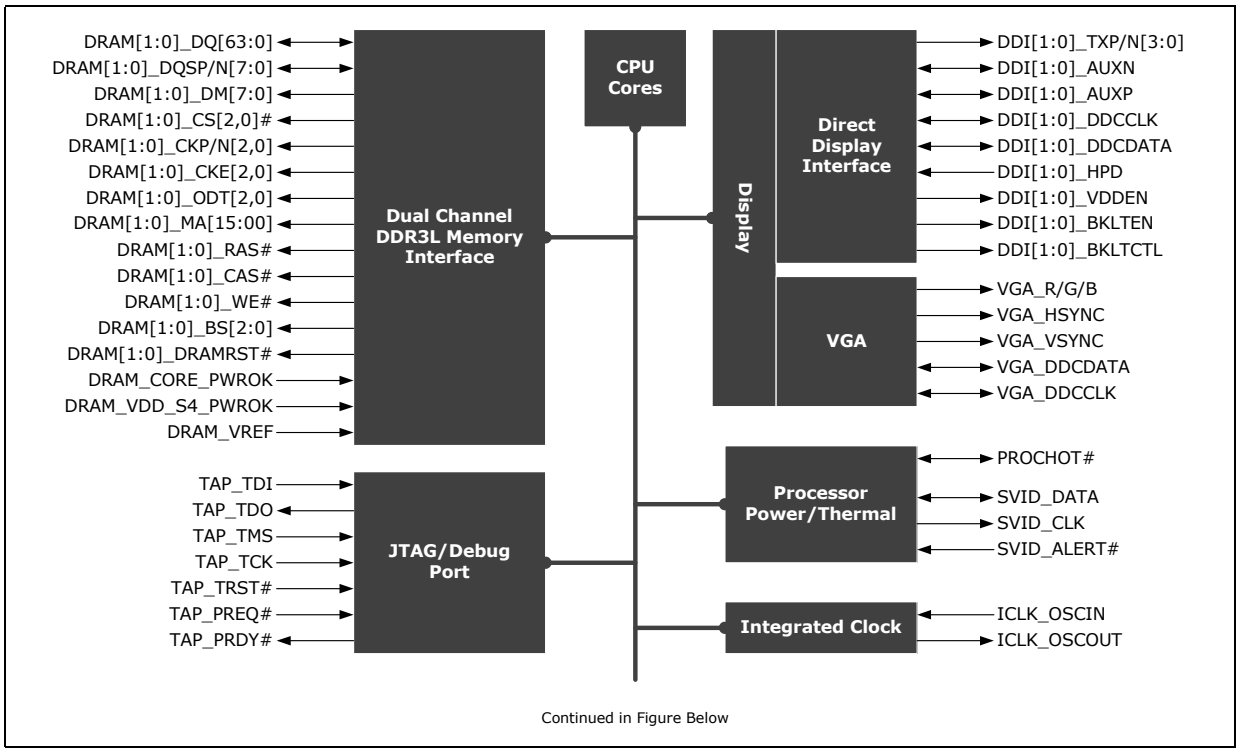
Table 1. Processor SKUs

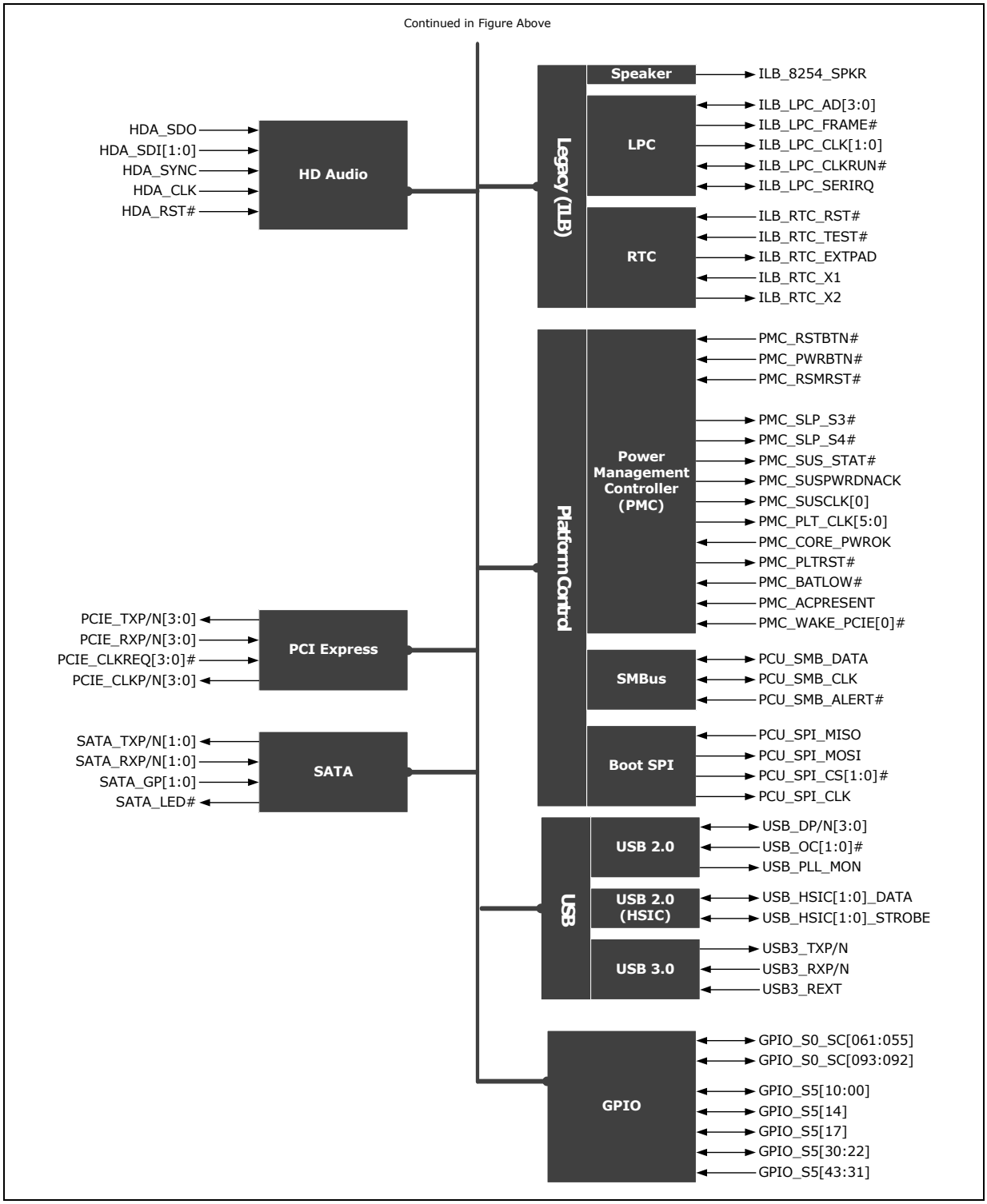
Processor Number	CPU	TDP (SDP) (W)	Core LFM (MHz)/ HFM (GHz)	Tj (°C)	GFX Normal / Burst (MHz)	DDR (MT/s)
N3540	4	7.5 (4.5)	500 / 2.66	100	313 / 896	1333
N3530	4	7.5 (4.5)	500 / 2.17	100	313 / 896	1333
N3510	4	7.5 (4.5)	500 / 2.00	100	313 / 750	1333
N2940	4	7.5 (4.5)	500 / 2.25	100	313 / 854	1333
N2930	4	7.5 (4.5)	500 / 183	100	313 / 854	1333
N2910	4	7.5 (4.5)	533 / 1.60	100	311 / 756	1066
N2840	2	7.5 (4.5)	500 / 2.58	100	313 / 792	1333
N2830	2	7.5 (4.5)	500 / 2.17	100	313 / 750	1333
N2810	2	7.5 (4.5)	533 / 2.00	100	311 / 756	1066
N2808	2	4.5 (3.0)	500 / 2.25	100	313 / 792	1333
N2807	2	4.3 (3.0)	500 / 1.58	80	313 / 750	1333
N2805	2	4.3 (2.5)	533 / 1.46	80	311 / 667	1066
J2850	4	10	1333 / 2.41	100	688 / 854	1333
J1850	4	10	500 / 2.00	100	688 / 792	1333
J1750	2	10	500 / 2.41	100	688 / 750	1333
J2900	4	10	1333 / 2.41-2.67	105	688 / 896	1333
J1900	4	10	1333 / 2.00-2.42	105	688 / 854	1333
J1800	2	10	1333 / 2.41-2.58	105	688 / 792	1333

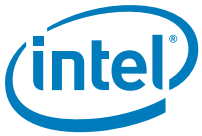
§

2 Physical Interfaces

Many interfaces contain physical pins. These groups of pins make up the physical interfaces. Because of the large number of interfaces and the small size of the package, some interfaces share pins with GPIOs, while others use dedicated physical pins. This chapter summarizes the physical interfaces, including the diversity in GPIO multiplexing options.




Continued in Figure Above
HDA_SDO
HDA_SDI[1:0]
HDA_SYNC
HDA_CLK
HDA_RST#
HD Audio
PCIE_TXP/N[3:0]
PCIE_RXP/N[3:0]
PCIE_CLKREQ[3:0]#
PCIE_CLKP/N[3:0]
PCI Express
SATA_TXP/N[1:0]
SATA_RXP/N[1:0]
SATA_GP[1:0]
SATA_LED#
SATA
Legacy (ILB)
Speaker
ILB_8254_SPKR
LPC
ILB_LPC_AD[3:0]
ILB_LPC_FRAME#
ILB_LPC_CLK[1:0]
ILB_LPC_CLKRUN#
ILB_LPC_SERIRQ
RTC
ILB_RTC_RST#
ILB_RTC_TEST#
ILB_RTC_EXTPAD
ILB_RTC_X1
ILB_RTC_X2
Platform Control
Power Management Controller (PMC)
PMC_RSTBTN#
PMC_PWRBTN#
PMC_RSMRST#
PMC_SLP_S3#
PMC_SLP_S4#
PMC_SUS_STAT#
PMC_SUSPWRDNACK
PMC_SUSCLK[0]
PMC_PLT_CLK[5:0]
PMC_CORE_PWROK
PMC_PLTRST#
PMC_BATLOW#
PMC_ACPRESENT
PMC_WAKE_PCIE[0]#
SMBus
PCU_SMB_DATA
PCU_SMB_CLK
PCU_SMB_ALERT#
Boot SPI
PCU_SPI_MISO
PCU_SPI_MOSI
PCU_SPI_CS[1:0]#
PCU_SPI_CLK
USB
USB 2.0
USB_DP/N[3:0]
USB_OC[1:0]#
USB_PLL_MON
USB 2.0 (HSIC)
USB_HSIC[1:0]_DATA
USB_HSIC[1:0]_STROBE
USB 3.0
USB3_TXP/N
USB3_RXP/N
USB3_REXT
GPIO
GPIO_S0_SC[061:055]
GPIO_S0_SC[093:092]
GPIO_S5[10:00]
GPIO_S5[14]
GPIO_S5[17]
GPIO_S5[30:22]
GPIO_S5[43:31]



2.1 Pin States Through Reset

This chapter describes the states of each signal before, during, and directly after reset. Additionally, Some signals have internal pull-up/pull-down termination resistors; the values are also provided. All signals with the "†" symbol are multiplexed and may not be available without configuration. See Section 2.22, "Configurable IO – GPIO Multiplexing" on page 42.

Table 2. Platform Power Well Definitions

Power Type	Power Well Description
V1P05S	1.05 V rail. On in S0 only.
V1P0A	1.0 V rail. On in S0 through S4/5.
V1P0S	1.0 V rail. On in S0 only.
V1P0Sx	1.0 V rail. On in S0 only.
V1P24A	1.24 V rail. On in S0 through S4/5.
V1P24S	1.24 V rail. On in S0 only.
V1P24Sx	1.24 V rail. On in S0 only.
V1P35U	1.35 V rail. On in S0 through S3.
V1P8A	1.8 V rail. On in S0 through S4/5.
V1P35S	1.35 V rail. On in S0
V1P8S	1.8 V rail. On in S0 only.
V3P3A	3.3 V rail. On in S0 through S4/5.
VAUD	1.5 V rail for HD Audio. On in S0 only.
VCC	Variable core rail. On in S0 only.
VLPC	1.8 or 3.3 V rail for LPC. On in S0 only.
VNN	Variable rail. On in S0 only.
VPCIESATA	1.0 V rail for PCIe* and SATA. On in S0 only.
VRTC	RTC voltage rail. On in S0 through G3.
VSDIO	1.8 or 3.3 V rail for SD3. On in S0 only.
VSFR	1.35 V rail for internal PLLs. On in S0 only.
VUSB2	3.3 V rail. On in S0 through S4/5.

Table 3. Default Buffer State Definitions (Sheet 1 of 2)

Buffer State	Description
High-Z	The processor places this output in a high-impedance state. For inputs, external drivers are not expected.
Do Not Care	The state of the input (driven or tri-stated) does not affect the processor. For outputs, it is assumed that the output buffer is in a high-impedance state.
V_{OH}	The processor drives this signal high with a termination of 50 Ω.
V_{OL}	The processor drives this signal low with a termination of 50 Ω.
Unknown	The Processor drives or expects an indeterminate value.
V_{IH}	The processor expects/requires the signal to be driven high.
V_{IL}	The processor expects/requires the signal to be driven low.

Table 3. Default Buffer State Definitions (Sheet 2 of 2)

Buffer State	Description
Pull-up	This signal is pulled high by a pull-up resistor (internal value specified in "Term" column).
Pull-down	This signal is pulled low by a pull-down resistor (internal value specified in "Term" column).
Running/T	The clock is toggling, or the signal is transitioning.
Off	The power plane for this signal is powered down. The Processor does not drive outputs, and inputs should not be driven to the Processor. (VSS on output)

2.2 System Memory Controller Interface Signals

See Chapter , "System Memory Controller" for more details.

Table 4. DDR3L System Memory Signals (Sheet 1 of 2)

				Default Buffer State			
Signal Name	Dir	Term	Plat. Power	S4/S5	S3	Reset	Enter S0
DRAM0_CKP[2,0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM0_CKN[2,0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM0_CS#[2,0]	O	-	V1P35U	Off	V_{OH}	V_{OH}	V_{OH}
DRAM0_CKE[2,0]	O	-	V1P35U	Off	V_{OL}	V_{OL}	V_{OL}
DRAM0_CAS#	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM0_RAS#	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM0_WE#	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM0_BS[2:0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM0_DRAMRST#	O	-	V1P35U	Off	-	-	-
DRAM0_ODT[2,0]	O	-	V1P35U	Off	V_{OL}	V_{OL}	V_{OL}
DRAM0_DQ[63:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM0_DM[7:0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM0_DQSP[7:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM0_DQSN[7:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM1_CKP[2,0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM1_CKN[2,0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM1_CKE[2,0]	O	-	V1P35U	Off	V_{OL}	V_{OL}	V_{OL}
DRAM1_CS#[2,0]	O	-	V1P35U	Off	V_{OH}	V_{OH}	V_{OH}
DRAM1_CAS#	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM1_RAS#	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM1_WE#	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM1_BS[2:0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM1_DRAMRST#	O	-	V1P35U	Off	-	-	-
DRAM1_ODT[2,0]	O	-	V1P35U	Off	V_{OL}	V_{OL}	V_{OL}
DRAM1_DQ[63:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM1_DM[7:0]	O	-	V1P35U	Off	High-Z	High-Z	High-Z

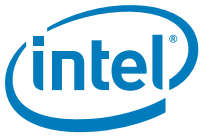


Table 4. DDR3L System Memory Signals (Sheet 2 of 2)

				Default Buffer State			
Signal Name	**Dir**	**Term**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
DRAM1_DQSP[7:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM1_DQSN[7:0]	I/O	-	V1P35U	Off	High-Z	High-Z	High-Z
DRAM_VDD_S4_PWROK	I	-	V1P35U	V_{IL}	V_{IH}	Unknown	V_{IH}
DRAM_CORE_PWROK	I	-	V1P35U	V_{IL}	V_{IL}	Unknown	V_{IH}
DRAM_VREF	I	-	V1P35U				
DRAM_RCOMP[2:0]	-	-	V1P35U				

2.3 PCI Express* 2.0 Interface Signals

See Chapter 18, "PCI Express* 2.0" for more details.

Table 5. PCI Express* 2.0 Interface Signals

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
PCIE_TXP[3:0]	O	50	VPCIESATA	Off	Off	V_{OL}	V_{OL}
PCIE_TXN[3:0]	O	50	VPCIESATA	Off	Off	V_{OL}	V_{OL}
PCIE_RXP[3:0]	I	50	VPCIESATA	Off	Off	High-Z	High-Z
PCIE_RXN[3:0]	I	50	VPCIESATA	Off	Off	High-Z	High-Z
PCIE_CLKP[3:0]	O	-	V1P0S	Off	Off	Running/ V_{IL}	Running/ V_{IL}
PCIE_CLKN[3:0]	O	-	V1P0S	Off	Off	Running/ V_{IL}	Running/ V_{IL}
PCIE_CLKREQ[3:0]#†	I	20k(H)	V1P8S	Off	Off	Pull_up	Pull_up
PCIE_RCOMP_P/N	-	-					

NOTE: All signals with the "†" symbol are multiplexed and may not be available without configuration.

2.4 USB 2.0 Host (EHCI/xHCI) Interface Signals

See Chapter 14, "USB Host Controller Interfaces (xHCI, EHCI)" for more details.

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
USB_DN[3:0]	I/O	-	VUSB2				
USB_DP[3:0]	I/O	-	VUSB2				
USB_OC[1:0]#†	I	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
USB_RCOMPI	I	-	-				
USB_RCOMPO	O	-	-				

NOTE: All signals with the "†" symbol are multiplexed and may not be available without configuration.

2.5 USB 2.0 HSIC Interface Signals

See Chapter 14, "USB Host Controller Interfaces (xHCI, EHCI)" for more details.

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
USB_HSIC0_DATA	I/O	-	V1P24A	Running	Running	V_{OH}	Running
USB_HSIC0_STROBE	I/O	-	V1P24A	V_{OH}			
USB_HSIC1_DATA	I/O	-	V1P24A			V_{OH}	
USB_HSIC1_STROBE	I/O	-	V1P24A	V_{OH}			
USB_HSIC_RCOMP	I	-	V1P24A			V_{OH}	

2.6 USB 3.0 (xHCI) Host Interface Signals

See Chapter 14, "USB Host Controller Interfaces (xHCI, EHCI)" for more details.

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
USB3_TXN[0]	O	-	V1P0A				
USB3_TXP[0]	O	-	V1P0A				
USB3_RXN[0]	I	-	V1P0A				
USB3_RXP[0]	I	-	V1P0A				
USB3_REXT[0]	I	-	V1P0A	V_{OL}	V_{OL}	V_{OH}	V_{OH}

2.7 Serial ATA (SATA) 2.0 Interface Signals

See Chapter 13, "Serial ATA (SATA)" for more details.

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
SATA_TXP[1:0]	O		VPCIESATA	Off	Off		
SATA_TXN[1:0]	O		VPCIESATA	Off	Off		
SATA_RXP[1:0]	I		VPCIESATA	Off	Off		
SATA_RXN[1:0]	I		VPCIESATA	Off	Off		

Signal Name	Dir	Term (Ω)	Plat. Power	Default Buffer State			
				S4/S5	S3	Reset	Enter S0
SATA_LED#†	O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up
SATA_GP[1:0]†	I	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
SATA_DEVSLP[1:0]†	O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
SATA_RCOMP_P/N	-	-	1.0 V				

NOTE: All signals with the "†" symbol are multiplexed and may not be available without configuration.

2.8 Integrated Clock Interface Signals

See Chapter 5, "Integrated Clock" for more details.

Signal Name	Dir	Term (Ω)	Plat. Power	Default Buffer State			
				S4/S5	S3	Reset	Enter S0
ICLK_OSCIN	I	-		Off	Off	Running	Running
ICLK_OSCOUT	O	-		Off	Off	Running	Running
ICLK_ICOMP	-	-		Off	Off		
ICLK_RCOMP	-	-		Off	Off		
ICLK_DRAM_TERM[1:0]	-	-	-	Pull-down	Pull-down	Pull-down	Pull-down
ICLK_USB_TERM[1:0]	-	-	-	Pull-down	Pull-down	Pull-down	Pull-down

2.9 Display – Digital Display Interface (DDI) Signals

See Chapter 12, "Graphics, Video, and Display" for more details.

Table 10. Digital Display Interface Signals

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
DDI0_TXP[3:0]	O		V1P0Sx	Off	Off		
DDI0_TXN[3:0]	O		V1P0Sx	Off	Off		
DDI0_AUXP	I/O		V1P0Sx	Off	Off		
DDI0_AUXN	I/O		V1P0Sx	Off	Off		
DDI0_BKLTCTL†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
DDI0_BKLTEN†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
DDI0_DDCCLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up
DDI0_DDCDATA†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
DDI0_HPD†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
DDI0_VDDEN†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
DDI_RCOMP_P/N	-	-	V1P0Sx				
DDI1_TXP[3:0]	O		V1P0Sx	Off	Off		
DDI1_TXN[3:0]	O		V1P0Sx	Off	Off		
DDI1_AUXP	I/O		V1P0Sx	Off	Off		
DDI1_AUXN	I/O		V1P0Sx	Off	Off		
DDI1_BKLTCTL†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
DDI1_BKLTEN†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
DDI1_DDCCLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up
DDI1_DDCDATA†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
DDI1_HPD†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
DDI1_VDDEN†	I/O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down

NOTE: All signals with the "†" symbol are multiplexed and may not be available without configuration.

2.10 Display – VGA Interface Signals

See Chapter 12, "Graphics, Video, and Display" for more details.

					Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**Type**	**S4/S5**	**S3**	**Reset**	**Enter S0**
VGA_RED	O		VVGA_GPIO		Off	Off	High-Z	
VGA_GREEN	O		VVGA_GPIO		Off	Off	High-Z	
VGA_BLUE	O		VVGA_GPIO		Off	Off	High-Z	
VGA_IREF					Off	Off	V_{OL}	
VGA_IRTN					Off	Off	High-Z	
VGA_HSYNC	O		VVGA_GPIO		Off	Off	V_{OL}	
VGA_VSYNC	O		VVGA_GPIO		Off	Off	V_{OL}	
VGA_DDCCLK	O		VVGA_GPIO		Off	Off	High-Z	
VGA_DDCDATA	I/O		VVGA_GPIO		Off	Off	High-Z	

2.11 Intel® High Definition Audio Interface Signals

See Chapter 15, "Intel® High Definition Audio (Intel® HD Audio)" for more details.

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
HDA_SDO†	O	20k(L)	VAUD	Off	Off	Pull-down	Pull-down
HDA_SDI[1:0]†	I	20k(L)	VAUD	Off	Off	Pull-down	Pull-down
HDA_CLK†	O	20k(L)	VAUD	Off	Off	Pull-down	Pull-down
HDA_RST#†	O	20k(L)	VAUD	Off	Off	Pull-down	Pull-down
HDA_SYNC†	O	20k(L)	VAUD	Off	Off	Pull-down	Pull-down

NOTE: All signals with the "†" symbol are multiplexed and may not be available without configuration.

2.12 SPCU – iLB – Real Time Clock (RTC) Interface Signals

See Chapter 26, "PCU – iLB – Real Time Clock (RTC)" for more details.

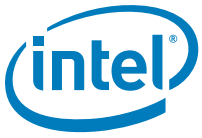
				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
ILB_RTC_X1	I	-	VRTC	Running	Running	Running	Running
ILB_RTC_X2	O	-	VRTC	Running	Running	Running	Running
ILB_RTC_RST#	I	-	VRTC	V_{IH}	V_{IH}	V_{IH}	V_{IH}
ILB_RTC_TEST#	I	-	VRTC	V_{IH}	V_{IH}	V_{IH}	V_{IH}
ILB_RTC_EXTPAD	O	-	VRTC				

2.13 PCU – iLB – Low Pin Count (LPC) Bridge Interface Signals

See Chapter 25, "PCU – iLB – Low Pin Count (LPC) Bridge" for more details.

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
ILB_LPC_AD[3:0]†	I/O	20k(H)	VLPC	Off	Off	Pull-up	Running
ILB_LPC_FRAME#†	I/O	20k(H)	VLPC	Off	Off	V_{OH}	Running
ILB_LPC_SERIRQ†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Running
ILB_LPC_CLKRUN#†	I/O	20k(H)	VLPC	Off	Off	Pull-up	Running
ILB_LPC_CLK[1:0]†	I/O	20k(L)	VLPC	Off	Off	V_{OL}	Running
LPC_RCOMP	-		VLPC				

NOTE: All signals with the "†" symbol are multiplexed and may not be available without configuration.



2.14 PCU – Serial Peripheral Interface (SPI) Signals

See Chapter 21, "PCU – Serial Peripheral Interface (SPI)" for more details.

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
PCU_SPI_CLK	O	-	V1P8A	Pull-up	Pull-up	Pull-up	Running
PCU_SPI_CS[0]#	O	-	V1P8A	Pull-up	Pull-up	Pull-up	Running
PCU_SPI_CS[1]#†	O	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Running
PCU_SPI_MOSI	I/O	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
PCU_SPI_MISO	I	20k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up

NOTE: All signals with the "†" symbol are multiplexed and may not be available without configuration.

2.15 PCU – System Management Bus (SMBus) Interface Signals

See Chapter 23, "PCU – System Management Bus (SMBus)" for more details.

Table 14. PCU - System Management Bus (SMBus) Interface Signals

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
PCU_SMB_CLK†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up
PCU_SMB_DATA†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up
PCU_SMB_ALERT#†	I/O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up

2.16 PCU – Power Management Controller (PMC) Interface Signals

See Chapter 20, "PCU – Power Management Controller (PMC)" for more details.

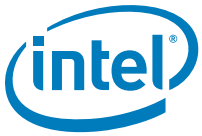
				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
PMC_PLTRST#	O	-	V1P8A	Off/V_{OL}	V_{OL}	V_{OL}->V_{OH}	V_{OH}
PMC_PWRBTN#†	I	20k(H)	V1P8A	Off/Pull-up	Pull-up	Pull-up	Pull-up
PMC_RSTBTN#	I	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up
PMC_SUSPWRDNACK†	O	-	V1P8A	V_{OH}/V_{OL}	V_{OH}/V_{OL}	V_{OH}	V_{OH}/V_{OL}
PMC_SUS_STAT#†	O	-	V1P8A	V_{OL}	V_{OL}	V_{OL}	V_{OH}
PMC_SUSCLK[0]†	O	-	V1P8A	Off/Running	Running	Running	Running
PMC_SUSCLK[3:1]†	O	-					
PMC_SLP_S3#	O	-	V1P8A	Off/V_{OL}	V_{OL}	V_{OH}	V_{OH}
PMC_SLP_S4#	O	-	V1P8A	Off/V_{OL}	V_{OH}	V_{OH}	V_{OH}
PMC_WAKE_PCIE[0]#	I	20k(H)	V1P8A	Off/Pull-up	Pull-up	Pull-up	Pull-up
PMC_WAKE_PCIE[3:1]#†	I	20k(H)	V1P8A	Off/Pull-up	Pull-up	Pull-up	Pull-up
PMC_ACPRESENT	I	20k(L)	V1P8A	Off/High-Z	Pull-down	Pull-down	Pull-down
PMC_BATLOW#	I	20k(H)	V1P8A	Off/Pull-up	Pull-up	Pull-up	Pull-up
PMC_CORE_PWROK	I		VRTC	V_{IL}	V_{IL}	V_{IL}	V_{IH}
PMC_RSMRST#	I		VRTC	V_{IH}	V_{IH}	V_{IH}	V_{IH}

NOTE: All signals with the "†" symbol are multiplexed and may not be available without configuration.

2.17 JTAG and Debug Interface Signals

Table 17. JTAG and Debug Interface Signals

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
TAP_TCK	I	2k(L)	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
TAP_TDI	I	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
TAP_TDO	O	-	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
TAP_TMS	I	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
TAP_TRST#	I	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
TAP_PRDY#	O	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
TAP_PREQ#	I	2k(H)	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up



2.18 Miscellaneous Signals

Table 19. Miscellaneous Signals and Clocks

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
SVID_DATA	I/O	2k(H)	V1P0S	Off	Off	Pull-up	Pull-up
SVID_CLK	O	2k(H)	V1P0S	Off	Off	Pull-up	Pull-up
SVID_ALERT#	I	2k(H)	V1P0S	Off	Off	Pull-up	Pull-up
PROCHOT#	I/O	2k(H)	V1P0S	Off	Off	Pull-up	Pull-up
ILB_8254_SPKR†	O	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up
ILB_NMI†	I	20k(H)	V1P8S	Off	Off	Pull-up	Pull-up
PMC_PLT_CLK[5:0]†	O	20k(L)	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_RCOMP	-	-	V1P8S	Off	Off	Active	Active

NOTE: All signals with the "†" symbol are multiplexed and may not be available without configuration.
NOTE: GPIO_RCOMP provides compensation for the following pins: GPIO_S5[10], PMC_SUSPWRDNACK PMC_SUSCLK[0], PMC_SLP_S4#, PMC_SLP_S3#, GPIO_S5[14], PMC_ACPRESENT, PMC_WAKE_PCIE[0]#, PMC_BATLOW#, PMC_PWRBTN#, PMC_PLTRST#, GPIO_S5[17], PMC_SUS_STAT#, USB_OC[1:0]#, GPIO_S5[09:00], GPIO_S5[30:22], TAP_TCK TAP_TRST#, TAP_TMS, TAP_TDI, TAP_TDO, TAP_PRDY#, TAP_PREQ#

2.19 GPIO Signals

Most GPIOs are configurable using multiplexors.

Table 21. GPIO Signals (Sheet 1 of 5)

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
GPIO_S0_SC[000]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[001]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[002]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[003]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[004]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[005]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[006]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[007]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[008]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[009]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[010]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[011]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[012]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[013]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[014]†	I/O	20k,L	VAUD	Off	Off	Pull-down	Pull-down

Table 21. GPIO Signals (Sheet 2 of 5)

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
GPIO_S0_SC[015]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[016]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[017]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[018]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[019]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[020]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[021]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[022]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[023]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[024]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[025]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[026]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[027]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[028]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[029]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[030]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[031]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[032]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[033]†	I/O	20k,L	VSDIO	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[034]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[035]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[036]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[037]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[038]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[039]†	I/O	20k,H	VSDIO	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[040]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[041]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[042]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[043]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[044]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[045]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[046]†	I/O	20k,H	VLPC	Off	Off	1	1
GPIO_S0_SC[047]†	I/O	20k,L	VLPC	Off	Off	0	00
GPIO_S0_SC[048]†	I/O	20k,L	VLPC	Off	Off	0	0
GPIO_S0_SC[049]†	I/O	20k,H	VLPC	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[050]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[051]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up

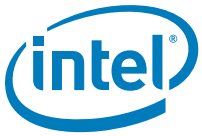


Table 21. GPIO Signals (Sheet 3 of 5)

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
GPIO_S0_SC[052]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[053]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[054]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[055]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[056]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[057]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[058]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[059]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[060]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[061]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[062]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[063]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[064]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[065]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[066]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[067]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[068]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[069]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[070]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[071]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[072]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[073]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[074]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[075]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[076]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[077]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[078]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[079]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[080]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[081]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[082]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[083]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[084]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[085]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[086]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[087]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[088]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up

Table 21. GPIO Signals (Sheet 4 of 5)

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
GPIO_S0_SC[089]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[090]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[091]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[092]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[093]†	I/O	20k,H	V1P8S	Off	Off	Pull-up	Pull-up
GPIO_S0_SC[094]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[095]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[096]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[097]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[098]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[099]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[100]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S0_SC[101]†	I/O	20k,L	V1P8S	Off	Off	Pull-down	Pull-down
GPIO_S5[00]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[01]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[02]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[03]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[04]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[05]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[06]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[07]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[08]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[09]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[10]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[11]†	I/O	-	V1P8A	0/1	0/1	0	0/1
GPIO_S5[12]†	I/O	-	V1P8A	T	T	T	T
GPIO_S5[13]†	I/O	-	V1P8A	0	0	0	0/1
GPIO_S5[14]†	I/O	-	V1P8A	0	0	0	0/1
GPIO_S5[15]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[16]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[17]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[18]†	I/O	-	V1P8A	0	0	0	1
GPIO_S5[19]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[20]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[21]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[22]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[23]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down

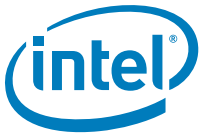


Table 21. GPIO Signals (Sheet 5 of 5)

				Default Buffer State			
Signal Name	**Dir**	**Term (Ω)**	**Plat. Power**	**S4/S5**	**S3**	**Reset**	**Enter S0**
GPIO_S5[24]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[25]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[26]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[27]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[28]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[29]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[30]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[31]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[32]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[33]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[34]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[35]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[36]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[37]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[38]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[39]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[40]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[41]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down
GPIO_S5[42]†	I/O	20k,H	V1P8A	Pull-up	Pull-up	Pull-up	Pull-up
GPIO_S5[43]†	I/O	20k,L	V1P8A	Pull-down	Pull-down	Pull-down	Pull-down

2.20 Power And Ground Pins

Power Rail Ball Name Format: [Function]_[Voltage]_[S-State]{_[Filter]}:

- [Function]: The Processor function associated with the power rail.
  - Such as CORE, PCIE, USB, …
- [Voltage]: The nominal voltage associated with the power rail.
  - Such as 1P05, 3P3, VCC, …
- [S-State]: The ACPI system state, from S0 to G3, when the this rail is turned off.
- [Filter]: An optional indicator that one or more power rail balls have unique filtering requirements or requirement to be uniquely identified.

Note: The Resume power well is a set of supply rails (where [S-State] = G3) that must be powered even when S3/4/5 states are not used. The "Resume Well" is also referred to as the "Suspend Power Well", "Always on/SUS", "SUS power", or "SUS well".

Table 22. Power and Ground Pins (Sheet 1 of 2)

Power Rails	Platform Power	Nominal Voltage	First Off State
CORE_V1P05_S3	V1P05S	1.05 V	S3
CORE_VCC_S3	VCC	Variable	S3
CORE_VCC_SENSE	-	-	-
CORE_VSS_SENSE	-	-	-
DDI_V1P0_S3	V1P0Sx	1.0 V	S3
DRAM_V1P0_S3	V1P0Sx	1.0 V	S3
DRAM_V1P35_S3_F1	VSFR	1.35 V	S3
DRAM_VDD_S4	V1P35U	1.35 V	S4
GPIO_V1P0_S3	V1P0S	1.0 V	S3
HDA_LPE_V1P5V1P8_S3	VAUD	1.5/1.8 V	S3
ICLK_V1P35_S3_F1	V1P35S	1.35 V	S3
ICLK_V1P35_S3_F2	V1P35S	1.35 V	S3
LPC_V1P8V3P3_S3	VLPC	1.8/3.3 V	S3
PCIE_SATA_V1P0_S3	VPCIESATA	1.0 V	S3
PCIE_V1P0_S3	VPCIESATA	1.0 V	S3
PCU_V1P8_G3	V1P8A	1.8 V	G3
PCU_V3P3_G3	V3P3A	3.3 V	G3
PMC_V1P8_G3	V1P8A	1.8 V	G3
RTC_VCC	VRTC	2.0-3.3	(normally battery backed)
SATA_V1P0_S3	VPCIESATA	1.0 V	S3
SD3_V1P8V3P3_S3	VSDIO	1.8/3.3 V	S3

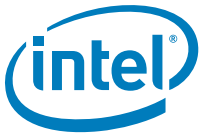


Table 22. Power and Ground Pins (Sheet 2 of 2)

Power Rails	Platform Power	Nominal Voltage	First Off State
SVID_V1P0_S3	V1P0S	1.0 V	S3
UNCORE_V1P0_G3	V1P0A	1.0 V	G3
UNCORE_V1P0_S3	V1P0Sx	1.0 V	S3
UNCORE_V1P0_S3	V1P0S	1.0 V	S3
UNCORE_V1P35_S3	VSFR	1.35 V	S3
UNCORE_V1P35_S3	VSFR	1.35 V	S3
UNCORE_V1P35_S3	VSFR	1.35 V	S3
UNCORE_V1P35_S3	VSFR	1.35 V	S3
UNCORE_V1P35_S3	VSFR	1.35 V	S3
UNCORE_V1P35_S3	VSFR	1.35 V	S3
UNCORE_V1P8_G3	V1P8A	1.8 V	G3
UNCORE_V1P8_S3	V1P8S	1.8 V	S3
UNCORE_VNN_S3	VNN	Variable	S3
UNCORE_VNN_SENSE	-	-	-
USB_HSIC_V1P24_G3*	V1P24A	1.24 V	G3
USB_V1P0_S3	V1P0S	1.0 V	S3
USB_V1P8_G3	V1P8A	1.8 V	G3
USB_V3P3_G3	VUSB2	3.3 V	G3
USB_VSSA	-	-	-
USB3_V1P0_G3	V1P0A	1.0 V	G3
VGA_V1P0_S3	V1P0S	1.0 V	S3
VGA_V1P35_S3_F1	VSFR	1.35 V	S3
VGA_V3P3_S3	VVGA_GPIO	3.3 V	S3
VSS	-	-	-
VSSA	-	-	-

Note: USB_HSIC_V1P24_G3 pin(s) can be connected to V1P0A platform rail if USB HSIC is not used.

2.21 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK. Defaults are based on internal termination.

Table 23. Straps

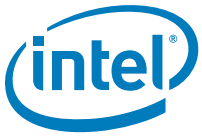
Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is unchanged 1 = Top address bit is inverted
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

2.22 Configurable IO – GPIO Multiplexing

Not all interfaces may be active at the same time. To provide flexibility, some interfaces are multiplexed with configurable IO balls. An interface's signal is selected by a function number..

Note: Configurable IO defaults to function 0 at boot. All configurable IO with GPIOs for function 0 default to input at boot.

§



3 Register Access Methods

There are six different common register access methods:

- Fixed IO Register Access
- Fixed Memory Mapped Register Access
- IO Referenced Register Access
- Memory Referenced Register Access
- PCI Configuration Register Access (Indirect - using Memory or IO registers)
- Message Bus Register Access (Indirect - using PCI Configuration Registers)

3.1 Fixed IO Register Access

Fixed IO registers are accessed by specifying the 16-bit address in a PORT IN and/or PORT OUT transaction from the processor core. This allows direct manipulation of the registers. Fixed IO registers are unmovable registers in IO space.

Table 24. Fixed IO Register Access Method Example (P80 Register)

Type: I/O Register (Size: 32 bits)	**P80:** 80h

3.2 Fixed Memory Mapped Register Access

Fixed Memory Mapped IO (MMIO) registers are accessed by specifying the 32/36-bit address in a memory transaction from the processor core. This allows direct manipulation of the registers. Fixed MMIO registers are unmovable registers in memory space.

Table 25. Fixed Memory Mapped Register Access Method Example (IDX Register)

Type: Memory Mapped I/O Register (Size: 32 bits)	**IDX:** FEC00000h

3.3 IO Referenced Register Access

IO referenced registers use programmable base address registers (BARs) to select a range of IO addresses that it will use to decode PORT IN and/or PORT OUT transactions from the processor to directly access a register. Thus, the IO BARs act as pointers to blocks of actual IO registers. To access an IO referenced register for a specific IO base address, start with that base address and add the register's offset. Example pseudo code for an IO referenced register read is shown below:

```
Register_Snapshot = IOREAD([IO_BAR]+Register_Offset)
```

Base address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other base address register types may include fixed memory registers, fixed IO registers, or message bus registers.

Table 26. Referenced IO Register Access Method Example (HSTS Register)

Type: I/O Register (Size: 8bits)	**HSTS:** [SMB_IOBAR] + 0h **SMB_IOBAR Type:** PCI Configuration Register (Size: 32 bits) **SMB_IOBAR Reference:** [B:0, D:31, F:3] + 20h

3.4 Memory Referenced Register Access

The processor uses programmable base address registers (BARs) to set a range of physical address (memory) locations that it will use to decode memory reads and writes from the processor to directly access a register. These BARs act as pointers to blocks of actual memory mapped IO (MMIO) registers. To access a memory referenced register for a specific base address, start with that base address and add the register's offset. Example pseudo code for a read is shown below:

```
Register_Snapshot = MEMREAD([Mem_BAR]+Register_Offset)
```

Base address registers are often located in the PCI configuration space and are programmable by the BIOS/OS. Other common base address register types include fixed memory registers and IO registers that point to MMIO register blocks.

Table 27. Memory Mapped Register Access Method Example (SMB_MBAR Register)

Type: Memory Mapped I/O Register (Size: 8bits)	**HSTS:** [SMB_MBAR] + 0h **SMB_MBAR Type:** PCI Configuration Register (Size: 32 bits) **SMB_MBAR Reference:** [B:0, D:31, F:3] + 10h

3.5 PCI Configuration Register Access

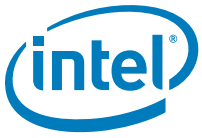
Access to PCI configuration space registers is performed through one of two different configuration access methods (CAMs):

- IO indexed – PCI CAM
- Memory mapped – PCI Enhanced CAM (ECAM)

Each PCI function has a standard PCI header consisting of 256 bytes for the IO access scheme (CAM), or 4096 bytes for the enhanced memory access method (ECAM). Invalid read accesses return binary strings of 1s.

Table 28. PCI Register Access Method Example (VID Register)

Type: PCI Configuration Register (Size: 16bits)	**VID:** [B:0, D:31, F:3] + 0h



3.5.1 PCI Configuration Access – CAM: IO Indexed Scheme

Accesses to configuration space using the IO method relies on two 32-bit IO registers:

- **CONFIG_ADDRESS** – IO Port CF8h
- **CONFIG_DATA** – IO Port CFCh

These two registers are both 32-bit registers in IO space. Using this indirect access mode, software uses CONFIG_ADDRESS (CF8h) as an index register, indicating which configuration space register to access, and CONFIG_DATA (CFCh) acts as a window to the register pointed to in CONFIG_ADDRESS. Accesses to CONFIG_ADDRESS (CF8h) are internally captured. Upon a read or write access to CONFIG_DATA (CFCh), configuration cycles will be generated to the PCI function specified by the address captured in CONFIG_ADDRESS. The format of the address is shown in the following table.

Table 29. PCI CONFIG_ADDRESS Register (IO PORT CF8h) Mapping

Field	CONFIG_ADDRESS Bits
Enable PCI Configuration Space Mapping	31
Reserved	30:24
Bus Number	23:16
Device Number	15:11
Function Number	10:08
Register/Offset Number	07:02

Note: Bit 31 of CONFIG_ADDRESS must be set for a configuration cycle to be generated.

Pseudo code for a PCI register read is shown below:

- MyCfgAddr[23:16] = bus; MyCfgAddr[15:11] = device; MyCfgAddr[10:8] = funct;
- MyCfgAddr[7:2] = dWordMask(offset); MyCfgAddr[31] = 1;
- IOWRITE(0xCF8, MyCfgAddr)
- Register_Snapshot = IOREAD(0xCFC)

3.5.2 PCI Configuration Access – ECAM: Memory Mapped Scheme

A flat, 256 MiB memory space may also be allocated to perform configuration transactions. This is enabled through the BUNIT.BECREG message bus register (Port: 3h, Register: 27h) found in the Processor Transaction Router. BUNIT.BECREG allows remapping this 256 MiB region anywhere in physical memory space. Memory accesses within the programmed MMIO range result in configuration cycles to the appropriate PCI devices specified by the memory address as shown in the following table.

Table 30. PCI Configuration Memory Bar Mapping

ECAM Memory Address Field	ECAM Memory Address Bits
Use from BAR: BUNIT.BECREG[31:28]	31:28
Bus Number	27:20
Device Number	19:15
Function Number	14:12
Register Number	11:02

Note: ECAM accesses are only possible when BUNIT.BECREG.ECENABLE (bit 0) is set.

Pseudo code for an enhanced PCI configuration register read is shown below:

- MyCfgAddr[27:20] = bus; MyCfgAddr[19:15] = device; MyCfgAddr[14:12] = funct;
- MyCfgAddr[11:2] = dw_offset; MyCfgAddr[31:28] = BECREG[31:28];
- Register_Snapshot = MEMREAD(MyCfgAddr)

3.6 Message Bus Register Access

Accesses to the message bus space is through the Processor Transaction Router's PCI configuration registers. This unit relies on three 32-bit PCI configuration registers to generate messages:

- Message Bus Control Register (MCR) – PCI[B:0,D:0,F:0] + D0h
- Message Data Register (MDR) – PCI[B:0,D:0,F:0] + D4h
- Message Control Register eXtension (MCRX) – PCI[B:0,D:0,F:0] + D8h

This indirect access mode is similar to PCI CAM. Software uses the MCR/MCRX as an index register, indicating which message bus space register to access (MCRX only when required), and MDR as the data register. Writes to the MCR trigger message bus transactions.

Writes to MCRX and MDR will be captured. Writes to MCR will generate an internal 'message bus' transaction with the opcode and target (port, offset, bytes) specified in the MCR and the captured MCRX. When a write opcode is specified in the MCR, the data that was captured by MDR is used for the write. When a data read opcode is specified in the MCR, the data will be available in the MDR register after the MCR write completes (non-posted). The format of MCR and MCRX are shown in the following tables.

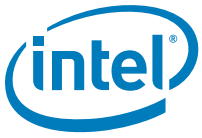


Table 31. MCR Description

Field	MBPR Bits
OpCode (typically 10h for read, 11h for write)	31:24
Port	23:16
Offset/Register	15:08
Byte Enable	07:04

Table 32. MCRX Description

Field	MBPER Bits
Offset/Register Extension. This is used for messages sent to end points that require more than 8 bits for the offset/register. These bits are a direct extension of MCR[15:8].	31:08

Most message bus registers are located in the Processor Transaction Router. The default opcode messages for those registers are as follows:

- Message 'Read Register' Opcode: 06h
- Message 'Write Register' Opcode: 07h

Registers with different opcodes will be specified as applicable. Pseudo code of a message bus register read is shown below (where ReadOp==0x06):

- MyMCR[31:24] = ReadOp; MyMCR[23:16] = port; MyMCR[15:8] = offset;
- MyMCR[7:4] = 0xf
- PCIWRITE(0, 0, 0, 0xD0, MyMCR)
- Register_Snapshot = PCIREAD(0, 0, 0, 0xD4)

3.7 Register Field Access Types

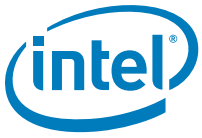
Table 33. Register Access Types and Definitions (Sheet 1 of 2)

Access Type	Meaning	Description
RO	Read Only	In some cases, if a register is read only, writes to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
WO	Write Only	In some cases, if a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
R/W	Read/Write	A register with this attribute can be read and written.
R/WC	Read/Write Clear	A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.

Table 33. Register Access Types and Definitions (Sheet 2 of 2)

Access Type	Meaning	Description
R/WO	Read/Write-Once	A register bit with this attribute can be written only once after power up. After the first write, the bit becomes read only.
R/WLO	Read/Write, Lock-Once	A register bit with this attribute can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes read only.
Default	Default	When the processor is reset, it sets its registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software to determine configuration, operating parameters, and optional system features that are applicable, and to program the processor registers accordingly.

§



4 Mapping Address Spaces

The processor supports four different address spaces:

- Physical Address Space Mappings
- IO Address Space
- PCI Configuration Space
- Message Bus Space

The CPU core can only directly access *memory space* through memory reads and writes and *IO space* through the IN and OUT IO port instructions. *PCI configuration space* is indirectly accessed through IO or memory space, and the *Message Bus space* is accessed through PCI configuration space. See Chapter 3, "Register Access Methods" for details.

This chapter describes how the memory, IO, PCI, and Message Bus spaces are mapped to interfaces in the processor.

Note: See Chapter 11, "Processor Transaction Router" for registers specified in the chapter.

4.1 Physical Address Space Mappings

There are 64 GB (36-bits) of physical address space that can be used as:

- Memory Mapped IO (MMIO – IO fabric)
- Physical Memory (DRAM)

The CPU core can access the full physical address space, while downstream devices can only access processor DRAM, and each CPU core's local APIC. Peer-to-peer transactions are not supported.

Most devices map their registers and memory to the physical address space. This section summarizes the possible mappings.

4.1.1 Processor Transaction Router Memory Map

The Processor Transaction Router maps the physical address space as follows:

- CPU core to DRAM
- CPU core to IO fabric (MMIO)
- CPU core to extended PCI registers (ECAM accesses)
- IO fabric to CPU cores (local APIC interrupts)

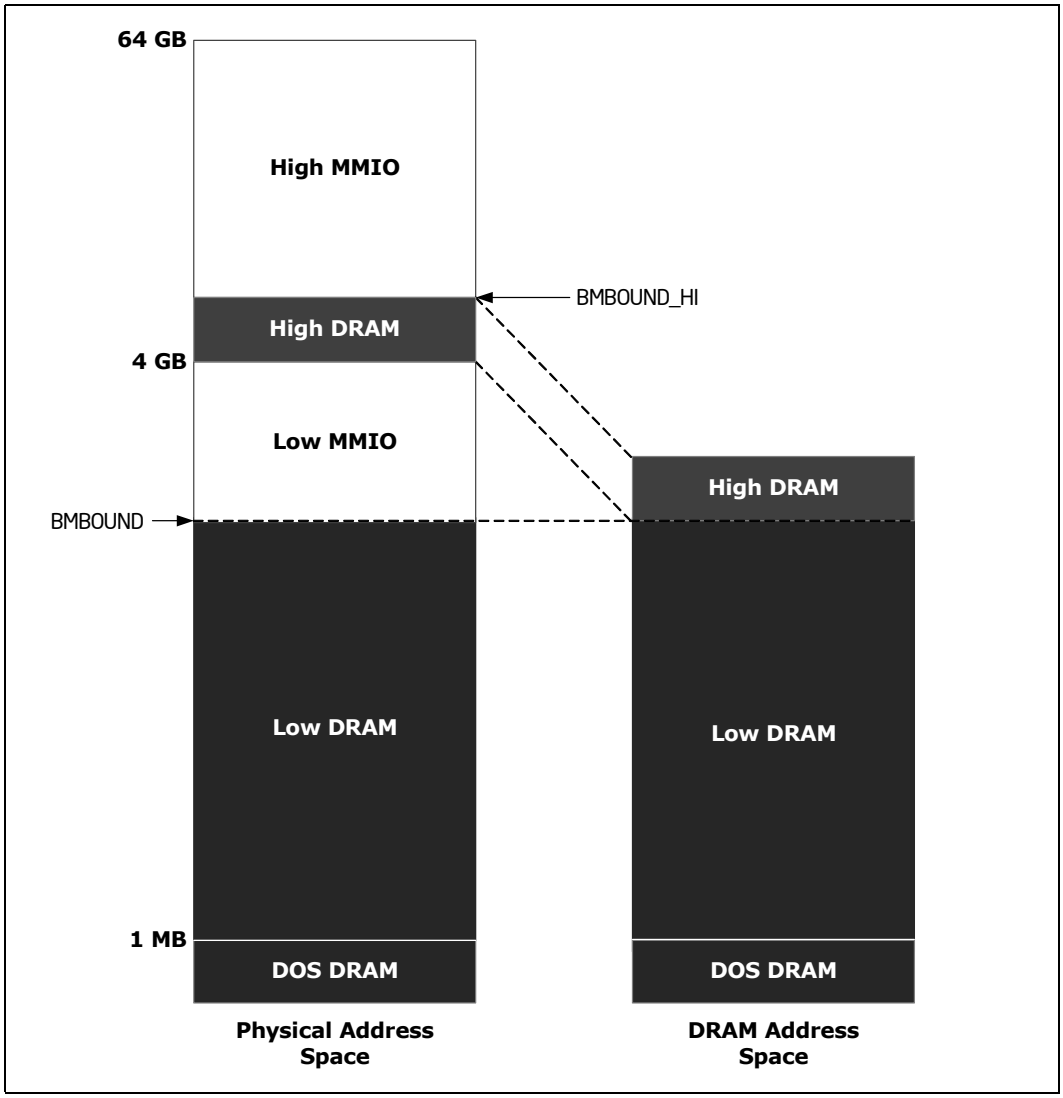
Although 64 GB (36-bits) of physical address space is accessible, some MMIO must exist for devices and software with 32-bit limits. Further, all DRAM should remain accessible for devices and software with access to memory above 4 GB. These goals

are accomplished by moving a section DRAM to start at the fixed 4 GB boundary, leaving a hole below 4 GB for MMIO. This creates the following distinct memory regions:

- DOS DRAM + Low DRAM
- Low MMIO
- High DRAM
- High MMIO

There are two registers used to create these regions – BMBOUND and BMBOUND_HI. Their use is shown in Figure 2.

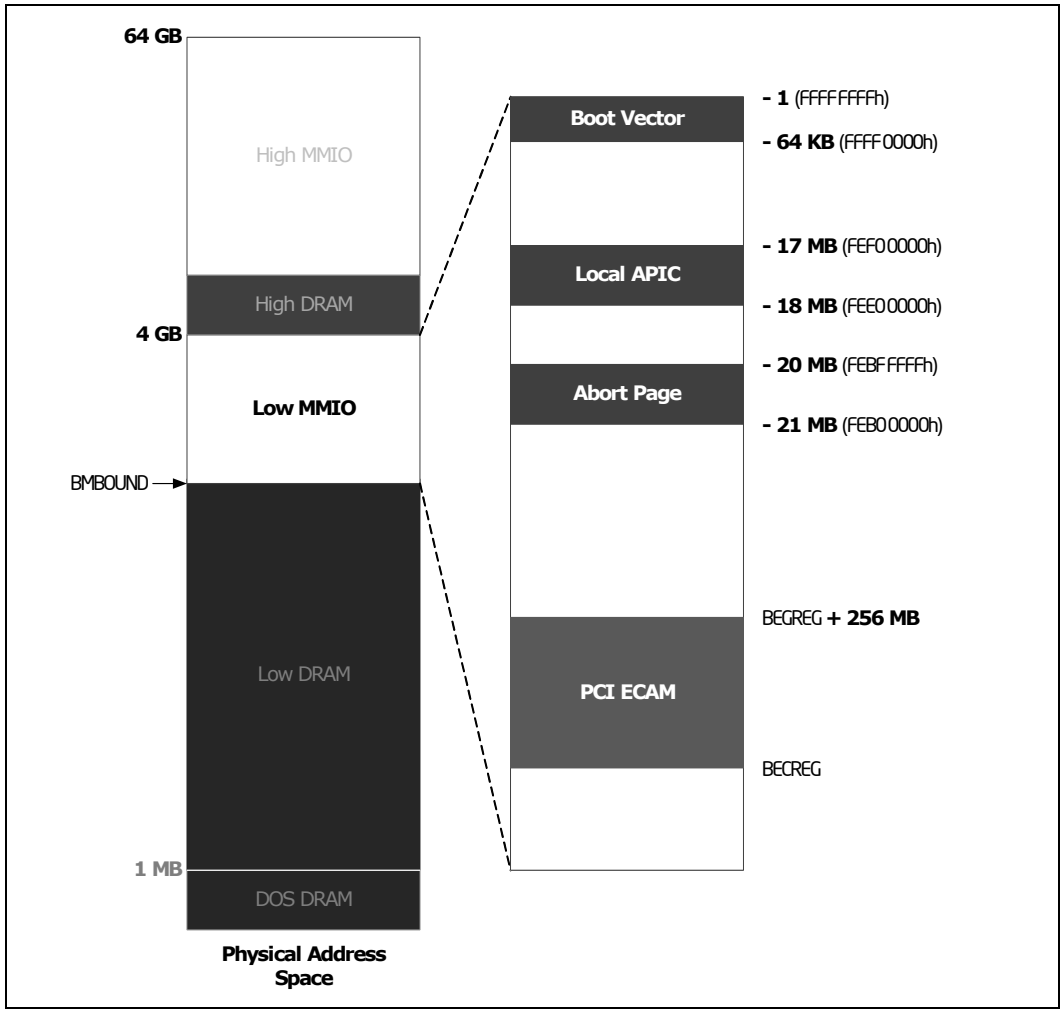
Figure 2. Physical Address Space – DRAM & MMIO



4.1.1.1 Low MMIO

The low MMIO mappings are shown in Figure 3.

Figure 3. Physical Address Space – Low MMIO



By default, CPU core reads targeting the **Boot Vector** range (FFFFFFFFh–FFFF0000h) are sent to the boot Flash connected to the Platform Controller Unit, and write accesses target DRAM. This allows the boot strap CPU core to fetch boot code from the boot Flash, and then shadow that code to DRAM.

Upstream writes from the IO fabric to the **Local APIC** range (FEE00000h–FEF00000h) are sent to the appropriate CPU core's APIC.

Write accesses from a CPU core to the **Abort Page** range (FEB00000h–FEBFFFFFh) will be dropped, and reads will always return all 1s in binary.

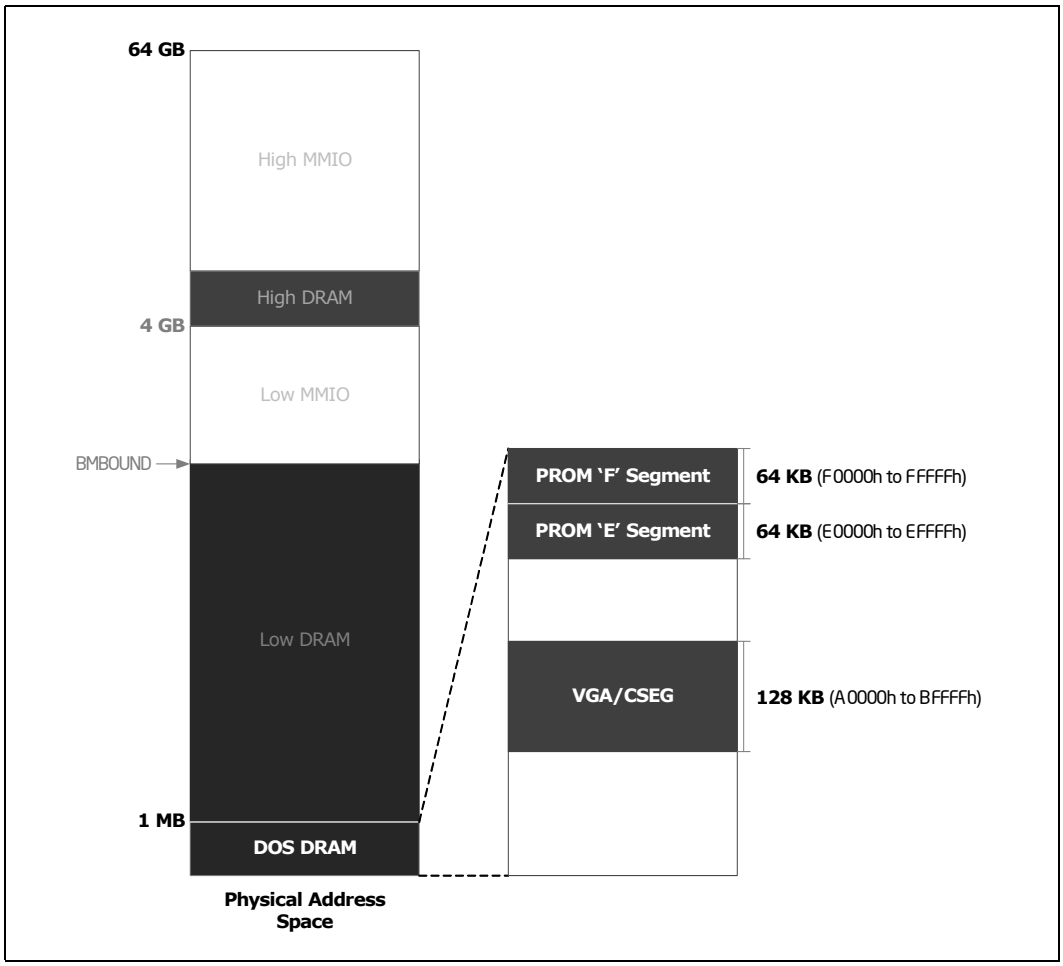
Accesses in the 256 MB **PCI ECAM** range, starting at BECREG, generate enhanced PCI configuration register accesses when enabled (BECREG.ECENABLE). Unlike traditional memory writes, writes to this range are non-posted when enabled. See Chapter 3, "Register Access Methods" for more details.

All other downstream accesses in the Low MMIO range are sent to the IO Fabric for further decode based on PCI resource allocations. The IO Fabric's subtractive agent (for unclaimed accesses) is the Platform Controller Hub.

4.1.1.2 DOS DRAM

The DOS DRAM is the memory space below 1 MB. In general, accesses from a processor targeting DOS DRAM target system DRAM. Exceptions are shown in the following figure.

Figure 4. Physical Address Space – DOS DRAM



Processor writes to the 64 KB (each) **PROM 'E'** and **'F'** segments (E0000h–EFFFFh and F0000h–FFFFFh) always target DRAM. The BMISC register is used to direct CPU core reads in these two segments to DRAM or the IO fabric (MMIO).

CPU core accesses to the 128 KB **VGA/CSEG** range (A0000h–BFFFFh) can target DRAM or the IO fabric (MMIO). The target is selected with the BMISC.ABSEGINDRAM register.

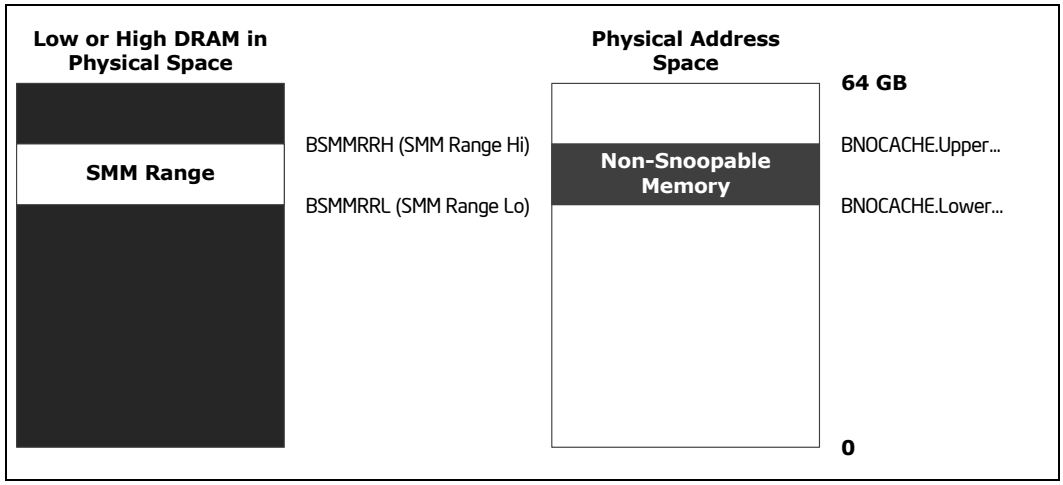
4.1.1.3 Additional Mappings

There are two additional mappings available in the Processor Transaction Router:

- SMM range
- Non-snoop range

Figure 5 shows these mappings.

Figure 5. Physical Address Space – SMM and Non-Snoop Mappings



SMI handlers running on a CPU core execute out of SMM memory. To protect this memory from non-CPU core access, the **SMM Range** (BSMMRRL-BSMMRRH) may be programmed anywhere in low or high DRAM space (1 MB aligned). This range will only allow accesses from the CPU cores.

To prevent snoops of the CPU cores when DMA devices access a specific memory region, the **Non-Snoopable Memory range** (BNOCACHE.Lower-BNOCACHE.Upper) can be programmed anywhere in physical address space. This range is enabled via the BNOCACHECTL register's enable bit (BNOCACHECTL.Enable).

4.1.2 IO Fabric (MMIO) Map

Memory accesses targeting MMIO are routed by the IO fabric to programmed PCI ranges, or routed to the PCU by default (subtractive agent). Programmed PCI ranges can be moved within low or high MMIO, and most can be disabled.

Note: Not all devices can be mapped to high MMIO.

Fixed MMIO is claimed by the Platform Controller Unit (PCU). The default regions are listed below. Movable ranges are not shown. See the register maps of all PCU devices for details.

Table 34. Fixed Memory Ranges in the Platform Controller Unit (PCU)

Device	Start Address	End Address	Comments
Low BIOS (Flash Boot)	000E0000h	000FFFFFh	Starts 128 KB below 1 MB; Firmware/BIOS
IO APIC	FEC00000h	FEC00040h	Starts 20 MB below 4 GB
HPET	FED00000h	FED003FFh	Starts 19 MB below 4 GB
TPM (LPC)	FFD40000h	FFD40FFFh	Starts 16 KB above HPET range
High BIOS/Boot Vector	FFFF0000h	FFFFFFFFh	Starts 64 KB below 4 GB; Firmware/BIOS

The following PCI devices may claim memory resources in MMIO space:

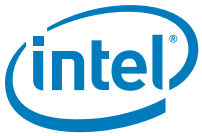
- Graphics/Display (High MMIO capable)
- PCI Express* (High MMIO capable)
- SATA
- HD Audio
- Platform Controller Unit (PCU) (Multiple BARs)
- xHCI USB
- EHCI USB

See each device's interface chapter for details.

Warning: Variable memory ranges should not be set to conflict with other memory ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

4.2 IO Address Space

There are 64 KB + 3 bytes of IO space (0h–10002h) for accessing IO registers. Most IO registers exists for legacy functions in the PCU or for PCI devices, while some are claimed by the Processor Transaction Router for graphics and for the PCI configuration space access registers.



4.2.1 Processor Transaction Router IO Map

The processor claims IO transactions for VGA/Extended VGA found in the display/ graphics interface. It also claims the two 32-bit registers at port CF8h and CFCh used to access PCI configuration space.

4.2.2 IO Fabric IO Map

4.2.2.1 PCU Fixed IO Address Ranges

The following table shows the fixed IO space ranges seen by a processor.

Table 35. Fixed IO Ranges in the Platform Controller Unit (PCU)

Device	IO Address	Comments
8259 Master	20h–21h, 24h–25h, 28h–29h, 2Ch–2Dh, 30h–31h, 34h–35h, 38h–39-, 3Ch–3Dh	
8254s	40h–43h, 50h–53h	
PS2 Control	60h, 64h	
NMI Controller	61h, 63h, 65h, 67h	
RTC	70h–77h	
Port 80h	80h–83h	
Init Register	92h	
8259 Slave	A0h–A1h, A4h–A5h, A8h–A9h, ACh–ADh, B0h–B1h, B4h–B5h, B8h–B9h, BCh–BDh, 4D0h–4D1h	
PCU UART	3F8h–3FFh	
Reset Control	CF9h	Overlaps PCI IO registers
Active Power Management	B2h–B3h	

4.2.2.2 Variable IO Address Ranges

Table 36 shows the variable IO decode ranges. They are set using base address registers (BARs) or other similar means. Plug-and-play (PnP) software (PCI/ACPI) can use their configuration mechanisms to set and adjust these values.

Warning: The variable IO ranges should not be set to conflict with other IO ranges. There will be unpredictable results if the configuration software allows conflicts to occur. Hardware does not check for conflicts.

Table 36. Movable IO Ranges Decoded by PCI Devices on the IO Fabric (Sheet 1 of 2)

Device	Size (bytes)	Target
SATA		See SATA register map for details.
ACPI Power Management (PCU)	128	ACPI_BASE_ADDR (PM1BLK): PCI[B:0,D:31,F:0] + 40h

Table 36. Movable IO Ranges Decoded by PCI Devices on the IO Fabric (Sheet 2 of 2)

Device	Size (bytes)	Target
SMBus (PCU)	32	SMBA: PCI[B:0,D:31,F:3] + 20h
GPIO (PCU)	256	GBA: PCI[B:0,D:31,F:0] + 48h
RCBA (PCU)	1024	RCRB_BA: PCI[B:0,D:31,F:0] + F0h

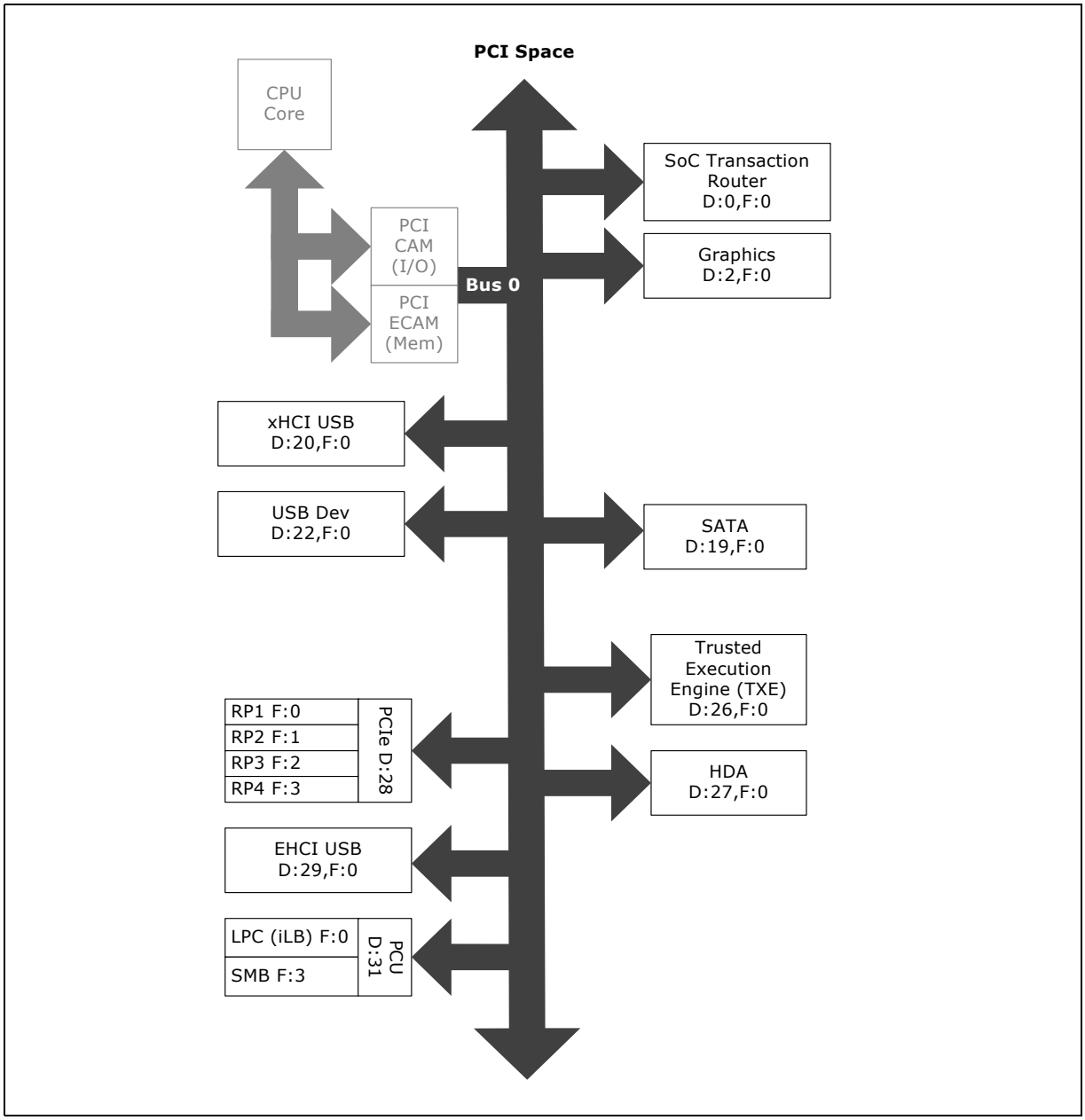
4.3 PCI Configuration Space

All PCI devices/functions are shown below.

Table 37. PCI Devices and Functions

Bus	Device	Function	Device ID	Device Description	Function Description
0	0	0	0F00h	Processor Transaction Router	
0	2	0	0F31h	Graphics & Display	
0	18	0	0F16h	Storage Control Cluster (SCC)	SD Port
0	19	0	0F20h (IDE) 0F21h (IDE) 0F22h (AHCI) 0F23h (AHCI)	SATA	
0	20	0	0F35h	xHCI USB	
0	26	0	0F18h	Trusted Execution Engine	
0	27	0	0F04h	HD Audio	
0	28	0	0F48h	PCI Express*	Root Port 1
		1	0F4Ah		Root Port 2
		2	0F4Ch		Root Port 3
		3	0F4Eh		Root Port 4
0	29	0	0F34h	EHCI USB	
0	31	0	0F1Ch	Platform Controller Unit	LPC: Bridge to Intel Legacy Block
		3	0F12h		SMBus Port

Figure 6. Bus 0 PCI Devices and Functions



§ §

5 Integrated Clock

Clocks are integrated, consisting of multiple variable frequency clock domains, across different voltage domains. This architecture achieves a low power clocking solution that supports the various clocking requirements of the processor's many interfaces.

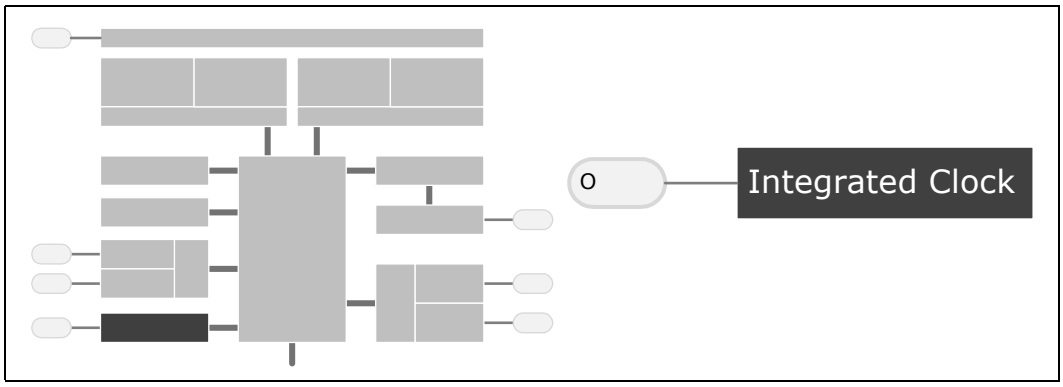
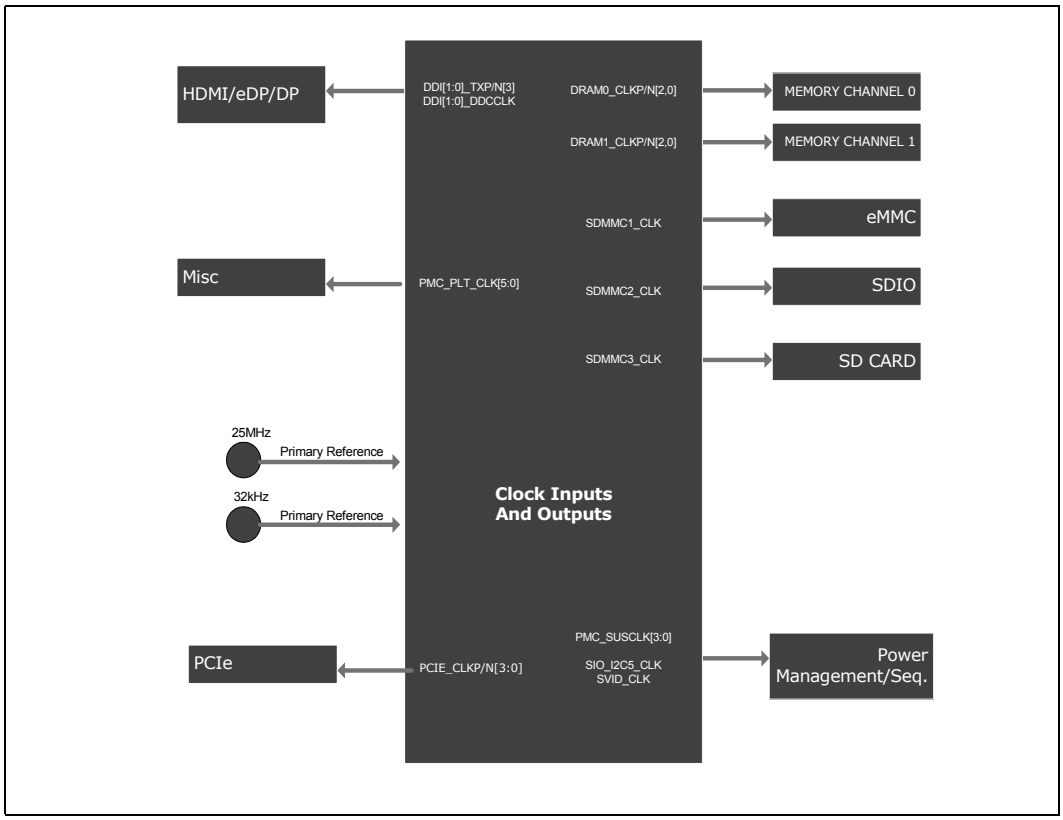
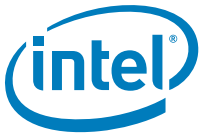


Figure 7. Clocking Example





5.1 Features

Platform clocking is provided internally by the Integrated Clock logic. No external clock chips are required for the processor to function. All the required platform clocks are provided by two crystal inputs: a 25 MHz primary reference for the integrated clock block and a 32.768 kHz reference for the Real Time Clock (RTC) block.

The different inputs and outputs are listed below.

Table 38. Processor Clock Inputs

Clock Domain	Signal Name	Frequency	Usage/Description
Main	ICLK_OSCIN ICLK_OSCOUT	25 MHz	Reference crystal for the iCLK PLL
RTC	ILB_RTC_X1 ILB_RTC_X2	32.768 kHz	RTC crystal I/O for RTC block
LPC	ILB_LPC_CLK[1]	25 MHz	Can be configured as an input to compensate for board routing delays through Soft Strap.

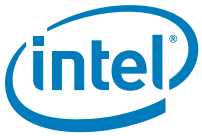
Table 39. Processor Clock Outputs (Sheet 1 of 2)

Clock Domain	Signal Name	Frequency	Usage/Description
Memory	DRAM0_CKP/N[2,0] DRAM1_CKP/N[2,0]	533/667 MHz	Drives the Memory ranks 0-1. Data rate (MT/s) is 2x the clock rate. Note: The frequency is fused in each Processor. It is not possible to support both frequencies on one Processor.
eMMC	MMC1_CLK MMC1_45_CLK	25-50 MHz 25-200 MHz	Clock for eMMC 4.41 devices Clock for eMMC 4.51 devices Actual clock can run as low as 400 kHz during initialization.
SDIO	SD2_CLK	25-50 MHz	Clock for SDIO devices
SD Card	SD3_CLK	25-50 MHz	Clock for SD card devices
SPI	PCU_SPI_CLK	20 MHz, 33 MHz, 50 MHz	Clock for SPI flash
PMIC/COMMS	PMC_SUSCLK[3:0]	32.768 kHz	Pass through clock from RTC oscillator
LPC	ILB_LPC_CLK[0:1]	25 MHz	Provided to devices requiring LPC clock
HDA	HDA_CLK	24 MHz	Serial clock for external HDA codec device
PCI Express	PCIE_CLKN[3:0] PCIE_CLKP[3:0]	100 MHz	Differential Clocks supplied to external PCI express devices based on assertion of PCIE_CLKREQ[3:0]# inputs
HDMI	DDI[1:0]_TXP/N[3]	25-148.5 MHz	Differential clock for HDMI devices
HDMI DDC	DDI[1:0]_DDCCLK	100 kHz	Clock for HDMI DDC devices
VGA DDC	VGA_DDCCLK	100 kHz	Clock for VGA DDC devices
SVID	SVID_CLK	25 MHz	Clock used by voltage regulator
I^2S	LPE_I2S[2:0]_CLK	12.5 MHz	Continuous serial clock for I^2S interfaces

Table 39. Processor Clock Outputs (Sheet 2 of 2)

Clock Domain	Signal Name	Frequency	Usage/Description
Platform Clocks	PMC_PLT_CLK [5:0]	19.2/25 MHz	Platform clocks. For example: PLT_CLK [2:0] - Camera PLT_CLK [3] - Audio Codec **NOTE:** Intel recommends 25 MHz. 19.2 MHz is not validated.
SIO SPI	SIO_SPI_CLK	15 MHz	SPI clock output
I^2C	SIO_I2C[6:0]_CLK	100 kHz, 400 kHz, 1 MHz, 3.4 MHz	I^2C clocks **NOTE:** In I^2C Controller the parameter called IC_CAP_LOADING can be set to 400pf/100pf. As per specification 3.4MHz is supported in 100pf loading while 1.7MHz is the maximum frequency at 400pf load.
SMBus	PCU_SMB_CLK	10-100 kHz	Drives SMBus device

§



6 Power Management

This chapter provides information on the following power management topics:

- ACPI States
- Processor Core
- PCI Express
- Integrated Graphics Controller

6.1 Power Management Features

- ACPI System States support (S0, S3, S4, S5)
- Processor Core/Package States support (C0 – C7)
- Processor Graphics Adapter States support D0 – D3.
- Support Link Power Management (LPM)
- Thermal throttling
- Dynamic I/O power reductions (disabling sense amps on input buffers, tri-stating output buffers)
- Active power down of Display links

6.2 Power Management States Supported

The Power Management states supported by the processor are described in this section.

6.2.1 S-State Definition

6.2.1.1 S0 – Full On

This is the normal operating state of the processor. In S0, the core processor will transition in and out of the various processor C-States and P-States.

6.2.1.2 S3 - Suspend to RAM (Standby)

S3 is a suspend state in which the core power planes of the processor are turned off and the suspend wells remain powered.

- All power wells are disabled, except for the suspend and RTC wells.
- The core processor’s macro-state is saved in memory.
- Memory is held in self-refresh and the memory interface is disabled, except the CKE pin as it is powered from the memory voltage rail. CKE is driven low.

6.2.1.3 S4 – Suspend to Disk (Hibernate)

S4 is a suspend state in which most power planes of the processor are turned off, except for the suspend and RTC well. In this ACPI state, system context is saved to the hard disk.

Key features:

- No activity is allowed.
- All power wells are disabled, except for the suspend and RTC well.

6.2.1.4 S5 – Soft Off

From a hardware perspective, the S5 state is identical to the S4 state. The difference is purely software; software does not write system context to hard disk when entering S5.

The following table shows the differences in the sleeping states with regards to the processor's output signals.

NOTES: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S5#. PMC_SUS_STAT# is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT# also warns of upcoming reset.

Table 40. Processor Sx-States to SLP_S*#

State	S0	S3	S4	S5	Reset w/o Power Cycle	Reset w/ Power Cycle
CPU Executing	In C0	OFF	OFF	OFF	No	OFF
PMC_SLP_S3#	HIGH	LOW	LOW	LOW	HIGH	LOW
PMC_SLP_S4#	HIGH	HIGH	LOW	LOW	HIGH	LOW
S0 Power Rails	ON	OFF	OFF	OFF	ON	OFF
PMC_PLTRST#	HIGH	LOW	LOW	LOW	LOW	LOW
PMC_SUS_STAT#	HIGH	LOW	LOW	LOW	HIGH	LOW
PCIe Links	L0, L1	L3	L3	L3	L3 Ready	L3

NOTES: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S5#. PMC_SUS_STAT# is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT# also warns of upcoming reset.

6.2.2 System States

Table 41. General Power States for System (Sheet 1 of 2)

States/Sub-states	Legacy Name / Description
G0/S0/C0	**FULL ON:** CPU operating. Individual devices may be shut down to save power. The different CPU operating levels are defined by Cx states.
G0/S0/Cx	**Cx State:** CPU manages C-state itself.
G0/S3	**S3 State:** Low power platform active state. All DRAM and IOSF traffic are halted. PLL are configured to be off.

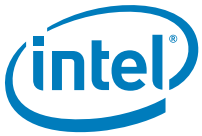


Table 41. General Power States for System (Sheet 2 of 2)

States/Sub-states	Legacy Name / Description
G1/S3	**Suspend-To-RAM(STR):** The system context is maintained in system DRAM, but power is shut to non-critical circuits. Memory is retained, and refreshes continue. All external clocks are shut off; RTC clock and internal ring oscillator clocks are still toggling.
G1/S4	**Suspend-To-Disk (STD):** The context of the system is maintained on the disk. All of the power is shut down except power for the logic to resume. The S4 and S5 states are treated the same.
G2/S5	**Soft-Off:** System context is not maintained. All of the power is shut down except power for the logic to restart. A full boot is required to restart. A full boot is required when waking. The S4 and S5 states are treated the same.
G3	**Mechanical OFF.** System content is not maintained. All power shutdown except for the RTC. No "Wake" events are possible, because the system does not have any power. This state occurs if the user removes the batteries, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depend on the state just prior to the entry to G3.

Table 42 shows the transitions rules among the various states. Note that transitions among the various states may appear to temporarily transition through intermediate states. These intermediate transitions and states are not listed in the table.

Table 42. ACPI PM State Transition Rules

Present State	Transition Trigger	Next State
G0/S0/C0	IA Code **MWAIT** or LVL Rd	C0/S0/Cx
	PM1_CNT.SLP_EN bit set	G1/Sx or G2/S5 state (specified by PM1_CNT.SLP_TYP)
	Power Button Override	G2/S5
	Mechanical Off/Power Failure	G3
G0/S0/Cx	Cx break events which include: CPU snoop, MSI, Legacy Interrupt, AONT timer	G0/S0/C0
	Power Button Override	G2/S5
	System Power Failure	G3
G1/S3,G1/S4	Any Enabled Wake Event	G0/S0/C0
	Power button Override	G2/S5
	Resume Well Power Failure	G3
G2/S5	Any Enabled Wake Event	G0/S0/C0
	Resume Well Power Failure	G3
G3	Power Returns	Option to go to S0/C0 (reboot) or G2/S5 (stay off until power button pressed or other enabled wake event) or G1/S4 (if system state was S4 prior to the power failure). Some wake events are preserved through a power failure.

6.2.3 Processor States

Table 43. Processor Core States Support

State	Description
C0	Active mode, processor executing code
C1	AutoHALT state
C6	Deep Power Down. Prior to entering the Deep Power Down Technology (code named C6) State, The core process will flush its cache and save its core context to a special on die SRAM on a different power plane. Once Deep Power Down Technology (code named C6) sequence has completed. The core processor's voltage is completely shut off.
C7	Execution cores in this state behave similarly to the C6 state. Voltage is removed from the system agent domain

6.2.4 Integrated Graphics Display States

Table 44. Processor Graphics Adapter State Control

State	Description
D0	Full on, Display active
D3	Power off display

6.2.5 Integrated Memory Controller States

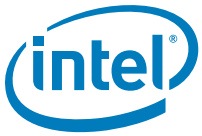
Table 45. Main Memory States

States	Description
Powerup	CKE asserted. Active mode.
Precharge Powerdown	CKE de-asserted (not self-refresh) with all banks closed.
Active Powerdown	CKE de-asserted (not self-refresh) with at least one bank active.
Self-Refresh	CKE de-asserted using device self-refresh

6.2.6 PCIe* States

Table 46. PCIe* States

States	Description
L0	Full on – Active transfer state
L0s	First Active Power Management low power state – Low exit latency
L1	Lowest Active Power Management - Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency



6.2.7 Interface State Combinations

Table 47. G, S and C State Combinations

Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1	Auto-Halt	On	Auto-Halt
G0	S0	C6	Deep Power Down	On	Deep Power Down
G1	S3	Power off		Off except RTC & internal ring OSC	Suspend to RAM
G1	S4	Power off		Off except RTC & internal ring OSC	Suspend to Disk
G2	S5	Power off		Off except RTC & internal ring OSC	Soft Off
G3	NA	Power Off		Power off	Hard Off

Table 48. D, S and C State Combinations

Graphics Adapter (D) State	Sleep (S) State	(C) State	Description
D0	S0	C0	Full On, Displaying
D0	S0	C1	Auto-Halt, Displaying
D0	S0	C6	Deep Sleep, Display Off
D3	S0	Any	Not Displaying
D3	S3		Not Displaying Graphics Core power off.
D3	S4		Not Displaying Suspend to disk Core power off

6.3 Processor Core Power Management

While executing code, Enhanced Intel® SpeedStep® Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

6.3.1 Enhanced Intel® SpeedStep® Technology

The following are the key features of Enhanced Intel® SpeedStep® Technology:

- Applicable to processor Core Voltage and Graphic Core Voltage
- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.

- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency:
  - If the target frequency is higher than the current frequency, core_VCC_S3is ramped up slowly to an optimized voltage. This voltage is signaled by the SVID signals to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the SVID signals.
- The processor controls voltage ramp rates by requesting appropriate ramp rates from an external SVID controller.
- Because there is low transition latency between P-states, a significant number of transitions per second are possible.
- Thermal Monitor mode.
  - Please refer to Thermal Management Chapter

6.3.2 Dynamic Cache Sizing

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following condition:

- The C0 timer that tracks continuous residency in the Normal state, has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The predefined L2 shrink threshold is triggered.

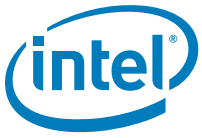
The number of L2 cache ways disabled upon each Deeper Sleep entry is configured in the BBL_CR_CTL3 MSR. The C0 timer is referenced through the CLOCK_CORE_CST_CONTROL_STT MSR. The shrink threshold under which the L2 cache size is reduced is configured in the PMG_CST_CONFIG_CONTROL MSR. If the ratio is zero, then the ratio will not be taken into account for Dynamic Cache Sizing decisions.

6.3.3 Low-Power Idle States

When the processor core is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-state. However, higher C-states have longer exit and entry latencies. Resolution of C-state occur at the thread, processor core, and processor core level.

6.3.3.1 Clock Control and Low-Power States

The processor core supports low power states at core level. The central power management logic ensures the entire processor core enters the new common processor core power state. For processor core power states higher than C1, this would be done



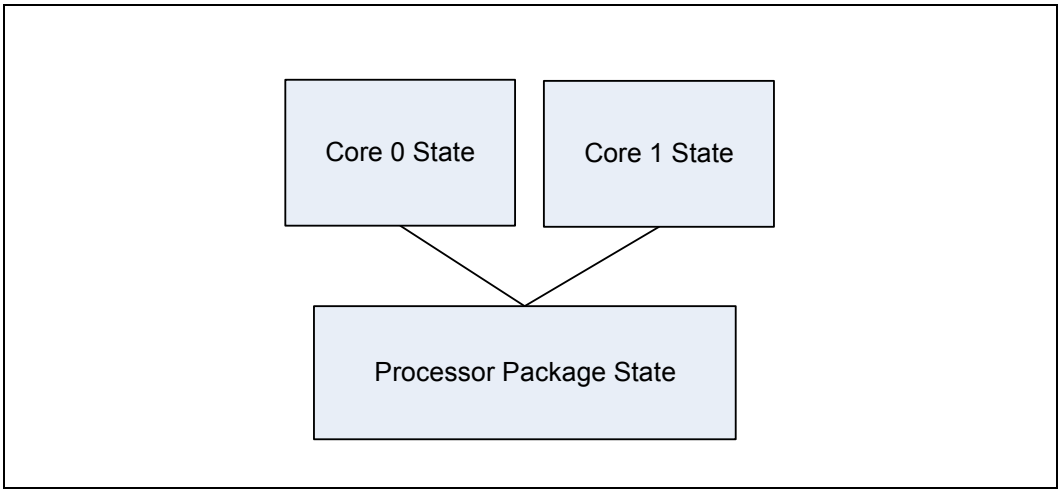
by initiating a P_LVLx (P_LVL6) I/O read to all of the cores. States that require external intervention and typically map back to processor core power states. States for processor core include Normal (C0, C1).

The processor core implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state specifies and P_LVLx reads to the ACPI P_BLK register block mapped in the processor core's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor core and do not directly result in I/O reads on the processor core bus. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state specifications used for each P_LVLx read can be configured in a software programmable MSR by BIOS.

The Cx state ends due to a break event. Based on the break event, the processor returns the system to C0. The following are examples of such break events:

- Any unmasked interrupt goes active
- Any internal event that will cause an NMI or SMI_B
- CPU Pending Break Event (PBE_B)
- MSI

Figure 8. Idle Power Management Breakdown of the Processor Cores



6.3.4 Processor Core C-States Description

The following state descriptions assume that both threads are in common low power state.

6.3.4.1 Core C0 State

The normal operating state of a core where code is being executed.

6.3.4.2 Core C1 State

C1 is a low power state entered when a core execute a HLT or MWAIT(C1) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1 state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide* for more information.

While a core is in C1 state, it processes bus snoops and snoops from other threads.

6.3.4.3 Core C6 State

Individual core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM. Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored.

There are various types of C-state:

- C6NS implies only the core should be powergated, but the L2 cache contents should be retained.
- C6FS implies the core should be powergates, and the L2 cache can be fully flushed to get even more power savings.

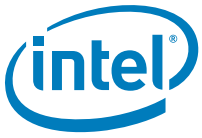
6.3.4.4 Core C7 State

Individual core can enter the C7 state by initiating a P_LVL7 I/O read or an MWAIT(C7) instruction. The core C7 state exhibits the same behavior as core C6 state, but in addition gives permission to the internal Power Management logic to enter a package state if possible.

6.3.5 Package C-States

The processor supports C0, C1, C6 and C7 power states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states unless specified otherwise:

- Package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
- Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
- The platform may allow additional power savings to be realized in the processor.
- For package C-states, the processor is not required to enter C0 before entering any other C-state.
- Entry in to a package C-state may be subject to auto-demotion – that is, the processor may keep the package in a shallower package C-state then requested by



the operating system if the processor determines, using heuristics, that the shallower C-state results in better power/performance.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
  - If the break event is not masked, the target core enters the core C0 state and the processor enters package C0.
  - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request.
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

Table 49. Coordination of Core/Module Power States at the Package Level

Package C-State		Core/Module 1			
		C0	C1	C6NS	C7 (C6FS)
Core/Module 0	C0	C0	C1	C0	C0
	C1	C0	C1	C1	C1
	C6NS	C0	C1	C6C	C6C
	C7 (C6FS)	C0	C1	C6C	C7

NOTES:
1. 2 Cores of the Processor will make up one module.

6.3.5.1 Package C0 State

The normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

6.3.5.2 Package C1 State

No additional power reduction actions are taken in the package C1 state.

The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 state or lower power state.

No notification to the system occurs upon entry to C1 state.

6.3.5.3 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 state or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C7 state but has allowed a package C6 state.

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts.

6.3.5.4 Package C7 State

A processor enters the package C7 low power state when all cores are in the C7 state. In package C7, the processor will take action to remove power from portions of the system agent.

Core break events are handled the same way as in package C6.

6.3.6 Graphics Power Management

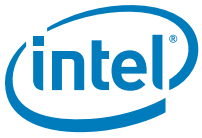
6.3.6.1 Graphics and video decoder C-State

GFX C-State (GC6) and VED C-state (VC6) are designed to optimize the average power to the graphics and video decoder engines during times of idleness. GFX C-state is entered when the graphics engine, has no workload being currently worked on and no outstanding graphics memory transactions. VED S-state is entered when the video decoder engine has no workload being currently worked on and no outstanding video memory transactions. When the idleness condition is met, the processor will power gate the Graphics and video decoder engines.

6.3.6.2 Intel® Display Power Saving Technology (Intel® DPST)

The Intel DPST technique achieves backlight power savings while maintaining visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user image quality at a decreased backlight power level.

1. The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel® DPST software is generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)



2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image. Intel DPST 5.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

6.3.6.3 Intel® Automatic Display Brightness

The Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the back light setting.

6.3.6.4 Intel® Seamless Display Refresh Rate Switching Technology (Intel® SDRRS Technology)

When a Local Flat Panel (LFP) supports multiple refresh rates, the Intel® Display Refresh Rate Switching power conservation feature can be enabled. The higher refresh rate will be used when on plugged in power or when the end user has not selected/ enabled this feature. The graphics software will automatically switch to a lower refresh rate for maximum battery life when the design application is on battery power and when the user has selected/enabled this feature.

There are two distinct implementations of Intel SDRRS – static and seamless. The static Intel SDRRS method uses a mode change to assign the new refresh rate. The seamless Intel SDRRS method is able to accomplish the refresh rate assignment without a mode change and therefore does not experience some of the visual artifacts associated with the mode change (SetMode) method.

6.4 Memory Controller Power Management

The main memory is power managed during normal operation and in low-power ACPI Cx states.

6.4.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as DIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.

- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tri-stated with an SO-DIMM present, the DIMM is not guaranteed to maintain data integrity.

SCKE tri-state should be enabled by BIOS where appropriate, since at reset all rows must be assumed to be populated.

6.4.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals, which the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

6.4.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that is recognized (other than the DDR3 reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up.

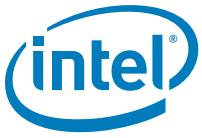
CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is guaranteed to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

6.4.2.2 Conditional Self-Refresh

Intel Rapid Memory Power Management (Intel RMPM) conditionally places memory into self-refresh in the package C3 and C6 low-power states. RMPM functionality depends on graphics/display state (relevant only when internal graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

When entering the Suspend-to-RAM (STR) state, the processor core flushes pending cycles and then places all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for the package C3 and C6 states as long as there are no memory requests to service.



6.4.2.3 Dynamic Power Down Operation

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor core controller can be configured to put the devices in active power-down (CKE deassertion with open pages) or precharge power-down (CKE deassertion with all pages closed). Precharge power-down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

6.4.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks can be controlled on a per SO-DIMM basis. Exceptions are made for per SO-DIMM control signals such as CS#, CKE, and ODT for unpopulated SO-DIMM slots.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

6.5 PCI Express* (PCIe*) Power Management

- Active power management support using L0s, and L1 states.
- All inputs and outputs disabled in L3 Ready state.

§

7 Thermal Management

7.1 Overview

The processor's thermal management system helps in managing the overall thermal profile of the system to prevent overheating and system breakdown. The architecture implements various proven methods of maintaining maximum performance while remaining within the thermal spec. Throttling mechanisms are used to reduce power consumption when thermal limits of the device are exceeded and the system is notified of critical conditions using interrupts or thermal signalling pins. Processor thermal management differs from legacy implementations primarily by replacing dedicated thermal management hardware with firmware.

The thermal management features are:

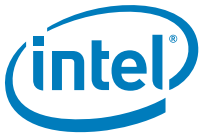
- Five digital thermal sensors (DTS)
- Supports a hardware trip point and four programmable trip points based on the temperature indicated by thermal sensors.
- Supports different thermal throttling mechanisms.

7.2 Thermal Design Power (TDP)

The processor TDP is the maximum sustained power that should be used for design of the processor thermal solution. TDP represents an expected maximum sustained power from realistic applications. TDP may be exceeded for short periods of time or if running a "power virus" workload. The processor integrates multiple processing and graphics cores. This may result in differences in the power distribution across the die and must be considered when designing the thermal solution.

Intel Graphics Dynamic Frequency Technology has the ability of the processor graphics cores to opportunistically increase frequency and/or voltage above the guaranteed graphics frequency for the given part. It is invoked opportunistically and automatically as long as the processor is conforming to its temperature, power delivery, and current specification limits. When Intel Graphics Dynamic Frequency Technology is enabled:

- Applications are expected to run closer to TDP more often as the processor will attempt to maximize performance by taking advantage of available TDP headroom in the processor package.
- The processor may exceed the TDP for short durations to use any available thermal capacitance within the thermal solution. The duration and time of such operation can be limited by platform runtime configurable registers within the processor.
- Thermal solutions and platform cooling that are designed to less than thermal design guidance may experience thermal and performance issues since more applications will tend to run at or near TDP for significant periods of time.



7.3 Scenario Design Power (SDP)

Scenario Design Power (SDP) is a usage-based design specification, and provides additional guidance for power constrained platforms. SDP is defined at a specific scenario workload, temperature and frequency.

SDP in the processor can either be set statically or dynamically by changing the POWER_LIMIT (PL1), it is required that the system cooling capability sustainable such power level. While the SDP specification is characterized at Tj of 80 °C, the functional limit for the product remains at TjMAX. Customers may choose to have the processor invoke TCC Activation Throttling at 80 °C, but is not required. The processors that have SDP specified can still exceed SDP under certain workloads such as TDP workloads. TDP power dissipation is still possible with the intended usage models, and protection mechanisms to handle levels beyond cooling capabilities are recommended. Intel recommends using such thermal control mechanisms to manage situations where power may exceed the thermal design capability.

Note: Although SDP is defined at 80 °C, the thermal throttling set point will default to 90 °C, and may be changed by the BIOS to 80 °C.

7.4 Thermal Sensors

The processor provides thermal sensors that use ring oscillator based DTS (Digital Thermal Sensor) to provide more accurate measure of system thermals.

The processor instantiates multiple digital thermal sensors (one DTS for each processor core, one for each BIU-Bus Interface Unit, and two for non-core processor) and sensor grouping configurations are provided to optionally select the maximum of all sensors for thermal readout and interrupt generation.

DTS output are adjusted for silicon variations. For a given temperature, the output from DTS is always the same irrespective of silicon.

Table 50. Temperature Reading Based on DTS (If $T_{J\text{-}MAX}$ =90°C)

DTS Counter Value	Temperature Reading
127	90°C
137	80°C
147	70°C
157	60°C
167	50°C
177	40°C
187	30°C
197	20°C
207	10°C

NOTE: DTS encoding of 127 always represents $T_{J\text{-}MAX}$.If $T_{J\text{-}MAX}$ is at 100°C instead of 90°C then the encoding 127 from DTS indicates 100°C, 137 indicates 90°C and so forth.

Thermal trip points are of two types:

- **Hard Trip**: The Catastrophic trip points generated by DTS's based on predefined temperature setting defined in fuses.
- **Programmable Trips**: four programmable trip settings (Hot, Aux2, Aux1, Aux0) that can be set by firmware/software. Default value for Hot Trip is from Fuses.

Note: DTS accuracy is around 8 ^{o}C under 60 ^{o}C and around 6^{o}C above 60 ^{o}C.

7.5 Hardware Trips

7.5.1 Catastrophic Trip (THERMTRIP)

Catastrophic trip is generated by DTS whenever the ambient temperature around it reaches (or extends) beyond the maximum value (indicated by a fuse). Catastrophic trip will not trip unless enabled (DTS are enabled only after HFPLL is locked). Within each DTS, Catastrophic trips are flopped to prevent any glitches on Catastrophic signals from affecting the processor behavior. Catastrophic trips are reset, once set, during power cycles.

Catastrophic trip signals from all DTS in the processor are combined to generate THERMTRIP function, which will in turn shut off all the PLLs and power rails to prevent processor breakdown. To prevent glitches from triggering shutdown events, Catastrophic trips from DTS's are registered before being sent out.

7.6 Processor Programmable Trips

Programmable trips can be programmed to cause different actions when triggered to reduce temperature of the die.

7.6.1 Aux3 Trip

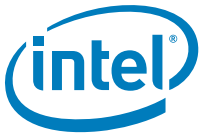
By default, the Aux 3 (Hot Trip) point is set by fuses but the software/firmware has an option to set these to a different value.

This trip point is enabled by firmware to monitor and control the system temperature while the rest of the system is being set up.

7.6.2 Aux2, Aux1, Aux0 Trip

These are fully programmable trip points for general hardware protection mechanisms. The programmable trips are only active after software/firmware enables the trip.

Note: Unlike Aux3, the Aux[2:0] trip registers are defaulted to zero. To prevent spurious results, software/firmware should program the trip values prior to enabling the trip point.



7.7 Platform Trips

7.7.1 PROCHOT#

The platform components use the signal PROCHOT# to indicate thermal events to the processor.

The processor core HOT trip as well as the processor AUX 3 trip are individually sent to firmware, which internally combines them and drives the appropriate PROCHOT back. Assertion of the PROCHOT# input will trigger Thermal Monitor 1 or Thermal Monitor 2 throttling mechanisms if they are enabled.

7.8 Thermal Throttling Mechanisms

Thermal throttling mechanisms are implemented to try to reduce temperature by reducing power consumption in response to a HOT condition. Actions taken as a result of Thermal Trip indication can be as simple as throttling bandwidth and frequency to as drastic as shutting down the PLLs and the entire system. Actions are primarily taken in to prevent system breakdown and are dependent on the severity of the trips.

7.9 Thermal Status

The firmware captures Thermal Trip events (other than THERMTRIP) in status registers to trigger thermal actions. Associated with each event is a set of programmable actions.

§

8 Electrical Specifications

This chapter contains the following sections:

8.1 Thermal Specifications

These specifications define the operating thermal limits of the processor. Thermal solutions not designed to provide the following level of thermal capability may affect the long-term reliability of the processor and system, but more likely result in performance throttling to ensure silicon junction temperatures within specification.

This section specifies the thermal specifications for all SKUs. Some definitions are needed, however. "Tj Max" defines the maximum operating silicon junction temperature. Unless otherwise specified, all specifications in this document assume Tj Max as the worse case junction temperature. This is the temperature needed to ensure TDP specifications when running at guaranteed processor and graphics frequencies. "TDP" defines the thermal dissipated power for a worse case estimated real world thermal scenario. "SDP", or scenario dissipated power, defines the thermal dissipated power under a lighter workload specific to a user scenario and at a lower thermal junction temperature than Tj Max. Note that turbo frequencies are opportunistically selected when thermal headroom exists. Automatic throttling along with a proper thermal solution ensure Tj Max will not be exceeded.

Table 51. Processor Thermal Specifications (Sheet 1 of 2)

SKU	T_j Max	TDP	SDP
N3540 - Quad Core Pentium	100 °C	7.5 W @ Tj Max	4.5 W @ 80 °C
N3530 - Quad Core Pentium	100 °C	7.5 W @ Tj Max	4.5 W @ 80 °C
N3510 - Quad Core Pentium	100 °C	7.5 W @ Tj Max	4.5 W @ 80 °C
N2940 - Quad Core Celeron	100 °C	7.5 W @ Tj Max	4.5 W @ 80 °C
N2930 - Quad Core Celeron	100 °C	7.5 W @ Tj Max	4.5 W @ 80 °C
N2910 - Quad Core Celeron	100 °C	7.5 W @ Tj Max	4.5 W @ 80 °C
N2840 - Dual Core Celeron	100 °C	7.5 W @ Tj Max	4.5 W @ 80 °C
N2830 - Dual Core Celeron	100 °C	7.5 W @ Tj Max	4.5 W @ 80 °C
N2810 - Dual Core Celeron	100 °C	7.5 W @ Tj Max	4.5 W @ 80 °C
N2808 - Dual Core Celeron	100 °C	4.5 W @ Tj Max	3.0 W @ 60 °C
N2807 - Dual Core Celeron	80 °C	4.3 W @ Tj Max	2.5 W @ 60 °C

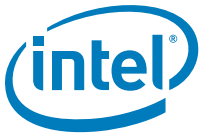


Table 51. Processor Thermal Specifications (Sheet 2 of 2)

SKU	T_j Max	TDP	SDP
N2805 - Dual Core	80 °C	4.3 W @ Tj Max	2.5 W @ 60 °C
J2850 - Quad Core Pentium	100 °C	10 W @ Tj Max	-
J1850 - Quad Core Celeron	100 °C	10 W @ Tj Max	-
J1750 - Dual Core Celeron	100 °C	10 W @ Tj Max	-
J2900 - Quad Core Pentium	0 to 105 °C	10 W @ 100 °C	-
J1900 - Quad Core Celeron	0 to 105 °C	10 W @ 100 °C	-
J1800 - Dual Core Celeron	0 to 105 °C	10 W @ 100 °C	-

8.2 Storage Conditions

This section specifies the absolute maximum and minimum storage temperature and humidity limits for given time durations. Failure to adhere to the specified limits could result in physical damage to the component. If this is suspected, Intel recommends a visual inspection to determine possible physical damage to the silicon or surface components.

Table 52. Storage Conditions Prior to Board Attach

Symbol	Parameter	Min	Max
Tabsolute storage	Device storage temperature when exceeded for any length of time.	-25 °C	125 °C
Tshort term storage	The ambient storage temperature and time for up to 72 hours.	-25 °C	85 °C
Tsustained storage	The ambient storage temperature and time for up to 30 months.	-5 °C	40 °C
RHsustained storage	The maximum device storage relative humidity for up to 30 months.		60% @ 24 °C

Note:

- Specified temperatures are not to exceed values based on data collected. Exceptions for surface mount re-flow are specified by the applicable JEDEC standard. Non-adherence may affect processor reliability.
- Component product device storage temperature qualification methods may follow JESD22-A119 (low temperature) and JESD22-A103 (high temperature) standards when applicable for volatile memory.
- Component stress testing is conducted in conformance with JESD22-A104.
- The JEDEC J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.

8.2.1 Post Board-Attach

The storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component-level certification assessments post board-attach given the multitude of attach methods, socket types, and board types used by customers.

Provided as general guidance only, board-level Intel-branded products are specified and certified to meet the following temperature and humidity limits:

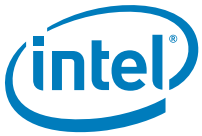
- Non-Operating Temperature Limit: -40 °C to 70 °C
- Humidity: 50% to 90%, non-condensing with a maximum wet-bulb of 28 °C

8.3 Voltage and Current Specifications

The I/O buffer supply voltages are specified at the processor package balls. The tolerances shown in the following table are inclusive of all noise from DC up to 20 MHz. The voltage rails should be measured with a bandwidth limited oscilloscope with a roll-off of 3 dB/decade above 20 MHz under all operating conditions. Table 74 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltage rails that are connected to a filter, they should be measured at the input of the filter. If the recommended platform decoupling guidelines cannot be met, the system designer will have to make trade-offs between the voltage regulator out DC tolerance and the decoupling performances of the capacitor network to stay within the voltage tolerances listed below.

Note: The SoC is a pre-launch product. Voltage and current specifications are subject to change.

Platform Rail	Voltage Tolerances	Max Icc -M (2.xW SDP)	Max Icc -M	Max Icc -D
V1P0A - UNCORE_V1P0_G3 - USB3_V1P0_G3	1.0 V DC: ±2% AC: ±3%	325 mA	325 mA	350 mA
V1P24A - USB_HSIC_V1P24_G3 (Can connect to V1P0A when USB HSIC isn't used)	1.24 V DC: ±3% AC: ±2%	35 mA	35 mA	35 mA
V1P8A - PCU_V1P8_G3 - PMC_V1P8_G3 - UNCORE_V1P8_G3 - USB_V1P8_G3 - USB_ULPI_V1P8_G3	1.8 V DC: ±3% AC: ±2%	65 mA	65 mA	65 mA
V3P3A - PCU_V3P3_G3 - USB_V3P3_G3	3.3 V DC: ±2% AC: ±3%	50 mA	50 mA	55 mA



Platform Rail	Voltage Tolerances	Max Icc -M (2.xW SDP)	Max Icc -M	Max Icc -D
V1P0Sx - UNCORE_V1P0_S3 - DRAM_V1P0_S3 - DDI_V1P0_S3	1.0 V DC: ±2% AC: ±3%	1.9 A	1.9 A	2.1 A
V1P35Sx (VSFR) - DRAM_V1P35_S3_F1 - UNCORE_V1P35_S3_F[6:1]	1.35 V DC: ±3% AC: ±2%	375 mA	375 mA	400 mA
V1P0S - GPIO_V1P0_S3 - PCIE_SATA_V1P0_S3 - PCIE_V1P0_S3 - SATA_V1P0_S3 - SVID_V1P0_S3 - UNCORE_V1P0_S3 - USB_V1P0_S3 - VGA_V1P0_S3	1.0 V DC: ±3% AC: ±2%	850 mA	850 mA	900 mA
V1P05S - CORE_V1P05_S3	1.05 V DC: ±2% AC: ±3%	1.0 A	1.0 A	1.1 A
V1P35S - ICLK_V1P35_S3_F[2:1] - VGA_V1P35_S3_F1	1.35 V DC: ±3% AC: ±2%	45 mA	45 mA	45 mA
V1P5V1P8S (VAUD)	1.5 V (LV HDA)	See V1P8S	See V1P8S	See V1P8S
V1P8S - UNCORE_V1P8_S3	1.8 V DC: ±3% AC: ±2%	10 mA	10 mA	10 mA
V1P8V3P3S (VSDIO,VLPC) - LPC_V1P8V3P3_S3 - SD3_V1P8V3P3_S3	1.8 V 3.3 V DC: ±3% AC: ±2%	8 mA	8 mA	8 mA
V3P3S - VGA_V3P3_S3	3.3 V DC: ±2% AC: ±3%	25 mA	25 mA	30 mA
VDD - DRAM_VDD_S4	1.35 V DC: ±2% AC: ±3%	1.25 A	1.25 A	1.25 A
VRTC - RTC_VCC	G3: 2-3 V at battery Otherwise V3P3A (pre diode drop)	100 uA (6 uA Avg.) (see note)	100 uA (6 uA Avg.) (see note)	100 uA (6 uA Avg.) (see note)

Note: RTC_VCC average current draw (G3) is specified at 27 °C under battery conditions.

Table 53. Processor VCC and VNN Currents

SKU	VCC Icc Max	VNN Icc Max
N3520 - Quad Core Pentium	10.5 A	10.5 A
N2920 - Quad Core Celeron	8.5 A	10.5 A
N2820 - Dual Core Celeron	5.2 A	10.5 A
N2815 - Dual Core Celeron	5.2 A	10.5 A
N2806 - Dual Core	4 A	7 A
N2807 - Dual Core	4 A	7 A
J2900 - Quad Core Pentium	13.5 A	11 A
J1900 - Quad Core Celeron	10.5 A	11 A
J1800 - Dual Core Celeron	7 A	10.5 A

8.3.1 VCC and VNN Voltage Specifications

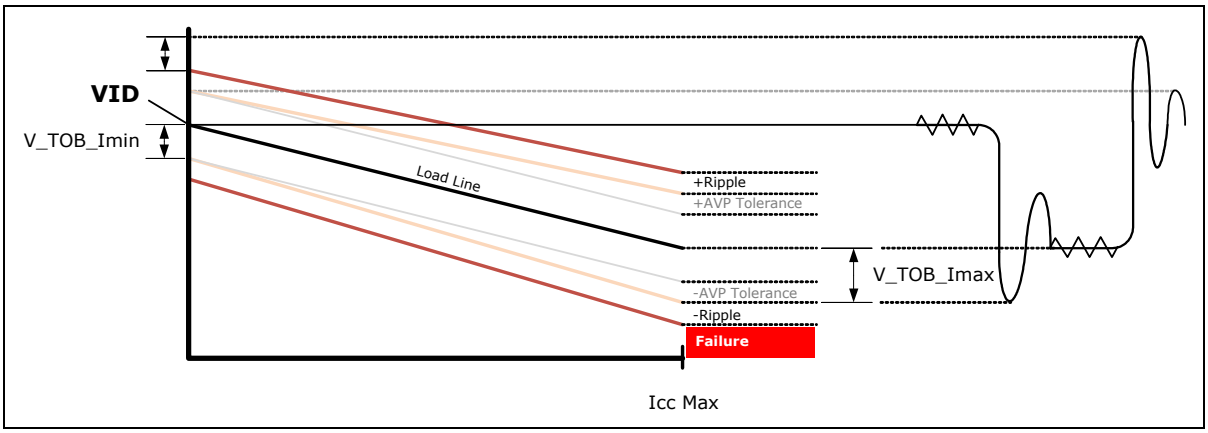
Table 54 and Figure 9 list the DC specifications for the processor power rails. They are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 54. VCC and VNN DC Voltage Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
CORE_VCC VID	Core VID Target Range	0.40		1.14	V	
CORE_VCC_S3	V_{CC} for Processor Core	See VCC VID			V	2, 3, 5
UNCORE_VNN VID	Uncore VID Target Range	0.50		1.05	V	
UNCORE_VNN_S3	V_{NN} for Processor Uncore	See VNN VID			V	2, 3, 5
CORE_VCC/ UNCORE_VNN V_{BOOT}	Default target V_{CC}/V_{NN} voltage for initial power up.		1.0 or 1.1		V	4
$SLOPE_{LL}$	Processor Core Supply DC Loadline		-5.9		mΩ	Figure 9

NOTES:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual VID values are calibrated during manufacturing such that two SoCs at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power management event.
3. These are pre-silicon estimates and are subject to change.
4. See the VR12/IMVP7 Pulse Width Modulation specification for additional details. Either value is ok.
5. N/A

Figure 9. CORE_VCC_S3 and UNCORE_VCC_S3 Processor Loadline



8.3.2 Voltage Identification (VID)

The VID specifications for the processor CORE_VCC_S3 and UNCORE_VNN_S3 are defined by the IMVP7 Pulse Width Modulation (PWM) Specification. Table 55 specifies the voltage level corresponding to the 8-bit VID value transmitted over serial VID (SVID) interface per IMVP7 specification. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. The SVID signals are CMOS push/pull drivers. Refer to Table 83 for the DC specifications for these signals. The VID codes will change due to performance, temperature and/or current load changes in order to minimize the power of the part. A voltage range is provided in Table 54. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in Table 54. The processor provides the ability to operate while transitioning to an adjacent VID and its associated voltage. This will represent a DC shift in the loadline.

Note: The following table lists all voltages possible per IMVP7 specification. Not all voltages are valid on actual SKUs.

Table 55. IMVP7.0 Voltage Identification Reference (Sheet 1 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
0	0	0	0	0	0	0	0	0	0	0.00000
0	0	0	0	0	0	0	1	0	1	0.25000
0	0	0	0	0	0	1	0	0	2	0.25500
0	0	0	0	0	0	1	1	0	3	0.26000
0	0	0	0	0	1	0	0	0	4	0.26500

Table 55. IMVP7.0 Voltage Identification Reference (Sheet 2 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
0	0	0	0	0	1	0	1	0	5	0.27000
0	0	0	0	0	1	1	0	0	6	0.27500
0	0	0	0	0	1	1	1	0	7	0.28000
0	0	0	0	1	0	0	0	0	8	0.28500
0	0	0	0	1	0	0	1	0	9	0.29000
0	0	0	0	1	0	1	0	0	A	0.29500
0	0	0	0	1	0	1	1	0	B	0.30000
0	0	0	0	1	1	0	0	0	C	0.30500
0	0	0	0	1	1	0	1	0	D	0.31000
0	0	0	0	1	1	1	0	0	E	0.31500
0	0	0	0	1	1	1	1	0	F	0.32000
0	0	0	1	0	0	0	0	1	0	0.32500
0	0	0	1	0	0	0	1	1	1	0.33000
0	0	0	1	0	0	1	0	1	2	0.33500
0	0	0	1	0	0	1	1	1	3	0.34000
0	0	0	1	0	1	0	0	1	4	0.34500
0	0	0	1	0	1	0	1	1	5	0.35000
0	0	0	1	0	1	1	0	1	6	0.35500
0	0	0	1	0	1	1	1	1	7	0.36000
0	0	0	1	1	0	0	0	1	8	0.36500
0	0	0	1	1	0	0	1	1	9	0.37000
0	0	0	1	1	0	1	0	1	A	0.37500
0	0	0	1	1	0	1	1	1	B	0.38000
0	0	0	1	1	1	0	0	1	C	0.38500
0	0	0	1	1	1	0	1	1	D	0.39000
0	0	0	1	1	1	1	0	1	E	0.39500
0	0	0	1	1	1	1	1	1	F	0.40000
0	0	1	0	0	0	0	0	2	0	0.40500
0	0	1	0	0	0	0	1	2	1	0.41000
0	0	1	0	0	0	1	0	2	2	0.41500
0	0	1	0	0	0	1	1	2	3	0.42000
0	0	1	0	0	1	0	0	2	4	0.42500
0	0	1	0	0	1	0	1	2	5	0.43000
0	0	1	0	0	1	1	0	2	6	0.43500
0	0	1	0	0	1	1	1	2	7	0.44000
0	0	1	0	1	0	0	0	2	8	0.44500
0	0	1	0	1	0	0	1	2	9	0.45000
0	0	1	0	1	0	1	0	2	A	0.45500
0	0	1	0	1	0	1	1	2	B	0.46000
0	0	1	0	1	1	0	0	2	C	0.46500
0	0	1	0	1	1	0	1	2	D	0.47000
0	0	1	0	1	1	1	0	2	E	0.47500

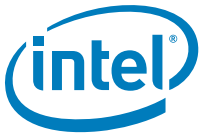


Table 55. IMVP7.0 Voltage Identification Reference (Sheet 3 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
0	0	1	0	1	1	1	1	2	F	0.48000
0	0	1	1	0	0	0	0	3	0	0.48500
0	0	1	1	0	0	0	1	3	1	0.49000
0	0	1	1	0	0	1	0	3	2	0.49500
0	0	1	1	0	0	1	1	3	3	0.50000
0	0	1	1	0	1	0	0	3	4	0.50500
0	0	1	1	0	1	0	1	3	5	0.51000
0	0	1	1	0	1	1	0	3	6	0.51500
0	0	1	1	0	1	1	1	3	7	0.52000
0	0	1	1	1	0	0	0	3	8	0.52500
0	0	1	1	1	0	0	1	3	9	0.53000
0	0	1	1	1	0	1	0	3	A	0.53500
0	0	1	1	1	0	1	1	3	B	0.54000
0	0	1	1	1	1	0	0	3	C	0.54500
0	0	1	1	1	1	0	1	3	D	0.55000
0	0	1	1	1	1	1	0	3	E	0.55500
0	0	1	1	1	1	1	1	3	F	0.56000
0	1	0	0	0	0	0	0	4	0	0.56500
0	1	0	0	0	0	0	1	4	1	0.57000
0	1	0	0	0	0	1	0	4	2	0.57500
0	1	0	0	0	0	1	1	4	3	0.58000
0	1	0	0	0	1	0	0	4	4	0.58500
0	1	0	0	0	1	0	1	4	5	0.59000
0	1	0	0	0	1	1	0	4	6	0.59500
0	1	0	0	0	1	1	1	4	7	0.60000
0	1	0	0	1	0	0	0	4	8	0.60500
0	1	0	0	1	0	0	1	4	9	0.61000
0	1	0	0	1	0	1	0	4	A	0.61500
0	1	0	0	1	0	1	1	4	B	0.62000
0	1	0	0	1	1	0	0	4	C	0.62500
0	1	0	0	1	1	0	1	4	D	0.63000
0	1	0	0	1	1	1	0	4	E	0.63500
0	1	0	0	1	1	1	1	4	F	0.64000
0	1	0	1	0	0	0	0	5	0	0.64500
0	1	0	1	0	0	0	1	5	1	0.65000
0	1	0	1	0	0	1	0	5	2	0.65500
0	1	0	1	0	0	1	1	5	3	0.66000
0	1	0	1	0	1	0	0	5	4	0.66500
0	1	0	1	0	1	0	1	5	5	0.67000
0	1	0	1	0	1	1	0	5	6	0.67500
0	1	0	1	0	1	1	1	5	7	0.68000
0	1	0	1	1	0	0	0	5	8	0.68500

Table 55. IMVP7.0 Voltage Identification Reference (Sheet 4 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
0	1	0	1	1	0	0	1	5	9	0.69000
0	1	0	1	1	0	1	0	5	A	0.69500
0	1	0	1	1	0	1	1	5	B	0.70000
0	1	0	1	1	1	0	0	5	C	0.70500
0	1	0	1	1	1	0	1	5	D	0.71000
0	1	0	1	1	1	1	0	5	E	0.71500
0	1	0	1	1	1	1	1	5	F	0.72000
0	1	1	0	0	0	0	0	6	0	0.72500
0	1	1	0	0	0	0	1	6	1	0.73000
0	1	1	0	0	0	1	0	6	2	0.73500
0	1	1	0	0	0	1	1	6	3	0.74000
0	1	1	0	0	1	0	0	6	4	0.74500
0	1	1	0	0	1	0	1	6	5	0.75000
0	1	1	0	0	1	1	0	6	6	0.75500
0	1	1	0	0	1	1	1	6	7	0.76000
0	1	1	0	1	0	0	0	6	8	0.76500
0	1	1	0	1	0	0	1	6	9	0.77000
0	1	1	0	1	0	1	0	6	A	0.77500
0	1	1	0	1	0	1	1	6	B	0.78000
0	1	1	0	1	1	0	0	6	C	0.78500
0	1	1	0	1	1	0	1	6	D	0.79000
0	1	1	0	1	1	1	0	6	E	0.79500
0	1	1	0	1	1	1	1	6	F	0.80000
0	1	1	1	0	0	0	0	7	0	0.80500
0	1	1	1	0	0	0	1	7	1	0.81000
0	1	1	1	0	0	1	0	7	2	0.81500
0	1	1	1	0	0	1	1	7	3	0.82000
0	1	1	1	0	1	0	0	7	4	0.82500
0	1	1	1	0	1	0	1	7	5	0.83000
0	1	1	1	0	1	1	0	7	6	0.83500
0	1	1	1	0	1	1	1	7	7	0.84000
0	1	1	1	1	0	0	0	7	8	0.84500
0	1	1	1	1	0	0	1	7	9	0.85000
0	1	1	1	1	0	1	0	7	A	0.85500
0	1	1	1	1	0	1	1	7	B	0.86000
0	1	1	1	1	1	0	0	7	C	0.86500
0	1	1	1	1	1	0	1	7	D	0.87000
0	1	1	1	1	1	1	0	7	E	0.87500
0	1	1	1	1	1	1	1	7	F	0.88000
1	0	0	1	0	0	0	0	8	0	0.88500
1	0	0	1	0	0	0	1	8	1	0.89000
1	0	0	1	0	0	1	0	8	2	0.89500

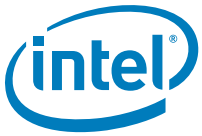


Table 55. IMVP7.0 Voltage Identification Reference (Sheet 5 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
1	0	0	0	0	0	1	1	8	3	0.90000
1	0	0	0	0	1	0	0	8	4	0.90500
1	0	0	0	0	1	0	1	8	5	0.91000
1	0	0	0	0	1	1	0	8	6	0.91500
1	0	0	0	0	1	1	1	8	7	0.92000
1	0	0	0	1	0	0	0	8	8	0.92500
1	0	0	0	1	0	0	1	8	9	0.93000
1	0	0	0	1	0	1	0	8	A	0.93500
1	0	0	0	1	0	1	1	8	B	0.94000
1	0	0	0	1	1	0	0	8	C	0.94500
1	0	0	0	1	1	0	1	8	D	0.95000
1	0	0	0	1	1	1	0	8	E	0.95500
1	0	0	0	1	1	1	1	8	F	0.96000
1	0	0	0	0	0	0	0	9	0	0.96500
1	0	0	0	0	0	0	1	9	1	0.97000
1	0	0	0	0	0	1	0	9	2	0.97500
1	0	0	1	0	0	1	1	9	3	0.98000
1	0	0	1	0	1	0	0	9	4	0.98500
1	0	0	1	0	1	0	1	9	5	0.99000
1	0	0	1	0	1	1	0	9	6	0.99500
1	0	0	1	0	1	1	1	9	7	1.00000
1	0	0	1	1	0	0	0	9	8	1.00500
1	0	0	1	1	0	0	1	9	9	1.01000
1	0	0	1	1	0	1	0	9	A	1.01500
1	0	0	1	1	0	1	1	9	B	1.02000
1	0	0	1	1	1	0	0	9	C	1.02500
1	0	0	1	1	1	0	1	9	D	1.03000
1	0	0	1	1	1	1	0	9	E	1.03500
1	0	0	1	1	1	1	1	9	F	1.04000
1	0	1	1	0	0	0	0	A	0	1.04500
1	0	1	1	0	0	0	1	A	1	1.05000
1	0	1	1	0	0	1	0	A	2	1.05500
1	0	1	0	0	0	1	1	A	3	1.06000
1	0	1	0	0	1	0	0	A	4	1.06500
1	0	1	0	0	1	0	1	A	5	1.07000
1	0	1	0	0	1	1	0	A	6	1.07500
1	0	1	0	0	1	1	1	A	7	1.08000
1	0	1	0	1	0	0	0	A	8	1.08500
1	0	1	0	1	0	0	1	A	9	1.09000
1	0	1	0	1	0	1	0	A	A	1.09500
1	0	1	0	1	0	1	1	A	B	1.10000
1	0	1	0	1	1	0	0	A	C	1.10500

Table 55. IMVP7.0 Voltage Identification Reference (Sheet 6 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
1	0	1	0	1	1	0	1	A	D	1.11000
1	0	1	0	1	1	1	0	A	E	1.11500
1	0	1	0	1	1	1	1	A	F	1.12000
1	0	1	0	0	0	0	0	B	0	1.12500
1	0	1	0	0	0	0	1	B	1	1.13000
1	0	1	0	0	0	1	0	B	2	1.13500
1	0	1	1	0	0	1	1	B	3	1.14000
1	0	1	1	0	1	0	0	B	4	1.14500
1	0	1	1	0	1	0	1	B	5	1.15000
1	0	1	1	0	1	1	0	B	6	1.15500
1	0	1	1	0	1	1	1	B	7	1.16000
1	0	1	1	1	0	0	0	B	8	1.16500
1	0	1	1	1	0	0	1	B	9	1.17000
1	0	1	1	1	0	1	0	B	A	1.17500
1	0	1	1	1	0	1	1	B	B	1.18000
1	0	1	1	1	1	0	0	B	C	1.18500
1	0	1	1	1	1	0	1	B	D	1.19000
1	0	1	1	1	1	1	0	B	E	1.19500
1	0	1	1	1	1	1	1	B	F	1.20000
1	1	0	0	0	0	0	0	C	0	1.20500
1	1	0	0	0	0	0	1	C	1	1.21000
1	1	0	0	0	0	1	0	C	2	1.21500
1	1	0	0	0	0	1	1	C	3	1.22000
1	1	0	0	0	1	0	0	C	4	1.22500
1	1	0	0	0	1	0	1	C	5	1.23000
1	1	0	0	0	1	1	0	C	6	1.23500
1	1	0	0	0	1	1	1	C	7	1.24000
1	1	0	0	1	1	0	0	C	8	1.24500
1	1	0	0	1	0	0	1	C	9	1.25000
1	1	0	0	1	0	1	0	C	A	1.25500
1	1	0	0	1	0	1	1	C	B	1.26000
1	1	0	0	1	0	0	0	C	C	1.26500
1	1	0	0	1	1	0	1	C	D	1.27000
1	1	0	0	1	1	1	0	C	E	1.27500
1	1	0	0	1	1	1	1	C	F	1.28000
1	1	0	1	0	1	0	0	D	0	1.28500
1	1	0	1	0	1	0	1	D	1	1.29000
1	1	0	1	0	0	1	0	D	2	1.29500
1	1	0	1	0	0	1	1	D	3	1.30000
1	1	0	1	0	1	0	0	D	4	1.30500
1	1	0	1	0	1	0	1	D	5	1.31000
1	1	0	1	0	1	1	0	D	6	1.31500

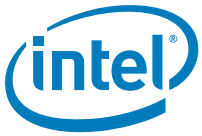


Table 55. IMVP7.0 Voltage Identification Reference (Sheet 7 of 7)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex bit 1	Hex bit 0	V_{CC} (V)
1	1	0	1	0	1	1	1	D	7	1.32000
1	1	0	1	1	0	0	0	D	8	1.32500
1	1	0	1	1	0	0	1	D	9	1.33000
1	1	0	1	1	0	1	0	D	A	1.33500
1	1	0	1	1	0	1	1	D	B	1.34000
1	1	0	1	1	1	0	0	D	C	1.34500
1	1	0	1	1	1	0	1	D	D	1.35000
1	1	0	1	1	1	1	0	D	E	1.35500
1	1	0	1	1	1	1	1	D	F	1.36000
1	1	1	0	0	0	0	0	E	0	1.36500
1	1	1	0	0	0	0	1	E	1	1.37000
1	1	1	0	0	0	1	0	E	2	1.37500
1	1	1	0	0	0	1	1	E	3	1.38000
1	1	1	0	0	1	0	0	E	4	1.38500
1	1	1	0	0	1	0	1	E	5	1.39000
1	1	1	0	0	1	1	0	E	6	1.39500
1	1	1	0	0	1	1	1	E	7	1.40000
1	1	1	0	1	0	0	0	E	8	1.40500
1	1	1	0	1	0	0	1	E	9	1.41000
1	1	1	0	1	0	1	0	E	A	1.41500
1	1	1	0	1	0	1	1	E	B	1.42000
1	1	1	0	1	1	0	0	E	C	1.42500
1	1	1	0	1	1	0	1	E	D	1.43000
1	1	1	0	1	1	1	0	E	E	1.43500
1	1	1	0	1	1	1	1	E	F	1.44000
1	1	1	1	0	0	0	0	F	0	1.44500
1	1	1	1	0	0	0	1	F	1	1.45000
1	1	1	1	0	0	1	0	F	2	1.45500
1	1	1	1	0	0	1	1	F	3	1.46000
1	1	1	1	0	1	0	0	F	4	1.46500
1	1	1	1	0	1	0	1	F	5	1.47000
1	1	1	1	0	1	1	0	F	6	1.47500
1	1	1	1	0	1	1	1	F	7	1.48000
1	1	1	1	1	0	0	0	F	8	1.48500
1	1	1	1	1	0	0	1	F	9	1.49000
1	1	1	1	1	0	1	0	F	A	1.49500
1	1	1	1	1	0	1	1	F	B	1.50000
1	1	1	1	1	1	0	0	F	C	1.49500
1	1	1	1	1	1	0	1	F	D	1.50000
1	1	1	1	1	1	1	0	F	E	1.49500
1	1	1	1	1	1	1	1	F	F	1.50000

8.4 Crystal Specifications

There are two crystal oscillators. One for RTC that maintains time and provides initial timing reference for power sequencing. The other is for the Integrated Clock, which covers clocking for the entire processor.

Table 56. ILB RTC Crystal Specification

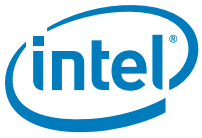
Symbol	Parameter	Min	Typ	Max	Units	Notes
F_{RTC}	Frequency	-	32.768	-	kHz	1
T_{PPM}	Crystal frequency tolerance (see notes)	-	-	±50	ppm	1
R_{ESR}	ESR	-	-	50	kOhm	1
$C_{X1,2}$	Capacitance of X1, X2 pins				pF	1

NOTES:
1. These are the specifications needed to select a crystal oscillator for the RTC circuit.
2. Crystal tolerance impacts RTC time. A 10 ppm crystal is recommended for 1.7 s tolerance per day, RTC circuit itself contributes addition 10 ppm for a total of 20 ppm in this example.

Table 57. Integrated Clock Crystal Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
F_{ICLK}	Frequency	-	25	-	MHz	1
T_{PPM}	Crystal frequency tolerance & stability	-	-	±30	ppm	1
P_{DRIVE}	Crystal drive load	-	-	100	uW	1
R_{ESR}	ESR	-	-	100	Ohm	1
C_{LOAD}	Crystal load capacitance		18		pF	
C_{SHUNT}	Crystal shunt capacitance	-	-	6	pF	1
$C_{IN/OUT}$	Capacitance of oscillator pins				pF	1

NOTES:
1. These are the specifications needed to select a crystal oscillator for the Integrated Clock circuit. Crystal must be AT cut, fundamental, parallel resonance.



8.5 DC Specifications

Platform reference voltages are specified at DC only. V_{REF} measurements should be made with respect to the supply voltages specified in "Voltage and Current Specifications".

Note: The SoC is a pre-launch product. DC specifications are subject to change.

See the following DC Specifications in this section:

- "Display DC Specification"
- "PCI Express* DC Specification"
- "DDR3L Memory Controller DC Specification"
- "USB 2.0 Host DC Specification"
- "USB 3.0 DC Specification"
- "PCU – iLB – LPC DC Specification"
- "PCU – SPI (Platform Control Unit) DC Specification"
- "PCU – Power Management/Thermal (PMC) and iLB RTC DC Specification"
- "SVID DC Specification"
- "GPIO DC Specification"

Note: Care should be taken to read all notes associated with each parameter.

8.5.1 Display DC Specification

DC specifications for display interfaces:

- "Analog VGA Video DC Specification"
- "Digital Display Interface (DDI) Signals DC Specification"

8.5.1.1 Analog VGA Video DC Specification

Interface DC Specifications are referred to the VESA Video Signal Standard, version 1 revision 2.

Table 58. R,G,B/VGA DAC Display DC specification (Functional Operating Range) (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Resolution		8		bits	1
	Max Luminance (full-scale)	0.665	0.700	0.770	V	1,2,4 (white video level voltage)
	Min Luminance		0.0		V	1,3,4 (black video level voltage)
	LSB Current		73.2	8	µA	4,5

Table 58. R,G,B/VGA DAC Display DC specification (Functional Operating Range) (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Integral Non Linearity (INL)	-1.0		+1.0	LSB	1,6
	Differential Non-Linearity (DNL)	-1.0		+1.0	LSB	1,6
	Video Channel-to-Channel Voltage amplitude mismatch			6	%	7
	Monotonicity		Guaranteed			

NOTES:
1. Measured at each R,G,B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude
3. Min steady-state amplitude
4. Defined for a double 75 Ω termination
5. Set by external reference resistor value
6. INL & DNL measured and calculated according to VESA Video Signal Standards
7. Max fill-scale voltage difference among R,G,B outputs (percentage of steady-state full-scale voltage).

Table 59. VGA_DDCCLK, VGA_DDCDATA Signal DC Specification

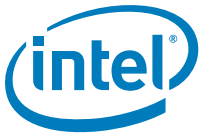
Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	VGA_V3P3_S3				
V_{IH}	Input High Voltage	2			V	1
V_{IL}	Input Low Voltage	0		0.8	V	2
V_{OL}	Output Low Voltage			0.4	V	3
I_i	Input Pin Leakage	-45		45	µA	4

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. 3 mA sink current.
4. For VIN between 0V and VGA_V3P3_S3. Measured when driver is tri-stated.

Table 60. VGA_HSYNC and VGA_VSYNC DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	VGA_V3P3_S3				
V_{OH}	Output High Voltage	2.4		V_{REF}	V	
V_{OL}	Output Low Voltage	0		0.5	V	
I_{OH}	Output High Current			8	mA	
I_{OL}	Output Low Current			8	mA	
I_i	Input Pin Leakage	-35		35	µA	1

NOTE:
1. For V_{IN} between 0-V and VGA_V3P3_S3. Measured when driver is tri-stated.



8.5.1.2 Digital Display Interface (DDI) Signals DC Specification

Table 61. DDI Main Transmitter DC specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{TX-DIFFp-p-Level0}$	Differential Peak-to-peak Output Voltage Level 0	0.34	0.4	0.46	V	1
$V_{TX-DIFFp-p-Level1}$	Differential Peak-to-peak Output Voltage Level 1	0.51	0.6	0.68	V	1
$V_{TX-DIFFp-p-Level2}$	Differential Peak-to-peak Output Voltage Level 2	0.69	0.8	0.92	V	1
$VT_{X-DIFFp-p-Level3}$	Differential Peak-to-peak Output Voltage Level 3	0.85	1.2	1.38	V	1
$V_{TX-PREEMP-RATIO}$	No Pre-emphasis	0.0	0.0	0.0	dB	1
	3.5 dB Pre-emphasis	2.8	3.5	4.2	dB	1
	6.0 dB Pre-emphasis	4.8	6.0	7.2	dB	1
	9.5 dB Pre-emphasis	7.5	9.5	11.4	dB	1
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0		2.0	V	1
RLTX-DIFF	Differential Return Loss at 0.675GHz at Tx Package pins	12			dB	4
	Differential Return Loss at 1.35 GHz at Tx Package pins	9			dB	4
C_{TX}	AC Coupling Capacitor	75		200	nF	5
Voff	Single Ended Standby (off), output voltage	-10		10	mV	6 @ AVcc
Vswing	Single Ended output swing voltage	400		600	mV	
V_{OH} (<=165 MHz)	Single Ended high level, output voltage	-10		10	mv	6 @ AVcc
V_{OH}(>165 MHz)	Single Ended high level, output voltage	-200		10	mV	6 @ AVcc
V_{OL}(<=165 MHz)	Single Ended low level, output voltage	-600		-400	mV	6 @ AVcc
V_{OL}(>165MHz)	Single Ended low level, output voltage	-700		-400	mV	6 @ AVcc

NOTES:
1. For embedded connection, support of programmable voltage swing levels is optional.
2. Total drive current of the transmitter when it is shorted to its ground.
3. Common mode voltage is equal to Vbias_Tx voltage shown in Figure 10.
4. Straight loss line between 0.675 GHz and 1.35 GHz.
5. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.
6. AVcc =Analog Voltage level

Table 62. DDI AUX Channel DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
$V_{AUX-DIFFp-p}$	AUX Peak-to-peak Voltage at a transmitting Device	0.29		1.38	V	1
$V_{AUX-\_TERM\_R}$	AUX CH termination DC resistance		100		Ω	
$V_{AUX-DC-CM}$	AUX DC Common Mode Voltage	0		2.0	V	2
$V_{AUX-TURN-CM}$	AUX turn around common mode voltage			0.3	V	3
I_{AUX_SHORT}	AUX Short Circuit Current Limit			90	mA	4
C_{AUX}	AC Coupling Capacitor	75		200	nF	5

NOTES:
1. $V_{AUX-DIFFp-p} = 2*|V_{AUXP} - V_{AUXM}|$
2. Common mode voltage is equal to V_{bias_Tx} (or V_{bias_Rx}) voltage.
3. Steady state common mode voltage shift between transmit and receive modes of operation.
4. Total drive current of the transmitter when it is shorted to its ground.
5. All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.

Figure 10. Definition of Differential Voltage and Differential Voltage Peak-to-Peak

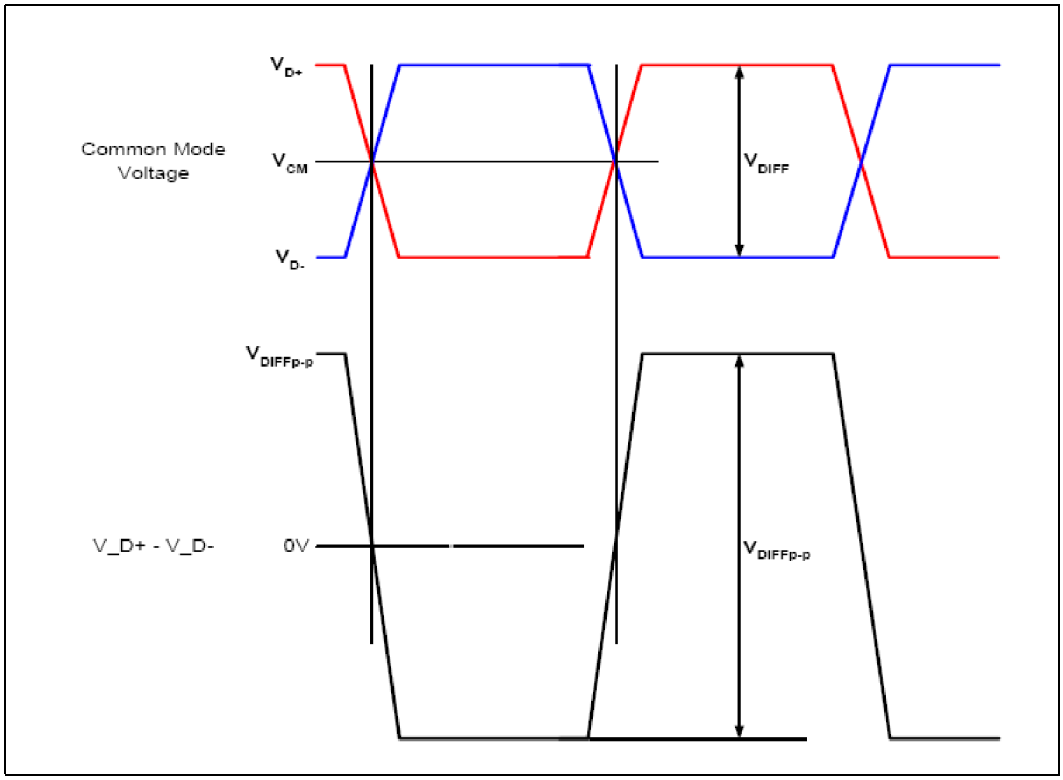
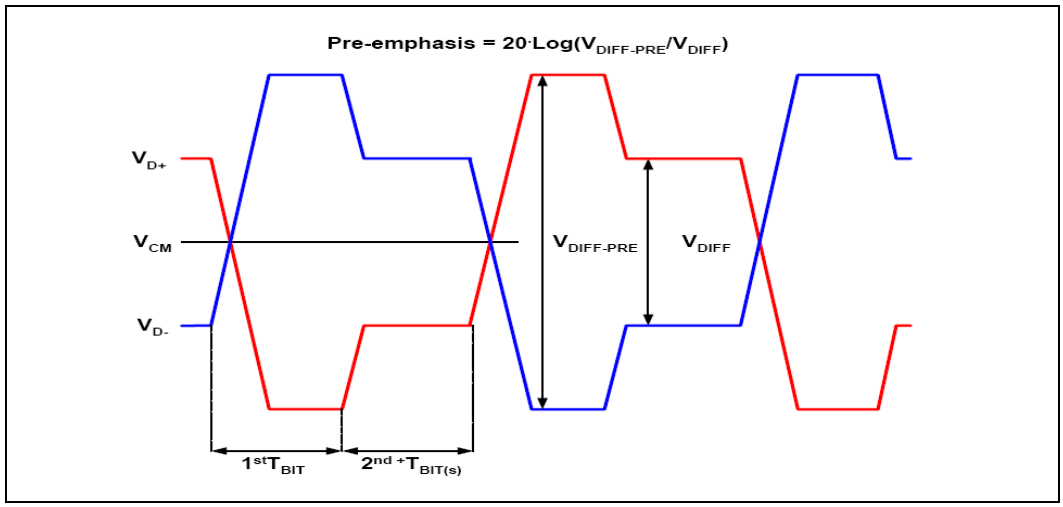


Figure 11. Definition of Pre-emphasis



8.5.2 PCI Express* DC Specification

Table 63. PCI Express* DC Receive Signal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{RXDIFF\ Gen1}$	Differential RX Peak to Peak	175		1200	mV	1
$V_{RXDIFF\ Gen2}$	Differential RX Peak to Peak	100		1200	mV	1

NOTE:
1. PCI Express differential peak to peak = 2*|RXp[x] – RXn[x]|

Table 64. PCI Express DC Transmit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{TXDIFF}	Differential TX Peak to Peak	800		1200	mV	1
$V_{TXDIFF-LP}$	Differential TX Peak to Peak (low power mode)	400		1200	mV	1

NOTE: PCI Express differential peak to peak = 2*|TXp[x] – TXn[x]|

Table 65. PCI Express* DC Clock Request Input Signal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{REF}	I/O Voltage	UNCORE_V1P8_S3				
V_{IL}	Input Low Voltage			0.3*V_{REF}	V	1
V_{IH}	Input High Voltage	0.65*V_{REF}			V	1

NOTE:
1. 3.3 V refers to UNCORE_3P3_S0 for signals in the core well. See Chapter 2, "Physical Interfaces" for signal and power well association.

Table 66. TAP Signal Group DC Specification (TAP_TCK, TAP_TRSRT#, TAP_TMS, TAP_TDI)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PMC_V1P8_G3				
V_{IH}	Input High Voltage	0.8*V_{REF}			V	1
V_{IL}	Input Low Voltage			0.4*V_{REF}	V	2
Z_{pu}	Pull up Impedance			60	Ω	3
Z_{pd}	Pull down Impedance			60	Ω	3
R_{wpu}	Weak Pull Impedance	1		4	kΩ	3
R_{wpd}	Weak Pull Down Impedance	1		4	kΩ	3
$R_{wpu-40K}$	Weak Pull Up Impedance 40K	20		70	kΩ	4
$R_{wpd-40K}$	Weak Pull Down Impedance 40K	20		70	kΩ	4

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at PMC_V1P8_G3/2.
4. Rwpu_40k and Rwpd_40k are only used for TAP_TRST#.

Table 67. TAP Signal Group DC Specification (TAP_TDO)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PMC_V1P8_G3				
V_{IH}	Input High Voltage	0.8*V_{REF}			V	1
V_{IL}	Input Low Voltage			0.5*V_{REF}	V	2
Z_{pd}	Pull down Impedance			30	Ω	3
R_{wpu}	Weak Pull Impedance	1		4	kΩ	3
R_{wpd}	Weak Pull Down Impedance	1		4	kΩ	3

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at PMC_V1P8_G3/2.

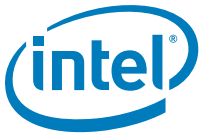


Table 68. TAP Signal Group DC Specification (TAP_PRDY#, TAP_PREQ#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PMC_V1P8_G3				
V_{IH}	Input High Voltage	0.64*V_{REF}			V	1
V_{IL}	Input Low Voltage			0.4*V_{REF}	V	2
Z_{pd}	Pull down Impedance			30	Ω	3
R_{wpu}	Weak Pull Impedance	1		4	kΩ	3

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.
3. Measured at PMC_V1P8_G3/2.

8.5.3 DDR3L Memory Controller DC Specification

Table 69. DDR3L Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input Low Voltage			DRAM_VREF – 200mV	V	1
V_{IH}	Input High Voltage	DRAM_VREF + 200mV			V	2, 3
V_{OL}	Output Low Voltage		(DRAM_VDD_S4 / 2)* (RON / (RON+RVTT_TERM))			3,4
V_{OH}	Output High Voltage		DRAM_VDD_S4 – ((DRAM_VDD_S4 /2)* (RON/(RON+RVTT_TERM))		V	3,4
I_{IL}	Input Leakage Current			5	µA	For all DRAM Signals
R_{ON}	DDR3L Clock Buffer strength	26		40	Ω	5
C_{IO}	DQ/DQS/ DQS# DDR3L IO Pin Capacitance		3.0		pF	

NOTES:
1. V_{IL} is defined as the maximum voltage level at the receiving agent that will be received as a logical low value. DRAM_VREF is normally DRAM_VDD_S4/2.
2. V_{IH} is defined as the minimum voltage level at the receiving agent that will be received as a logical high value. DRAM_VREF is normally DRAM_VDD_S4/2.
3. V_{IH} and V_{OH} may experience excursions above DRAM_VDD_S4. However, input signal drivers must comply with the signal quality specifications.
4. RON is DRAM driver resistance whereas RTT_TERM is DRAM ODT resistance which is controlled by DRAM.
5. DDR3L-1333 CLK buffer Ron is 26 ohm and SR target is 4V/ns; DQ-DQS buffer Ron is 30ohms and SR target is 4V/ns; CMD/CTL buffer Ron is 20 ohms and SR target is 1.8V/ns.

8.5.4 Intel® High Definition Audio (Intel® HD Audio) DC Specification

Table 70. HDA Signal Group DC Specifications

Symbol	Parameter	Condition	Min	Max	Unit	Notes
V_{IH_HDA}	Input High Voltage		0.7*VCC_{HDA}		V	
V_{IL_HDA}	Input Low Voltage			0.3*VCC_{HDA}	V	
V_{OH_HDA}	Output High Voltage	Iout = -500µA	0.9*VCC_{HDA}		V	
V_{OL_HDA}	Output Low Voltage	Iout = 1500µA		0.1*VCC_{HDA}	V	
IIL_HDA	Input Leakage Current	0<Vin<VCC_{HDA}		±175	µA	1
C_{IN_HDA}	Input Pin Capacitance			7.5	pF	
L_{PIN_HDA}	Pin Inductance			20	nH	2

NOTES:
1. For HDA_SDI[x] buffers (or in general any bidirectional buffer with tri-state output), input leakage current also include hi-Z output leakage.
2. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

8.5.5 USB 2.0 Host DC Specification

Table 71. USB 2.0 Host DC Specification (Sheet 1 of 3)

Symbol	Parameter	Min	Typ	Max	Units	Notes
Supply Voltage						
VBUS	High-power Port	4.75		5.25	V	2
VBUS	Low-power Port					
Supply Current						
ICCPRT	High-power Hub Port (out)	500			mA	
ICCUPT	Low-power Hub Port (out)	100			mA	
ICCHPF	High-power Function (in)			500	mA	
ICCLPF	Low-power Function (in)			100	mA	
ICCINIT	Unconfigured Function/Hub (in)			100	mA	
ICCSH	Suspended High-power Device			2.5	mA	15
ICCSL	Suspended Low-power Device			500	µA	
Input Levels for Low-/full-speed						
VIH	High (driven)	2.0			V	4
VIHZ	High (floating)	2.7		3.6	V	4
VIL	Low			0.8	V	4
VDI	Differential Input Sensitivity	0.2			V	|(D+)-(D-)|; Figure; Note 4

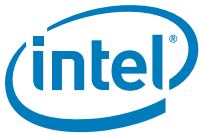


Table 71. USB 2.0 Host DC Specification (Sheet 2 of 3)

Symbol	Parameter	Min	Typ	Max	Units	Notes
VCM	Differential Common Mode Range	0.8		2.5	V	Includes VDI range; Figure; Note 4
Input Levels for High-speed						
VHSSQ	High-speed squelch detection threshold (differential signal amplitude)	100		150	mV	
VHSDSC	High speed disconnect detection threshold (differential signal amplitude)	525		625	mV	
	High-speed differential input signaling levels					
VHSCM	High-speed data signaling common mode voltage range (guideline for receiver)	-50		500	mV	
Output Levels for Low-/full-speed						
VOL	Low	0.0		0.3	V	4,5
VOH	High (Driven)	2.8		3.6	V	4,6
VOSE1	SE1	0.8			V	
VCRS	Output Signal Crossover Voltage	1.3		2.0	V	10
Output Levels for High-speed						
VHSOI	High-speed idle level	-10		10	mV	
VHSOH	High-speed data signaling high	360		440	mV	
VHSOL	High-speed data signaling low	-10		10	mV	
VCHIRPJ	Chirp J level (differential voltage)	700		1100	mV	
VCHIRPK	Chirp K level (differential voltage)	-900		-500	mV	
Decoupling Capacitance						
CHPB	Downstream Facing Port Bypass Capacitance (per hub)	120			µF	
CRPB	Upstream Facing Port Bypass Capacitance	1.0		10.0	µF	9
Input Capacitance for Low-/full-speed						
CIND	Downstream Facing Port			150	pF	2
CINUB	Upstream Facing Port (w/o cable)			100	pF	3
CEDGE	Transceiver edge rate control capacitance			75	pF	
Input Impedance for High-speed						
	TDR spec for high-speed termination					
Terminations						
RPU	Bus Pull-up Resistor on Upstream Facing Port	1.425		1.575	kΩ	1.5 kΩ ±5%
RPD	Bus Pull-down Resistor on Downstream Facing Port	14.25		15.75	kΩ	1.5 kΩ ±5%

Table 71. USB 2.0 Host DC Specification (Sheet 3 of 3)

Symbol	Parameter	Min	Typ	Max	Units	Notes
ZINP	Input impedance exclusive of pull-up/pull-down (for low-/full speed)	300			kΩ	
VTERM	Termination voltage for upstream facing port pull-up (RPU)	3.0		3.6	V	
Terminations in High-speed						
VHSTERM	Termination voltage in high speed	-10		10	mV	

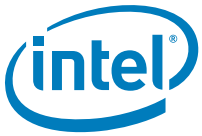
NOTES:
1. Measured at A plug.
2. Measured at A receptacle.
3. Measured at B receptacle.
4. Measured at A or B connector.
5. Measured with RL of 1.425 kΩ to 3.6 V.
6. Measured with RL of 14.25 kΩ to GND.
7. Timing difference between the differential data signals.
8. Measured at crossover point of differential data signals.
9. The maximum load specification is the maximum effective capacitive load allowed that meets the target VBUS drop of 330 mV.
10. Excluding the first transition from the Idle state.
11. The two transitions should be a (nominal) bit time apart.
12. For both transitions of differential signaling.
13. Must accept as valid EOP.
14. Single-ended capacitance of D+ or D- is the capacitance of D+/D- to all other conductors and, if present, shield in the cable. That is, to measure the single-ended capacitance of D+, short D-, VBUS, GND, and the shield line together and measure the capacitance of D+ to the other conductors.
15. For high power devices (non-hubs) when enabled for remote wakeup.

8.5.6 USB 3.0 DC Specification

Table 72. USB 3.0 DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	199.94		200.06	ps	1
$V_{TX-DIFF-PP}$	Differential peak-peak Tx voltage swing	0.9	1	1.05	V	
$V_{TX-DIFF-PP-LOW}$	Low-Power Differential peak-peak Tx voltage swing	0.4		1.2	V	2
$V_{TX-DE-RATIO}$	Tx De-Emphasis	3.45	3.5	3.65	dB	
$R_{TX-DIFF-DC}$	DC differential impedance	88		92	Ω	
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection			0.6	V	3
$C_{AC-COUPLING}$	AC Coupling Capacitor	75		200	nF	4
$t_{CDR\_SLEW\_MAX}$	Maximum slew rate			10	ms/s	

NOTES:
1. The specified UI is equivalent to a tolerance of 300ppm for each device. Period does not account for SSC induced variations.
2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode.
3. Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an “off” receiver's input goes below output.
4. All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.



8.5.7 SATA DC Specification

Table 73. SATA TX/RX Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IMIN_Gen1i}	Minimum Input Voltage for 1.5 Gb/s	325	-	mVdiffp-p	1
V_{IMAX_Gen1i}	Maximum Input Voltage for 1.5 Gb/s	-	600	mVdiffp-p	1
V_{IMIN_Gen2i}	Minimum Input Voltage for 3 Gb/s	275	-	mVdiffp-p	2
V_{IMAX_Gen2i}	Maximum Input Voltage for 3 Gb/s	-	750	mVdiffp-p	2
$V_{OMIN\_Gen1i,m}$	Minimum Output Voltage for 1.5 Gb/s	400	-	mVdiffp-p	3
$V_{OMAX\_Gen1i,m}$	Maximum Output Voltage for 1.5 Gb/s	-	600	mVdiffp-p	3
$V_{OMIN\_Gen2i,m}$	Minimum Output Voltage for 3 Gb/s	400	-	mVdiffp-p	3
$V_{OMAX\_Gen2i,m}$	Maximum Output Voltage for 3 Gb/s	-	700	mVdiffp-p	3

NOTE:
1. Applicable only when SATA port signaling rate is 1.5 Gb/s: SATA Vdiff, rx is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA_RXP[x] – SATA_RXN[x]|
2. Applicable only when SATA port signaling rate is 3 Gb/s: SATA Vdiff, rx is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA_RXP[x] – SATA_RXN[x]|
3. SATA Vdiff, tx is measured at the SATA connector on the transmit side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA_TXP[x] – SATA_TXN[x]|

For SATA_GP[x], SATA_DEVSLP[x] and SATA_LED#, refer to the GPIO Buffer (1.8V) DC Specification in section "GPIO DC Specification".

8.5.8 PCU – SMBus DC Specification

For SMBus, refer to the GPIO Buffer (1.8V) DC Specification in section "GPIO DC Specification".

8.5.9 PCU – iLB – LPC DC Specification

Table 74. LPC Signal Group DC Specification (LPC_V1P8V3P3_S3 = 1.8V (ILB_LPC_AD][3:0], ILB_LPC_FRAME#, ILB_LPC_SERIRQ, ILB_LPC_CLKRUN#))

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	1.27	1.8	1.8 +0.1	V	
V_{IL}	Input Low Voltage	-0.1	0	0.58	V	
V_{OH}	Output High Voltage	0.9 x 1.8			V	
V_{OL}	Output Low Voltage			0.1 x 1.8	V	
I_{OH}	Output High Current		1.5		mA	
I_{OL}	Output Low Current		-0.5		mA	
I_{LEAK}	Input Leakage Current			30	µA	
C_{IN}	Input Capacitance	1		9	pF	

Table 75. LPC Signal Group DC Specification LPC_V1P8V3P3_S3 = 3.3V (ILB_LPC_AD[3:0], ILB_LPC_FRAME#, ILB_LPC_CLKRUN#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	0.5 x 3.3+ 0.7	3.3	3.3 +0.1	V	1
V_{IL}	Input Low Voltage	-0.1	0	0.5 x 3.3 - 0.7	V	2
V_{OH}	Output High Voltage	0.9 x 3.3			V	3
V_{OL}	Output Low Voltage			0.1 x 3.3	V	3
I_{OH}	Output High Current		1.5		mA	3
I_{OL}	Output Low Current		-0.5		mA	3
I_{LEAK}	Input Leakage Current			30	µA	
C_{IN}	Input Capacitance	1		9	pF	

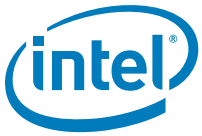
NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value, Applies to ILB_LPC_AD[3:0], ILB_LPC_CLKRUN#
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value. Applies to ILB_LPC_AD[3:0], ILB_LPC_CLKRUN#
3. V_{OH} is tested with Iout=500uA, V_{OL} is tested with Iout=1500uA
4. Applies to ILB_LPC_AD[3:0],ILB_LPC_CLKRUN# and ILB_LPC_FRAME#
5. ILB_LPC_SERIRQ is always a 1.8V I/O irrespective of the value of LPC_V1P8V3P3_S3.

8.5.10 PCU – SPI (Platform Control Unit) DC Specification

Table 76. SPI Signal Group DC Specification (PCU_SPI_MISO, PCU_SPI_CS[1:0]#, PCU_SPI_MOSI, PCU_SPI_CLK)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PCU_1P8_G3			V	3
V_{IH}	Input High Voltage	0.5 *V_{REF}		V_{REF} + 0.5	V	2
V_{IL}	Input Low Voltage	-0.5		0.3 * V_{REF}	V	2
V_{OH}	Output High Voltage	0.9 * V_{REF}		1.8V	V	1
V_{OL}	Output Low Voltage			0.1 * V_{REF}	V	1
I_{OH}	Output High Current			1.5	mA	1
I_{OL}	Output Low Current	-0.5			mA	1

NOTES:
1. Applies to PCU_SPI_CS[1:0], PCU_SPI_CLK, PCU_SPI_MOSI
2. Applies to PCU_SPI_MISO and PCU_SPI_MOSI
3. The I/O buffer supply voltage is measured at the processor package pins. The tolerances shown are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a rolloff of 3 dB/decade above 20 MHz.



8.5.11 PCU – Power Management/Thermal (PMC) and iLB RTC DC Specification

Table 77. Power Management 1.8V Suspend Well Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PCU_1P8_G3			V	
V_{IH}	Input High Voltage	0.8*V_{REF}			V	1
V_{IL}	Input Low Voltage			0.5*V_{REF}	V	2
V_{OH}	Output High Voltage	0.9*V_{REF}		V_{REF}	V	1
V_{OL}	Output Low Voltage			0.1*V_{REF}	V	1

NOTES:
1. The data in this table apply to signals - PMC_ACPRESENT, PMC_BATLOW#, PMC_PLTRST#, PMC_PWRBTN#, PMC_SLP_S3#, PMC_SLP_S4#, PMC_SUS_STAT#, PMC_SUSCLK[3:0], PMC_SUSPWRDNACK, PMC_WAKE_PCIE[0:3]#
2. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
3. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 78. PMC_RSTBTN# 1.8V Core Well Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
VREF	I/O Voltage	UNCORE_V1P8_S3			V	
V_{IH}	Input High Voltage	0.8* VREF			V	1
V_{IL}	Input Low Voltage			0.5* VREF	V	2

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 79. Power Management & RTC Well Signal Group DC Specification (PMC_RSMRST#, PMC_CORE_PWROK, ILB_RTC_RST#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
VREF	I/O Voltage	RTC_VCC				
V_{IH}	Input High Voltage	2.0	-	-	V	1
V_{IL}	Input Low Voltage	-	-	0.78	V	2

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 80. iLB RTC Well DC Specification (ILB_RTC_TEST#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	2.3	-	-	V	1
V_{IL}	Input Low Voltage	-	-	0.78	V	1

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

Table 81. ILB RTC Oscillator Optional DC Specification (ILB_RTC_X1)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IH}	Input High Voltage	0.65	0.8	1.2	V	1
V_{IL}	Input Low Voltage			0.25	V	1

NOTES:
1. ILB_RTC_X1 DC specification is **only** used for applications with an active external clock source instead of a crystal. When a crystal is used (typical case) between ILB_RTC_X2 and ILB_RTC_X1, this specification is not used.

Table 82. PROCHOT# Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	CORE_V1P0_S3				
V_{IH}	Input High Voltage	$0.8*V_{REF}$		V_{REF}	V	1
V_{IL}	Input Low Voltage			$0.4*V_{REF}$	V	2
V_{OH}	Output High Voltage	$0.9*V_{REF}$		V_{REF}	V	
V_{OL}	Output Low Voltage			$0.1*V_{REF}$	V	

NOTES:
1. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
2. V_{IL} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical low value.

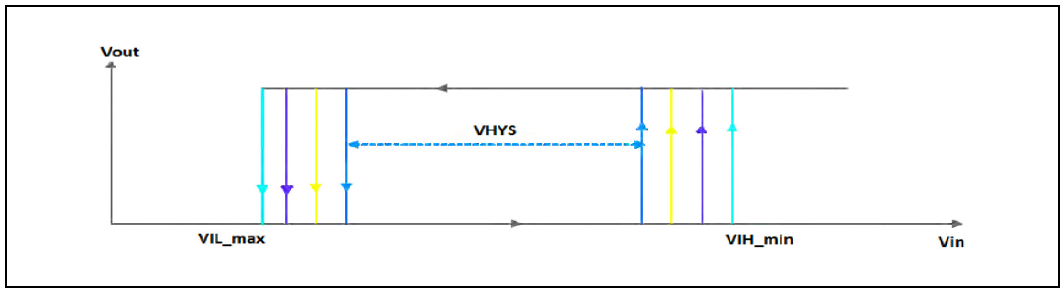
8.5.12 SVID DC Specification

Table 83. SVID Signal Group DC Specification (SVID_DATA, SVID_CLK, SVID_ALERT#)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	SVID_V1P0_S3				
V_{IH}	Input High Voltage	0.65*V_{REF}			V	1
V_{IL}	Input Low Voltage			0.44*V_{REF}	V	1
V_{OH}	Output High Voltage				V	1
V_{OL}	Output Low Voltage			0.1*V_{REF}	V	4
V_{HYS}	Hysteresis Voltage	0.05			V	
R_{ON}	BUffer on Resistance	10		20	Ω	2
I_L	Leakage Current	-100		100	µA	3
C_{PAD}	Pad Capacitance			4.0	pF	4
V_{PIN}	Pin Capacitance			5.0	pF	

NOTES:
1. SVID_V1P0_S3 refers to instantaneous voltage VSS_SENSE
2. Measured at 0.31 * SVID_V1P0_S3
3. V_{IN} between 0V and SVID_V1P0_S3
4. CPAD includes die capacitance only. No package parasitic included.

Figure 12. Definition of VHYS in Table 169



8.5.13 GPIO DC Specification

GPIO Buffer is used across various interfaces on the processor such as, GPIOs, SPI, SVID, UART, JTAG and ULPI.

Table 84. GPIO 1.8V Core Well Signal Group DC Specification (GPIO_S0_SC[101:0])

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	UNCORE_V1P8_S3				
V_{IH}	Input High Voltage	0.65*V_{REF}			V	
V_{IL}	Input Low Voltage			0.35 * V_{REF}	V	
V_{OH}	Output High Voltage	V_{REF} – 0.45			V	
V_{OL}	Output Low Voltage			0.45	V	

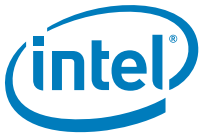
Table 84. GPIO 1.8V Core Well Signal Group DC Specification (GPIO_S0_SC[101:0])

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{Hys}	Input Hysteresis	0.1			V	
I_L	Leakage Current			5	µA	
C_{LOAD}	Load Capacitance	2		75	pF	

Table 85. GPIO 1.8V Suspend Well Signal Group DC Specification (GPIO_S5[43:0])

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{REF}	I/O Voltage	PMC_V1P8_G3			V	
V_{IH}	Input High Voltage	$0.65*V_{REF}$			V	
V_{IL}	Input Low Voltage			$0.35*V_{REF}$	V	
V_{OH}	Output High Voltage	V_{REF} – 0.45			V	
V_{OL}	Output Low Voltage			0.45	V	
V_{Hys}	Input Hysteresis	0.1			V	
I_L	Leakage Current			5	µA	
C_{LOAD}	Load Capacitance	2		75	pF	

§



9 Package Information

The processor comes in a **25 mm X 27 mm** Flip-Chip Ball Grid Array (FCBGA) package and consists of a silicon die mounted face down on an organic substrate populated with 1170 solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out zone, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

9.1 Processor Attributes

- Package parameters: 25 mm X 27 mm
- Ball Count:1170

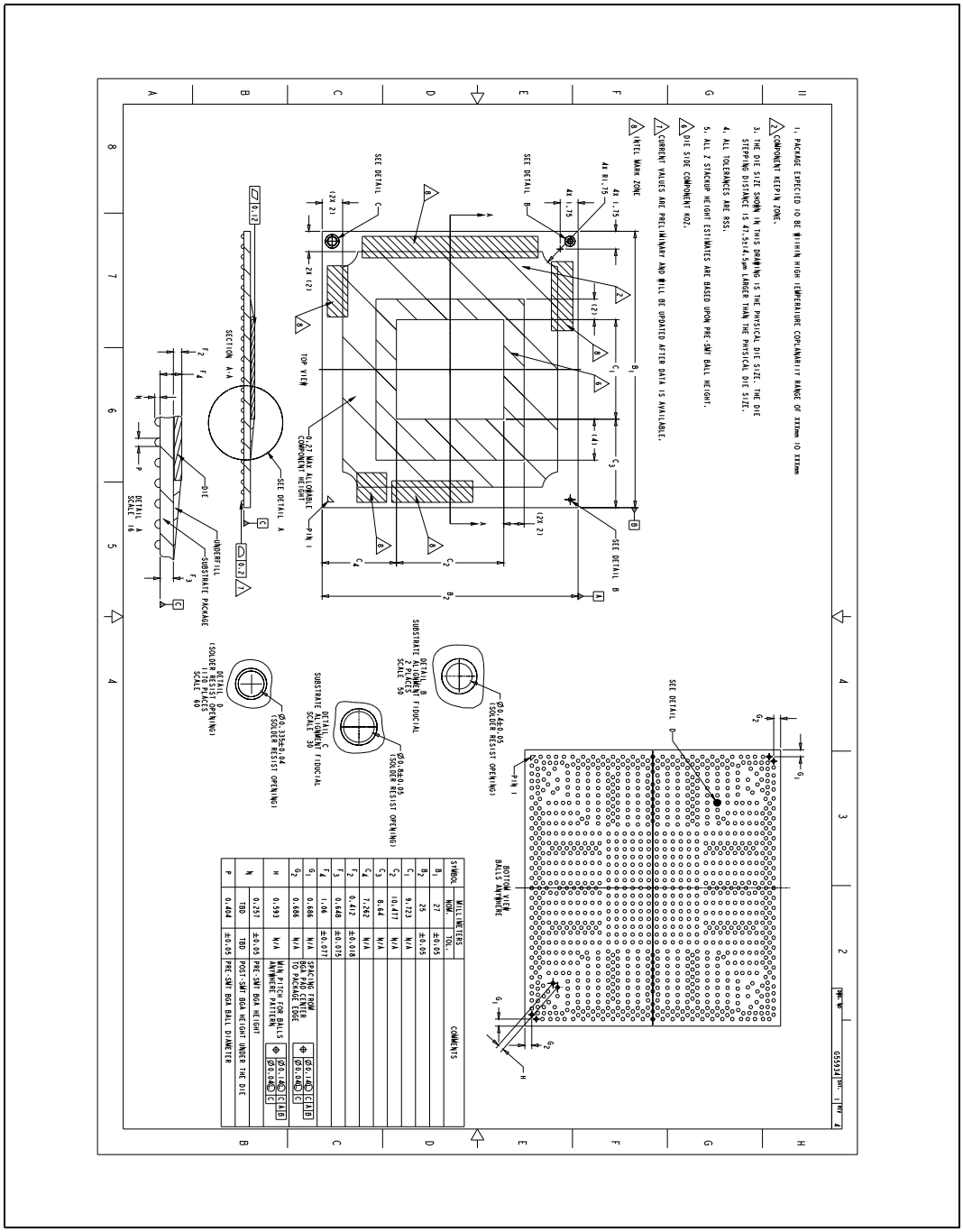
All Units: mm

Tolerances if not specified:

- .X: ± 0.1
- .XX: ± 0.05
- Angles: ± 1.0 degrees

9.2 Package Diagrams

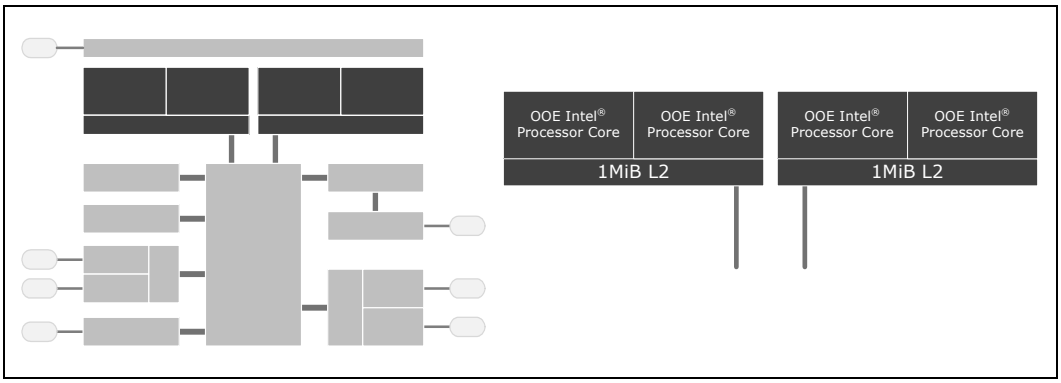
Figure 13. Package Mechanical Drawing



§

10 Processor Core

Up to four out-of-order execution processor cores are supported, each dual core module supports up to 1 MiB of L2 cache.



10.1 Features

- Dual or Quad Out-of-Order Execution (OOE) processor cores
- Primary 32 KiB, 8-way L1 instruction cache and 24 KiB, 6-way L1 write-back data cache
- Cores are grouped into dual-core modules: modules share a 1 MiB, 16-way L2 cache (2 MiB total for Quad Core, 1MiB total for Dual Core)
- Intel® Streaming SIMD Extensions 4.1 and 4.2 (SSE4.1 and SSE4.2), which include new instructions for media and for fast XML parsing
- Intel® 64 architecture
- Support for IA 32-bit
- Support for Intel® VT-x
- Support for Intel® Carry-Less Multiplication Instruction (PCLMULQDQ)
- Support for a Digital Random Number Generator (DRNG)
- Supports C0, C1, C6, C7 states

Note:

- Thermal management support using Intel® Thermal Monitor (TM1 & TM2)
- Uses Power Aware Interrupt Routing (PAIR)
- Uses 22 nm process technology

Note: Intel® Hyper-Threading Technology is not supported.

10.1.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

Intel® VT-x specifications and functional descriptions are included in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B* and is available at: http://www.intel.com/products/processor/manuals/index.htm

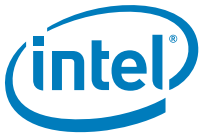
Other Intel® VT documents can be referenced at: http://www.intel.com/technology/virtualization/index.htm

10.1.1.1 Intel® VT-x Objectives

- Robust: VMMs no longer need to use paravirtualization or binary translation. This means that they will be able to run off-the-shelf OSs and applications without any special steps.
- Enhanced: Intel® VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- More reliable: Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- More secure: The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system. Intel® VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel® VT-x features to provide improved reliable virtualized platform.

10.1.1.1.1 Intel® VT-x Features

- Extended Page Tables (EPT)
  - EPT is hardware assisted page table physical memory virtualization
  - Support guest VM execution in unpaged protected mode or in real-address mode
  - It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
  - A VM Virtual Processor ID is used to tag processor core hardware structures (such as TLBs) to allow a logic processor to cache information (such as TLBs) for multiple linear address spaces
  - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead



- Guest Preemption Timer
  - Mechanism for a VMM to preempt the execution of a guest OS VM after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest.
  - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees flexibility in guest VM scheduling and building Quality of Service (QoS) schemes
- Descriptor-Table Exiting
  - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector)
  - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software
- VM Functions
  - A VM function is an operation provided by the processor that can be invoked using the VMFUNC instruction from guest VM without a VM exit
  - A VM function to perform EPTP switching is supported and allows guest VM to load a new value for the EPT pointer, thereby establishing a different EPT paging structure hierarchy

10.1.2 Security and Cryptography Technologies

10.1.2.1 PCLMULQDQ Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two, 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

10.1.2.2 Digital Random Number Generator

The processor introduces a software visible digital random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the new RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards (ANSI X9.82 and NIST SP 800-90).

Some possible uses of the new RDRAND instruction include cryptographic key generation as used in a variety of applications including communication, digital signatures, secure storage, etc.

10.1.3 Power Aware Interrupt Routing

PAIR is an improvement in H/W routing of "redirectable" interrupts. Each core power-state is considered in the routing selection to reduce the power or performance impact of interrupts. System BIOS configures the routing algorithm, e.g. fixed-priority, rotating, hash, or PAIR, during setup via non-architectural register. The PAIR algorithm can be biased to optimize for power or performance and the largest gains will be seen in systems with high interrupt rates.

10.2 Platform Identification and CPUID

In addition to verifying the processor signature, the intended processor platform type must be determined to properly target the microcode update. The intended processor platform type is determined by reading bits [52:50] of the IA32_PLATFORM_ID register, (MSR 17h) within the processor. This is a 64-bit register that must be read using the RDMSR instruction. The 3 Platform Id bits, when read as a binary coded decimal (BCD) number, indicate the bit position in the microcode update header's Processor Flags field that is asSoCiated with the installed processor.

Executing the CPUID instruction with EAX=1 will provide the following information.

EAX	Field description
[31:28]	Reserved
[27:20]	Extended Family value
[19:16]	Extended Model value
[15:13]	Reserved
[12]	Processor Type Bit
[11:8]	Family value
[7:4]	Model value
[3:0]	Stepping ID Value

10.3 References

For further details of Intel® 64 and IA-32 architectures, refer to Intel® 64 and IA-32 Architectures Software Developer's Manual Combined Volumes:1, 2A, 2B, 2C, 3A, 3B, and 3C:

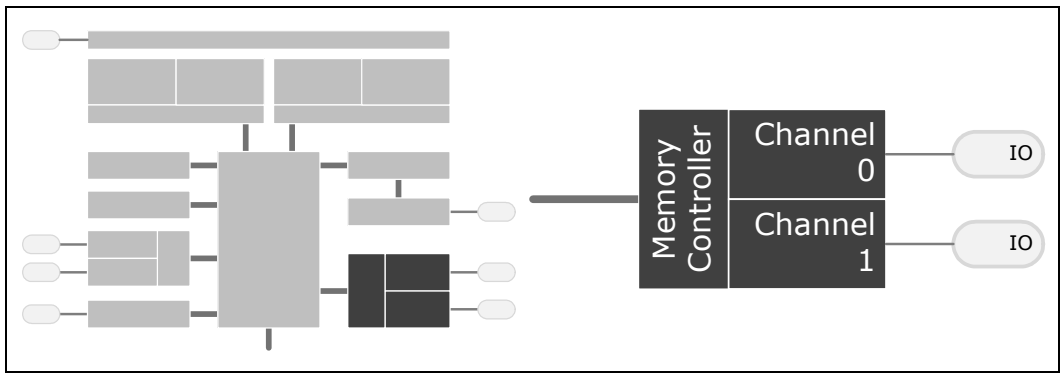
- http://www.intel.com/content/www/µs/en/processors/architectures-software-developer-manuals.html

§

10.4 System Memory Controller

The system memory controller supports DDR3L protocol with up to two 64-bit wide dual rank channels at data rates up to 1333 MT/s.

Note: The memory data rate is fixed for each SKU. Example, for processor supporting 1333 MT/s, only memory devices with 1333 MT/s is supported. For single channel use cases, Channel 0 must be used.



10.5 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 87. Memory Channel 0 DDR3L Signals (Sheet 1 of 2)

Signal Name	Direction Type	Description
DRAM0_CKP[2,0] DRAM0_CKN[2,0]	O DDR3	**SDRAM and inverted Differential Clock:** (1 pair per Rank) The differential clock pair is used to latch the command into DRAM. Each pair corresponds to one rank on DRAM side.
DRAM0_CS[2,0]#	O DDR3	**Chip Select:** (1 per Rank). Used to qualify the command on the command bus for a particular rank.
DRAM0_CKE[2,0]	O DDR3	**Clock Enable:** (power management) It is used during DRAM power up/power down and Self refresh. **Note:** DDR3L uses only DRAM0_CKE[2,0]. DRAM0_CKE[1,3] are not being used for DDR3L.
DRAM0_MA[15:0]	O DDR3	**Memory Address:** Memory address bus for writing data to memory and reading data from memory. These signals follow common clock protocol w.r.t. DRAM0_CKN, DRAM0_CKP pairs

Table 87. Memory Channel 0 DDR3L Signals (Sheet 2 of 2)

Signal Name	Direction Type	Description
DRAM0_BS[2:0]	O DDR3	**Bank Select:** These signals define which banks are selected within each DRAM rank
DRAM0_RAS#	O DDR3	**Row Address Select:** Used with DRAM0_CAS# and DRAM0_WE# (along with DRAM0_CS#) to define the DRAM Commands
DRAM0_CAS#	O DDR3	**Column Address Select:** Used with DRAM0_RAS# and DRAM0_WE# (along with DRAM0_CS#) to define the SRAM Commands
DRAM0_WE#	O DDR3	**Write Enable Control Signal:** Used with DRAM0_WE# and DRAM0_CAS# (along with control signal, DRAM0_CS#) to define the DRAM Commands.
DRAM0_DQ[63:0]	I/O DDR3	**Data Lines:** Data signal interface to the DRAM data bus
DRAM0_DM[7:0]	O DDR3	**Data Mask:** DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
DRAM0_DQSP[7:0] DRAM0_DQSN[7:0]	I/O DDR3	**Data Strobes:** The data is captured at the crossing point of each 'P' and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
DRAM0_ODT[2,0]	O DDR3	**On Die Termination:** ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.
DRAM_RCOMP[2]	O Analog	**Resistor Compensation:** This signal needs to be terminated to VSS on board. This external resistor termination scheme is used for Resistor compensation of DRAM ODT strength.
DRAM_RCOMP[1]	O Analog	**Resistor Compensation:** This signal needs to be terminated to VSS on board. This external resistor termination scheme is used for Resistor compensation of DQ buffers
DRAM_RCOMP[0]	O Analog	**Resistor Compensation:** This signal needs to be terminated to VSS on board. This external resistor termination scheme is used for Resistor compensation of CMD buffers.
DRAM_VREF	I Analog	**Reference Voltage:** DRAM interface Reference Voltage
DRAM_CORE_PWROK	I Asynchronous CMOS	**Core Power OK:** This signal indicates the status of the DRAM Core power supply (power on in S0).
DRAM_VDD_S4_PWROK	I Asynchronous CMOS	**VDD Power OK:** Asserted once the VRM is settled. Used primarily in the DRAM PHY to determine S3 state.
DRAM0_DRAMRST#	O	**DRAM Reset:** This signal is used to reset DRAM devices.
ICLK_DRAM_TERM [1:0]	I/O	Pull-down to VSS through an 100kOhm 1% resistor.

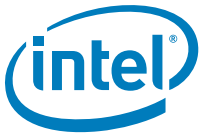


Table 88. Memory Channel 1 DDR3L Signals

Signal Name	Direction Type	Description
DRAM1_CKP[2,0] DRAM1_CKN[2,0]	O DDR3	**SDRAM and inverted Differential Clock:** (1 pair per Rank) The differential clock pair is used to latch the command into DRAM. Each pair corresponds to one rank on DRAM side.
DRAM1_CS[2,0]#	O DDR3	**Chip Select:** (1 per Rank). Used to qualify the command on the command bus for a particular rank.
DRAM1_CKE[2,0]	O DDR3	**Clock Enable:** (power management) It is used during DRAM power up/power down and Self refresh. **Note:** DDR3L uses only DRAM1_CKE[0,2]. DRAM1_CKE[1,3] are not being used for DDR3L.
DRAM1_MA[15:0]	O DDR3	**Memory Address:** Memory address bus for writing data to memory and reading data from memory. These signals follow common clock protocol relative to DRAM1_CKN, DRAM1_CKP pairs
DRAM1_BS[2:0]	O DDR3	**Bank Select:** These signals define which banks are selected within each DRAM rank
DRAM1_RAS#	O DDR3	**Row Address Select:** Used with DRAM1_CAS# and DRAM1_WE# (along with DRAM1_CS#) to define the DRAM Commands
DRAM1_CAS#	O DDR3	**Column Address Select:** Used with DRAM1_RAS# and DRAM1_WE# (along with DRAM1_CS#) to define the SRAM Commands
DRAM1_WE#	O DDR3	**Write Enable Control Signal:** Used with DRAM1_WE# and DRAM1_CAS# (along with control signal, DRAM1_CS#) to define the DRAM Commands.
DRAM1_DQ[63:0]	I/O DDR3	**Data Lines:** Data signal interface to the DRAM data bus.
DRAM1_DM[7:0]	O DDR3	**Data Mask:** DM is an output mask signal for write data. Output data is masked when DM is sampled HIGH coincident with that output data during a Write access. DM is sampled on both edges of DQS.
DRAM1_DQSP[7:0] DRAM1_DQSN[7:0]	I/O DDR3	**Data Strobes:** The data is captured at the crossing point of DRAM1_DQSP[7:0] and its compliment 'N' during read and write transactions. For reads, the strobe crossover and data are edge aligned, whereas in the Write command, the strobe crossing is in the centre of the data window.
DRAM1_ODT[2,0]	O DDR3	**On Die Termination:** ODT signal going to DRAM in order to turn ON the DRAM ODT during Write.
DRAM1_DRAMRST#	O	**Reset DRAM:** This signal can be used to reset DRAM devices.

10.6 Features

10.6.1 System Memory Technology Supported

The system memory controller supports the following DDR3L, DRAM technologies, Data Transfer Rates, SO-DIMM Modules and other features:

- DDR3L Data Transfer Rates (Fixed per SKU): 1066MT/s (8.5 GB/s per channel) or 1333MT/s (10.6 GB/s per channel)
- DDR3L SDRAM (1.35 V DRAM interface I/Os, including DDR3L)
- DDR3L SO-DIMM Modules (unbuffered)
  - — Raw Card A = 2 rank of x16 SDRAM (double sided)
  - — Raw Card B = 1 rank of x8 SDRAM (double sided)

  - Raw Card C = 1 rank of x16 SDRAM (single sided)
  - Raw Card F = 2 ranks of x8 SDRAM (double sided)
  - No mixed Raw Card support
  - Refer to design guidelines for platform supportable memory configurations and limitations based on layout and firmware initialization (MRC) requirements
- DDR3L DRAM Device Technology
  - Standard 1Gb, 2Gb and 4Gb technologies and addressing.
  - Read latency 5, 6, 7, 8, 9, 10, 11
  - Write latency 5, 6, 7, 8
- Support Trunk Clock Gating
- Support channel 0 only for single channel configuration
- Support early SR exit
- Support slow power down
- Supported DDR3L SO-DIMM module configurations:

"Single sided" above is a logical term referring to the number of chip selects attached to the SO-DIMM. A real SO-DIMM may put the components on both sides of the substrate, but be logically indistinguishable from single sided SO-DIMM if all components on the SO-DIMM are attached to the same chip select signal.

10.6.2 System Memory Technology Support

There is no support for SO-DIMMs with different technologies or capacities on opposite sides of the same SO-DIMM. If one side of a SO-DIMM is populated, the other side is either identical or empty.

Table 89. Supported DDR3L DRAM Devices

DRAM Density	Data Width	Banks	Bank Address	Row Address	Column Address	Page Size
1Gb	x8	8	BA[2:0]	A[13:0]	A[9:0]	1KB
2Gb	x8	8	BA[2:0]	A[14:0]	A[9:0]	1KB
4Gb	x8	8	BA[2:0]	A[15:0]	A[9:0]	1KB
1Gb	x16	8	BA[2:0]	A[12:0]	A[9:0]	2KB
2Gb	x16	8	BA[2:0]	A[13:0]	A[9:0]	2KB
4Gb	x16	8	BA[2:0]	A[14:0]	A[9:0]	2KB
8Gb	x16	8	BA[2:0]	A[15:0]	A[9:0]	2KB

Table 90. Supported DDR3L Memory Size Per Rank (Sheet 1 of 2)

Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus
1GB	8	1Gb	x8	8KB = 1KB * 8 chips
2GB	8	2Gb	x8	8KB = 1KB * 8 chips
4GB	8	4Gb	x8	8KB = 1KB * 8 chips

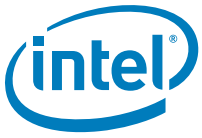


Table 90. Supported DDR3L Memory Size Per Rank (Sheet 2 of 2)

Memory Size/ Rank	DRAM Chips/ Rank	DRAM Chip Density	DRAM Chip Data Width	Page Size @ 64-bit Data Bus
8GB	8	8Gb	x8	16KB = 2KB * 8 chips
512MB	4	1Gb	x16	8KB = 2KB * 4 chips
1GB	4	2Gb	x16	8KB = 2KB * 4 chips
2GB	4	4Gb	x16	8KB = 2KB * 4 chips
4GB	4	8Gb	x16	8KB = 2KB * 4 chips

Table 91. Supported DDR3L SO-DIMM Size

DRAM Chip Density	Module Size	# of chips needed	DRAM Chip Data Width	Data Bus Width	# of Ranks needed	# of chips / rank
1Gbit	512MB	4	x16	x64	1	4
1Gbit	1GB	8	x8	x64	1	8
1Gbit	1GB	8	x16	x64	2	4
1Gbit	2GB	16	x8	x64	2	8
2Gbit	1GB	4	x16	x64	1	4
2Gbit	2GB	8	x8	x64	1	8
2Gbit	2GB	8	x16	x64	2	4
2Gbit	4GB	16	x8	x64	2	8
4Gbit	2GB	4	x16	x64	1	4
4Gbit	4GB	8	x8	x64	1	8
4Gbit	4GB	8	x16	x64	2	4
4Gbit	8GB	16	x8	x64	2	8
8Gbit	4GB	4	x16	x64	1	4
8Gbit	8GB	8	x16	x64	2	4
8Gbit	8GB	8	x8	x64	1	8

The frequency of system memory is fixed based on SKU. Timing parameters (CAS latency or CL + AL for DDR3, tRAS, tRCD, tRP) must be programmed to match within a channel (Contact your Intel field representative for more information on memory reference code (MRC)). The controller supports these configurations:

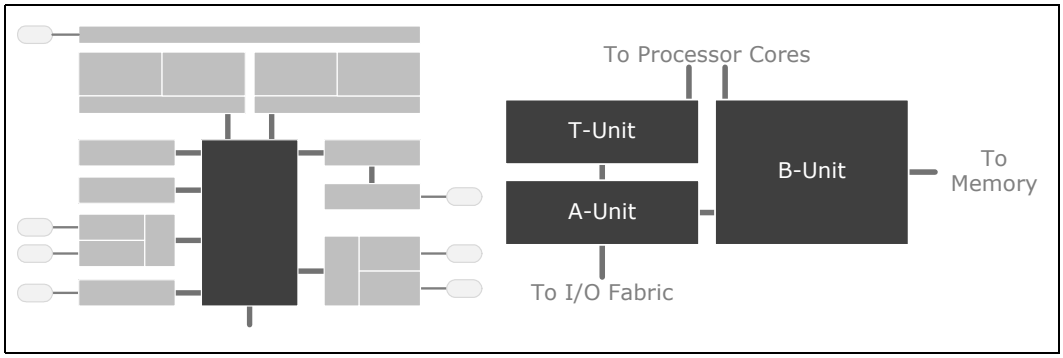
- Supports 1 SO-DIMM per channel.
- Each SO-DIMM can have 1 or 2 ranks.
- If a SO-DIMM has two ranks, then both ranks must be symmetrical (same chip width, same chip density, and same total memory size per rank).
- For dual channel population, the two channels must be populated symmetrically (chip width, density, ranks).
- The maximum total memory supported by the processor is 8 GB.

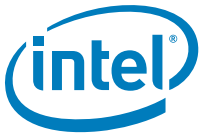
§

11 Processor Transaction Router

The Processor Transaction Router is a central hub that routes transactions between the processor cores, graphics controller, IO, and the memory controller. In general, it handles:

- Processor Core Interface: Requests for processor Core-initiated memory and IO read and write operations and processor-initiated message-signaled interrupt transactions
- Device MMIO and PCI configuration routing
- Buffering and memory arbitration
- PCI Configuration and MMIO accesses to host device (0/0/0)





11.1 Transaction Router C-Unit PCI Configuration Registers

Table 92. Summary of Transaction Router PCI Configuration Registers—0/0/0

Offset	Size	Register ID—Description	Default Value
0h	1	"CUNIT_REG_DEVICEID—Offset 0h" on page 119	00008086h
4h	1	"CUNIT_CFG_REG_PCISTATUS—Offset 4h" on page 120	00000007h
8h	1	"CUNIT_CFG_REG_CLASSCODE—Offset 8h" on page 120	06000000h
Ch	1	"CUNIT_CFG_REG_HDR_TYPE—Offset Ch" on page 121	00000000h
2Ch	1	"CUNIT_CFG_REG_STRAP_SSID—Offset 2Ch" on page 121	00000000h
F8h	1	"CUNIT_MANUFACTURING_ID—Offset F8h" on page 122	00000000h

11.1.1 CUNIT_REG_DEVICEID—Offset 0h

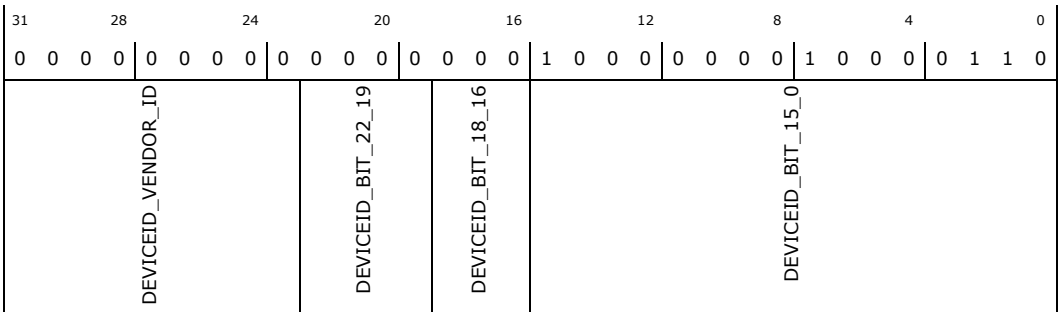
CUnit Configuration Register Device ID/Vendor ID. Device ID and Vendor ID Strapped in from top level. Reset value to strapDID[15:3],fuse[2:0], 16'h8086 these bits can be re-written from SETIDVALUE message 1st DW data byte 2, byte 3

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CUNIT_REG_DEVICEID: [B:0, D:0, F:0] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:23	0h RW	**DEVICEID_VENDOR_ID:** Device ID and Vendor ID bit [15:7] are strapped in from top level. These bits can be re-written from SETIDVALUE message 1st DW data byte 2, byte 3. for VLV/VLV2, final setting of this field is from SETIDVALUE message, while for TNG it uses the strapped setting. For all processor's, the RDL default is set to the strapped setting in that processor. Please refer to the processor documentation to determine the proper Device ID for the chip.
22:19	0h RO	**DEVICEID_bit_22_19 (DEVICEID_BIT_22_19):** Device ID [6:3] Hardwired in the design. SETIDVALUE message will not re-write this field. RDL default is set to the strapped value
18:16	0h RO	**DEVICEID_bit_18_16 (DEVICEID_BIT_18_16):** Device ID [2:0]. Strapped in from top level and tied to fuses to determine product SKU. SETIDVALUE message will not re-write this field.
15:0	8086h RO	**DEVICEID_bit_15_0 (DEVICEID_BIT_15_0):** Hardwired

11.1.2 CUNIT_CFG_REG_PCISTATUS—Offset 4h

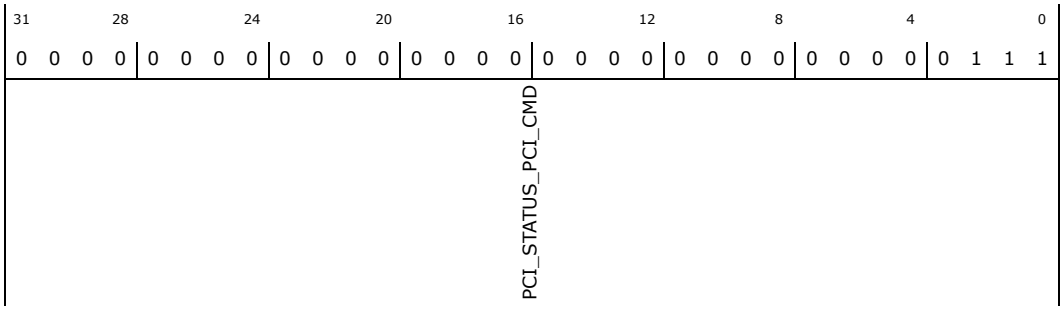
CUnit Configuration Register Device ID/Vendor ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CUNIT_CFG_REG_PCISTATUS: [B:0, D:0, F:0] + 4h

Default: 00000007h



Bit Range	Default & Access	Description
31:0	00000007h RO	**PCI_STATUS_PCI_CMD:** PCI Status and PCI Command. Hardwired to 32'h00000007

11.1.3 CUNIT_CFG_REG_CLASSCODE—Offset 8h

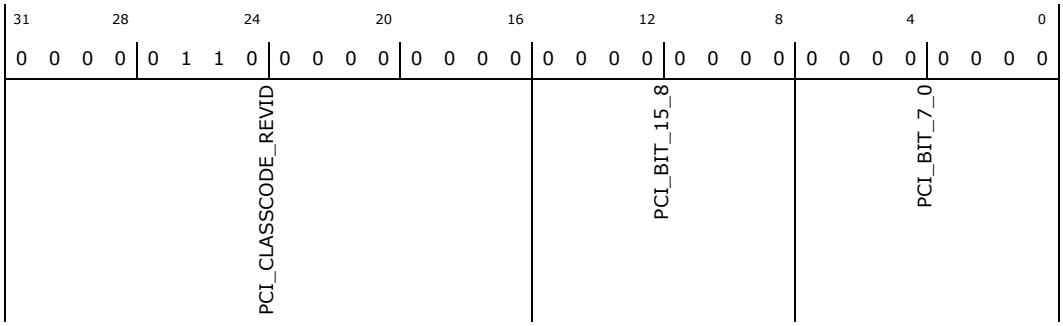
CUnit Configuration register Header Type and Master Latency Time

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CUNIT_CFG_REG_CLASSCODE: [B:0, D:0, F:0] + 8h

Default: 06000000h



Bit Range	Default & Access	Description
31:16	0600h RO	**PCI_CLASSCODE_REVID:** PCI Class Code
15:8	00h RO	**PCI_BIT_15_8:** Hardwired to 8'h00

Bit Range	Default & Access	Description
7:0	0h RW	**PCI_BIT_7_0:** PCI revision ID. these bits can be re-written from SETIDVALUE message 1st DW data byte 0

11.1.4 CUNIT_CFG_REG_HDR_TYPE—Offset Ch

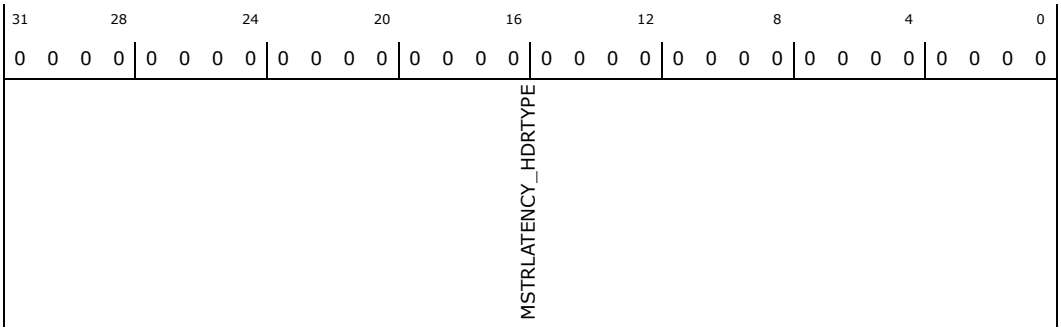
CUnit Configuration Register Device ID/Vendor ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CUNIT_CFG_REG_HDR_TYPE: [B:0, D:0, F:0] + Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**MSTRLATENCY_HDRTYPE:** Master Latency Timer and Header Type hardwired to 0

11.1.5 CUNIT_CFG_REG_STRAP_SSID—Offset 2Ch

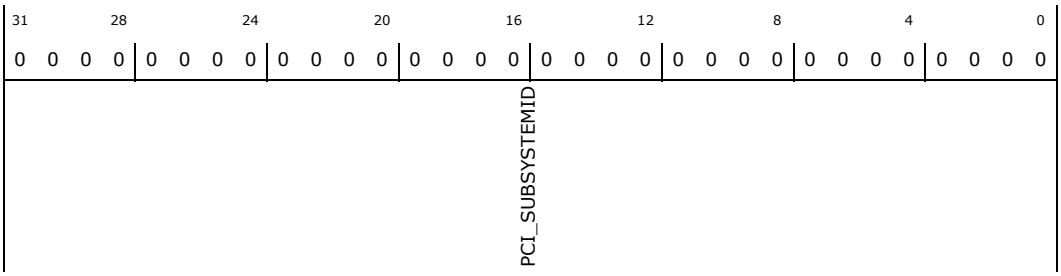
CUnit Configuration Register Device ID/Vendor ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CUNIT_CFG_REG_STRAP_SSID: [B:0, D:0, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**PCI_SUBSYSTEMID:** PCI Subsystem ID passed in from top-level straps strapSSID[31:0]

11.1.6 CUNIT_MANUFACTURING_ID—Offset F8h

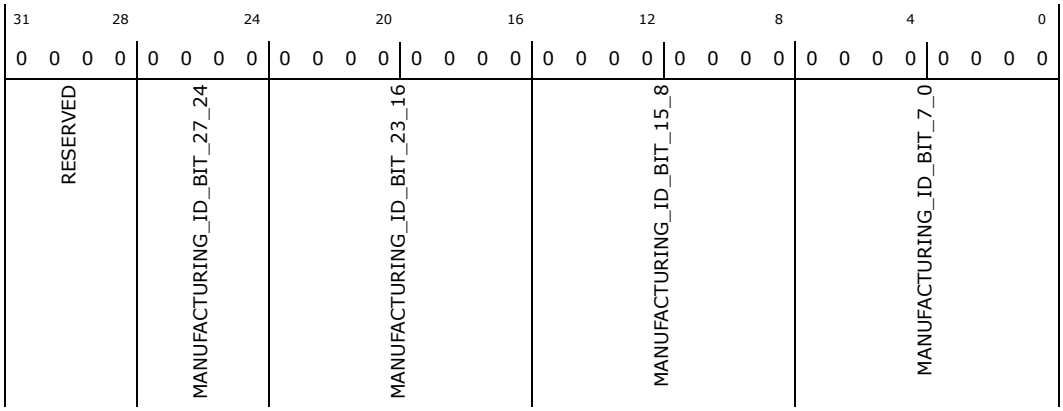
CUnit Manufacturing ID Register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

CUNIT_MANUFACTURING_ID: [B:0, D:0, F:0] + F8h

Default: 00000000h

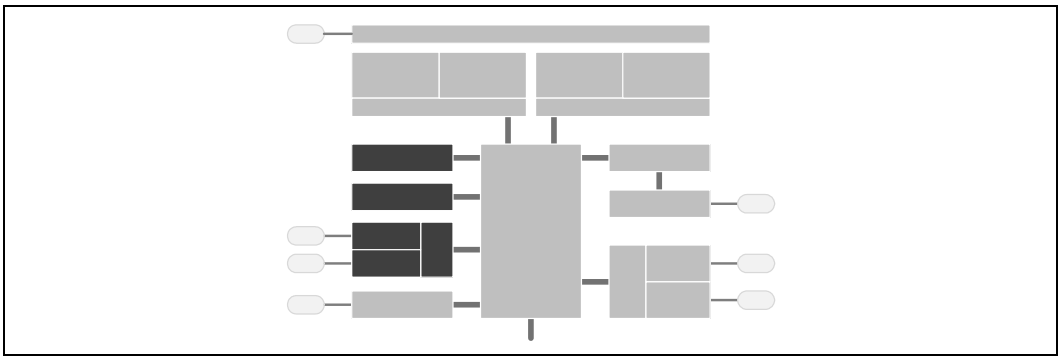


Bit Range	Default & Access	Description
31:28	0h RW	**RESERVED:** These bits can be re-written from SETIDVALUE message 2nd DW data byte 3 upper nibble
27:24	0h RW	**MANUFACTURING_ID_BIT_27_24:** Dot Portion of Process, these bits can be re-written from SETIDVALUE message 2nd DW data byte 3 lower nibble
23:16	0h RW	**MANUFACTURING_ID_BIT_23_16:** Process Portion of Process ID, these bits can be re-written from SETIDVALUE message 2nd DW data byte 0
15:8	0h RW	**MANUFACTURING_ID_BIT_15_8:** Manufacturing ID (MID), these bits can be re-written from SETIDVALUE message 2nd DW data byte 1
7:0	0h RW	**MANUFACTURING_ID_BIT_7_0:** Manufacturing Stepping ID (MSID), these bits can be re-written from SETIDVALUE message 2nd DW data byte 2

§ §

12 Graphics, Video, and Display

This section provides an overview of Graphics, Video and Display features of the processor.

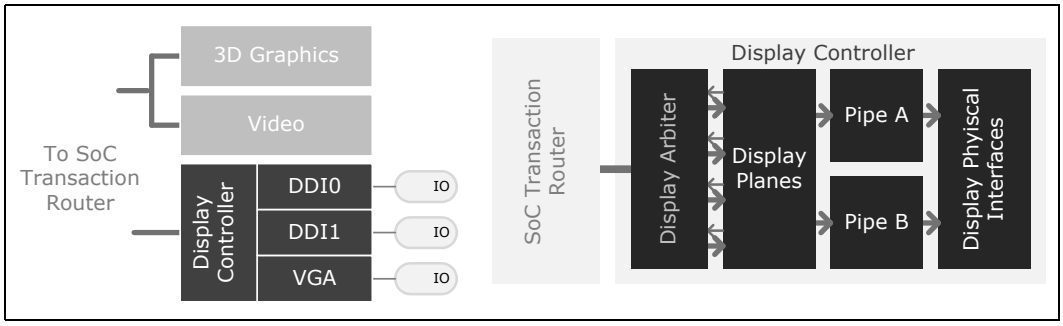


12.1 Features

The key features of the individual blocks are as follows:

- Refreshed seventh generation Intel graphics core with four Execution Units (EUs)
  - 3D graphics hardware acceleration including support for DirectX*11, OCL 1.2, OGL ES Halti/2.0/1.1, OGL 3.2
  - Video decode hardware acceleration including support for H.264, MPEG2, MVC, VC-1, WMV9 and VP8 formats
  - Video encode hardware acceleration including support for H.264, MPEG2 and MVC formats
  - Display controller, incorporating the display planes, pipes and physical interfaces
  - Four planes available per pipe - 1x Primary, 2x Video Sprite & 1x Cursor - plus a single legacy VGA plane
  - A single Analog Display physical interface, implementing VGA support
  - Two multi-purpose Digital Display Interface (DDI) PHYs implementing HDMI, DVI, DisplayPort (DP) or embedded DisplayPort* (eDP*) support

12.2 Processor Graphics Display



The processor Graphics controller display pipe can be broken down into three components:

- Display Planes
- Display Pipes
- Display Physical Interfaces

A display plane is a single displayed surface in memory and contains one image (desktop, cursor, overlay). It is the portion of the display hardware logic that defines the format and location of a rectangular region of memory that can be displayed on a display output device and delivers that data to a display pipe. This is clocked by the Core Display Clock.

12.2.1 Primary Planes A and B

Planes A and B are the main display planes and are associated with Pipes A and B respectively. Each plane supports per-pixel alpha blending.

12.2.2 Video Sprite Planes A, B, C and D

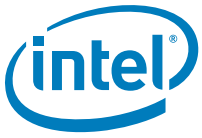
Video Sprite Planes A, B, C & D are planes optimized for video decode. Planes A and B are associated with Pipe A and Planes C and D are associated with Pipe B.

12.2.3 Cursors A and B

Cursors A and B are small, fixed-sized planes dedicated for mouse cursor acceleration, and are associated with Planes A and B respectively.

12.2.4 VGA

VGA is used for boot, safe mode, legacy games, etc. It can be changed by an application without OS/driver notification, due to legacy requirements.



12.3 Display Pipes

The display pipe blends and synchronizes pixel data received from one or more display planes and adds the timing of the display output device upon which the image is displayed.

The display pipes A and B operate independently of each other at the rate of one pixel per clock. They can attach to any of the display interfaces.

12.4 Display Physical Interfaces

The display physical interfaces consist of output logic and pins that transmit the display data to the associated encoding logic and send the data to the display device. These interfaces can be subdivided into analog (VGA) and digital (DisplayPort*, embedded DisplayPort*, DVI and HDMI*) interfaces.

12.4.1 Analog Display Physical Interface

The analog port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated Display Data Channel (DDC) signal pair dedicated to the analog port. The intended target device is for a monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactorily but no functionality is added to the signals to enhance that capability.

12.4.1.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 93. Analog Display Interface Signals

Signal Name	Direction Type	Description
VGA_BLUE	O	**Blue Analog Video Output:** This signal is a VGA Analog video output from the internal color palette DAC.
VGA_GREEN	O	**Green Analog Video Output:** This signal is a VGA Analog video output from the internal color palette DAC.
VGA_RED	O	**Red Analog Video Output:** This signal is a VGA Analog video output from the internal color palette DAC.
VGA_HSYNC	O	**VGA Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or "sync interval".
VGA_VSYNC	O	**VGA Vertical Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or "sync interval".

Table 93. Analog Display Interface Signals

Signal Name	Direction Type	Description
VGA_DDCCLK	I/O	**VGA DDC Clock:** EDID support for an external VGA display
VGA_DDCDATA	I/O	**VGA DDC Data:** EDID support for an external VGA display
VGA_IREF	I	**Resistor Set:** Set point resistor for the internal color palette DAC. A 357ohm+/-0.5% precision resistor is required between VGA_IREF and motherboard ground.
VGA_IRTN	O	This signal is the complement video signal output from the internal color palette DAC channels and this signal connects directly to the ground plane of the board.
LPC_RCOMP	-	VGA Impedance Compensation.

12.4.1.2 Features

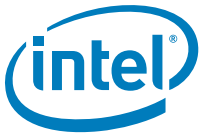
Table 94 lists the characteristics of the analog port.

Table 94. Analog Port Characteristics

Signal	Port Characteristics	Support
RGB	Voltage range	0.7 Vp-p nominal only
	CRT/Monitor sense	Analog compare
	Analog copy protection	No
	Sync on green	No
HSYNC VSYNC	Voltage	3.3 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite sync support	No
	Special flat panel sync	No
	Stereo sync	No
DDC	Voltage	External buffered to 5 V
	Control	Through GPIO interface

12.4.1.2.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the VGA monitor. The processor integrated 320 MHz RAMDAC supports resolutions up to 2560x1600 at 60 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.



12.4.1.2.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support are included.

12.4.1.2.3 VESA/VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

12.4.1.2.4 Display Data Channel (DDC)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug-and-play systems to be realized. Support for DDC 1 and 2 is implemented. The processor uses the VGA_DDCCLK and VGA_DDCDATA signals to communicate with the analog monitor. The processor does not generate these signals at 5 V; thus, external pull-up resistors and level shifting circuitry should be implemented on the board.

12.4.2 Digital Display Interfaces

12.4.2.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 95. Display Physical Interfaces Signal Names (Sheet 1 of 2)

Signal Name	Direction	Description	
		HDMI / DVI	DP / eDP*
DDI[1,0]_TXP[0] DDI[1,0]_TXP[1] DDI[1,0]_TXP[2] DDI[1,0]_TXP[3]	O	**Ports 1,0: Transmit Signals**	
		TMDS[1,0]_DATAP[2] TMDS[1,0]_DATAP[1] TMDS[1,0]_DATAP[0] TMDS[1,0]_CLKP	DP[1,0]_MAINP[0] DP[1,0]_MAINP[1] DP[1,0]_MAINP[2] DP[1,0]_MAINP[3]

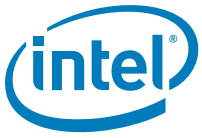
Table 95. Display Physical Interfaces Signal Names (Sheet 2 of 2)

Signal Name	Direction	Description	
		HDMI / DVI	DP / eDP*
DDI[1,0]_TXN[0] DDI[1,0]_TXN[1] DDI[1,0]_TXN[2] DDI[1,0]_TXN[3]	O	**Ports 1,0: Transmit Complement Signals**	
		TMDS[1,0]_DATAN[2] TMDS[1,0]_DATAN[1] TMDS[1,0]_DATAN[0] TMDS[1,0]_CLKN	DP[1,0]_MAINN[0] DP[1,0]_MAINN[1] DP[1,0]_MAINN[2] DP[1,0]_MAINN[3]
DDI[1,0]_AUXP	I/O	**Ports 1,0: Display Port Auxiliary Channel**	
		Unused	DP[1,0]_AUXP
DDI[1,0]_AUXN	I/O	**Ports 1,0: Display Port Auxiliary Channel Complement**	
		Unused	DP[1,0]_AUXN
DDI[1,0]_HPD	I	**Ports 1,0: Hot Plug Detect**	
		TMDS[1,0]_HPD	DP[1,0]_HPD
DDI[1,0]_DDCCLK	I/O	**Ports 1,0: DDC Clock**	
		TMDS[1,0]_DDCCLK	Unused
DDI[1,0]_DDCDATA	I/O	**Ports 1,0: DDC Data**	
		TMDS[1,0]_DDCDATA	DP[1,0]_EN - Port 0 Enable Strap
DDI[1,0]_BKLTCTL	O	**Ports 1,0: Panel Backlight Brightness Control**	
		HDMI / DVI / DP	**eDP* Only**
		Unused	EDP[1,0]_BKLTCTL
DDI[1,0]_BKLTEN	O	**Ports 1,0: Panel Backlight Enable**	
		HDMI / DVI / DP	**eDP* Only**
		Unused	EDP[1,0]_BKLTEN
DDI[1,0]_VDDEN	O	**Ports 1,0: Panel Power Enable**	
		HDMI / DVI / DP	**eDP* Only**
		Unused	EDP[1,0]_VDDEN
DDI_RCOMP_P/N	I/O	**DDI RCOMP** This signal is used for pre-driver slew rate compensation. An external precision resistor of 402 Ω ±1% should be connected between DDI_RCOMP_P and DDI_RCOMP_N.	

12.4.2.2 High-Definition Multimedia Interface

The High-Definition Multimedia Interface (HDMI) is provided for transmitting digital audio and video signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. It can carry high quality multi-channel audio data and all standard and high-definition consumer electronics video formats. HDMI display interface connecting the processor and display devices utilizes transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control) (not supported by the processor). As shown in Figure 14, the HDMI cable carries four differential pairs that make up the TMDS data



and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the processor are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

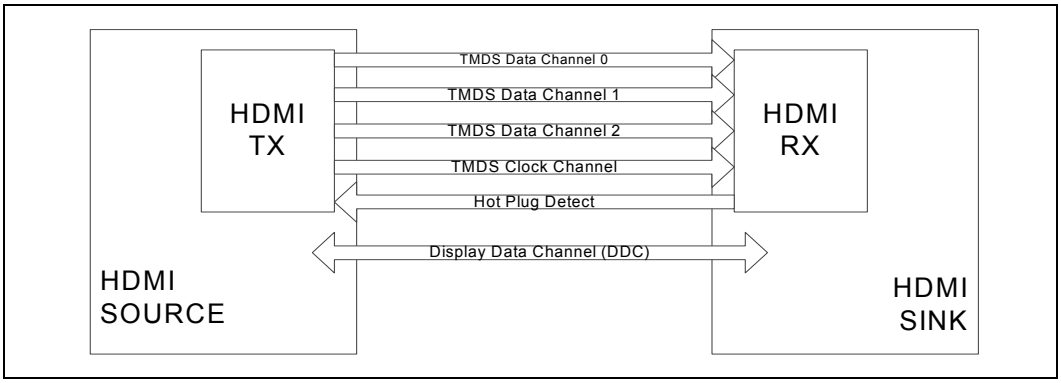
The processor HDMI interface is designed as per the High-Definition Multimedia Interface Specification 1.4. The processor supports High-Definition Multimedia Interface Compliance Test Specification 1.4.

12.4.2.2.1 Stereoscopic Support on HDMI

The processor display supports HDMI 1.4 3D video formats. If the HDMI panel is detected to support 3D video format, then the software driver will program Pipe2dB for the correct pipe timing parameters.

The left and right frames can be loaded from independent frame buffers in the main memory. Depending on the input S3D format, the display controller can be enabled do perform frame repositioning, image scaling, line interleaving.

Figure 14. HDMI Overview



12.4.2.3 Digital Video Interface (DVI)

The Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver which is similar to the HDMI protocol but without the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. To drive DVI-I through the back panel the VGA DDC signals are connected along with the digital data and clock signals from one of the Digital Ports. When a system has support for a DVI-I port, then either VGA or the DVI-D through a single DVI-I connector can be driven but not both simultaneously.

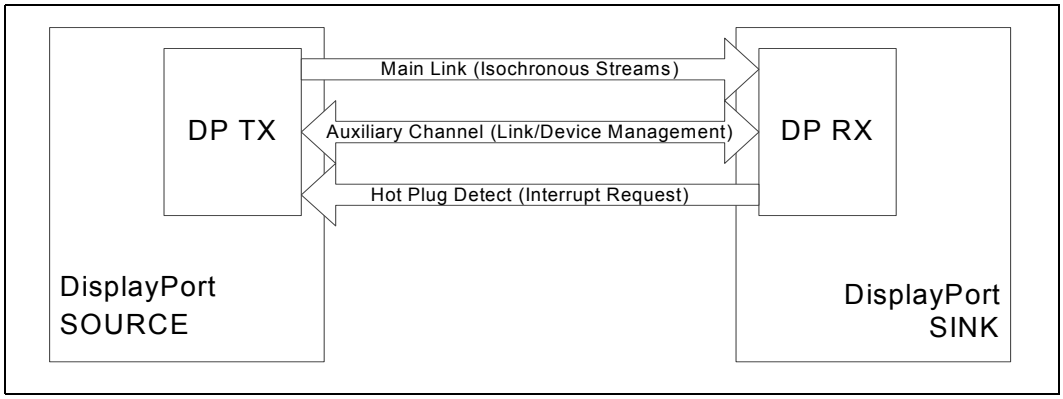
12.4.2.4 Display Port

Display Port is a digital communication interface that utilizes differential signalling to achieve a high bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays. The Display Port is also suitable for display connections between consumer electronics devices such as high definition optical disc players, set top boxes, and TV displays.

A Display Port consists of a Main Link, Auxiliary channel, and a Hot Plug Detect signal. The Main Link is a uni-directional, high-bandwidth, and low latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The processor supports DisplayPort Standard Version 1.1.

Figure 15. DisplayPort* Overview



12.4.2.5 embedded DisplayPort* (eDP*)

embedded DisplayPort* (eDP*) is a embedded version of the DisplayPort standard oriented towards applications, such as notebook and All-In-One PCs. eDP is supported only on Digital Display Interfaces 0 and/or 1. Like DisplayPort, embedded DisplayPort* also consists of a Main Link, Auxiliary channel, and a optional Hot Plug Detect signal.

Each eDP port can be configured for up-to 4 lanes.

The processor supports embedded DisplayPort Standard Version 1.3.

12.4.2.5.1 Hot-Plug Detect (HPD)

The processor supports HPD for Hot-Plug sink events on the HDMI and DisplayPort interfaces.

12.4.2.5.2 Integrated Audio over HDMI and DisplayPort

The processor can support two audio streams on DP/HDMI ports. Each stream can be programmable to either DDI port. HDMI/DP audio streams can be sent with video streams as follows.

12.4.2.5.3 High-Bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, etc.) and the sink (panels, monitor, and TV). The processor supports HDCP 1.4/2.1 for content protection over wired displays (HDMI, DisplayPort and embedded DisplayPort*).

12.5 References

- High-Definition Multimedia Interface Specification, Version 1.4
- High-bandwidth Digital Content Protection System, Revision 1.4
- VESA DisplayPort Standard, Version 1.1
- VESA embedded DisplayPort Standard, Version 1.3

12.6 3D Graphics and Video

The processor implements a derivative of the Generation 7 graphics engine, which consists of rendering engine and bit stream encoder/decoder engine. The rendering engine is used for 3D rendering, media compositing, and video encoding. The Graphics engine is built around four execution units (EUs).

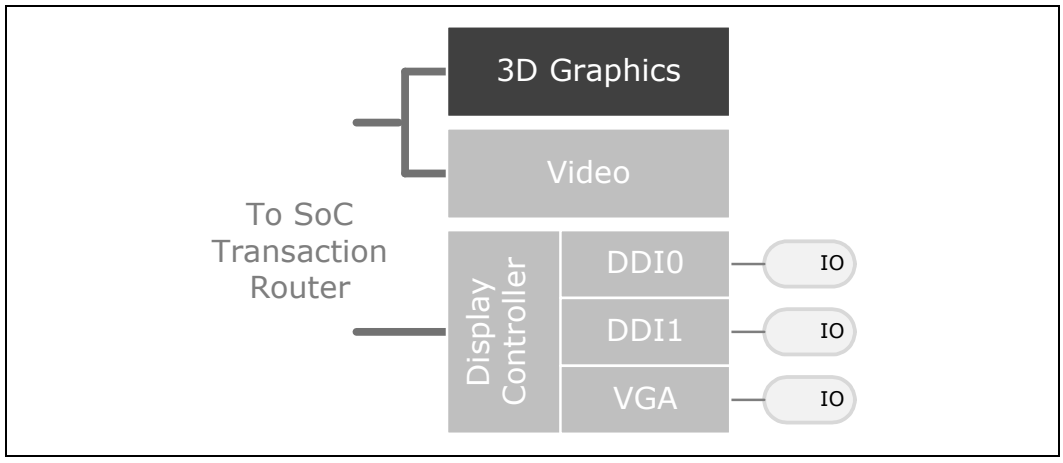
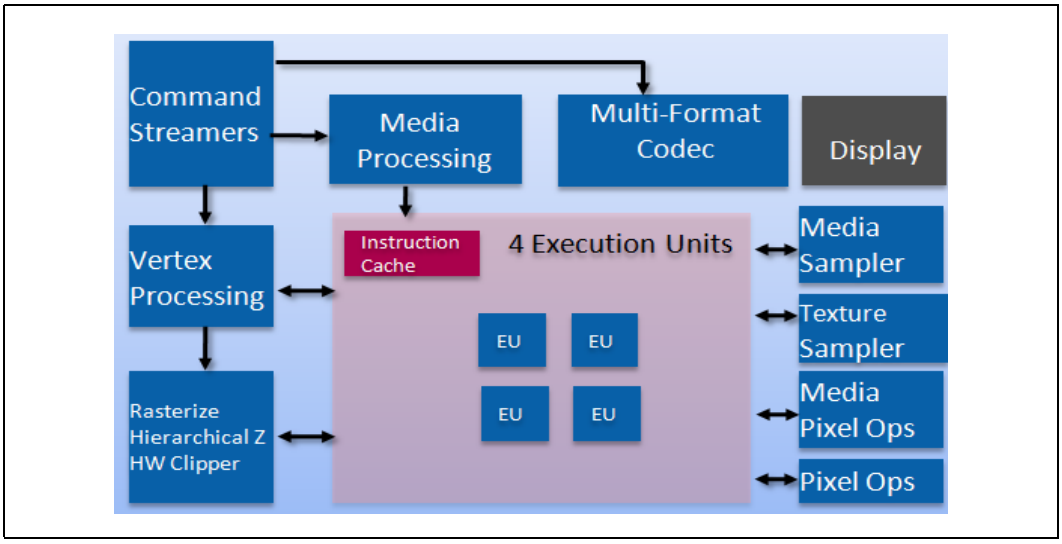


Figure 16. 3D Graphics Block Diagram



12.7 Features

The 3D graphics pipeline architecture simultaneously operates on different primitives or on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine. The Gen 7.0 3D engine provides the following performance and power-management enhancements:

- Hierarchal-Z
- Video quality enhancements

12.7.1 3D Engine Execution Units

- The EUs perform 128-bit wide execution per clock.
- Support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing.

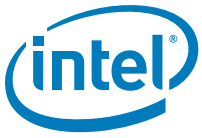
12.7.2 3D Pipeline

12.7.2.1 Vertex Fetch (VF) Stage

The VF stage executes 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as SGI OpenGL*.

12.7.2.2 Vertex Shader (VS) Stage

The VS stage performs shading of vertices output by the VF function. The VS unit produces an output vertex reference for every input vertex reference received from the VF unit, in the order received.



12.7.2.3 Geometry Shader (GS) Stage

The GS stage receives inputs from the VS stage. Compiled application-provided GS programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from the edges.

12.7.2.4 Clip Stage

The Clip stage performs general processing on incoming 3D objects. However, it also includes specialized logic to perform a Clip Test function on incoming objects. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.

12.7.2.5 Strips and Fans (SF) Stage

The SF stage performs setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage contain implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

12.7.2.6 Windower/IZ (WIZ) Stage

The WIZ unit performs an early depth test, which removes failing pixels and eliminates unnecessary processing overhead.

The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels. The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering diffuses the sharp color bands seen on smooth-shaded objects.

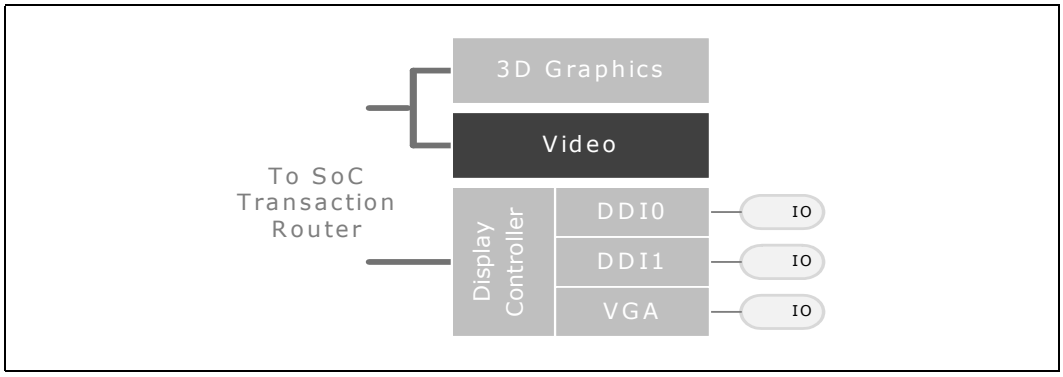
12.7.3 Video Engine

The video engine is part of the Intel Processor Graphics for image processing, play-back and transcode of Video applications. The processor Graphics video engine has a dedicated fixed hardware pipe-line for high quality decode and encode of media content. This engine supports Full HW acceleration for decode of AVC/H.264, VC-1 and MPEG -2 contents along with encode of MPEG-2 and AVC/H.264 apart from various video processing features. The new Processor Graphics Video engine adds support for processing features such as frame rate conversion, image stabilization and gamut conversion.

12.8 VED (Video Encode/Decode)

The video engine is part of the Intel Processor Graphics for image processing, play-back and transcode of Video applications. The Processor Graphics video engine has a dedicated fixed hardware pipe-line for high-quality decode and encode of media content. The Processor Video Encode Decode block incorporates VXD 392 video decode core and supports the following codec: VP8.

Note: Video encode is NOT supported on all SKUs.



12.8.1 Features

The features for the Video decode hardware accelerator in the processor are:

- VED core can be configured on a time division multiplex basis to handle single, dual and multi-stream HD decoding.
- VED provides full hardware acceleration support for VP8.

Table 96. Hardware Accelerated Video Decode Codec Support

Codec Format	Level
VP8	1080p30

Note: The processor uses IMG VP8 video decode engine. There are 21 functional units in this decoder. The Specification states that you can dynamically clock gate some of these units.

§

13 Serial ATA (SATA)

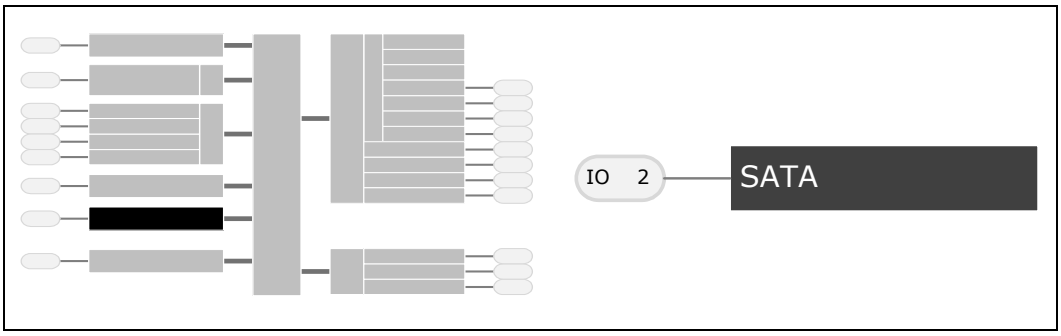
The processor has one integrated SATA host controller that supports independent DMA operation on up to 2 ports and supports data transfer rates of 1.5 Gb/s (150 MB/s) and 3.0 Gb/s (300 MB/s). The SATA controller contains two modes of operation – a legacy mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities.

The processor supports the Serial ATA Specification, Revision 2.6. The processor also supports several optional sections of the SATA Revision 2.0 Specifications: Extensions to Serial ATA 1.0 Specification, Revision 1.0 (AHCI support is required for some elements).

The SATA controllers feature two sets of interface signals (ports) that can be independently enabled or disabled (they cannot be tri-stated or driven low). Each interface is supported by an independent DMA controller.

The SATA controllers interact with an attached mass storage device through a register interface that is equivalent to that presented by a traditional IDE host adapter. The host software follows existing standards and conventions when accessing the register interface and follows standard command protocol conventions.

Note: SATA interface transfer rates are independent of UDMA mode settings. SATA interface transfer rates will operate at the bus's maximum speed, regardless of the UDMA mode reported by the SATA device or the system BIOS.



13.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 97. Signals

Signal Name	Direction/ Type	Description
SATA_GP[0]	I CMOS1.8	**Serial ATA 0 General Purpose:** This is an input pin that can be configured as an interlock switch or as a general purpose I/O, depending on the platform. When used as an interlock switch status indication, this signal should be driven to '0' to indicate that the switch is closed, and to '1' to indicate that the switch is open.
SATA_GP[1]	I CMOS1.8	**Serial ATA 1 General Purpose:** Same as above.
SATA_LED#	O CMOS1.8_OD	**Serial ATA LED:** This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off.
SATA_TXP[1:0] **SATA_TXN[1:0]**	O SATA	**Serial ATA Port 1 and 0:** These are outbound high-speed differential signals to Port 1 and 0.
SATA_RXP[1:0] **SATA_RXN[1:0]**	I SATA	**Serial ATA Port 1 and 0:** These are inbound high-speed differential signals to Port 1 and 0.
SATA_DEVSLP[1:0]	I/O SATA	These pins are used for hardware DEVSLP enabling. SATA_DEVSLP[0] is multiplexed with SATA_GPI[1], MMC1_RST#.
SATA_RCOMP_P SATA_RCOMP_N	O	These pins are used to connect the external resistors used for Rcomp.

13.2 Features

13.2.1 Supported Features

Table 98. SATA Feature List

Feature	Description
Native Command Queuing (NCQ)	Allows the device to reorder commands for more efficient data transfers
Auto Activate for DMA	Collapses a DMA Setup then DMA Activate sequence into a DMA Setup only
Hot Plug Support	Allows for device detection without power being applied and ability to connect and disconnect devices without prior notification to the system
Asynchronous Signal Recovery	Provides a recovery from a loss of signal or establishing communication after hot plug
3 Gb/s Transfer Rate	Capable of data transfers up to 3 Gb/s
ATAPI Asynchronous Notification	A mechanism for a device to send a notification to the host that the device requires attention
Host & Link Initiated Power Management	Capability for the host controller or device to request Partial and Slumber interface power states
Staggered Spin-Up	Enables the host to spin up hard drives sequentially to prevent power load problems on boot
Command Completion Coalescing	Reduces interrupt and completion overhead by allowing a specified number of commands to complete and then generating an interrupt to process the commands

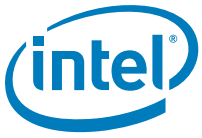


Table 99. SATA/AHCI Feature Matrix

Feature	AHCI Disabled	AHCI Enabled
Native Command Queuing (NCQ)	N/A	Supported
Auto Activate for DMA	N/A	Supported
Hot Plug Support	N/A	Supported
Asynchronous Signal Recovery	N/A	Supported
3 Gb/s Transfer Rate	Supported	Supported
ATAPI Asynchronous Notification	N/A	Supported
Host & Link Initiated Power Management	N/A	Supported
Staggered Spin-Up	Supported	Supported
Command Completion Coalescing	N/A	N/A

13.2.2 Theory of Operation

13.2.2.1 Standard ATA Emulation

The processor contains a set of registers that shadow the contents of the legacy IDE registers. The behavior of the Command and Control Block registers, PIO, and DMA data transfers, resets, and interrupts are all emulated.

Note: The processor will assert INTR when the master device completes the EDD command regardless of the command completion status of the slave device. If the master completes EDD first, an INTR is generated and BSY will remain '1' until the slave completes the command. If the slave completes EDD first, BSY will be '0' when the master completes the EDD command and asserts INTR. Software must wait for busy to clear (0) before completing an EDD command, as required by the ATA5 through ATA7 (T13) industry standards.

13.2.2.2 48-Bit LBA Operation

The SATA host controller supports 48-bit LBA through the host-to-device register FIS when accesses are performed using writes to the task file. The SATA host controller will ensure that the correct data is put into the correct byte of the host-to-device FIS.

There are special considerations when reading from the task file to support 48-bit LBA operation. Software may need to read all 16-bits. Since the registers are only 8-bits wide and act as a FIFO, a bit must be set in the device/control register, which is at offset 3F6h for primary and 376h for secondary (or their native counterparts).

If software clears Bit 7 of the control register before performing a read, the last item written will be returned from the FIFO. If software sets Bit 7 of the control register before performing a read, the first item written will be returned from the FIFO.

13.2.3 AHCI Operation

The processor provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers developed through a joint industry effort. AHCI defines transactions between the SATA controller and software and enables advanced performance and usability with SATA. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices—each device is treated as a master—and hardware assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug. AHCI requires appropriate software support (such as, an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

The processor supports all of the mandatory features of the *Serial ATA Advanced Host Controller Interface Specification*, Revision 1.3 and many optional features, such as hardware assisted native command queuing, aggressive power management, LED indicator support, and Hot-Plug through the use of interlock switch support (additional platform hardware and software may be required depending upon the implementation).

Note: For reliable device removal notification while in AHCI operation without the use of interlock switches (surprise removal), interface power management should be disabled for the associated port.

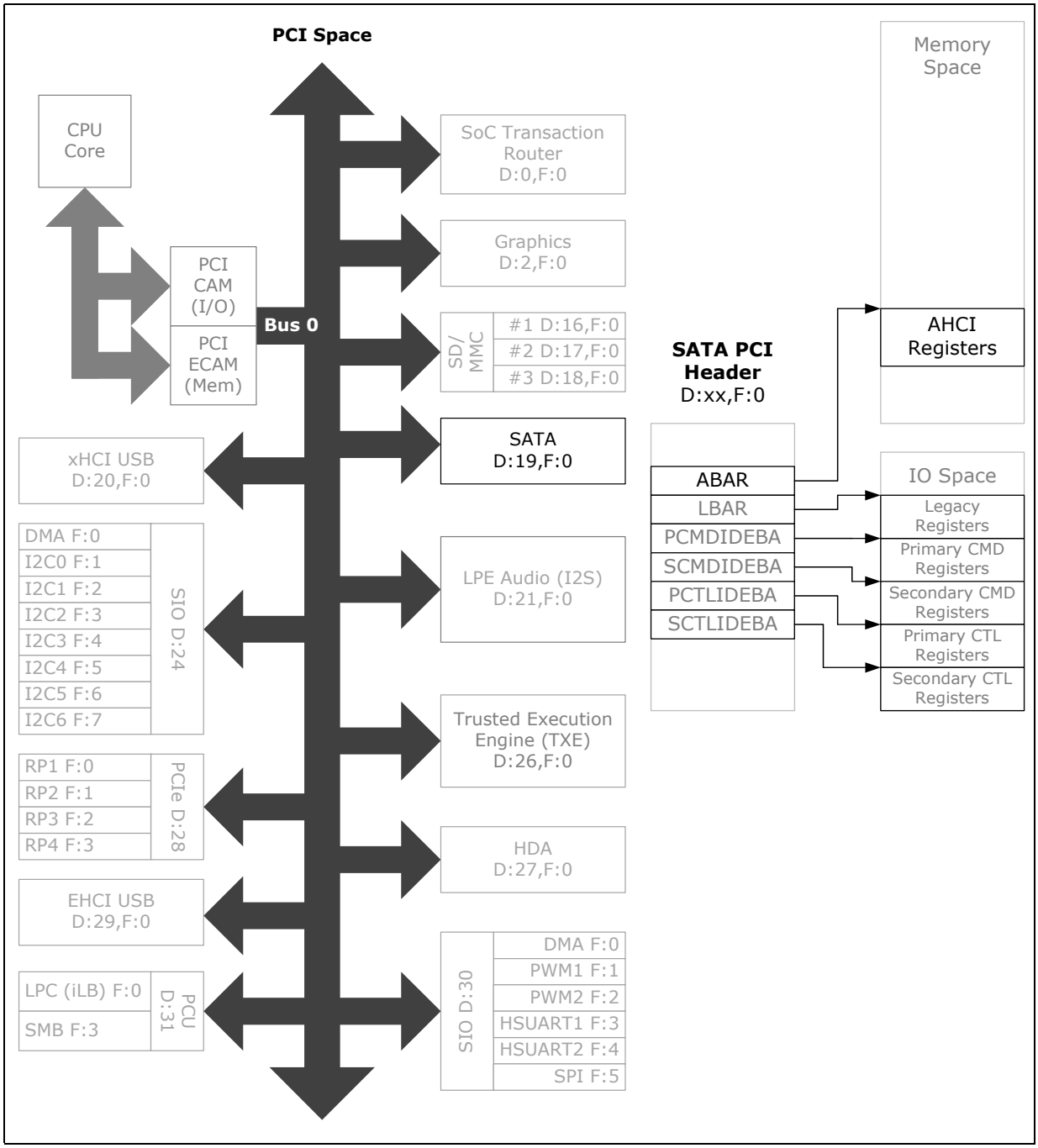
13.3 References

- Serial ATA Specification rev 2.6
- Serial ATA Advanced Host Controller Interface (AHCI) Specification rev 1.3
- Serial ATA II: Extensions to Serial ATA 1.0 Specification, Revision 1.0

13.4 Register Map

See Chapters 3 and 4 for additional information.

Figure 17. SATA Register Map



13.5 SATA PCI Configuration Registers

Table 100. Summary of SATA PCI Configuration Registers—0/19/0

Offset	Size	Register ID—Description	Default Value
0h	4	"Identifiers (ID)—Offset 0h" on page 141	0F208086h
4h	2	"Command (CMD)—Offset 4h" on page 142	0000h
6h	2	"Device Status (STS)—Offset 6h" on page 143	02B0h
8h	1	"Revision ID (RID)—Offset 8h" on page 144	00h
9h	1	"Programming Interface (PI)—Offset 9h" on page 144	8Ah
Ah	2	"Class Code (CC)—Offset Ah" on page 145	0106h
Ch	1	"Cache Line Size (CLS)—Offset Ch" on page 145	00h
Dh	1	"Master Latency Timer (MLT)—Offset Dh" on page 146	00h
Eh	1	"Header Type (HTYPE)—Offset Eh" on page 146	00h
10h	4	"Primary Command Block Base Address (PCMDBA)—Offset 10h" on page 147	00000001h
14h	4	"Primary Control Block Base Address (PCTLBA)—Offset 14h" on page 147	00000001h
18h	4	"Secondary Command Block Base Address (SCMDBA)—Offset 18h" on page 148	00000001h
1Ch	4	"Secondary Control Block Base Address (SCTLBA)—Offset 1Ch" on page 148	00000001h
20h	4	"Legacy IDE Base Address / AHCI Index Data Pair Base Address (LBAR)—Offset 20h" on page 149	00000001h
24h	4	"AHCI Base Address/Serial ATA Index Data Pair Base Address (ABAR)—Offset 24h" on page 149	00000000h
2Ch	4	"Sub System Identifiers (SS)—Offset 2Ch" on page 150	00000000h
34h	1	"Capabilities Pointer (CAP)—Offset 34h" on page 151	80h
3Ch	2	"Interrupt Information (INTR)—Offset 3Ch" on page 151	0100h
3Eh	1	"Minimum Grant (MGNT)—Offset 3Eh" on page 152	00h
3Fh	1	"Maximum Latency (MLAT)—Offset 3Fh" on page 152	00h
40h	2	"Primary Timing (PTIM)—Offset 40h" on page 153	0000h
42h	2	"Secondary Timing (STIM)—Offset 42h" on page 154	0000h
44h	1	"Device 1 IDE Timing (D1TIM)—Offset 44h" on page 155	00h
48h	1	"Synchronous DMA Control (Synchronous_DMA_Control)—Offset 48h" on page 155	00h
4Ah	2	"Synchronous_DMA_Timing—Offset 4Ah" on page 156	0000h
54h	4	"IDE I/O Configuration (IIOC)—Offset 54h" on page 156	00000000h
70h	2	"PCI Power Management Capability ID (PID)—Offset 70h" on page 157	A801h
72h	2	"Primary Command Block Base Address (PCMDBA)—Offset 10h" on page 147	4003h
74h	2	"PCI Power Management Control and Status (PMCS)—Offset 74h" on page 158	0008h
80h	2	"Message Signaled Interrupt Identifier (MID)—Offset 80h" on page 159	7005h
82h	2	"Message Signaled Interrupt Message Control (MC)—Offset 82h" on page 159	0000h
84h	4	"Message Signaled Interrupt Message Address (MA)—Offset 84h" on page 160	00000000h
88h	2	"Message Signaled Interrupt Message Data (MD)—Offset 88h" on page 160	0000h
90h	2	"Port Mapping Register (MAP)—Offset 90h" on page 161	0420h
92h	2	"Port Control and Status (PCS)—Offset 92h" on page 162	0000h

Table 100. Summary of SATA PCI Configuration Registers—0/19/0 (Continued)

Offset	Size	Register ID—Description	Default Value
94h	4	"Test Mode Register (TM)—Offset 94h" on page 163	00000000h
9Ch	4	"SATA General Configuration (SATAGC)—Offset 9Ch" on page 163	00000000h
A0h	1	"SATA Initialization Register Index (SIRI)—Offset A0h" on page 165	00h
A4h	4	"SATA Initialization Register Data (SIRD)—Offset A4h" on page 165	00000000h
A8h	4	"Serial ATA Capability Register 0 (SATACR0)—Offset A8h" on page 166	00100012h
ACh	4	"Serial ATA Capability Register 1 (SATACR1)—Offset ACh" on page 167	00000048h
B0h	2	"FLR Capability ID (FLRCID)—Offset B0h" on page 167	0000h
B4h	2	"FLR Control (FLRCTL)—Offset B4h" on page 168	0000h
D0h	4	"Scratch Pad (SP)—Offset D0h" on page 168	00000000h
E0h	4	"BIST FIS Control/Status (BFCS)—Offset E0h" on page 169	00000000h
E4h	4	"BIST FIS Transmit Data 1 (BFTD1)—Offset E4h" on page 170	00000000h
E8h	4	"BIST FIS Transmit Data 2 (BFTD2)—Offset E8h" on page 170	00000000h
F8h	4	"Manufacturing ID (MFID)—Offset F8h" on page 171	08000FB1h

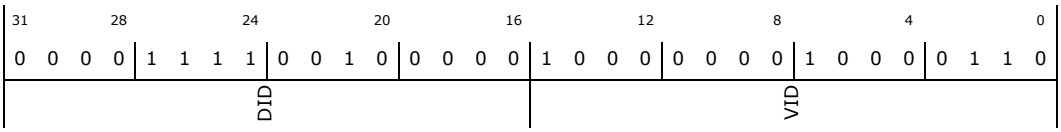
13.5.1 Identifiers (ID)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ID: [B:0, D:19, F:0] + 0h

Default: 0F208086h



Bit Range	Default & Access	Description
31:16	0F20h RO	**Device ID (DID):** The specific value is dependent on config bits and fuses. The value is product specific. VLV SATA DID can be within the range of 0F20-0F27 and 0F2E and 0F2F. However, since VLV SATA does not support RAID, DID can be either 0F20 or OF22.
15:0	8086h RO	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel.

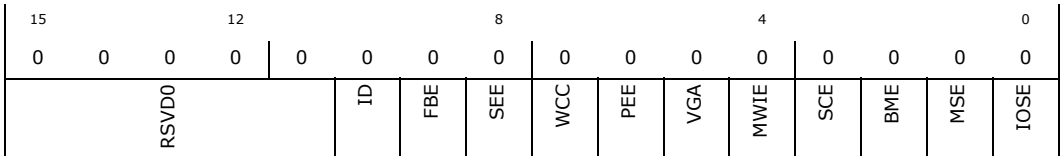
13.5.2 Command (CMD)—Offset 4h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

CMD: [B:0, D:19, F:0] + 4h

Default: 0000h



Bit Range	Default & Access	Description
15:11	0b RO	**RSVD0:** Reserved
10	0h RW	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# will not be generated. When cleared, internal INTx# is generated if there is an interrupt and MSI is not enabled.
9	0h RO	**Fast Back-to-Back Enable (FBE):** Reserved.
8	0h RW	**SERR# Enable (SEE):** When set to 1, the HBA is allowed to generate SERR# on DPD or SATAGC.URD event that is enabled for SERR# generation. When cleared to 0, it is not.
7	0h RO	**Wait Cycle Enable (WCC):** Reserved.
6	0h RW	**Parity Error Response Enable (PEE):** When set, the SATA Controller will corrupt the outbound DATA FIS CRC if a forwarded data parity error is indicated.
5	0h RO	**VGA Palette Snooping Enable (VGA):** Reserved.
4	0h RO	**Memory Write and Invalidate Enable (MWIE):** Reserved.
3	0h RO	**Special Cycle Enable (SCE):** Reserved.
2	0h RW	**Bus Master Enable (BME):** Controls the SATA Controller's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	0h RW	**Memory Space Enable (MSE):** Controls access to the SATA Controller's target memory space (for AHCI).
0	0h RW	**I/O Space Enable (IOSE):** Controls access to the SATA Controller's target I/O space.

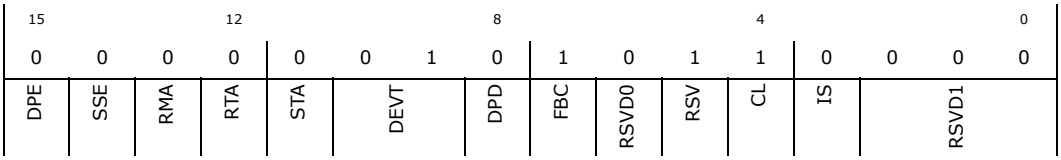
13.5.3 Device Status (STS)—Offset 6h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

STS: [B:0, D:19, F:0] + 6h

Default: 02B0h



Bit Range	Default & Access	Description
15	0h RW/1C	**Detected Parity Error (DPE):** Set when the SATA Controller detects a parity error on its interface.
14	0h RW/1C	**Signaled System Error (SSE):** Set when SATA Controller generates an SERR#.
13	0h RW/1C	**Received Master-Abort Status (RMA):** Set when the SATA Controller receives a master abort to a cycle it generated.
12	0h RW/1C	**Received Target-Abort Status (RTA):** Set when the SATA Controller receives a target abort to a cycle it generated.
11	0h RW/1C	**Signaled Target-Abort Status (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target-Abort do not need to implement this bit.
10:9	1h RO	**DEVSEL# Timing Status (DEVT):** Controls the device select time for the SATA Controller's PCI interface.
8	0h RW/1C	**Master Data Parity Error Detected (DPD):** Set when the SATA Controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit (bit 6 of the command register) is set. This bit can only be set on read completions received from the backbone where there is a parity error.
7	1h RO	**Fast Back-to-Back Capable (FBC):** Reserved.
6	0b RO	**RSVD0:** Reserved
5	1h RO	**66 MHz Capable (RSV):** Reserved.
4	1h RO	**Capabilities List (CL):** Indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA Controller.
3	0h RO	**Interrupt Status (IS):** Reflects the state of INTx# messages, IRQ14 or IRQ15. This bit is set when the interrupt is to be asserted. This bit is a 0 after the interrupt is cleared
2:0	0b RO	**RSVD1:** Reserved

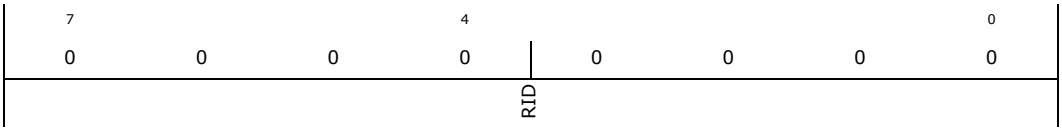
13.5.4 Revision ID (RID)—Offset 8h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

RID: [B:0, D:19, F:0] + 8h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**Revision ID (RID):** Indicates stepping of the host controller hardware.

13.5.5 Programming Interface (PI)—Offset 9h

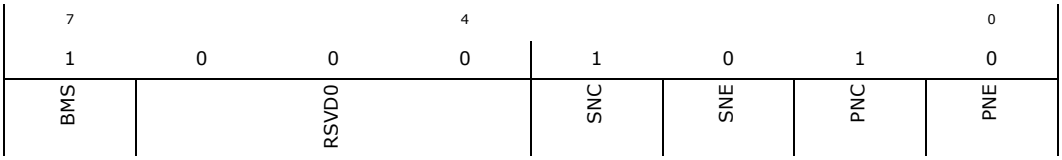
This register definition depends on the CC.SCC field. When the CC.SCC is 01h(IDE mode), register definition corresponds to 1st table. When CC.SCC is 06h(AHCI mode), register definition follows the 2nd table.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PI: [B:0, D:19, F:0] + 9h

Default: 8Ah



Bit Range	Default & Access	Description
7	1h RO	**Bus Master Support (BMS):** Indicates the SATA Controller supports bus master operation.
6:4	0b RO	**RSVD0:** Reserved
3	1h RO	**Secondary Mode Native Capable (SNC):** Indicates that the secondary controller supports both legacy and native modes.
2	0h RW	**Secondary Mode Native Enable (SNE):** Determines the mode that the secondary channel is operating in. 0 corresponds to 'compatibility', 1 means PCI native. If this bit is set by SW, then the PNE bit must also be set by SW. While in theory these bits can be programmed separately, such a configuration is not supported by today's software and is not supported by this hardware. If this bit is left unchanged before switching, the result is indeterminate.
1	1h RO	**Primary Mode Native Capable (PNC):** Indicates that the primary controller supports both legacy and native modes.

Bit Range	Default & Access	Description
0	0h RW	**Primary Mode Native Enable (PNE):** Determines the mode that the primary channel is operating in. 0 corresponds to 'compatibility', 1 means PCI native. If this bit is set by SW, then the SNE bit must also be set by SW. While in theory these bits can be programmed separately, such a configuration is not supported by today's software and is not supported by this hardware. If this bit is left unchanged before switching, the result is indeterminate.

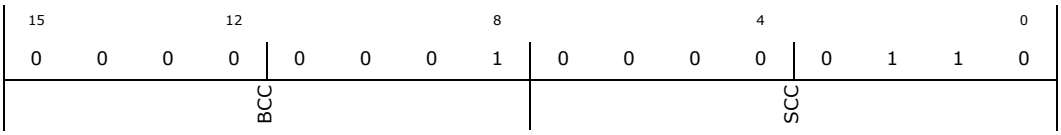
13.5.6 Class Code (CC)—Offset Ah

Access Method

Type: PCI Configuration Register (Size: 16 bits)

CC: [B:0, D:19, F:0] + Ah

Default: 0106h



Bit Range	Default & Access	Description
15:8	01h RO	**Base Class Code (BCC):** Indicates that this is a mass storage device.
7:0	06h RO	**Sub Class Code (SCC):** The value reported in this field is dependent on MAP.SMS and various fuses and configuration bits. The value is product specific. For VLV this field may read 01h (IDE) or 06h (AHCI).

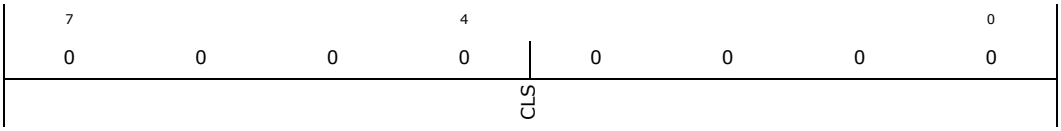
13.5.7 Cache Line Size (CLS)—Offset Ch

Access Method

Type: PCI Configuration Register (Size: 8 bits)

CLS: [B:0, D:19, F:0] + Ch

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**Cache Line Size (CLS):** This register has no meaning for the SATA controller.

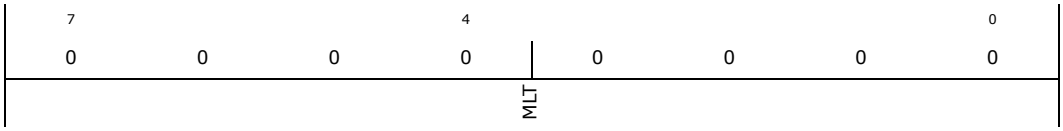
13.5.8 Master Latency Timer (MLT)—Offset Dh

Access Method

Type: PCI Configuration Register (Size: 8 bits)

MLT: [B:0, D:19, F:0] + Dh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**Master Latency Timer (MLT):** This register has no meaning for the SATA controller.

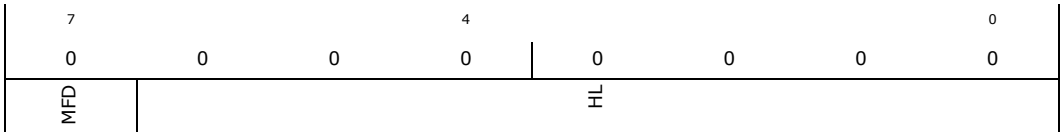
13.5.9 Header Type (HTYPE)—Offset Eh

Access Method

Type: PCI Configuration Register (Size: 8 bits)

HTYPE: [B:0, D:19, F:0] + Eh

Default: 00h



Bit Range	Default & Access	Description
7	0h RO	**Multi-function Device (MFD):** Indicates this controller is not part of a multi-function device.
6:0	00h RO	**Header Layout (HL):** Indicates that the controller uses a target device layout.

13.5.10 Primary Command Block Base Address (PCMDBA)—Offset 10h

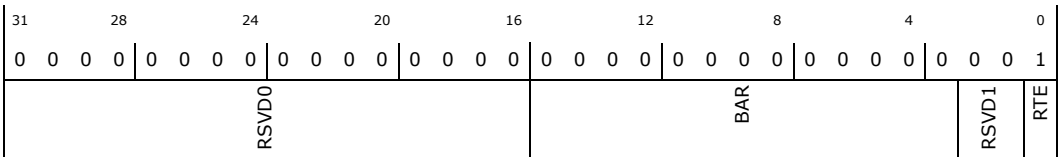
This 8-byte I/O space is used in Native Mode for the Primary Controller's Command Block.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCMDBA: [B:0, D:19, F:0] + 10h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:3	0h RW	**Base Address (BAR):** Base address of the I/O space (8 consecutive I/O locations).
2:1	0b RO	**RSVD1:** Reserved
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

13.5.11 Primary Control Block Base Address (PCTLBA)—Offset 14h

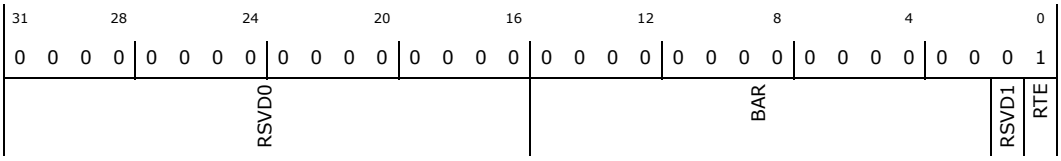
This 4-byte I/O space is used in Native Mode for the Primary Controller's Control Block.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCTLBA: [B:0, D:19, F:0] + 14h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:2	0h RW	**Base Address (BAR):** Base address of the I/O space (4 consecutive I/O locations).
1	0b RO	**RSVD1:** Reserved
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

13.5.12 Secondary Command Block Base Address (SCMDBA)—Offset 18h

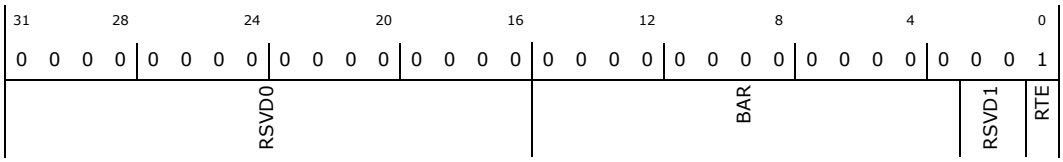
This 8-byte I/O space is used in Native Mode for the Secondary Controller's Command Block.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SCMDBA: [B:0, D:19, F:0] + 18h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:3	0h RW	**Base Address (BAR):** Base address of the I/O space (8 consecutive I/O locations).
2:1	0b RO	**RSVD1:** Reserved
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

13.5.13 Secondary Control Block Base Address (SCTLBA)—Offset 1Ch

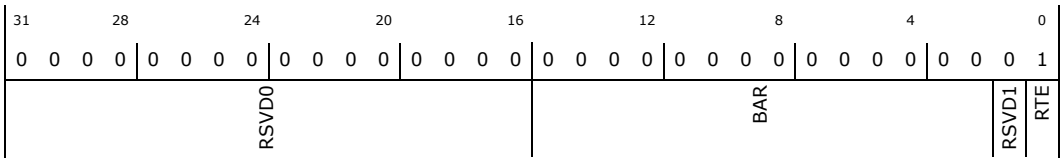
This 4-byte I/O space is used in Native Mode for the Secondary Controller's Control Block.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SCTLBA: [B:0, D:19, F:0] + 1Ch

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:2	0h RW	**Base Address (BAR):** Base address of the I/O space (4 consecutive I/O locations).
1	0b RO	**RSVD1:** Reserved

Bit Range	Default & Access	Description
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

13.5.14 Legacy IDE Base Address / AHCI Index Data Pair Base Address (LBAR)—Offset 20h

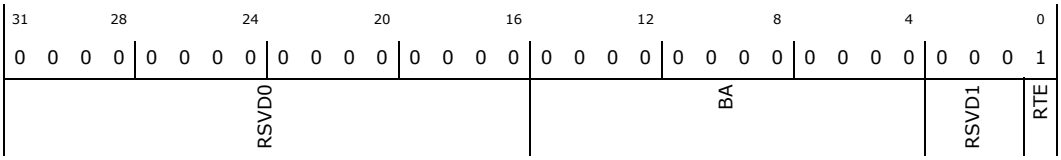
This BAR is used to allocate I/O space for the SFF-8038i mode of operation (also known as Bus Master IDE) and if CC.SCC is not 01h, it is used to allocate I/O space for the AHCI index/data pair mechanism as well. Note that hardware does not clear the BA bits (including BA4) when switching from IDE mode to non-IDE mode or vice versa. BIOS is responsible for clearing those bits to 0 since the number of writable bits changes after mode switching.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

LBAR: [B:0, D:19, F:0] + 20h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:4	0h RW	**Base Address (BA):** Base address of the I/O space. Note for Base Address bit 4: When CC.SCC is 01h, this bit will be RW resulting in requesting 16B of I/O space. When CC.SCC is not 01h, this bit will be RO=0 resulting in requesting 32B of I/O space.
3:1	0b RO	**RSVD1:** Reserved
0	1h RO	**Resource Type Indicator (RTE):** Indicates a request for IO space.

13.5.15 AHCI Base Address/Serial ATA Index Data Pair Base Address (ABAR)—Offset 24h

When the programming interface is not IDE (that is, CC.SCC is not 01h), this register is named ABAR. When the programming interface is IDE, this register becomes SIDPBA. Note that hardware does not clear those BA bits when switching from IDE SKU to non-IDE SKU or vice versa. BIOS is responsible for clearing those bits to 0 since the number of writable bits changes after SKU switching (as indicated by a change in CC.SCC). In the case, this register will then have to be re-programmed to a proper value. When the programming interface is not IDE, the register represents a memory BAR allocating space for the AHCI memory registers. Note that bit[31:16] of this register must be programmed to a value greater than 0 to ensure the memory is mapped to an address of 1 MBytes and greater (that is, ABAR must be 00010000h or greater). Otherwise, memory cycle targeting the ABAR range may not be accepted. When the programming interface is IDE, the register becomes an I/O BAR allocating 16 bytes of I/O space for

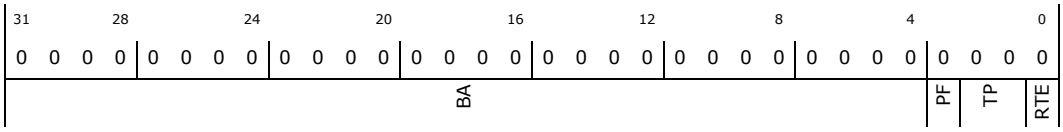
the I/O mapped registers defined in Memory Registers. Note that although 16 bytes of locations are allocated, only 8 bytes are used as SINDX and SDATA registers; with the remaining 8 bytes preserved for future enhancement.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ABAR: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0h RW	**Base Address (BA):** When programming interface is non IDE, this is base address of register memory space (aligned to 2 KB). Bits 31:11 are RW, bits 10:4 are RO of 0; When programming interface is IDE, this is base address of the I/O space. Bits 31:16 are RO of 0, bits 15:4 are RW
3	0h RO	**Prefetchable (PF):** When programming interface is non IDE, this indicates that this range is not prefetch-able
2:1	0h RO	**Type (TP):** When programming interface is non IDE, this indicates that this range can be mapped anywhere in 32-bit address space
0	0h RO	**Resource Type Indicator (RTE):** When programming interface is non IDE, this indicates a request for register memory space; When programming interface is IDE, this indicates a request for IO space.

13.5.16 Sub System Identifiers (SS)—Offset 2Ch

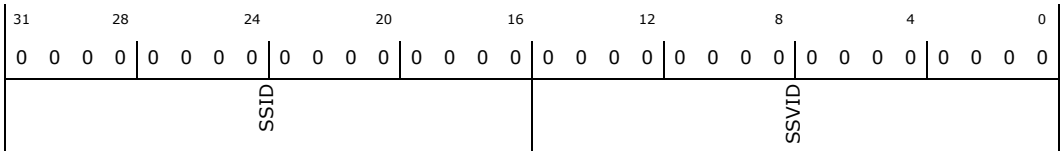
This register is initialized to logic 0 by the assertion of Backbone Reset. This register can be written only once after Backbone Reset de-assertion.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SS: [B:0, D:19, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	0000h RW/O	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

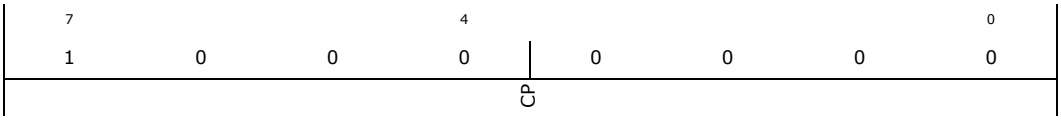
13.5.17 Capabilities Pointer (CAP)—Offset 34h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

CAP: [B:0, D:19, F:0] + 34h

Default: 80h



Bit Range	Default & Access	Description
7:0	80h RW/L	**Capability Pointer (CP):** Indicates that the first capability pointer offset is offset 80h (the Message Signaled Interrupt capability). The following capability structures are linked by default which is meant for non-IDE mode: CAP.CP - 80h (MSI) - 70h (PCI Power) - A8h (SATA) - 00h end. BIOS may alter the capability structure list above (by programming a leading capability structure's Next Pointer field) if BIOS wants to bypass any specific capability.[Br] If BIOS intends to operate in IDE mode, BIOS is requested to program this field to 70h and the subsequent capability list as such: CAP.CP - 70h (PCI Power) - end. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO.

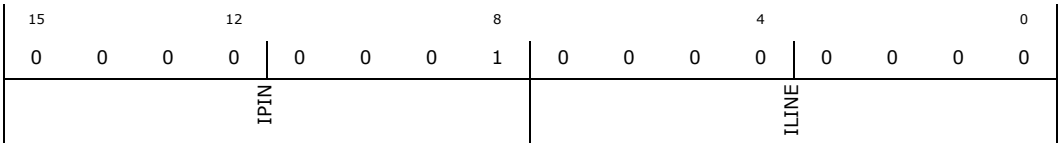
13.5.18 Interrupt Information (INTR)—Offset 3Ch

Access Method

Type: PCI Configuration Register (Size: 16 bits)

INTR: [B:0, D:19, F:0] + 3Ch

Default: 0100h



Bit Range	Default & Access	Description
15:8	01h RO	**Interrupt Pin (IPIN):** This register tells which interrupt pin the device function uses. A value of 1 corresponds to INTA#. A value of 2 corresponds to INTB#. A value of 3 corresponds to INTC#. A value of 4 corresponds to INTD#.
7:0	00h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

13.5.19 Minimum Grant (MGNT)—Offset 3Eh

Access Method

Type: PCI Configuration Register (Size: 8 bits)

MGNT: [B:0, D:19, F:0] + 3Eh

Default: 00h

Bit Range	Default & Access	Description
7:0	00h RO	**MGNT:** Minimum Grant

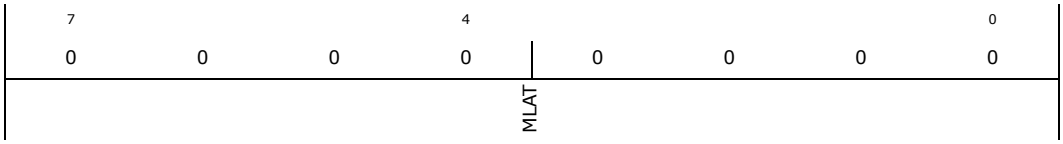
13.5.20 Maximum Latency (MLAT)—Offset 3Fh

Access Method

Type: PCI Configuration Register (Size: 8 bits)

MLAT: [B:0, D:19, F:0] + 3Fh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**MLAT:** Maximum Latency

13.5.21 Primary Timing (PTIM)—Offset 40h

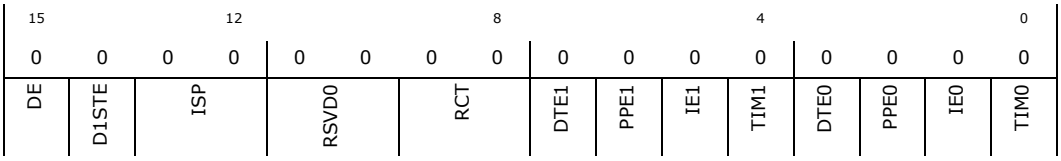
This controls the timings driven on the parallel cable.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PTIM: [B:0, D:19, F:0] + 40h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RW	**Decode Enable (DE):** Enables the SATA Controller to decode the Command Blocks (1F0-1F7h for primary, 170-177h for secondary or their native BAR equivalents) and Control Block (3F6h for primary and 376h for secondary or their native BAR equivalents). This bit still has functionality in SATA - if this bit is not set, the port that is mapped to this range will not be decoded.
14	0h RW	**Device 1 Separate Timing Enable (D1STE):** This register is not used by SATA controller.
13:12	0h RW	**IORDY Sample Point (ISP):** This register is not used by SATA controller.
11:10	0b RO	**RSVD0:** Reserved
9:8	0h RW	**Recovery Time (RCT):** This register is not used by SATA controller.
7	0h RW	**Device 1 DMA Timing Enable (DTE1):** This register is not used by SATA controller.
6	0h RW	**Device 1 Prefetch/Posting Enable (PPE1):** This register is not used by SATA controller.
5	0h RW	**Device 1 IORDY Sample Point Enable (IE1):** This register is not used by SATA controller.
4	0h RW	**Device 1 Fast Timing Bank (TIM1):** This register is not used by SATA controller.
3	0h RW	**Device 0 DMA Timing Enable (DTE0):** This register is not used by SATA controller.
2	0h RW	**Device 0 Prefetch/Posting Enable (PPE0):** This register is not used by SATA controller.
1	0h RW	**Device 0 IORDY Sample Point Enable (IE0):** This register is not used by SATA controller.
0	0h RW	**Device 0 Fast Timing Bank (TIM0):** This register is not used by SATA controller.

13.5.22 Secondary Timing (STIM)—Offset 42h

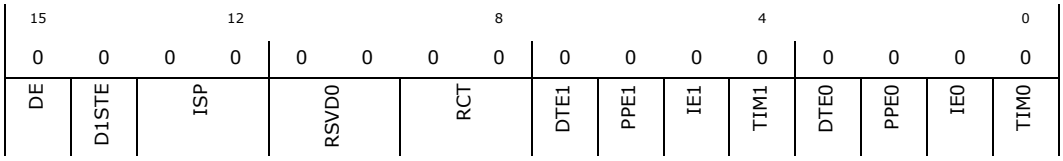
This controls the timings driven on the parallel cable.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

STIM: [B:0, D:19, F:0] + 42h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RW	**Decode Enable (DE):** Enables the SATA Controller to decode the Command Blocks (1F0-1F7h for primary, 170-177h for secondary or their native BAR equivalents) and Control Block (3F6h for primary and 376h for secondary or their native BAR equivalents). This bit still has functionality in SATA - if this bit is not set, the port that is mapped to this range will not be decoded.
14	0h RW	**Device 1 Separate Timing Enable (D1STE):** This register is not used by SATA controller.
13:12	0h RW	**IORDY Sample Point (ISP):** This register is not used by SATA controller.
11:10	0b RO	**RSVD0:** Reserved
9:8	0h RW	**Recovery Time (RCT):** This register is not used by SATA controller.
7	0h RW	**Device 1 DMA Timing Enable (DTE1):** This register is not used by SATA controller.
6	0h RW	**Device 1 Prefetch/Posting Enable (PPE1):** This register is not used by SATA controller.
5	0h RW	**Device 1 IORDY Sample Point Enable (IE1):** This register is not used by SATA controller.
4	0h RW	**Device 1 Fast Timing Bank (TIM1):** This register is not used by SATA controller.
3	0h RW	**Device 0 DMA Timing Enable (DTE0):** This register is not used by SATA controller.
2	0h RW	**Device 0 Prefetch/Posting Enable (PPE0):** This register is not used by SATA controller.
1	0h RW	**Device 0 IORDY Sample Point Enable (IE0):** This register is not used by SATA controller.
0	0h RW	**Device 0 Fast Timing Bank (TIM0):** This register is not used by SATA controller.

13.5.23 Device 1 IDE Timing (D1TIM)—Offset 44h

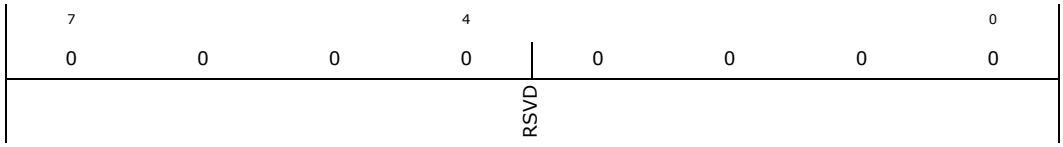
This register is not used by SATA controller.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

D1TIM: [B:0, D:19, F:0] + 44h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RW	**RSVD:** Reserved

13.5.24 Synchronous DMA Control (Synchronous_DMA_Control)—Offset 48h

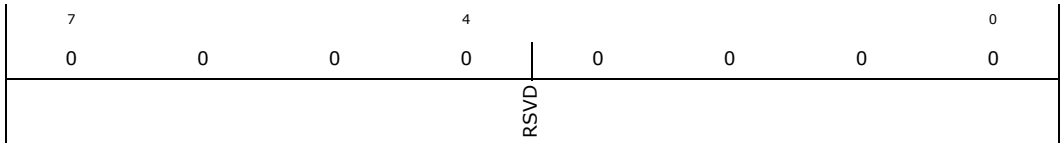
This register is not used by SATA controller.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Synchronous_DMA_Control: [B:0, D:19, F:0] + 48h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RW	**RSVD:** Reserved

13.5.25 Synchronous_DMA_Timing—Offset 4Ah

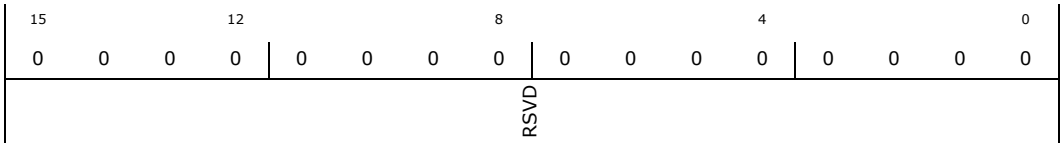
This register is not used by SATA controller.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Synchronous_DMA_Timing: [B:0, D:19, F:0] + 4Ah

Default: 0000h



Bit Range	Default & Access	Description
15:0	0h RW	**RSVD:** Reserved

13.5.26 IDE I/O Configuration (IIOC)—Offset 54h

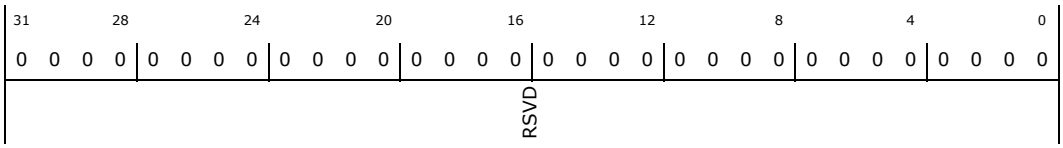
This register is not used by SATA controller.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IIOC: [B:0, D:19, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**RSVD:** Reserved

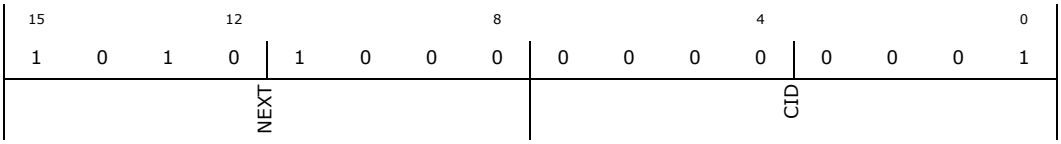
13.5.27 PCI Power Management Capability ID (PID)—Offset 70h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PID: [B:0, D:19, F:0] + 70h

Default: A801h



Bit Range	Default & Access	Description
15:8	A8h RW/L	**Next Capability (NEXT):** A8h is location of the Serial ATA Capability structure. This is recommended for non-IDE mode. If the controller is to operate in IDE mode, BIOS is requested to program this field to 00h indicating the end (recommended setting). The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO.
7:0	01h RO	**Cap ID (CID):** Indicates that this pointer is a PCI power management capability.

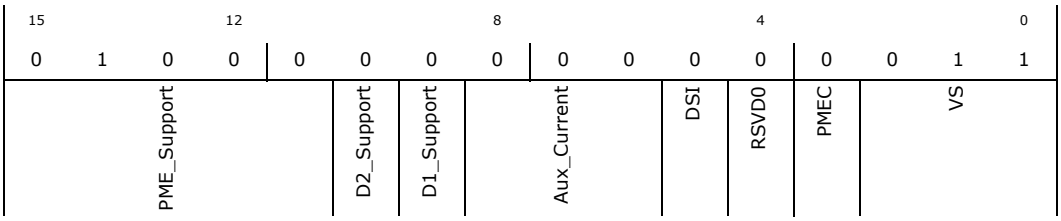
13.5.28 PCI Power Management Capabilities (PC)—Offset 72h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PC: [B:0, D:19, F:0] + 72h

Default: 4003h



Bit Range	Default & Access	Description
15:11	08h RO	**PME_Support:** By default with CC.SCC=01h, the default value is 00000 which indicates no PME Support in IDE mode. When CC.SCC is not 01h in non-IDE mode, the default value is 01000 which indicates PME# can be generated from the D3HOT state in the SATA controller.
10	0h RO	**D2_Support:** The D2 state is not supported.
9	0h RO	**D1_Support:** The D1 state is not supported.
8:6	0h RO	**Aux_Current:** PME# from D3COLD state is not supported, therefore this field is 000b.
5	0h RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.

Bit Range	Default & Access	Description
4	0b RO	**RSVD0:** Reserved
3	0h RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	3h RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

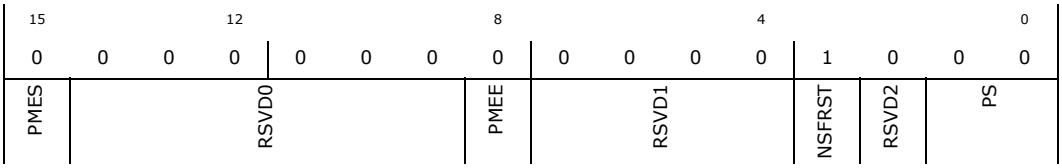
13.5.29 PCI Power Management Control and Status (PMCS)—Offset 74h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PMCS: [B:0, D:19, F:0] + 74h

Default: 0008h



Bit Range	Default & Access	Description
15	0h RW	**PME Status (PMES):** This bit is set when a PME event is to be requested, and if this bit is set and PMEE is set, a PME# will be generated. -Note: Whenever CC.SCC=01h either by default or just being updated, hardware shall automatically change the attribute to RO of 0.
14:9	0b RO	**RSVD0:** Reserved
8	0h RW	**PME Enable (PMEE):** When CC.SCC is not 01h, this bit is RW. When set, the SATA controller generates PME# from D3HOT on a wake event. Whenever CC.SCC=01h either by default or just being updated, hardware shall automatically change the attribute to RO of 0 since there is no PME Support in IDE mode. Note: Software is advised to clear PMEE together with PMES prior to changing CC.SCC thru MAP.SMS.
7:4	0b RO	**RSVD1:** Reserved
3	1h RO	**No Soft Reset (NSFRST):** A 1 indicates that devices transitioning from D3hot to D0 because of Power_State commands do not perform an internal reset. Configuration context is preserved. Upon transition from the D3hot to the D0 initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the Power_State bits. Regardless of this bit, the controller transition from D3hot to the D0 by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.
2	0b RO	**RSVD2:** Reserved
1:0	0h RW	**Power State (PS):** This field is used both to determine the current power state of the SATA Controller and to set a new power state. The values are: 00 = D0 state; 11 = D3HOT state. When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a 10 or 01 to these bits, the write will be ignored. Refer to PCI PM specification section 8.2.2. on software requirements in ensuring I/O space, memory space and Bus Master are disabled prior to entering D3 state.

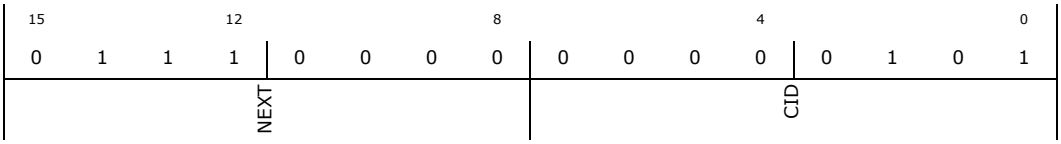
13.5.30 Message Signaled Interrupt Identifier (MID)—Offset 80h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MID: [B:0, D:19, F:0] + 80h

Default: 7005h



Bit Range	Default & Access	Description
15:8	70h RW/L	**Next Pointer (NEXT):** Indicates the next item in the list is the PCI power management pointer. This is the recommended value. BIOS may program this field to A8h indicating that the next item is Serial ATA Capability structure. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO.
7:0	05h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

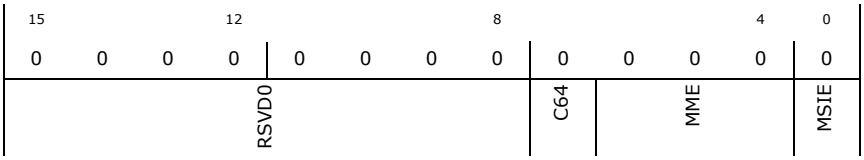
13.5.31 Message Signaled Interrupt Message Control (MC)—Offset 82h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MC: [B:0, D:19, F:0] + 82h

Default: 0000h



Bit Range	Default & Access	Description
15:8	0b RO	**RSVD0:** Reserved
7	0h RO	**64 Bit Address Capable (C64):** Capable of generating a 32-bit message only.
6:4	0h RO	**Multiple Message Enable (MME):** When this field is cleared to 000 (and MSIE is set), only a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0].
0	0h RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. Note that CMD.ID bit has not effect on MSI. Software must clear this bit to 0 to disable MSI first before changing the number of messages allocated in the MMC field. Software must also make sure this bit is cleared to 0 when operating in legacy mode (for AHCI SKUs when GHC.AE = 0). This bit is RW when CC.SCC is not 01h and is read-only 0 when CC.SCC is 01h.

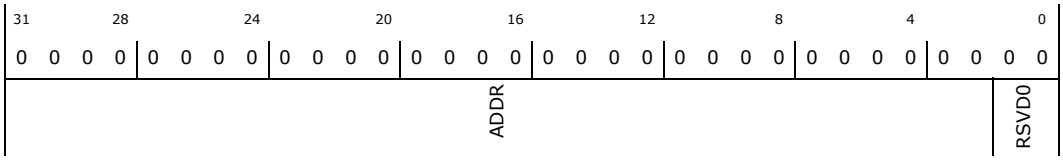
13.5.32 Message Signaled Interrupt Message Address (MA)—Offset 84h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MA: [B:0, D:19, F:0] + 84h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DWORD aligned.
1:0	0b RO	**RSVD0:** Reserved

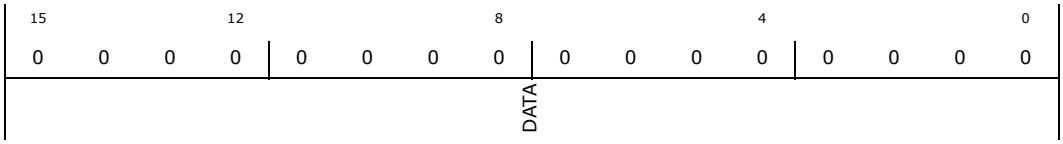
13.5.33 Message Signaled Interrupt Message Data (MD)—Offset 88h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MD: [B:0, D:19, F:0] + 88h

Default: 0000h



Bit Range	Default & Access	Description
15:0	0h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction.

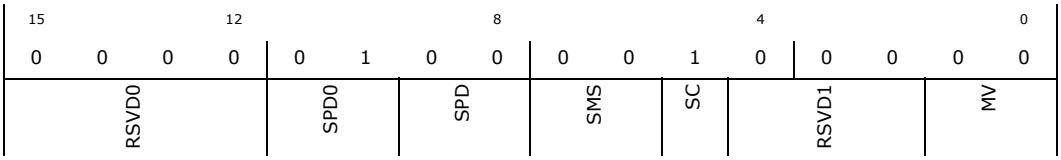
13.5.34 Port Mapping Register (MAP)—Offset 90h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MAP: [B:0, D:19, F:0] + 90h

Default: 0420h



Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:10	1h RO	**SATA Port Disable (SPD0):** A 1 in a bit position corresponding to the SATA port prevents the SATA port from being enabled via config PCS.PxE. Write of 1 to PCS.PxE has no effect when the corresponding SPD[x] bit is 1. In preventing a port(s) from being enabled, BIOS shall first configure MAP.SPD. And only then BIOS configures the PCS.PxE.
9:8	0h RO	**SATA Port Disable (SPD):** A 1 in a bit position corresponding to the SATA port prevents the SATA port from being enabled via config PCS.PxE. Write of 1 to PCS.PxE has no effect when the corresponding SPD[x] bit is 1. In preventing a port(s) from being enabled, BIOS shall first configure MAP.SPD. And only then BIOS configures the PCS.PxE.
7:6	0h RW	**SATA Mode Select (SMS):** Software (SW) programs these bits to control the mode in which the SATA HBA should operate: 00b = IDE mode which requires LBC01.LBGE=1 (refer to LBC01, LBC23 and LBC45 register in SIR register space); 01b = AHCI mode; 10b = RAID mode; 11b = Reserved. Notes: SW shall not manipulate MAP.SMS during runtime operation; that is, the OS will not do this. The BIOS may choose to switch from one mode to another during POST. IDE mode can be selected when AHCI and/or RAID are enabled. After switching from AHCI/RAID back to IDE mode, the number of usable ports on SATA Controller 1 shall be reduced to 4, dependent on SKUs. AHCI mode may only be selected when MV = 00b. AHCI mode may be selected when RAID feature is enabled by fuse. VLV does not support RAID mode. Programming these bits with values that are illegal will result in-deterministic behavior by the HW.
5	1h RW	**SATA Port-to-Controller Configuration (SC):** This bit changes number of SATA port availability within each SATA controller. When MAP.SPD[5] is 1 and MAP.SPD[4] is 1, this bit is reserved and is read-only 1 else it's RW-zero. When this bit is 0: Up to 2 SATA ports are available in the SATA controller 1 with port[1:0]. When this bit to 1: Up to 2 SATA ports are available in the SATA controller 1 with port [1:0]. For SMS=IDE mode, this bit should be 0 (note that this irrespective of the number of SATA ports). The number of port availability in this controller shall be discoverable thru this controller's config PCS.PxE, AHCI CAP.NP and AHCI PI[x] register fields. Prior to changing the state of this bit, all ports must be in quiescent state with no commands outstanding. Refer to Single and Dual Controller Switching Requirement for additional software and hardware requirements.
4:2	0b RO	**RSVD1:** Reserved
1:0	0h RO	**Map Value (MV):** This register is reserved.

13.5.35 Port Control and Status (PCS)—Offset 92h

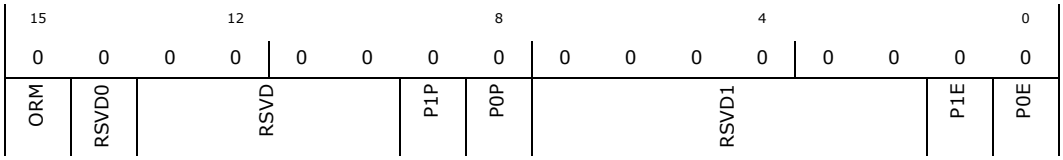
By default, the SATA ports are set (by hardware) to the disabled state (e.g. bits[5:0] == 0) as a result of an initial power on reset. When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices. Note: AHCI specific notes: If an AHCI-aware or RAID enabled operating system is being booted then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the OS. Once the AHCI aware OS is booted it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port's PxSCTL.DET and PxCMD.SUD fields. Because an AHCI or RAID aware OS will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to 1 prior to booting the OS, regardless as to whether or not a device is currently on the port.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCS: [B:0, D:19, F:0] + 92h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RW	**OOB Retry Mode (ORM):** When cleared, the SATA controller will not retry after an OOB failure. When set, the SATA controller will continue to retry after an OOB failure until successful (infinite retry). BIOS is requested to program this field to 1.
14	0b RO	**RSVD0:** Reserved
13:10	0h RO	**RSVD:** Reserved
9	0h RO	**Port 1 Present (P1P):** Same as P0P, except for port 1.
8	0h RO	**Port 0 Present (P0P):** When set, the SATA controller has detected the presence of a device on port 0. It may change at any time. Clearing P0E bit leads to clearing of this bit after implementation delay. Note: For system software that intends to clear all PCS.PxE bits that are previously 1 to 0 and then to 1 again in two consecutive write cycles, software shall poll on this bit being 0 before setting P0E bit to 1.
7:2	0b RO	**RSVD1:** Reserved
1	0h RW	**Port 1 Enabled (P1E):** When MAP.SPD[1] is 1, this bit is reserved and read-only 0. Otherwise if none of the above is true, this bit is RW and same as P0E but for port 1 and takes precedence over P1CMD.SUD.
0	0h RW	**Port 0 Enabled (P0E):** When MAP.SPD[0] is 1, this bit is reserved and read-only 0. When set, the port is enabled. When cleared, the port is disabled. When enabled, the port can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the off state and cannot detect any devices. This bit takes precedence over P0CMD.SUD. Note: The recommendation for software code that intends to clear all PCS.PxE bits that are previously 1 to 0 and then to 1 again immediately shall refer to the polling requirement as described in P0P register bit. At any time that BIOS or software is clearing PCS.PxE from 1 to 0, due to time needed for port staggering hardware process (up to 2 ports) to complete, BIOS and software shall delay the write to set the TM.PCD register by 1.4us.

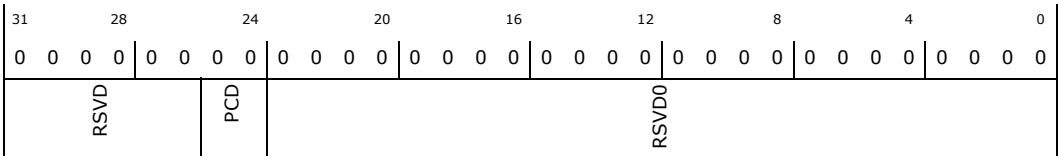
13.5.36 Test Mode Register (TM)—Offset 94h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

TM: [B:0, D:19, F:0] + 94h

Default: 00000000h



Bit Range	Default & Access	Description
31:26	0h RO	**Reserved (RSVD):** Reserved.
25:24	0h RW	**Port Clock Disable (PCD):** When any of these bits is set to 1, the backbone clock driven to the associated port logic is gated and will not toggle. When this bit is cleared to 0, all clocks to the associated port logic will operate normally.
23:0	0b RO	**RSVD0:** Reserved

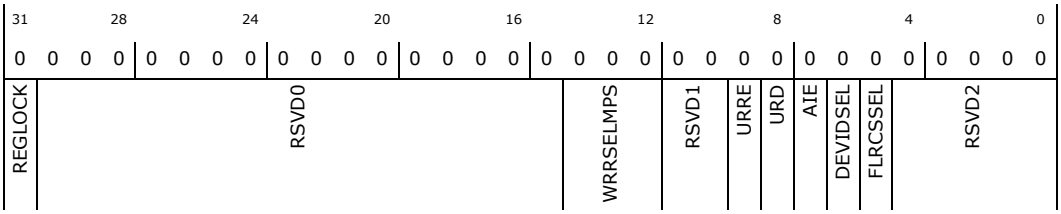
13.5.37 SATA General Configuration (SATAGC)—Offset 9Ch

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SATAGC: [B:0, D:19, F:0] + 9Ch

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW/O	**Register Lock (REGLOCK):** BIOS can set this bit to 1 to lock the following registers with RW/L attribute: CAP,CP, MID.NEXT, PIE.NEXT, SATACR0.NEXT. Once locked the register attribute of above list changes from RW/L to RO holding the existing value. BIOS is requested to program this field to 1 prior to handle off to OS. If BIOS needs the SATA host controller to change operation a few times (that is, changing CC.SCC mode) and need different capability structures for each specific operation mode, BIOS need not activate the lock until BIOS is ready to hand off to OS. BIOS may need to separate write access to this byte offset (x9Fh) from write to the lower 3-byte of the dword (x9C-9Eh) if there is a need to program the lower 3-byte dword location early during boot process.
30:15	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
14:12	0h RW	**Write Request_Size Select/Max_Payload_Size (WRRSELMPS):** These two bits select the max write request size that SATA host controller will initiate for DMA write to memory. SATA host controller will internally break up larger write request based on these bits. The request is address-aligned to the selected size. Defined encodings for this field are: 000b = 128 address aligned bytes max payload size; 111b = 64 address aligned bytes max payload size. All other values are reserved for SATA host controller.
11:10	0b RO	**RSVD1:** Reserved
9	0h RW	**Unsupported Request Reporting Enable (URRE):** If set to 1 by software, it allows reporting of an Unsupported Request as a system error. If both URRE and PCI configuration SERR# Enable registers are set to a 1, then the agent must set the Signaled System Error bit in the PCI Status register and send a DO_SERR message in IOSF-SB interface.
8	0h RW/1C	**Unsupported Request Detected (URD):** Set to 1 by hardware upon detecting an Unsupported Request on IOSF Primary interface that is not considered Advisory Non-Fatal. Cleared to 0 by SW.
7	0h RW/O	**Alternate ID Enable (AIE):** When programmed to 0, HW will report the following device id's: 2822h for desktop or 282Ah for mobile. When programmed to a 1, HW will not report these device id's. The value is product specific. Note: Programming this bit to a 1 will prevent the Windows in-box version of the Intel AHCI driver from loading on the platform - will require that the user perform an 'F6' install of the Intel driver that is appropriate for the reported DID. This field is applicable when the AHCI is configured for RAID mode of operation. It has no impact for AHCI and IDE modes of operation. Note: BIOS is recommended to program this bit prior to programming the MAP.SMS field to reflect RAID. This field is reset by Backbone Reset and BIOS is required to reprogram the value (either 0 or 1) after resuming from S3, S4 or S5. This insures that the value is properly and cannot be changed during runtime.
6	0h RW/O	**AIE0 DevID Selection (DEVIDSEL):** This register allows BIOS to select Device ID when AIE=0 and Server Feature Disable Fuse 7 =0. This bit only has effect in Desktop SKU. In Mobile SKU this bit has no effect at all. Refer to config register offset 09h PI for usage. 0: 2822h; 1: 2826h. NOTE: When Server Feature (SATA AIE DEVIDSEL) Disable Fuse 7 is programmed to 1, this disables the writeability of this DEVIDSEL register bit, and becomes RO with a value of 0, which only allows a choice of 2822h.
5	0h RW/O	**FLR Capability Selection (FLRCSSEL):** This allows the FLR Capability to be bypassed. Refer to config offset B0h. BIOS is requested to program this bit to 1 and config offset A8h SATACR0.NEXT to 00h.
4:0	0b RO	**RSVD2:** Reserved

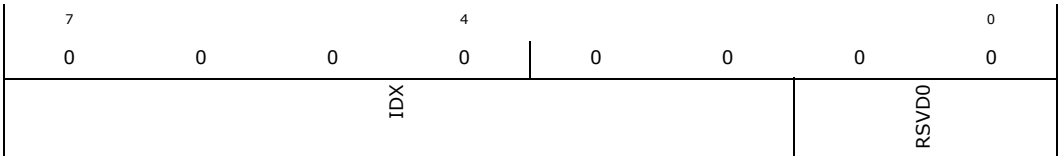
13.5.38 SATA Initialization Register Index (SIRI)—Offset A0h

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SIRI: [B:0, D:19, F:0] + A0h

Default: 00h



Bit Range	Default & Access	Description
7:2	00h RW	**Index (IDX):** 6-bit index pointer into the 256-byte space. Data is written into the SIRD register and read from the SIRD register. This point to a DWord register. The byte enables on the SIRD register affect what will be written. Note that this 256-byte register space setting is applicable to all ports in both SATA controllers 1 and 2 (if supported). Refer to SATA Initialization Register section for detail of the register space.
1:0	0b RO	**RSVD0:** Reserved

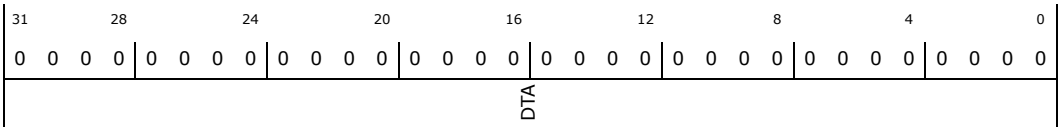
13.5.39 SATA Initialization Register Data (SIRD)—Offset A4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SIRD: [B:0, D:19, F:0] + A4h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Data (DTA):** 32-bit data value that is written to the register pointed to by SIRI, or read from the register pointed to by SIRI.

13.5.40 Serial ATA Capability Register 0 (SATACR0)—Offset A8h

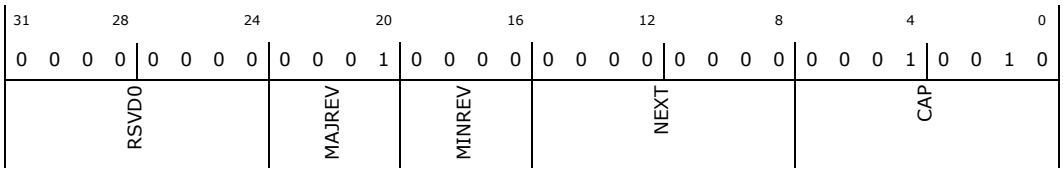
This register shall be read-only 0 when CC.SCC is 01h. Note that the SATACR0.NEXT is not changed from RO to become RWO because there is an existing method (SATAGC.FLRCSSEL bit) to bypass the FLR Capability structure. And FLR Capability ID.NEXT is already indicating end of capability structure, it does not need change to be RWO.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SATACR0: [B:0, D:19, F:0] + A8h

Default: 00100012h



Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23:20	1h RO	**Major Revision (MAJREV):** Major revision number of the SATA Capability Pointer implemented.
19:16	0h RO	**Minor Revision (MINREV):** Minor revision number of the SATA Capability Pointer implemented.
15:8	00h RW/L	**Next Capability Pointer (NEXT):** 00h indicating the final item in the Capability List. The RW/L register attribute allows for flexibility in determining the capability structure available in this PCI function. Refer to SATAGC.REGLOCK description in order to lock the register to become RO.
7:0	12h RO	**Capability ID (CAP):** The value of 12h has been assigned by the PCI SIG to designate the SATA Capability pointer.

13.5.41 Serial ATA Capability Register 1 (SATACR1)—Offset ACh

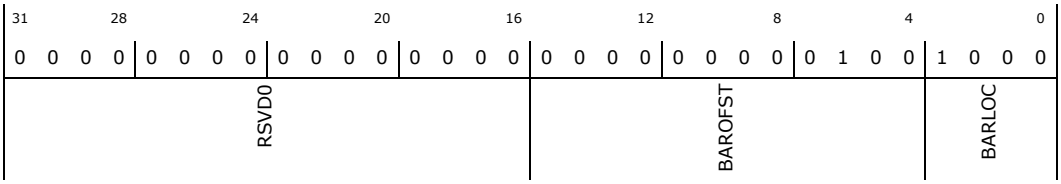
This register shall be read-only 0 when CC.SCC is 01h.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SATACR1: [B:0, D:19, F:0] + ACh

Default: 00000048h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:4	004h RO	**BAR Offset (BAROFST):** Indicates the offset into the BAR where the AHCI Index/Data pair are located (in Dword granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR (BAR4). A value of 004h indicates offset 10h. 000h = 0h offset; 001h = 4h offset; 002h = 8h offset; 003h = Ch offset; 004h = 10h offset... FFFh = 3FFFh offset (max 16 KB)
3:0	8h RO	**BAR Location (BARLOC):** Indicates the absolute PCI Configuration Register address of the BAR containing the Index/Data pair (in Dword granularity). The Index and Data I/O registers reside within the space defined by LBAR (BAR4) in the SATA controller. A value of 8h indicates offset 20h, which is LBAR (BAR4). 0000 - 0011b = reserved; 0100b = 10h =) BAR0; 0101b = 14h =) BAR1; 0110b = 18h =) BAR2; 0111b = 1Ch =) BAR3; 1000b = 20h =) LBAR; 1001b = 24h =) BAR5; 1010 - 1110b = reserved; 1111b = Index/Data pair in PCI Configuration space which is not supported.

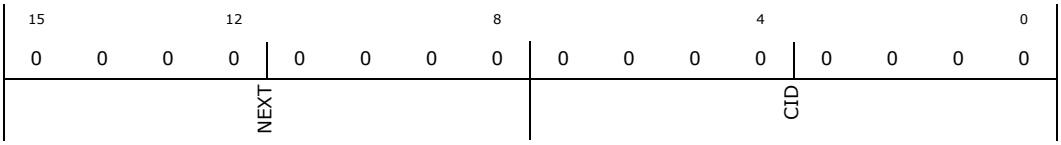
13.5.42 FLR Capability ID (FLRCID)—Offset B0h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

FLRCID: [B:0, D:19, F:0] + B0h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**Next Capability (NEXT):** 00h indicating the final item in the Capability List.
7:0	00h RO	**Capability ID (CID):** The value of this field depends on the FLRCSSEL bit. SATAGC.FLRCSSEL = 0, Capability ID = 13h; SATAGC.FLRCSSEL = 1, Capability ID = 00h (capability is bypassed).

13.5.43 FLR Control (FLRCTL)—Offset B4h

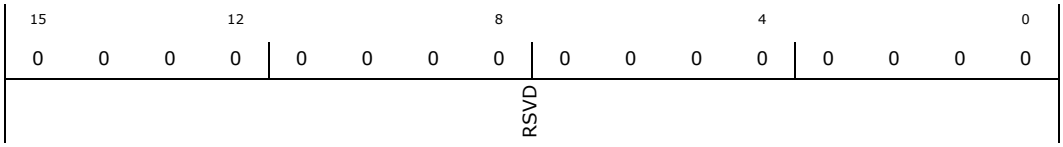
This register shall be read-only 0 when SATAGC.FLRCSSEL=1.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

FLRCTL: [B:0, D:19, F:0] + B4h

Default: 0000h



Bit Range	Default & Access	Description
15:0	0h RO	**RSVD:** Reserved

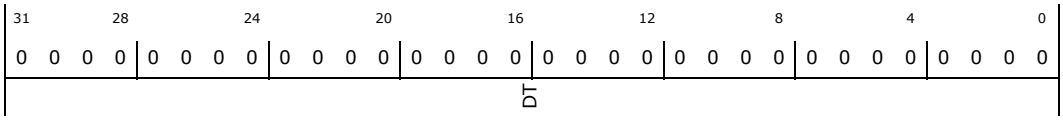
13.5.44 Scratch Pad (SP)—Offset D0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SP: [B:0, D:19, F:0] + D0h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Data (DT):** This is a read/write register that is available for software to use. No hardware action is taken on this register.

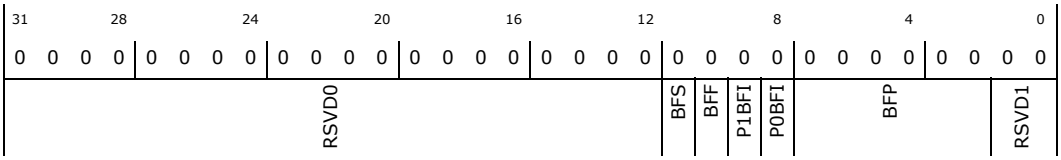
13.5.45 BIST FIS Control/Status (BFCS)—Offset E0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BFCS: [B:0, D:19, F:0] + E0h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0h RW	**BIST FIS Successful (BFS):** This bit is set any time that a BIST FIS transmitted by the SATA controller receives an R_OK completion status from the device
10	0h RW	**BIST FIS Failed (BFF):** This bit is set any time that a BIST FIS transmitted by the SATA controller receives an R_ERR completion status from the device
9	0h RW	**Port 1 BIST FIS Initiate (P1BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 1, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P1E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS.
8	0h RW	**Port 0 BIST FIS Initiate (P0BFI):** When a rising edge is detected on this bit, the SATA controller will initiate a BIST FIS to the device on port 0, using the parameters specified in this register and BFTD1 and BFTD2. The BIST FIS will only be initiated if a device is present and not in the partial or slumber states. After a BIST FIS is successfully completed, software must disable and re-enable PCS.P0E prior to attempting additional BIST FISes or to return the SATA controller to a normal operational mode. If the BIST FIS fails, as indicated by BFF in this register, software can clear and then set this bit to initiate another BIST FIS.
7:2	0h RW	**BIST FIS Parameters (BFP):** These bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in the BIST FIS transmitted by the SATA controller. This field is not port specific - its contents will be used for any BIST FIS initiated on the SATA controller. The specific bit definitions are: Bit 7 (T) Far End Transmit mode; bit 6 (A) Align Bypass mode; bit 5 (S) Bypass Scrambling; bit 4 (L) Far End Retimed Loopback; bit 3 (F) Far End Analog Loopback; bit 2 (P) Primitive bit for use with Transmit mode.
1:0	0b RO	**RSVD1:** Reserved

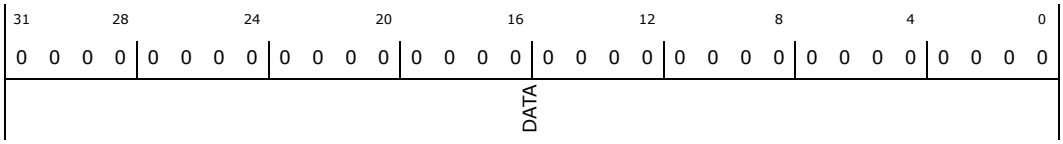
13.5.46 BIST FIS Transmit Data 1 (BFTD1)—Offset E4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BFTD1: [B:0, D:19, F:0] + E4h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the second DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 2nd DW regardless of whether or not the T bit is indicated in the BFCS register.

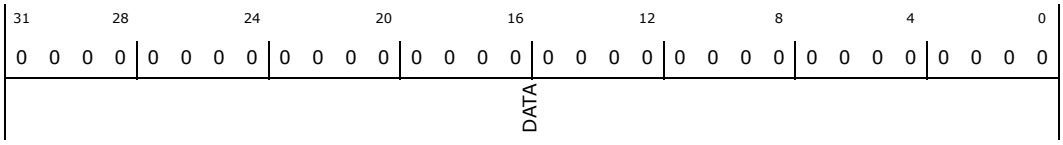
13.5.47 BIST FIS Transmit Data 2 (BFTD2)—Offset E8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

BFTD2: [B:0, D:19, F:0] + E8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**Data (DATA):** The data programmed into this register will form the contents of the third DW of any BIST FIS initiated by the SATA controller. This register is not port specific - its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWs of the BIST FIS are only meaningful when the T bit of the BIST FIS is set to indicate Far-End Transmit mode, this register's contents will be transmitted as the BIST FIS 3rd DW regardless of whether or not the T bit is set in the BFCS register.

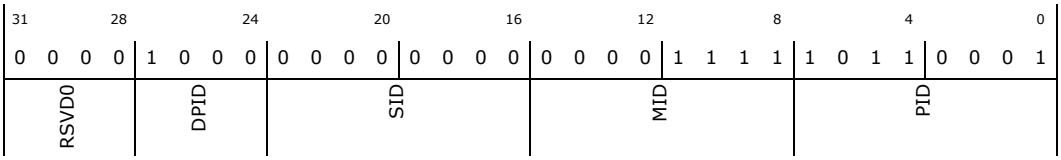
13.5.48 Manufacturing ID (MFID)—Offset F8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MFID: [B:0, D:19, F:0] + F8h

Default: 08000FB1h



Bit Range	Default & Access	Description
31:28	0b RO	**RSVD0:** Reserved
27:24	8h RO	**Dot portion of Process ID (DPID):** Indicates the dot. Process is reflected in bits [7:0]. The value is product specific.
23:16	0h RO	**Stepping Identifier (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. The value is product specific.
15:8	0Fh RO	**Manufacturer Identifier (MID):** Indicates Intel.
7:0	B1h RO	**Process/Dot Identifier (PID):** Indicates the Process. Dot is reflected in bits [27:24]. The value is product specific.

13.6 SATA Legacy IO Registers

Table 101. Summary of SATA Legacy I/O Registers—LBAR

Offset	Size	Register ID—Description	Default Value
0h	1	"Primary Command (PCMD)—Offset 0h" on page 172	00h
2h	1	"Primary Status (PSTS)—Offset 2h" on page 173	00h
4h	4	"Primary Descriptor Table Pointer (PDTP)—Offset 4h" on page 174	00000000h
8h	1	"Secondary Command (SCMD)—Offset 8h" on page 174	00h
Ah	1	"Secondary Status (SSTS)—Offset Ah" on page 175	00h
Ch	4	"Secondary Descriptor Table Pointer (SDTP)—Offset Ch" on page 176	00000000h
10h	4	"AHCI Index Register (INDEX)—Offset 10h" on page 176	00000000h
14h	4	"AHCI Data Register (DATA)—Offset 14h" on page 177	00000000h

13.6.1 Primary Command (PCMD)—Offset 0h

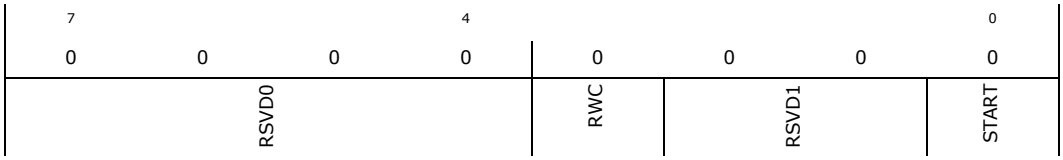
Access Method

Type: I/O Register (Size: 8 bits)

PCMD: [LBAR] + 0h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:4	0b RO	**RSVD0:** Reserved
3	0h RW	**Read / Write Control (RWC):** Sets the direction of the bus master transfer: 0 = memory to device, 1 = device to memory. This bit must not be changed when the bus master function is active.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**Start/Stop Bus Master (START):** Setting this bit enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit in PCI configuration space is also set. Clearing it halts bus master operation. All state information is lost when this bit is written to 0; Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active and the device has not yet finished its data transfer, the bus master command is said to be aborted. If this bit is cleared to 0 prior to the DMA data transfer being initiated by the drive in a device to memory data transfer, then not DMAT will be sent to terminate the data transfer. SW intervention (e.g. sending SRST) is required to reset the interface in this condition. This bit is intended to be cleared by software after the data transfer is completed - as indicated by either the ACT bit being cleared in the status register, or the I bit being set in the status register, or both.

13.6.2 Primary Status (PSTS)—Offset 2h

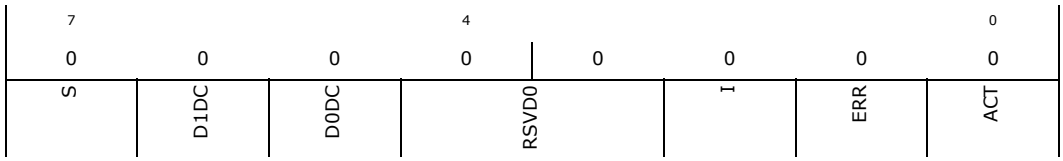
Access Method

Type: I/O Register
(Size: 8 bits)

PSTS: [LBAR] + 2h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00h



Bit Range	Default & Access	Description
7	0h RO	**Simplex Only (S):** This read-only bit indicates whether or not I both bus master channels (primary and secondary) can be operated at the same time. If the bit is a 0, then the channels operate independently and can be used at the same time. If the bit is a 1, then only one channel may be used at a time.
6	0h RW	**Device 1 DMA Capable (D1DC):** A scratch pad bit set by SW to indicate that device 1 of this channel is capable of DMA transfers. This bit has no effect on the hardware.
5	0h RW	**Device 0 DMA Capable (D0DC):** A scratch pad bit set by SW to indicate that device 0 of this channel is capable of DMA transfers. This bit has no effect on the hardware.
4:3	0b RO	**RSVD0:** Reserved
2	0h RW/1C	**Interrupt (I):** This bit is set when a device FIS is received with the I bit has been set provided that software has not disabled interrupt via the nIEN bit of Device Control Register.
1	0h RW/1C	**Error (ERR):** This bit is set when the controller encounters an error during the transfer and must stop the transfer. See Error Handling for the list of errors that set this bit.
0	0h RO	**Active (ACT):** Set by the host when the START bit is written to the Command register, and cleared by the host when the last transfer for a region is performed, where EOT for that region is set in the region descriptor, and when the START bit is cleared in the Command register and the controller has returned to an idle condition.

13.6.3 Primary Descriptor Table Pointer (PDTP)—Offset 4h

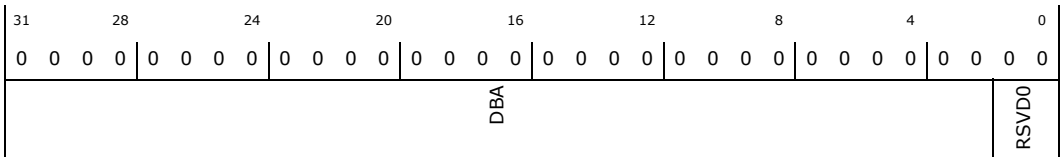
Access Method

Type: I/O Register
(Size: 32 bits)

PDTP: [LBAR] + 4h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**Descriptor Base Address (DBA):** Corresponds to A[31:2]. This table must not cross a 64K boundary in memory. When read, the current value of the pointer is returned
1:0	0b RO	**RSVD0:** Reserved

13.6.4 Secondary Command (SCMD)—Offset 8h

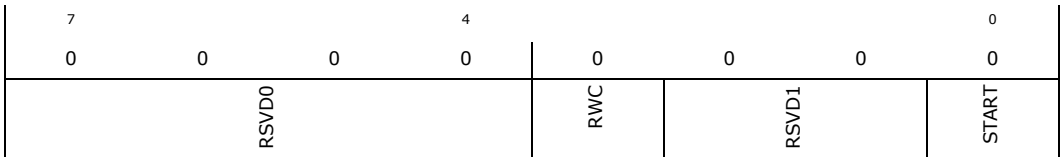
Access Method

Type: I/O Register
(Size: 8 bits)

SCMD: [LBAR] + 8h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:4	0b RO	**RSVD0:** Reserved
3	0h RW	**Read / Write Control (RWC):** Sets the direction of the bus master transfer: 0 = memory to device, 1 = device to memory. This bit must not be changed when the bus master function is active.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**Start/Stop Bus Master (START):** Setting this bit enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit in PCI configuration space is also set. Clearing it halts bus master operation.

13.6.5 Secondary Status (SSTS)—Offset Ah

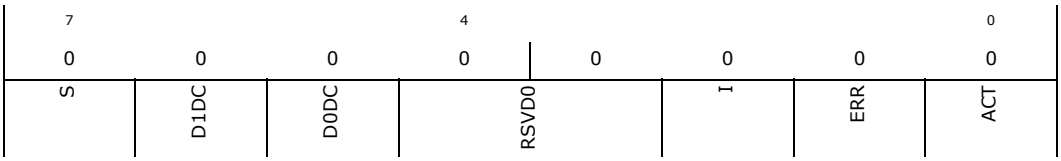
Access Method

Type: I/O Register
(Size: 8 bits)

SSTS: [LBAR] + Ah

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00h



Bit Range	Default & Access	Description
7	0h RO	**Simplex Only (S):** This read-only bit indicates whether or not I both bus master channels (primary and secondary) can be operated at the same time. If the bit is a 0, then the channels operate independently and can be used at the same time. If the bit is a 1, then only one channel may be used at a time.
6	0h RW	**Device 1 DMA Capable (D1DC):** A scratch pad bit set by SW to indicate that device 1 of this channel is capable of DMA transfers. This bit has no effect on the hardware.
5	0h RW	**Device 0 DMA Capable (D0DC):** A scratch pad bit set by SW to indicate that device 0 of this channel is capable of DMA transfers. This bit has no effect on the hardware.
4:3	0b RO	**RSVD0:** Reserved
2	0h RW/1C	**Interrupt (I):** This bit is set when a device FIS is received with the I bit has been set provided that software has not disabled interrupt via the nIEN bit of Device Control Register.
1	0h RW/1C	**Error (ERR):** This bit is set when the controller encounters an error during the transfer and must stop the transfer. See Error Handling for the list of errors that set this bit.
0	0h RO	**Active (ACT):** Set by the host when the START bit is written to the Command register, and cleared by the host when the last transfer for a region is performed, where EOT for that region is set in the region descriptor, and when the START bit is cleared in the Command register and the controller has returned to an idle condition.

13.6.6 Secondary Descriptor Table Pointer (SDTP)—Offset Ch

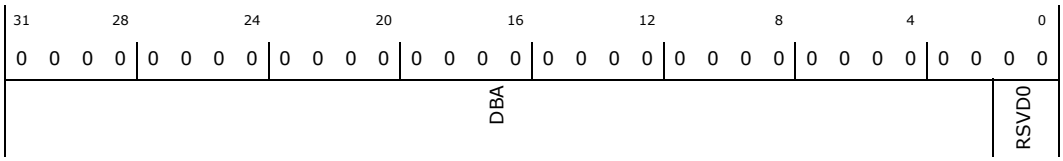
Access Method

Type: I/O Register
(Size: 32 bits)

SDTP: [LBAR] + Ch

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**Descriptor Base Address (DBA):** Corresponds to A[31:2]. This table must not cross a 64K boundary in memory. When read, the current value of the pointer is returned
1:0	0b RO	**RSVD0:** Reserved

13.6.7 AHCI Index Register (INDEX)—Offset 10h

This registers are only available if CC.SCC is not 01h to index into all memory registers defined in Memory Registers and the message buffer used for enclosure management. If CC.SCC is 01h, these AHCI Index Data Pair registers are not accessible and SINDEX/SDATA register pair shall be used to index into a subset of the memory registers defined in (See Memory Registers for more information on which registers could be indexed).

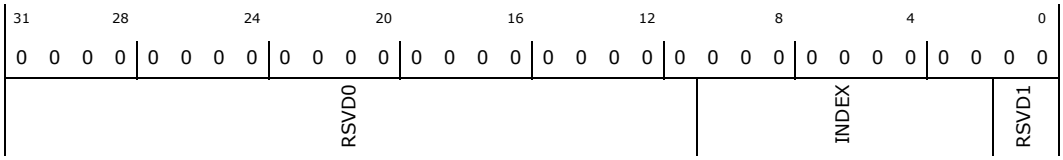
Access Method

Type: I/O Register
(Size: 32 bits)

INDEX: [LBAR] + 10h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RO	**RSVD0:** Reserved
10:2	000h RO	**Index (INDEX):** This Index register is used to select the Dword offset of the Memory Mapped AHCI register to be accessed. A Dword, Word or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	0b RO	**RSVD1:** Reserved

13.6.8 AHCI Data Register (DATA)—Offset 14h

This registers are only available if CC.SCC is not 01h to index into all memory registers defined in Memory Registers and the message buffer used for enclosure management. If CC.SCC is 01h, these AHCI Index Data Pair registers are not accessible and SINDEX/SDATA register pair shall be used to index into a subset of the memory registers defined in (See Memory Registers for more information on which registers could be indexed).

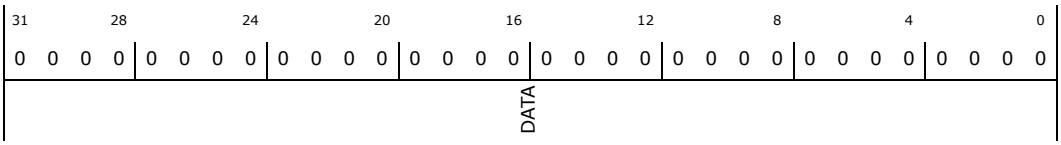
Access Method

Type: I/O Register (Size: 32 bits)

DATA: [LBAR] + 14h

LBAR Type: PCI Configuration Register (Size: 32 bits)
LBAR Reference: [B:0, D:19, F:0] + 20h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Data (DATA):** This Data register is a window through which data is read or written to the memory mapped register pointed to by the Index register. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by Index.

13.7 SATA Index Pair IO Registers

Table 102. Summary of SATA Index Pair I/O Registers—ABAR

Offset	Size	Register ID—Description	Default Value
0h	4	"Serial ATA Index (SINDX)—Offset 0h" on page 178	00000000h
4h	4	"Serial ATA Data (SDATA)—Offset 4h" on page 179	00000000h

13.7.1 Serial ATA Index (SINDX)—Offset 0h

All of these I/O registers are in the core well. They are exposed only when CC.SCC is 01h (that is, IDE programming interface). These are Index/Data Pair registers that are used to access the SerialATA superset registers (SerialATA Status, SerialATA Control and SerialATA Error). The I/O space for these registers is allocated through SIDPBA. Locations with offset from 08h to 0Fh are reserved for future expansion. Software write operations to the reserved locations shall have no effect while software read operations to the reserved locations shall return 0. Refer to Serial ATA Index/Data Pair Superset Registers for more details.

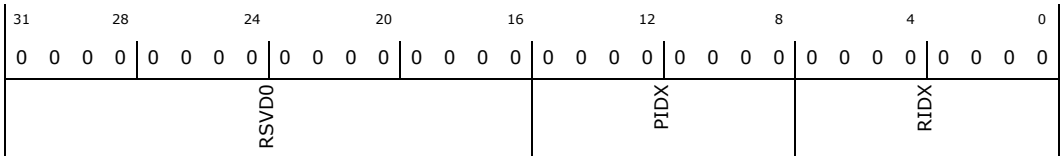
Access Method

Type: I/O Register
(Size: 32 bits)

SINDX: [ABAR] + 0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RW	**Port Index (PIDX):** This index field is used to specify the port of the SATA controller that the port specific SerialATA Status (SSTS), SerialATA Control (SCTL) and SerialATA Error (SERR) registers are to be read from or write to. 00h = Primary Master (Port 0); 01h = Primary Slave (Port 2); 02h = Secondary Master (Port 1); 03h = Secondary Slave (Port 3).
7:0	00h RW	**Register Index (RIDX):** This index field is used to specify one out of three registers currently being indexed into. These three registers are the Serial ATA superset SStatus, SControl and SError memory registers and are port specific, hence for this SATA controller, there are four sets of these registers. Refer to Offset 128h, 1A8h, 228h, 2A8h, 328h, 3A8h: PxSSTS - Port [0-5] Serial ATA Status, Offset 12Ch, 1ACh, 22Ch, 2ACh, 32Ch, 3ACh: PxSCTL - Port [0-5] Serial ATA Control, and Offset 130h, 1B0h, 230h, 2B0h, 330h, 3B0h: PxSERR - Port [0-5] Serial ATA Error for definitions of the SStatus, SControl and SError registers. 00h = SSTS; 01h = SCTL; 02h = SERR.

13.7.2 Serial ATA Data (SDATA)—Offset 4h

All of these I/O registers are in the core well. They are exposed only when CC.SCC is 01h (that is, IDE programming interface). These are Index/Data Pair registers that are used to access the SerialATA superset registers (SerialATA Status, SerialATA Control and SerialATA Error). The I/O space for these registers is allocated through SIDPBA. Locations with offset from 08h to 0Fh are reserved for future expansion. Software write operations to the reserved locations shall have no effect while software read operations to the reserved locations shall return 0. Refer to Serial ATA Index/Data Pair Superset Registers for more details.

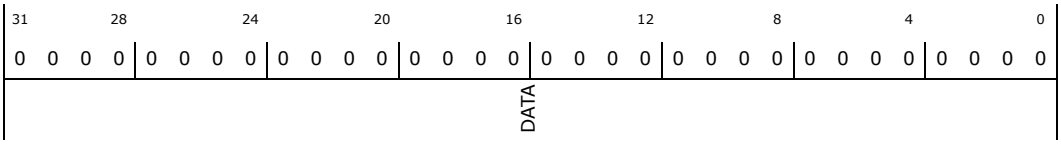
Access Method

Type: I/O Register (Size: 32 bits)

SDATA: [ABAR] + 4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Data (DATA):** This Data register is a window through which data is read or written to from the register pointed to by the Serial ATA Index (SINDX) register above. Note that a physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the default value is the same as the default value of the register pointed to by SINDX.RIDX field.

13.8 SATA AHCI Memory Mapped IO Registers

Table 103. Summary of SATA AHCI Memory Mapped I/O Registers—ABAR

Offset	Size	Register ID—Description	Default Value
0h	4	"HBA Capabilities (GHC_CAP)—Offset 0h" on page 181	DF20FF02h
4h	4	"HBA Capabilities (GHC_CAP)—Offset 0h" on page 181	00000000h
8h	4	"Interrupt Status (IS)—Offset 8h" on page 184	00000000h
Ch	4	"Ports Implemented (GHC_PI)—Offset Ch" on page 184	00000000h
10h	4	"AHCI Version (VS)—Offset 10h" on page 185	00010300h
24h	4	"HBA Capabilities Extended (GHC_CAP2)—Offset 24h" on page 186	0000003Ch
A0h	4	"Vendor Specific (VSP)—Offset A0h" on page 187	00000048h
A4h	4	"Vendor Specific Capabilities (VS_CAP)—Offset A4h" on page 188	018002FEh
C4h	2	"Premium Feature Block (PFB)—Offset C4h" on page 189	0000h
C8h	2	"SW Feature Mask (SFM)—Offset C8h" on page 190	003Fh
100h	4	"Port-Command List Base Address (PxCLB0)—Offset 100h" on page 191	00000000h
104h	4	"Port-Command List Base Address Upper 32-bits (PxCLBU0)—Offset 104h" on page 191	00000000h
108h	4	"Port-FIS Base Address (PxFB0)—Offset 108h" on page 192	00000000h
10Ch	4	"Port-FIS Base Address Upper 32-bits (PxFBU0)—Offset 10Ch" on page 192	00000000h
110h	4	"Port-Interrupt Status (PxIS0)—Offset 110h" on page 193	00000000h
114h	4	"Port-Interrupt Enable (PxIE0)—Offset 114h" on page 194	00000000h
118h	4	"Port-Command (PxCMD0)—Offset 118h" on page 196	00000004h
120h	4	"Port-Task File Data (PxTFD0)—Offset 120h" on page 198	0000007Fh
124h	4	"Port-Signature (PxSIG0)—Offset 124h" on page 199	FFFFFFFFh
128h	4	"Port-Serial ATA Status (PxSSTS0)—Offset 128h" on page 199	00000000h
12Ch	4	"Port-Serial ATA Control (PxSCTL0)—Offset 12Ch" on page 200	00000000h
130h	4	"Port-Serial ATA Error (PxSERR0)—Offset 130h" on page 201	00000000h
134h	4	"Port-Serial ATA Active (PxSACT0)—Offset 134h" on page 202	00000000h
138h	4	"Port-Commands Issued (PxCI0)—Offset 138h" on page 202	00000000h
144h	4	"Port-Device Sleep (PxDEVSLP0)—Offset 144h" on page 203	1E022852h
180h	4	"Port-Command List Base Address (PxCLB1)—Offset 180h" on page 204	00000000h
184h	4	"Port-Command List Base Address Upper 32-bits (PxCLBU1)—Offset 184h" on page 204	00000000h
188h	4	"Port-FIS Base Address (PxFB1)—Offset 188h" on page 205	00000000h
18Ch	4	"Port-FIS Base Address Upper 32-bits (PxFBU1)—Offset 18Ch" on page 205	00000000h
190h	4	"Port-Interrupt Status (PxIS1)—Offset 190h" on page 206	00000000h
194h	4	"Port-Interrupt Enable (PxIE1)—Offset 194h" on page 207	00000000h
198h	4	"Port-Command (PxCMD1)—Offset 198h" on page 209	00000004h
1A0h	4	"Port-Task File Data (PxTFD1)—Offset 1A0h" on page 212	0000007Fh
1A4h	4	"Port-Signature (PxSIG1)—Offset 1A4h" on page 213	FFFFFFFFh
1A8h	4	"Port-Serial ATA Status (PxSSTS1)—Offset 1A8h" on page 213	00000000h
1ACh	4	"Port-Serial ATA Control (PxSCTL1)—Offset 1ACh" on page 214	00000000h
1B0h	4	"Port-Serial ATA Error (PxSERR1)—Offset 1B0h" on page 215	00000000h
1B4h	4	"Port-Serial ATA Active (PxSACT1)—Offset 1B4h" on page 216	00000000h

Table 103. Summary of SATA AHCI Memory Mapped I/O Registers—ABAR (Continued)

Offset	Size	Register ID—Description	Default Value
1B8h	4	"Port-Commands Issued (PxCI1)—Offset 1B8h" on page 217	00000000h
1C4h	4	"Port-Device Sleep (PxDEVSLP1)—Offset 1C4h" on page 217	1E022852h
580h	4	"Enclosure Management Message Format (EM_MF)—Offset 580h" on page 218	00000000h
584h	4	"Enclosure Management LED (EM_LED)—Offset 584h" on page 218	00000000h

13.8.1 HBA Capabilities (GHC_CAP)—Offset 0h

This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon Backbone Reset.

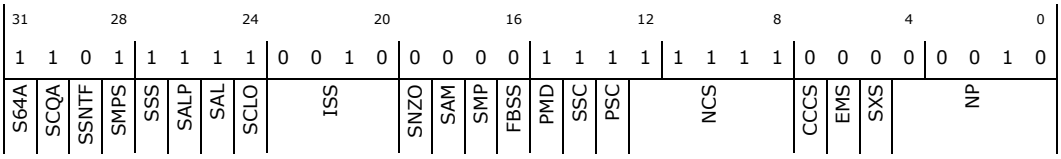
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHC_CAP: [ABAR] + 0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: DF20FF02h



Bit Range	Default & Access	Description
31	1h RW/O	**Supports 64-bit Addressing (S64A):** Indicates the S-ATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	1h RW/O	**Supports Native Command Queuing Acceleration (SCQA):** Indicates the SATA controller supports Serial-ATA Native Command Queuing. The HBA will handle DMA Setup FISes in hardware, including support for auto-activate optimization through the FIS.
29	0h RO	**Supports SNotification Register (SSNTF):** When set to 1, indicates that the HBA supports the PxSNTF (SNotification) register and its associated functionality. When cleared to 0, the HBA does not support the PxSNTF (SNotification) register and its associated functionality.
28	1h RW/O	**Supports Mechanical Presence Switch (SMPS):** When set to 1, the HBA supports mechanical presence switches on its ports for use in hot plug operations. When cleared to 0, this function is not supported. This value is loaded by the BIOS prior to OS initialization.
27	1h RW/O	**Supports Staggered Spin-up (SSS):** Indicates whether the S-ATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization.
26	1h RW/O	**Supports Aggressive Link Power Management (SALP):** Indicates the S-ATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process. When cleared to 0, software shall treat the PxCMD.ALPE and PxCMD.ASP bits as reserved.
25	1h RW/O	**Supports Activity LED (SAL):** Indicates the S-ATA controller supports a single output pin (SATALED#) which indicates activity.

Bit Range	Default & Access	Description
24	1h RW/O	**Supports Command List Override (SCLO):** When set to 1, indicates that the HBA supports the PxCMD.CLO bit and its associated function. When cleared to 0, The HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue software reset if these bits are still set from a previous operation.
23:20	2h RW/O	**Interface Speed Support (ISS):** Indicates the maximum speed the S-ATA controller can support on its ports. These encodings match the system software programmable PxSCTL.DET.SPD field. 0000 = Reserved; 0001 = Gen 1 (1.5 Gbps); 0010 = Gen 2 (3 Gbps); 0011 = Gen 3 (6 Gbps); 0100 - 1111 = Reserved.
19	0h RO	**Supports Non-Zero DMA Offsets (SNZO):** Reserved as per AHCI 1.3
18	0h RW/O	**Supports AHCI mode only (SAM):** The SATA controller may optionally support AHCI access mechanism only. A value of 0 indicates that in addition to the native AHCI mechanism (via ABAR), the SATA controller implements a legacy, task-file based register interface such as SFF-8038i. A value of 1 indicates that the SATA controller does not implement a legacy, task-file based register interface.
17	0h RO	**Supports Port Multiplier (SMP):** Not supported.
16	0h RO	**FIS-based Switching Supported (FBSS):** Not supported.
15	1h RO	**PIO Multiple DRQ Block (PMD):** If set to 1, the HBA supports multiple DRQ block data transfers for the PIO command protocol.
14	1h RW/O	**Slumber State Capable (SSC):** The SATA controller supports the slumber state.
13	1h RW/O	**Partial State Capable (PSC):** The SATA controller supports the partial state.
12:8	1Fh RO	**Number of Command Slots (NCS):** 1Fh indicating support for 32 slots.
7	0h RO	**Command Completion Coalescing Supported (CCCS):** When set to 1, indicates that the HBA supports command completion coalescing. When command completion coalescing is supported, the HBA has implemented the CCC_CTL and the CCC_PORTS global HBA registers. When cleared to 0, indicates that the HBA does not support command completion coalescing and the CCC_CTL and CCC_PORTS global HBA registers are not implemented.
6	0h RO	**Enclosure Management Supported (EMS):** Not supported
5	0h RW/O	**Supports External SATA (SXS):** When set to 1, indicates that the HBA has one or more Serial ATA ports that has a signal only connector that is externally accessible. If this bit is set, software may refer to the PxCMD.ESP bit to determine whether a specific port has its signal connector externally accessible as a signal only connector (that is, power is not part of that connector). When the bit is cleared to 0, indicates that the HBA has no Serial ATA ports that have a signal only connector externally accessible.
4:0	02h RO	**Number of Ports (NP):** 0's based value indicating the maximum number of ports supported. Note that the number of ports indicated in this field may be more than the number of ports indicated in the PI register. Number of ports shall be dependent on MAP.SC and PCIe/SATA multiplexing configuration where if ANY of these parameter disable a particular port then that port is disabled and not counted. The maximum number of ports supported by SIP is 2 and the least is 0 (that is, Function Disable). In the case of 0 port configuration, the value of NP is a don't care (while implementation has it fixed as 07h). Any combination in between is supported by SATA host controller. Indicates the number of supported ports.

13.8.2 Global HBA Control (GHC)—Offset 4h

This register controls various global actions of the HBA.

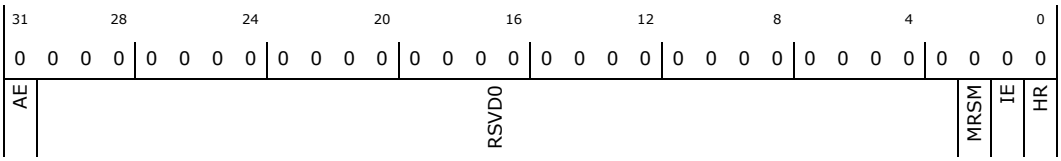
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHC: [ABAR] + 4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**AHCI Enable (AE):** When set, indicates that an AHCI driver is loaded and communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. When set, software shall only talk to the HBA using AHCI. The HBA will not have to allow command processing via both AHCI and legacy mechanisms. When cleared, software will only communicate with the HBA using legacy mechanisms. Software shall set this bit to 1 before accessing other AHCI registers. Note: The implementation of this bit is dependent upon the value of the CAP.SAM bit. If CAP.SAM is 0, then GHC.AE should be RW and shall have a reset value of 0. If CAP.SAM is 1, then AE shall be read only and shall have a reset value of 1.
30:3	0b RO	**RSVD0:** Reserved
2	0h RO	**MSI Revert to Single Message (MRSM):** When set to 1 by hardware, indicates that the HBA requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, the HBA has not reverted to single MSI mode (that is, hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME. The HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: MC.MSIE = 1 (MSI is enabled);) 0 (multiple messages requested); MC.MME) 0 (more than one message allocated); When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not reverting to that mode. The HBA shall always revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. Value of MRSM is a don't care when GHC.HR=1.
1	0h RW	**Interrupt Enable (IE):** This global bit enables interrupts from the HBA. When cleared (reset default), all interrupt sources from all ports are disabled. When set, interrupts are enabled.
0	0h RW/1S	**HBA Reset (HR):** When set by SW, this bit causes an internal reset of the HBA. All state machines that relate to data transfers and native command queuing will return to an idle condition, and all ports will be re-initialized via COMRESET. When the HBA has performed the reset action, it will reset this bit to 0. A software write of 0 will have no effect. For a description on which bits are reset when this bit is set, see the AHCI specification, section 10.3.3.

13.8.3 Interrupt Status (IS)—Offset 8h

This register indicates which of the ports within the controller have an interrupt pending and require service.

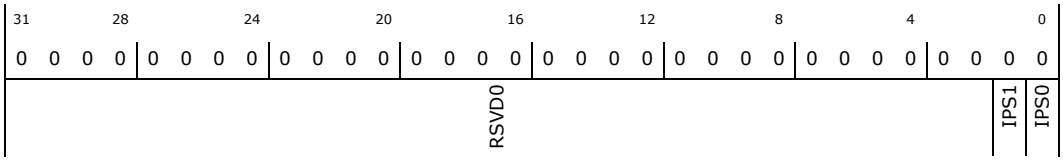
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IS: [ABAR] + 8h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	0h RW/1C	**Interrupt Pending Status Port 1 (IPS1):** If set, indicates that port 1 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s): That has port 1 physically.
0	0h RW/1C	**Interrupt Pending Status Port 0 (IPS0):** If set, indicates that port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. This bit is only applicable to project(s): That has port 0 physically.

13.8.4 Ports Implemented (GHC_PI)—Offset Ch

This register indicates which ports are exposed to the HBA. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. Any available port may not be implemented. There is BIOS programming requirement on the PI register.

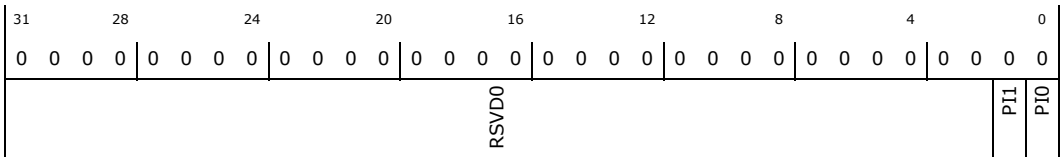
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHC_PI: [ABAR] + Ch

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
1	0h RW/O	**Port 1 Implemented (PI1):** If set, then port 1 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 1 is not available.
0	0h RW/O	**Port 0 Implemented (PI0):** If set, then port 0 is available for use. If cleared, the port is not available for use. This bit is reserved and is read-only 0 if below condition is true else it's RWO-zero: Refer to CAP.NP where port 0 is not available.

13.8.5 AHCI Version (VS)—Offset 10h

This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h.

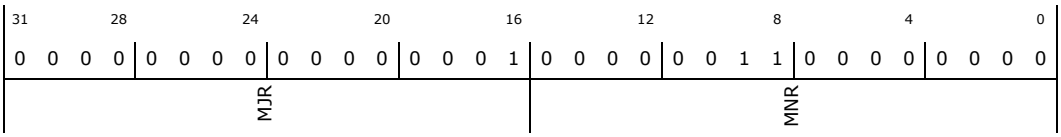
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VS: [ABAR] + 10h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00010300h



Bit Range	Default & Access	Description
31:16	0001h RO	**Major Version Number (MJR):** Indicates the major version is 1
15:0	0300h RO	**Minor Version Number (MNR):** Indicates the minor version is 30

13.8.6 HBA Capabilities Extended (GHC_CAP2)—Offset 24h

This register indicates basic capabilities of the HBA to driver software. The RWO bits in this register are only cleared upon Backbone Reset.

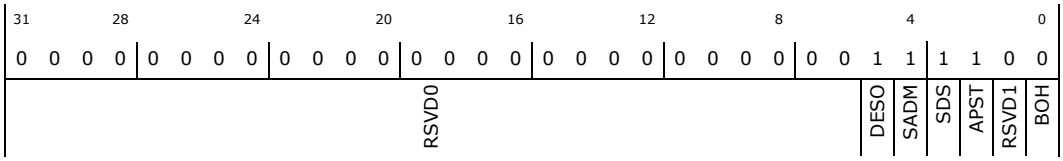
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GHC_CAP2: [ABAR] + 24h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 0000003Ch



Bit Range	Default & Access	Description
31:6	0b RO	**RSVD0:** Reserved
5	1h RW/O	**DEVSLP Entrance from Slumber Only (DESO):** This field specifies that the HBA shall only assert DEVSLP if the interface is in Slumber. When this bit is set to 1, the HBA shall ignore software directed entrance to DEVSLP via PxCMD.ICC unless PxSSTS.IPM = 6h. When this bit is cleared to 0, the HBA may enter DEVSLP from any link state (active, Partial, or Slumber). BIOS is requested to program this field to 1.
4	1h RW/O	**Supports Aggressive DEVSLP Management (SADM):** When set to 1, the HBA supports hardware assertion of the DEVSLP signal after the idle timeout expires. When cleared to 0, this function is not supported and software shall treat the PxDEVSLP.ADSE field as reserved. Note: If PHY IO PM Disable Fuse is 1, this register will read 0. Else this register will read 1 with RWO attribute.
3	1h RW/O	**Supports DEVSLP (SDS):** When set to 1, the HBA supports the DEVSLP feature. When cleared to 0, DEVSLP is not supported. Note: If PHY IO PM Disable Fuse is 1, this register will read 0. Else this register will read 1 with RWO attribute.
2	1h RW/O	**Automatic Partial to Slumber Transitions (APST):** When set to 1, the HBA supports Automatic Partial to Slumber Transitions. When cleared to 0, Automatic Partial to Slumber Transition is not supported. Note: If SATA PHY PM Disable Fuse is 1, this register will read only 0. Else this register will read 1 with RWO attribute.
1	0b RO	**RSVD1:** Reserved
0	0h RO	**BIOS/OS Handoff (BOH):** Not supported.

13.8.7 Vendor Specific (VSP)—Offset A0h

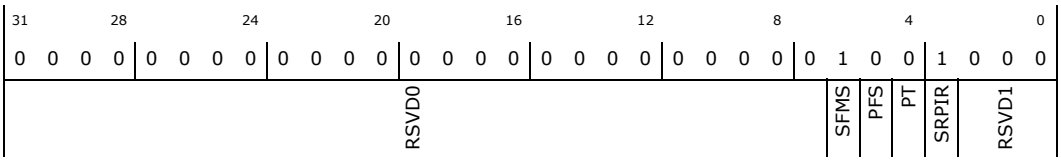
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VSP: [ABAR] + A0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000048h



Bit Range	Default & Access	Description
31:7	0b RO	**RSVD0:** Reserved
6	1h RO	**Software Feature Mask Supported (SFMS):** Set to 1 if the platform is enabled for premium storage features mask (SFM) as described in VS MMIO space at offset ABAR[RPID.(OFST*4)+4].
5	0h RO	**Premium Features Supported (PFS):** Set to 1 if the platform is enabled for premium storage features (PFB) as described in VS MMIO space at offset ABAR[RPID.OFST*4]. Set to 0 if the platform is not enabled for premium storage features.
4	0h RO	**Platform Type (PT):** Set to 1 if mobile platform. Clear (0) if desktop.
3	1h RO	**Supports RAID Platform ID Reporting (SRPIR):** If set to 1, then indicates that the RAID Platform ID is reported via ABAR + C0h. Set to 0 if this ID is not reported via MMIO space.
2:0	0b RO	**RSVD1:** Reserved

13.8.8 Vendor Specific Capabilities (VS_CAP)—Offset A4h

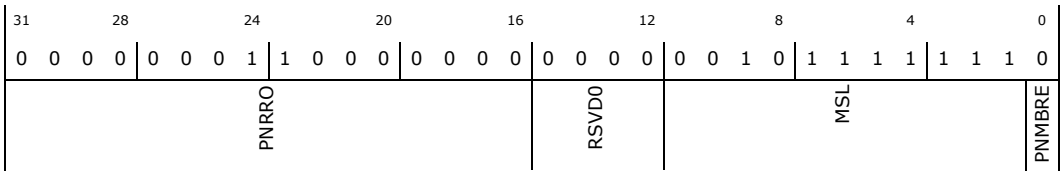
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VS_CAP: [ABAR] + A4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 018002FEh



Bit Range	Default & Access	Description
31:16	0180h RO	**PCIe NAND Remapped Register Offset (PNRRO):** Specifies the DWORD offset within ABAR as to where the PCIe NAND AHCI BAR register space is remapped. Only valid when PNABRE = 1. This places the start of the PCIe NAND AHCI BAR register space at ABAR + 600h
15:12	0b RO	**RSVD0:** Reserved
11:1	17Fh RW	**Memory Space Limit. (MSL):** This field specifies the size of the remapped memory space for the PCIe NAND device. It is a 0-based field. Memory BAR offset from 0 to MSL of the PCIe NAND device are remapped under the integrated AHCI controller memory space. The remapped offset into the AHCI memory space and the value programmed in this field must not exceed the allocated 2k AHCI memory space of the integrated AHCI controller. The reset default of this field is 17Fh (that is, bit[11:1] = 00101111111b) which specifies the size of the remapped memory space as 384 bytes.
0	0h RW/O	**PCIe NAND Memory BAR Remapped Enable (PNMBRE):** Set to 1 if a PCIe NAND device is present and remapping of its memory BAR register space is enabled. Cleared to 0 if there is no PCIe NAND device present or the remapping of its memory BAR register space is disabled.

13.8.9 Premium Feature Block (PFB)—Offset C4h

These registers indicate to the Intel Rapid Storage Technology AHCI driver that those premium RAID features that can be supported on the platform.

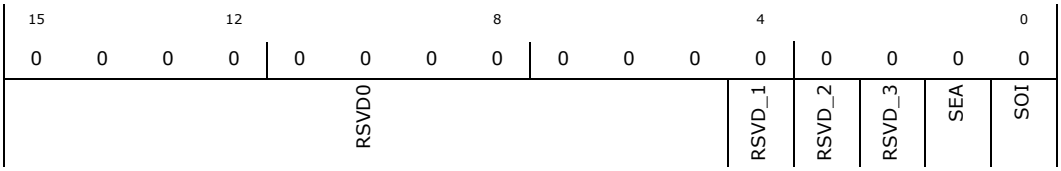
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

PFB: [ABAR] + C4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 0000h



Bit Range	Default & Access	Description
15:5	0b RO	**RSVD0:** Reserved
4	0h RO	**Reserved (RSVD_1):** Read value is the same as VSP.PFS.
3	0h RO	**Reserved (RSVD_2):** Read value is the same as VSP.PFS.
2	0h RO	**Reserved (RSVD_3):** Read value is the same as VSP.PFS.
1	0h RO	**Supports Email Alert (SEA):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.
0	0h RO	**Supports OEM IOCTL (SOI):** Read value is the same as VSP.PFS. If set to 1, then this feature is supported as part of the premium feature set.

13.8.10 SW Feature Mask (SFM)—Offset C8h

The following will be programmed by the BIOS when VS_CAP.SFMS == 1. The feature mask is used by SW to determine which non-premium features shall be supported by SW.

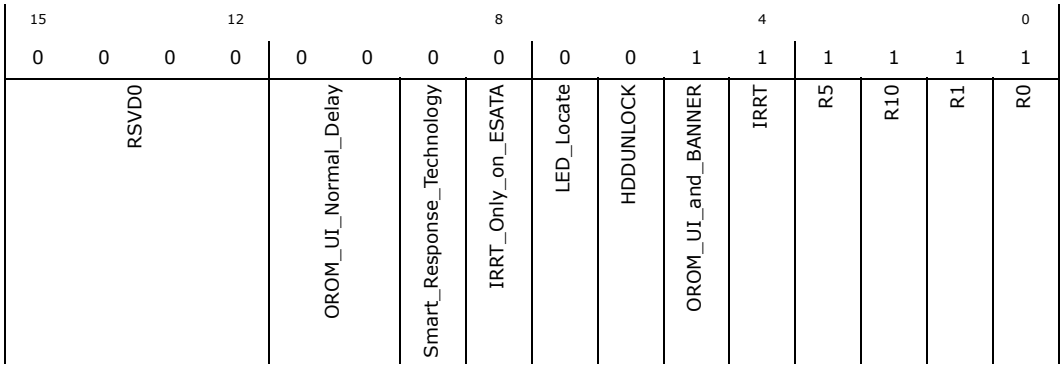
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

SFM: [ABAR] + C8h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 003Fh



Bit Range	Default & Access	Description
15:12	0b RO	**RSVD0:** Reserved
11:10	0h RW/O	**OROM UI Normal Delay. (OROM_UI_Normal_Delay):** Values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 secs (default and previous value); 01 = 4 secs; 10 = 6 secs; 11 = 8 secs. If bit 5 == 0, then these values are disregarded.
9	0h RW/O	**Smart Response Technology. (Smart_Response_Technology):** If set to 1, then Smart Response Technology is enabled. If cleared to 0, the feature is disabled.
8	0h RW/O	**RRT Only on ESATA (IRRT_Only_on_ESATA):** If set to 1, then only RRT volumes can span internal and external SATA ports (e.g. eSATA). If cleared to 0, then any RAID volume can span internal and external SATA ports (e.g. eSATA).
7	0h RW/O	**LED Locate (LED_Locate):** If set to 1, then LED/SGPIO hardware is attached and the ping to locate feature is enabled in the OS.
6	0h RW/O	**HDDUNLOCK:** If set to 1, then HDD password unlock is enabled in the OS.
5	1h RW/O	**OROM UI and BANNER (OROM_UI_and_BANNER):** If set to 1, then the OROM UI is displayed. When cleared to 0, the OROM UI and BANNER are not displayed if all disks and volumes have a normal status.
4	1h RW/O	**RRT (IRRT):** If set to 1, then Rapid Recovery Technology is enabled.
3	1h RW/O	**R5:** If set to 1, then RAID5 is enabled
2	1h RW/O	**R10:** If set to 1, then RAID10 is enabled

Bit Range	Default & Access	Description
1	1h RW/O	**R1:** If set to 1, then RAID1 is enabled
0	1h RW/O	**R0:** If set to 1, then RAID0 is enabled

13.8.11 Port-Command List Base Address (PxCLB0)—Offset 100h

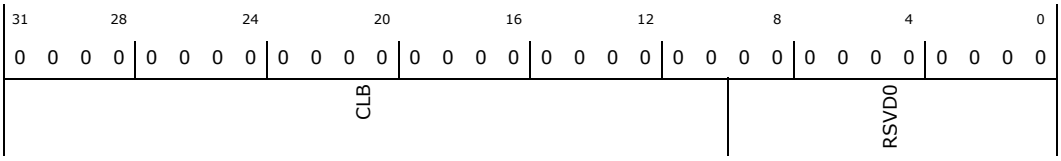
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCLB0: [ABAR] + 100h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	000000h RW	**Command List Base Address (CLB):** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	0b RO	**RSVD0:** Reserved

13.8.12 Port-Command List Base Address Upper 32-bits (PxCLBU0)—Offset 104h

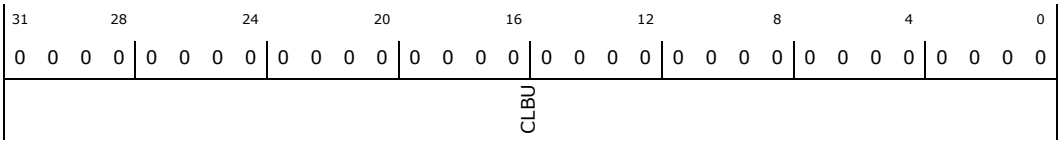
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCLBU0: [ABAR] + 104h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Command List Base Address Upper (CLBU):** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a HBA reset.

13.8.13 Port-FIS Base Address (PxFB0)—Offset 108h

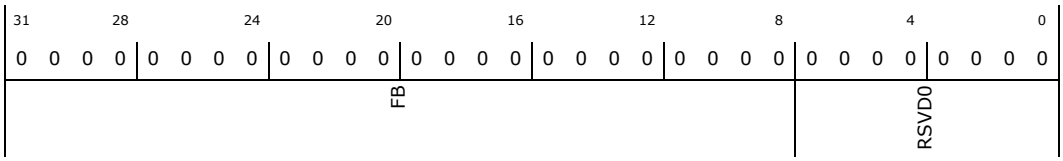
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxFB0: [ABAR] + 108h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0000000h RW	**FIS Base Address (FB):** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. Note that these bits are not reset on a HBA reset.
7:0	0b RO	**RSVD0:** Reserved

13.8.14 Port-FIS Base Address Upper 32-bits (PxFBU0)—Offset 10Ch

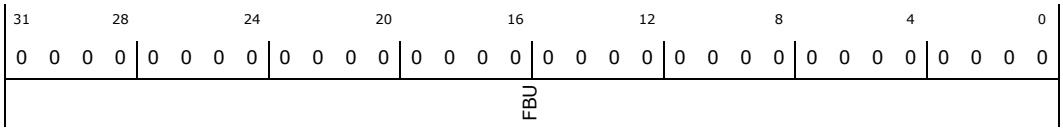
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxFBU0: [ABAR] + 10Ch

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**FIS Base Address Upper (FBU):** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a HBA reset.

13.8.15 Port-Interrupt Status (PxIS0)—Offset 110h

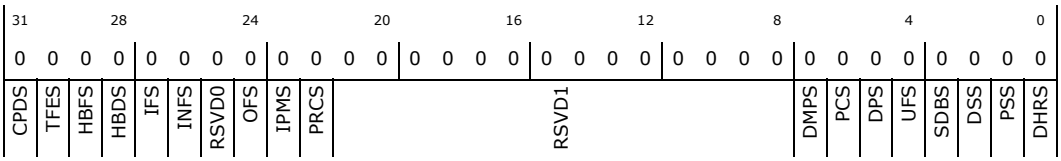
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxIS0: [ABAR] + 110h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RO	**Cold Presence Detect Status (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW/1C	**Task File Error Status (TFES):** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h RW/1C	**Host Bus Fatal Error Status (HBFS):** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master abort.
28	0h RW/1C	**Host Bus Data Error Status (HBDS):** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h RW/1C	**Interface Fatal Error Status (IFS):** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h RW/1C	**Interface Non-fatal Error Status (INFS):** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	0b RO	**RSVD0:** Reserved
24	0h RW/1C	**Overflow Status (OFS):** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h RW/1C	**Incorrect Port Multiplier Status (IPMS):** Not supported
22	0h RO	**PhyRdy Change Status (PRCS):** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared.
21:8	0b RO	**RSVD1:** Reserved
7	0h RW/1C	**Device Mechanical Presence Status (DMPS):** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set).
6	0h RO	**Port Connect Change Status (PCS):** 1=Change in Current Connect Status. 0=No change in Current Connect Status. This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared.
5	0h RW/1C	**Descriptor Processed (DPS):** A PRD with the I. bit set has transferred all of its data.

Bit Range	Default & Access	Description
4	0h RO	**Unknown FIS Interrupt (UFS):** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h RW/1C	**Set Device Bits Interrupt (SDBS):** A Set Device Bits FIS has been received with the I. bit set and has been copied into system memory.
2	0h RW/1C	**DMA Setup FIS Interrupt (DSS):** A DMA Setup FIS has been received with the I. bit set and has been copied into system memory.
1	0h RW/1C	**PIO Setup FIS Interrupt (PSS):** A PIO Setup FIS has been received with the I. bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	0h RW/1C	**Device to Host Register FIS Interrupt (DHRS):** A D2H register FIS has been received with the I. bit set, and has been copied into system memory.

13.8.16 Port-Interrupt Enable (PxIE0)—Offset 114h

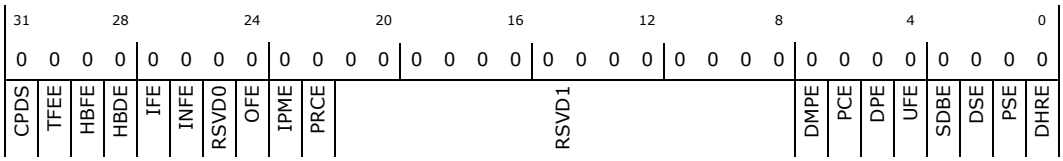
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

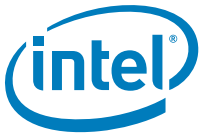
PxIE0: [ABAR] + 114h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RO	**Cold Presence Detect Enable (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW	**Task File Error Enable (TFEE):** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.
29	0h RW	**Host Bus Fatal Error Enable (HBFE):** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h RW	**Host Bus Data Error Enable (HBDE):** When set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h RW	**Interface Fatal Error Enable (IFE):** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h RW	**Interface Non-fatal Error Enable (INFE):** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	0b RO	**RSVD0:** Reserved
24	0h RW	**Overflow Enable (OFE):** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interrupt.



Bit Range	Default & Access	Description
23	0h RW	**Incorrect Port Multiplier Enable (IPME):** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interrupt.
22	0h RW	**PhyRdy Change Interrupt Enable (PRCE):** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.
21:8	0b RO	**RSVD1:** Reserved
7	0h RW	**Device Mechanical Enable (DMPE):** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.
6	0h RW	**Port Change Interrupt Enable (PCE):** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h RW	**Descriptor Processed Interrupt Enable (DPE):** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h RW	**Unknown FIS Interrupt Enable (UFE):** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h RW	**Set Device Bits FIS Interrupt Enable (SDBE):** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.
2	0h RW	**DMA Setup FIS Interrupt Enable (DSE):** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.
1	0h RW	**PIO Setup FIS Interrupt Enable (PSE):** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h RW	**Device to Host Register FIS Interrupt Enable (DHRE):** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

13.8.17 Port-Command (PxCMD0)—Offset 118h

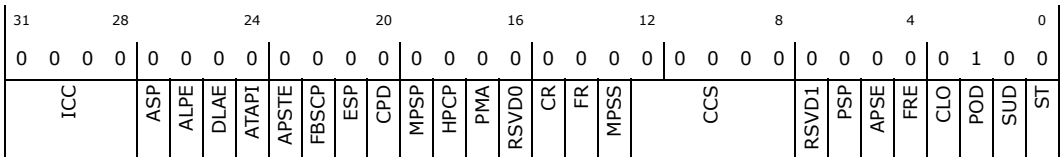
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

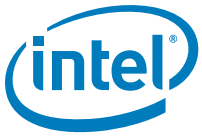
PxCMD0: [ABAR] + 118h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000004h



Bit Range	Default & Access	Description
31:28	0h RW	**Interface Communication Control (ICC):** This is a four bit field which can be used to control reset and power states of the interface. If the Link layer is currently in the L_IDLE state, writes to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writes to this field shall have no effect. Fh -9h Reserved. 8h DEVSLP: This shall cause the HBA to assert the DEVSLP signal associated with the port; the HBA shall ignore the DEVSLP Idle Timeout value specified by PxDEVSLP.DITO. Software shall only request DEVSLP when the interface is in an idle state (that is, PxCI is cleared to 0h and PxSACT is cleared to 0h); if the interface is not idle at the time the register is written, then the HBA takes no action and the interface remains in its current state. If PxCAP2.DESO is set to '1' and PxSSTS.IPM is not set to '6h', then the HBA takes no action and the interface remains in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion). 7h Reserved 6h Slumber: This shall cause the HBA to request a transition of the interface to the Slumber state. The SATA device may reject the request and the interface shall remain in its current state. 5h-3h Reserved. 2h Partial: This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state. 1h Active: This shall cause the HBA to request a transition of the interface into the active state. If the requested transition is from the DEVSLP state, then the HBA shall wait until PxDEVSLP.DMAT has expired before de-asserting the DEVSLP signal. 0h No-Op / Idle: When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not yet have occurred. When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (that is, interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and the software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state (with the exception of DEVSLP). The transition to DEVSLP may occur from any other state if CAP2.DESO is cleared to '0'. If CAP2.DESO is set to '1', then DEVSLP may only be transitioned to if the link is in Slumber.
27	0h RW	**Aggressive Slumber Partial (ASP):** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter Partial state when it clears a bit in the PxCI or PxSACT register and the register values are both 0h. If CAP.SALP is cleard to 0, software shall treat this bit as reserved.
26	0h RW	**Aggressive Link Power Management Enable (ALPE):** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit.
25	0h RW	**Drive LED on ATAPI Enable (DLAE):** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0. This bit is set by software



Bit Range	Default & Access	Description
24	0h RW	**Device is ATAPI (ATAPI):** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	0h RW	**Automatic Partial to Slumber Transitions Enabled (APSTE):** When set to 1, the HBA may perform Automatic Partial to Slumber Transitions. When cleared to 0 - the port shall not perform Automatic Partial to Slumber Transitions. Software shall only set this bit to 1 - if CAP2.APST is set to 1; if CAP2.APST is cleared to 0 - software shall treat this bit as reserved.
22	0h RO	**FIS-based Switching Capable Port (FBSCP):** The SATA controller does not support FIS-Based Switching.
21	0h RW/O	**External SATA Port (ESP):** When set to 1, indicates that this port is routed externally and will be used with an external SATA device. When set to 1, CAP.SXS must also be set to 1. When cleared (0), indicates that this port is not routed externally and supports internal SATA devices only. If ESP is set to 1, then the port may experience hot plug events.
20	0h RO	**Cold Presence Detection (CPD):** The SATA controller does not support cold presence detect.
19	0h RW/O	**Mechanical Presence Switch Attached to Port (MPSP):** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port.
18	0h RW/O	**Hot Plug Capable Port (HPCP):** This indicates whether this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user.
17	0h RO	**Port Multiplier Attached (PMA):** Not supported
16	0b RO	**RSVD0:** Reserved
15	0h RO	**Command List Running (CR):** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h RO	**FIS Receive Running (FR):** When this bit is set it indicates that the FIS Receive DMA engine for the port is running.
13	0h RO	**Mechanical Presence Switch State (MPSS):** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.
12:8	00h RO	**Current Command Slot (CCS):** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.
7	0b RO	**RSVD1:** Reserved
6	0h RO	**PHYSLP Present (PSP):** If set to 1, the platform supports PHYSLP on this port. If cleared to 0, the platform does not support PHYSLP on this port. This bit may only be set to 1 if CAP2.SPS is set to 1.

Bit Range	Default & Access	Description
5	0h RW	**Aggressive PHYSLP Enable (APSE):** This bit is read/write for HBAs that support aggressive PHYSLP management (CAP2.SAPM == 1). This bit is read-only for HBAs that do not support aggressive PHYSLP management (CAP2.SPS == 0). When this bit is set to 1, the HBA shall assert the PHYSLP signal after the port has been idle (PxCI == 0h and PxSACT == 0h) for the amount of time specified by the GHC.PITO register. When this bit is cleared to 0, the HBA does not enter PHYSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxCMD.PSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the PHYSLP signal if asserted.
4	0h RW	**FIS Receive Enable (FRE):** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence.
3	0h RW/1S	**Command List Override (CLO):** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.
2	1h RO	**Power On Device (POD):** The SATA controller does not support cold presence detect.
1	0h RW	**Spin-Up Device (SUD):** This bit is read/write for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1 for HBAs that do not support staggered spin-up. On an edge detect from 0 to 1, the HBA shall start a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET = 0h, the HBA will enter listen mode.
0	0h RW	**Start (ST):** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also.

13.8.18 Port-Task File Data (PxTFD0)—Offset 120h

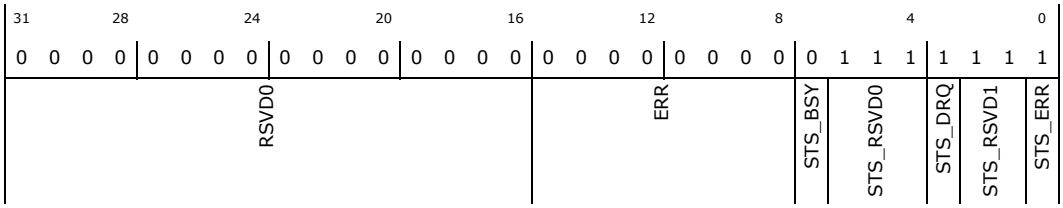
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxTFD0: [ABAR] + 120h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RO	**Error (ERR):** Contains the latest copy of the task file error register.

Bit Range	Default & Access	Description
7	0h RO	**Status Busy (STS_BSY):** Status - Indicates the interface is busy.
6:4	7h RO	**Status Rsvd0 (STS_RSVD0):** Status - Not Applicable.
3	1h RO	**Status Drq (STS_DRQ):** Status - Indicates a data transfer is requested.
2:1	3h RO	**Status Rsvd1 (STS_RSVD1):** Status - Not Applicable.
0	1h RO	**Status Err (STS_ERR):** Status - Indicates an error during the transfer.

13.8.19 Port-Signature (PxSIG0)—Offset 124h

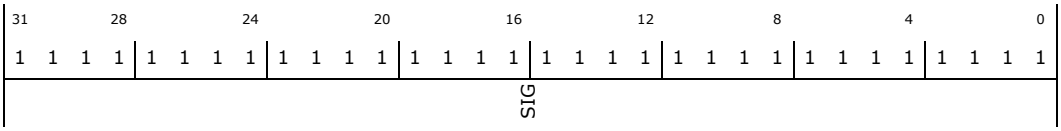
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSIG0: [ABAR] + 124h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RO	**Signature (SIG):** Contains the signature received from a device on the first D2H Register FIS.

13.8.20 Port-Serial ATA Status (PxSSTS0)—Offset 128h

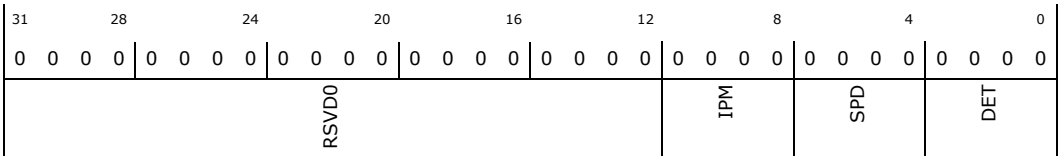
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSSTS0: [ABAR] + 128h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
11:8	0h RO	**Interface Power Management (IPM):** Indicates the current interface state 0h = Device not present or communication not established. 1h = Interface in active state. 2h = Interface in PARTIAL power management state. 6h = Interface in SLUMBER power management state. 8h = PHYSLP asserted. All other values reserved. This field reflects the interface power management state for both device and host initiated power management. Note: If an automatic partial to slumber transition occurs, PxSSTS.IPM shall reflect that the host has entered slumber (PxSSTS.IPM = 6h.)
7:4	0h RO	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed. 0h = Device not present or communication not established. 1h = Generation 1 communication rate negotiated. 2h = Generation 2 communication rate negotiated. 3h = Generation 3 communication rate negotiated. All other values reserved
3:0	0h RO	**Device Detection (DET):** Indicates the interface device detection and Phy state. 0h = No device detected and Phy communication not established. 1h = Device presence detected but Phy communication not established. 3h = Device presence detected and Phy communication established. 4h = Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved. Note that, while the true reset default value of this register is 0h, the value read from this register depends on drive presence and the point in time within the initialization process when the register is read. Note: The means by which the implementation determines device presence may be vendor specific. However, device presence shall always be indicated anytime a COMINIT signal is received.

13.8.21 Port-Serial ATA Control (PxSCTL0)—Offset 12Ch

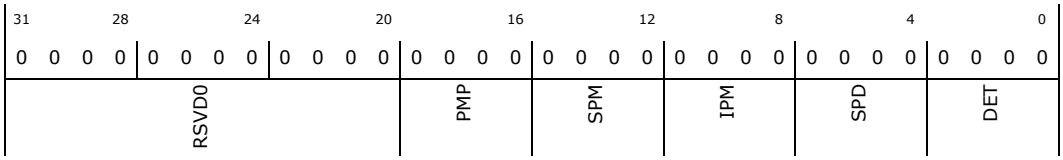
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSCTL0: [ABAR] + 12Ch

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19:16	0h RW	**Port Multiplier Port (PMP):** This field is not used by AHCI.
15:12	0h RW	**Select Power Management (SPM):** This field is not used by AHCI.
11:8	0h RW	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKP any request from the device to enter that state. 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3hTransitions to both PARTIAL and SLUMBER states disabled 4h Transitions to the DEVSLP power management state are disabled 5h Transitions to the Partial and DEVSLP power management states are disabled 6h Transitions to the Slumber and DEVSLP power management states are disabled 7h Transitions to the Partial, Slumber and DEVSLP power management states are disabled All other values reserved

Bit Range	Default & Access	Description
7:4	0h RW	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface. 0h No speed negotiation restrictions. 1h Limit speed negotiation to Generation 1 communication rate. 2h Limit speed negotiation to a rate not greater than Generation 2 communication rate. 3h Limit speed negotiation to a rate not greater than Generation 3 communication rate. All other values reserved. Note: If software changes SPD after port has been enabled, software is required to perform a port reset via DET=1h.
3:0	0h RW	**Device Detection Initialization (DET):** Controls HBA's device detection and interface initialization. 0h No device detection or initialization action requested. 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is continuously transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h Disable the Serial ATA interface and put Phy in offline mode. All other values reserved. This field may only be changed when PxCMD.ST is '0'. Changing this field while the HBA is running results in undefined behavior. When PxCMD.ST is set to '1', this field should have a value of 0h. It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when PxSCTL.DET = 1h

13.8.22 Port-Serial ATA Error (PxSERR0)—Offset 130h

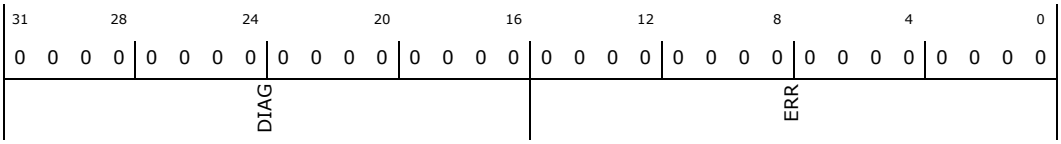
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSERR0: [ABAR] + 130h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/1C	**Diagnostics (DIAG):** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bit Field 31:27 Reserved 26 Exchanged (X): When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. The means by which the implementation determines that the device presence has changed is vendor specific. This bit shall always be set to one anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit. 25 Unrecognized FIS Type (F): Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized. 24 Transport state transition error (T): Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. 23 Link Sequence Error (S): Indicates that one or more Link state machine error conditions were encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. 22 Handshake Error (H): Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 CRC Error (C): Indicates that one or more CRC errors occurred with the Link Layer. 20 Disparity Error (D): This field is not used by AHCI. 19 10B to 8B Decode Error (B): Indicates that one or more 10B to 8B decoding errors occurred. 18 Comm Wake (W): Indicates that a Comm Wake signal was detected by the Phy. 17 Phy Internal Error (I): Indicates that the Phy detected some internal error. 16 PhyRdy Change (N): When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. The state of this bit is reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled.

Bit Range	Default & Access	Description
15:0	0000h RW/1C	**Error (ERR):** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer. 15:12 Reserved 11 Internal Error (E): The SATA controller failed due to a master or target abort when attempting to access system memory. 10 Protocol Error (P): A violation of the Serial ATA protocol was detected. 9 Persistent Communication or Data Integrity Error (C): A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 Transient Data Integrity Error (T): A data integrity error occurred that was not recovered by the interface. 7:2 Reserved 1 Recovered Communications Error (M): Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers. 0 Recovered Data Integrity Error (I): A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

13.8.23 Port-Serial ATA Active (PxSACT0)—Offset 134h

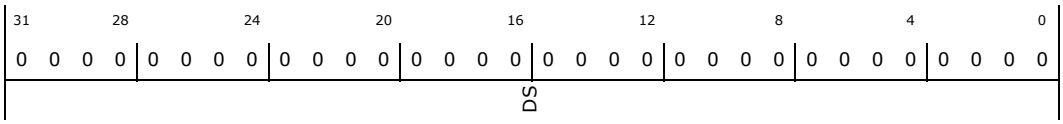
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSACT0: [ABAR] + 134h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW/1S	**Device Status (DS):** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS.

13.8.24 Port-Commands Issued (PxCI0)—Offset 138h

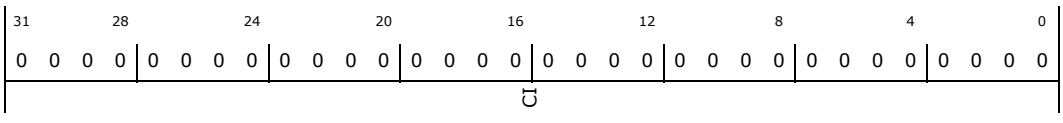
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCI0: [ABAR] + 138h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when PxCMD.ST is set to 1.

13.8.25 Port-Device Sleep (PxDEVSLP0)—Offset 144h

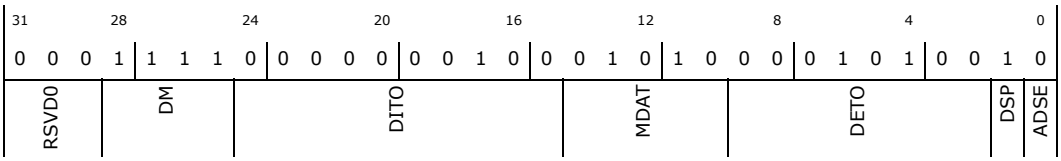
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxDEVSLP0: [ABAR] + 144h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 1E022852h



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:25	Fh RW/O	**DITO Multiplier (DM):** 0's based value that specifies the DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (that is, DITO actual = DITO * DM).
24:15	004h RW	**DEVSLP Idle Timeout (DITO):** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal.
14:10	0Ah RW	**DEVSLP Minimum Assertion Time (MDAT):** This field specifies the minimum amount of time (in 1ms granularity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The nominal value is 10ms and the minimum is 1ms depending on device identification information.
9:2	14h RW	**DEVSLP Exit Timeout (DETO):** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The nominal value is 20ms while the max value is 255ms depending on device identification information.
1	1h RW/O	**DEVSLP Present (DSP):** If set to 1, the platform supports DEVSLP on this port. If cleared to 0, the platform does not support DEVSLP on this port.
0	0h RW	**Aggressive DEVSLP Enable (ADSE):** When this bit is cleared to 0, the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxDEVSLP.DSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the DEVSLP signal if asserted.

13.8.26 Port-Command List Base Address (PxCLB1)—Offset 180h

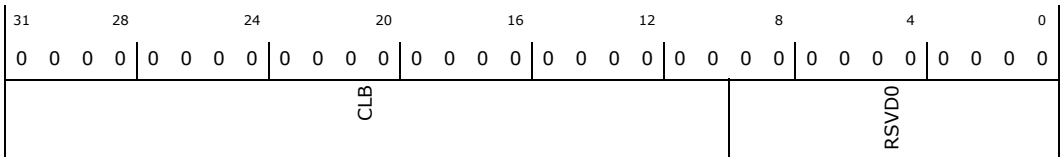
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCLB1: [ABAR] + 180h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	000000h RW	**Command List Base Address (CLB):** Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. This address must be 1K aligned as indicated by bits 31:10 being read/write. Note that these bits are not reset on a HBA reset.
9:0	0b RO	**RSVD0:** Reserved

13.8.27 Port-Command List Base Address Upper 32-bits (PxCLBU1)—Offset 184h

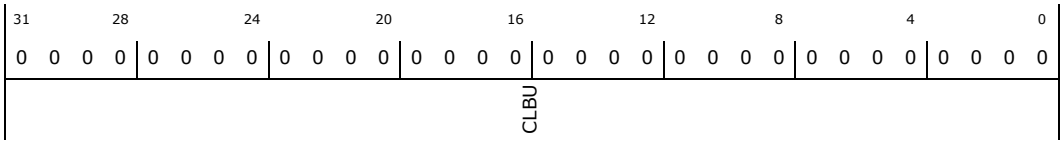
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCLBU1: [ABAR] + 184h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Command List Base Address Upper (CLBU):** Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. Note that these bits are not reset on a HBA reset.

13.8.28 Port-FIS Base Address (PxFB1)—Offset 188h

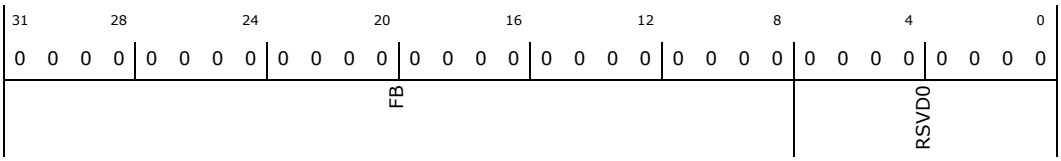
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxFB1: [ABAR] + 188h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0000000h RW	**FIS Base Address (FB):** Indicates the 32-bit base for received FISes. This address must be 256-byte aligned as indicated by bits 31:08 being read/write. When FIS-based switching is in use, this structure is 4KB in length and the address shall be 4KB aligned. Note that these bits are not reset on a HBA reset.
7:0	0b RO	**RSVD0:** Reserved

13.8.29 Port-FIS Base Address Upper 32-bits (PxFBU1)—Offset 18Ch

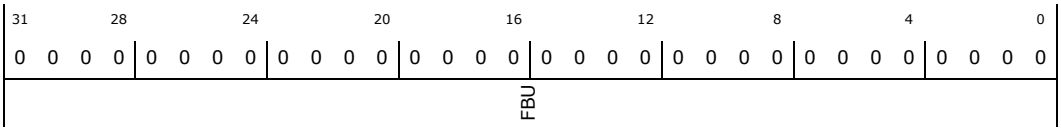
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxFBU1: [ABAR] + 18Ch

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**FIS Base Address Upper (FBU):** Indicates the upper 32-bits for the received FIS base for this port. Note that these bits are not reset on a HBA reset.

13.8.30 Port-Interrupt Status (PxIS1)—Offset 190h

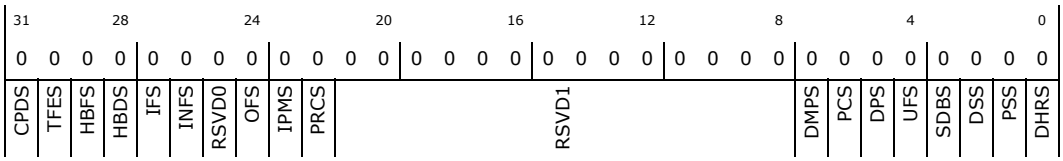
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxIS1: [ABAR] + 190h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RO	**Cold Presence Detect Status (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW/1C	**Task File Error Status (TFES):** This bit is set whenever the status register is updated by the device and the error bit (bit 0 of the Status field in the received FIS) is set.
29	0h RW/1C	**Host Bus Fatal Error Status (HBFS):** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master abort.
28	0h RW/1C	**Host Bus Data Error Status (HBDS):** Indicates that the HBA encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	0h RW/1C	**Interface Fatal Error Status (IFS):** Indicates that the HBA encountered an error on the SATA interface which caused the transfer to stop.
26	0h RW/1C	**Interface Non-fatal Error Status (INFS):** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.
25	0b RO	**RSVD0:** Reserved
24	0h RW/1C	**Overflow Status (OFS):** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.
23	0h RW/1C	**Incorrect Port Multiplier Status (IPMS):** Not supported
22	0h RO	**PhyRdy Change Status (PRCS):** When set to one indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. This bit is RO and is only cleared when PxSERR.DIAG.N is cleared.
21:8	0b RO	**RSVD1:** Reserved
7	0h RW/1C	**Device Mechanical Presence Status (DMPS):** When set, indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support mechanical presence switch (CAP.SMPS and PxCMD.MPSP are set).
6	0h RO	**Port Connect Change Status (PCS):** 1=Change in Current Connect Status. 0=No change in Current Connect Status. This bit reflects the state of PxSERR.DIAG.X. This bit is only cleared when PxSERR.DIAG.X is cleared.
5	0h RW/1C	**Descriptor Processed (DPS):** A PRD with the I. bit set has transferred all of its data.

Bit Range	Default & Access	Description
4	0h RO	**Unknown FIS Interrupt (UFS):** When set to 1 indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. Note that this bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	0h RW/1C	**Set Device Bits Interrupt (SDBS):** A Set Device Bits FIS has been received with the I. bit set and has been copied into system memory.
2	0h RW/1C	**DMA Setup FIS Interrupt (DSS):** A DMA Setup FIS has been received with the I. bit set and has been copied into system memory.
1	0h RW/1C	**PIO Setup FIS Interrupt (PSS):** A PIO Setup FIS has been received with the I. bit set, it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	0h RW/1C	**Device to Host Register FIS Interrupt (DHRS):** A D2H register FIS has been received with the I. bit set, and has been copied into system memory.

13.8.31 Port-Interrupt Enable (PxIE1)—Offset 194h

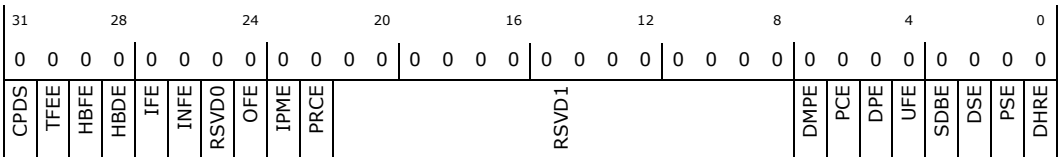
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxIE1: [ABAR] + 194h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RO	**Cold Presence Detect Enable (CPDS):** The SATA controller does not support cold presence detect.
30	0h RW	**Task File Error Enable (TFEE):** When set, GHC.IE is set, and P0S.TFES is set, the HBA shall generate an interrupt.
29	0h RW	**Host Bus Fatal Error Enable (HBFE):** When set, GHC.IE is set, and P0IS.HBFS is set, the HBA shall generate an interrupt.
28	0h RW	**Host Bus Data Error Enable (HBDE):** When set, GHC.IE is set, and P0IS.HBDS is set, the HBA shall generate an interrupt.
27	0h RW	**Interface Fatal Error Enable (IFE):** When set, GHC.IE is set, and P0IS.IFS is set, the HBA shall generate an interrupt.
26	0h RW	**Interface Non-fatal Error Enable (INFE):** When set, GHC.IE is set, and P0IS.INFS is set, the HBA shall generate an interrupt.
25	0b RO	**RSVD0:** Reserved
24	0h RW	**Overflow Enable (OFE):** When set, and GHC.IE and P0IS.OFS are set, the HBA shall generate an interrupt.

Bit Range	Default & Access	Description
23	0h RW	**Incorrect Port Multiplier Enable (IPME):** When set, and GHC.IE and P0IS.IPMS are set, the HBA shall generate an interrupt.
22	0h RW	**PhyRdy Change Interrupt Enable (PRCE):** When set, and GHC.IE is set, and PxIS.PRCS is set, the HBA shall generate an interrupt.
21:8	0b RO	**RSVD1:** Reserved
7	0h RW	**Device Mechanical Enable (DMPE):** When set, and P0IS.DMPS is set, the HBA shall generate an interrupt.
6	0h RW	**Port Change Interrupt Enable (PCE):** When set, GHC.IE is set, and P0IS.PCS is set, the HBA shall generate an interrupt.
5	0h RW	**Descriptor Processed Interrupt Enable (DPE):** When set, GHC.IE is set, and P0IS.DPS is set, the HBA shall generate an interrupt.
4	0h RW	**Unknown FIS Interrupt Enable (UFE):** When set, GHC.IE is set, and PxIS.UFS is set to 1, the HBA shall generate an interrupt.
3	0h RW	**Set Device Bits FIS Interrupt Enable (SDBE):** When set, GHC.IE is set, and P0IS.SDBS is set, the HBA shall generate an interrupt.
2	0h RW	**DMA Setup FIS Interrupt Enable (DSE):** When set, GHC.IE is set, and P0IS.DSS is set, the HBA shall generate an interrupt.
1	0h RW	**PIO Setup FIS Interrupt Enable (PSE):** When set, GHC.IE is set, and P0IS.PSS is set, the HBA shall generate an interrupt.
0	0h RW	**Device to Host Register FIS Interrupt Enable (DHRE):** When set, GHC.IE is set, and P0IS.DHRS is set, the HBA shall generate an interrupt.

13.8.32 Port-Command (PxCMD1)—Offset 198h

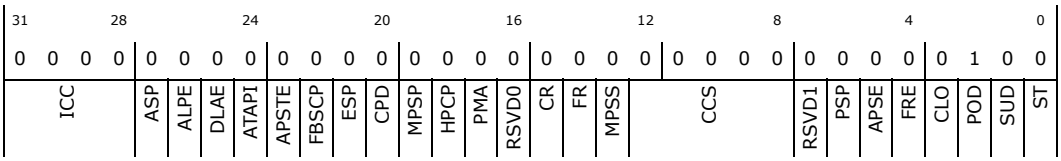
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCMD1: [ABAR] + 198h

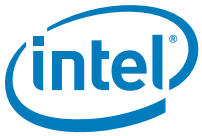
ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000004h



Bit Range	Default & Access	Description
31:28	0h RW	**Interface Communication Control (ICC):** This is a four bit field which can be used to control reset and power states of the interface. If the Link layer is currently in the L_IDLE state, writes to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writes to this field shall have no effect. Fh -9h Reserved. 8h DEVSLP: This shall cause the HBA to assert the DEVSLP signal associated with the port; the HBA shall ignore the DEVSLP Idle Timeout value specified by PxDEVSLP.DITO. Software shall only request DEVSLP when the interface is in an idle state (that is, PxCI is cleared to 0h and PxSACT is cleared to 0h); if the interface is not idle at the time the register is written, then the HBA takes no action and the interface remains in its current state. If PxCAP2.DESO is set to '1' and PxSSTS.IPM is not set to '6h', then the HBA takes no action and the interface remains in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion). 7h Reserved 6h Slumber: This shall cause the HBA to request a transition of the interface to the Slumber state. The SATA device may reject the request and the interface shall remain in its current state. 5h-3h Reserved. 2h Partial: This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state. 1h Active: This shall cause the HBA to request a transition of the interface into the active state. If the requested transition is from the DEVSLP state, then the HBA shall wait until PxDEVSLP.DMAT has expired before de-asserting the DEVSLP signal. 0h No-Op / Idle: When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not yet have occurred. When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (that is, interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and the software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state (with the exception of DEVSLP). The transition to DEVSLP may occur from any other state if CAP2.DESO is cleared to '0'. If CAP2.DESO is set to '1', then DEVSLP may only be transitioned to if the link is in Slumber.
27	0h RW	**Aggressive Slumber Partial (ASP):** When set to 1, and the ALPE bit is set, the HBA shall aggressively enter Slumber state when it clears a bit in the PxCI or PxSACT register and the register values are 0h. When cleared, and the ALPE bit is set, the HBA will aggressively enter Partial state when it clears a bit in the PxCI or PxSACT register and the register values are both 0h. If CAP.SALP is cleard to 0, software shall treat this bit as reserved.
26	0h RW	**Aggressive Link Power Management Enable (ALPE):** When set, the HBA will aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit.
25	0h RW	**Drive LED on ATAPI Enable (DLAE):** When set, the HBA will drive the LED pin active for commands regardless of the state of PxCMD.ATAPI. When cleared, the HBA will only drive the LED pin active for commands if PxCMD.ATAPI is set to 0. This bit is set by software

Bit Range	Default & Access	Description
24	0h RW	**Device is ATAPI (ATAPI):** When set, the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	0h RW	**Automatic Partial to Slumber Transitions Enabled (APSTE):** When set to 1, the HBA may perform Automatic Partial to Slumber Transitions. When cleared to 0 - the port shall not perform Automatic Partial to Slumber Transitions. Software shall only set this bit to 1 - if CAP2.APST is set to 1; if CAP2.APST is cleared to 0 - software shall treat this bit as reserved.
22	0h RO	**FIS-based Switching Capable Port (FBSCP):** The SATA controller does not support FIS-Based Switching.
21	0h RW/O	**External SATA Port (ESP):** When set to 1, indicates that this port is routed externally and will be used with an external SATA device. When set to 1, CAP.SXS must also be set to 1. When cleared (0), indicates that this port is not routed externally and supports internal SATA devices only. If ESP is set to 1, then the port may experience hot plug events.
20	0h RO	**Cold Presence Detection (CPD):** The SATA controller does not support cold presence detect.
19	0h RW/O	**Mechanical Presence Switch Attached to Port (MPSP):** If set to 1, the platform supports a mechanical presence switch attached to this port. If cleared to 0, the platform does not support a mechanical presence switch attached to this port.
18	0h RW/O	**Hot Plug Capable Port (HPCP):** This indicates whether this port is connected to a device which can be hot plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as eject device to the end-user.
17	0h RO	**Port Multiplier Attached (PMA):** Not supported
16	0b RO	**RSVD0:** Reserved
15	0h RO	**Command List Running (CR):** When this bit is set it indicates that the command list DMA engine for the port is running.
14	0h RO	**FIS Receive Running (FR):** When this bit is set it indicates that the FIS Receive DMA engine for the port is running.
13	0h RO	**Mechanical Presence Switch State (MPSS):** The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open then this bit is set to 1. If CAP.SMPS is set to 0 then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.
12:8	00h RO	**Current Command Slot (CCS):** Indicates the current command slot the HBA is processing. This field is valid when the PxCMD.ST bit is set, and is constantly updated by the HBA. This field can be updated as soon as the HBA recognizes an active command slot, or at some point soon after when it begins processing the command. When PxCMD.ST transitions from a 1 to a 0, the HBA will reset this field to 0. After PxCMD.ST transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is PxCMD.CCS + 1. For example, after the HBA has issued its first command, if PxCMD.CCS = 0h and PxCI is set to 3h, the next command that will be issued is from command slot 1.
7	0b RO	**RSVD1:** Reserved
6	0h RO	**PHYSLP Present (PSP):** If set to 1, the platform supports PHYSLP on this port. If cleared to 0, the platform does not support PHYSLP on this port. This bit may only be set to 1 if CAP2.SPS is set to 1.



Bit Range	Default & Access	Description
5	0h RW	**Aggressive PHYSLP Enable (APSE):** This bit is read/write for HBAs that support aggressive PHYSLP management (CAP2.SAPM == 1). This bit is read-only for HBAs that do not support aggressive PHYSLP management (CAP2.SPS == 0). When this bit is set to 1, the HBA shall assert the PHYSLP signal after the port has been idle (PxCI == 0h and PxSACT == 0h) for the amount of time specified by the GHC.PITO register. When this bit is cleared to 0, the HBA does not enter PHYSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxCMD.PSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the PHYSLP signal if asserted.
4	0h RW	**FIS Receive Enable (FRE):** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB and PxFBU. When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence.
3	0h RW/1S	**Command List Override (CLO):** Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.
2	1h RO	**Power On Device (POD):** The SATA controller does not support cold presence detect.
1	0h RW	**Spin-Up Device (SUD):** This bit is read/write for HBAs that support staggered spin-up via CAP.SSS. This bit is read only 1 for HBAs that do not support staggered spin-up. On an edge detect from 0 to 1, the HBA shall start a COMRESET initialization sequence to the device. Clearing this bit causes no action on the interface. Clearing this bit to0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET = 0h, the HBA will enter listen mode.
0	0h RW	**Start (ST):** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a 0 to a 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI and PxSACT register is cleared by the HBA upon the HBA putting the controller into an idle state. PxTFD shall be updated also.

13.8.33 Port-Task File Data (PxTFD1)—Offset 1A0h

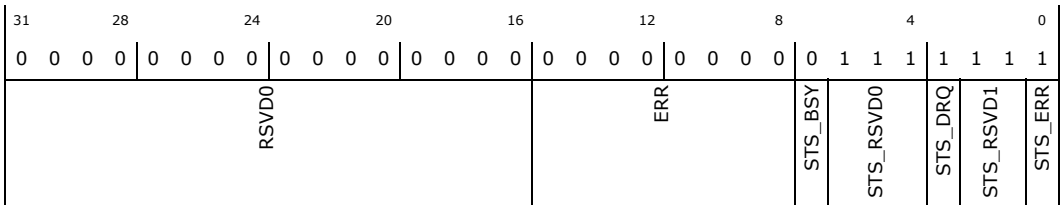
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxTFD1: [ABAR] + 1A0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 0000007Fh



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RO	**Error (ERR):** Contains the latest copy of the task file error register.
7	0h RO	**Status Busy (STS_BSY):** Status - Indicates the interface is busy.
6:4	7h RO	**Status Rsvd0 (STS_RSVD0):** Status - Not Applicable.
3	1h RO	**Status Drq (STS_DRQ):** Status - Indicates a data transfer is requested.
2:1	3h RO	**Status Rsvd1 (STS_RSVD1):** Status - Not Applicable.
0	1h RO	**Status Err (STS_ERR):** Status - Indicates an error during the transfer.

13.8.34 Port-Signature (PxSIG1)—Offset 1A4h

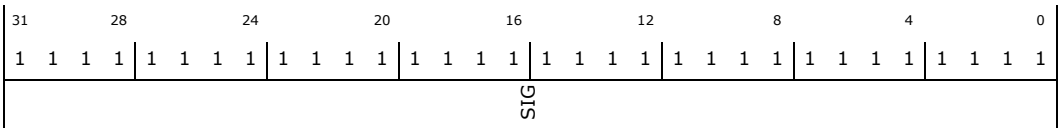
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSIG1: [ABAR] + 1A4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RO	**Signature (SIG):** Contains the signature received from a device on the first D2H Register FIS.

13.8.35 Port-Serial ATA Status (PxSSTS1)—Offset 1A8h

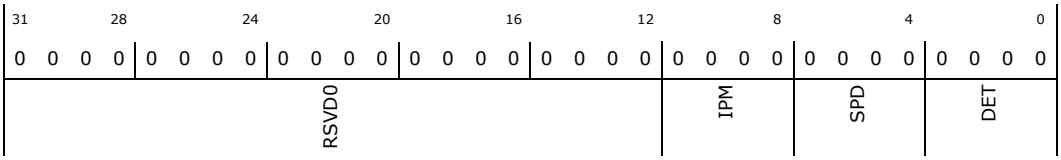
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSSTS1: [ABAR] + 1A8h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11:8	0h RO	**Interface Power Management (IPM):** Indicates the current interface state 0h = Device not present or communication not established. 1h = Interface in active state. 2h = Interface in PARTIAL power management state. 6h = Interface in SLUMBER power management state. 8h = PHYSLP asserted. All other values reserved. This field reflects the interface power management state for both device and host initiated power management. Note: If an automatic partial to slumber transition occurs, PxSSTS.IPM shall reflect that the host has entered slumber (PxSSTS.IPM = 6h.)
7:4	0h RO	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed. 0h = Device not present or communication not established. 1h = Generation 1 communication rate negotiated. 2h = Generation 2 communication rate negotiated. 3h = Generation 3 communication rate negotiated. All other values reserved

Bit Range	Default & Access	Description
3:0	0h RO	**Device Detection (DET):** Indicates the interface device detection and Phy state. 0h = No device detected and Phy communication not established. 1h = Device presence detected but Phy communication not established. 3h = Device presence detected and Phy communication established. 4h = Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode. All other values reserved. Note that, while the true reset default value of this register is 0h, the value read from this register depends on drive presence and the point in time within the initialization process when the register is read. Note: The means by which the implementation determines device presence may be vendor specific. However, device presence shall always be indicated anytime a COMINIT signal is received.

13.8.36 Port-Serial ATA Control (PxSCTL1)—Offset 1ACh

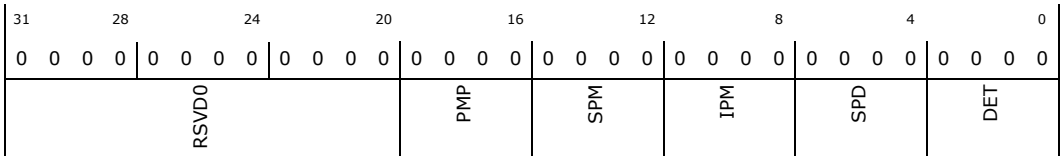
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSCTL1: [ABAR] + 1ACh

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	0b RO	**RSVD0:** Reserved
19:16	0h RW	**Port Multiplier Port (PMP):** This field is not used by AHCI.
15:12	0h RW	**Select Power Management (SPM):** This field is not used by AHCI.
11:8	0h RW	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is not allowed via this register field, the HBA will not initiate that state and the HBA will PMNAKP any request from the device to enter that state. 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3hTransitions to both PARTIAL and SLUMBER states disabled 4h Transitions to the DEVSLP power management state are disabled 5h Transitions to the Partial and DEVSLP power management states are disabled 6h Transitions to the Slumber and DEVSLP power management states are disabled 7h Transitions to the Partial, Slumber and DEVSLP power management states are disabled All other values reserved
7:4	0h RW	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface. 0h No speed negotiation restrictions. 1h Limit speed negotiation to Generation 1 communication rate. 2h Limit speed negotiation to a rate not greater than Generation 2 communication rate. 3h Limit speed negotiation to a rate not greater than Generation 3 communication rate. All other values reserved. Note: If software changes SPD after port has been enabled, software is required to perform a port reset via DET=1h.

Bit Range	Default & Access	Description
3:0	0h RW	**Device Detection Initialization (DET):** Controls HBA's device detection and interface initialization. 0h No device detection or initialization action requested. 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is continuously transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h Disable the Serial ATA interface and put Phy in offline mode. All other values reserved. This field may only be changed when PxCMD.ST is '0'. Changing this field while the HBA is running results in undefined behavior. When PxCMD.ST is set to '1', this field should have a value of 0h. It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when PxSCTL.DET = 1h

13.8.37 Port-Serial ATA Error (PxSERR1)—Offset 1B0h

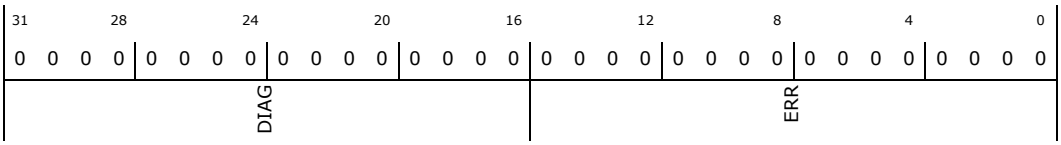
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSERR1: [ABAR] + 1B0h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/1C	**Diagnostics (DIAG):** Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bit Field 31:27 Reserved 26 Exchanged (X): When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. The means by which the implementation determines that the device presence has changed is vendor specific. This bit shall always be set to one anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit. 25 Unrecognized FIS Type (F): Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized. 24 Transport state transition error (T): Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. 23 Link Sequence Error (S): Indicates that one or more Link state machine error conditions were encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. 22 Handshake Error (H): Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame. 21 CRC Error (C): Indicates that one or more CRC errors occurred with the Link Layer. 20 Disparity Error (D): This field is not used by AHCI. 19 10B to 8B Decode Error (B): Indicates that one or more 10B to 8B decoding errors occurred. 18 Comm Wake (W): Indicates that a Comm Wake signal was detected by the Phy. 17 Phy Internal Error (I): Indicates that the Phy detected some internal error. 16 PhyRdy Change (N): When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. The state of this bit is reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled.

Bit Range	Default & Access	Description
15:0	0000h RW/1C	**Error (ERR):** The ERR field contains error information for use by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer. 15:12 Reserved 11 Internal Error (E): The SATA controller failed due to a master or target abort when attempting to access system memory. 10 Protocol Error (P): A violation of the Serial ATA protocol was detected. 9 Persistent Communication or Data Integrity Error (C): A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes. 8 Transient Data Integrity Error (T): A data integrity error occurred that was not recovered by the interface. 7:2 Reserved 1 Recovered Communications Error (M): Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers. 0 Recovered Data Integrity Error (I): A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

13.8.38 Port-Serial ATA Active (PxSACT1)—Offset 1B4h

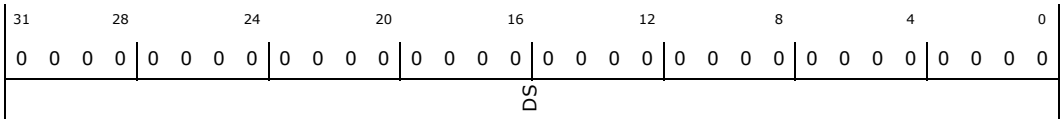
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxSACT1: [ABAR] + 1B4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW/1S	**Device Status (DS):** System software sets this bit for native command queuing commands prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared via the Set Device Bits FIS.

13.8.39 Port-Commands Issued (PxCI1)—Offset 1B8h

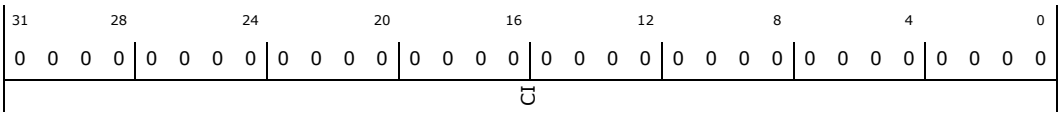
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxCI1: [ABAR] + 1B8h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, ERR, and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when PxCMD.ST is set to 1.

13.8.40 Port-Device Sleep (PxDEVSLP1)—Offset 1C4h

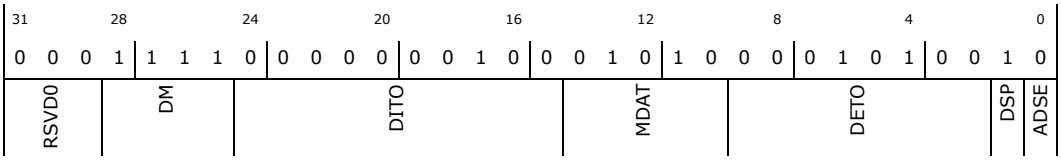
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PxDEVSLP1: [ABAR] + 1C4h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 1E022852h



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:25	Fh RW/O	**DITO Multiplier (DM):** 0's based value that specifies the DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. A value of 0h indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The HBA computes the total idle timeout as a product of DM and DITO (that is, DITO actual = DITO * DM).
24:15	004h RW	**DEVSLP Idle Timeout (DITO):** This field specifies the amount of the time (in approximate 1ms granularity) that the HBA shall wait before driving the DEVSLP signal.
14:10	0Ah RW	**DEVSLP Minimum Assertion Time (MDAT):** This field specifies the minimum amount of time (in 1ms granularity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The nominal value is 10ms and the minimum is 1ms depending on device identification information.
9:2	14h RW	**DEVSLP Exit Timeout (DETO):** This field specifies the maximum duration (in approximate 1ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The nominal value is 20ms while the max value is 255ms depending on device identification information.

Bit Range	Default & Access	Description
1	1h RW/O	**DEVSLP Present (DSP):** If set to 1, the platform supports DEVSLP on this port. If cleared to 0, the platform does not support DEVSLP on this port.
0	0h RW	**Aggressive DEVSLP Enable (ADSE):** When this bit is cleared to 0, the HBA does not enter DEVSLP unless software directed via PxCMD.ICC. This bit shall only be set to 1 if PxDEVSLP.DSP is set to 1. If this bit is set to 1 and software clears the bit to 0, then the HBA shall de-assert the DEVSLP signal if asserted.

13.8.41 Enclosure Management Message Format (EM_MF)—Offset 580h

This register is not implemented in VLV.

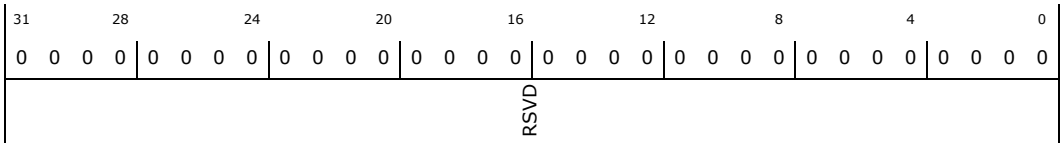
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

EM_MF: [ABAR] + 580h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**RSVD:** Reserved.

13.8.42 Enclosure Management LED (EM_LED)—Offset 584h

This register is not implemented in VLV.

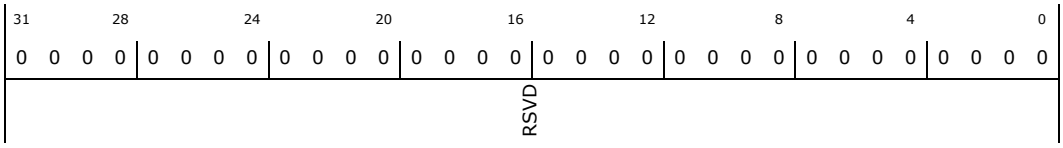
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

EM_LED: [ABAR] + 584h

ABAR Type: PCI Configuration Register (Size: 32 bits)
ABAR Reference: [B:0, D:19, F:0] + 24h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**RSVD:** Reserved.

13.9 SATA Primary Read Command IO Registers

Table 104. Summary of SATA Primary Read Command I/O Registers—PCMDIDEBA

Offset	Size	Register ID—Description	Default Value
1h	1	"Primary Channel Error register (P_ERROR)—Offset 1h" on page 219	00h
2h	1	"Primary Channel Sector Count register (P_SECTOR_COUNT)—Offset 2h" on page 220	00h
3h	1	"Primary Channel Sector Number register (P_SECTOR_NUMBER)—Offset 3h" on page 220	00h
4h	1	"Primary Channel Cylinder Low register (P_CYL_LOW)—Offset 4h" on page 221	00h
5h	1	"Primary Channel Cylinder High register (P_CYL_HIGH)—Offset 5h" on page 221	00h
6h	1	"Primary Channel Device register (P_DRIVE_HEAD)—Offset 6h" on page 222	00h
7h	1	"Primary Channel Status register (P_STATUS)—Offset 7h" on page 223	00h

13.9.1 Primary Channel Error register (P_ERROR)—Offset 1h

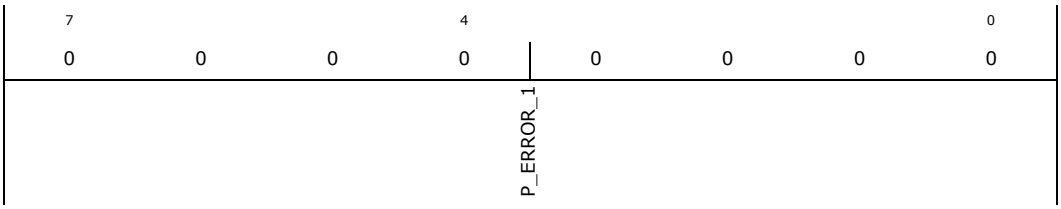
Access Method

Type: I/O Register
(Size: 8 bits)

P_ERROR: [PCMDIDEBA] + 1h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Error (P_ERROR_1):** Error.

13.9.2 Primary Channel Sector Count register (P_SECTOR_COUNT)—Offset 2h

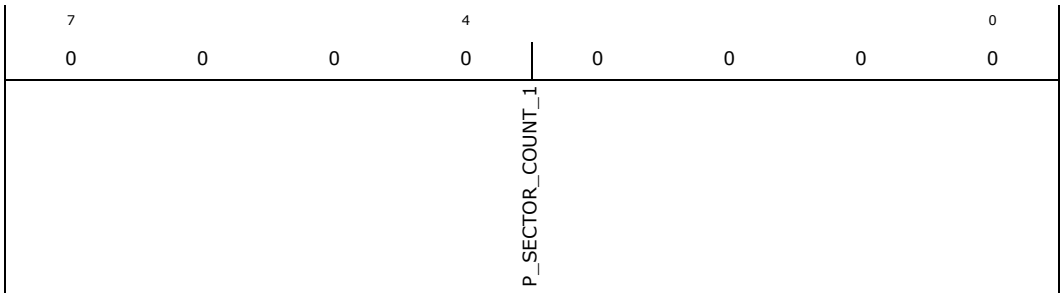
Access Method

Type: I/O Register
(Size: 8 bits)

P_SECTOR_COUNT: [PCMDIDEBA] + 2h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Sector Count (P_SECTOR_COUNT_1):** Sector Count.

13.9.3 Primary Channel Sector Number register (P_SECTOR_NUMBER)—Offset 3h

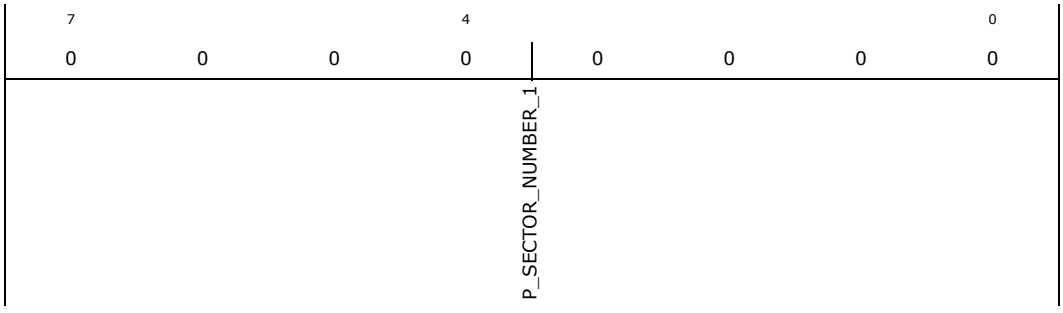
Access Method

Type: I/O Register
(Size: 8 bits)

P_SECTOR_NUMBER: [PCMDIDEBA] + 3h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Sector Number (P_SECTOR_NUMBER_1):** Sector Number.

13.9.4 Primary Channel Cylinder Low register (P_CYL_LOW)—Offset 4h

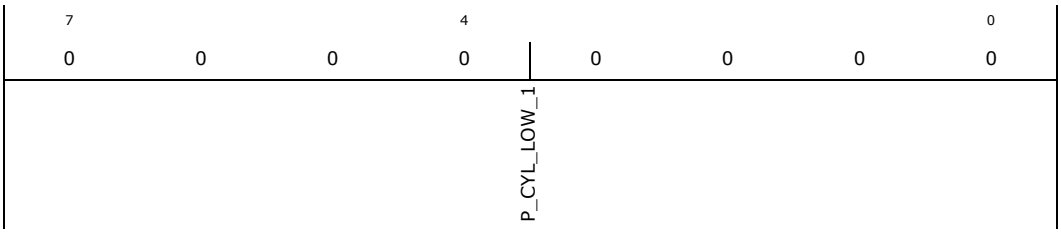
Access Method

Type: I/O Register
(Size: 8 bits)

P_CYL_LOW: [PCMDIDEBA] + 4h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Cylinder Low (P_CYL_LOW_1):** Cylinder Low.

13.9.5 Primary Channel Cylinder High register (P_CYL_HIGH)—Offset 5h

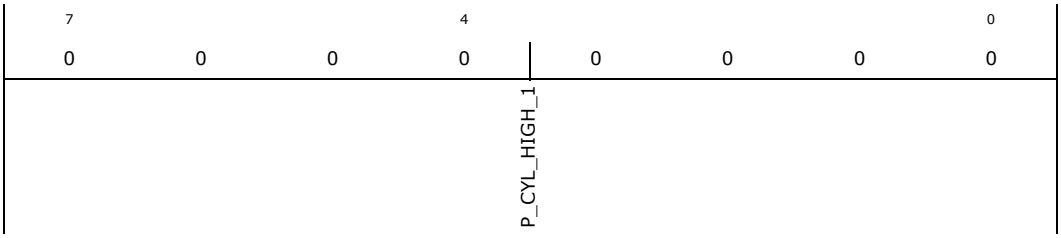
Access Method

Type: I/O Register
(Size: 8 bits)

P_CYL_HIGH: [PCMDIDEBA] + 5h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Cylinder High (P_CYL_HIGH_1):** Cylinder High.

13.9.6 Primary Channel Device register (P_DRIVE_HEAD)—Offset 6h

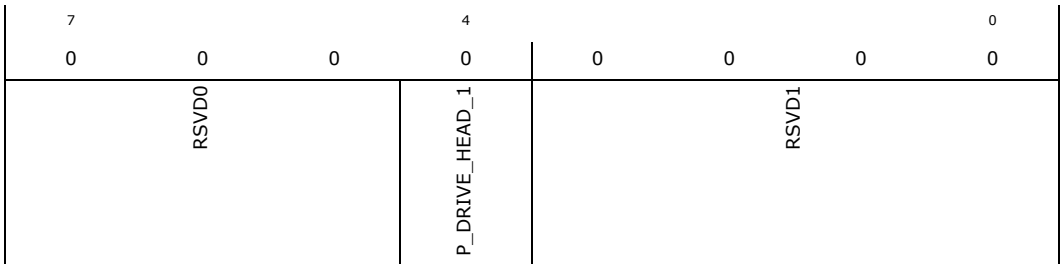
Access Method

Type: I/O Register (Size: 8 bits)

P_DRIVE_HEAD: [PCMDIDEBA] + 6h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h



Bit Range	Default & Access	Description
7:5	0b RO	**RSVD0:** Reserved
4	0h RW	**Device (P_DRIVE_HEAD_1):** Device.
3:0	0b RO	**RSVD1:** Reserved

13.9.7 Primary Channel Status register (P_STATUS)—Offset 7h

Access Method

Type: I/O Register
(Size: 8 bits)

P_STATUS: [PCMDIDEBA] + 7h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
P_STATUS_BSY	P_STATUS_DRDY	P_STATUS_DF	RSVD0	P_STATUS_DRQ	RSVD1		P_STATUS_ERR_CHK

Bit Range	Default & Access	Description
7	0h RW	**BUSY (P_STATUS_BSY):** BUSY.
6	0h RW	**Device Ready (P_STATUS_DRDY):** Device Ready.
5	0h RW	**Device Fault/Stream Error (P_STATUS_DF):** Device Fault/Stream Error.
4	0b RO	**RSVD0:** Reserved
3	0h RW	**Data Request (P_STATUS_DRQ):** Data Request.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**ERR/CHK (P_STATUS_ERR_CHK):** ERR/CHK.

13.10 SATA Primary Write Command IO Registers

Table 105. Summary of SATA Primary Write Command I/O Registers—PCMDIDEBA

Offset	Size	Register ID—Description	Default Value
1h	1	"Primary Channel Features register (P_FEATURES)—Offset 1h" on page 224	00h
7h	1	"Primary Channel Command register (P_COMMAND)—Offset 7h" on page 225	00h

13.10.1 Primary Channel Features register (P_FEATURES)—Offset 1h

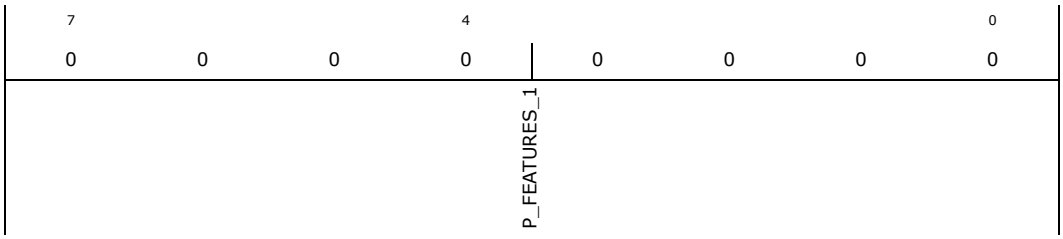
Access Method

Type: I/O Register (Size: 8 bits)

P_FEATURES: [PCMDIDEBA] + 1h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Features (P_FEATURES_1):** Features.

13.10.2 Primary Channel Command register (P_COMMAND)—Offset 7h

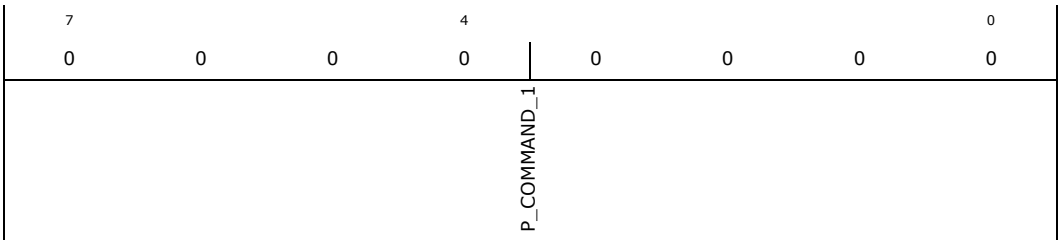
Access Method

Type: I/O Register
(Size: 8 bits)

P_COMMAND: [PCMDIDEBA] + 7h

PCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCMDIDEBA Reference: [B:0, D:19, F:0] + FCh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Command (P_COMMAND_1):** Command.

13.11 SATA Primary Read Control IO Registers

Table 106. Summary of SATA Primary Read Control I/O Registers—PCTLIDEBA

Offset	Size	Register ID—Description	Default Value
2h	1	"Primary Channel Alternate Status register (P_ALT_STATUS)—Offset 2h" on page 226	00h

13.11.1 Primary Channel Alternate Status register (P_ALT_STATUS)—Offset 2h

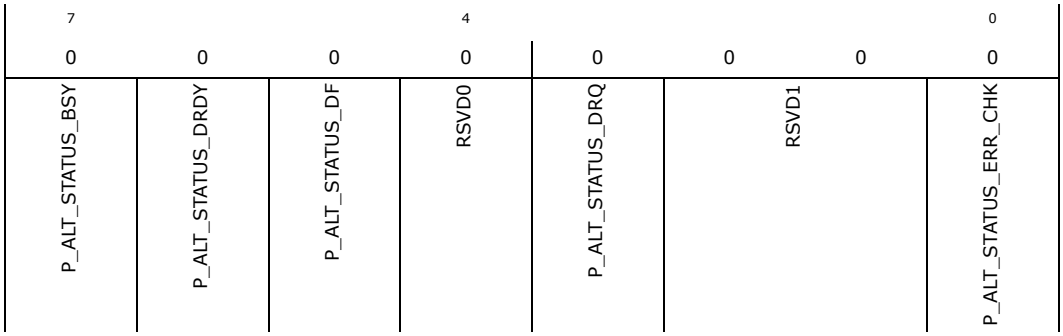
Access Method

Type: I/O Register (Size: 8 bits)

P_ALT_STATUS: [PCTLIDEBA] + 2h

PCTLIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCTLIDEBA Reference: [B:0, D:19, F:0] + 104h

Default: 00h



Bit Range	Default & Access	Description
7	0h RW	**BUSY (P_ALT_STATUS_BSY):** BUSY.
6	0h RW	**Device Ready (P_ALT_STATUS_DRDY):** Device Ready.
5	0h RW	**Device Fault/Stream Error (P_ALT_STATUS_DF):** Device Fault/Stream Error.
4	0b RO	**RSVD0:** Reserved
3	0h RW	**Data Request (P_ALT_STATUS_DRQ):** Data Request.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**ERR/CHK (P_ALT_STATUS_ERR_CHK):** ERR/CHK.

13.12 SATA Primary Write Control IO Registers

Table 107. Summary of SATA Primary Write Control I/O Registers—PCTLIDEBA

Offset	Size	Register ID—Description	Default Value
2h	1	"Primary Channel Device Control register (P_DEVICE_CTRL)—Offset 2h" on page 227	00h

13.12.1 Primary Channel Device Control register (P_DEVICE_CTRL)—Offset 2h

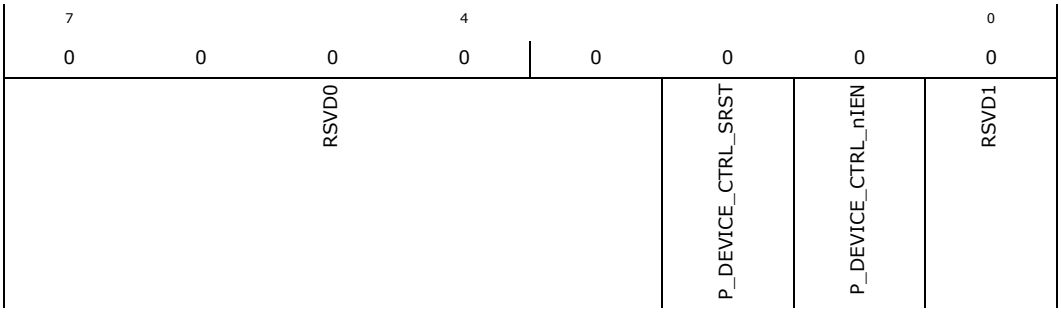
Access Method

Type: I/O Register (Size: 8 bits)

P_DEVICE_CTRL: [PCTLIDEBA] + 2h

PCTLIDEBA Type: PCI Configuration Register (Size: 32 bits)
PCTLIDEBA Reference: [B:0, D:19, F:0] + 104h

Default: 00h



Bit Range	Default & Access	Description
7:3	0b RO	**RSVD0:** Reserved
2	0h RW	**Soft Reset (P_DEVICE_CTRL_SRST):** Soft Reset.
1	0h RW	**Interrupt Enable, Negative Logic (P_DEVICE_CTRL_nIEN):** Interrupt Enable, Negative Logic.
0	0b RO	**RSVD1:** Reserved

13.13 SATA Secondary Read Command IO Registers

Table 108. Summary of SATA Secondary Read Command I/O Registers—SCMDIDEBA

Offset	Size	Register ID—Description	Default Value
1h	1	"Secondary Channel Error register (S_ERROR)—Offset 1h" on page 228	00h
2h	1	"Secondary Channel Sector Count register (S_SECTOR_COUNT)—Offset 2h" on page 229	00h
3h	1	"Secondary Channel Sector Number register (S_SECTOR_NUMBER)—Offset 3h" on page 229	00h
4h	1	"Secondary Channel Cylinder Low register (S_CYL_LOW)—Offset 4h" on page 230	00h
5h	1	"Secondary Channel Cylinder High register (S_CYL_HIGH)—Offset 5h" on page 230	00h
6h	1	"Secondary Channel Device register (S_DRIVE_HEAD)—Offset 6h" on page 231	00h
7h	1	"Secondary Channel Status register (S_STATUS)—Offset 7h" on page 231	00h

13.13.1 Secondary Channel Error register (S_ERROR)—Offset 1h

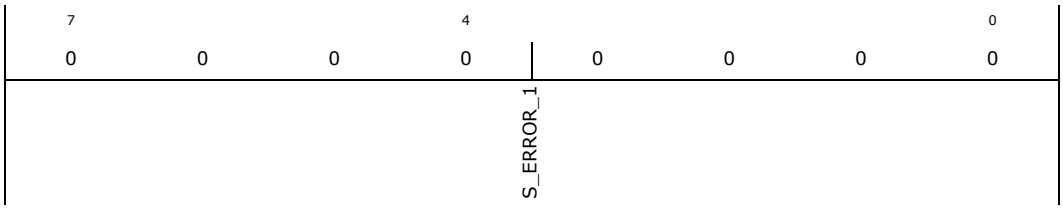
Access Method

Type: I/O Register (Size: 8 bits)

S_ERROR: [SCMDIDEBA] + 1h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Error (S_ERROR_1):** Error.

13.13.2 Secondary Channel Sector Count register (S_SECTOR_COUNT)—Offset 2h

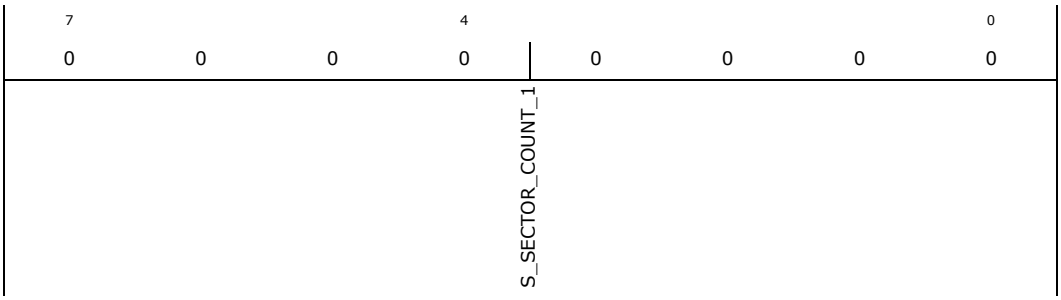
Access Method

Type: I/O Register
(Size: 8 bits)

S_SECTOR_COUNT: [SCMDIDEBA] + 2h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Sector Count (S_SECTOR_COUNT_1):** Sector Count.

13.13.3 Secondary Channel Sector Number register (S_SECTOR_NUMBER)—Offset 3h

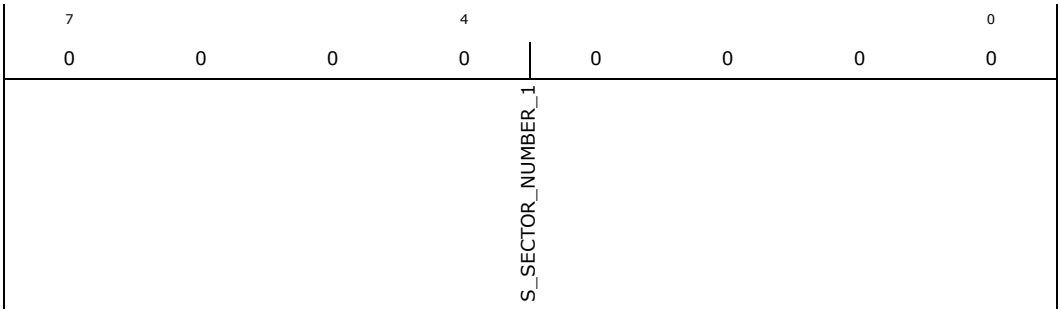
Access Method

Type: I/O Register
(Size: 8 bits)

S_SECTOR_NUMBER: [SCMDIDEBA] + 3h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Sector Number (S_SECTOR_NUMBER_1):** Sector Number.

13.13.4 Secondary Channel Cylinder Low register (S_CYL_LOW)—Offset 4h

Access Method

Type: I/O Register (Size: 8 bits)

S_CYL_LOW: [SCMDIDEBA] + 4h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h

Bit Range	Default & Access	Description
7:0	00h RW	**Cylinder Low (S_CYL_LOW_1):** Cylinder Low.

13.13.5 Secondary Channel Cylinder High register (S_CYL_HIGH)—Offset 5h

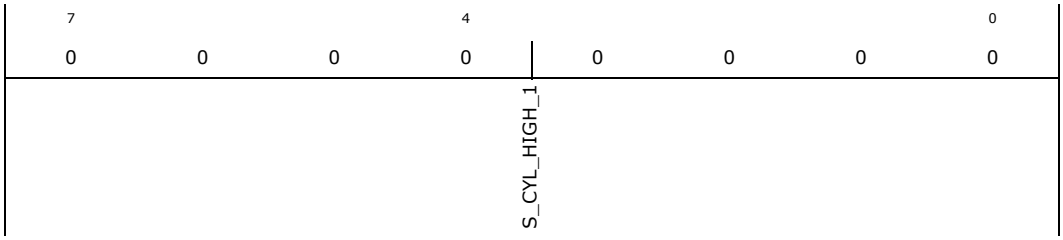
Access Method

Type: I/O Register (Size: 8 bits)

S_CYL_HIGH: [SCMDIDEBA] + 5h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Cylinder High (S_CYL_HIGH_1):** Cylinder High.

13.13.6 Secondary Channel Device register (S_DRIVE_HEAD)—Offset 6h

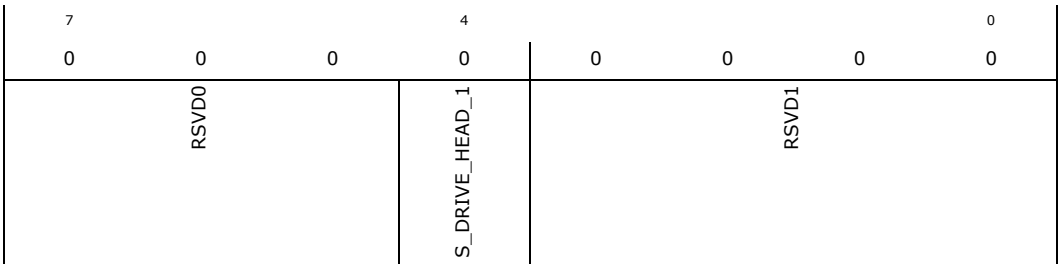
Access Method

Type: I/O Register
(Size: 8 bits)

S_DRIVE_HEAD: [SCMDIDEBA] + 6h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h



Bit Range	Default & Access	Description
7:5	0b RO	**RSVD0:** Reserved
4	0h RW	**Device (S_DRIVE_HEAD_1):** Device.
3:0	0b RO	**RSVD1:** Reserved

13.13.7 Secondary Channel Status register (S_STATUS)—Offset 7h

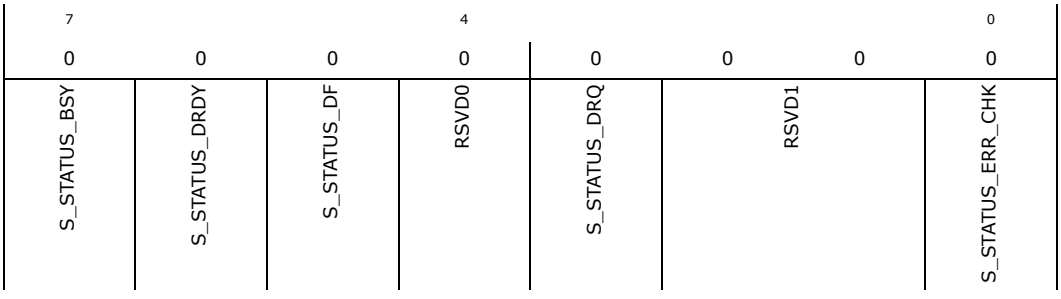
Access Method

Type: I/O Register
(Size: 8 bits)

S_STATUS: [SCMDIDEBA] + 7h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h



Bit Range	Default & Access	Description
7	0h RW	**BUSY (S_STATUS_BSY):** BUSY.

Bit Range	Default & Access	Description
6	0h RW	**Device Ready (S_STATUS_DRDY):** Device Ready.
5	0h RW	**Device Fault/Stream Error (S_STATUS_DF):** Device Fault/Stream Error.
4	0b RO	**RSVD0:** Reserved
3	0h RW	**Data Request (S_STATUS_DRQ):** Data Request.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**ERR/CHK (S_STATUS_ERR_CHK):** ERR/CHK.

13.14 SATA Secondary Write Command IO Registers

Table 109. Summary of SATA Secondary Write Command I/O Registers—SCMDIDEBA

Offset	Size	Register ID—Description	Default Value
1h	1	"Secondary Channel Features register (S_FEATURES)—Offset 1h" on page 233	00h
7h	1	"Secondary Channel Command register (S_COMMAND)—Offset 7h" on page 234	00h

13.14.1 Secondary Channel Features register (S_FEATURES)—Offset 1h

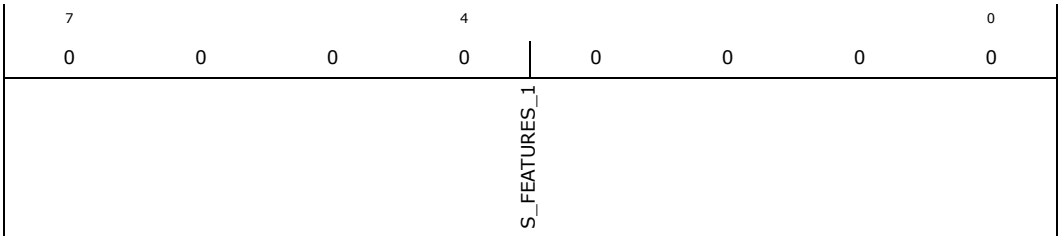
Access Method

Type: I/O Register
(Size: 8 bits)

S_FEATURES: [SCMDIDEBA] + 1h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Features (S_FEATURES_1):** Features.

13.14.2 Secondary Channel Command register (S_COMMAND)—Offset 7h

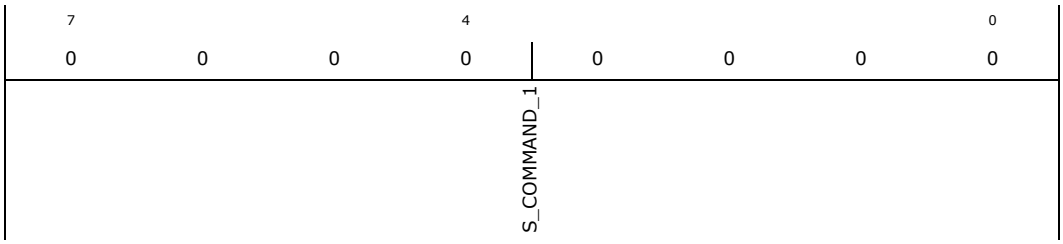
Access Method

Type: I/O Register (Size: 8 bits)

S_COMMAND: [SCMDIDEBA] + 7h

SCMDIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCMDIDEBA Reference: [B:0, D:19, F:0] + 100h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Command (S_COMMAND_1):** Command.

13.15 SATA Secondary Read Control IO Registers

Table 110. Summary of SATA Secondary Read Control I/O Registers—SCTLIDEBA

Offset	Size	Register ID—Description	Default Value
2h	1	"Secondary Channel Alternate Status register (S_ALT_STATUS)—Offset 2h" on page 235	00h

13.15.1 Secondary Channel Alternate Status register (S_ALT_STATUS)—Offset 2h

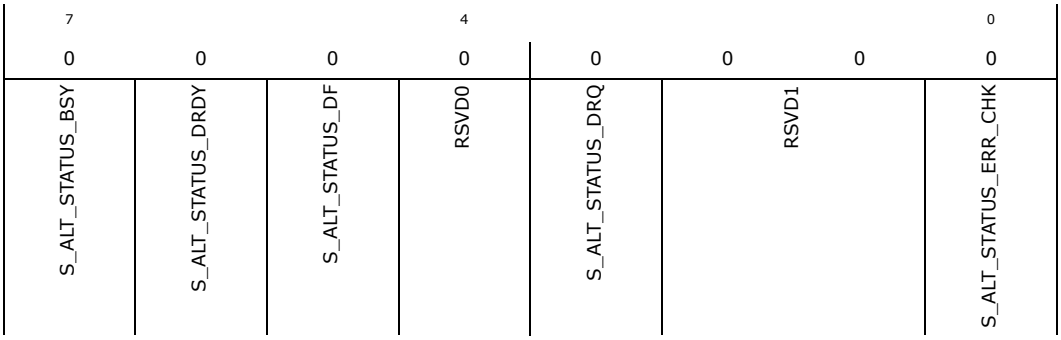
Access Method

Type: I/O Register (Size: 8 bits)

S_ALT_STATUS: [SCTLIDEBA] + 2h

SCTLIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCTLIDEBA Reference: [B:0, D:19, F:0] + 108h

Default: 00h



Bit Range	Default & Access	Description
7	0h RW	**BUSY (S_ALT_STATUS_BSY):** BUSY.
6	0h RW	**Device Ready (S_ALT_STATUS_DRDY):** Device Ready.
5	0h RW	**Device Fault/Stream Error (S_ALT_STATUS_DF):** Device Fault/Stream Error.
4	0b RO	**RSVD0:** Reserved
3	0h RW	**Data Request (S_ALT_STATUS_DRQ):** Data Request.
2:1	0b RO	**RSVD1:** Reserved
0	0h RW	**ERR/CHK (S_ALT_STATUS_ERR_CHK):** ERR/CHK.

13.16 SATA Secondary Write Control IO Registers

Table 111. Summary of SATA Secondary Write Control I/O Registers—SCTLIDEBA

Offset	Size	Register ID—Description	Default Value
2h	1	"Secondary Channel Device Control register (S_DEVICE_CTRL)—Offset 2h" on page 236	00h

13.16.1 Secondary Channel Device Control register (S_DEVICE_CTRL)—Offset 2h

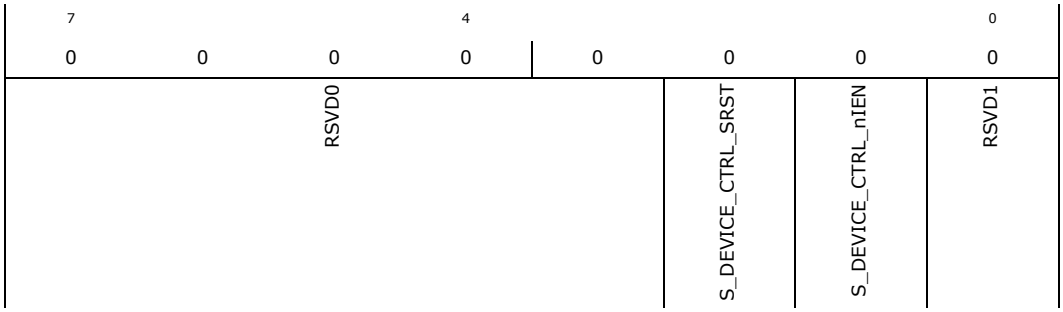
Access Method

Type: I/O Register
(Size: 8 bits)

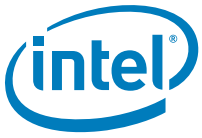
S_DEVICE_CTRL: [SCTLIDEBA] + 2h

SCTLIDEBA Type: PCI Configuration Register (Size: 32 bits)
SCTLIDEBA Reference: [B:0, D:19, F:0] + 108h

Default: 00h



Bit Range	Default & Access	Description
7:3	0b RO	**RSVD0:** Reserved
2	0h RW	**Soft Reset (S_DEVICE_CTRL_SRST):** Soft Reset.
1	0h RW	**Interrupt Enable, Negative Logic (S_DEVICE_CTRL_nIEN):** Interrupt Enable, Negative Logic.
0	0b RO	**RSVD1:** Reserved



13.17 SATA Lane 0 Electrical Register Address Map

Table 112. Summary of SATA Lane 0 Electrical Message Bus Registers—0xA3 (Global Offset 2200h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 238	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 239	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 241	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 242	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 243	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 244	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 245	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 246	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 247	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 248	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 250	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 251	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 253	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 254	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 255	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 256	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 258	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 260	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 262	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 263	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 264	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 265	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 266	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 267	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 268	0001C020h

13.17.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

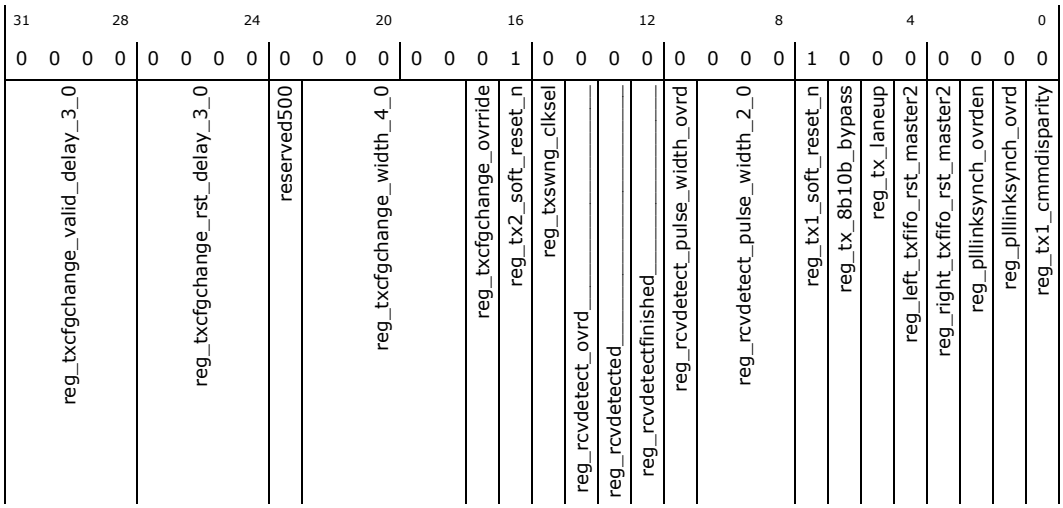
Type: Message Bus Register (Size: 32 bits)

pcs_dword0: [Port: 0xA3] + (2200h + 0h)

Op Codes:

0h - Read, 1h - Write

Default: 00010080h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished:** override for rcvdetectfinished

Bit Range	Default & Access	Description
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

13.17.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

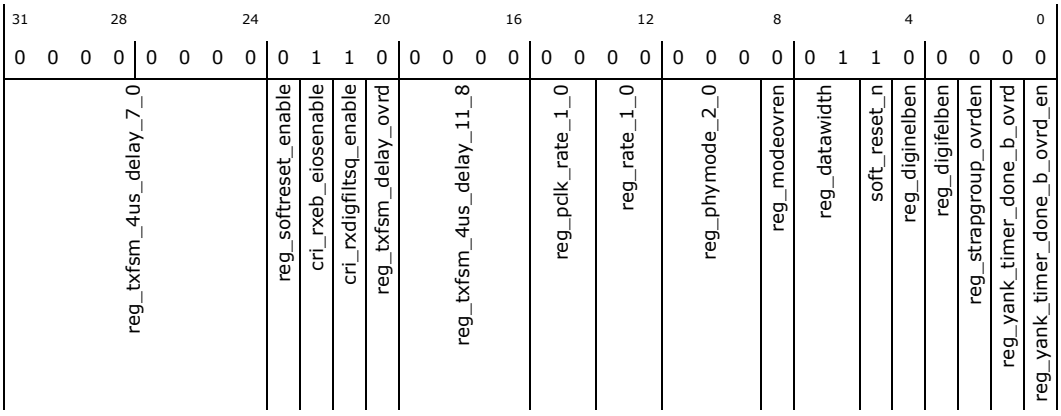
Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA3] + (2200h + 4h)

Op Codes:

0h - Read, 1h - Write

Default: 00600060h



Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

13.17.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

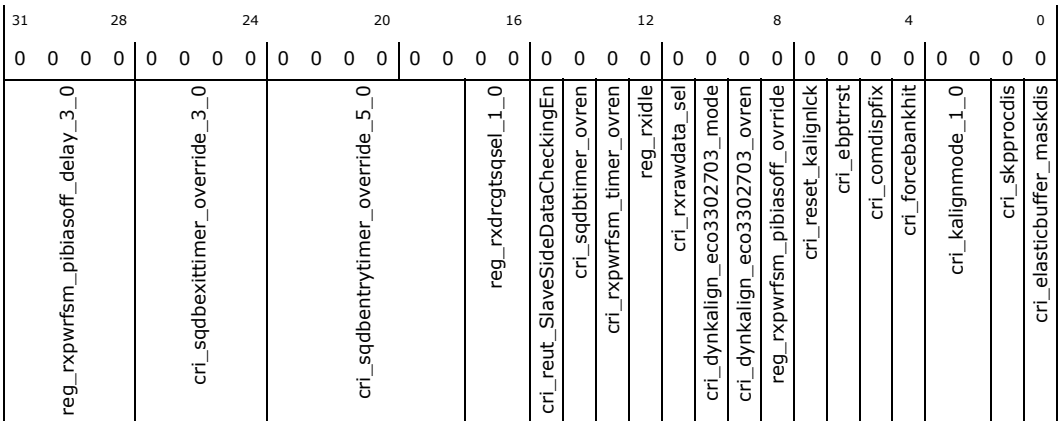
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword2: [Port: 0xA3] + (2200h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]

Bit Range	Default & Access	Description
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

13.17.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

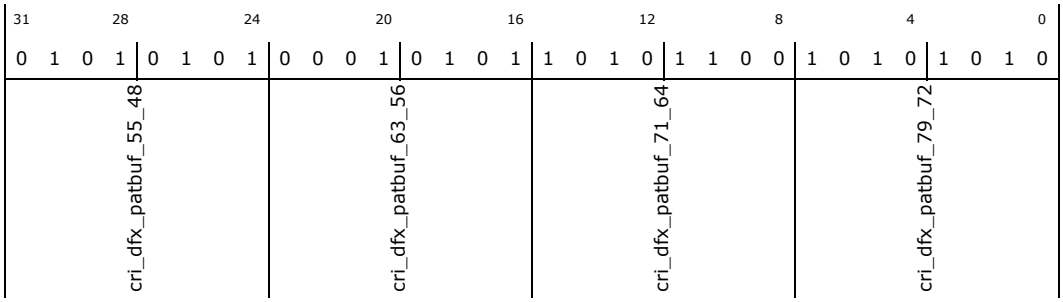
Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA3] + (2200h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 5515ACAAh



Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

Bit Range	Default & Access	Description
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

13.17.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

Access Method

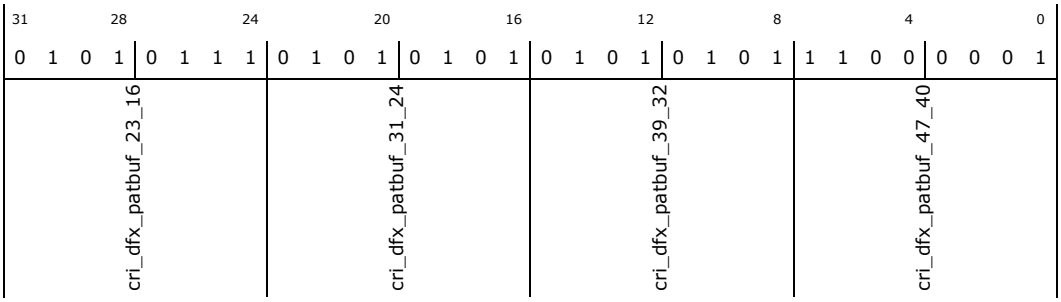
Type: Message Bus Register (Size: 32 bits)

pcs_dword4: [Port: 0xA3] + (2200h + 10h)

Op Codes:

0h - Read, 1h - Write

Default: 575555C1h



Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

13.17.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

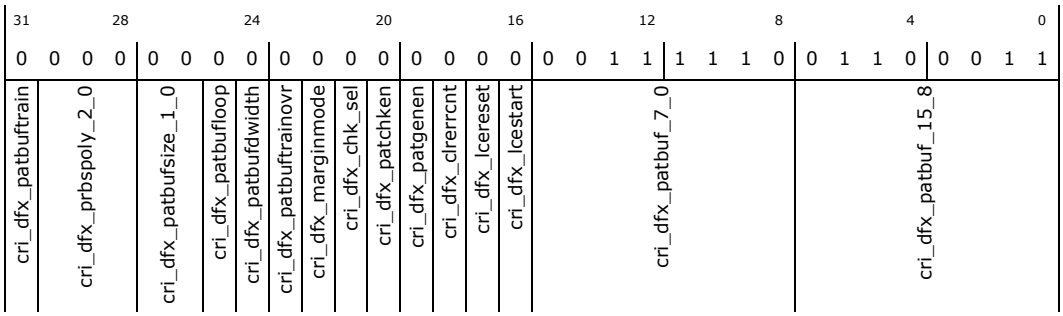
Type: Message Bus Register (Size: 32 bits)

pcs_dword5: [Port: 0xA3] + (2200h + 14h)

Op Codes:

0h - Read, 1h - Write

Default: 00003E63h



Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0: Standard Mode (default) 1: Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0: Disable Pattern Checker (default) 1: Enable Pattern Checker

Bit Range	Default & Access	Description
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass multiplexes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

13.17.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

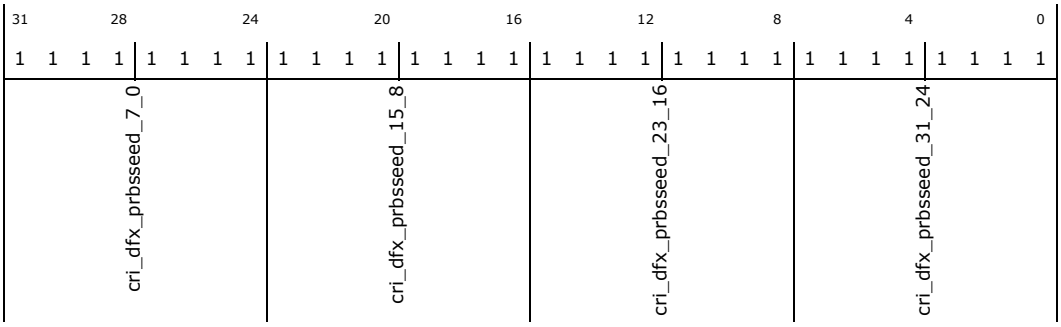
Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA3] + (2200h + 18h)

Op Codes:

0h - Read, 1h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

13.17.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

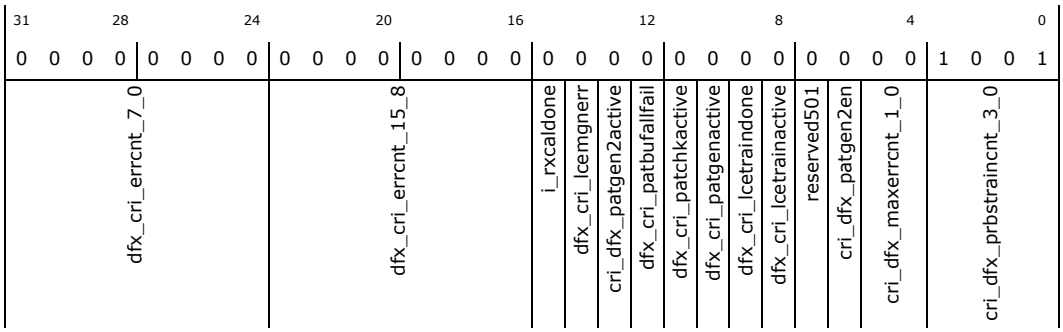
Type: Message Bus Register (Size: 32 bits)

pcs_dword7: [Port: 0xA3] + (2200h + 1Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000009h



Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0: Disable second Pattern Generator (default) 1: Enable second Pattern Generator

Bit Range	Default & Access	Description
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00: 2^16 (default) 01: 2^10 10: 2^8 11: 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

13.17.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

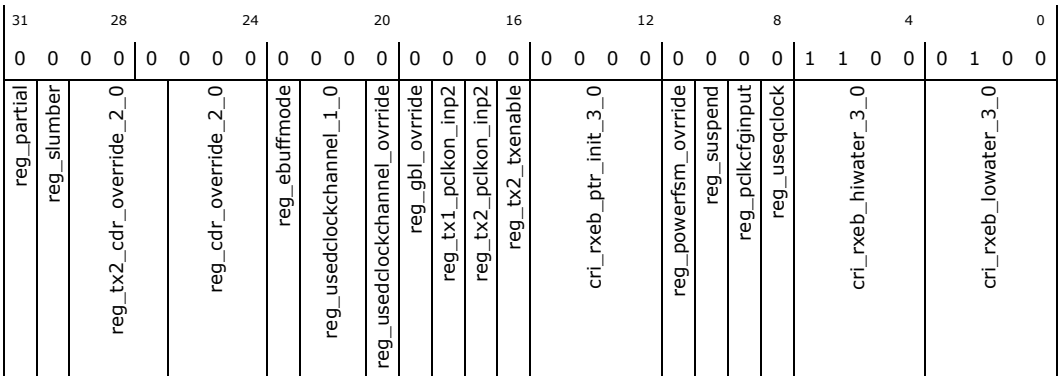
Type: Message Bus Register (Size: 32 bits)

pcs_dword8: [Port: 0xA3] + (2200h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 000000C4h



Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1

Bit Range	Default & Access	Description
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; multiplex select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

13.17.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

Access Method

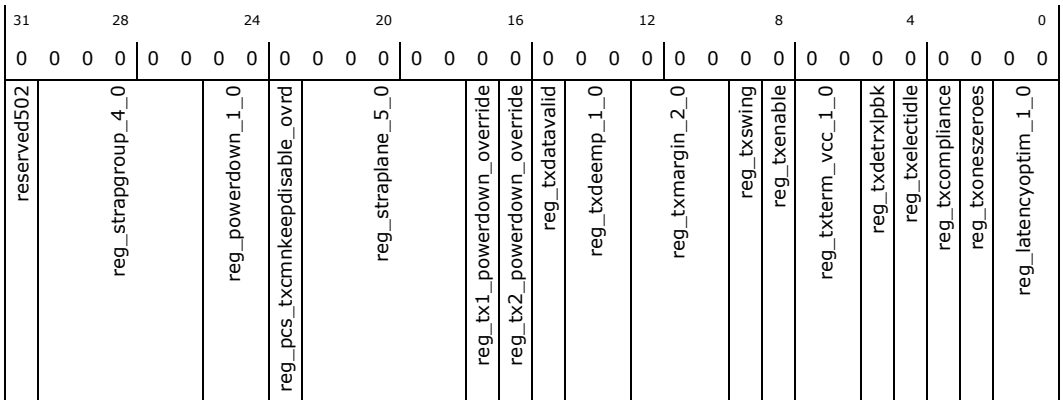
Type: Message Bus Register (Size: 32 bits)

pcs_dword9: [Port: 0xA3] + (2200h + 24h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup

Bit Range	Default & Access	Description
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1: selects reg_powerdown[1:0] 0: selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1: selects reg_powerdown[1:0] 0: selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

13.17.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

Access Method

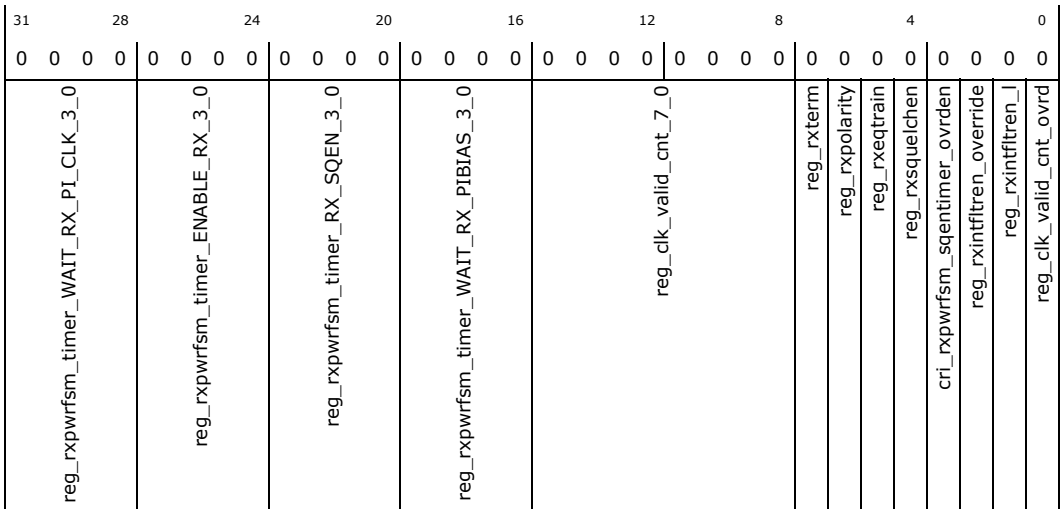
Type: Message Bus Register (Size: 32 bits)

pcs_dword10: [Port: 0xA3] + (2200h + 28h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling PHY status.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).

Bit Range	Default & Access	Description
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

13.17.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

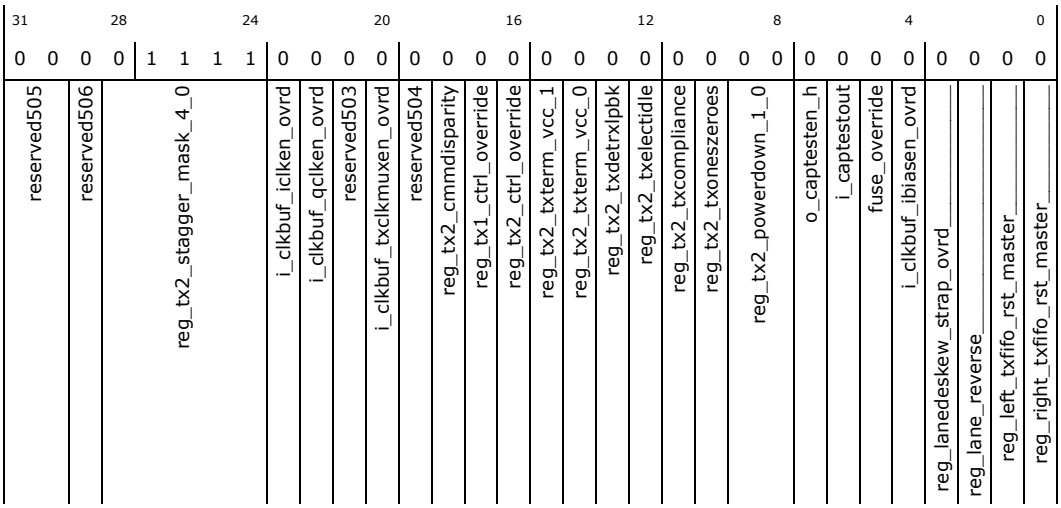
Type: Message Bus Register (Size: 32 bits)

pcs_dword11: [Port: 0xA3] + (2200h + 2Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0F000000h



Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved

Bit Range	Default & Access	Description
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection multiplex Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd_____:** reserved
2	0h RW	**reg_lane_reverse_____:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____:** reserved
0	0h RW	**reg_right_txfifo_rst_master_____:** reserved

13.17.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

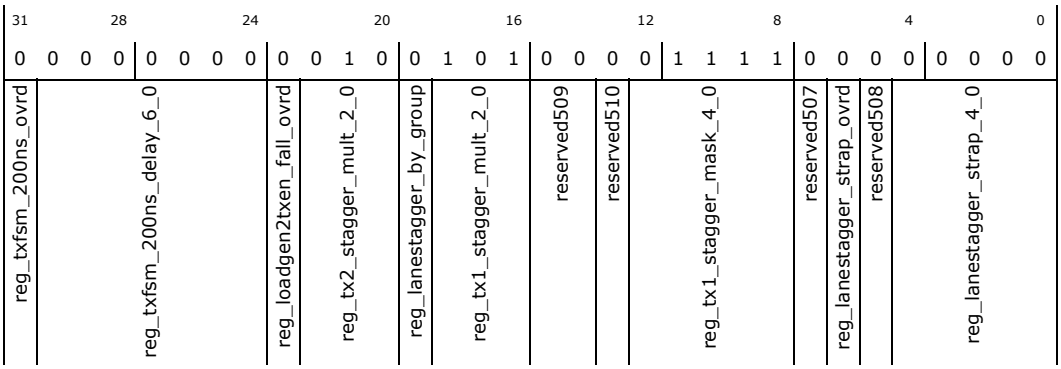
Type: Message Bus Register (Size: 32 bits)

pcs_dword12: [Port: 0xA3] + (2200h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00250F00h



Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved

Bit Range	Default & Access	Description
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

13.17.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

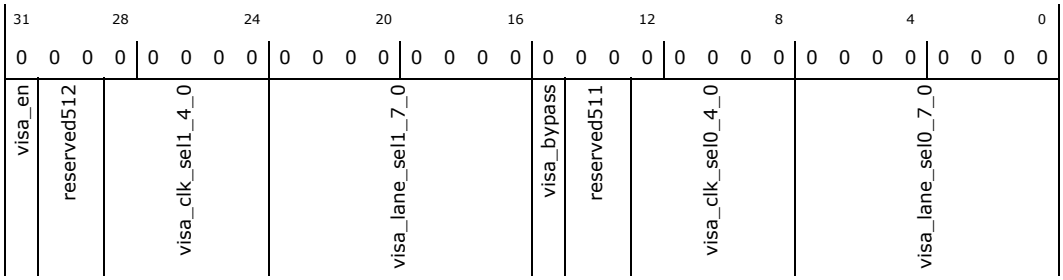
Type: Message Bus Register (Size: 32 bits)

pcs_dword13: [Port: 0xA3] + (2200h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

13.17.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

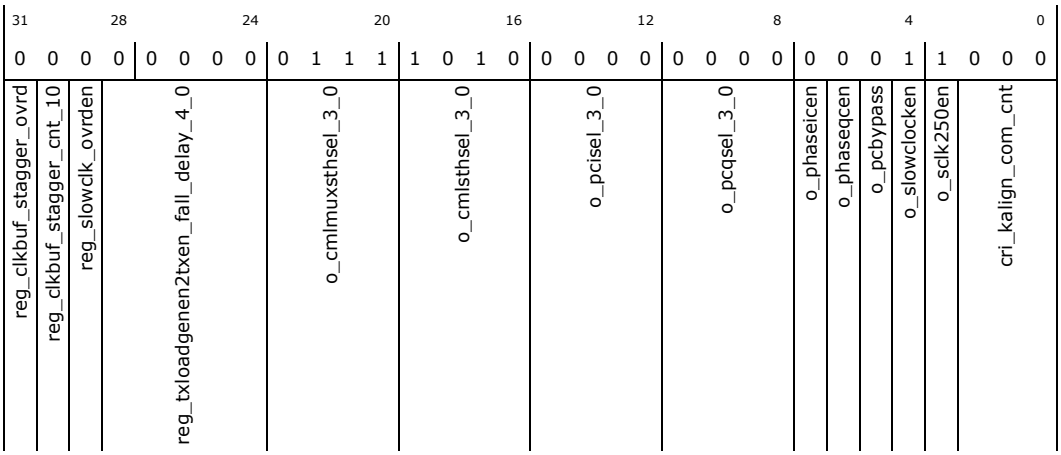
Type: Message Bus Register (Size: 32 bits)

pcs_dword14: [Port: 0xA3] + (2200h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 007A0018h



Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.

Bit Range	Default & Access	Description
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

13.17.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

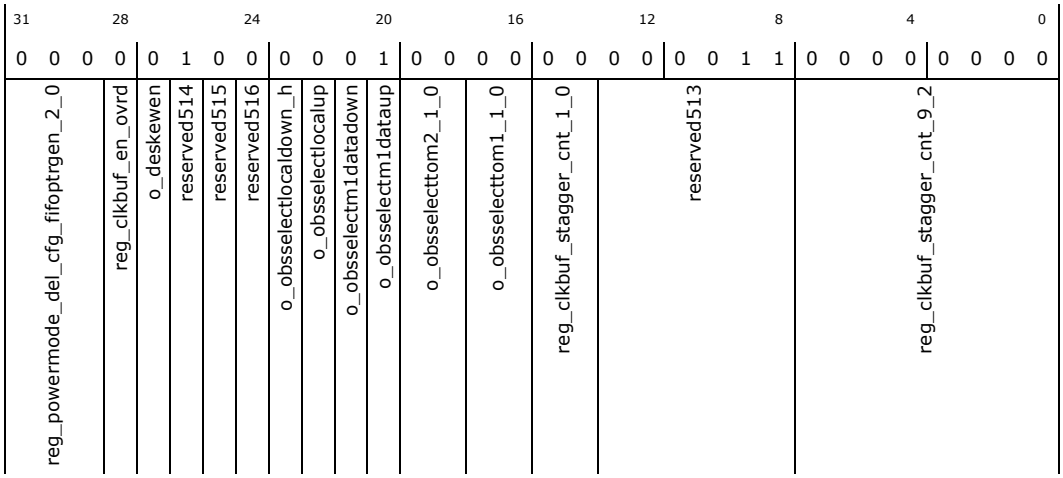
Type: Message Bus Register (Size: 32 bits)

pcs_dword15: [Port: 0xA3] + (2200h + 3Ch)

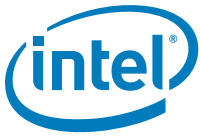
Op Codes:

0h - Read, 1h - Write

Default: 04100300h



Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved



Bit Range	Default & Access	Description
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select multiplexes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select multiplexes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

13.17.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

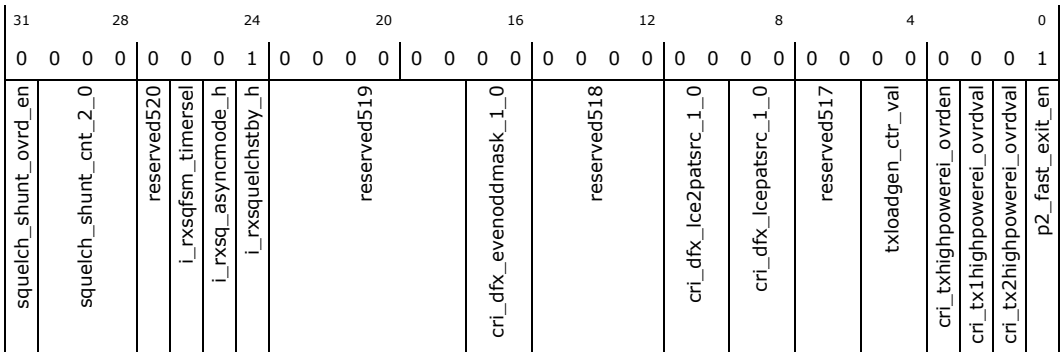
Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA3] + (2200h + 40h)

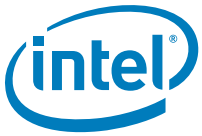
Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved



Bit Range	Default & Access	Description
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

13.17.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

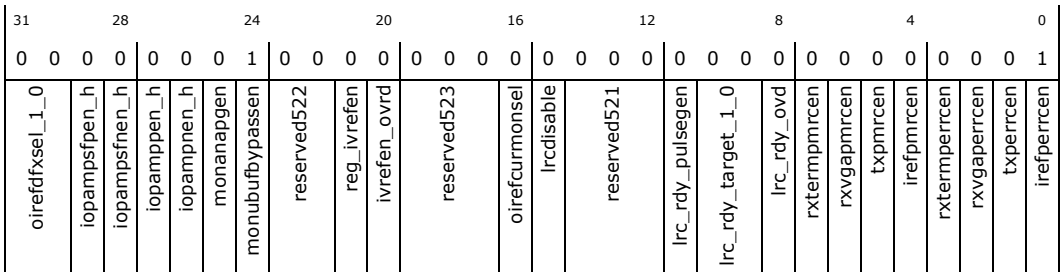
Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA3] + (2200h + 44h)

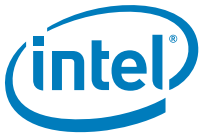
Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved



Bit Range	Default & Access	Description
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

13.17.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

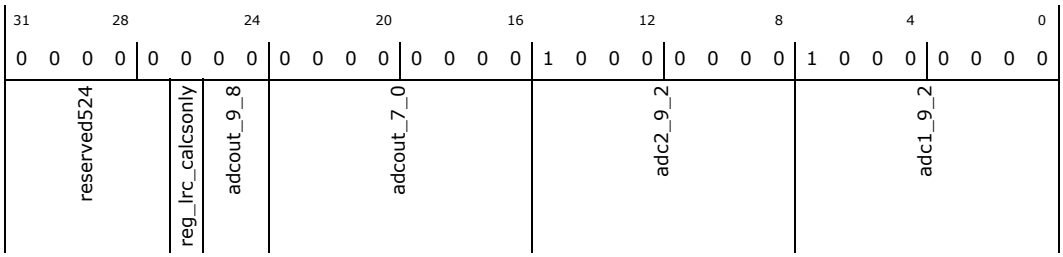
Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA3] + (2200h + 48h)

Op Codes:

0h - Read, 1h - Write

Default: 00008080h



Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimation filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimation filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

13.17.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

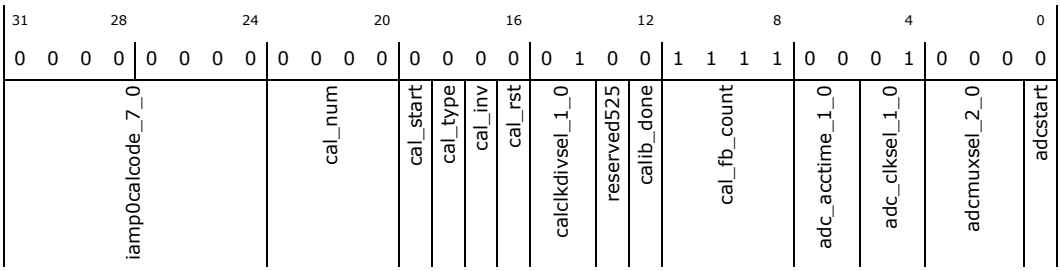
Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA3] + (2200h + 4Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00004F10h



Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [Iyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.

Bit Range	Default & Access	Description
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

13.17.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

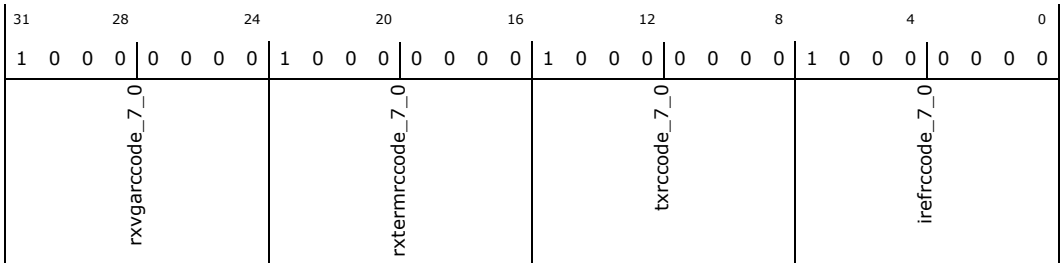
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA3] + (2200h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

13.17.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

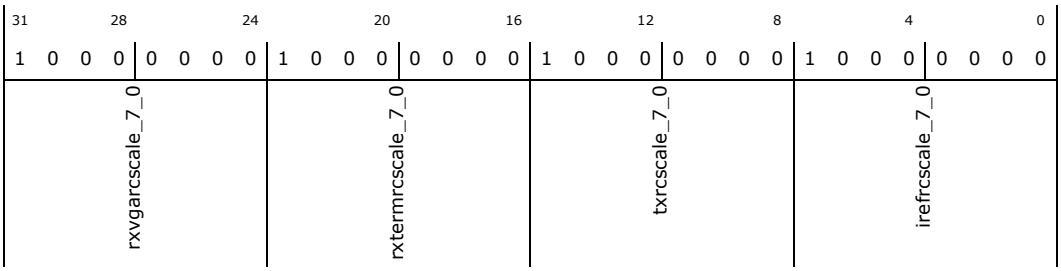
Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA3] + (2200h + 54h)

Op Codes:

0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

13.17.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

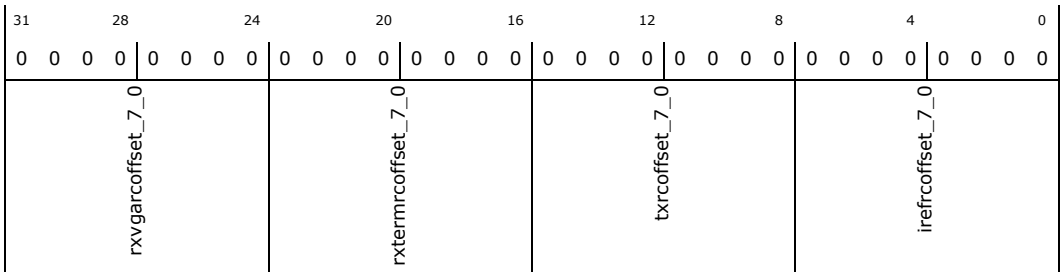
Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA3] + (2200h + 58h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

13.17.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

Access Method

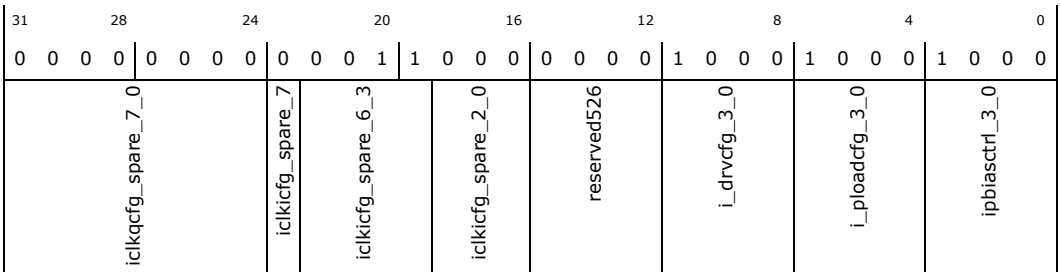
Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA3] + (2200h + 5Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00180888h



Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

13.17.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

Access Method

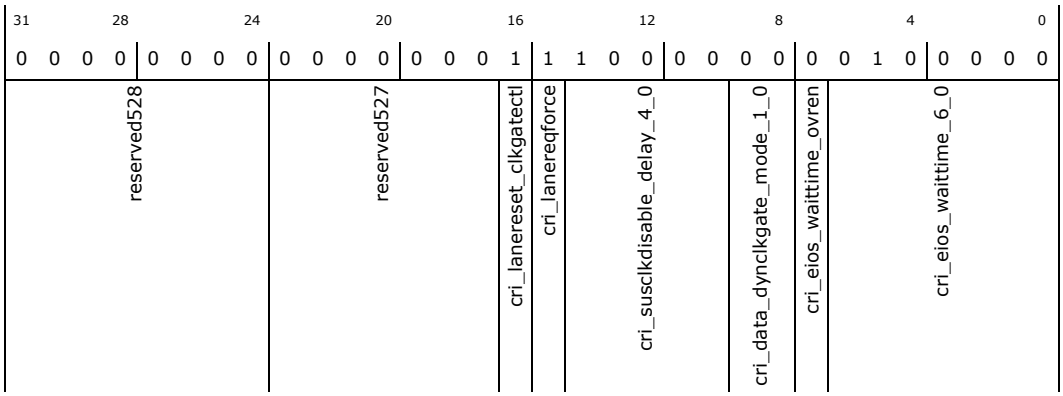
Type: Message Bus Register (Size: 32 bits)

pcs_dword24: [Port: 0xA3] + (2200h + 60h)

Op Codes:

0h - Read, 1h - Write

Default: 0001C020h



Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (that is, 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay ..... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay

Bit Range	Default & Access	Description
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

13.18 SATA Lane 0 Electrical Register Address Map

Table 113. Summary of SATA Lane 0 Electrical Message Bus Registers—0xA3 (Global Offset 2280h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 270	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 271	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 272	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 273	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 274	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 275	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 275	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 276	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 277	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 278	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 279	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 280	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 282	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 283	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 284	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 285	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 286	00008A00h

13.18.1 TX_DWORD0 (tx_dword0)—Offset 0h

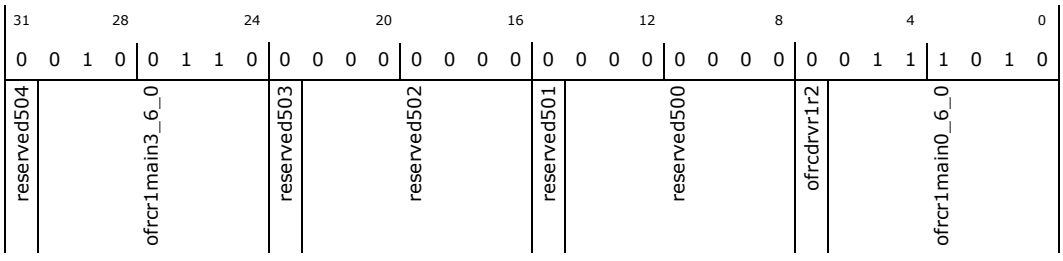
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword0: [Port: 0xA3] + (2280h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah



Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

13.18.2 TX_DWORD1 (tx_dword1)—Offset 4h

Access Method

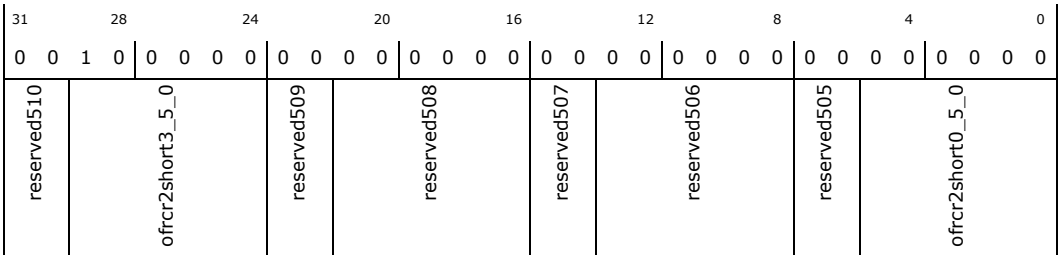
Type: Message Bus Register (Size: 32 bits)

tx_dword1: [Port: 0xA3] + (2280h + 4h)

Op Codes:

0h - Read, 1h - Write

Default: 20000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

13.18.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

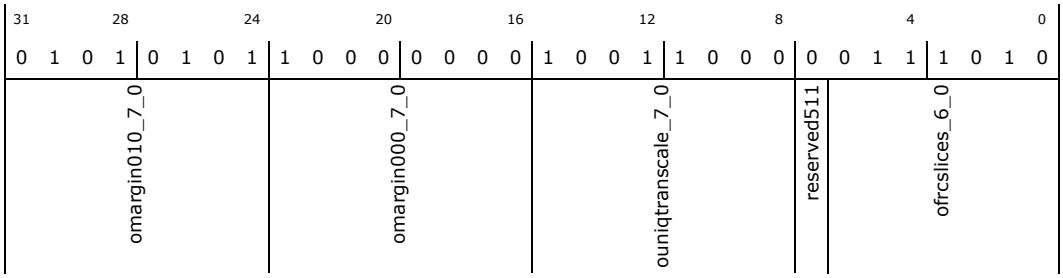
Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA3] + (2280h + 8h)

Op Codes:

0h - Read, 1h - Write

Default: 5580983Ah



Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on datarateﬁt and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

13.18.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

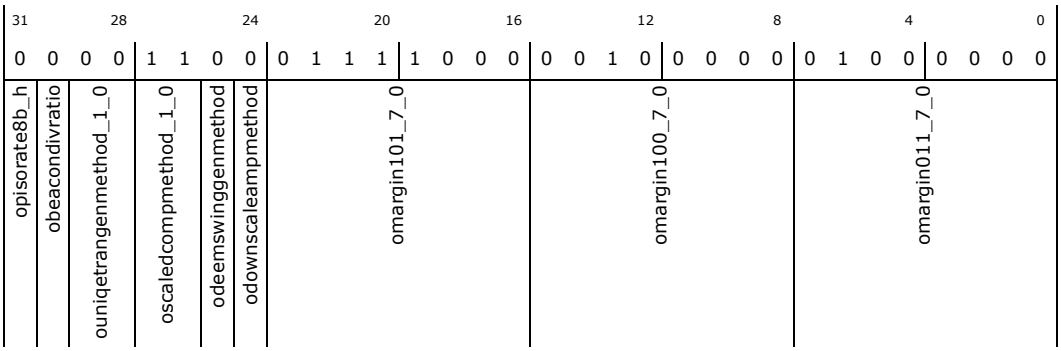
Type: Message Bus Register (Size: 32 bits)

tx_dword3: [Port: 0xA3] + (2280h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0C782040h



Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p

Bit Range	Default & Access	Description
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

13.18.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

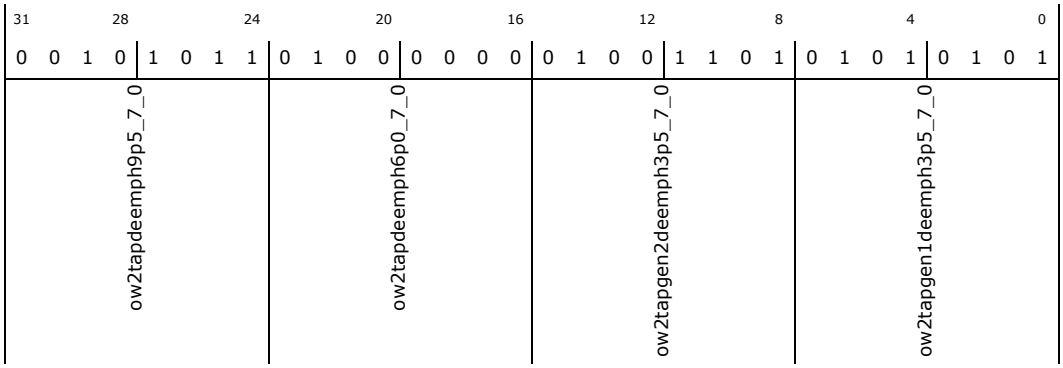
Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA3] + (2280h + 10h)

Op Codes:

0h - Read, 1h - Write

Default: 2B404D55h



Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

13.18.6 TX_DWORD5 (tx_dword5)—Offset 14h

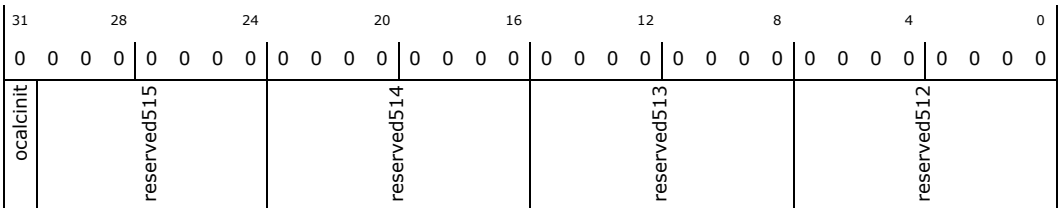
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA3] + (2280h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

13.18.7 TX_DWORD6 (tx_dword6)—Offset 18h

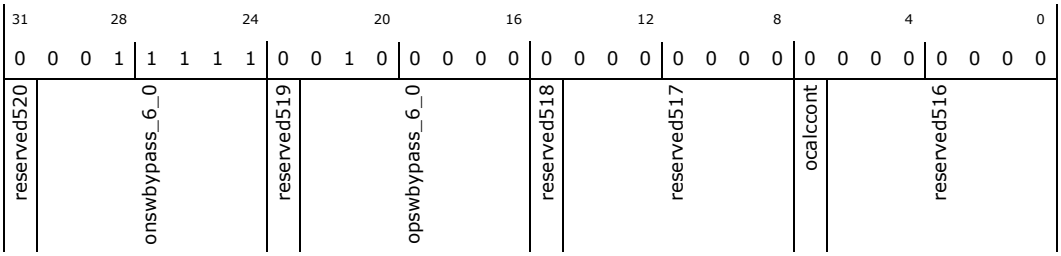
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword6: [Port: 0xA3] + (2280h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h



Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved

Bit Range	Default & Access	Description
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively
6:0	0h RO	**reserved516:** reserved

13.18.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

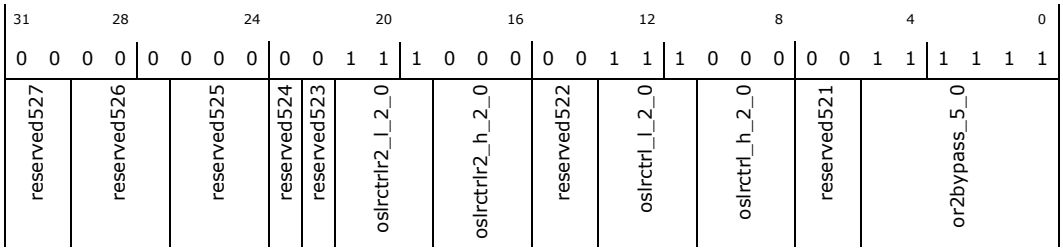
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword7: [Port: 0xA3] + (2280h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh



Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved

Bit Range	Default & Access	Description
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

13.18.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

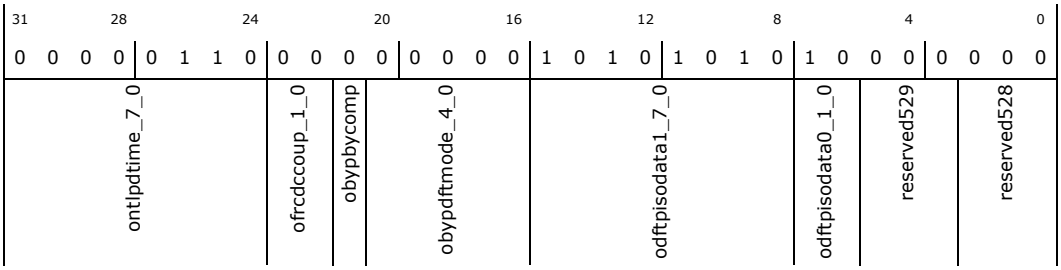
Type: Message Bus Register (Size: 32 bits)

tx_dword8: [Port: 0xA3] + (2280h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 0600AA80h



Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG

Bit Range	Default & Access	Description
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

13.18.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

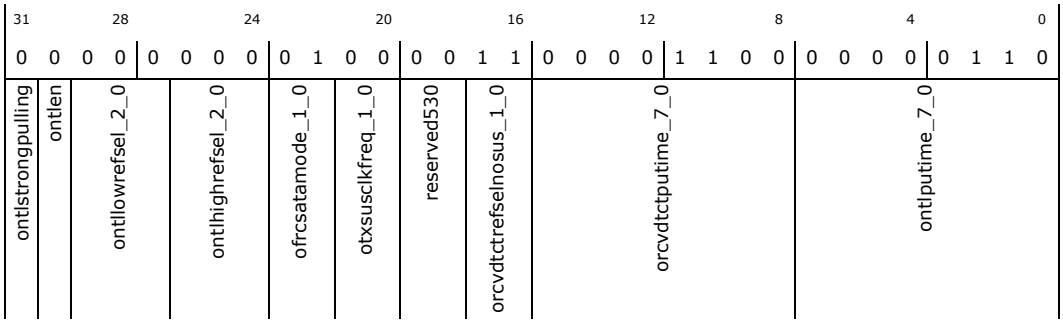
Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA3] + (2280h + 24h)

Op Codes:

0h - Read, 1h - Write

Default: 00430C06h



Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active

Bit Range	Default & Access	Description
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

13.18.11 TX_DWORD10 (tx_dword10)—Offset 28h

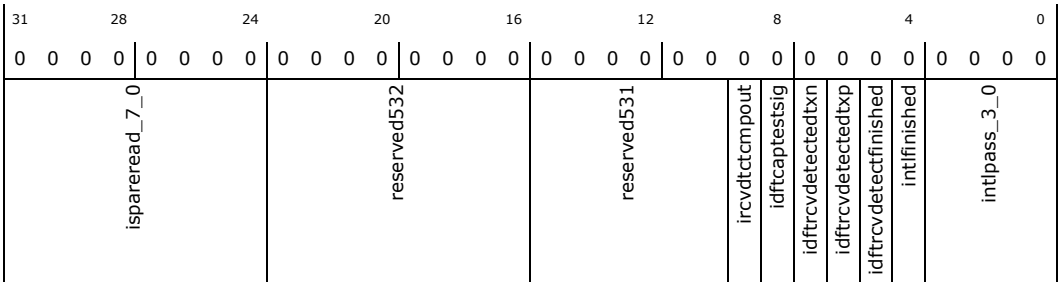
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword10: [Port: 0xA3] + (2280h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

13.18.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

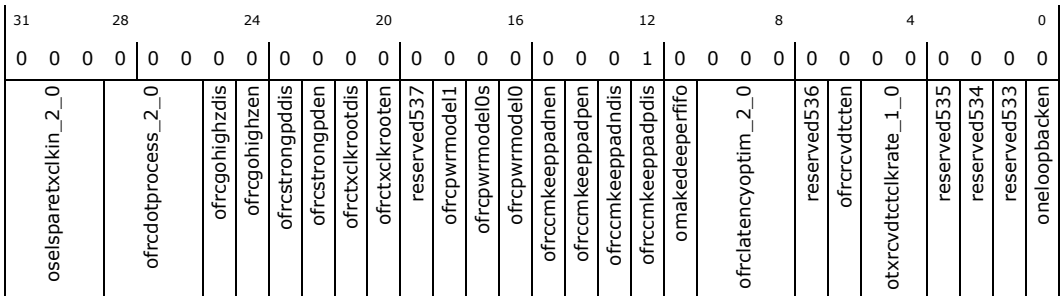
Type: Message Bus Register (Size: 32 bits)

tx_dword11: [Port: 0xA3] + (2280h + 2Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00001000h



Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN

Bit Range	Default & Access	Description
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

13.18.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

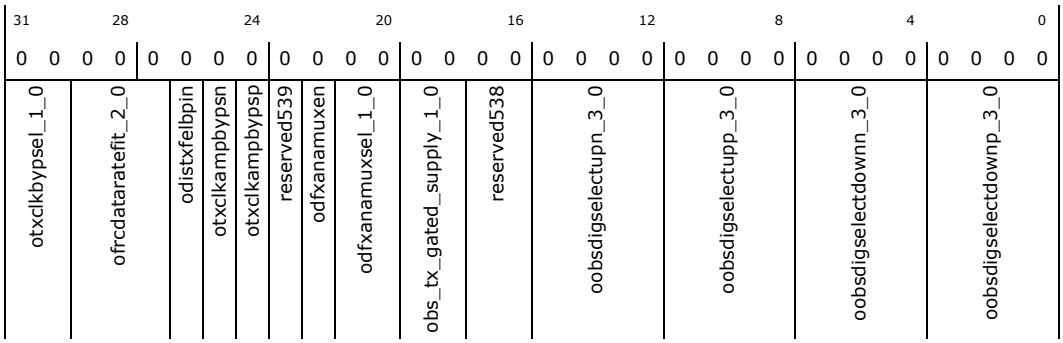
Type: Message Bus Register (Size: 32 bits)

tx_dword12: [Port: 0xA3] + (2280h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - datarate fit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - datarate fit must be '11'
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]

Bit Range	Default & Access	Description
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

13.18.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

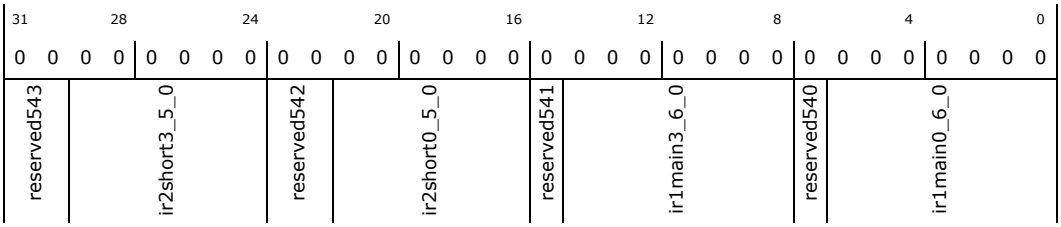
Type: Message Bus Register (Size: 32 bits)

tx_dword13: [Port: 0xA3] + (2280h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

13.18.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

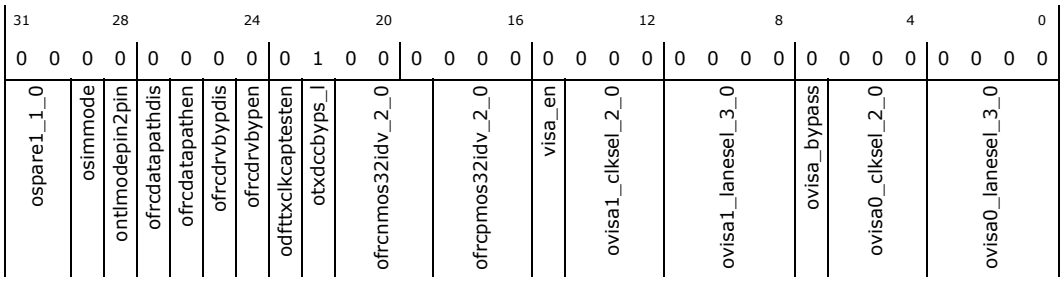
Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA3] + (2280h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 00400000h



Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.

Bit Range	Default & Access	Description
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

13.18.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

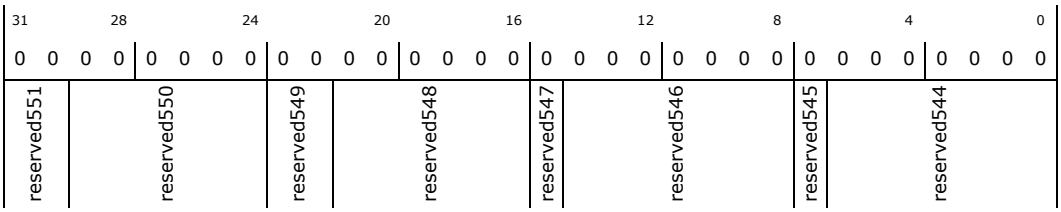
Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA3] + (2280h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

13.18.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

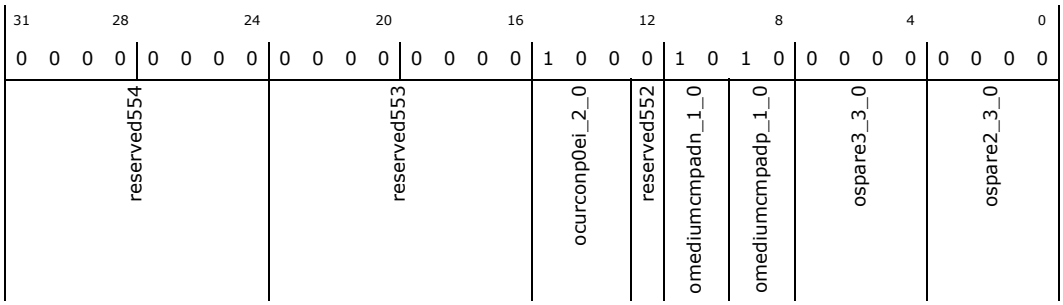
Type: Message Bus Register (Size: 32 bits)

tx_dword16: [Port: 0xA3] + (2280h + 40h)

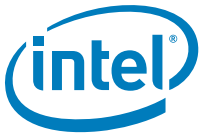
Op Codes:

0h - Read, 1h - Write

Default: 00008A00h



Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits



13.19 SATA Lane 1 Electrical Register Address Map

Table 114. Summary of SATA Lane 1 Electrical Message Bus Registers—0xA3 (Global Offset 2400h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 288	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 290	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 291	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 293	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 294	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 295	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 296	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 297	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 298	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 299	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 301	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 302	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 304	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 305	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 306	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 307	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 309	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 311	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 313	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 314	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 315	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 316	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 317	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 318	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 319	0001C020h

13.19.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

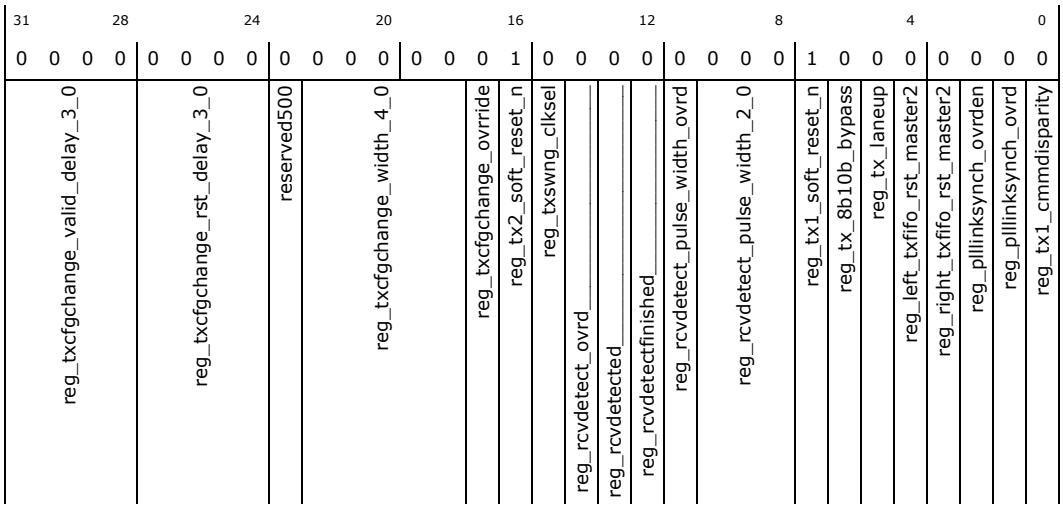
Type: Message Bus Register (Size: 32 bits)

pcs_dword0: [Port: 0xA3] + (2400h + 0h)

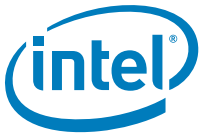
Op Codes:

0h - Read, 1h - Write

Default: 00010080h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd_____:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected_____:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished_____:** override for rcvdetectfinished



Bit Range	Default & Access	Description
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

13.19.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

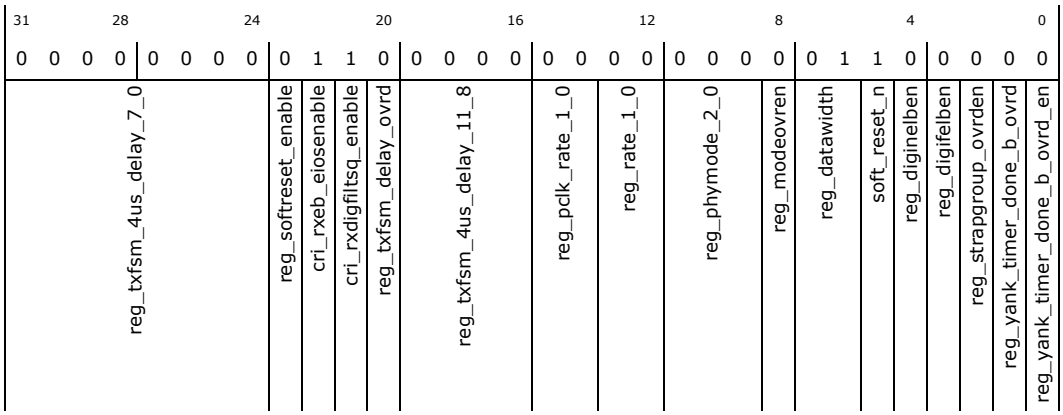
Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA3] + (2400h + 4h)

Op Codes:

0h - Read, 1h - Write

Default: 00600060h



Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width

Bit Range	Default & Access	Description
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

13.19.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

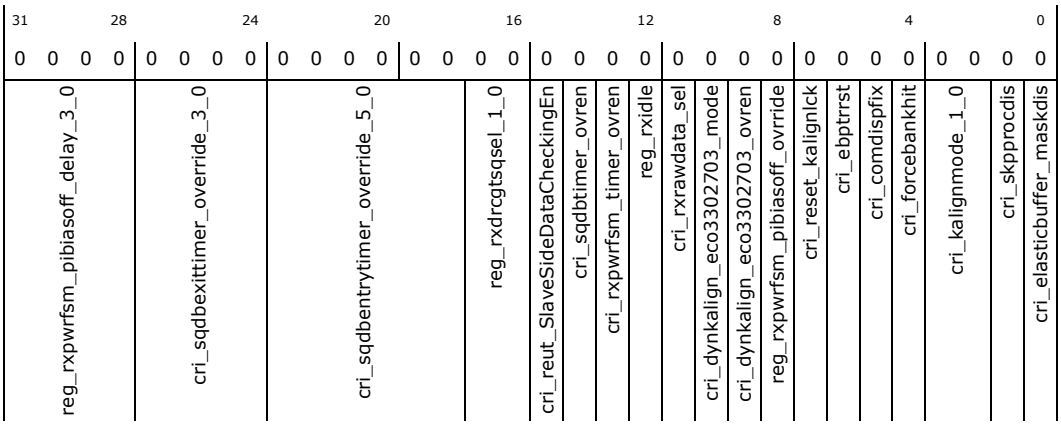
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword2: [Port: 0xA3] + (2400h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select

Bit Range	Default & Access	Description
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

13.19.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

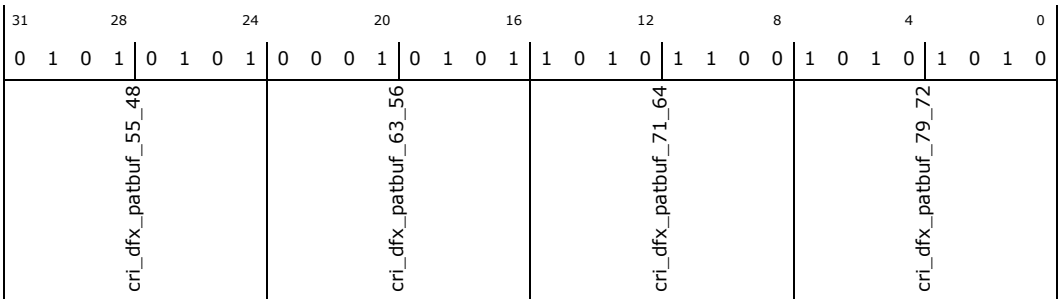
Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA3] + (2400h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 5515ACAAh



Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

13.19.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

Access Method

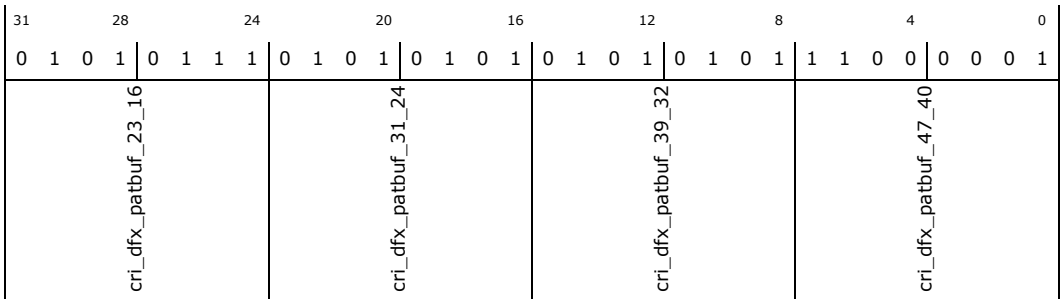
Type: Message Bus Register (Size: 32 bits)

pcs_dword4: [Port: 0xA3] + (2400h + 10h)

Op Codes:

0h - Read, 1h - Write

Default: 575555C1h



Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

13.19.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

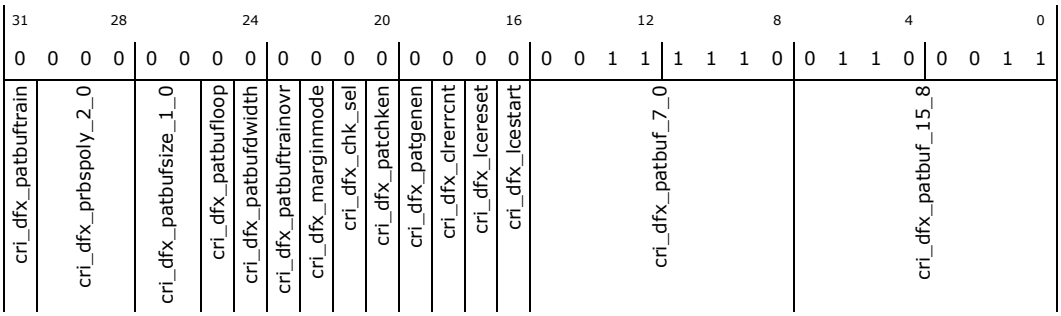
Type: Message Bus Register (Size: 32 bits)

pcs_dword5: [Port: 0xA3] + (2400h + 14h)

Op Codes:

0h - Read, 1h - Write

Default: 00003E63h



Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker

Bit Range	Default & Access	Description
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

13.19.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

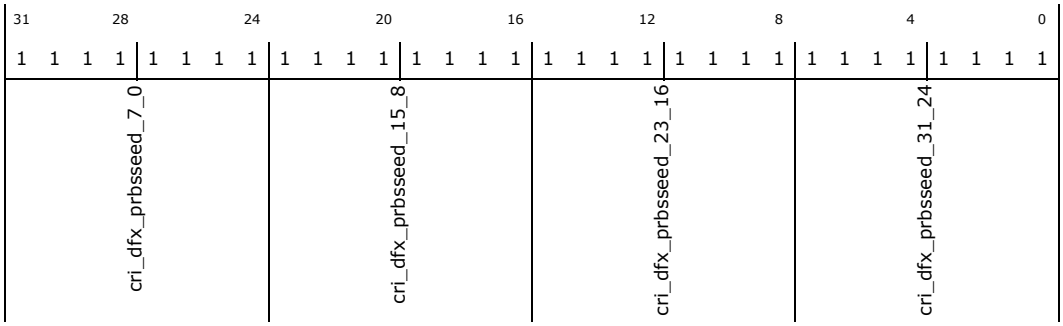
Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA3] + (2400h + 18h)

Op Codes:

0h - Read, 1h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

13.19.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

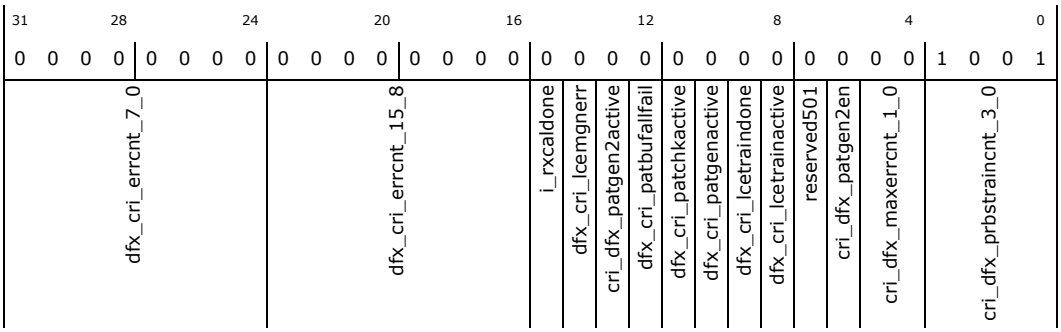
Type: Message Bus Register (Size: 32 bits)

pcs_dword7: [Port: 0xA3] + (2400h + 1Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000009h



Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator

Bit Range	Default & Access	Description
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

13.19.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

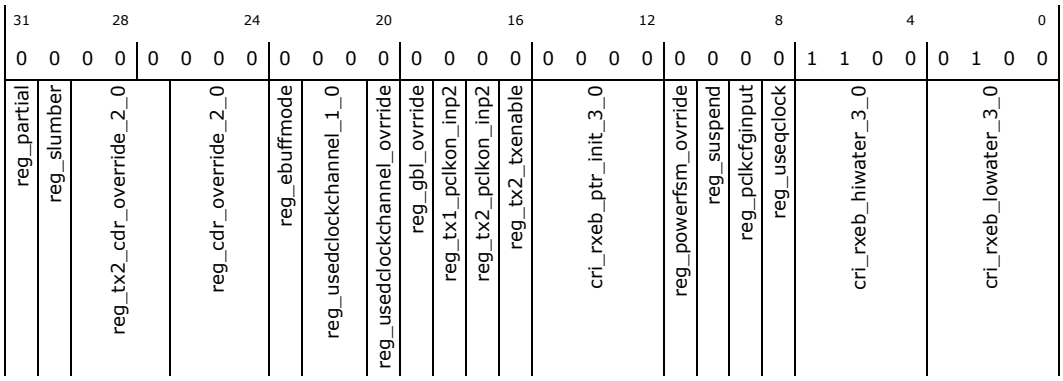
Type: Message Bus Register (Size: 32 bits)

pcs_dword8: [Port: 0xA3] + (2400h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 000000C4h



Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1

Bit Range	Default & Access	Description
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

13.19.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

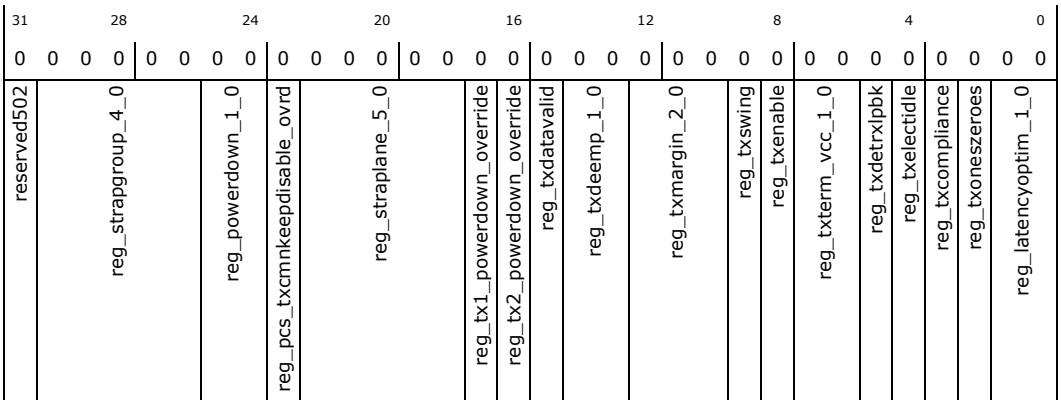
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword9: [Port: 0xA3] + (2400h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup

Bit Range	Default & Access	Description
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

13.19.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

Access Method

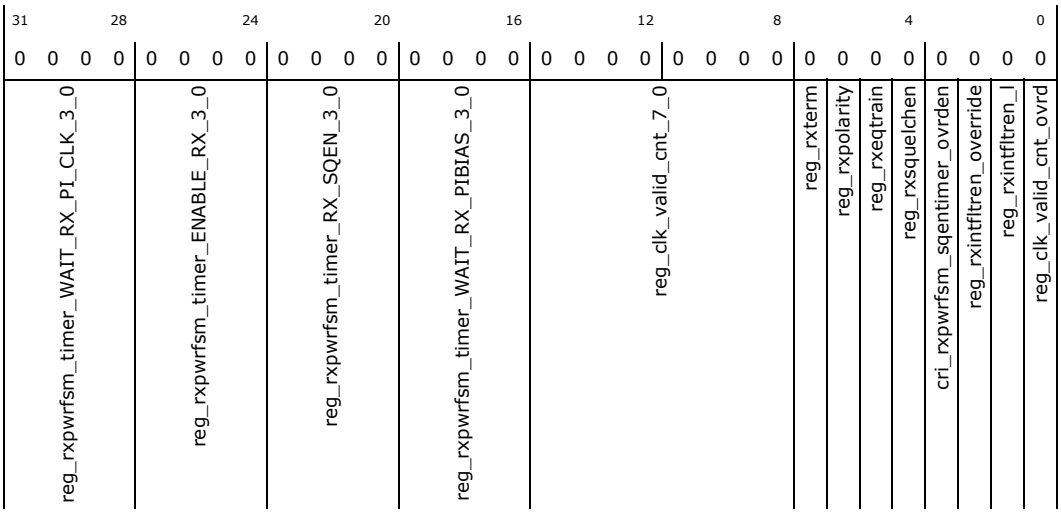
Type: Message Bus Register (Size: 32 bits)

pcs_dword10: [Port: 0xA3] + (2400h + 28h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).

Bit Range	Default & Access	Description
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

13.19.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

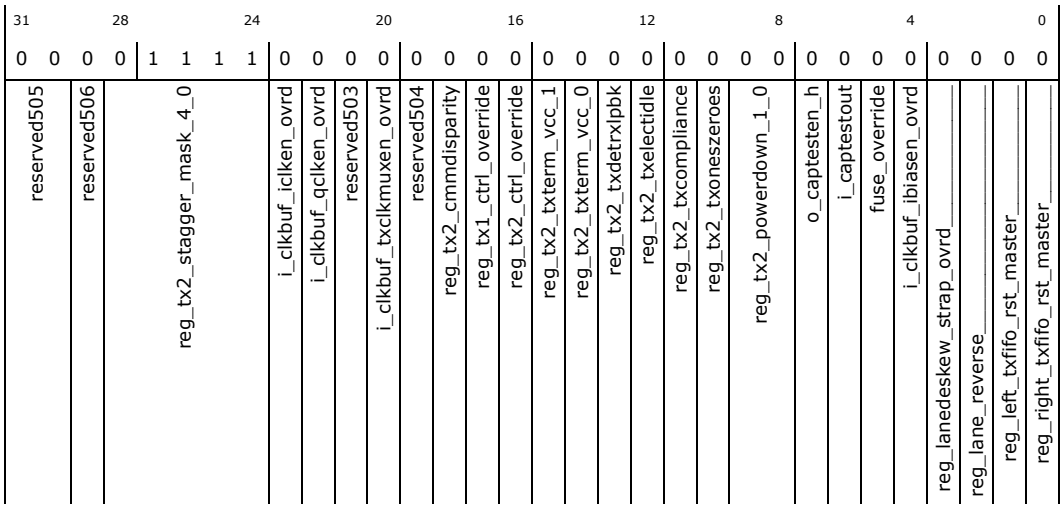
Type: Message Bus Register (Size: 32 bits)

pcs_dword11: [Port: 0xA3] + (2400h + 2Ch)

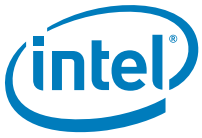
Op Codes:

0h - Read, 1h - Write

Default: 0F000000h



Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved



Bit Range	Default & Access	Description
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd_____:** reserved
2	0h RW	**reg_lane_reverse_____:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____:** reserved
0	0h RW	**reg_right_txfifo_rst_master_____:** reserved

13.19.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

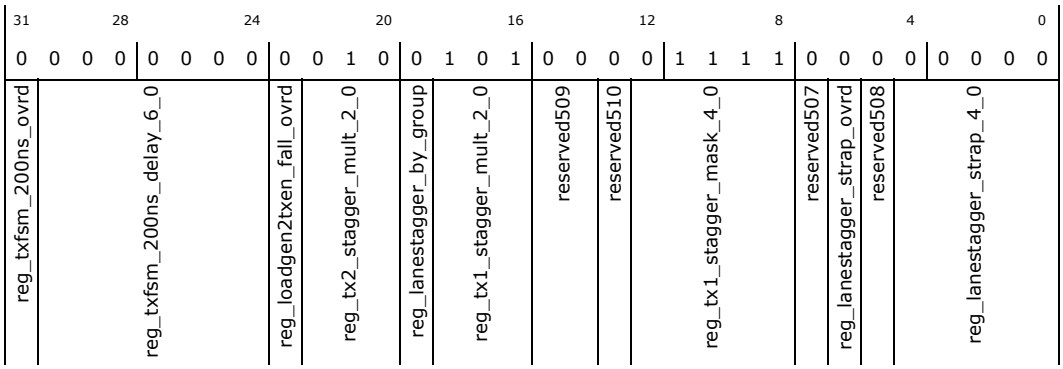
Type: Message Bus Register (Size: 32 bits)

pcs_dword12: [Port: 0xA3] + (2400h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00250F00h



Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved

Bit Range	Default & Access	Description
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

13.19.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

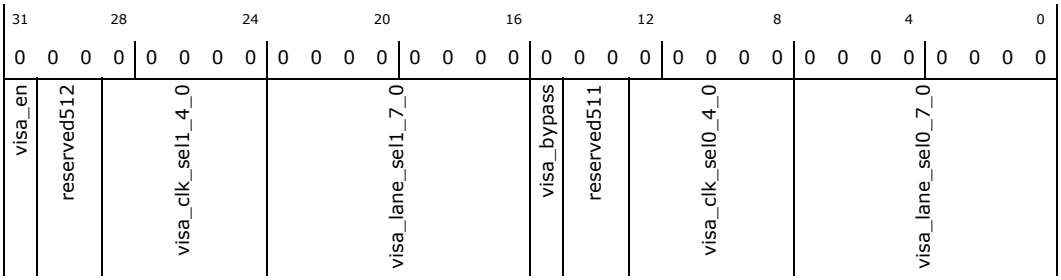
Type: Message Bus Register (Size: 32 bits)

pcs_dword13: [Port: 0xA3] + (2400h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

13.19.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

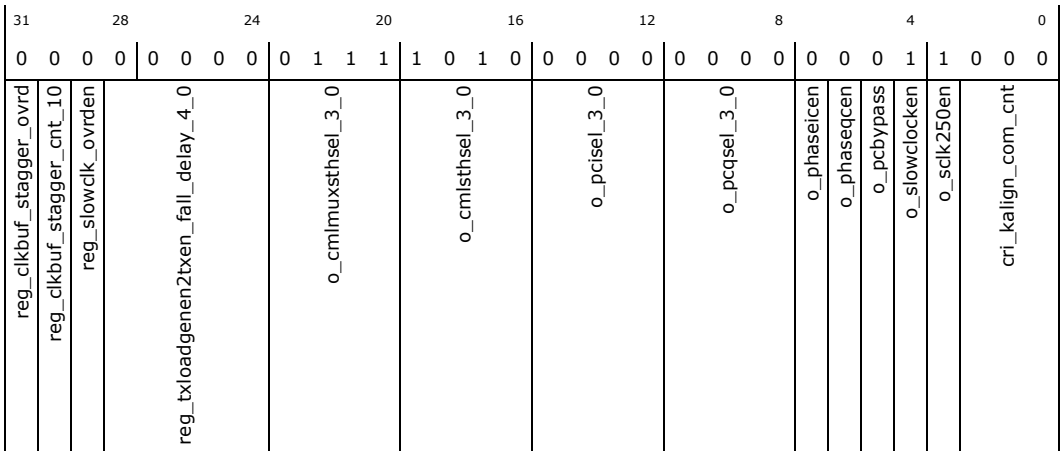
Type: Message Bus Register (Size: 32 bits)

pcs_dword14: [Port: 0xA3] + (2400h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 007A0018h



Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.

Bit Range	Default & Access	Description
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

13.19.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

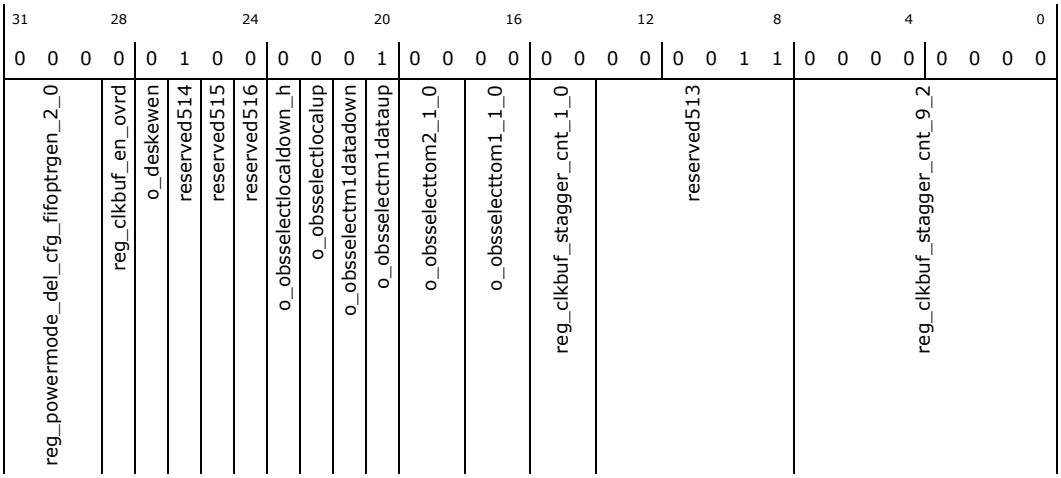
Type: Message Bus Register (Size: 32 bits)

pcs_dword15: [Port: 0xA3] + (2400h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 04100300h



Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved

Bit Range	Default & Access	Description
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

13.19.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

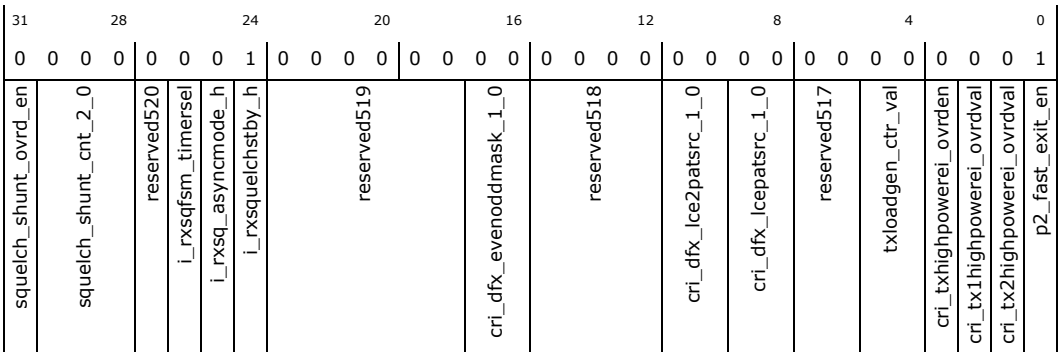
Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA3] + (2400h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved

Bit Range	Default & Access	Description
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

13.19.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

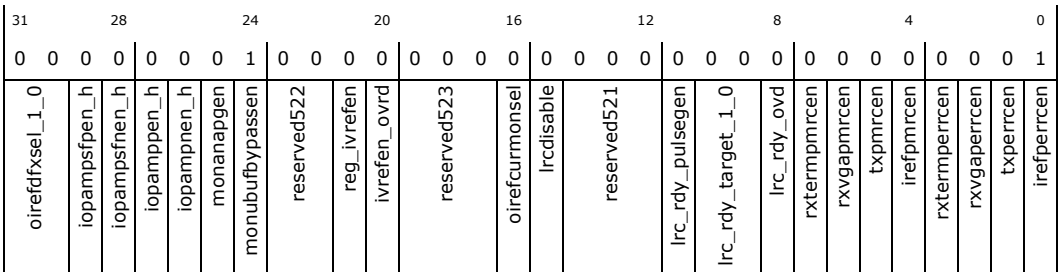
Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA3] + (2400h + 44h)

Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved

Bit Range	Default & Access	Description
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

13.19.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

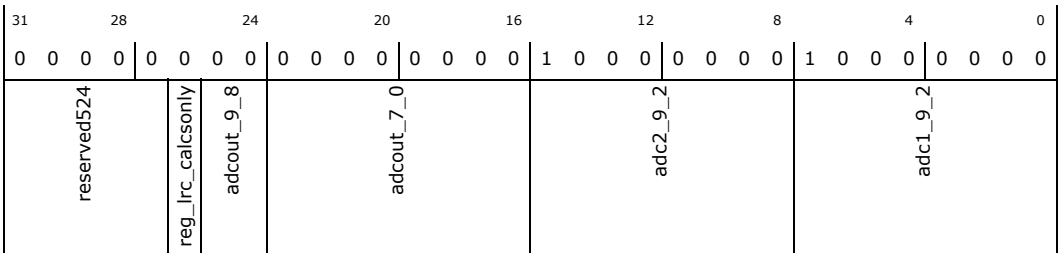
Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA3] + (2400h + 48h)

Op Codes:

0h - Read, 1h - Write

Default: 00008080h



Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimation filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimation filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

13.19.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

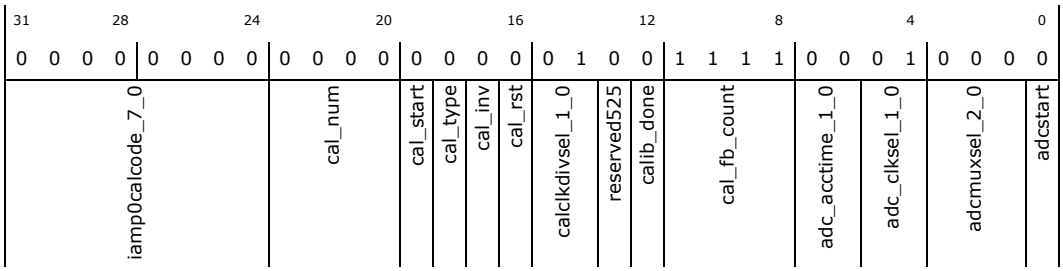
Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA3] + (2400h + 4Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00004F10h



Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [lyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.

Bit Range	Default & Access	Description
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

13.19.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

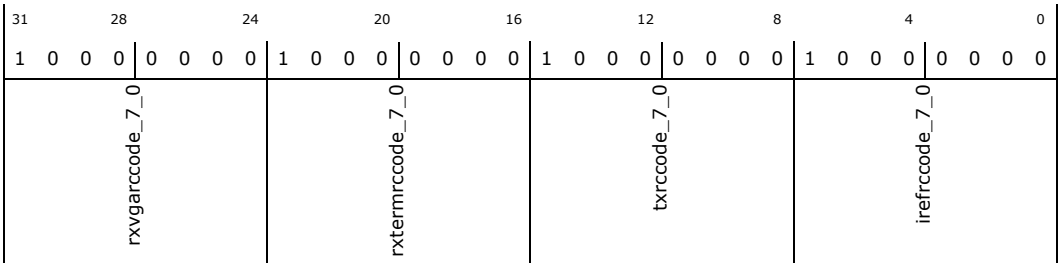
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA3] + (2400h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

13.19.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

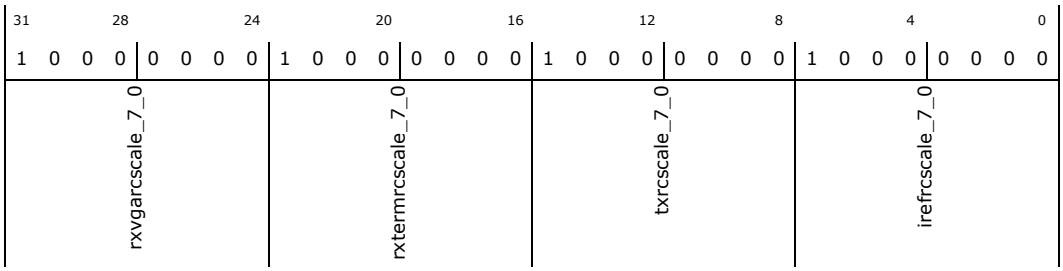
Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA3] + (2400h + 54h)

Op Codes:

0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

13.19.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

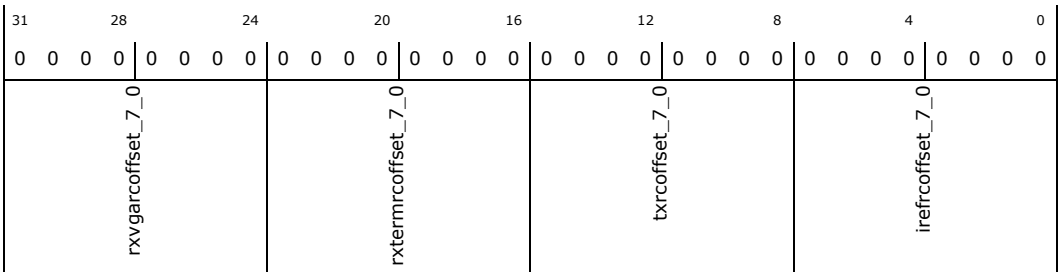
Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA3] + (2400h + 58h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

13.19.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

Access Method

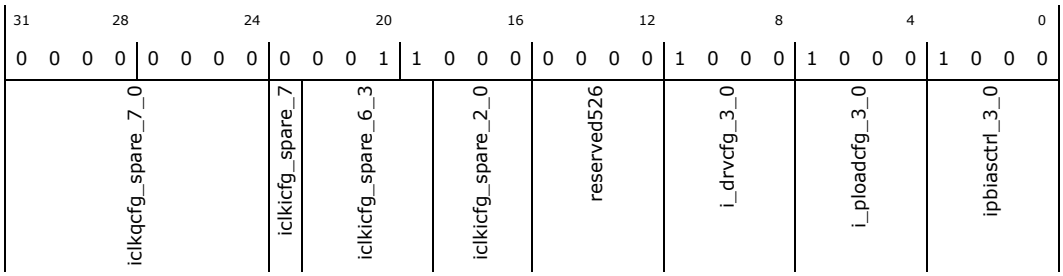
Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA3] + (2400h + 5Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00180888h



Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

13.19.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

Access Method

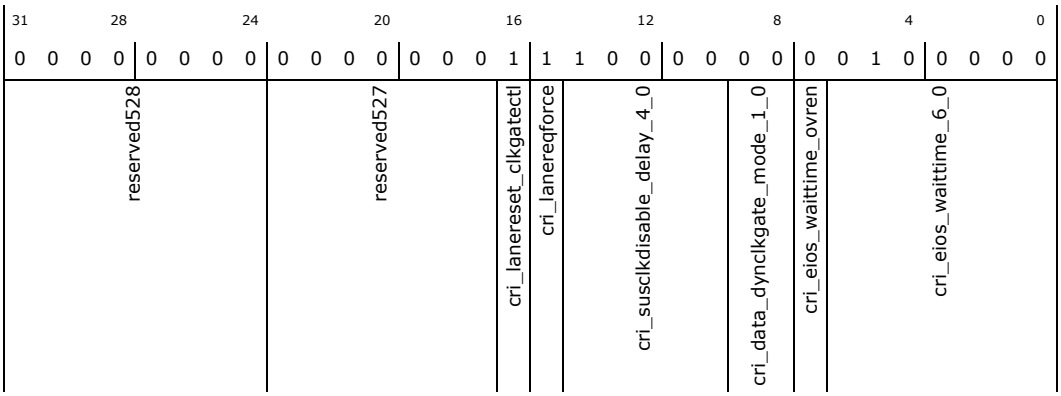
Type: Message Bus Register (Size: 32 bits)

pcs_dword24: [Port: 0xA3] + (2400h + 60h)

Op Codes:

0h - Read, 1h - Write

Default: 0001C020h



Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (that is, 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay ..... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay

Bit Range	Default & Access	Description
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

13.20 SATA Lane 1 Electrical Register Address Map

Table 115. Summary of SATA Lane 1 Electrical Message Bus Registers—0xA3 (Global Offset 2480h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 321	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 322	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 323	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 324	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 325	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 326	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 326	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 327	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 328	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 329	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 330	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 331	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 333	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 334	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 335	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 336	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 337	00008A00h

13.20.1 TX_DWORD0 (tx_dword0)—Offset 0h

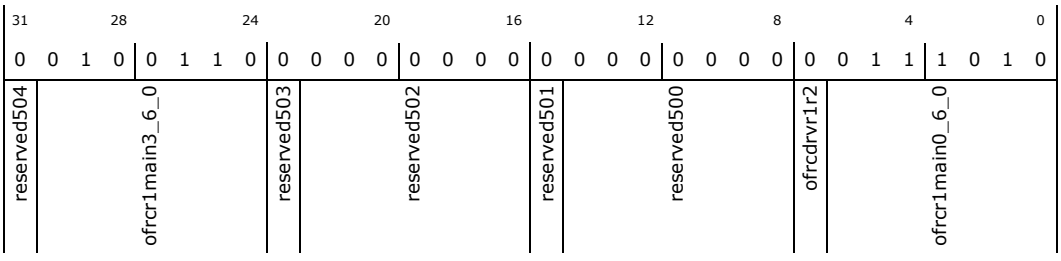
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword0: [Port: 0xA3] + (2480h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah



Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

13.20.2 TX_DWORD1 (tx_dword1)—Offset 4h

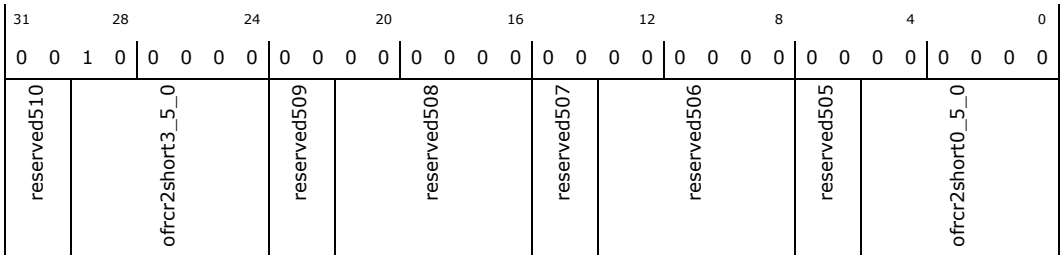
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword1: [Port: 0xA3] + (2480h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

13.20.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

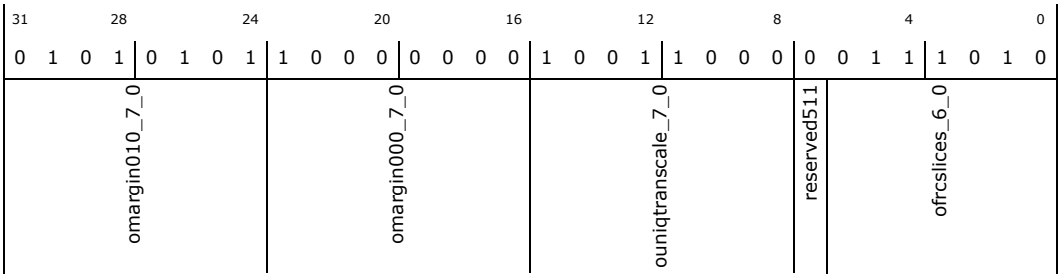
Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA3] + (2480h + 8h)

Op Codes:

0h - Read, 1h - Write

Default: 5580983Ah



Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on dataratefit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

13.20.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

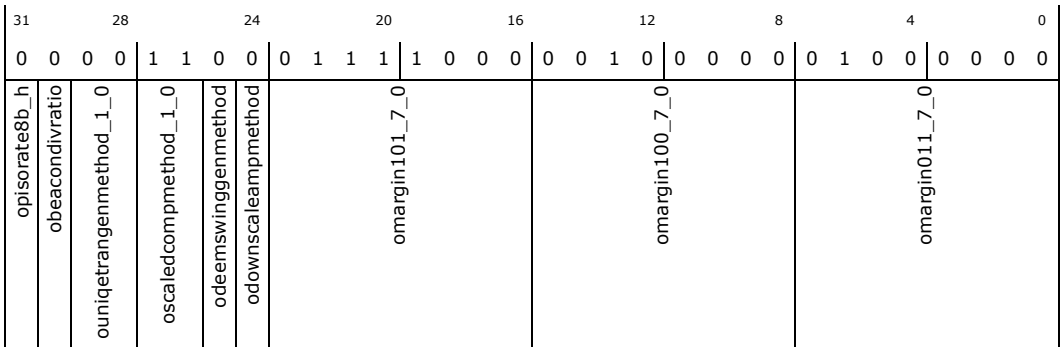
Type: Message Bus Register (Size: 32 bits)

tx_dword3: [Port: 0xA3] + (2480h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0C782040h



Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p

Bit Range	Default & Access	Description
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

13.20.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

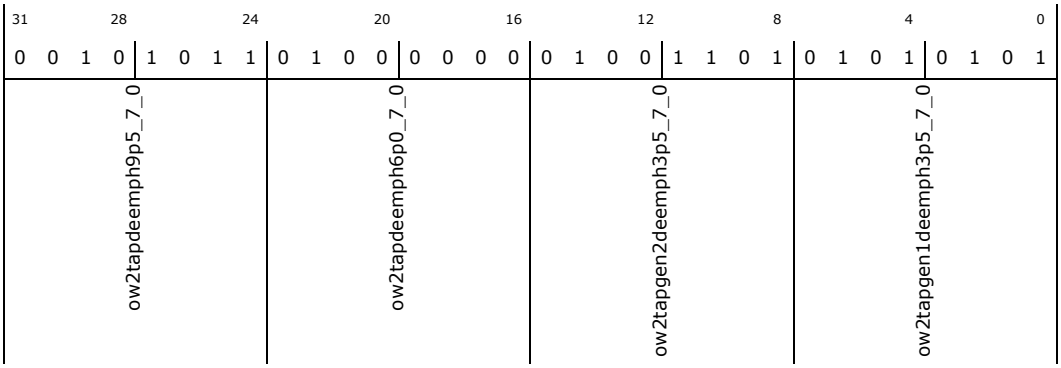
Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA3] + (2480h + 10h)

Op Codes:

0h - Read, 1h - Write

Default: 2B404D55h



Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

13.20.6 TX_DWORD5 (tx_dword5)—Offset 14h

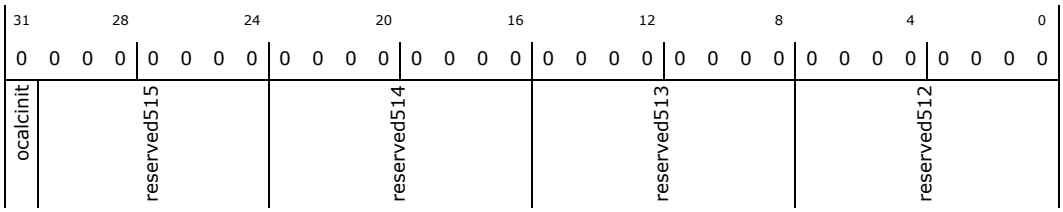
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA3] + (2480h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

13.20.7 TX_DWORD6 (tx_dword6)—Offset 18h

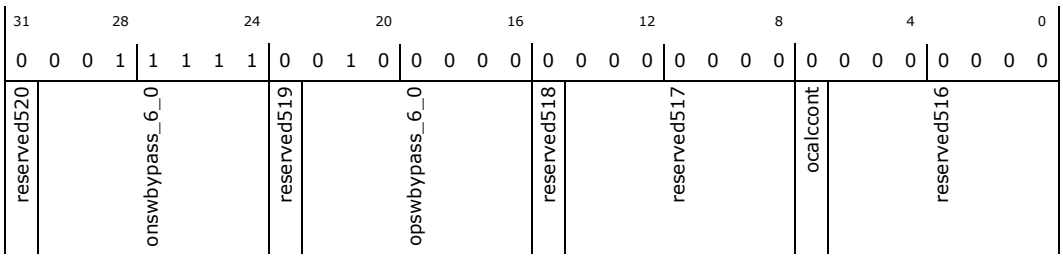
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword6: [Port: 0xA3] + (2480h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h



Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved

Bit Range	Default & Access	Description
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively
6:0	0h RO	**reserved516:** reserved

13.20.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

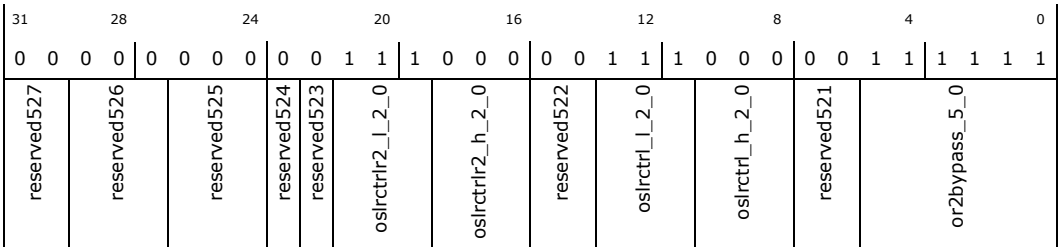
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword7: [Port: 0xA3] + (2480h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh



Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved

Bit Range	Default & Access	Description
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

13.20.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

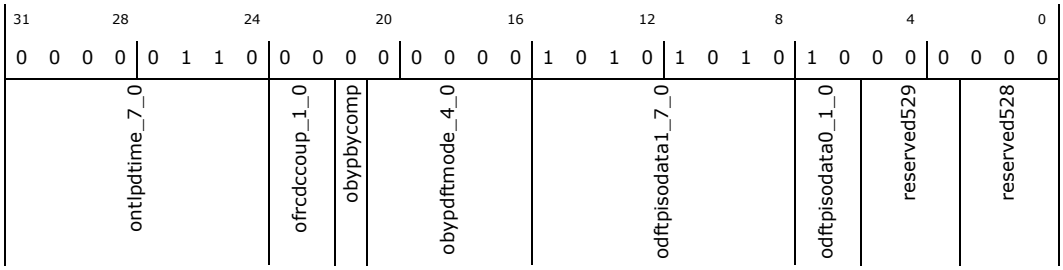
Type: Message Bus Register (Size: 32 bits)

tx_dword8: [Port: 0xA3] + (2480h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 0600AA80h



Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG

Bit Range	Default & Access	Description
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

13.20.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

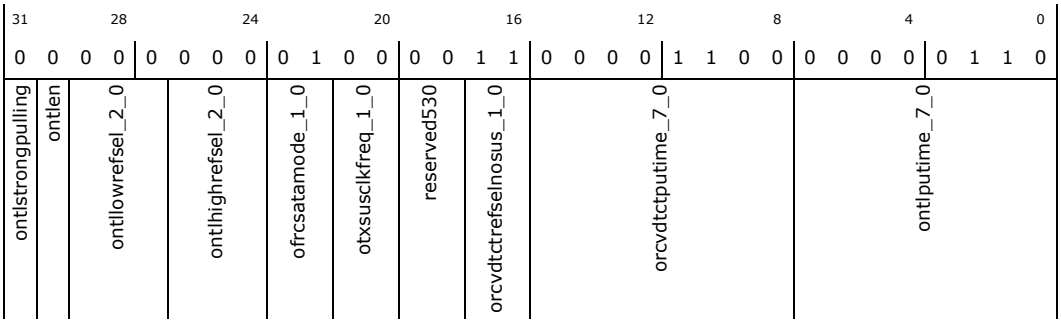
Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA3] + (2480h + 24h)

Op Codes:

0h - Read, 1h - Write

Default: 00430C06h



Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active

Bit Range	Default & Access	Description
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

13.20.11 TX_DWORD10 (tx_dword10)—Offset 28h

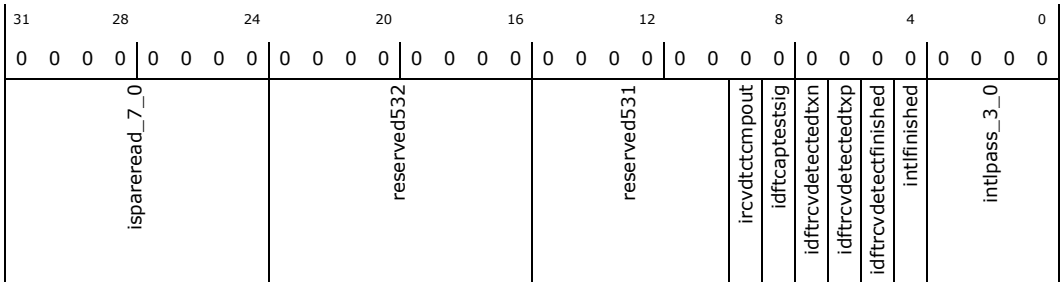
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword10: [Port: 0xA3] + (2480h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

13.20.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

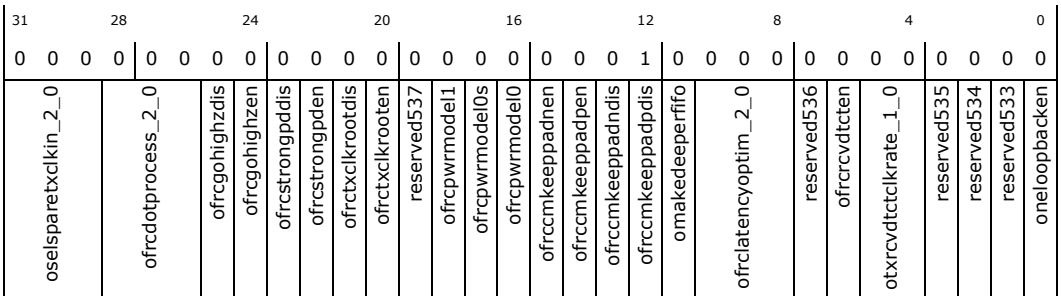
Type: Message Bus Register (Size: 32 bits)

tx_dword11: [Port: 0xA3] + (2480h + 2Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00001000h



Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN

Bit Range	Default & Access	Description
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

13.20.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

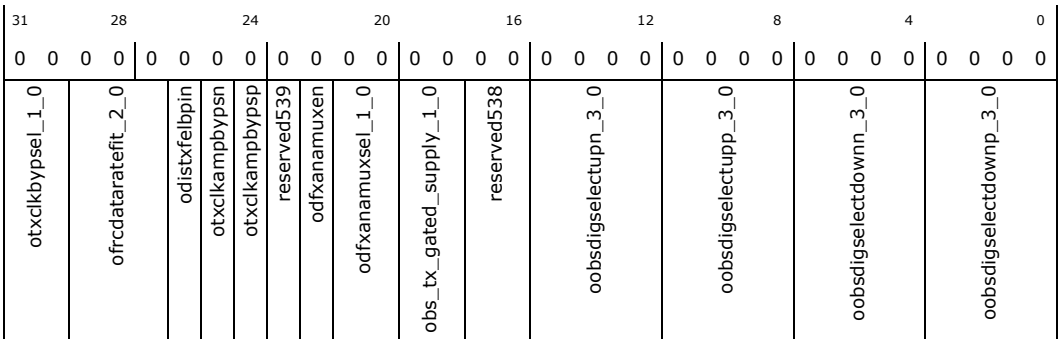
Type: Message Bus Register (Size: 32 bits)

tx_dword12: [Port: 0xA3] + (2480h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - datarateﬁt must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - datarateﬁt must be '11'
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]

Bit Range	Default & Access	Description
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

13.20.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

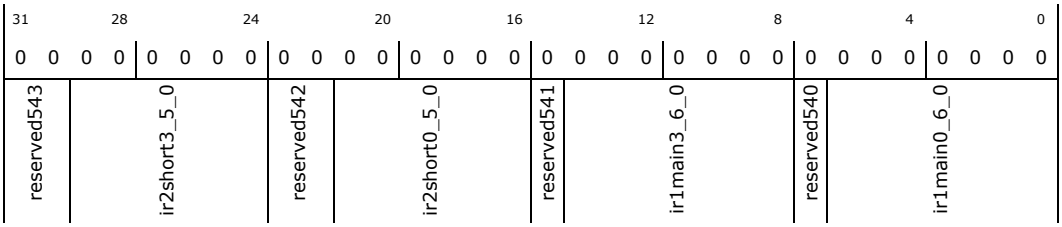
Type: Message Bus Register (Size: 32 bits)

tx_dword13: [Port: 0xA3] + (2480h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

13.20.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

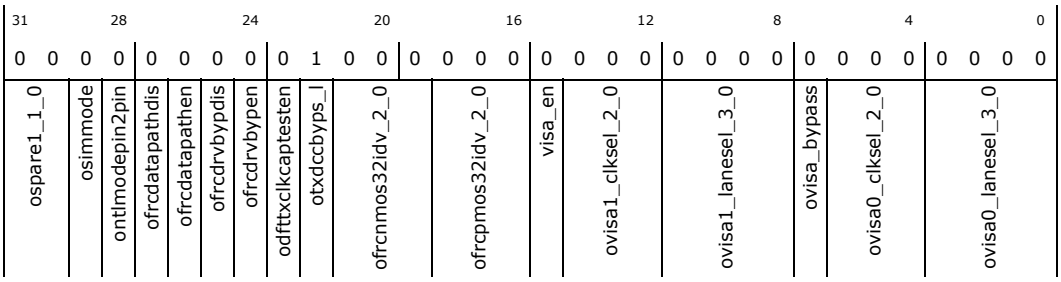
Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA3] + (2480h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 00400000h



Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.

Bit Range	Default & Access	Description
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

13.20.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

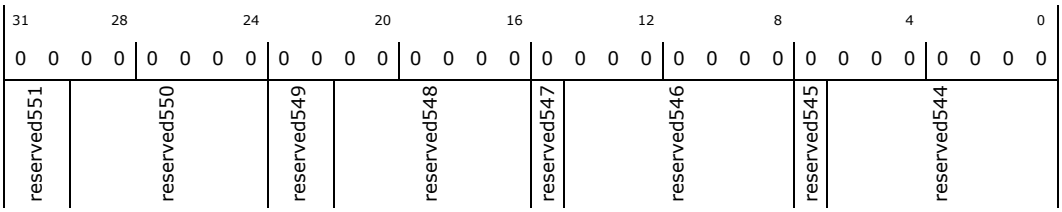
Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA3] + (2480h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

13.20.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

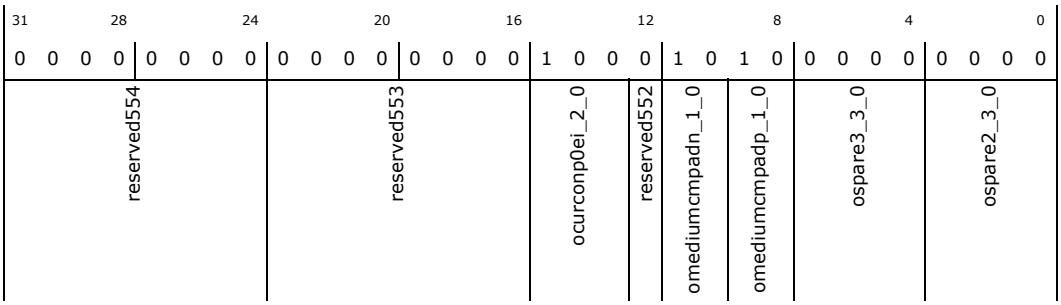
Type: Message Bus Register (Size: 32 bits)

tx_dword16: [Port: 0xA3] + (2480h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 00008A00h



Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

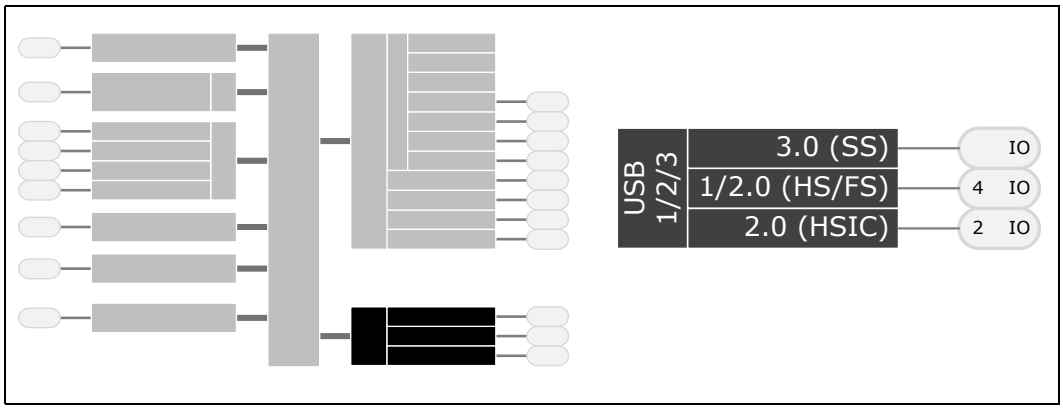
14 USB Host Controller Interfaces (xHCI, EHCI)

The USB Host Controllers (xHCI, EHCI) supports:

- One (1) Super Speed (SS) port on xHCI
- Four (4) Full Speed (FS)/High Speed (HS) ports on xHCI or EHCI
- Two (2) High Speed (HS) High Speed Inter-Chip (HSIC) ports on xHCI

Note: The SS port must share a FS/HS port to have a full SS connector leaving three FS/HS ports available.

Note: Only one host controller (xHCI or ECHI) can be used. To enable HSIC and SS ports, xHCI must be used.



14.1 Signal Descriptions

Please see Chapter 2, “Physical Interfaces” for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, “Electrical Specifications”
- **Description**: A brief explanation of the signal’s function

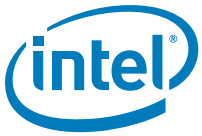


Table 116. USB 3 SS Signals

Signal Name	Direction/ Type	Description
USB3_TXP/N[0]	O USB3	**Data Out:** High speed serialized data outputs. Used for debug mode in xHCI operation.
USB3_RXP/N[0]	I USB3	**Data In:** High speed serialized data inputs. Used for debug mode in xHCI operation.
USB3_REXT[0]	I Analog	**Resistor Compensation:** An external resistor must be connected between this pin and package ground.

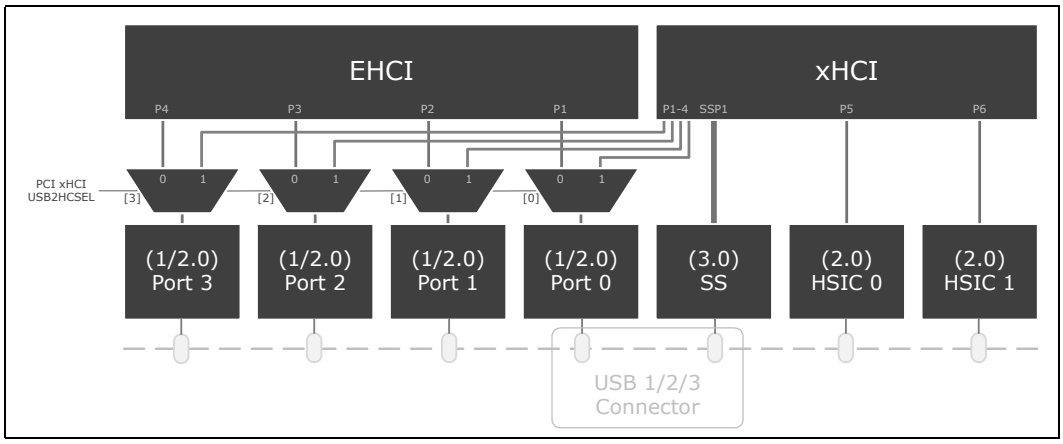
Table 117. USB 2 FS/HS Signals

Signal Name	Direction/ Type	Description
USB_DP/N[0:3]	I/O USB2	**USB Data:** High speed serialized data I/O. **Note:** USB_DP/N[1] used for debug mode in EHCI operation only. SS port must be implemented to have debug mode during xHCI operation.
USB_OC[0:1]#	I USB2	**Over-Current Protection:** Over-current notification for all USB ports (SS/FS/HS).
USB_RCOMPI	I Analog	**Resistor Compensation:** An external resistor must be connected.
USB_RCOMPO	O Analog	**Resistor Compensation:** An external resistor must be connected.

Table 118. USB 2 HSIC Signals

Signal Name	Direction/ Type	Description
USB_HSIC[0:1]_DATA	I/O USB3	**HSIC Data:** High speed serialized data.
USB_HSIC[0:1]_STROBE	I/O USB3	**HSIC Strobe:** Strobe reference for data.
USB_HSIC_RCOMP	I Analog	**Resistor Compensation:** An external resistor must be connected.

Figure 18. xHCI and EHCI Port Mapping



NOTE: xHCI (3.0) SS is the debug port for xHCI controller.
NOTE: EHCI (1/2.0) Port 1 is the debug port of the EHCI controller

14.2 USB 3.0 xHCI (Extensible Host Controller Interface)

The xHCI compliant host controller can control up to 7 USB host ports. It supports devices conforming to USB 1.x to 3.0 at bit rates up to 5 Gbps.

14.2.1 Features of USB 3.0 Host

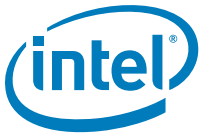
The USB 3.0 Super Speed data interface is a four wire differential (TX and RX pairs) interface that supports simultaneous bi-directional data transmission. The interface supports a bit rate of 5 Gbps with a maximum theoretical data throughput over 3.2 Gbps due to 8b/10b symbol encoding scheme and protocol overhead (link flow control, packet framing and protocol overhead).

Low Frequency Periodic signaling (LFPS) is used to communicate initialization, training and power management information across a link that is in low power link state without using Super Speed signaling. This reduces power consumption.

The USB3.0 port may be paired with any USB2 port at the connector – selection of any USB2 port other than port 0 will require the appropriate mapping.Figure 18 shows the USB3 port paired with USB2 port.

USB3.0 Controller Features

- Supported by xHCI software host controller interface
- USB3 port disable
- Supports local dynamic clock gating and trunk clock gating
- Supports USB 3.0 LPM (U0, U1, U2, and U3) and also a SS Disabled low power state
- Support for USB3 Debug Device



Note: Recommended not to disconnect the connection when a debug session is in progress.

14.2.2 Features of USB HSIC

HSIC is a 2-signal (strobe and data) source synchronous serial interface for on board inter-chip USB communication. The interface uses 240 MHz DDR signaling to provide High-Speed 480 Mb/s USB transfers which are 100% host driver compatible with traditional USB cable connected topologies. Full Speed (FS) and Low Speed (LS) USB transfers are not directly supported by the HSIC interface.

For details of HSIC applications supported, please contact local Intel Sales office.

Major feature and performance highlights are as follows:

- Supported by xHCI software host controller interface
- High-Speed 480 Mb/s data rate only
- Source-synchronous serial interface
- Interface Power is only consumed when a transfer is in progress
- No hot plug removal/attach at HSIC pins
- Signals driven at 1.2V standard LVCMOS levels
- Designed for low power applications
- Support for two host ports compliant to High Speed Inter-Chip Supplement (HSIC) to the USB 2.0 Specification. (USB 2.0)

14.3 USB 2.0 Enhanced Host Controller Interface (EHCI)

The EHCI compliant host controller supports up to 4 USB 2.0 ports in legacy mode. USB 2.0 allows data transfers up to 480 Mbps. The controller integrates a Root Matching Hub (RMH) to support USB 1.1 devices.

Note: The EHCI is not used when the xHCI is used. The EHCI is primarily present for legacy usage, in cases when xHCI support is not available.

Note: Intel recommends using the xHCI controller for the USB2.0 ports irrespective of whether USB3.0 ports are implemented. The EHCI controller is provided for legacy OS/ driver compatibility which is generally not required for tablet platforms. Using the xHCI controller will deliver significant power and performance benefits.

When following this recommendation on a platform with no USB3.0 support, the Windows logo requirement of USB debug port may not be met. Please consult with Intel regarding the impact of this.

Note: Unlike the xHCI, bandwidth of all four ports on the EHCI is shared across a single HS (480 Mbps) internal link.

14.3.1 Features of EHCI USB 2.0 Controller

The EHCI USB2.0 Controller supports the following features:

- Compliant with the specification for: USB 1.x, 2.0 (1.5 Mbps, 12 Mbps, 480 Mbps).
- 4 Ports shared with xHCI controller
- Enhanced EHCI descriptor caching
- All ports provided through USB Rate Matching Hubs (RMH) to support FS/LS devices
- Supports one Debug port at USB2 transfer rates
- Supports of USB suspend mode including PLL turn off in S0.
- Supports wakeup from suspend states S3-S5 and remote-suspend wakeup
- All USB2 ports provide support for HS/FS/LS devices
- Per port USB disable
- Supports local dynamic clock gating and trunk clock gating
- Supports USB 2.0 LPM (L0, L1 and L2 low power states)

14.4 References

USB 3.0 Specification

USB 2.0 Specification (Includes High-Speed Inter-Chip USB Electrical Specification)

14.4.1 Host Controller Specifications

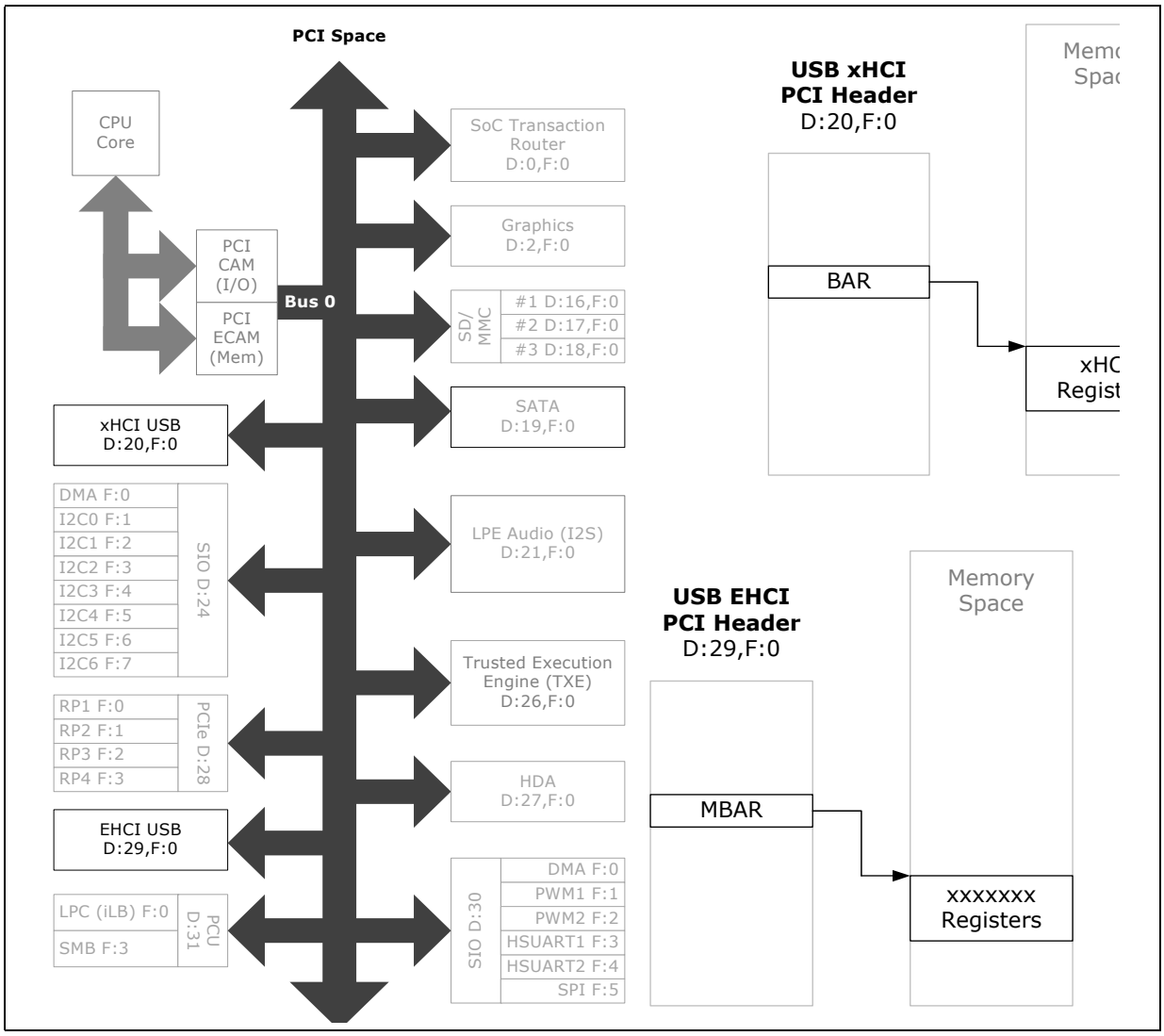
Extensible Host Controller Interface (xHCI) Specification for USB 3.0 version 1.0

Enhanced Host Controller Interface (EHCI) Specification for USB 2.0

14.5 Register Map

Refer to Chapter 3, "Register Access Methods" and Chapter 4, "Mapping Address Spaces" for additional information.

Figure 19. USB Host Controller Register Map



14.6 USB xHCI PCI Configuration Registers

Table 119. Summary of USB xHCI PCI Configuration Registers—0/20/0

Offset	Size	Register ID—Description	Default Value
0h	2	"Vendor ID (VID)—Offset 0h" on page 345	8086h
2h	2	"Device ID (DID)—Offset 2h" on page 346	8C31h
4h	2	"Command (CMD)—Offset 4h" on page 346	0000h
6h	2	"Device Status (STS)—Offset 6h" on page 347	0290h
8h	1	"Revision ID (RID)—Offset 8h" on page 348	00h
9h	1	"Programming Interface (PI)—Offset 9h" on page 349	30h
Ah	1	"Sub Class Code (SCC)—Offset Ah" on page 349	03h
Bh	1	"Base Class Code (BCC)—Offset Bh" on page 350	0Ch
Dh	1	"Master Latency Timer (MLT)—Offset Dh" on page 350	00h
Eh	1	"Header Type (HT)—Offset Eh" on page 351	00h
10h	8	"Memory Base Address (MBAR)—Offset 10h" on page 351	0000000000000004h
2Ch	2	"USB Subsystem Vendor ID (SSVID)—Offset 2Ch" on page 352	0000h
2Eh	2	"USB Subsystem ID (SSID)—Offset 2Eh" on page 352	0000h
34h	1	"Capabilities Pointer (CAP_PTR)—Offset 34h" on page 353	70h
3Ch	1	"Interrupt Line (ILINE)—Offset 3Ch" on page 353	00h
3Dh	1	"Interrupt Pin (IPIN)—Offset 3Dh" on page 354	00h
40h	4	"XHC System Bus Configuration 1 (XHCC1)—Offset 40h" on page 354	000000FDh
44h	4	"XHC System Bus Configuration 2 (XHCC2)—Offset 44h" on page 356	0003C000h
50h	4	"Clock Gating (XHCLKGTEN)—Offset 50h" on page 357	00000120h
58h	4	"Audio Time Synchronization (AUDSYNC)—Offset 58h" on page 359	00000000h
60h	1	"Serial Bus Release Number (SBRN)—Offset 60h" on page 360	30h
61h	1	"Frame Length Adjustment (FLADJ)—Offset 61h" on page 360	20h
62h	1	"Best Effort Service Latency (BESL)—Offset 62h" on page 361	00h
70h	1	"PCI Power Management Capability ID (PM_CID)—Offset 70h" on page 362	01h
71h	1	"Next Item Pointer #1 (PM_NEXT)—Offset 71h" on page 362	80h
72h	2	"Power Management Capabilities (PM_CAP)—Offset 72h" on page 363	C1C2h
74h	2	"Power Management Control/Status (PM_CS)—Offset 74h" on page 364	0008h
80h	1	"Message Signaled Interrupt CID (MSI_CID)—Offset 80h" on page 365	05h
81h	1	"Next item pointer (MSI_NEXT)—Offset 81h" on page 365	00h
82h	2	"Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h" on page 366	0086h
84h	4	"Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h" on page 366	00000000h
88h	4	"Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h" on page 367	00000000h
8Ch	2	"Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch" on page 367	0000h
A4h	4	"High Speed Configuration 2 (HSCFG2)—Offset A4h" on page 368	00002000h

Table 119. Summary of USB xHCI PCI Configuration Registers—0/20/0 (Continued)

Offset	Size	Register ID—Description	Default Value
B0h	4	"Super Speed Configuration 1 (SSCFG1)—Offset B0h" on page 369	0000008Fh
C0h	4	"XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1)—Offset C0h" on page 371	00000000h
C4h	4	"XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2)—Offset C4h" on page 371	00000000h
C8h	4	"XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1)—Offset C8h" on page 372	00000000h
CCh	4	"XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2)—Offset CCh" on page 373	00000000h
D0h	4	"USB2 Port Routing (USB2PR)—Offset D0h" on page 374	00000000h
D4h	4	"USB2 Port Routing Mask (USB2PRM)—Offset D4h" on page 374	00000000h
D8h	4	"USB3 Port Routing (USB3PR)—Offset D8h" on page 375	00000000h
DCh	4	"USB3 Port Routing Mask (USB3PRM)—Offset DCh" on page 376	00000000h
E0h	4	"Fuse and Strap (FUS)—Offset E0h" on page 377	00000000h
E4h	4	"USB2 Port Disable Override (USB2PDO)—Offset E4h" on page 378	00000000h
E8h	4	"USB3 Port Disable Override (USB3PDO)—Offset E8h" on page 378	00000000h
ECh	4	"USB2 FS/LS Port Staggering Control (FSLSPS)—Offset ECh" on page 379	0000D8D8h

14.6.1 Vendor ID (VID)—Offset 0h

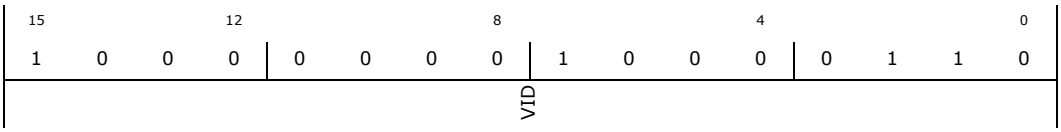
Access Method

Type: PCI Configuration Register (Size: 16 bits)

VID: [B:0, D:20, F:0] + 0h

Power Well: Core

Default: 8086h



Bit Range	Default & Access	Description
15:0	8086h RO	**Vendor ID (VID):** Reserved.

14.6.2 Device ID (DID)—Offset 2h

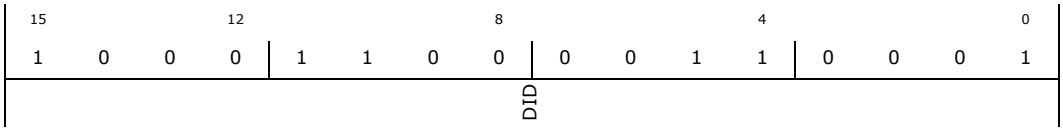
Access Method

Type: PCI Configuration Register (Size: 16 bits)

DID: [B:0, D:20, F:0] + 2h

Power Well: Core

Default: 8C31h



Bit Range	Default & Access	Description
15:0	8C31h RO/V	**Device ID (DID):** See Global Device ID table in Chap. 6 for value

14.6.3 Command (CMD)—Offset 4h

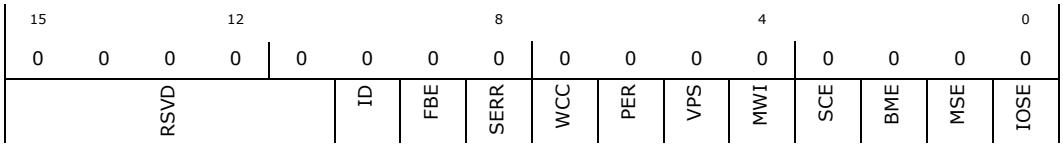
Access Method

Type: PCI Configuration Register (Size: 16 bits)

CMD: [B:0, D:20, F:0] + 4h

Power Well: Core

Default: 0000h



Bit Range	Default & Access	Description
15:11	00h RO	**Reserved (RSVD):** Reserved.
10	0b RW	**Interrupt Disable (ID):** When cleared to 0, the function is capable of generating interrupts. When 1, the function can not generate its interrupt to the interrupt controller. Note that the corresponding Interrupt Status bit is not affected by the interrupt enable.
9	0b RO	**Fast Back to Back Enable (FBE):** Reserved.
8	0b RW	**SERR# Enable (SERR):** When set to 1, the XHC is capable of generating (internally) SERR#. See section on error handling.
7	0b RO	**Wait Cycle Control (WCC):** Reserved.
6	0b RW	**Parity Error Response (PER):** When set to 1, the XHCI Host Controller will check for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase as recommended by the XHCI specification. Note that this applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	0b RO	**VGA Palette Snoop (VPS):** Reserved.

Bit Range	Default & Access	Description
4	0b RO	**Memory Write Invalidate (MWI):** Reserved.
3	0b RO	**Special Cycle Enable (SCE):** Reserved.
2	0b RW	**Bus Master Enable (BME):** When set, it allows XHC to act as a bus master. When cleared, it disable XHC from initiating transactions on the system bus.
1	0b RW	**Memory Space Enable (MSE):** This bit controls access to the XHC Memory Space registers. If this bit is set, accesses to the XHC registers are enabled. The Base Address register for the XHC should be programmed before this bit is set.
0	0b RO	**I/O Space Enable (IOSE):** Reserved as 0. Read-Only.

14.6.4 Device Status (STS)—Offset 6h

Access Method

Type: PCI Configuration Register (Size: 16 bits)

STS: [B:0, D:20, F:0] + 6h

Power Well: Core

Default: 0290h

15			12				8				4				0
0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		MDPED	FBBC	UDF	MC	CL	IS	RSVD		

Bit Range	Default & Access	Description
15	0b RW/1C	**Detected Parity Error (DPE):** This bit is set by the Intel PCH whenever a parity error is seen on the internal interface to the XHC host controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions. Software clears this bit by writing a 1 to this bit location.
14	0b RW/1C	**Signaled System Error (SSE):** This bit is set by the Intel PCH whenever it signals SERR# (internally). The SERR_EN bit (bit 8 in the Command Register) must be 1 for this bit to be set. See error handling section for complete list of conditions handled. Software clears this bit by writing a 1 to this bit location.
13	0b RW/1C	**Received Master-Abort Status (RMA):** This bit is set when XHC, as a master, receives a master-abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
12	0b RW/1C	**Received Target Abort Status (RTA):** This bit is set when XHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. Software clears this bit by writing a 1 to this bit location.
11	0b RW/1C	**Signaled Target-Abort Status (STA):** This bit is used to indicate when the XHC function responds to a cycle with a target abort.
10:9	01b RO	**DEVSEL# Timing Status (DEVT):** This 2-bit field defines the timing for DEVSEL# assertion. Read-Only.
8	0b RW/1C	**Master Data Parity Error Detected (MDPED):** This bit is set by the Intel PCH whenever a data parity error is detected on a XHC read completion packet on the internal interface to the XHC host controller and bit 6 of the Command register is set to 1. Software clears this bit by writing a 1 to this bit location.

Bit Range	Default & Access	Description
7	1b RO	**Fast Back-to-Back Capable (FBBC):** Reserved as 1 Read-Only.
6	0b RO	**User Definable Features (UDF):** Reserved as 0. Read-Only.
5	0b RO	**66 MHz Capable (MC):** Reserved as 0. Read-Only.
4	1b RO	**Capabilities List (CL):** Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	0b RO/V	**Interrupt Status (IS):** This read-only bit reflects the state of this function's interrupt at the input of the enable/disable logic. This bit is a 1 when the interrupt is asserted. This bit will be 0 when the interrupt is deasserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	000b RO	**Reserved (RSVD):** Reserved.

14.6.5 Revision ID (RID)—Offset 8h

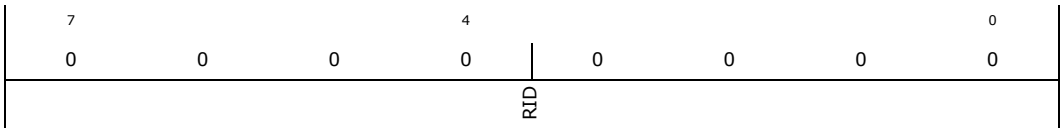
Access Method

Type: PCI Configuration Register (Size: 8 bits)

RID: [B:0, D:20, F:0] + 8h

Power Well: Core

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO/V	**Revision ID (RID):** See Chap 6 for value.

14.6.6 Programming Interface (PI)—Offset 9h

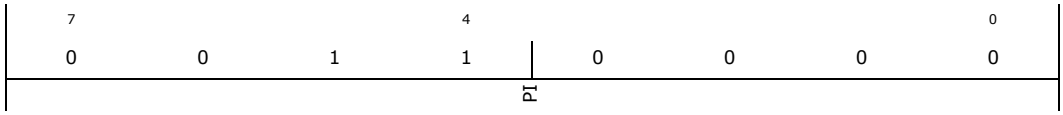
Access Method

Type: PCI Configuration Register (Size: 8 bits)

PI: [B:0, D:20, F:0] + 9h

Power Well: Core

Default: 30h



Bit Range	Default & Access	Description
7:0	30h RO	**Programming Interface (PI):** A value of 30h indicates that this USB Host Controller conforms to the XHCI specification.

14.6.7 Sub Class Code (SCC)—Offset Ah

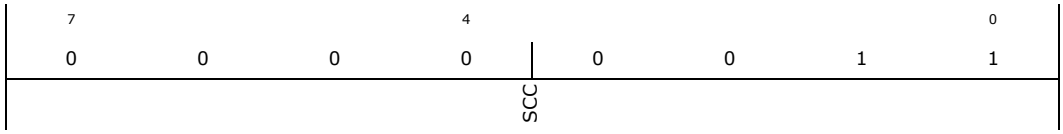
Access Method

Type: PCI Configuration Register (Size: 8 bits)

SCC: [B:0, D:20, F:0] + Ah

Power Well: Core

Default: 03h



Bit Range	Default & Access	Description
7:0	03h RO	**Sub Class Code (SCC):** A value of 03h indicates that this is a Universal Serial Bus Host Controller.

14.6.8 Base Class Code (BCC)—Offset Bh

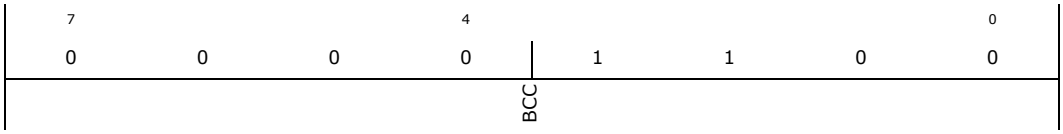
Access Method

Type: PCI Configuration Register (Size: 8 bits)

BCC: [B:0, D:20, F:0] + Bh

Power Well: Core

Default: 0Ch



Bit Range	Default & Access	Description
7:0	0Ch RO	**Base Class Code (BCC):** A value of 0Ch indicates that this is a Serial Bus controller.

14.6.9 Master Latency Timer (MLT)—Offset Dh

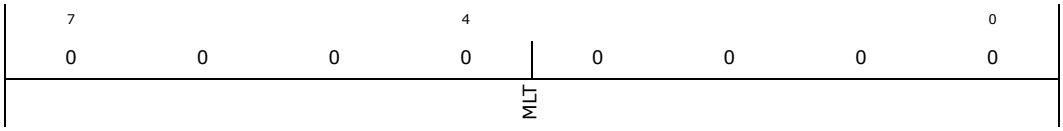
Access Method

Type: PCI Configuration Register (Size: 8 bits)

MLT: [B:0, D:20, F:0] + Dh

Power Well: Core

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**Master Latency Timer (MLT):** Because the XHC controller is internally implemented with arbitration on an internal interface, it does not need a master latency timer. The bits will be fixed at 0.

14.6.10 Header Type (HT)—Offset Eh

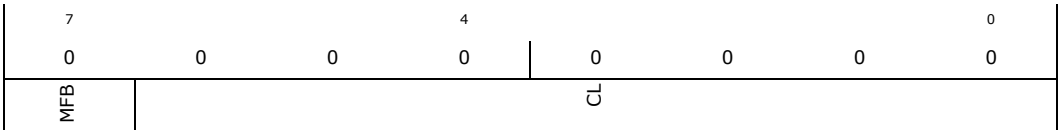
Access Method

Type: PCI Configuration Register (Size: 8 bits)

HT: [B:0, D:20, F:0] + Eh

Power Well: Core

Default: 00h



Bit Range	Default & Access	Description
7	0b RO	**Multi-Function Bit (MFB):** Read only indicating single function device.
6:0	00h RO	**Configuration layout (CL):** Hardwired to 0 to indicate a standard PCI configuration layout.

14.6.11 Memory Base Address (MBAR)—Offset 10h

Value in this register will be different after the enumeration process.

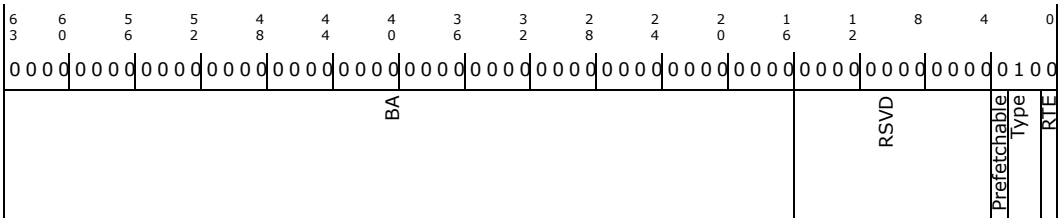
Access Method

Type: PCI Configuration Register (Size: 64 bits)

MBAR: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0000000000000004h



Bit Range	Default & Access	Description
63:16	0000000000 000h RW	**Base Address (BA):** Bits (63:16) correspond to memory address signals (63:16), respectively. This gives 64 KB of relocatable memory space aligned to 64 KB boundaries.
15:4	000h RO	**Reserved (RSVD):** Reserved. Read-Only 0, this indicates that this function is requesting an 64KB block of memory.
3	0b RO	**Prefetchable:** This bit is hardwired to 0 indicating that this range should not be prefetched.
2:1	10b RO	**Type:** If this field is hardwired to 00 it indicates that this range can be mapped anywhere within 32-bit address space. If this field is hardwired to 10 it indicates that this range can be mapped anywhere within 64-bit address space.

Bit Range	Default & Access	Description
0	0b RO	**Resource Type Indicator (RTE):** This bit is hardwired to 0 indicating that the base address field in this register maps to memory space

14.6.12 USB Subsystem Vendor ID (SSVID)—Offset 2Ch

This register is modified and maintained by BIOS

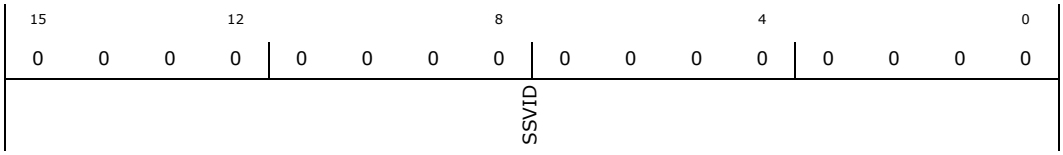
Access Method

Type: PCI Configuration Register (Size: 16 bits)

SSVID: [B:0, D:20, F:0] + 2Ch

Power Well: Core

Default: 0000h



Bit Range	Default & Access	Description
15:0	0000h RW/L	**USB Subsystem Vendor ID (SSVID):** This register, in combination with the USB Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

14.6.13 USB Subsystem ID (SSID)—Offset 2Eh

This register is modified and maintained by BIOS

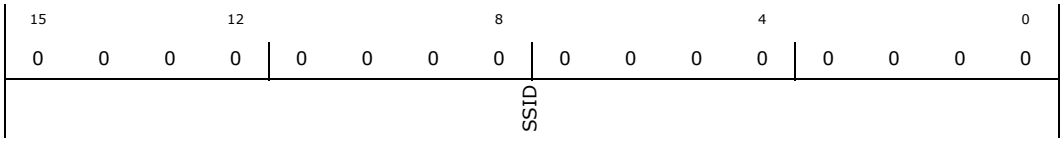
Access Method

Type: PCI Configuration Register (Size: 16 bits)

SSID: [B:0, D:20, F:0] + 2Eh

Power Well: Core

Default: 0000h



Bit Range	Default & Access	Description
15:0	0000h RW/L	**USB Subsystem ID (SSID):** BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

14.6.14 Capabilities Pointer (CAP_PTR)—Offset 34h

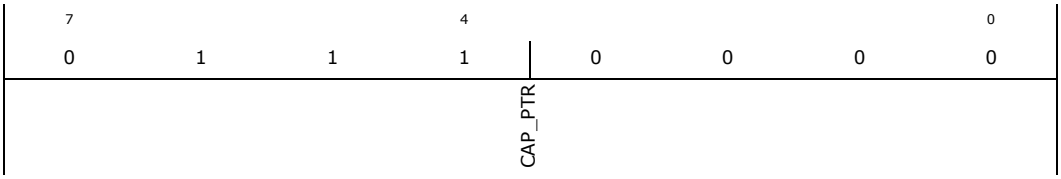
Access Method

Type: PCI Configuration Register (Size: 8 bits)

CAP_PTR: [B:0, D:20, F:0] + 34h

Power Well: Core

Default: 70h



Bit Range	Default & Access	Description
7:0	70h RO	**Capabilities Pointer (CAP_PTR):** This register points to the starting offset of the capabilities ranges.

14.6.15 Interrupt Line (ILINE)—Offset 3Ch

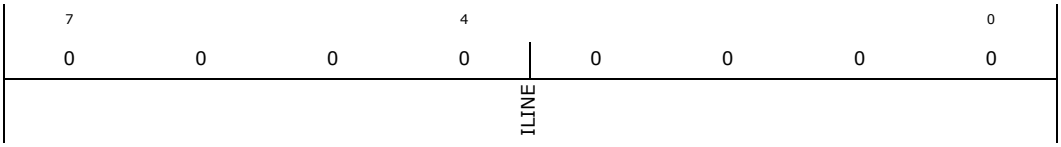
Access Method

Type: PCI Configuration Register (Size: 8 bits)

ILINE: [B:0, D:20, F:0] + 3Ch

Power Well: Core

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Interrupt Line (ILINE):** This data is not used by the Intel PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

14.6.16 Interrupt Pin (IPIN)—Offset 3Dh

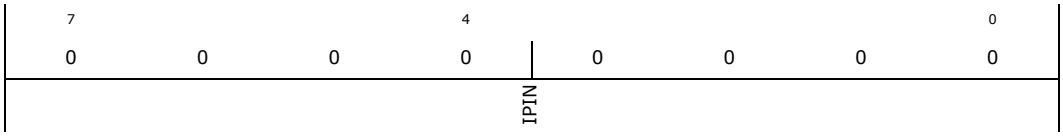
Access Method

Type: PCI Configuration Register (Size: 8 bits)

IPIN: [B:0, D:20, F:0] + 3Dh

Power Well: Core

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO/V	**Interrupt pin (IPIN):** Bits 3:0 reflect the value programmed in the interrupt pin registers in chipset configuration space. Bits 7:4 are hardwired to 0000b. See Chap 6 for value.

14.6.17 XHC System Bus Configuration 1 (XHCC1)—Offset 40h

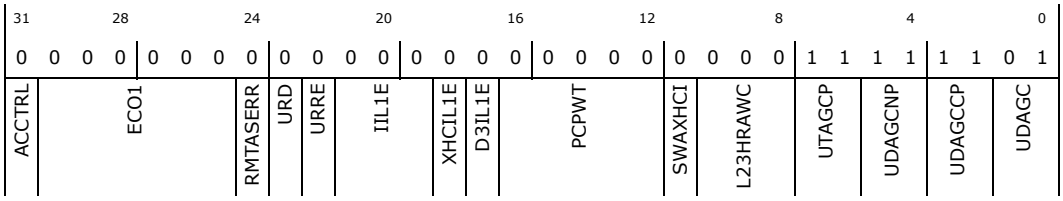
Access Method

Type: PCI Configuration Register (Size: 32 bits)

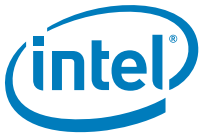
XHCC1: [B:0, D:20, F:0] + 40h

Power Well: Core

Default: 000000FDh



Bit Range	Default & Access	Description
31	0b RW/O	**Access Control (ACCTRL):** This bit is used by BIOS to lock/unlock lockable bits. When set to '1' the write access to bits locked by this bit is disabled (locked state). When set to '0', the write access to bit locked by this bit is enabled (unlocked state). Writable once after platform reset.
30:25	00h RW	**ECO1:** ECO bits are used during silicon bringup for FIBing.
24	0b RW	**Master/Target Abort SERR (RMTASERR):** When set, it allows the out-of-band error reporting from the xHCI Controller to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.
23	0b RW/C	**Unsupported Request Detected (URD):** Set the HW when xHCI Controller received an unsupported request posted cycle. Cleared by SW when the bit is written with value of '1'.
22	0b RW	**Unsupported Request Report Enable (URRE):** When set this bit allows the URD bit to be reported as SERR# (if SERR# reporting is enabled) and thus set the STS.SSE bit.



Bit Range	Default & Access	Description
21:19	000b RW	**Inactivity Initiated L1 Enable (IIL1E):** If programmed to non-zero, it allows L1 power managed to be enabled after the time-out period specified. 000: Disabled 001: 32 bb_cclk 010: 64 bb_cclk 011: 128 bb_cclk 100: 256 bb_cclk 101: 512 bb_cclk 110: 1024 bb_cclk 111: 131072 bb_cclk
18	0b RW	**XHC Initiated L1 Enable (XHCIL1E):** If set, allow the XHC initiated L1 power mangement to be enabled.
17	0b RW	**D3 Initiated L1 Enable (D3IL1E):** If set, allow PCI device state D3 initiated L1 power managment to be enables. This bit can only be set if the XHCI L1 Override P2 chicken bit is set.
16:12	00h RW	**Periodic Complete Pre Wake Time (PCPWT):** signal . This allows for platform wake time before the next scheduled periodic transaction. The value programmed in this field represents the # of bytes consumed in the current micro-frame which is required to allow for the periodic complete to de-assert. This allows for a programmable time to cause the periodic complete to de-assert prior to the start of the next micro-frame. Register Format: Bits (16:12) represnets the # of bytes remaining with a 256B granularity. Periodic Complete will de-assert if the bytes consumed in the current micro-frame is less
11	0h RW	**SW Assisted xHC Idle (SWAXHCI):** This bit being set will indicate xHC idleness (through SW means), which must be a '1' to allow L1 entry, and subsequently allow backbone clock to be gated. This bit is to be set by Intel xHCI driver after checking that the xHCI Controller will stay in idle state for a significant period of time, e.g. all ports disconnected. This bit can be cleared under the following conditions (see SWAXHCI Policy bits in xHC System Bus Configuration 2 register): n SW: SW could write 0 to clear this bit. n HW: HW, under policy control, will clear this bit on an MMIO access to the Host Controller. n HW: HW, under policy control, will clear this bit when HW exits Idle state.
10:8	000b RW	**L23 to Host Reset Acknowledge Wait Count (L23HRAWC):** If programmed to non zero, it allows a wait period after the L23 PHY has shutdown before returning host reset acknowledge to PMC. 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
7:6	11b RW	**Upstream Type Arbiter Grant Count Posted (UTAGCP):** Grant count for IOSF upstream L2 request type arbiter for posted type
5:4	11b RW	**Upstream Type Arbiter Grant Count Non Posted (UDAGCNP):** Grant count for IOSF upstream L2 type arbiter for non-posted type
3:2	11b RW	**Upstream Type Arbiter Grant Count Completion (UDAGCCP) (UDAGCCP):** Grant count for IOSF upstream L2 type arbiter for completion type
1:0	01b RW	**Upstream Device Arbiter Grant Count (UDAGC) (UDAGC):** Grant count for IOSF upstream L1 device arbiter

14.6.18 XHC System Bus Configuration 2 (XHCC2)—Offset 44h

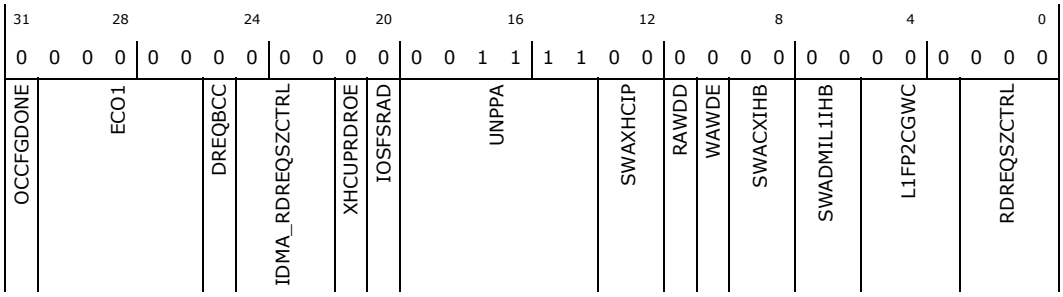
Access Method

Type: PCI Configuration Register (Size: 32 bits)

XHCC2: [B:0, D:20, F:0] + 44h

Power Well: SUS

Default: 0003C000h



Bit Range	Default & Access	Description
31	0b RW/O	**OC Configuration Done (OCCFGDONE):** This bit is used by BIOS to prevent spurious switching during OC configuration. It must be set by BIOS after configuration of the OC mapping bits is complete. Once this bit is set, OC mapping shall not be changed by SW.
30:26	00h RW	**ECO1:** ECO bits are used during silicon bringup for FIBing.
25	0b RW	**DMA Request Boundary Crossing Control (DREQBCC):** This bit controls the boundary crossing limit of each Read/Write Request. 0: 4KB 1: 64B
24:22	0h RW	**IDMA Read Request Size Control (IDMA_RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 011 - 110: Reserved 111: 64B
21	0b RW	**XHC Upstream Read Relaxed Ordering Enable (XHCUPRDROE):** This policy controls the Relaxed Ordering attribute for upstream reads. 0 - xHC will clear RO for all upstream read requests. 1 - xHC will set RO for all upstream read requests.
20	0b RW	**IOSF Sideband Register Access Disable (IOSFSRAD):** When set, it disables the IOSF sideband interface from accepting any host space register access.
19:14	0Fh RW	**Upstream Non-Posted Pre-Allocation (UNPPA):** This field reserves data sizes, in 64 byte chunks, of the downstream completion resource. This value is zero based. 000000 - 111111: Pre-allocate 64 bytes - 4096 bytes If set greater than the default allows over-allocation If set less than default allows under-allocation Only allowed to be programmed when BME = 0 and no outstanding downstream completion
13:12	00b RW	**SW Assisted xHC Idle Policy (SWAXHCIP):** Note: Irrespective of the setting of this field, SW write of 0 to SWAXHCI will clear the bit. 00b (default): xHC HW clears SWAXHCI bit upon: n MMIO access to Host Controller OR n xHC HW exits Idle state 01b: xHC HW does not autonomously clear SWAXHCI bit. The bit could be cleared only by SW. 10b: xHC HW clears SWAXHCI upon MMIO acces to Host Controller. xHC HW exit from Idle state will not clear SWAXHCI. 11b: Reserved
11	0h RW	**MMIO Read After MMIO Write Delay Disable (RAWDD):** This field controls delay on MMIO Read after MMIO Write. 0b (Default): Delay MMIO Read after MMIO Write 1b: Do not delay MMIO Read after MMIO Write Note that this delay applies after the second of the two DW writes in the case where the IOSF Gasket splits a QW write into two single DW writes to the IP.

Bit Range	Default & Access	Description
10	0h RW	**MMIO Write After MMIO Write Delay Enable (WAWDE):** This field controls delay on MMIO Write after previous MMIO Write. 0b (Default): Do not delay MMIO Write after previous MMIO Write 1b: Delay MMIO Write after previous MMIO Write Note that the delay count does not apply on the second of the two DW writes that are generated by IOSF Gasket when it splits a QW write into two. In other words, the second of the two DW writes could happen without any delay with respect to the first DW write. This choice is being made for ease of ECO. The delay count, in this case, will apply after the second of the two DW writes.
9:8	0h RW	**SW Assisted Cx Inhibit (SWACXIHB):** This field controls how the DMI L1 inhibit signal from USB3 to PMC will behave. 00: Never inhibit Cx 01: Inhibit Cx when Isochronous Endpoint is active (PPT Behavior) 10: Inhibit Cx when Periodic Active as defined in 40.4.3.2.1 11: Always inhibit Cx
7:6	0h RW	**SW Assisted DMI L1 Inhibit (SWADMIL1IHB):** This field controls how the DMI L1 inhibit signal from USB3 to DMI will behave. 00: Never inhibit DMI L1. 01: Inhibit DMI L1 when Isochronous Endpoint is active (PPT Behavior). 10: Inhibit DMI L1 when Priodic Active as defined in 40.4.3.2.1. 11: Inhibit DMI L1 if XHCC1.SWAXHCI = 0.
5:3	0h RW	**L1 Force P2 Clock Gating Wait Count (L1FP2CGWC):** If programmed to non zero, it allows L1 force P2 gating off the clock to be delayed after the time-out period specified. If wake up event is detected before the time-out, pclk remains alive and trigger L1 exit as though CPU host is causing the wake, 000: Disabled 001: 128 bb_cclk 010: 256 bb_cclk 011: 512 bb_cclk 100: 1024 bb_cclk 101: 2048 bb_cclk 110: 4096 bb_cclk 111: 131072 bb_cclk
2:0	000b RW	**Read Request Size Control (RDREQSZCTRL):** Read Request Size Control: This bit controls the maximum size of each Read Request. 000: 128B 001: 256B 010: 512B 011 - 110: Reserved 111: 64B

14.6.19 Clock Gating (XHCLKGTEN)—Offset 50h

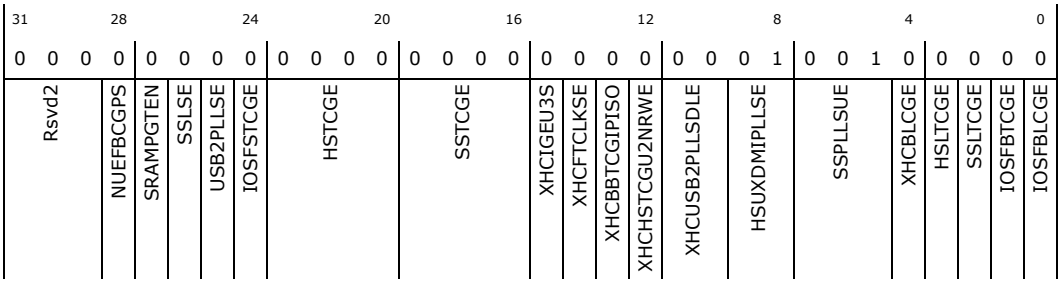
Access Method

Type: PCI Configuration Register (Size: 32 bits)

XHCLKGTEN: [B:0, D:20, F:0] + 50h

Power Well: Core

Default: 00000120h



Bit Range	Default & Access	Description
31:29	0h RO	**Rsvd2:** Reserved
28	0b RW	**Nak'ing USB2.0 EPs for Backbone Clock Gating and PLL Shutdown (NUEFBCGPS):** This field controls whether Naking USB2.0 EPs, once in Naking low priority schedule, should be considered as active for the considerations for backbone clock gating and PLL shutdown or not. 0: Naking USB2.0 EPs are not considered to be active for Backbone Clock Gating and PLL Shutdown evaluation. 1: Naking USB2.0 EPs are considered to be active for Backbone clock gating and PLL shutdown evaluation.

Bit Range	Default & Access	Description
27	0b RW	**SRAM Power Gate Enable (SRAMPGTEN):** This register enables the SRAM Power Gating when PLL shutdown conditions for all clock domains have been met 0 - Disallow SRAM Power Gating. 1 - Allow SRAM Power Gating
26	0h RW	**SS Link PLL Shutdown Enable (SSLSE):** This register enables the SS P3 state to be exposed to PXP PLL Shutdown conditions on behalf of all USB SS Ports ontop of trunk clock gating. 0 - P3 state NOT allowed to result in PXP PLL shutdown. 1- P3 state allowed to result in PXP PLL shutdown
25	0h RW	**USB2 PLL Shutdown Enable (USB2PLLSE):** When set, this bit allows USB2 PLL to be shutdown when HS Link trunk clock is gated, and xHC can tolerate PLL spin up time for subsequent clock request. Note: if USB2 PLL Shutdown Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
24	0h RW	**IOSF Sideband Trunk Clock Gating Enable (IOSFSTCGE):** When set, this bit allows the IOSF sideband clock trunk to be gated when idle conditions are met.
23:20	0h RW	**HS Backbone PXP Trunk Clock Gate Enable (HSTCGE):** This register determines the HS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) NA (no support for U1) (2) ==) U2 (L1) or deeper (3) ==) U3 (L2) or deeper
19:16	0h RW	**SS Backbone PXP Trunk Clock Gate Enable (SSTCGE):** This register determines the SS Ux state(s) which will be exposed to Backbone PXP trunk gating of core clock. Uy is a state allowed to result in trunk gating when ss_tcg_ux_en(x) is asserted. (0) ==) U0 or deeper (1) ==) U1 or deeper (2) ==) U2 or deeper (3) ==) U3 or deeper
15	0h RW	**XHC Ignore_EU3S (XHCIGEU3S):** This register determines if the xHC will use the EU3S as a condition to allow for Frame timer gating. 0 - xHC may allow frame timer to be gated when EU3S is set and all ports are in the required state. 1 - xHC may allow frame timer to be gated regardless of EU3S.
14	0h RW	**XHC Frame Timer Clock Shutdown Enable (XHCFTCLKSE):** This register determines if the xHC will allow the frame timer clock to be gated. 0 - xHC will not allow ICC PLL 96MHz output to be shutdown thus keeping the frame timer running. 1 - xHC will allow ICC PLL 96MHz output to be shutdown under specific conditions.
13	0h RW	**XHC Backbone PXP Trunk Clock Gate In Presence of ISOCH EP (XHCBBTCGIPISO):** This register controls the policy on allowing Backbone PXP trunk clock gate in the presence of IDLE ISOCH EP s with active DB. Allows the periodic active to be used in enabling Backbone PXP trunk clock gating of core clock. 0 Trunk gate of core clock is not allowed when ISOCH EP DB is set and ISOCH EP s are idle. 1 Allow trunk gate of core clock when ISOCH EP DB is set and ISOCH EP s are idle.
12	0h RW	**XHC HS Backbone PXP Trunk Clock Gate U2 non RWE (XHCHSTCGU2NRWE):** This register controls the policy on allowing Backbone PXP trunk gating of core clock when there is atleast 1 non Remote Wake Enabled HS Port in U2. 0 Prevent trunk gate of core clock when a non RWE HS Port is in U2. 1 Allow trunk gate of core clock when a non RWE HS Port is in U2.
11:10	0h RW	**XHC USB2 PLL Shutdown Lx Enable (XHCUSB2PLLSDLE):** This register determines the HS Link state(s) which will be exposed to USB2 PLL Shutdown conditions on behalf of all USB2 HS Ports. Ly is a state allowed to result in USB2 PLL Shutdown when en(x) is asserted. (0) ==) L1 or deeper (1) ==) L2 or deeper
9:8	01b RW	**HS Backbone PXP PLL Shutdown Ux Enable (HSUXDMIPLLSE):** This register determines the Ux state(s) which will be exposed to PXP PLL Shutdown conditions. PLL Shutdown is allowed in: 00b Disabled (Link states shall be disabled for DMI PLL shutdown) 01b U0 or conditions for 10b setting. 10b U2 or conditions for 11b setting. 10b U3, Disconnected, Disabled or Powered-Off.
7:5	001b RW	**SS Backbone PXP PLL Shutdown Ux Enable (SSPLLSUE):** This register determines the Ux state(s) which will be exposed to DMI PLL Shutdown conditions. PLL Shutdown is allowed in: 000b Disabled (Link states shall be ignored for DMI PLL shutdown). 001b U0 or conditions for 010b setting 010b U1 or conditions for 011b setting 011b U2 or conditions for 100b setting 100b U3, Disconnected, Disabled or Powered-Off

Bit Range	Default & Access	Description
4	0b RW	**XHC Backbone Local Clock Gating Enable (XHCBLCGE):** When set, this bit allows XHCI Controller IP backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value.
3	0b RW	**HS Link Trunk Clock Gating Enable (HSLTCGE):** When set, this bit allows High Speed Link control's 480 MHz and its 48/60 MHz link clock trunk to be gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.
2	0b RW	**SS Link Trunk Clock Gating Enable (SSLTCGE):** When set, this bit allows the SuperSpeed Link control's 250 MHz and its divided 125 MHz link clock trunk to ge gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.
1	0b RW	**IOSF Backbone Trunk Clock Gating Enable (IOSFBTCGE):** When set, this bit allows the IOSF backbone clock trunk to be gated when idle conditions are met.
0	0b RW	**IOSF Gasket Backbone Local Clock Gating Enable (IOSFBLCGE):** When set, this bit allows the IOSF Gasket backbone clock to be locally gated when idle conditions are met. Note: if XHC Dynamic Clock Gating Disable Fuse is '1', hardware will always see '0' as an output from this register. BIOS reading this register should always return the correct value. BIOS need to query fuses to see if HW is enabled.

14.6.20 Audio Time Synchronization (AUDSYNC)—Offset 58h

This 32 bit register is used for audio stream synchronization across different devices. Global signal sample_now captures a value in AUDSYNC register.

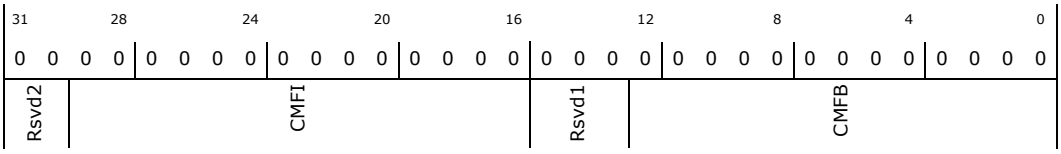
Access Method

Type: PCI Configuration Register (Size: 32 bits)

AUDSYNC: [B:0, D:20, F:0] + 58h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**Rsvd2:** Reserved.
29:16	0000h RO/V	**Captured Frame List Current Index/Frame Number (CMFI):** The value in this register is updated in response to sample_now signal. Bits (29:16) reflect state of bits (13:0) of FRINDEX
15:13	0h RO	**Rsvd1:** Reserved.

Bit Range	Default & Access	Description
12:0	0000h RO/V	**Captured Micro-frame BLIF (CMFB):** The value is updated in response to sample_now signal and provides information about offset within micro-frame. Captured value represents number of 8 high-speed bit time units from start of micro-frame. At the beginning of micro-frame captured value will be 0 and increase to maximum value at the end. Default maximum value is 7499 but it may be changed as result of adjustment done in FLA.

14.6.21 Serial Bus Release Number (SBRN)—Offset 60h

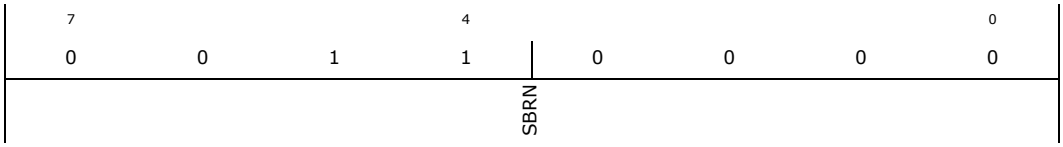
Access Method

Type: PCI Configuration Register (Size: 8 bits)

SBRN: [B:0, D:20, F:0] + 60h

Power Well: SUS

Default: 30h



Bit Range	Default & Access	Description
7:0	30h RO	**Serial Bus Release Number (SBRN):** A value of 30h indicates that this controller follows USB release 3.0.

14.6.22 Frame Length Adjustment (FLADJ)—Offset 61h

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit in the USBSTS register is a one. Changing value of this register while the host controller is operating yields undefined results.

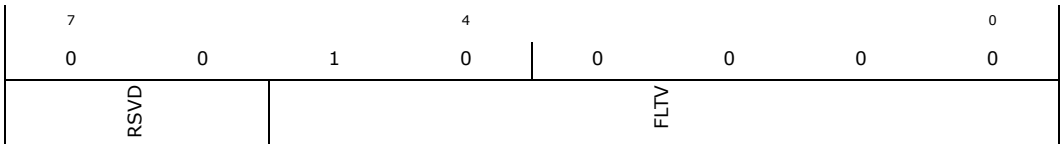
Access Method

Type: PCI Configuration Register (Size: 8 bits)

FLADJ: [B:0, D:20, F:0] + 61h

Power Well: SUS

Default: 20h



Bit Range	Default & Access	Description
7:6	00b RO	**Reserved (RSVD):** .

Bit Range	Default & Access	Description
5:0	20h RW	**Frame Length Timing Value (FLTV):** SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (number of High Speed bit times) FLADJ Value (decimal) (decimal) 59488 0 (00h) 59504 1 (01h) 59520 2 (02h) ... 59984 31 (1Fh) 60000 32 (20h) ... 60480 62 (3Eh) 60496 63 (3Fh) Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000. Frame Length (# High Speed bit times) FLADJ Value

14.6.23 Best Effort Service Latency (BESL)—Offset 62h

Bset Effort Service Latency.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

BESL: [B:0, D:20, F:0] + 62h

Power Well: Core

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
DBESLD				DBESL			

Bit Range	Default & Access	Description
7:4	0h RW/L	**Default Best Effort Service Latency Deep (DBESLD):** Default Best Effort Service Latency (DBESLD) If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESLD field. This is programmed by BIOS based on platform parameters.
3:0	0h RW/L	**Default Best Effort Service Latency (DBESL):** If the value of this field is non-zero, it defines the recommended value for programming the PORTPMSC register BESL field. This is programmed by BIOS based on platform parameters.

14.6.24 PCI Power Management Capability ID (PM_CID)—Offset 70h

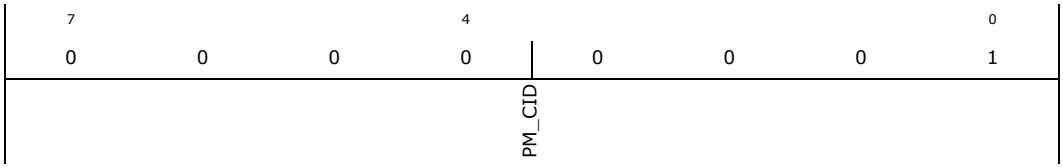
Access Method

Type: PCI Configuration Register (Size: 8 bits)

PM_CID: [B:0, D:20, F:0] + 70h

Power Well: Core

Default: 01h



Bit Range	Default & Access	Description
7:0	01h RO	**PCI Power Management Capability ID (PM_CID):** A value of 01h indicates that this is a PCI Power Management capabilities field.

14.6.25 Next Item Pointer #1 (PM_NEXT)—Offset 71h

This register is modified and maintained by BIOS

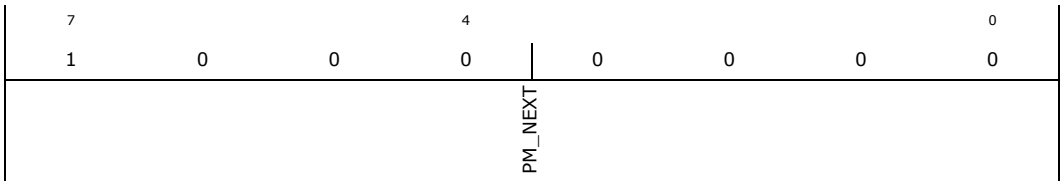
Access Method

Type: PCI Configuration Register (Size: 8 bits)

PM_NEXT: [B:0, D:20, F:0] + 71h

Power Well: Core

Default: 80h



Bit Range	Default & Access	Description
7:0	80h RW/L	**Next Item Pointer #1 (PM_NEXT):** This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the Access Control bit is set to '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of: 80h implies next capability is MSI 00h implies that MSI capability is hidden. Note: This value is never expected to be programmed.

14.6.26 Power Management Capabilities (PM_CAP)—Offset 72h

Normally, this register is read-only to report capabilities to the power management software. In order to report different power management capabilities depending on the system in which the Intel PCH is used, the write access to this register is controlled by the Access Control bit (ACCTRL). The value written to this register does not affect the hardware other than changing the value returned during a read. This register is modified and maintained by BIOS

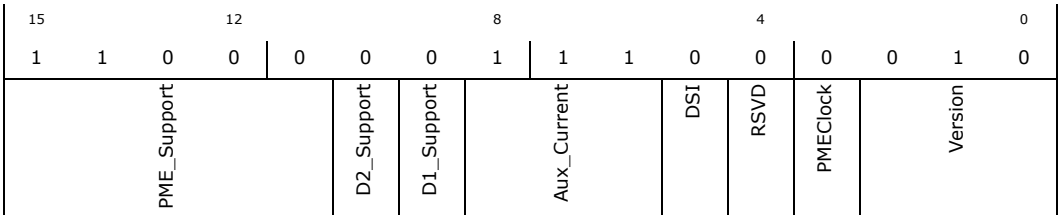
Access Method

Type: PCI Configuration Register (Size: 16 bits)

PM_CAP: [B:0, D:20, F:0] + 72h

Power Well: Core

Default: C1C2h



Bit Range	Default & Access	Description
15:11	11000b RW/L	**PME_Support:** This 5-bit field indicates the power states in which the function may assert PME#. The Intel PCH XHC does not support the D1 or D2 states. For all other states, the Intel PCH XHC is capable of generating PME#. Software should never need to modify this field.
10	0b RW/L	**D2_Support:** The D2 state is not supported.
9	0b RW/L	**D1_Support:** The D1 state is not supported.
8:6	111b RW/L	**Aux_Current:** The Intel PCH XHC reports 375mA maximum Suspend well current required when in the D3cold state. This value can be written by BIOS when a more accurate value is known.
5	0b RW/L	**DSI:** The Intel PCH reports 0, indicating that no device-specific initialization is required.
4	0b RO	**Reserved (RSVD):** Reserved.
3	0b RW/L	**PME Clock (PMEClock):** The Intel PCH reports 0, indicating that no PCI clock is required to generate PME#.
2:0	010b RW/L	**Version:** The Intel PCH reports 010, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

14.6.27 Power Management Control/Status (PM_CS)—Offset 74h

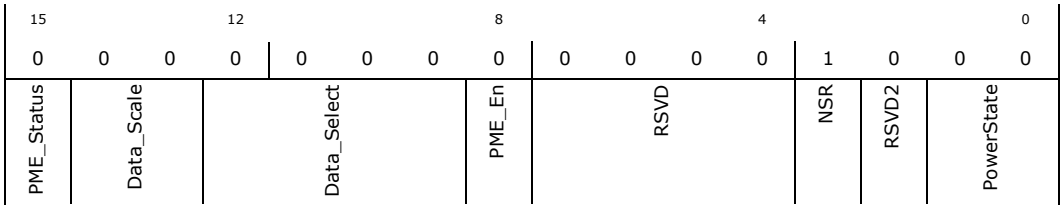
Access Method

Type: PCI Configuration Register (Size: 16 bits)

PM_CS: [B:0, D:20, F:0] + 74h

Power Well: SUS

Default: 0008h



Bit Range	Default & Access	Description
15	0b RW/1C	**PME_Status:** This bit is set when the Intel PCH XHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to deassert (if enabled). Writing a 0 has no effect. This bit must be explicitly cleared by the operating system each time the operating system is loaded.
14:13	00b RO	**Data_Scale:** The Intel PCH hardwires these bits to 00 because it does not support the associated Data register.
12:9	0h RO	**Data_Select:** The Intel PCH hardwires these bits to 0000 because it does not support the associated Data register.
8	0b RW	**PME_En:** A 1 enables the Intel PCH XHC to generate an internal PME signal when PME_Status is 1. This bit must be explicitly cleared by the operating system each time it is initially loaded.
7:4	0h RO	**Reserved (RSVD):** Reserved.
3	1b RO	**No Soft Reset (NSR):**), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. Transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0b RO	**Reserved (RSVD2):** Reserved.
1:0	00b RW	**PowerState:** This 2-bit field is used both to determine the current power state of XHC function and to set a new power state. The definition of the field values are: 00b - D0 state 11b - D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally, however, the data is discarded and no state change occurs. When in the D3hot state, the Intel PCH must not accept accesses to the XHC memory range, but the configuration space must still be accessible.

14.6.28 Message Signaled Interrupt CID (MSI_CID)—Offset 80h

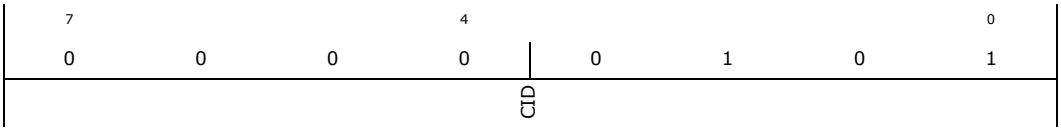
Access Method

Type: PCI Configuration Register (Size: 8 bits)

MSI_CID: [B:0, D:20, F:0] + 80h

Power Well: Core

Default: 05h



Bit Range	Default & Access	Description
7:0	05h RO	**Capability ID (CID):** Indicates that this is an MSI capability

14.6.29 Next item pointer (MSI_NEXT)—Offset 81h

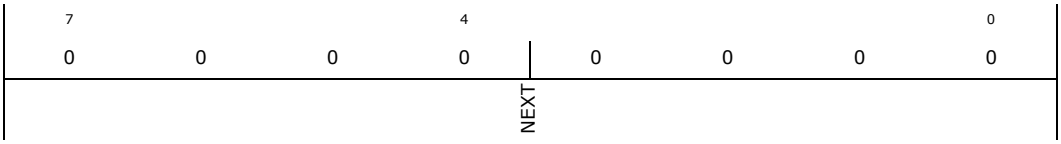
Access Method

Type: PCI Configuration Register (Size: 8 bits)

MSI_NEXT: [B:0, D:20, F:0] + 81h

Power Well: Core

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**Next Pointer (NEXT):** Indicates that this is the last item on the capability list

14.6.30 Message Signaled Interrupt Message Control (MSI_MCTL)—Offset 82h

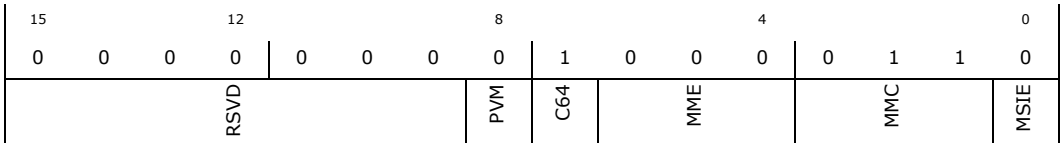
Access Method

Type: PCI Configuration Register (Size: 16 bits)

MSI_MCTL: [B:0, D:20, F:0] + 82h

Power Well: Core

Default: 0086h



Bit Range	Default & Access	Description
15:9	00h RO	**Reserved (RSVD):** Reserved.
8	0b RO	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per vector masking. Not supported
7	1b RO	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. This device is 64-bit capable.
6:4	0h RW	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. This device supports multiple message MSI.
0	0b RW	**MSI Enable (MSIE):** If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

14.6.31 Message Signaled Interrupt Message Address (MSI_MAD)—Offset 84h

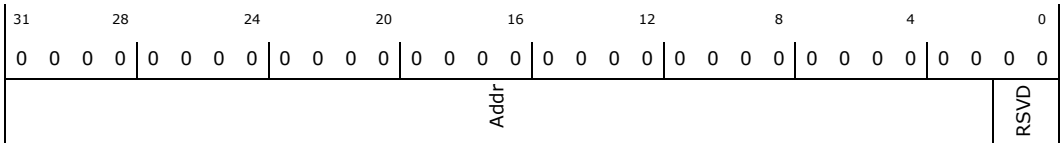
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MSI_MAD: [B:0, D:20, F:0] + 84h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**Addr:** Lower DW of system specified message address, always DWORD aligned

Bit Range	Default & Access	Description
1:0	00b RO	**Reserved (RSVD):** Reserved.

14.6.32 Message Signaled Interrupt Upper Address (MSI_MUAD)—Offset 88h

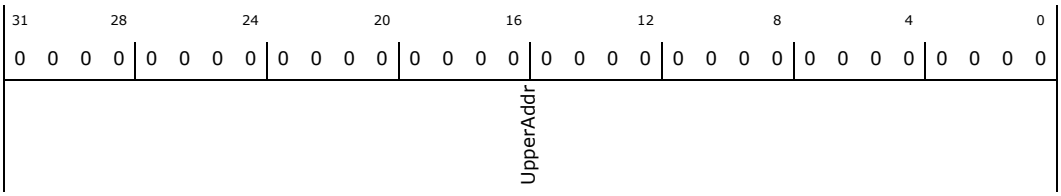
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MSI_MUAD: [B:0, D:20, F:0] + 88h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Upper Addr (UpperAddr):** Upper DW of system specified message address.

14.6.33 Message Signaled Interrupt Message Data (MSI_MD)—Offset 8Ch

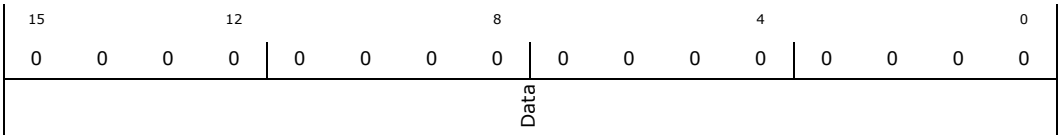
Access Method

Type: PCI Configuration Register (Size: 16 bits)

MSI_MD: [B:0, D:20, F:0] + 8Ch

Power Well: Core

Default: 0000h



Bit Range	Default & Access	Description
15:0	0000h RW	**Data:** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD(15:0)) during the data phase of the MSI memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated vectors. For example, a Multiple Message Enable encoding of 010 indicates the function has been allocated four vectors and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of vectors). If the Multiple Message Enable field is 000, the function is not permitted to modify the message data.

14.6.34 High Speed Configuration 2 (HSCFG2)—Offset A4h

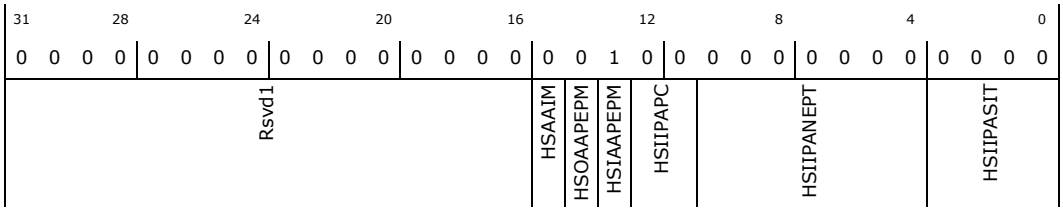
Access Method

Type: PCI Configuration Register (Size: 32 bits)

HSCFG2: [B:0, D:20, F:0] + A4h

Power Well: Core

Default: 00002000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Rsvd1:** Reserved.
15	0h RW	**HS ASYNC Active IN Mask (HSAAIM):** Determines if the Async Active will mask/ ignore IN EP s. 0 HS ASYNC Active will include IN EP s. 1 HS ASYNC Active will mask/ ignore IN EP s.
14	0h RW	**HS OUT ASYNC Active Polling EP Mask (HSOAAPEPM):** Determines if the Async Active for OUT HS/FS/LS masks/ignores EP s that are polling/PINGing (HS) due to NAK. 0 HS OUT ASYNC Active will include EP s that are polling. 1 HS OUT ASYNC Active will mask/ignore EP s that are polling.
13	1h RW	**HS IN ASYNC Active Polling EP Mask (HSIAAPEPM):** Determines if the Async Active for IN HS/FS/LS masks/ignores EP s that are polling due to NAK. 0 HS IN ASYNC Active will include EP s that are polling. 1 HS IN ASYNC Active will mask/ignore EP s that are polling.
12:11	0h RW	**HS INTR IN Periodic Active Policy Control (HSIIPAPC):** Controls how the HS INTR IN periodic active is used to generate the global periodic active. This will determine how the smallest service interval among active EP s and number of active EP s are used. 0 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold OR Numb of EP Threshold values meet the requirement. 1 HS INTR IN periodic active will be used to generate periodic active if Service Interval Threshold AND Numb of EP Threshold values meet the requirement. 2 Always allow HS INTR EP s to be used in the generation of the global Periodic Active indication. 3 Never allow HS INTR EP s to be used in the generation of the global Periodic Active indicaiton
10:4	00h RW	**HS INTR IN Periodic Active Num of EP Threshold (HSIIPANEPT):** Defines the threshold used to determine if Periodic Acive may include HS/FS/LS INTR IN EP active indication. If there are more than NumEPThreshold active HS/FS/LS INTR EP s then they may be included as part of the periodic active generation.
3:0	0h RW	**HS INTR IN Periodic Active Service Interval Threshold (HSIIPASIT):** Defines the Service Interval threshold used to determine if Periodic Acive will include HS/FS/LS INTR IN EP active indication. If there are any active HS/FS/LS INTR EP s with a service interval less than or equal to this threshold then they may be included as part of the periodic active generation.

14.6.35 Super Speed Configuration 1 (SSCFG1)—Offset B0h

Refer to the switching flows section of this document.

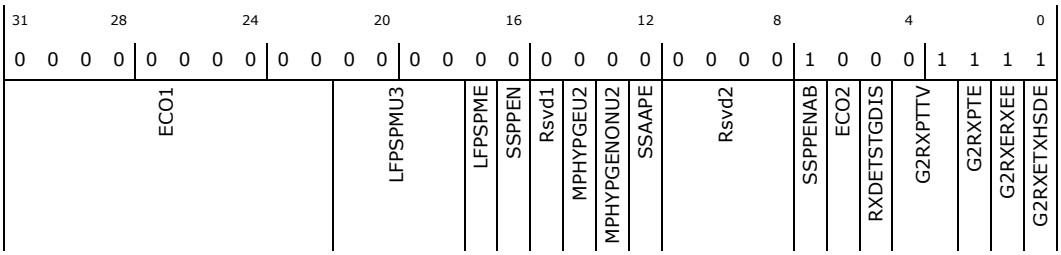
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SSCFG1: [B:0, D:20, F:0] + B0h

Power Well: Core

Default: 0000008Fh



Bit Range	Default & Access	Description
31:22	000h RW	**ECO1:** ECO bits are used during silicon bringup for FIBing.
21:18	0h RW	**LFPS Power Management in U3 Enable (LFPSPMU3):** This field allows xHC to turn off LFPS Receiver when the port is in U3. This allows the Host Controller to save some extra power (about 50W per port) in idle states if device connected on a port is not Resume capable or Resume enabled. This choice has to be done by BIOS and based on platform knowledge. For example, if an in-box device is not Resume Capable, BIOS could allow xHC to turn-off Rx LFPS when the port is in U3. Each bit represents a port. Bit (16) is for USB3.0 Port 0, Bit (17) is for USB3.0 Port 1 and so on. 0 in a bit position: LFPS Receiver shall be kept enabled when the port is in U3. 1 in a bit position: LFPS Receiver shall be disabled when the port is in U3.
17	0b RW	**LFPS Power Management Enable (LFPSPME):** This field provides programmability of LFPS Receiver power management capability when USB3.0 ports are Disabled or in Disconnected state. 0: Do not power manage LFPS receiver. LFPS receivers are enabled in all states. 1: Power manage LFPS receiver. LFPS receivers will be turned off if USB3.0 port is Disabled or Disconnected. Note: Default value is being kept at 0 in case EXI architecture/design takes the path of not doing dynamic Rx LFPS enabling for EXI signature detect and disable LFPS Power Management to keep Rx LFPS buffer on for debug.
16	0b RW	**USB3 SS Port Polling Enable (SSPPEN):** 0: Prevent USB3 Super-speed port to start Polling.LFPS. 1: Allow USB3 Super-speed port to start Polling.LFPS. NOTE: This bit will take effect in allowing/preventing USB3 SS port from starting Polling.LFPS only if SSPPENAB is cleared.
15	0b RO	**Rsvd1:** Reserved.
14	0b RW	**MODPHY Power Gate Enable for U2 (MPHYPGEU2):** This bit controls whether LPT-LPT xHC will allow modPHY power gating or not when a port is in U2 state. Note that this single bit controls all ports of xHC. 0b xHC shall not initiate Power Gate Request If xHC had initiated Power Gate Request before this bit is programmed to 0, xHC shall initiate the handshake to wake modPHY from power gated state. 1b xHC is enabled to initiate Power Gate Request if power gating conditions are met.
13	0b RW	**MODPHY Power Gate Enable for non-U2 states (MPHYPGENONU2):** This bit controls whether LPT-LPT xHC will allow modPHY power gating or not when a port is in states other than U2. Note that this single bit controls all ports of xHC. 0b xHC shall not initiate Power Gate Request If xHC had initiated Power Gate Request before this bit is programmed to 0, xHC shall initiate the handshake to wake modPHY from power gated state. 1b xHC is enabled to initiate Power Gate Request if power gating conditions are met.

Bit Range	Default & Access	Description
12	0h RW	**xHC SS Async Active Propogation Enable (SSAAPE):** This register controls the ss async active exposusre to PMC via the xHC active indication 0 SS Async Active is not propogated to PMC 1 SS Async Active is propogated to PMC
11:8	0h RO	**Rsvd2:** Reserved
7	1b RW	**USB3 SS Port Polling Enable Active (SSPPENAB):** 0: Allow blocking of USB3 Super-speed port from starting Polling.LFPS. 1: Disallow blocking of USB3 Super-speed port from starting Polling.LFPS (A stepping behavior). NOTE: When this bit is cleared, Polling.LFPS blocking is controlled by SSPPEN bit.
6	0h RW	**ECO2:** ECO bits are used during silicon bringup for FIBing.
5	0h RW	**Receiver Detect Staggering Disable (RXDETSTGDIS):** When set, this regiter bit disables receiver detect staggering between all 6 USB3 lanes Note that the bit is ONLY meant for SW to disable the staggering if desired. Once it is set to disabled, SW is not allowed to re-enable the staggering by clearing the bit.
4:3	1h RW	**Gotorxelecidle Polling Timer Timeout Value (G2RXPTTV):** Timeout value for Gotorxelecidle Polling Timer: 00: 1 to 2 us (Simulation speed up mode only). 01: 19 to 20 us (Default). 10: 23 to 24 us. 11: 199 to 200 us. This register needs to be programmed when G2RXPOLLTMREN = 0.
2	1b RW	**Gotorxelecidle Polling Timer Enable (G2RXPTE):** If enabled (1), Gasket starts a timer after transmitting high speed data AND not receiving LFPS, and will only de-assert GoToRxElecIdle after timer expires during Polling. If disabled (0), Gasket will assert / de-assert GoToRxElecIdle purely based on Gotorxelecidle assertion upon RxElecIdle de-assertion (LFPS detected) enable bit (G2RXERXEE) and Gotorxelecidle assertion when not transmitting high speed data enable bit (G2RXETXHSDE)
1	1b RW	**GotoRxElecidle Assertion Upon RxElecIdle Exit Enable (G2RXERXEE):** When enabled (set to '1'), allow Gasket to assert GoToRxElecIdle to UAFE to turn off its receiver upon the de-assertion of GoToRxElecIdle (LFPS detected). This bit needs to be programmed when the USB3 port is not enabled.
0	1b RW	**GotoRxElecidle Assertion When Transmitting High Speed Data Enable (G2RXETXHSDE):** When enabled (set to '1'), allow Gaskets to assert GoToRxElecIdle to UAFE to turn off its receiver when not transmitting high speed data: P0 and TxElecIdle = 1. This bit needs to be programmed when the USB3 port is not enabled.

14.6.36 XHCI USB2 Overcurrent Pin Mapping 1 (U2OCM1)—Offset C0h

The RW/L property of this register is controlled by OCCFGDONE bit.

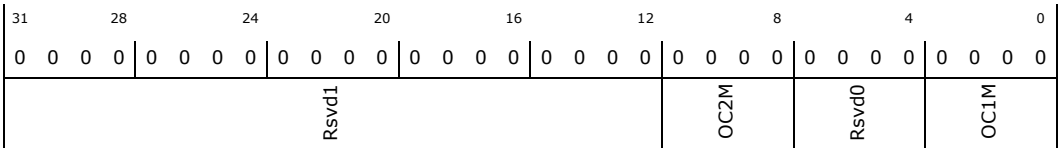
Access Method

Type: PCI Configuration Register (Size: 32 bits)

U2OCM1: [B:0, D:20, F:0] + C0h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0h RO	**Rsvd1:** Reserved
11:8	0h RW/L	**OC2 Mapping (OC2M):** Each bit position maps OC2 to a set of ports as follows: The OC2 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. Bit 15 14 13 12 11 10 9 8 Port 8 7 6 5 4 3 2 1
7:4	0h RO	**Rsvd0:** Reserved
3:0	0h RW/L	**OC1 Mapping (OC1M):** Each bit position maps OC1 to a set of ports as follows: The OC1 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin Bit 7 6 5 4 3 2 1 0 Port 8 7 6 5 4 3 2 1

14.6.37 XHCI USB2 Overcurrent Pin Mapping 2 (U2OCM2)—Offset C4h

Reserved

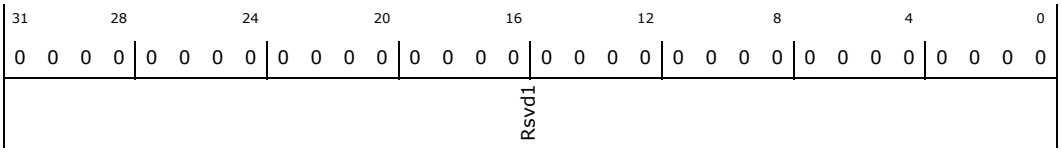
Access Method

Type: PCI Configuration Register (Size: 32 bits)

U2OCM2: [B:0, D:20, F:0] + C4h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Rsvd1:** Reserved

14.6.38 XHCI USB3 Overcurrent Pin Mapping 1 (U3OCM1)—Offset C8h

The RW/L property of this register is controlled by OCCFGDONE bit.

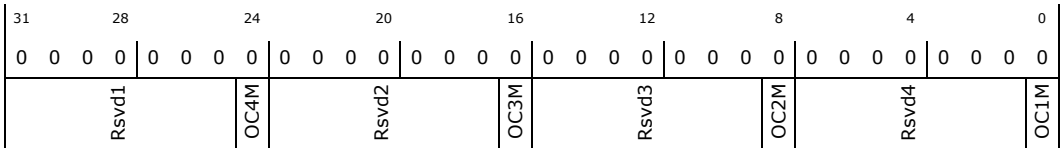
Access Method

Type: PCI Configuration Register (Size: 32 bits)

U3OCM1: [B:0, D:20, F:0] + C8h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:25	00h RO	**Rsvd1:** Reserved.
24	0b RW/L	**OC4 Mapping (OC4M):** Each bit position maps OC4 to a set of ports as follows: The OC4 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. Bit 27 26 25 24 Port 4 3 2 1
23:17	00h RO	**Rsvd2:** Reserved.
16	0b RW/L	**OC3 Mapping (OC3M):** Each bit position maps OC3 to a set of ports as follows: The OC3 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. Bit 19 18 17 16 Port 4 3 2 1
15:9	00h RO	**Rsvd3:** Reserved.
8	0b RW/L	**OC2 Mapping (OC2M):** Each bit position maps OC2 to a set of ports as follows: The OC2 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin. Bit 11 10 9 8 Port 4 3 2 1
7:1	00h RO	**Rsvd4:** Reserved.
0	0b RW/L	**OC1 Mapping (OC1M):** Each bit position maps OC1 to a set of ports as follows: The OC1 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to ensure that a given port's bit map is set only for one OC pin Bit 3 2 1 0 Port 4 3 2 1

14.6.39 XHCI USB3 Overcurrent Pin Mapping 2 (U3OCM2)—Offset CCh

The RW/L property of this register is controlled by OCCFGDONE bit. Note: U3OCM2 allows the OC pins 8:5 to be mapped to the same 6 SS ports that U3OCM1 allows. This a llows flexibility in pairing SS ports with HS ports at the connector. Care must be taken to make s ure OC pin assignment is consistent across USB3 and USB2 ports (depending upon the pairing).

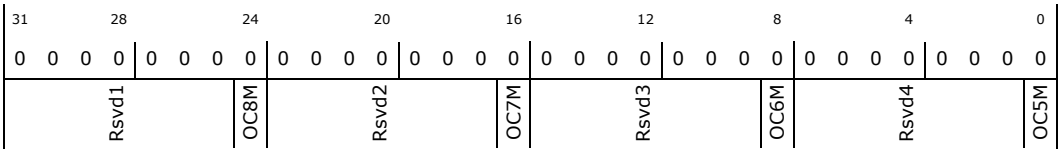
Access Method

Type: PCI Configuration Register (Size: 32 bits)

U3OCM2: [B:0, D:20, F:0] + CCh

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:25	00h RO	**Rsvd1:** Reserved.
24	0b RW/L	**OC8 Mapping (OC8M):** Each bit position maps OC8 to a set of ports as follows: The OC8 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to e nsure that a given port's bit map is set only for one OC pin. Bit 24 Port 1
23:17	00h RO	**Rsvd2:** Reserved.
16	0b RW/L	**OC7 Mapping (OC7M):** Each bit position maps OC7 to a set of ports as follows: The OC7 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to e nsure that a given port's bit map is set only for one OC pin. Bit 16 Port 1
15:9	00h RO	**Rsvd3:** Reserved.
8	0b RW/L	**OC6 Mapping (OC6M):** Each bit position maps OC6 to a set of ports as follows: The OC6 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to e nsure that a given port's bit map is set only for one OC pin. Bit 8 Port 1
7:1	00h RO	**Rsvd4:** Reserved.
0	0b RW/L	**OC5 Mapping (OC5M):** Each bit position maps OC5 to a set of ports as follows: The OC5 pin is ganged to the overcurrent signal of each port that has its corresponding bit set. It is SW's responsibility to e nsure that a given port's bit map is set only for one OC pin Bit 0 Port 1

14.6.40 USB2 Port Routing (USB2PR)—Offset D0h

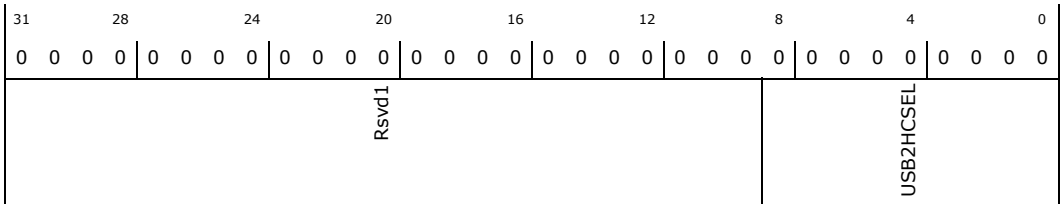
Access Method

Type: PCI Configuration Register (Size: 32 bits)

USB2PR: [B:0, D:20, F:0] + D0h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:9	000000h RO	**Rsvd1:** Reserved.
8:0	000h RW	**USB2 HC Selector (USB2HCSEL):** This field maps the USB2 port between the XHCI and EHCI controller (it has no effect on USB3). When set to 1, Routes USB2 pins to the XHCI controller. Routes OC pin to XHCI (based on the mapping in the OC register). Masks the USB2 port from the EHCI. Masks OC pin from ECHI. When set to 0, Routes all the USB2 pins to the legacy EHCI. Routes OC pin to EHCI (based on the mapping in the OC register). Masks the USB2 port from the XHCI. Masks OC pin from XHCI. Port to bit mapping is in one-hot encoding; that is, bit 0 controls port 1 and so on.

14.6.41 USB2 Port Routing Mask (USB2PRM)—Offset D4h

The RW/L property of this register is controlled by the ACCTRL bit.

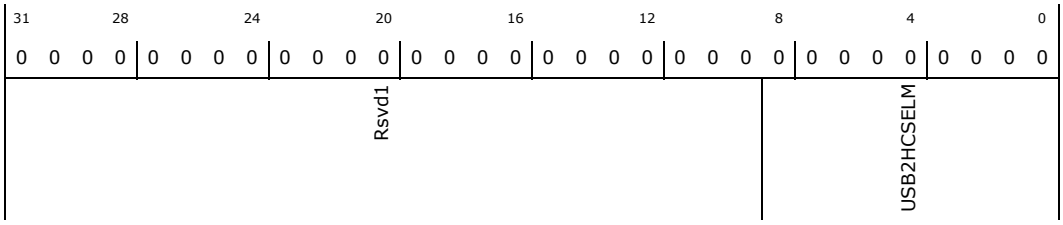
Access Method

Type: PCI Configuration Register (Size: 32 bits)

USB2PRM: [B:0, D:20, F:0] + D4h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:9	000000h RO	**Rsvd1:** Reserved.

Bit Range	Default & Access	Description
8:0	000h RW/L	**USB2 HC Selector Mask (USB2HCSELM):** This field allows the BIOS to communicate to the OS which USB 2.0 ports can be switched from the EHCI controller to the xHCI controller. When set to 1, The OS may switch the USB 2.0 port between the EHCI and xHCI host controllers by modifying the corresponding USB2HCSEL bit. When set to 0, The OS shall not modify the corresponding USB2HCSEL bit. BIOS shall set this bit to a '1' if the corresponding USB2HCSEL bit is RW, unless it knows an internal USB 2.0 device attached to that port will not work under xHCI. Port to bit mapping is in one-hot encoding; that is, bit 0 controls port 1 and so on.

14.6.42 USB3 Port Routing (USB3PR)—Offset D8h

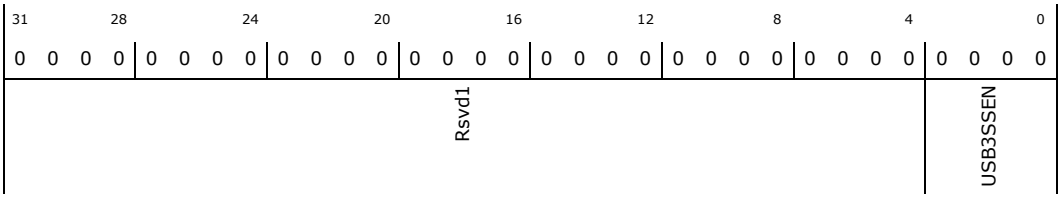
Access Method

Type: PCI Configuration Register (Size: 32 bits)

USB3PR: [B:0, D:20, F:0] + D8h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0000000h RO	**Rsvd1:** Reserved.
3:0	0h RW	**USB3 SS Enable (USB3SSEN):** This field controls whether SuperSpeed capability is enabled for a given USB3 port. When set to 1, Enables SS termination Enables PORTSC to to see the connects on the ports. When set to 0, Disables SS termination Blocks PORTSC from reporting attach/connect. Places port in the lowest power state.

14.6.43 USB3 Port Routing Mask (USB3PRM)—Offset DCh

The RW/L property of this register is controlled by the ACCTRL bit.

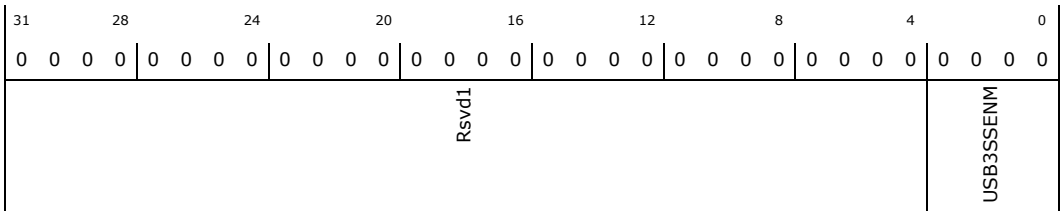
Access Method

Type: PCI Configuration Register (Size: 32 bits)

USB3PRM: [B:0, D:20, F:0] + DCh

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0000000h RO	**Rsvd1:** Reserved.
3:0	0h RW/L	**USB3 SS Enable Mask (USB3SSENM):** This field allows the BIOS to communicate to the OS which USB 3.0 ports can have the SuperSpeed capabilities enabled. When set to 1, The OS may enable or disable the SuperSpeed capabilities by modifying the corresponding USB3SSEN bit. When set to 0, The OS shall not modify the corresponding USB3SSEN bit. BIOS shall set this bit to a '1' if the corresponding USB3SSEN bit is RW, unless the BIOS has cleared the USB2HCSELM bit for a USB 2.0 port and the BIOS wishes the OS to disable the corresponding SuperSpeed terminations for that physical connector. Port to bit mapping is in one-hot encoding; that is, bit 0 controls port 1 and so on.

14.6.44 Fuse and Strap (FUS)—Offset E0h

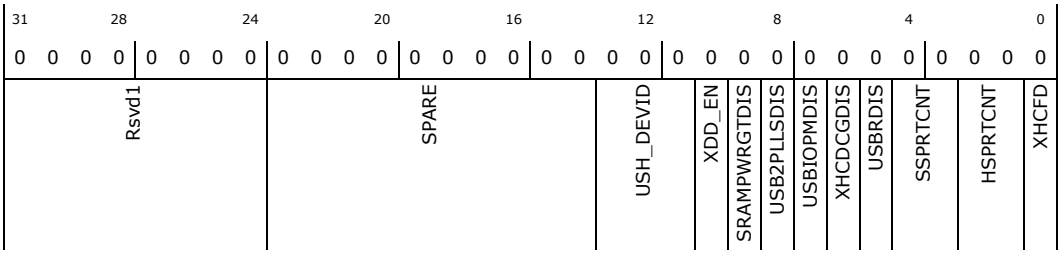
Access Method

Type: PCI Configuration Register (Size: 32 bits)

FUS: [B:0, D:20, F:0] + E0h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Rsvd1:** Reserved.
23:14	000h RO/V	**Spare Fuses (SPARE):** Will be used for VLV2.
13:11	000b RO/V	**USH DevID (USH_DEVID):** LSB bits of USH PCIe Device ID The 3 LSB bits enable defining up to 8 separate USH SKUs if required
10	0b RO/V	**Debug Device Enable (XDD_EN):** 0 : Debug Device is Enabled 1: Debug Device is Disabled
9	0h RO/V	**SRAM Power Gating Disable (SRAMPWRGTDIS):** 0: SRAM Power Gating Enabled 1: SRAM Power Gating Disabled
8	0h RO/V	**USB2 PLL Shutdown Disable (USB2PLLSDIS):** 0: USB2 PLL shutdown enabled 1: USB2 PLL shutdown disabled
7	0h RO/V	**USB I/O Power Management Disable (USBIOPMDIS):** 0: USB2 HW LPM and USB3 HW Ux under XHC enabled 1: USB2 HW LPM and USB3 HW Ux under XHC disabled
6	0h RO/V	**XHC Dynamic Clock Gating Disable (XHCDCGDIS):** 0: USB3 (XHC) dynamic clock gating enabled 1: USB3 (XHC) dynamic clock gating disabled
5	0h RO/V	**USBr Disable (USBRDIS):** 0: USBr enabled 1: USBr disabled
4:3	0h RO/V	**SS Port Count (SSPRTCNT):** This field specifies number of SS ports present. Supported combinations are: 00: 6 SS ports 01: 4 SS ports 10: 2 SS ports 11: 0 SS ports
2:1	0h RO/V	**HS Port Count (HSPRTCNT):** This field specifies number HS ports present. Supported combinations are: 00: 14 HS ports 01: 12 HS ports 10: 10 HS ports 11: N/A (reserved)
0	0h RO/V	**XHCI Function Disable (XHCFD):** When asserted, it indicates the XHCI is fused to function disabled.

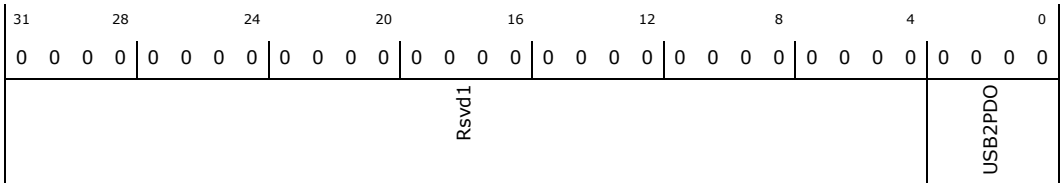
14.6.45 USB2 Port Disable Override (USB2PDO)—Offset E4h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

USB2PDO: [B:0, D:20, F:0] + E4h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
3:0	000h RW/O	**USB2 Port Disable Override (USB2PDO):** A '1' in a bit position prevents the corresponding USB2 port from reporting a Device Connection to the XHC. **Power Well:** SUS

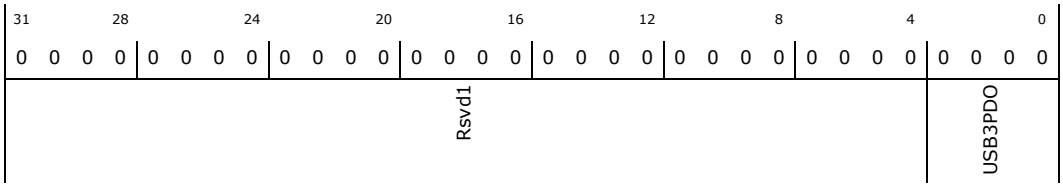
14.6.46 USB3 Port Disable Override (USB3PDO)—Offset E8h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

USB3PDO: [B:0, D:20, F:0] + E8h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0000000h RO	**Rsvd1:** Reserved. **Power Well:** Core
3:0	0h RW/O	**USB3 Port Disable Override (USB3PDO):** A '1' in a bit position prevents the corresponding USB3 port from reporting a Device Connection to the XHC. **Power Well:** Core

14.6.47 USB2 FS/LS Port Staggering Control (FSLSPS)—Offset ECh

The host controller provides a programmable time offset for each FS/LS port. Based on the value programmed in these registers, the controller will inject a fixed delay on each FS or LS transaction initiated on that port.

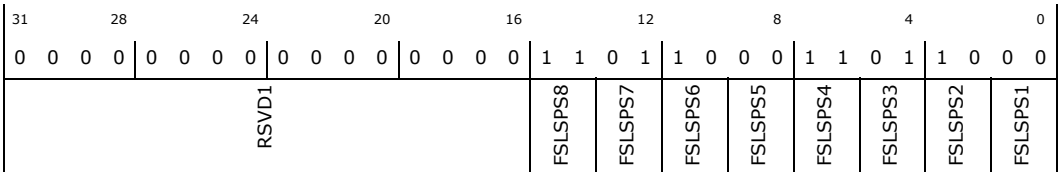
Access Method

Type: PCI Configuration Register (Size: 32 bits)

FSLSPS: [B:0, D:20, F:0] + ECh

Power Well: Core

Default: 0000D8D8h



Bit Range	Default & Access	Description
31:16	0000h RO	**Rsvd1 (RSVD1):** Reserved for Future Use
15:14	11b RW	**FS/LS Stagger Offset for USB2 Port 8 (FSLSPS8):** FS/LS Stagger Offset for USB2 Port 8 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset
13:12	01b RW	**FS/LS Stagger Offset for USB2 Port 7 (FSLSPS7):** FS/LS Stagger Offset for USB2 Port 7 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset
11:10	10b RW	**FS/LS Stagger Offset for USB2 Port 6 (FSLSPS6):** FS/LS Stagger Offset for USB2 Port 6 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset
9:8	00b RW	**FS/LS Stagger Offset for USB2 Port 5 (FSLSPS5):** FS/LS Stagger Offset for USB2 Port 5 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset
7:6	11b RW	**FS/LS Stagger Offser for USB2 Port 4 (FSLSPS4):** FS/LS Stagger Offset for USB2 Port 4 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset
5:4	01b RW	**FS/LS Stagger Offset for USB2 Port 3 (FSLSPS3):** FS/LS Stagger Offset for USB2 Port 3 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset
3:2	10b RW	**FS/LS Stagger Offser for USB2 Port 2 (FSLSPS2):** FS/LS Stagger Offset for USB2 Port 2 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset
1:0	00b RW	**FS/LS Stagger Offset for USB2 Port 1 (FSLSPS1):** FS/LS Stagger Offset for USB2 Port 1 00: No time offset / Staggering disabled 01: 4ns time offset 10: 8ns time offset 11: 12ns time offset

§ §

14.7 USB xHCI Memory Mapped I/O Registers

Table 120. Summary of USB xHCI Memory Mapped I/O Registers—MBAR

Offset Start	Offset End	Register ID—Description	Default Value
0h	0h	"Capability Registers Length (CAPLENGTH)—Offset 0h" on page 387	80h
2h	3h	"Host Controller Interface Version Number (HCIVERSION)—Offset 2h" on page 387	0100h
4h	7h	"Structural Parameters 1 (HCSPARAMS1)—Offset 4h" on page 388	07000820h
8h	Bh	"Structural Parameters 2 (HCSPARAMS2)—Offset 8h" on page 388	84000054h
Ch	Fh	"Structural Parameters 3 (HCSPARAMS3)—Offset Ch" on page 389	00040001h
10h	13h	"Capability Parameters (HCCPARAMS)—Offset 10h" on page 390	200071E1h
14h	17h	"Doorbell Offset (DBOFF)—Offset 14h" on page 391	00003000h
18h	1Bh	"Runtime Register Space Offset (RTSOFF)—Offset 18h" on page 391	00002000h
80h	83h	"USB Command (USBCMD)—Offset 80h" on page 392	00000000h
84h	87h	"USB Status (USBSTS)—Offset 84h" on page 393	00000001h
88h	8Bh	"Page Size (PAGESIZE)—Offset 88h" on page 394	00000001h
94h	97h	"Device Notification Control (DNCTRL)—Offset 94h" on page 394	00000000h
98h	9Bh	"Command Ring Low (CRCR_LO)—Offset 98h" on page 395	00000000h
9Ch	9Fh	"Command Ring High (CRCR_HI)—Offset 9Ch" on page 395	00000000h
B0h	B3h	"Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h" on page 396	00000000h
B4h	B7h	"Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h" on page 396	00000000h
B8h	BBh	"Configure (CONFIG)—Offset B8h" on page 397	00000000h
480h	483h	"Port 1 Status and Control USB3 (PORTSC1USB2)—Offset 480h" on page 397	000002A0h
484h	487h	"Port 1 Power Management Status and Control USB2 (PORTPMSC1USB2)—Offset 484h" on page 399	00000000h
48Ch	48Fh	"Port X Hardware LPM Control Register (PORTHLPM1)—Offset 48Ch" on page 399	00000000h
490h	493h	"Port 2 Status and Control USB3 (PORTSC2USB2)—Offset 490h" on page 400	000002A0h
494h	497h	"Port 2 Power Management Status and Control USB2 (PORTPMSC2USB2)—Offset 494h" on page 402	00000000h
49Ch	49Fh	"Port X Hardware LPM Control Register (PORTHLPM2)—Offset 49Ch" on page 402	00000000h
4A0h	4A3h	"Port 3 Status and Control USB3 (PORTSC3USB2)—Offset 4A0h" on page 403	000002A0h
4A4h	4A7h	"Port 3 Power Management Status and Control USB2 (PORTPMSC3USB2)—Offset 4A4h" on page 405	00000000h
4ACh	4AFh	"Port X Hardware LPM Control Register (PORTHLPM3)—Offset 4ACh" on page 405	00000000h
4B0h	4B3h	"Port 4 Status and Control USB3 (PORTSC4USB2)—Offset 4B0h" on page 406	000002A0h
4B4h	4B7h	"Port 4 Power Management Status and Control USB2 (PORTPMSC4USB2)—Offset 4B4h" on page 408	00000000h
4BCh	4BFh	"Port X Hardware LPM Control Register (PORTHLPM4)—Offset 4BCh" on page 408	00000000h
4C0h	4C3h	"Port 8 Status and Control USB2 (PORTSC5USB2)—Offset 4C0h" on page 409	000002A0h
4C4h	4C7h	"Port 5 Power Management Status and Control USB2 (PORTPMSC5USB2)—Offset 4C4h" on page 411	00000000h
4CCh	4CFh	"Port X Hardware LPM Control Register (PORTHLPM5)—Offset 4CCh" on page 411	00000000h

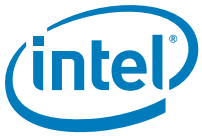


Table 120. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset Start	Offset End	Register ID—Description	Default Value
4D0h	4D3h	"Port 6 Status and Control USB2 (PORTSC6USB2)—Offset 4D0h" on page 412	000002A0h
4D4h	4D7h	"Port 6 Power Management Status and Control USB2 (PORTPMSC6USB2)—Offset 4D4h" on page 414	00000000h
4DCh	4DFh	"Port X Hardware LPM Control Register (PORTHLPM6)—Offset 4DCh" on page 414	00000000h
4E0h	4E3h	"Port 1 Status and Control USB3 (PORTSC1USB3)—Offset 4E0h" on page 415	000002A0h
4E4h	4E7h	"Port 1 Power Management Status and Control USB3 (PORTPMSC1USB3)—Offset 4E4h" on page 417	00000000h
4E8h	4EBh	"Port 1 Link Info (PORTLI1)—Offset 4E8h" on page 418	00000000h
2000h	2003h	"Microframe Index (MFINDEX)—Offset 2000h" on page 418	00000000h
2020h	2023h	"Interrupter 1 Management (IMAN1)—Offset 2020h" on page 419	00000000h
2024h	2027h	"Interrupter 1 Moderation (IMOD1)—Offset 2024h" on page 419	00000FA0h
2028h	202Bh	"Event Ring Segment Table Size 1 (ERSTSZ1)—Offset 2028h" on page 420	00000000h
2030h	2033h	"Event Ring Segment Table Base Address Low 1 (ERSTBA_LO1)—Offset 2030h" on page 420	00000000h
2034h	2037h	"Event Ring Segment Table Base Address High 1 (ERSTBA_HI1)—Offset 2034h" on page 421	00000000h
2038h	203Bh	"Event Ring Dequeue Pointer Low 1 (ERDP_LO1)—Offset 2038h" on page 421	00000000h
203Ch	203Fh	"Event Ring Dequeue Pointer High 1 (ERDP_HI1)—Offset 203Ch" on page 422	00000000h
2040h	2043h	"Interrupter 2 Management (IMAN2)—Offset 2040h" on page 422	00000000h
2044h	2047h	"Interrupter 2 Moderation (IMOD2)—Offset 2044h" on page 423	00000FA0h
2048h	204Bh	"Event Ring Segment Table Size 2 (ERSTSZ2)—Offset 2048h" on page 423	00000000h
2050h	2053h	"Event Ring Segment Table Base Address Low 2 (ERSTBA_LO2)—Offset 2050h" on page 424	00000000h
2054h	2057h	"Event Ring Segment Table Base Address High 2 (ERSTBA_HI2)—Offset 2054h" on page 424	00000000h
2058h	205Bh	"Event Ring Dequeue Pointer Low 2 (ERDP_LO2)—Offset 2058h" on page 425	00000000h
205Ch	205Fh	"Event Ring Dequeue Pointer High 2 (ERDP_HI2)—Offset 205Ch" on page 425	00000000h
2060h	2063h	"Interrupter 3 Management (IMAN3)—Offset 2060h" on page 426	00000000h
2064h	2067h	"Interrupter 3 Moderation (IMOD3)—Offset 2064h" on page 426	00000FA0h
2068h	206Bh	"Event Ring Segment Table Size 3 (ERSTSZ3)—Offset 2068h" on page 427	00000000h
2070h	2073h	"Event Ring Segment Table Base Address Low 3 (ERSTBA_LO3)—Offset 2070h" on page 427	00000000h
2074h	2077h	"Event Ring Segment Table Base Address High 3 (ERSTBA_HI3)—Offset 2074h" on page 428	00000000h
2078h	207Bh	"Event Ring Dequeue Pointer Low 3 (ERDP_LO3)—Offset 2078h" on page 428	00000000h
207Ch	207Fh	"Event Ring Dequeue Pointer High 3 (ERDP_HI3)—Offset 207Ch" on page 429	00000000h
2080h	2083h	"Interrupter 4 Management (IMAN4)—Offset 2080h" on page 429	00000000h
2084h	2087h	"Interrupter 4 Moderation (IMOD4)—Offset 2084h" on page 430	00000FA0h
2088h	208Bh	"Event Ring Segment Table Size 4 (ERSTSZ4)—Offset 2088h" on page 430	00000000h
2090h	2093h	"Event Ring Segment Table Base Address Low 4 (ERSTBA_LO4)—Offset 2090h" on page 431	00000000h
2094h	2097h	"Event Ring Segment Table Base Address High 4 (ERSTBA_HI4)—Offset 2094h" on page 431	00000000h

Table 120. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset Start	Offset End	Register ID—Description	Default Value
2098h	209Bh	"Event Ring Dequeue Pointer Low 4 (ERDP_LO4)—Offset 2098h" on page 432	00000000h
209Ch	209Fh	"Event Ring Dequeue Pointer High 4 (ERDP_HI4)—Offset 209Ch" on page 432	00000000h
20A0h	20A3h	"Interrupter 5 Management (IMAN5)—Offset 20A0h" on page 433	00000000h
20A4h	20A7h	"Interrupter 5 Moderation (IMOD5)—Offset 20A4h" on page 433	00000FA0h
20A8h	20ABh	"Event Ring Segment Table Size 5 (ERSTSZ5)—Offset 20A8h" on page 434	00000000h
20B0h	20B3h	"Event Ring Segment Table Base Address Low 5 (ERSTBA_LO5)—Offset 20B0h" on page 434	00000000h
20B4h	20B7h	"Event Ring Segment Table Base Address High 5 (ERSTBA_HI5)—Offset 20B4h" on page 435	00000000h
20B8h	20BBh	"Event Ring Dequeue Pointer Low 5 (ERDP_LO5)—Offset 20B8h" on page 435	00000000h
20BCh	20BFh	"Event Ring Dequeue Pointer High 5 (ERDP_HI5)—Offset 20BCh" on page 436	00000000h
20C0h	20C3h	"Interrupter 6 Management (IMAN6)—Offset 20C0h" on page 436	00000000h
20C4h	20C7h	"Interrupter 6 Moderation (IMOD6)—Offset 20C4h" on page 437	00000FA0h
20C8h	20CBh	"Event Ring Segment Table Size 6 (ERSTSZ6)—Offset 20C8h" on page 437	00000000h
20D0h	20D3h	"Event Ring Segment Table Base Address Low 6 (ERSTBA_LO6)—Offset 20D0h" on page 438	00000000h
20D4h	20D7h	"Event Ring Segment Table Base Address High 6 (ERSTBA_HI6)—Offset 20D4h" on page 438	00000000h
20D8h	20DBh	"Event Ring Dequeue Pointer Low 6 (ERDP_LO6)—Offset 20D8h" on page 439	00000000h
20DCh	20DFh	"Event Ring Dequeue Pointer High 6 (ERDP_HI6)—Offset 20DCh" on page 439	00000000h
20E0h	20E3h	"Interrupter 7 Management (IMAN7)—Offset 20E0h" on page 440	00000000h
20E4h	20E7h	"Interrupter 7 Moderation (IMOD7)—Offset 20E4h" on page 440	00000FA0h
20E8h	20EBh	"Event Ring Segment Table Size 7 (ERSTSZ7)—Offset 20E8h" on page 441	00000000h
20F0h	20F3h	"Event Ring Segment Table Base Address Low 7 (ERSTBA_LO7)—Offset 20F0h" on page 441	00000000h
20F4h	20F7h	"Event Ring Segment Table Base Address High 7 (ERSTBA_HI7)—Offset 20F4h" on page 442	00000000h
20F8h	20FBh	"Event Ring Dequeue Pointer Low 7 (ERDP_LO7)—Offset 20F8h" on page 442	00000000h
20FCh	20FFh	"Event Ring Dequeue Pointer High 7 (ERDP_HI7)—Offset 20FCh" on page 443	00000000h
2100h	2103h	"Interrupter 8 Management (IMAN8)—Offset 2100h" on page 443	00000000h
2104h	2107h	"Interrupter 8 Moderation (IMOD8)—Offset 2104h" on page 444	00000FA0h
2108h	210Bh	"Event Ring Segment Table Size 8 (ERSTSZ8)—Offset 2108h" on page 444	00000000h
2110h	2113h	"Event Ring Segment Table Base Address Low 8 (ERSTBA_LO8)—Offset 2110h" on page 445	00000000h
2114h	2117h	"Event Ring Segment Table Base Address High 8 (ERSTBA_HI8)—Offset 2114h" on page 445	00000000h
2118h	211Bh	"Event Ring Dequeue Pointer Low 8 (ERDP_LO8)—Offset 2118h" on page 446	00000000h
211Ch	211Fh	"Event Ring Dequeue Pointer High 8 (ERDP_HI8)—Offset 211Ch" on page 446	00000000h
3000h	3003h	"Door Bell 1 (DOORBELL1)—Offset 3000h" on page 447	00000000h
3004h	3007h	"Door Bell 2 (DOORBELL2)—Offset 3004h" on page 447	00000000h
3008h	300Bh	"Door Bell 3 (DOORBELL3)—Offset 3008h" on page 448	00000000h
300Ch	300Fh	"Door Bell 4 (DOORBELL4)—Offset 300Ch" on page 448	00000000h

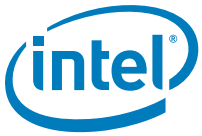


Table 120. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset Start	Offset End	Register ID—Description	Default Value
3010h	3013h	"Door Bell 5 (DOORBELL5)—Offset 3010h" on page 449	00000000h
3014h	3017h	"Door Bell 6 (DOORBELL6)—Offset 3014h" on page 450	00000000h
3018h	301Bh	"Door Bell 7 (DOORBELL7)—Offset 3018h" on page 450	00000000h
301Ch	301Fh	"Door Bell 8 (DOORBELL8)—Offset 301Ch" on page 451	00000000h
3020h	3023h	"Door Bell 9 (DOORBELL9)—Offset 3020h" on page 451	00000000h
3024h	3027h	"Door Bell 10 (DOORBELL10)—Offset 3024h" on page 452	00000000h
3028h	302Bh	"Door Bell 11 (DOORBELL11)—Offset 3028h" on page 453	00000000h
302Ch	302Fh	"Door Bell 12 (DOORBELL12)—Offset 302Ch" on page 453	00000000h
3030h	3033h	"Door Bell 13 (DOORBELL13)—Offset 3030h" on page 454	00000000h
3034h	3037h	"Door Bell 14 (DOORBELL14)—Offset 3034h" on page 455	00000000h
3038h	303Bh	"Door Bell 15 (DOORBELL15)—Offset 3038h" on page 455	00000000h
303Ch	303Fh	"Door Bell 16 (DOORBELL16)—Offset 303Ch" on page 456	00000000h
3040h	3043h	"Door Bell 17 (DOORBELL17)—Offset 3040h" on page 456	00000000h
3044h	3047h	"Door Bell 18 (DOORBELL18)—Offset 3044h" on page 457	00000000h
3048h	304Bh	"Door Bell 19 (DOORBELL19)—Offset 3048h" on page 458	00000000h
304Ch	304Fh	"Door Bell 20 (DOORBELL20)—Offset 304Ch" on page 458	00000000h
3050h	3053h	"Door Bell 21 (DOORBELL21)—Offset 3050h" on page 459	00000000h
3054h	3057h	"Door Bell 22 (DOORBELL22)—Offset 3054h" on page 459	00000000h
3058h	305Bh	"Door Bell 23 (DOORBELL23)—Offset 3058h" on page 460	00000000h
305Ch	305Fh	"Door Bell 24 (DOORBELL24)—Offset 305Ch" on page 461	00000000h
3060h	3063h	"Door Bell 25 (DOORBELL25)—Offset 3060h" on page 461	00000000h
3064h	3067h	"Door Bell 26 (DOORBELL26)—Offset 3064h" on page 462	00000000h
3068h	306Bh	"Door Bell 27 (DOORBELL27)—Offset 3068h" on page 462	00000000h
306Ch	306Fh	"Door Bell 28 (DOORBELL28)—Offset 306Ch" on page 463	00000000h
3070h	3073h	"Door Bell 29 (DOORBELL29)—Offset 3070h" on page 464	00000000h
3074h	3077h	"Door Bell 30 (DOORBELL30)—Offset 3074h" on page 464	00000000h
3078h	307Bh	"Door Bell 31 (DOORBELL31)—Offset 3078h" on page 465	00000000h
307Ch	307Fh	"Door Bell 32 (DOORBELL32)—Offset 307Ch" on page 465	00000000h
8000h	8003h	"XECP_SUPP_USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h" on page 466	02000802h
8004h	8007h	"XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h" on page 467	20425355h
8008h	800Bh	"XECP_SUPP_USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h" on page 467	30190601h
8010h	8013h	"XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h" on page 468	000C0021h
8014h	8017h	"XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h" on page 469	05DC0012h
8018h	801Bh	"XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h" on page 469	01E00023h
8020h	8023h	"XECP_SUPP_USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h" on page 470	03000802h
8024h	8027h	"XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h" on page 471	20425355h
8028h	802Bh	"XECP_SUPP_USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h" on page 471	10000107h

Table 120. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset Start	Offset End	Register ID—Description	Default Value
8030h	8033h	"XECP_SUPP_USB3_3 (XECP_SUPP_USB3_3)—Offset 8030h" on page 472	00050134h
8040h	8043h	"XECP_CMDM_STS0 (XECP_CMDM_STS0)—Offset 8040h" on page 472	00000CC1h
8044h	8047h	"XECP_CMDM_STS1 (XECP_CMDM_STS1)—Offset 8044h" on page 474	03FC0000h
8048h	804Bh	"XECP_CMDM_STS2 (XECP_CMDM_STS2)—Offset 8048h" on page 475	00000000h
804Ch	804Fh	"XECP_CMDM_STS3 (XECP_CMDM_STS3)—Offset 804Ch" on page 475	00000000h
8050h	8053h	"XECP_CMDM_STS4 (XECP_CMDM_STS4)—Offset 8050h" on page 476	00000000h
8054h	8057h	"XECP_CMDM_STS5 (XECP_CMDM_STS5)—Offset 8054h" on page 476	00000000h
8058h	805Bh	"Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h" on page 477	3500AFFCh
8070h	8073h	"Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h" on page 477	0000FCC0h
8078h	807Bh	"Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h" on page 477	00000000h
807Ch	807Fh	"Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch" on page 478	00000000h
8080h	8083h	"Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h" on page 479	00000000h
8084h	8087h	"Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h" on page 480	00000000h
8094h	8097h	"Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h" on page 480	00008100h
8098h	809Bh	"Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h" on page 481	14003002h
80A0h	80A3h	"Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h" on page 481	00003C0Fh
80C0h	80C3h	"AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h" on page 482	015FC0F0h
80C4h	80C7h	"Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h" on page 484	004A4008h
80C8h	80CBh	"High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h" on page 485	0001A01Fh
80CCh	80CFh	"Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh" on page 486	00014080h
80D0h	80D3h	"System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h" on page 487	00032010h
80D4h	80D7h	"Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h" on page 488	00000000h
80D8h	80DBh	"AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 80D8h" on page 489	00000000h
80E0h	80E3h	"AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h" on page 490	808DBCA0h
80E4h	80E7h	"Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h" on page 492	00000000h
80E8h	80EBh	"Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h" on page 493	00800080h
80ECh	80EFh	"SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh" on page 493	18010600h
80F0h	80F3h	"USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h" on page 495	310003A0h
80F4h	80F7h	"USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h" on page 497	80C40620h
80F8h	80FBh	"USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h" on page 498	F865EB6Bh
80FCh	80FFh	"USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh" on page 499	00008003h
8100h	8103h	"Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h" on page 500	00008008h

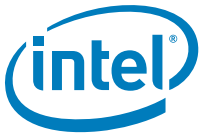


Table 120. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset Start	Offset End	Register ID—Description	Default Value
8108h	810Bh	"Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h" on page 500	00000001h
810Ch	810Fh	"Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch" on page 501	00008020h
8110h	8113h	"USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h" on page 502	F0EC838Ch
8128h	812Fh	"USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h" on page 502	0F425285056 47F00h
8130h	8133h	"USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h" on page 502	00000000h
8134h	813Bh	"USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h" on page 504	000C3C640C0 5140Ch
813Ch	813Fh	"USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch" on page 505	8D4258B8h
8140h	8143h	"Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h" on page 506	0A019132h
8144h	8147h	"Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h" on page 506	0000033Fh
8150h	8153h	"Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8150h" on page 508	00000000h
8154h	8157h	"AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h" on page 508	01390206h
8164h	8167h	"USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h" on page 511	000000FCh
8168h	816Bh	"USB Power Gating Control (USB_PGC)—Offset 8168h" on page 512	00000000h
816Ch	816Fh	"xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch" on page 513	00000400h
8170h	8173h	"USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h" on page 514	00090032h
8174h	8177h	"xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h" on page 516	0040047Dh
8178h	817Bh	"xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h" on page 517	000017FFh
817Ch	817Fh	"xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch" on page 518	00000000h
8180h	8183h	"xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h" on page 519	00000000h
8184h	8187h	"xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h" on page 520	00000000h
8344h	8347h	"USB EP Type Lock Policy (USB_EP_TLP)—Offset 8344h" on page 521	00000000h
8348h	834Bh	"USB EP Type Lock Policy - Port Control 1 (USB_EP_TLP1)—Offset 8348h" on page 523	00000000h
834Ch	834Fh	"USB EP Type Lock Policy - Port Control 2 (USB_EP_TLP2)—Offset 834Ch" on page 525	00000000h
8460h	8463h	"USB Legacy Support Capability (USBLEGSUP)—Offset 8460h" on page 526	00000801h
8464h	8467h	"USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8464h" on page 527	00000000h
8480h	8483h	"Debug Capability ID Register (DCID)—Offset 8480h" on page 528	0005000Ah
8484h	8487h	"Debug Capability Doorbell Register (DCDB)—Offset 8484h" on page 528	00000000h
8488h	848Bh	"Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8488h" on page 529	00000000h
8490h	8497h	"Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8490h" on page 530	00000000000 00000h

Table 120. Summary of USB xHCI Memory Mapped I/O Registers—MBAR (Continued)

Offset Start	Offset End	Register ID—Description	Default Value
8498h	849Fh	"Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8498h" on page 530	0000000000000000h
84A0h	84A3h	"Debug Capability Control Register (DCCTRL)—Offset 84A0h" on page 531	00000000h
84A4h	84A7h	"Debug Capability Status Register (DCST)—Offset 84A4h" on page 532	00000000h
84A8h	84ABh	"Debug Capability Port Status and Control Register (DCPORTSC)—Offset 84A8h" on page 532	00000000h
84B0h	84B7h	"Debug Capability Context Pointer Register (DCCP)—Offset 84B0h" on page 534	0000000000000000h
84B8h	84BBh	"Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 84B8h" on page 534	00000000h
84BCh	84BFh	"Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 84BCh" on page 535	00000000h
8530h	8533h	"Debug Capability Descriptor Parameters (DCDP)—Offset 8530h" on page 535	00000000h
8534h	8537h	"Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8538h" on page 536	0C101105h
8538h	853Bh	"Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8538h" on page 536	00000000h
853Ch	853Fh	"" on page 536	00000000h

14.7.1 Capability Registers Length (CAPLENGTH)—Offset 0h

This register is modified and maintained by BIOS

Access Method

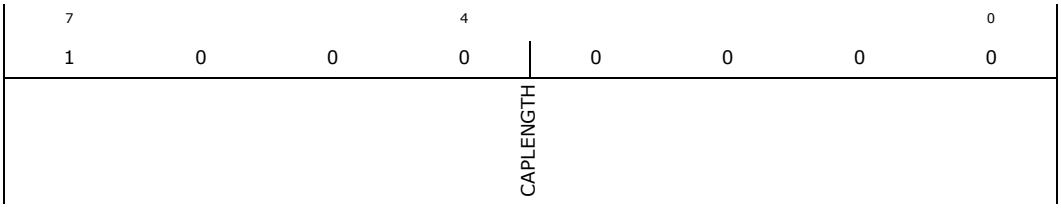
Type: Memory Mapped I/O Register (Size: 8 bits)

CAPLENGTH: [MBAR] + 0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 80h



Bit Range	Default & Access	Description
7: 0	80h RW/L	**Capability Registers Length (CAPLENGTH):** Reserved.

14.7.2 Host Controller Interface Version Number (HCIVERSION)—Offset 2h

This register is modified and maintained by BIOS

Access Method

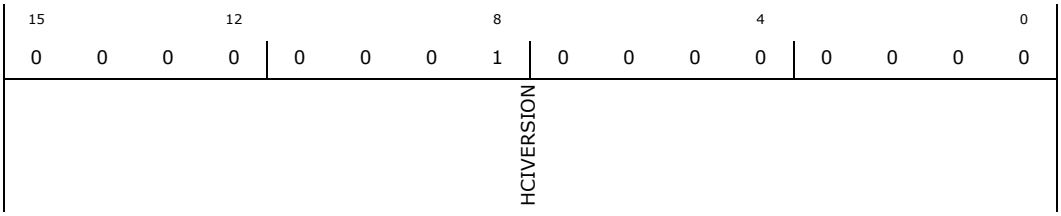
Type: Memory Mapped I/O Register (Size: 16 bits)

HCIVERSION: [MBAR] + 2h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0100h



Bit Range	Default & Access	Description
15: 0	0100h RO	**Host Controller Interface Version Number (HCIVERSION):** Reserved.

14.7.3 Structural Parameters 1 (HCSPARAMS1)—Offset 4h

This register is modified and maintained by BIOS

Access Method

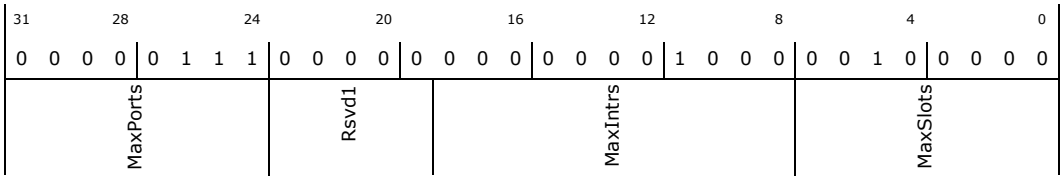
Type: Memory Mapped I/O Register (Size: 32 bits)

HCSPARAMS1: [MBAR] + 4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 07000820h



Bit Range	Default & Access	Description
31: 24	07h RO	**Number of Ports (MaxPorts):** Reserved.
23: 19	00h RW/L	**Rsvd1 (Rsvd1):** Reserved.
18: 8	008h RW/L	**Number of Interrupters (MaxIntrs):** Reserved.
7: 0	20h RW/L	**Number of Device Slots (MaxSlots):** Reserved.

14.7.4 Structural Parameters 2 (HCSPARAMS2)—Offset 8h

This register is modified and maintained by BIOS

Access Method

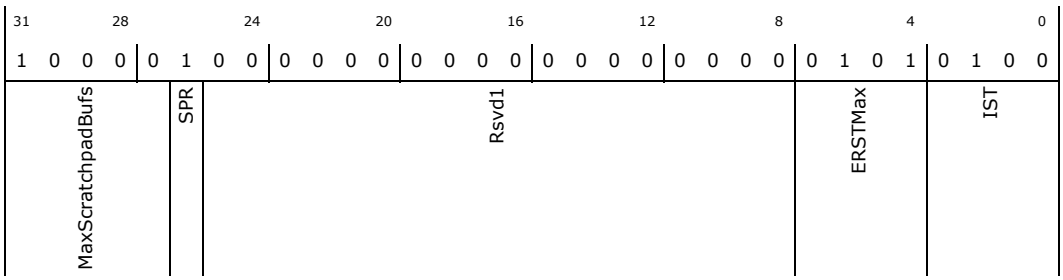
Type: Memory Mapped I/O Register (Size: 32 bits)

HCSPARAMS2: [MBAR] + 8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 84000054h



Bit Range	Default & Access	Description
31: 27	10h RW/L	**Max Scratchpad Buffers (MaxScratchpadBufs):** Reserved.
26	1b RW/L	**Scratchpad Restore (SPR):** Reserved.
25: 8	00000h RW/L	**Rsvd1 (Rsvd1):** Reserved.
7: 4	5h RW/L	**Event Ring Segment Table Max (ERSTMax):** Reserved.
3: 0	4h RW/L	**Isochronous Scheduling Threshold (IST):** Reserved.

14.7.5 Structural Parameters 3 (HCSPARAMS3)—Offset Ch

This register is modified and maintained by BIOS

Access Method

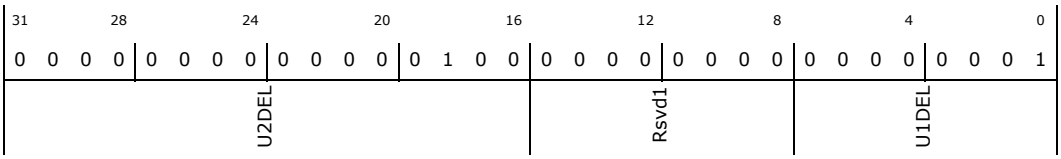
Type: Memory Mapped I/O Register (Size: 32 bits)

HCSPARAMS3: [MBAR] + Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00040001h



Bit Range	Default & Access	Description
31: 16	0004h RW/L	**U2 Device Exit Latency (U2DEL):** Reserved.
15: 8	00h RW/L	**Rsvd1 (Rsvd1):** Reserved.
7: 0	01h RW/L	**U1 Device Exit Latency (U1DEL):** Reserved.

14.7.6 Capability Parameters (HCCPARAMS)—Offset 10h

This register is modified and maintained by BIOS

Access Method

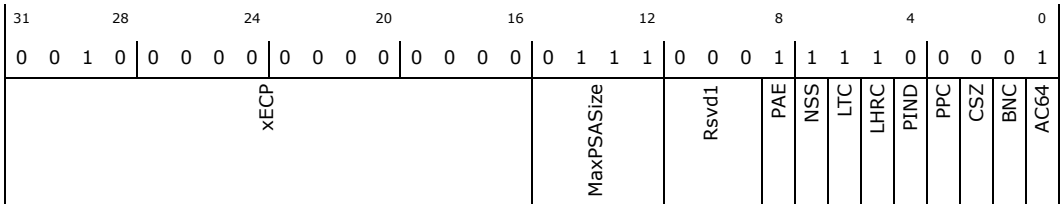
Type: Memory Mapped I/O Register (Size: 32 bits)

HCCPARAMS: [MBAR] + 10h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 200071E1h



Bit Range	Default & Access	Description
31: 16	2000h RW/L	**xHCI Extended Capabilities Pointer (xECP):** Reserved.
15: 12	7h RW/L	**Maximum Primary Stream Array Size (MaxPSASize):** Reserved.
11: 9	0h RW/L	**Rsvd1 (Rsvd1):** Reserved.
8	1b RW/L	**Parst All Event Data (PAE):** Reserved.
7	1b RW/L	**No Secondary SID Support (NSS):** Reserved.
6	1b RW/L	**Latency Tolerance Messaging Capability (LTC):** Reserved.
5	1b RW/L	**Light HC Reset Capability (LHRC):** Reserved.
4	0b RW/L	**Port Indicators (PIND):** Reserved.
3	0b RO	**Port Power Control (PPC):** Reserved.
2	0b RW/L	**Context Size (CSZ):** Reserved.
1	0b RW/L	**BW Negotiation Capability (BNC):** Reserved.
0	1b RW/L	**64-bit Addressing Capability (AC64):** Reserved.

14.7.7 Doorbell Offset (DBOFF)—Offset 14h

Access Method

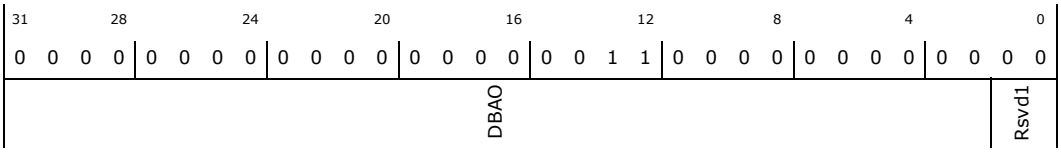
Type: Memory Mapped I/O Register (Size: 32 bits)

DBOFF: [MBAR] + 14h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00003000h



Bit Range	Default & Access	Description
31: 2	00000C00h RO	**Doorbell Array Offset (DBAO):** Reserved.
1: 0	0h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.8 Runtime Register Space Offset (RTSOFF)—Offset 18h

Access Method

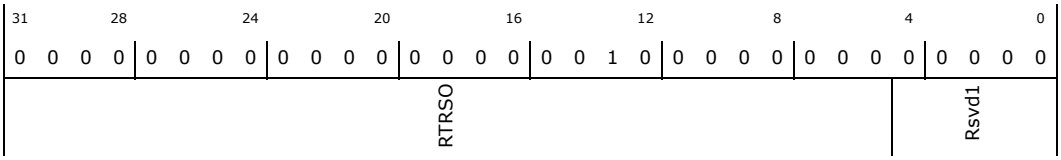
Type: Memory Mapped I/O Register (Size: 32 bits)

RTSOFF: [MBAR] + 18h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00002000h



Bit Range	Default & Access	Description
31: 5	0000100h RO	**Runtime Register Space Offset (RTRSO):** Reserved.
4: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.9 USB Command (USBCMD)—Offset 80h

Access Method

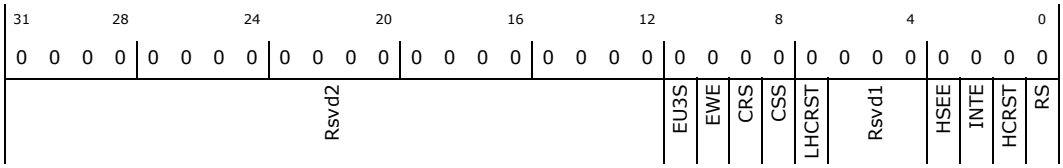
Type: Memory Mapped I/O Register (Size: 32 bits)

USBCMD: [MBAR] + 80h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 12	00000h RO	**Rsvd2 (Rsvd2):** Reserved.
11	0b RW	**Enable U3 MFINDEX Stop (EU3S):** Reserved.
10	0b RW	**Enable Wrap Event (EWE):** Reserved.
9	0b RW	**Controller Restore State (CRS):** Reserved.
8	0b RW	**Controller Save State (CSS):** Reserved.
7	0b RW	**Light Host Controller Reset (LHCRST):** Reserved.
6: 4	0h RO	**Rsvd1 (Rsvd1):** Reserved.
3	0b RW	**Host System Error Enable (HSEE):** Reserved.
2	0b RW	**Interrupter Enable (INTE):** Reserved.
1	0b RW	**Host Controller Reset (HCRST):** Reserved.
0	0b RW	**Run/Stop (RS):** Reserved.

14.7.10 USB Status (USBSTS)—Offset 84h

Access Method

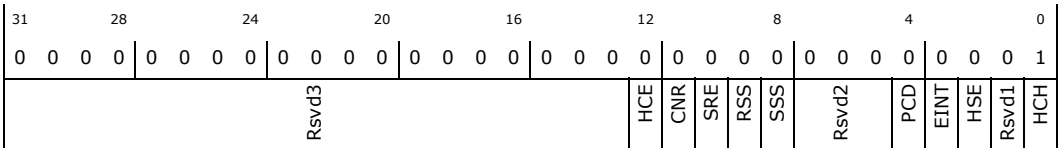
Type: Memory Mapped I/O Register (Size: 32 bits)

USBSTS: [MBAR] + 84h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000001h



Bit Range	Default & Access	Description
31: 13	00000h RO	**Rsvd3 (Rsvd3):** Reserved.
12	0b RO	**Host Controller Error (HCE):** This bit is not preset in HC, this is deviation from XHCI 1.0 spec.
11	0b RO	**Controller Not Ready (CNR):** This is deviation from XHCI 1.0 spec.
10	0b RW/C	**Save/Restore Error (SRE):** Reserved.
9	0b RO	**Restore State Status (RSS):** Reserved.
8	0b RO	**Save State Status (SSS):** Reserved.
7: 5	0h RO	**Rsvd2 (Rsvd2):** Reserved.
4	0b RW/C	**Port Change Detect (PCD):** Reserved.
3	0b RW/C	**Event Interrupt (EINT):** Reserved.
2	0b RW/C	**Host System Error (HSE):** Reserved.
1	0b RO	**Rsvd1 (Rsvd1):** Reserved.
0	1b RO	**HCHalted (HCH):** Reserved.

14.7.11 Page Size (PAGESIZE)—Offset 88h

Access Method

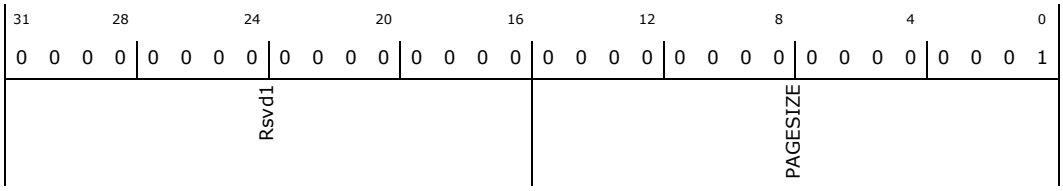
Type: Memory Mapped I/O Register (Size: 32 bits)

PAGESIZE: [MBAR] + 88h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000001h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0001h RO	**Page Size (PAGESIZE):** Reserved.

14.7.12 Device Notification Control (DNCTRL)—Offset 94h

Access Method

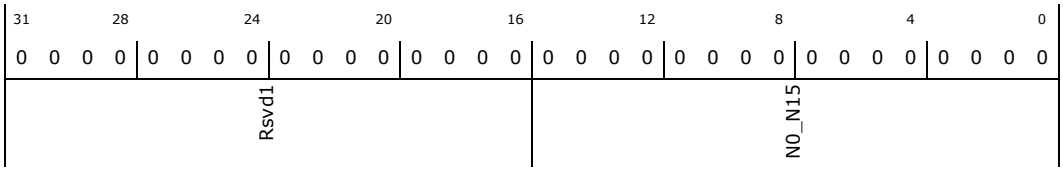
Type: Memory Mapped I/O Register (Size: 32 bits)

DNCTRL: [MBAR] + 94h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RW	**Notification Enable (N0_N15):** Reserved.

14.7.13 Command Ring Low (CRCR_LO)—Offset 98h

Access Method

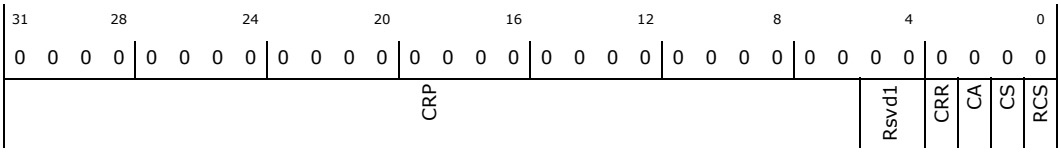
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCR_LO: [MBAR] + 98h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Command Ring Pointer (CRP):** Reserved.
5: 4	0h RO	**Rsvd1 (Rsvd1):** Reserved.
3	0b RO	**Command Ring Running (CRR):** Reserved.
2	0b RW/S	**Command Abort (CA):** Reserved.
1	0b RW/S	**Command Stop (CS):** Reserved.
0	0b RW	**Ring Cycle State (RCS):** Reserved.

14.7.14 Command Ring High (CRCR_HI)—Offset 9Ch

Access Method

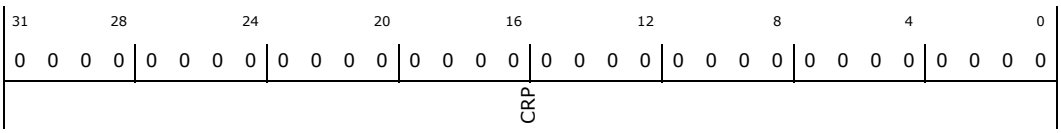
Type: Memory Mapped I/O Register (Size: 32 bits)

CRCR_HI: [MBAR] + 9Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Command Ring Pointer (CRP):** Reserved.

14.7.15 Device Context Base Address Array Pointer Low (DCBAAP_LO)—Offset B0h

Access Method

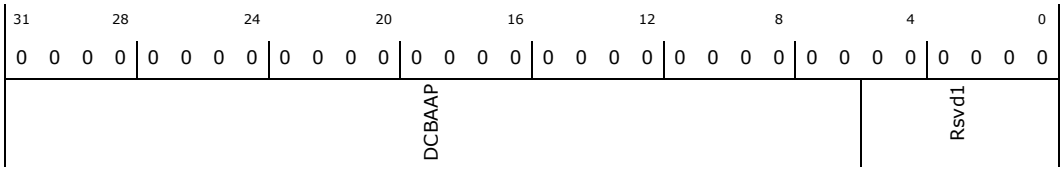
Type: Memory Mapped I/O Register (Size: 32 bits)

DCBAAP_LO: [MBAR] + B0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Device Context Base Address Array Pointer (DCBAAP):** Reserved.
5: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.16 Device Context Base Address Array Pointer High (DCBAAP_HI)—Offset B4h

Access Method

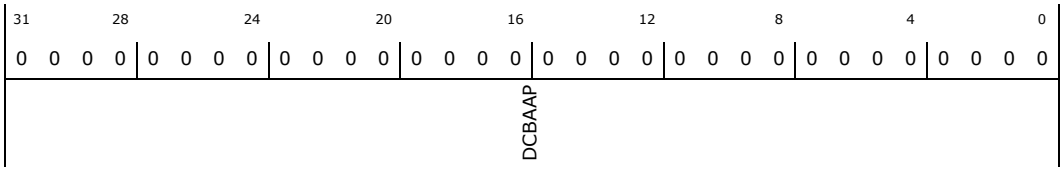
Type: Memory Mapped I/O Register (Size: 32 bits)

DCBAAP_HI: [MBAR] + B4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Device Context Base Address Array Pointer (DCBAAP):** Reserved.

14.7.17 Configure (CONFIG)—Offset B8h

Access Method

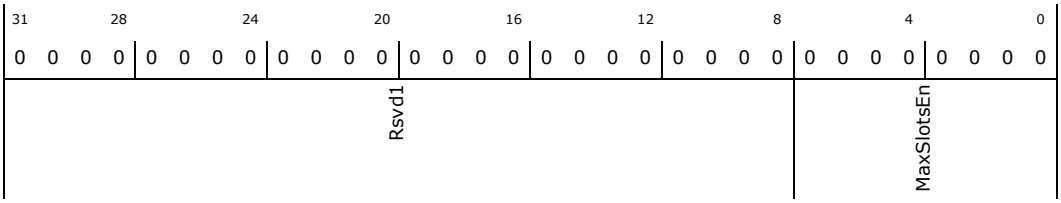
Type: Memory Mapped I/O Register (Size: 32 bits)

CONFIG: [MBAR] + B8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 8	000000h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**Max Device Slots Enabled (MaxSlotsEn):** Reserved.

14.7.18 Port 1 Status and Control USB3 (PORTSC1USB2)—Offset 480h

Access Method

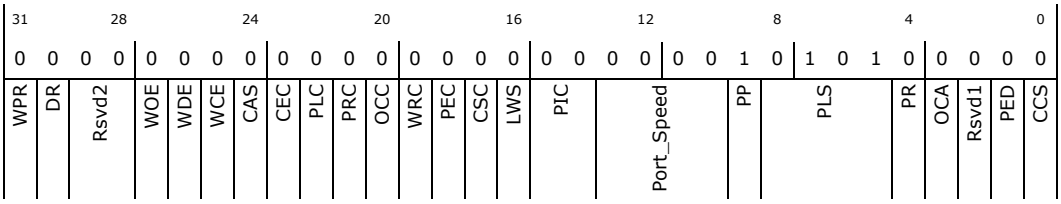
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC1USB2: [MBAR] + 480h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 000002A0h



Bit Range	Default & Access	Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved.
30	0b RO	**Device Removable (DR):** Reserved.
29: 28	0h RO	**Rsvd2 (Rsvd2):** Reserved.

Bit Range	Default & Access	Description
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0b RO	**Cold Attach Status (CAS):** Reserved.
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved.
15: 14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13: 10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky.
9	1b RW	**Port Power (PP):** Note: This register is sticky.
8: 5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0b RW/S	**Port Reset (PR):** Reserved.
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0b RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky.

14.7.19 Port 1 Power Management Status and Control USB2 (PORTPMSC1USB2)—Offset 484h

Access Method

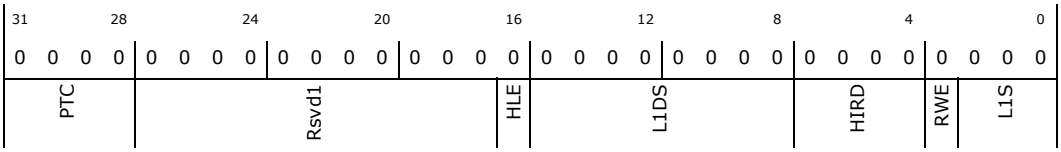
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTPMSC1USB2: [MBAR] + 484h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31: 28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27: 17	000h RO	**Rsvd1 (Rsvd1):** Reserved.
16	0b RO	**Hardware LPM Enable (HLE):** Reserved.
15: 8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky.
7: 4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2: 0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

14.7.20 Port X Hardware LPM Control Register (PORTHLPM1)—Offset 48Ch

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

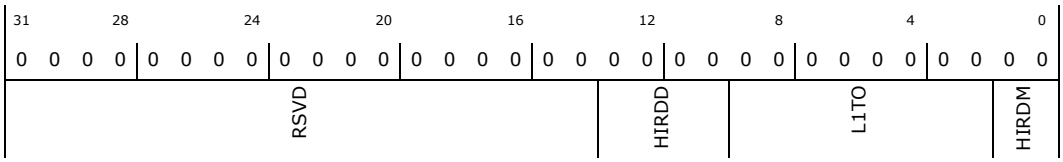
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTHLPM1: [MBAR] + 48Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 14	00000h RO	**RESERVED (RSVD):** Reserved.
13: 10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9: 2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1: 0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

14.7.21 Port 2 Status and Control USB3 (PORTSC2USB2)—Offset 490h

Access Method

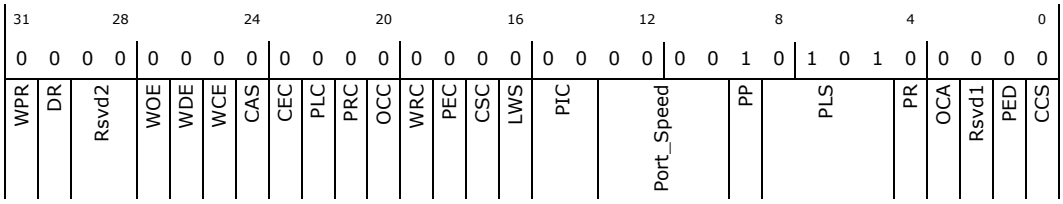
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC2USB2: [MBAR] + 490h

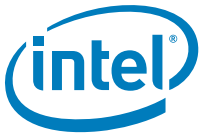
MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 000002A0h



Bit Range	Default & Access	Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved.
30	0b RO	**Device Removable (DR):** Reserved.
29: 28	0h RO	**Rsvd2 (Rsvd2):** Reserved.
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.



Bit Range	Default & Access	Description
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0b RO	**Cold Attach Status (CAS):** Reserved.
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved.
15: 14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13: 10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky.
9	1b RW	**Port Power (PP):** Note: This register is sticky.
8: 5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0b RW/S	**Port Reset (PR):** Reserved.
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0b RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky.

14.7.22 Port 2 Power Management Status and Control USB2 (PORTPMSC2USB2)—Offset 494h

Access Method

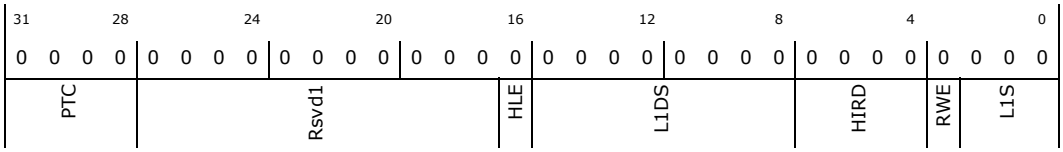
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTPMSC2USB2: [MBAR] + 494h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31: 28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27: 17	000h RO	**Rsvd1 (Rsvd1):** Reserved.
16	0b RO	**Hardware LPM Enable (HLE):** Reserved.
15: 8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky.
7: 4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2: 0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

14.7.23 Port X Hardware LPM Control Register (PORTHLPM2)—Offset 49Ch

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

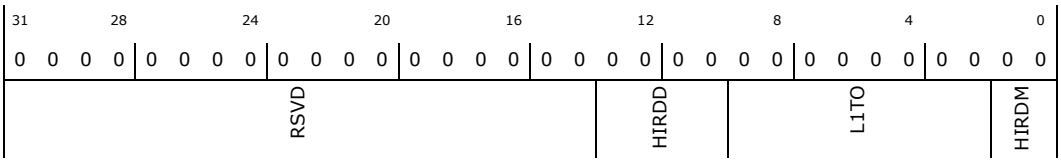
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTHLPM2: [MBAR] + 49Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 14	00000h RO	**RESERVED (RSVD):** Reserved.
13: 10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9: 2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1: 0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

14.7.24 Port 3 Status and Control USB3 (PORTSC3USB2)—Offset 4A0h

Access Method

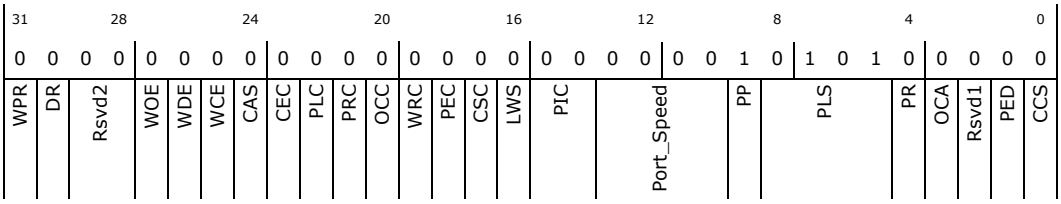
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC3USB2: [MBAR] + 4A0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 000002A0h



Bit Range	Default & Access	Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved.
30	0b RO	**Device Removable (DR):** Reserved.
29: 28	0h RO	**Rsvd2 (Rsvd2):** Reserved.
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.

Bit Range	Default & Access	Description
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0b RO	**Cold Attach Status (CAS):** Reserved.
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved.
15: 14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13: 10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky.
9	1b RW	**Port Power (PP):** Note: This register is sticky.
8: 5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0b RW/S	**Port Reset (PR):** Reserved.
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0b RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky.

14.7.25 Port 3 Power Management Status and Control USB2 (PORTPMSC3USB2)—Offset 4A4h

Access Method

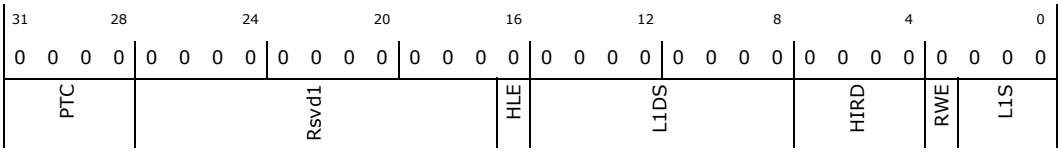
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTPMSC3USB2: [MBAR] + 4A4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31: 28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27: 17	000h RO	**Rsvd1 (Rsvd1):** Reserved.
16	0b RO	**Hardware LPM Enable (HLE):** Reserved.
15: 8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky.
7: 4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2: 0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

14.7.26 Port X Hardware LPM Control Register (PORTHLPM3)—Offset 4ACh

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

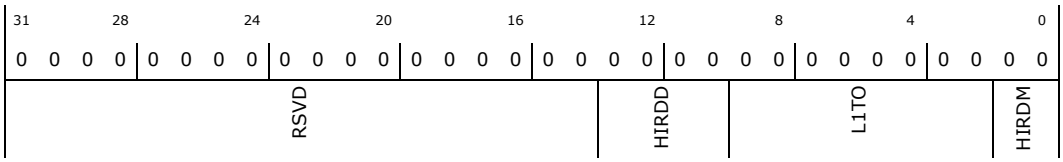
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTHLPM3: [MBAR] + 4ACh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 14	00000h RO	**RESERVED (RSVD):** Reserved.
13: 10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9: 2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1: 0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

14.7.27 Port 4 Status and Control USB3 (PORTSC4USB2)—Offset 4B0h

Access Method

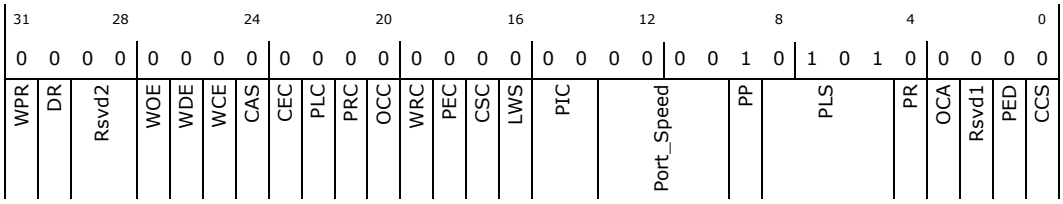
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC4USB2: [MBAR] + 4B0h

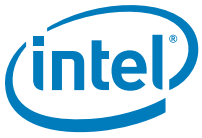
MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 000002A0h



Bit Range	Default & Access	Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved.
30	0b RO	**Device Removable (DR):** Reserved.
29: 28	0h RO	**Rsvd2 (Rsvd2):** Reserved.
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.



Bit Range	Default & Access	Description
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0b RO	**Cold Attach Status (CAS):** Reserved.
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved.
15: 14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13: 10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky.
9	1b RW	**Port Power (PP):** Note: This register is sticky.
8: 5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0b RW/S	**Port Reset (PR):** Reserved.
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0b RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky.

14.7.28 Port 4 Power Management Status and Control USB2 (PORTPMSC4USB2)—Offset 4B4h

Access Method

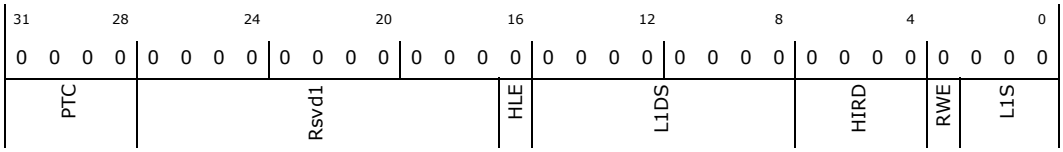
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTPMSC4USB2: [MBAR] + 4B4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31: 28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27: 17	000h RO	**Rsvd1 (Rsvd1):** Reserved.
16	0b RO	**Hardware LPM Enable (HLE):** Reserved.
15: 8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky.
7: 4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2: 0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

14.7.29 Port X Hardware LPM Control Register (PORTHLPM4)—Offset 4BCh

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

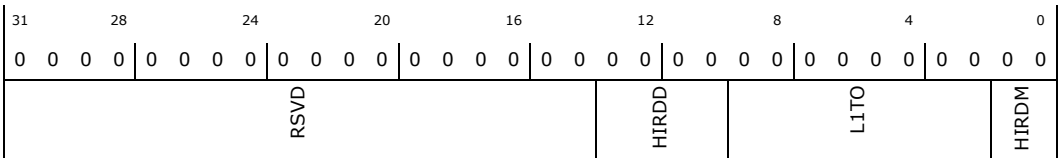
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTHLPM4: [MBAR] + 4BCh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 14	00000h RO	**RESERVED (RSVD):** Reserved.
13: 10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9: 2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1: 0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

14.7.30 Port 8 Status and Control USB2 (PORTSC5USB2)—Offset 4C0h

Access Method

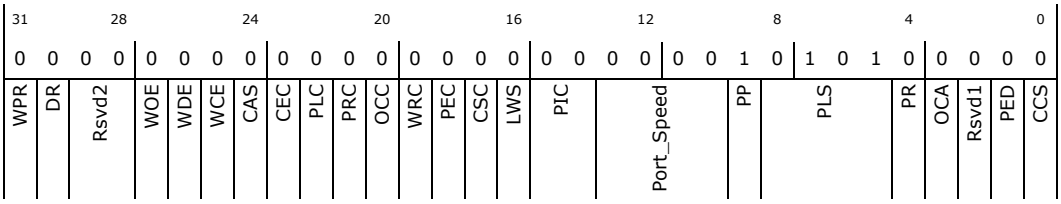
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC5USB2: [MBAR] + 4C0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 000002A0h



Bit Range	Default & Access	Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved.
30	0b RO	**Device Removable (DR):** Reserved.
29: 28	0h RO	**Rsvd2 (Rsvd2):** Reserved.
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.

Bit Range	Default & Access	Description
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0b RO	**Cold Attach Status (CAS):** Reserved.
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved.
15: 14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13: 10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky.
9	1b RW	**Port Power (PP):** Note: This register is sticky.
8: 5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0b RW/S	**Port Reset (PR):** Reserved.
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0b RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky.

14.7.31 Port 5 Power Management Status and Control USB2 (PORTPMSC5USB2)—Offset 4C4h

Access Method

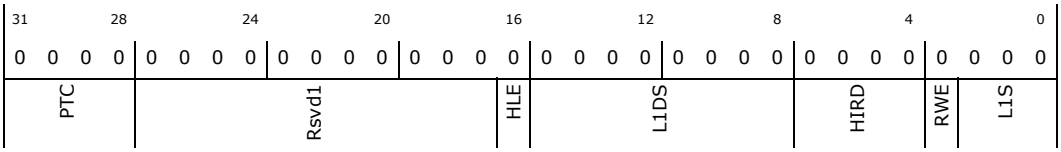
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTPMSC5USB2: [MBAR] + 4C4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31: 28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27: 17	000h RO	**Rsvd1 (Rsvd1):** Reserved.
16	0b RO	**Hardware LPM Enable (HLE):** Reserved.
15: 8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky.
7: 4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2: 0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

14.7.32 Port X Hardware LPM Control Register (PORTHLPM5)—Offset 4CCh

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

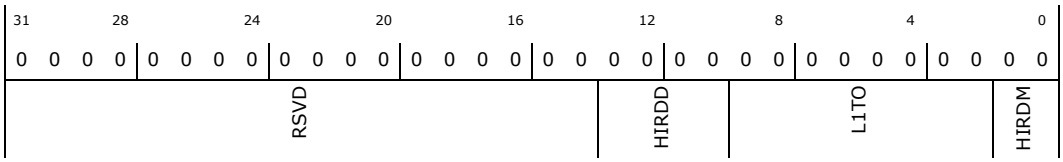
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTHLPM5: [MBAR] + 4CCh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 14	00000h RO	**RESERVED (RSVD):** Reserved.
13: 10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9: 2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1: 0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

14.7.33 Port 6 Status and Control USB2 (PORTSC6USB2)—Offset 4D0h

Access Method

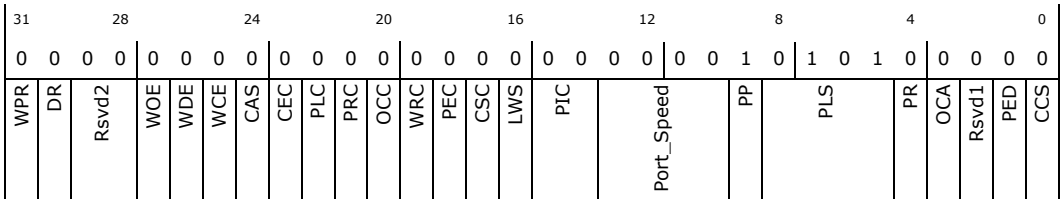
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC6USB2: [MBAR] + 4D0h

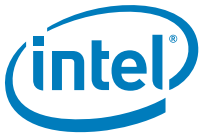
MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 000002A0h



Bit Range	Default & Access	Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved.
30	0b RO	**Device Removable (DR):** Reserved.
29: 28	0h RO	**Rsvd2 (Rsvd2):** Reserved.
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.



Bit Range	Default & Access	Description
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0b RO	**Cold Attach Status (CAS):** Reserved.
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved.
15: 14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13: 10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky.
9	1b RW	**Port Power (PP):** Note: This register is sticky.
8: 5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0b RW/S	**Port Reset (PR):** Reserved.
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0b RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky.

14.7.34 Port 6 Power Management Status and Control USB2 (PORTPMSC6USB2)—Offset 4D4h

Access Method

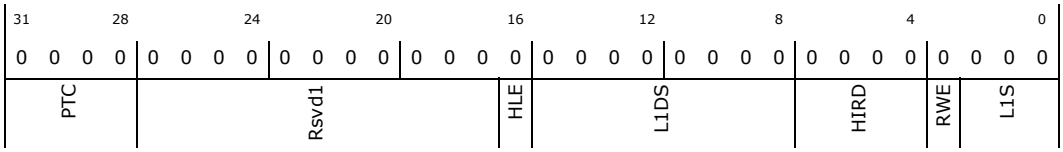
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTPMSC6USB2: [MBAR] + 4D4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31: 28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27: 17	000h RO	**Rsvd1 (Rsvd1):** Reserved.
16	0b RO	**Hardware LPM Enable (HLE):** Reserved.
15: 8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky.
7: 4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2: 0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

14.7.35 Port X Hardware LPM Control Register (PORTHLPM6)—Offset 4DCh

There are 9 PORTHLPM registers at offsets 48Ch, 49Ch, 4ACh, 4BCh, 4CCh, 4DCh, 4ECh, 4FCh, 50Ch This register is reset only by platform hardware during cold reset or in response to a Host Controller Reset (HCRST). The definition for the fields depend on the protocol supported. For USB3 this register is reserved and shall be treated by software as RsvdP. For USB2 the definition is given below. Fields contain parameters neccessary for xHC to automatically generate an LPM Token to the downstream device.

Access Method

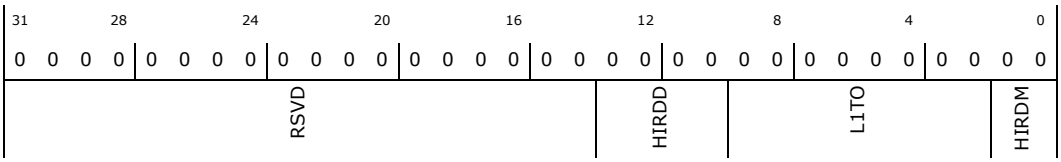
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTHLPM6: [MBAR] + 4DCh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 14	00000h RO	**RESERVED (RSVD):** Reserved.
13: 10	0h RW	**Host Initiated Resume Duration-Deep (HIRDD):** System software sets this field to indicate to the recipient device how long the xHC will drive resume if an exit from L1. The HIRDD value is is encoded as follows: 0h: 50 us (default) 1h: 125 us 2h: 200 us ... Fh: 1.175ms The value of 0h is interpreted as 50 us. Each incrementing value adds 75 us to the previous value.
9: 2	00h RW	**L1 Timeout (L1TO):** Timeout value for L1 inactivity timer. This field shall be set to 00h by assertion of PR to '1'. Following are permissible values: 00h: 128 us (default) 01h: 256 us. ... FFh: 65,280us Note: This register is sticky.
1: 0	0h RW	**Host Initiated Resume Duration Mode (HIRDM):** Indicates which HIRD value should be used. Following are permissible values: 0: Initiate L1 using HIRD only time out (default) 1: Initiate HIRDDon timeout. If rejected by device, initiate L1 using HIRD 2,3: Reserved Note: This register is sticky.

14.7.36 Port 1 Status and Control USB3 (PORTSC1USB3)—Offset 4E0h

Access Method

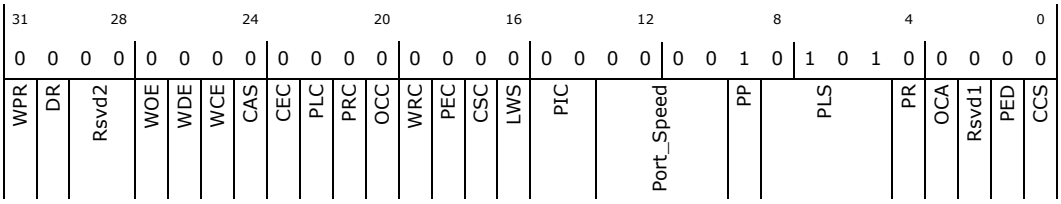
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTSC1USB3: [MBAR] + 4E0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 000002A0h



Bit Range	Default & Access	Description
31	0b RW/S	**Warm Port Reset (WPR):** Reserved.
30	0b RO	**Device Removable (DR):** Reserved.
29: 28	0h RO	**Rsvd2 (Rsvd2):** Reserved.
27	0b RW	**Wake on Over-current Enable (WOE):** Note: This register is sticky.

Bit Range	Default & Access	Description
26	0b RW	**Wake on Disconnect Enable (WDE):** Note: This register is sticky.
25	0b RW	**Wake on Connect Enable (WCE):** Note: This register is sticky.
24	0b RO	**Cold Attach Status (CAS):** Reserved.
23	0b RW/C	**Port Config Error Change (CEC):** Note: This register is sticky.
22	0b RW/C	**Port Link State Change (PLC):** Note: This register is sticky.
21	0b RW/C	**Port Reset Change (PRC):** Note: This register is sticky.
20	0b RW/C	**Over-current Change (OCC):** Note: This register is sticky.
19	0b RW/C	**Warm Port Reset Change (WRC):** Note: This register is sticky.
18	0b RW/C	**Port Enabled Disabled Change (PEC):** Note: This register is sticky.
17	0b RW/C	**Connect Status Change (CSC):** Note: This register is sticky.
16	0b RW	**Port Link State Write Strobe (LWS):** Reserved.
15: 14	0h RW	**Port Indicator Control (PIC):** Note: This register is sticky.
13: 10	0h RW	**Port Speed (Port_Speed):** Note: This register is sticky.
9	1b RW	**Port Power (PP):** Note: This register is sticky.
8: 5	5h RW	**Port Link State (PLS):** Note: This register is sticky.
4	0b RW/S	**Port Reset (PR):** Reserved.
3	0b RW	**Over-current Active (OCA):** Note: This register is sticky.
2	0b RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW/C	**Port Enabled Disabled (PED):** Note: This register is sticky.
0	0b RW	**Current Connect Status (CCS):** Note: This register is sticky.

14.7.37 Port 1 Power Management Status and Control USB3 (PORTPMSC1USB3)—Offset 4E4h

Access Method

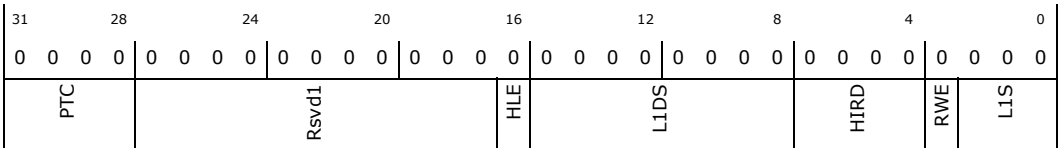
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTPMSC1USB3: [MBAR] + 4E4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31: 28	0h RW	**Port Test Control (PTC):** Note: This register is sticky.
27: 17	000h RO	**Rsvd1 (Rsvd1):** Reserved.
16	0b RO	**Hardware LPM Enable (HLE):** Reserved.
15: 8	00h RW	**L1 Device Slot (L1DS):** Note: This register is sticky.
7: 4	0h RW	**Host Initiated Resume Duration (HIRD):** Note: This register is sticky.
3	0b RW	**Remote Wake Enable (RWE):** Note: This register is sticky.
2: 0	0h RW	**L1 Status (L1S):** Note: This register is sticky.

14.7.38 Port 1 Link Info (PORTLI1)—Offset 4E8h

Access Method

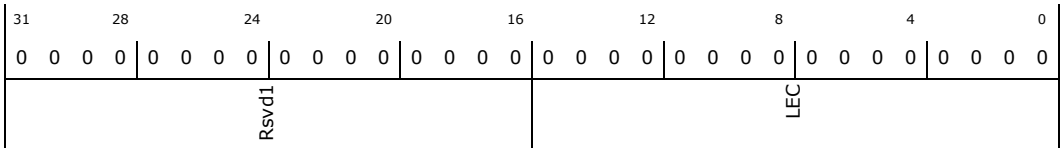
Type: Memory Mapped I/O Register (Size: 32 bits)

PORTLI1: [MBAR] + 4E8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RO	**Link Error Count (LEC):** Reserved.

14.7.39 Microframe Index (MFINDEX)—Offset 2000h

Access Method

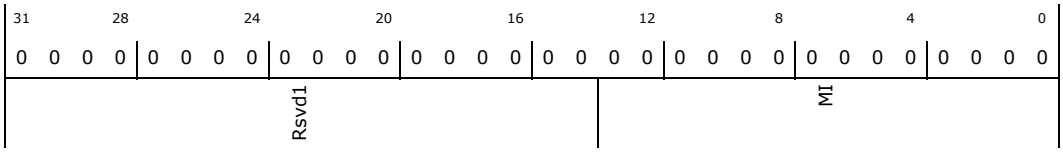
Type: Memory Mapped I/O Register (Size: 32 bits)

MFINDEX: [MBAR] + 2000h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 14	00000h RO	**Rsvd1 (Rsvd1):** Reserved.
13: 0	0000h RO	**Microframe Index (MI):** Reserved.

14.7.40 Interrupter 1 Management (IMAN1)—Offset 2020h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

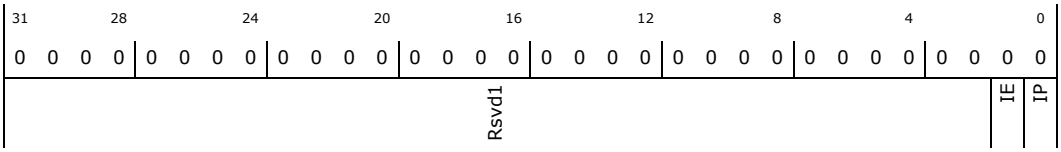
Type: Memory Mapped I/O Register (Size: 32 bits)

IMAN1: [MBAR] + 2020h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 2	00000000h RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW	**Interrupt Enable (IE):** Reserved.
0	0b RW/C	**Interrupt Pending (IP):** Reserved.

14.7.41 Interrupter 1 Moderation (IMOD1)—Offset 2024h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

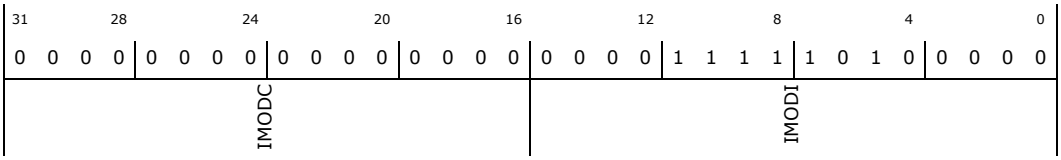
Type: Memory Mapped I/O Register (Size: 32 bits)

IMOD1: [MBAR] + 2024h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000FA0h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Interrupt Moderation Counter (IMODC):** Reserved.
15: 0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Reserved.

14.7.42 Event Ring Segment Table Size 1 (ERSTSZ1)—Offset 2028h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

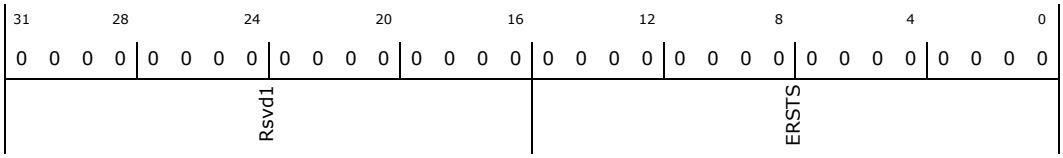
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTSZ1: [MBAR] + 2028h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Reserved.

14.7.43 Event Ring Segment Table Base Address Low 1 (ERSTBA_LO1)—Offset 2030h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

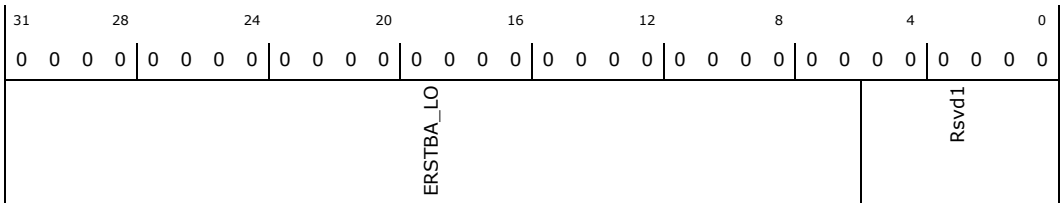
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO1: [MBAR] + 2030h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** Reserved.
5: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.44 Event Ring Segment Table Base Address High 1 (ERSTBA_HI1)—Offset 2034h

Access Method

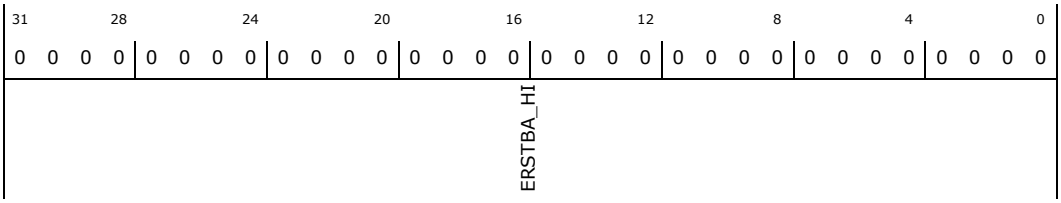
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI1: [MBAR] + 2034h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** Reserved.

14.7.45 Event Ring Dequeue Pointer Low 1 (ERDP_LO1)—Offset 2038h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

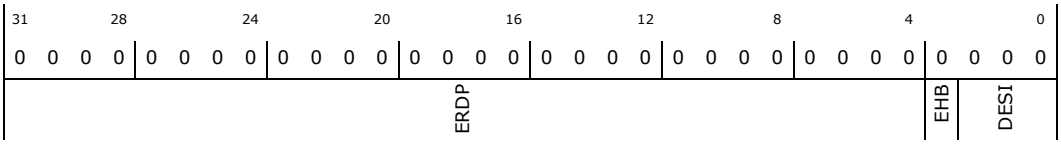
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_LO1: [MBAR] + 2038h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.
3	0b RW/C	**Event Handler Busy (EHB):** Reserved.
2: 0	0h RW	**Dequeue ERST Segment Index (DESI):** Reserved.

14.7.46 Event Ring Dequeue Pointer High 1 (ERDP_HI1)—Offset 203Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

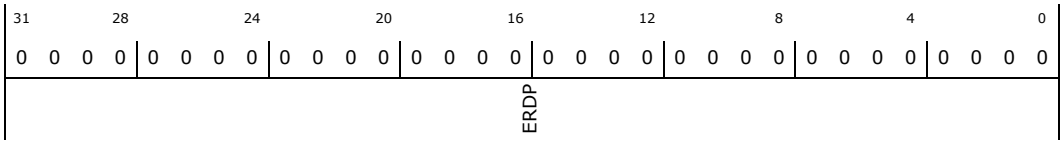
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_HI1: [MBAR] + 203Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.

14.7.47 Interrupter 2 Management (IMAN2)—Offset 2040h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

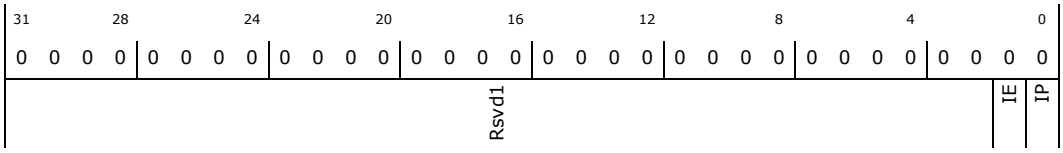
Type: Memory Mapped I/O Register (Size: 32 bits)

IMAN2: [MBAR] + 2040h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 2	00000000h RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW	**Interrupt Enable (IE):** Reserved.
0	0b RW/C	**Interrupt Pending (IP):** Reserved.

14.7.48 Interrupter 2 Moderation (IMOD2)—Offset 2044h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

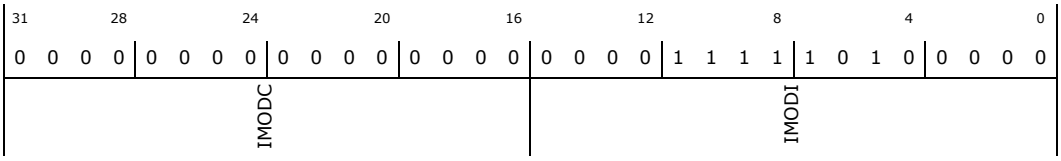
Type: Memory Mapped I/O Register (Size: 32 bits)

IMOD2: [MBAR] + 2044h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000FA0h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Interrupt Moderation Counter (IMODC):** Reserved.
15: 0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Reserved.

14.7.49 Event Ring Segment Table Size 2 (ERSTSZ2)—Offset 2048h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

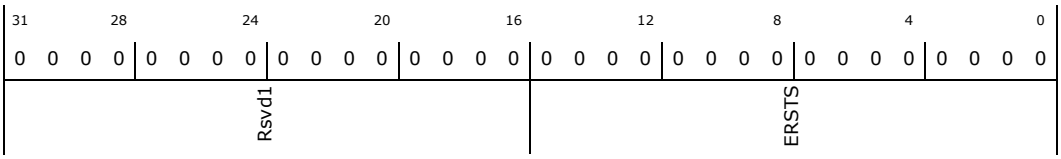
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTSZ2: [MBAR] + 2048h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Reserved.

14.7.50 Event Ring Segment Table Base Address Low 2 (ERSTBA_LO2)—Offset 2050h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

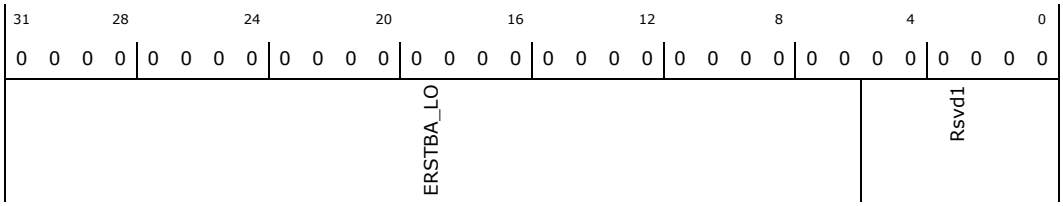
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO2: [MBAR] + 2050h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** Reserved.
5: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.51 Event Ring Segment Table Base Address High 2 (ERSTBA_HI2)—Offset 2054h

Access Method

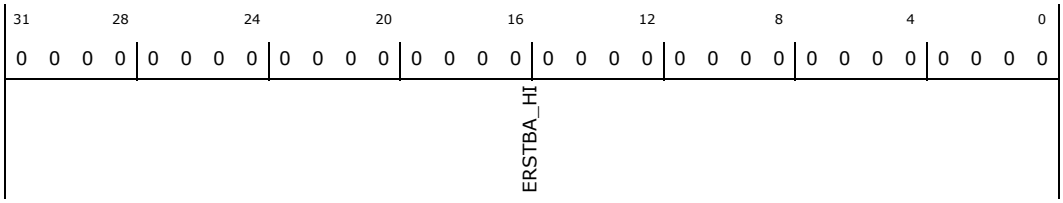
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI2: [MBAR] + 2054h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** Reserved.

14.7.52 Event Ring Dequeue Pointer Low 2 (ERDP_LO2)—Offset 2058h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

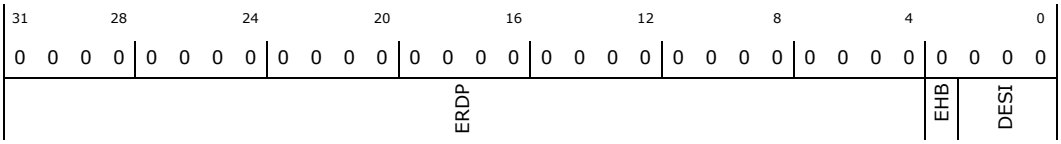
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_LO2: [MBAR] + 2058h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.
3	0b RW/C	**Event Handler Busy (EHB):** Reserved.
2: 0	0h RW	**Dequeue ERST Segment Index (DESI):** Reserved.

14.7.53 Event Ring Dequeue Pointer High 2 (ERDP_HI2)—Offset 205Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

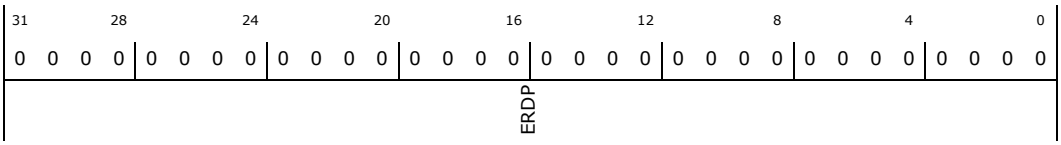
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_HI2: [MBAR] + 205Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.

14.7.54 Interrupter 3 Management (IMAN3)—Offset 2060h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

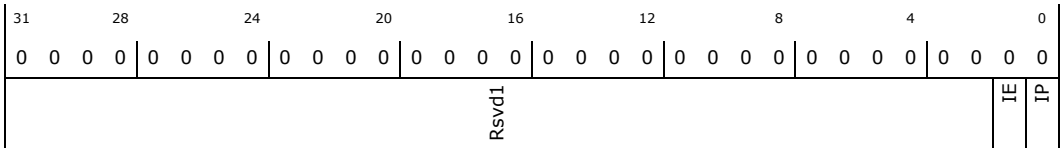
Type: Memory Mapped I/O Register (Size: 32 bits)

IMAN3: [MBAR] + 2060h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 2	00000000h RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW	**Interrupt Enable (IE):** Reserved.
0	0b RW/C	**Interrupt Pending (IP):** Reserved.

14.7.55 Interrupter 3 Moderation (IMOD3)—Offset 2064h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

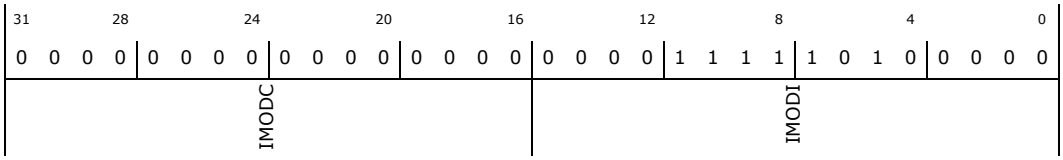
Type: Memory Mapped I/O Register (Size: 32 bits)

IMOD3: [MBAR] + 2064h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000FA0h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Interrupt Moderation Counter (IMODC):** Reserved.
15: 0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Reserved.

14.7.56 Event Ring Segment Table Size 3 (ERSTSZ3)—Offset 2068h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

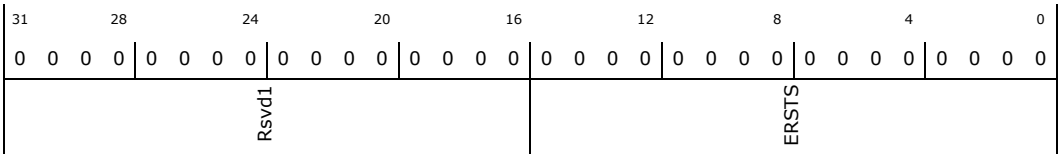
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTSZ3: [MBAR] + 2068h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Reserved.

14.7.57 Event Ring Segment Table Base Address Low 3 (ERSTBA_LO3)—Offset 2070h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

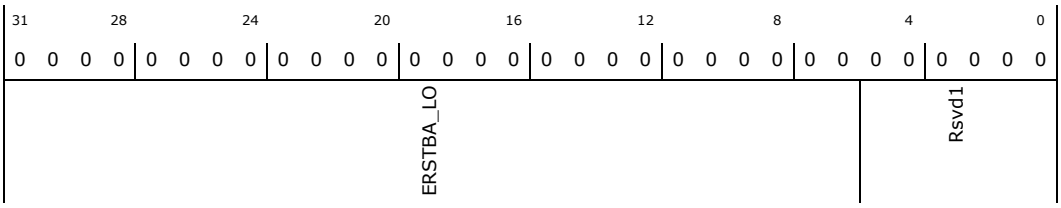
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO3: [MBAR] + 2070h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** Reserved.
5: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.58 Event Ring Segment Table Base Address High 3 (ERSTBA_HI3)—Offset 2074h

Access Method

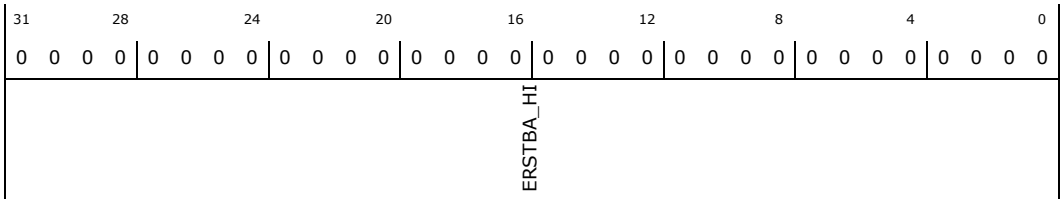
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI3: [MBAR] + 2074h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** Reserved.

14.7.59 Event Ring Dequeue Pointer Low 3 (ERDP_LO3)—Offset 2078h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

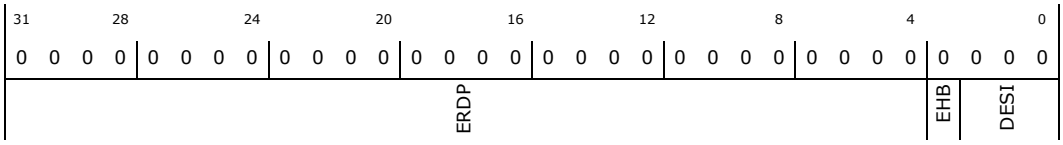
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_LO3: [MBAR] + 2078h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.
3	0b RW/C	**Event Handler Busy (EHB):** Reserved.
2: 0	0h RW	**Dequeue ERST Segment Index (DESI):** Reserved.

14.7.60 Event Ring Dequeue Pointer High 3 (ERDP_HI3)—Offset 207Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

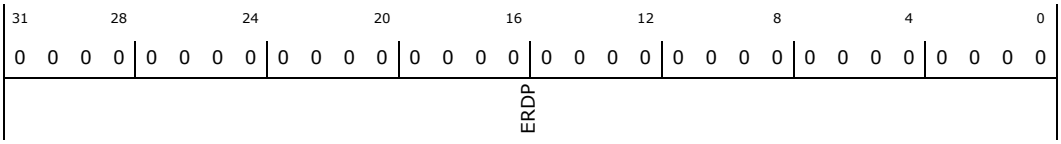
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_HI3: [MBAR] + 207Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.

14.7.61 Interrupter 4 Management (IMAN4)—Offset 2080h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

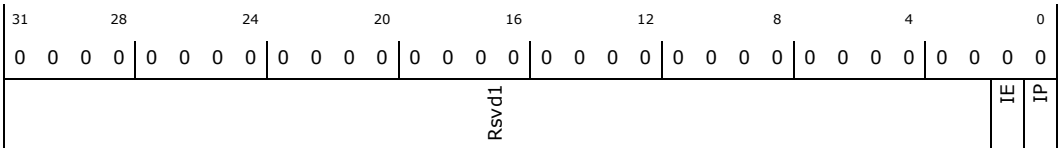
Type: Memory Mapped I/O Register (Size: 32 bits)

IMAN4: [MBAR] + 2080h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 2	00000000h RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW	**Interrupt Enable (IE):** Reserved.
0	0b RW/C	**Interrupt Pending (IP):** Reserved.

14.7.62 Interrupter 4 Moderation (IMOD4)—Offset 2084h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

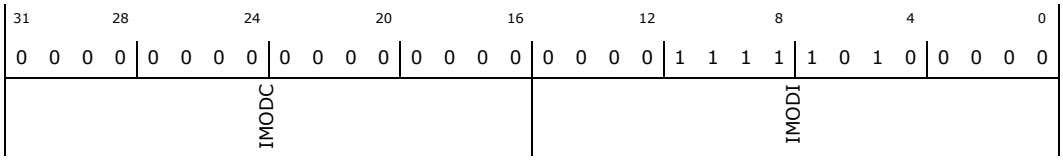
Type: Memory Mapped I/O Register (Size: 32 bits)

IMOD4: [MBAR] + 2084h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000FA0h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Interrupt Moderation Counter (IMODC):** Reserved.
15: 0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Reserved.

14.7.63 Event Ring Segment Table Size 4 (ERSTSZ4)—Offset 2088h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

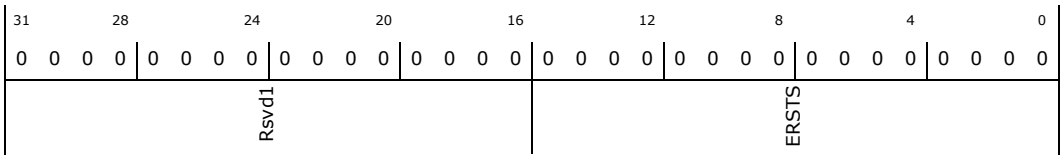
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTSZ4: [MBAR] + 2088h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Reserved.

14.7.64 Event Ring Segment Table Base Address Low 4 (ERSTBA_LO4)—Offset 2090h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

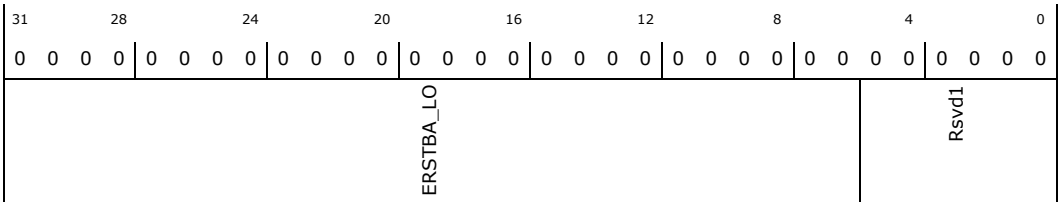
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO4: [MBAR] + 2090h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** Reserved.
5: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.65 Event Ring Segment Table Base Address High 4 (ERSTBA_HI4)—Offset 2094h

Access Method

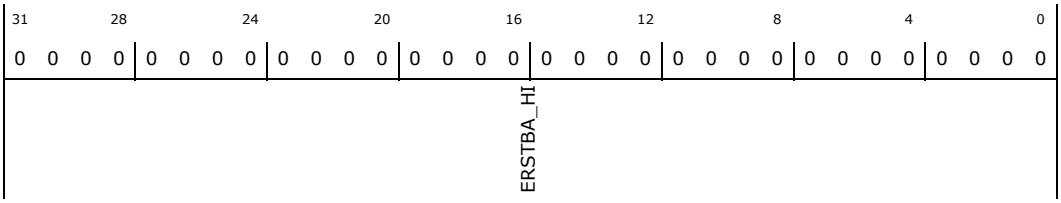
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI4: [MBAR] + 2094h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** Reserved.

14.7.66 Event Ring Dequeue Pointer Low 4 (ERDP_LO4)—Offset 2098h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

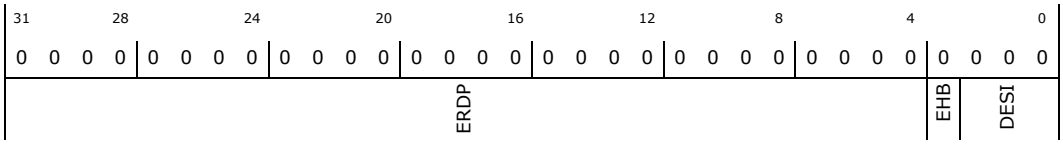
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_LO4: [MBAR] + 2098h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.
3	0b RW/C	**Event Handler Busy (EHB):** Reserved.
2: 0	0h RW	**Dequeue ERST Segment Index (DESI):** Reserved.

14.7.67 Event Ring Dequeue Pointer High 4 (ERDP_HI4)—Offset 209Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

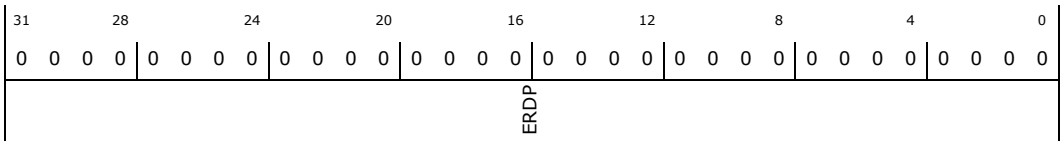
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_HI4: [MBAR] + 209Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.

14.7.68 Interrupter 5 Management (IMAN5)—Offset 20A0h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

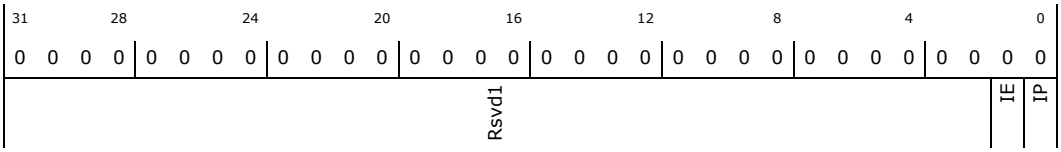
Type: Memory Mapped I/O Register (Size: 32 bits)

IMAN5: [MBAR] + 20A0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 2	00000000h RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW	**Interrupt Enable (IE):** Reserved.
0	0b RW/C	**Interrupt Pending (IP):** Reserved.

14.7.69 Interrupter 5 Moderation (IMOD5)—Offset 20A4h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

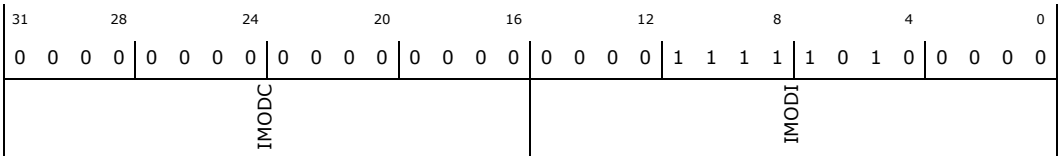
Type: Memory Mapped I/O Register (Size: 32 bits)

IMOD5: [MBAR] + 20A4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000FA0h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Interrupt Moderation Counter (IMODC):** Reserved.
15: 0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Reserved.

14.7.70 Event Ring Segment Table Size 5 (ERSTSZ5)—Offset 20A8h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

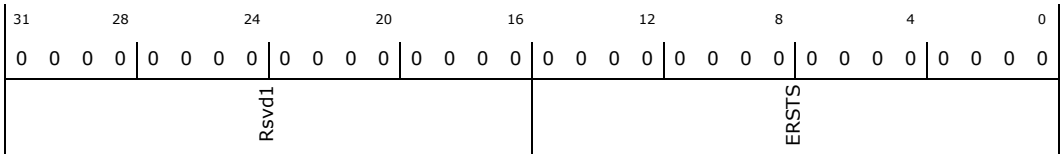
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTSZ5: [MBAR] + 20A8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Reserved.

14.7.71 Event Ring Segment Table Base Address Low 5 (ERSTBA_LO5)—Offset 20B0h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

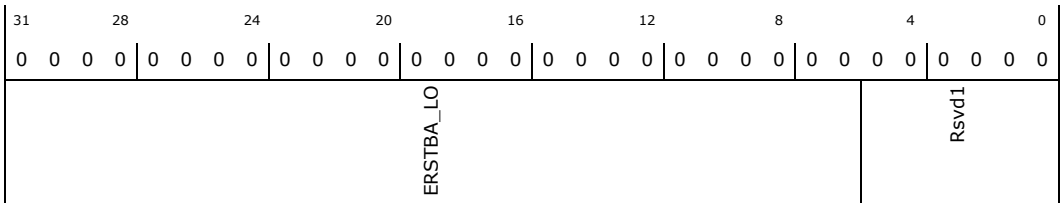
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO5: [MBAR] + 20B0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** Reserved.
5: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.72 Event Ring Segment Table Base Address High 5 (ERSTBA_HI5)—Offset 20B4h

Access Method

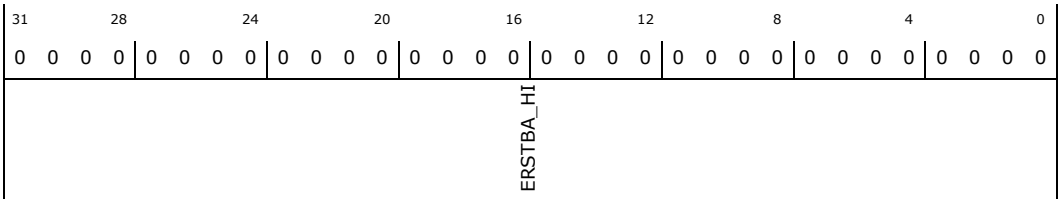
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI5: [MBAR] + 20B4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** Reserved.

14.7.73 Event Ring Dequeue Pointer Low 5 (ERDP_LO5)—Offset 20B8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

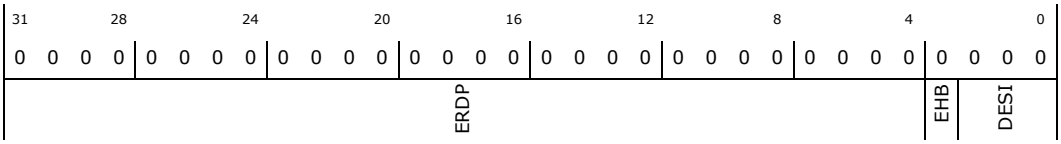
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_LO5: [MBAR] + 20B8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.
3	0b RW/C	**Event Handler Busy (EHB):** Reserved.
2: 0	0h RW	**Dequeue ERST Segment Index (DESI):** Reserved.

14.7.74 Event Ring Dequeue Pointer High 5 (ERDP_HI5)—Offset 20BCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

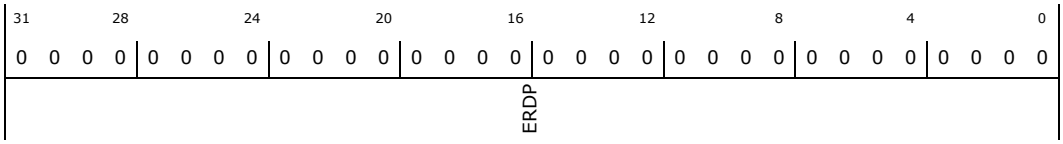
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_HI5: [MBAR] + 20BCh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.

14.7.75 Interrupter 6 Management (IMAN6)—Offset 20C0h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

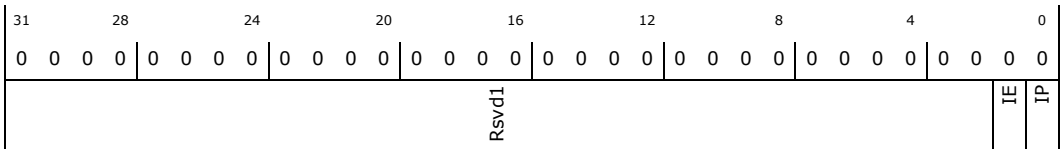
Type: Memory Mapped I/O Register (Size: 32 bits)

IMAN6: [MBAR] + 20C0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 2	00000000h RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW	**Interrupt Enable (IE):** Reserved.
0	0b RW/C	**Interrupt Pending (IP):** Reserved.

14.7.76 Interrupter 6 Moderation (IMOD6)—Offset 20C4h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

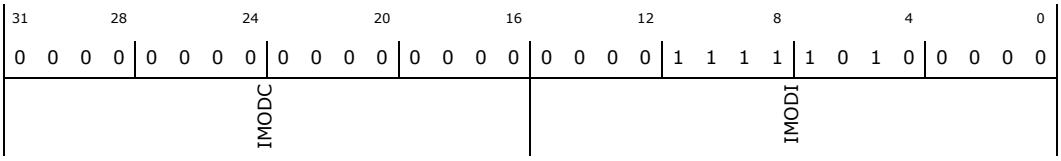
Type: Memory Mapped I/O Register (Size: 32 bits)

IMOD6: [MBAR] + 20C4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000FA0h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Interrupt Moderation Counter (IMODC):** Reserved.
15: 0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Reserved.

14.7.77 Event Ring Segment Table Size 6 (ERSTSZ6)—Offset 20C8h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

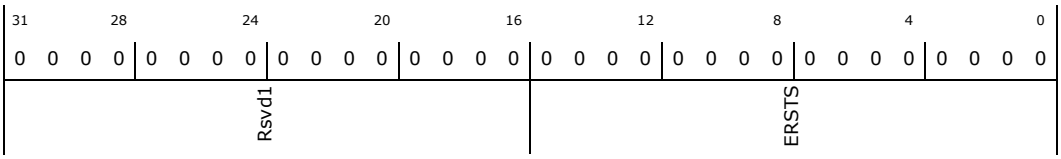
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTSZ6: [MBAR] + 20C8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Reserved.

14.7.78 Event Ring Segment Table Base Address Low 6 (ERSTBA_LO6)—Offset 20D0h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

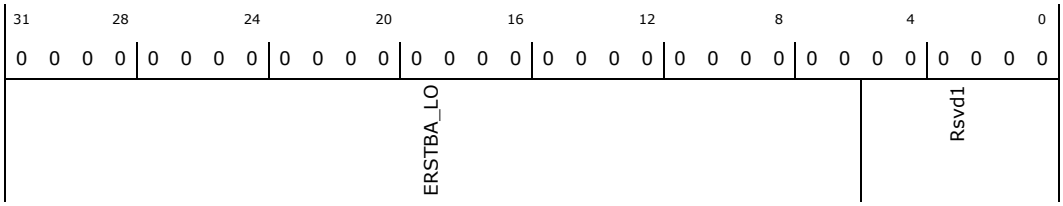
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO6: [MBAR] + 20D0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** Reserved.
5: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.79 Event Ring Segment Table Base Address High 6 (ERSTBA_HI6)—Offset 20D4h

Access Method

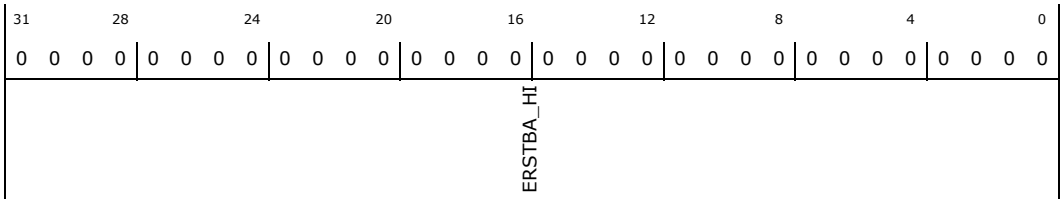
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI6: [MBAR] + 20D4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** Reserved.

14.7.80 Event Ring Dequeue Pointer Low 6 (ERDP_LO6)—Offset 20D8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

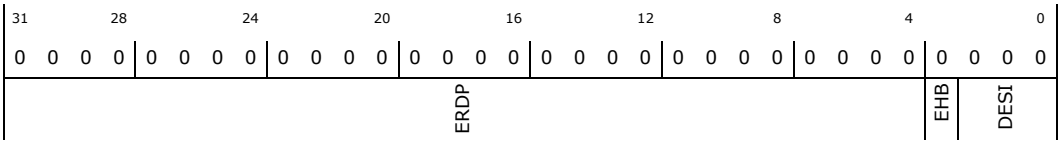
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_LO6: [MBAR] + 20D8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.
3	0b RW/C	**Event Handler Busy (EHB):** Reserved.
2: 0	0h RW	**Dequeue ERST Segment Index (DESI):** Reserved.

14.7.81 Event Ring Dequeue Pointer High 6 (ERDP_HI6)—Offset 20DCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

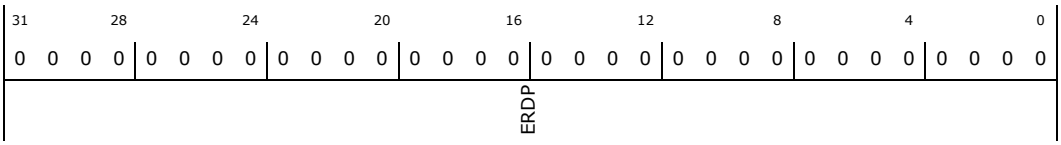
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_HI6: [MBAR] + 20DCh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.

14.7.82 Interrupter 7 Management (IMAN7)—Offset 20E0h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

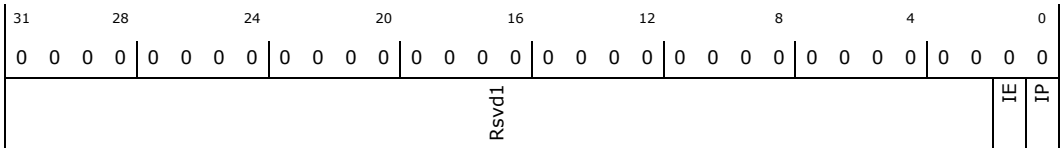
Type: Memory Mapped I/O Register (Size: 32 bits)

IMAN7: [MBAR] + 20E0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 2	00000000h RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW	**Interrupt Enable (IE):** Reserved.
0	0b RW/C	**Interrupt Pending (IP):** Reserved.

14.7.83 Interrupter 7 Moderation (IMOD7)—Offset 20E4h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

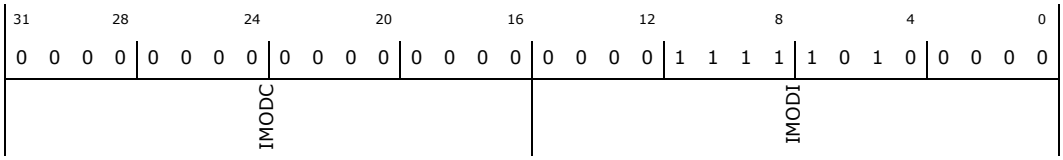
Type: Memory Mapped I/O Register (Size: 32 bits)

IMOD7: [MBAR] + 20E4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000FA0h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Interrupt Moderation Counter (IMODC):** Reserved.
15: 0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Reserved.

14.7.84 Event Ring Segment Table Size 7 (ERSTSZ7)—Offset 20E8h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

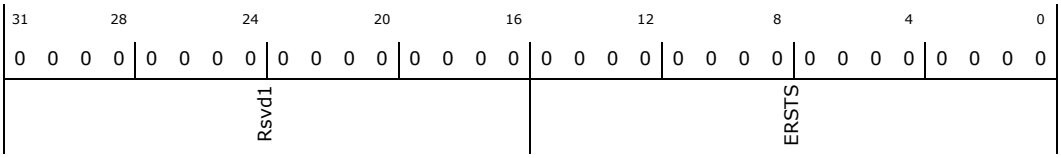
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTSZ7: [MBAR] + 20E8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Reserved.

14.7.85 Event Ring Segment Table Base Address Low 7 (ERSTBA_LO7)—Offset 20F0h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

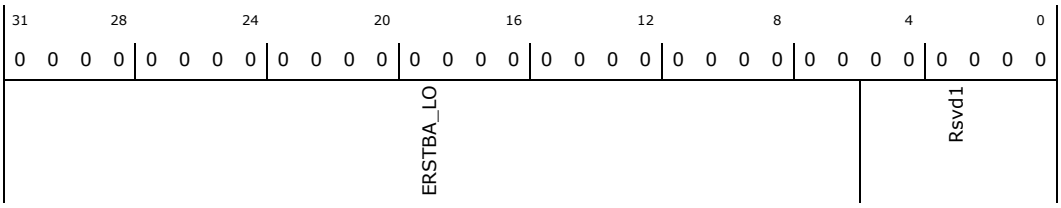
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO7: [MBAR] + 20F0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** Reserved.
5: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.86 Event Ring Segment Table Base Address High 7 (ERSTBA_HI7)—Offset 20F4h

Access Method

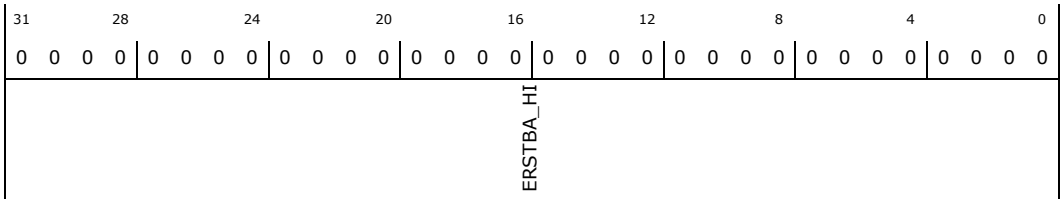
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI7: [MBAR] + 20F4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** Reserved.

14.7.87 Event Ring Dequeue Pointer Low 7 (ERDP_LO7)—Offset 20F8h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

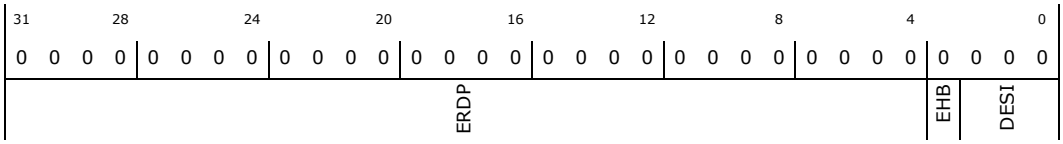
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_LO7: [MBAR] + 20F8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.
3	0b RW/C	**Event Handler Busy (EHB):** Reserved.
2: 0	0h RW	**Dequeue ERST Segment Index (DESI):** Reserved.

14.7.88 Event Ring Dequeue Pointer High 7 (ERDP_HI7)—Offset 20FCh

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

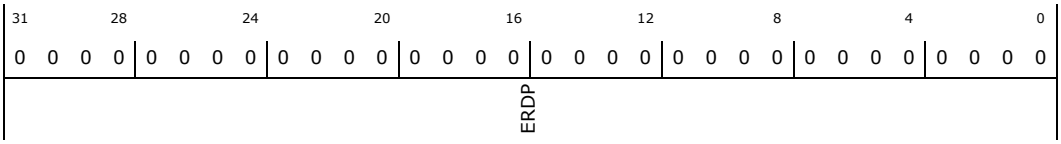
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_HI7: [MBAR] + 20FCh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.

14.7.89 Interrupter 8 Management (IMAN8)—Offset 2100h

There are 8 IMAN registers. x = 1, 2, ..., 8

Access Method

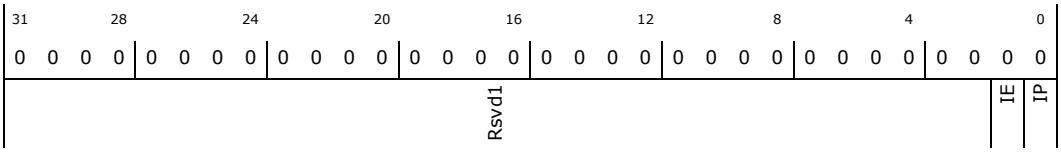
Type: Memory Mapped I/O Register (Size: 32 bits)

IMAN8: [MBAR] + 2100h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 2	00000000h RO	**Rsvd1 (Rsvd1):** Reserved.
1	0b RW	**Interrupt Enable (IE):** Reserved.
0	0b RW/C	**Interrupt Pending (IP):** Reserved.

14.7.90 Interrupter 8 Moderation (IMOD8)—Offset 2104h

There are 8 IMOD registers. x = 1, 2, ..., 8

Access Method

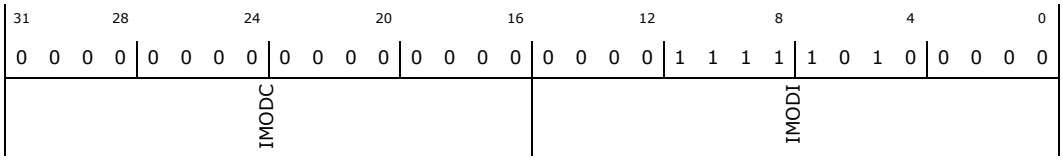
Type: Memory Mapped I/O Register (Size: 32 bits)

IMOD8: [MBAR] + 2104h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000FA0h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Interrupt Moderation Counter (IMODC):** Reserved.
15: 0	0FA0h RW	**Interrupt Moderation Interval (IMODI):** Reserved.

14.7.91 Event Ring Segment Table Size 8 (ERSTSZ8)—Offset 2108h

There are 8 ERSTSZ register. x = 1, 2, ..., 8

Access Method

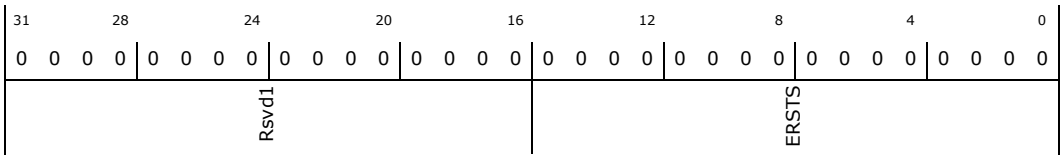
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTSZ8: [MBAR] + 2108h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd1 (Rsvd1):** Reserved.
15: 0	0000h RW	**Event Ring Segment Table Size (ERSTS):** Reserved.

14.7.92 Event Ring Segment Table Base Address Low 8 (ERSTBA_LO8)—Offset 2110h

There are 8 ERSTBA_LO registers x = 1, 2, ..., 8

Access Method

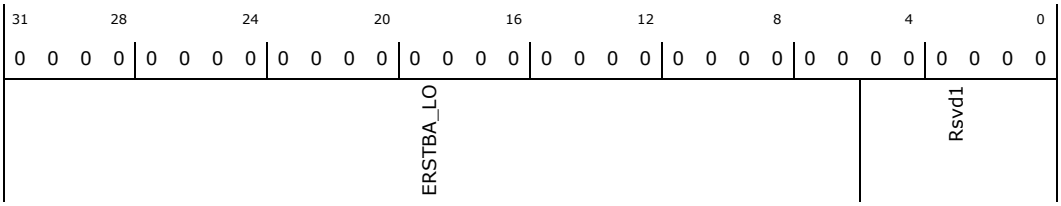
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_LO8: [MBAR] + 2110h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 6	0000000h RW	**Event Ring Segment Table Base Address Register (ERSTBA_LO):** Reserved.
5: 0	00h RO	**Rsvd1 (Rsvd1):** Reserved.

14.7.93 Event Ring Segment Table Base Address High 8 (ERSTBA_HI8)—Offset 2114h

Access Method

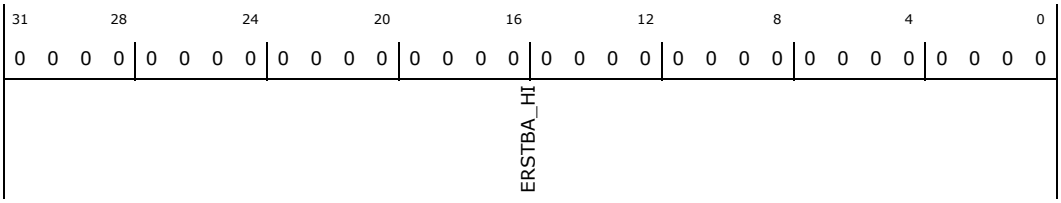
Type: Memory Mapped I/O Register (Size: 32 bits)

ERSTBA_HI8: [MBAR] + 2114h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Segment Table Base Address (ERSTBA_HI):** Reserved.

14.7.94 Event Ring Dequeue Pointer Low 8 (ERDP_LO8)—Offset 2118h

There are 8 ERDP_LO registers. x = 1, 2, ...,8

Access Method

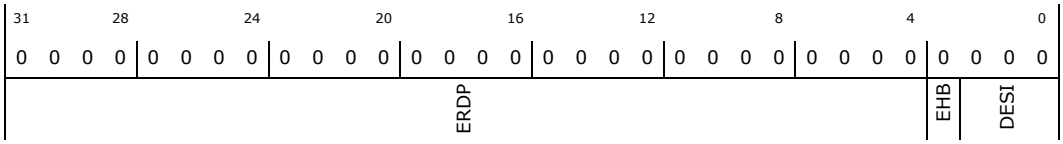
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_LO8: [MBAR] + 2118h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 4	0000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.
3	0b RW/C	**Event Handler Busy (EHB):** Reserved.
2: 0	0h RW	**Dequeue ERST Segment Index (DESI):** Reserved.

14.7.95 Event Ring Dequeue Pointer High 8 (ERDP_HI8)—Offset 211Ch

There are 8 ERDP_HI registers. x = 1, 2, ..., 8

Access Method

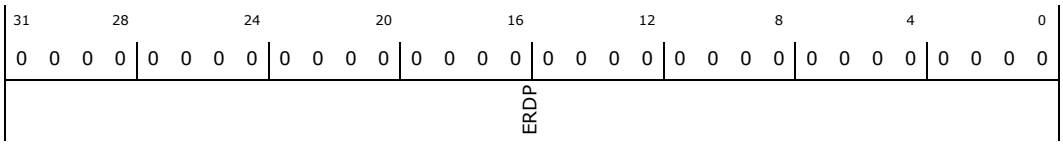
Type: Memory Mapped I/O Register (Size: 32 bits)

ERDP_HI8: [MBAR] + 211Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Event Ring Dequeue Pointer (ERDP):** Reserved.

14.7.96 Door Bell 1 (DOORBELL1)—Offset 3000h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

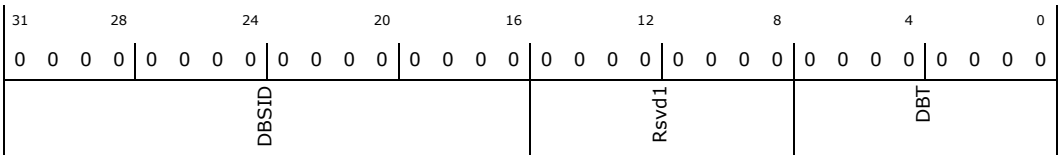
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL1: [MBAR] + 3000h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.97 Door Bell 2 (DOORBELL2)—Offset 3004h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

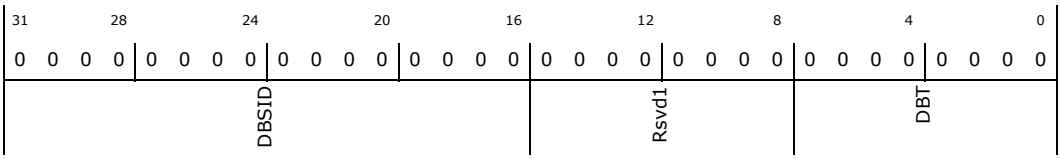
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL2: [MBAR] + 3004h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.

Bit Range	Default & Access	Description
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.98 Door Bell 3 (DOORBELL3)—Offset 3008h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

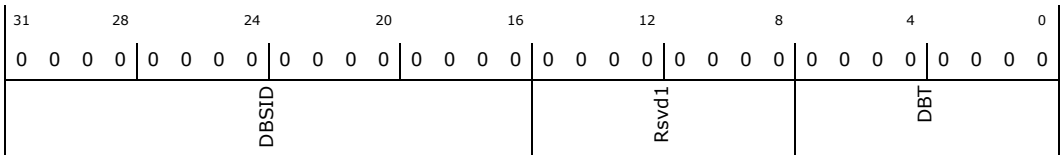
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL3: [MBAR] + 3008h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.99 Door Bell 4 (DOORBELL4)—Offset 300Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

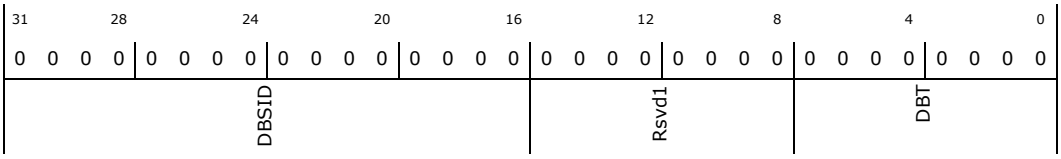
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL4: [MBAR] + 300Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.100 Door Bell 5 (DOORBELL5)—Offset 3010h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

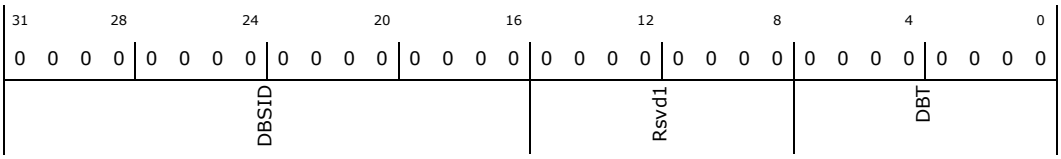
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL5: [MBAR] + 3010h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.101 Door Bell 6 (DOORBELL6)—Offset 3014h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

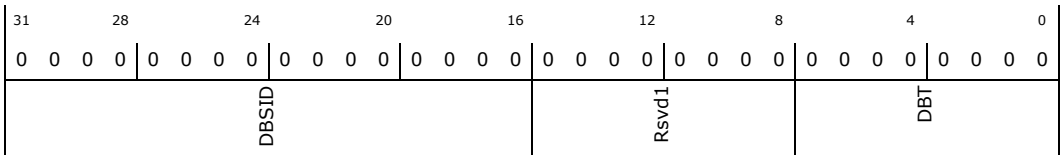
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL6: [MBAR] + 3014h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.102 Door Bell 7 (DOORBELL7)—Offset 3018h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

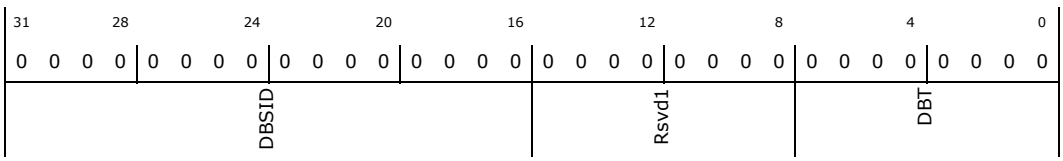
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL7: [MBAR] + 3018h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.

Bit Range	Default & Access	Description
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.103 Door Bell 8 (DOORBELL8)—Offset 301Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

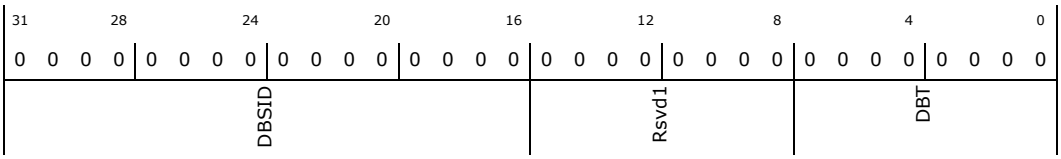
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL8: [MBAR] + 301Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.104 Door Bell 9 (DOORBELL9)—Offset 3020h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

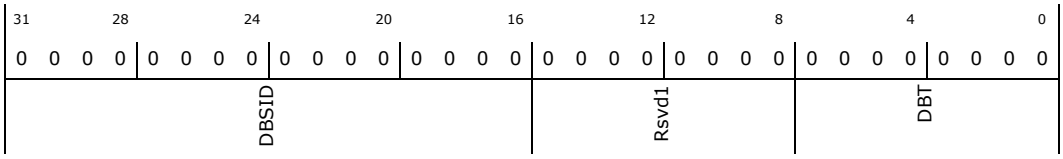
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL9: [MBAR] + 3020h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.105 Door Bell 10 (DOORBELL10)—Offset 3024h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

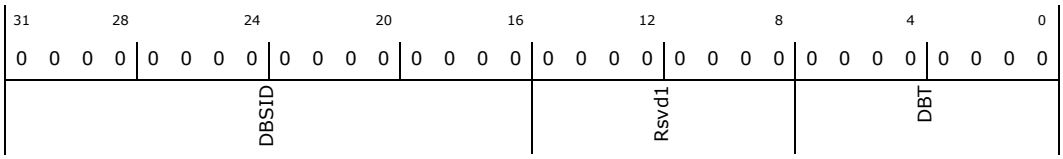
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL10: [MBAR] + 3024h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.106 Door Bell 11 (DOORBELL11)—Offset 3028h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

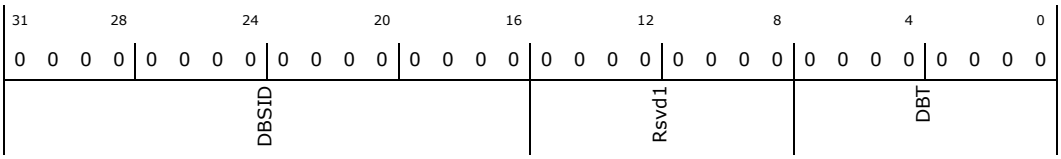
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL11: [MBAR] + 3028h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.107 Door Bell 12 (DOORBELL12)—Offset 302Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

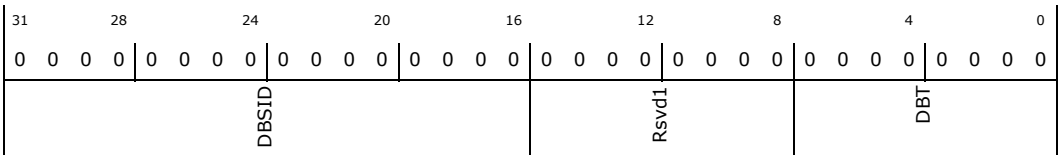
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL12: [MBAR] + 302Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.

Bit Range	Default & Access	Description
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.108 Door Bell 13 (DOORBELL13)—Offset 3030h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

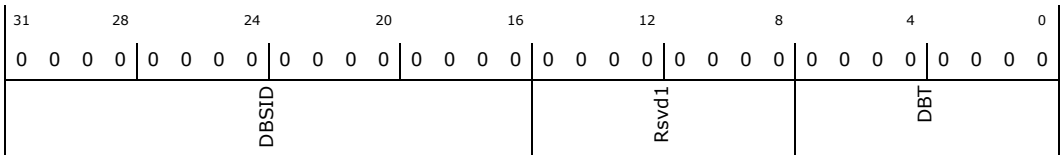
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL13: [MBAR] + 3030h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.109 Door Bell 14 (DOORBELL14)—Offset 3034h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

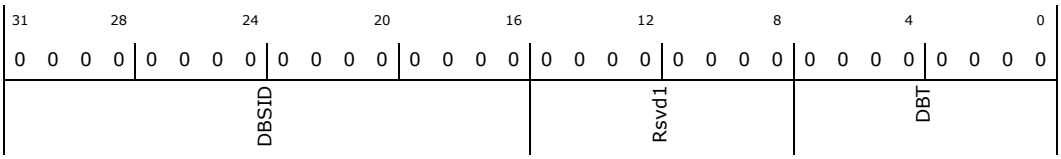
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL14: [MBAR] + 3034h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.110 Door Bell 15 (DOORBELL15)—Offset 3038h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

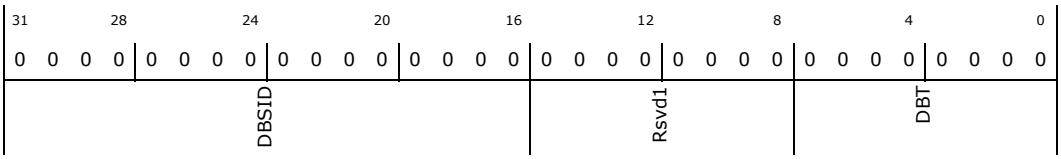
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL15: [MBAR] + 3038h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.

Bit Range	Default & Access	Description
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.111 Door Bell 16 (DOORBELL16)—Offset 303Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

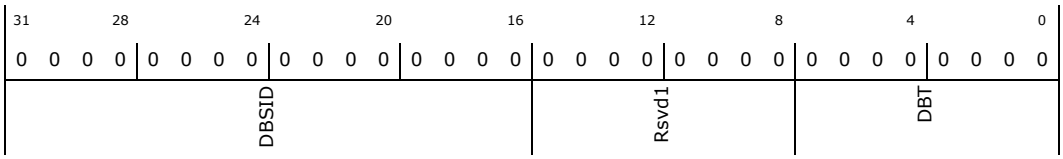
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL16: [MBAR] + 303Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.112 Door Bell 17 (DOORBELL17)—Offset 3040h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

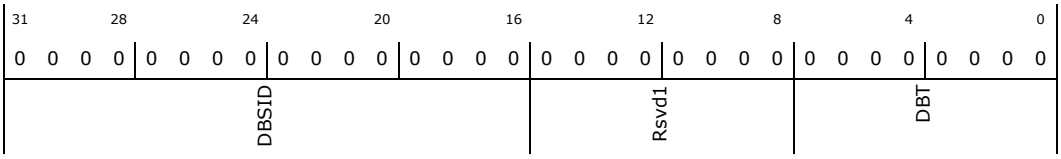
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL17: [MBAR] + 3040h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.113 Door Bell 18 (DOORBELL18)—Offset 3044h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

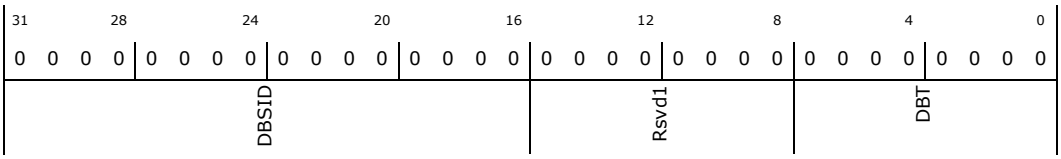
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL18: [MBAR] + 3044h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.114 Door Bell 19 (DOORBELL19)—Offset 3048h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

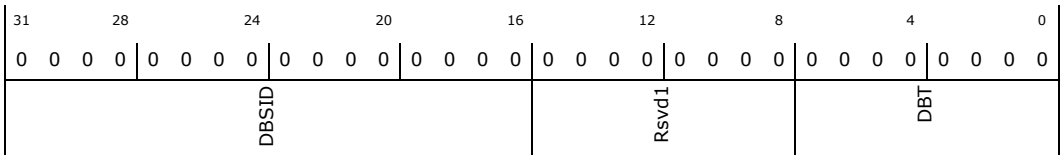
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL19: [MBAR] + 3048h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.115 Door Bell 20 (DOORBELL20)—Offset 304Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

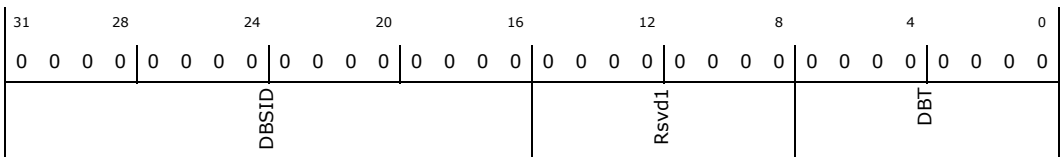
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL20: [MBAR] + 304Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.

Bit Range	Default & Access	Description
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.116 Door Bell 21 (DOORBELL21)—Offset 3050h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

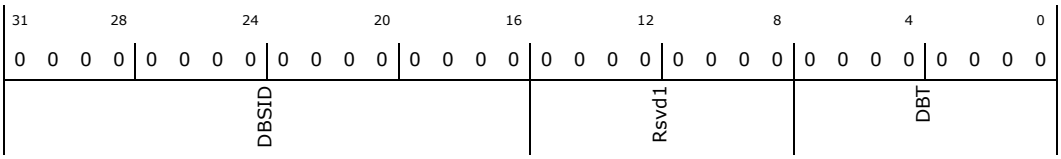
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL21: [MBAR] + 3050h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.117 Door Bell 22 (DOORBELL22)—Offset 3054h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

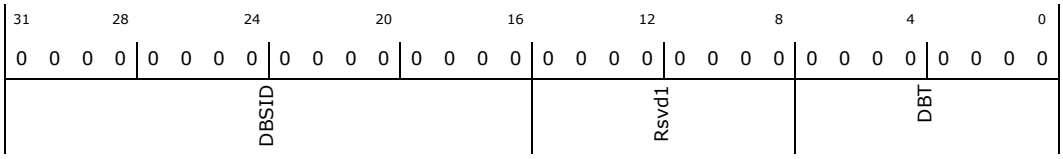
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL22: [MBAR] + 3054h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.118 Door Bell 23 (DOORBELL23)—Offset 3058h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

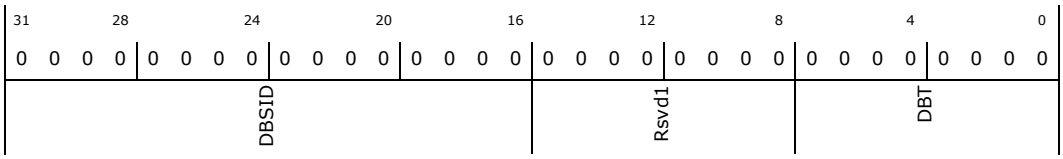
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL23: [MBAR] + 3058h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.119 Door Bell 24 (DOORBELL24)—Offset 305Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

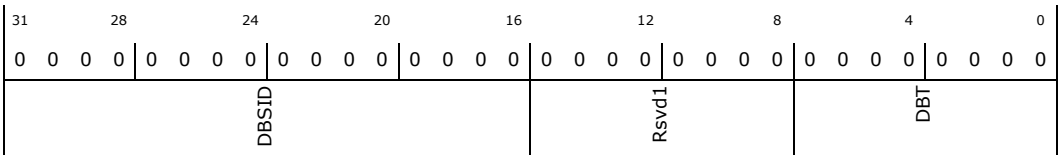
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL24: [MBAR] + 305Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.120 Door Bell 25 (DOORBELL25)—Offset 3060h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

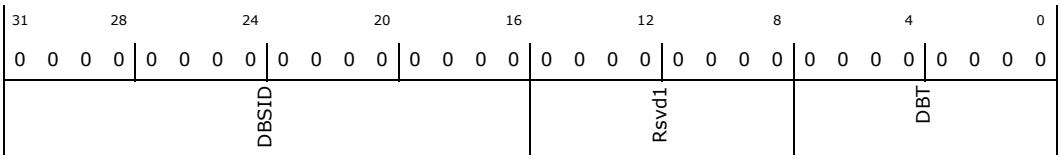
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL25: [MBAR] + 3060h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.

Bit Range	Default & Access	Description
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.121 Door Bell 26 (DOORBELL26)—Offset 3064h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

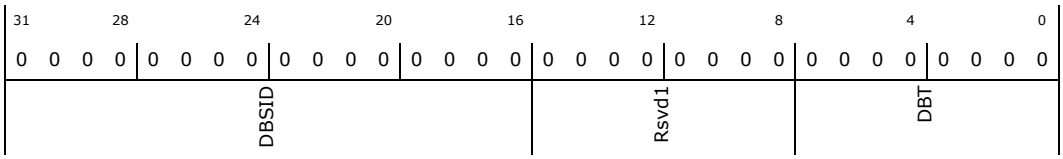
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL26: [MBAR] + 3064h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.122 Door Bell 27 (DOORBELL27)—Offset 3068h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

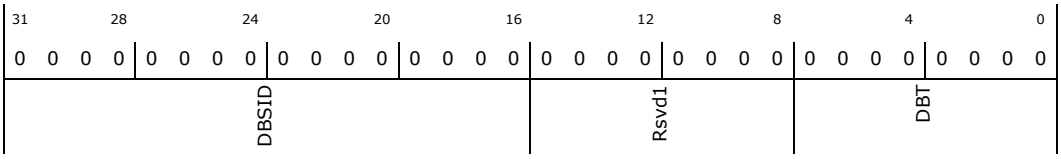
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL27: [MBAR] + 3068h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.123 Door Bell 28 (DOORBELL28)—Offset 306Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

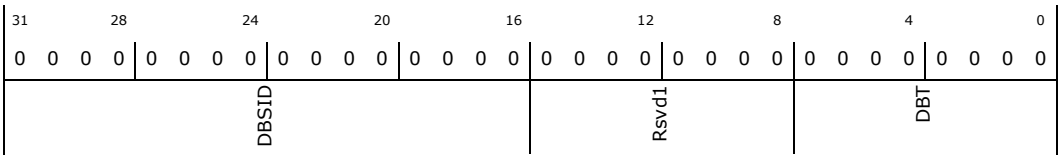
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL28: [MBAR] + 306Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.124 Door Bell 29 (DOORBELL29)—Offset 3070h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

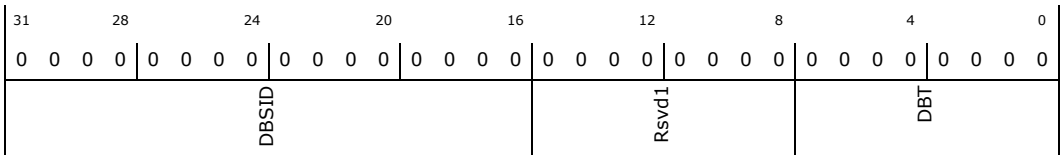
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL29: [MBAR] + 3070h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.125 Door Bell 30 (DOORBELL30)—Offset 3074h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

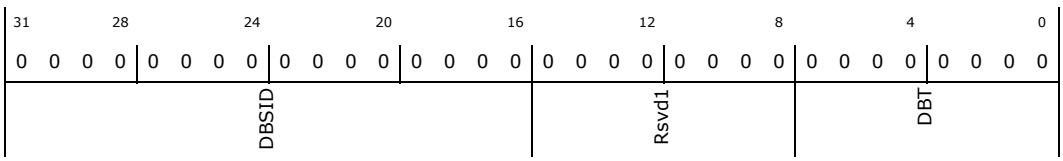
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL30: [MBAR] + 3074h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.

Bit Range	Default & Access	Description
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.126 Door Bell 31 (DOORBELL31)—Offset 3078h

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

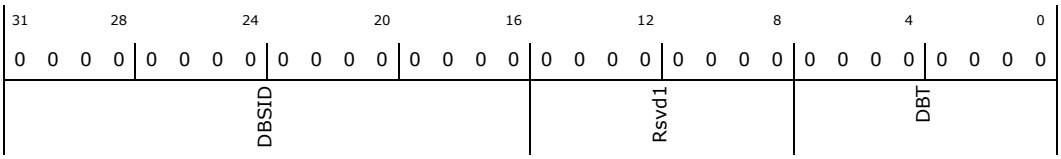
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL31: [MBAR] + 3078h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.127 Door Bell 32 (DOORBELL32)—Offset 307Ch

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the XHC and the rest being reserved.

Access Method

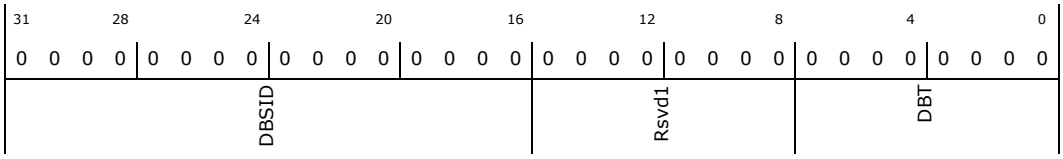
Type: Memory Mapped I/O Register (Size: 32 bits)

DOORBELL32: [MBAR] + 307Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**DB Stream ID (DBSID):** Reserved.
15: 8	00h RO	**Rsvd1 (Rsvd1):** Reserved.
7: 0	00h RW	**DB Target (DBT):** Reserved.

14.7.128 XECP_SUPP_USB2_0 (XECP_SUPP_USB2_0)—Offset 8000h

Access Method

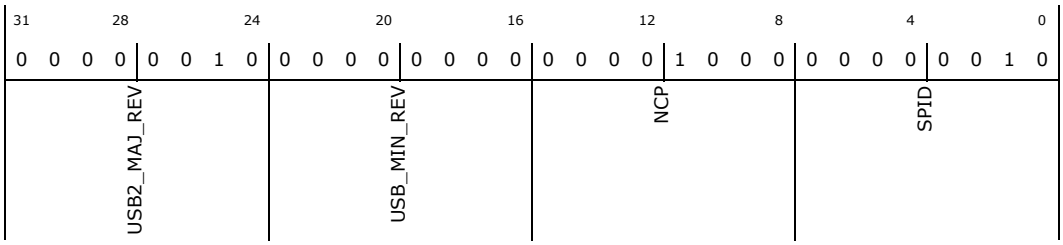
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB2_0: [MBAR] + 8000h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 02000802h



Bit Range	Default & Access	Description
31: 24	02h RO	**USB Major Revision: 2.0 (USB2_MAJ_REV):** Reserved.
23: 16	00h RO	**USB Minor Revision (USB_MIN_REV):** Reserved.
15: 8	08h RO	**Next Capability Pointer (NCP):** Reserved.
7: 0	02h RO	**Supported Protocol ID (SPID):** Reserved.

14.7.129 XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1)—Offset 8004h

Access Method

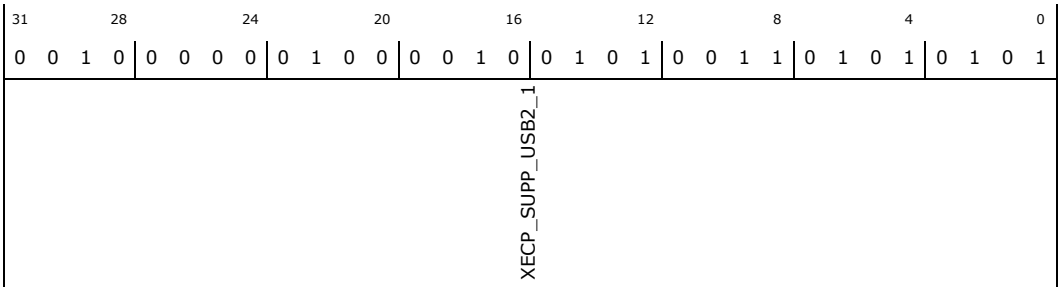
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB2_1: [MBAR] + 8004h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 20425355h



Bit Range	Default & Access	Description
31: 0	20425355h RO	**XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1):** Namestring USB

14.7.130 XECP_SUPP_USB2_2 (XECP_SUPP_USB2_2)—Offset 8008h

Access Method

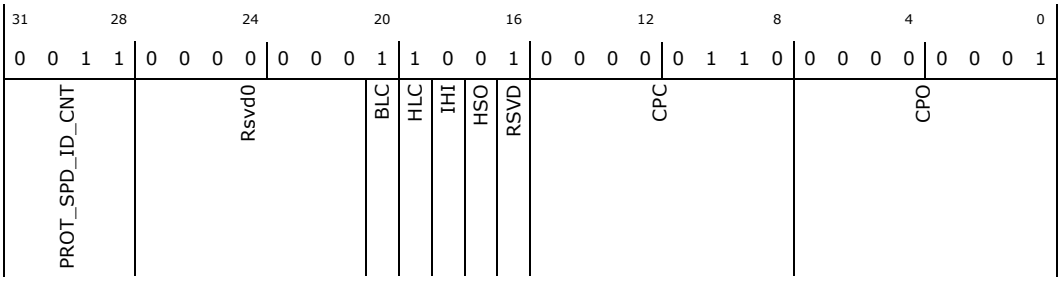
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB2_2: [MBAR] + 8008h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 30190601h



Bit Range	Default & Access	Description
31: 28	3h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 3 USB 2.0 Speed (High, Full, Low)

Bit Range	Default & Access	Description
27: 21	00h RO	**Rsvd0 (Rsvd0):** Reserved.
20	1b RO	**BESL LPM Capability (BLC):** Bit is set to 1 to indicate that the the ports described by this xHCI Supported Protocol Capability will apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers.
19	1b RO	**Protocol Defined - Hardware LMP Capability (HLC):** Reserved.
18	0b RO	**Protocol Defined - Integrated Hub Implementation (IHI):** Reserved.
17	0b RO	**Protocol Defined - High SPeed Only (HSO):** Reserved.
16	1b RO	**Reserved (RSVD):** Reserved.
15: 8	06h RO	**Compatible Port Count (CPC):** Reserved.
7: 0	01h RO	**Compatible Port Offset (CPO):** Reserved.

14.7.131 XECP_SUPP_USB2_3 (Full Speed) (XECP_SUPP_USB2_3)—Offset 8010h

Access Method

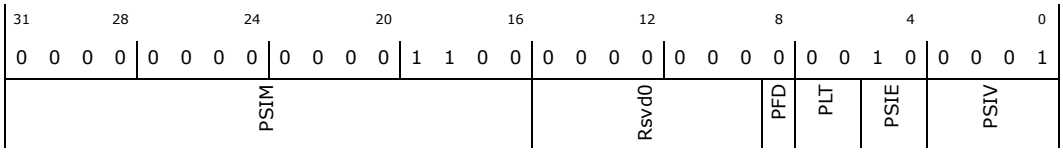
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB2_3: [MBAR] + 8010h

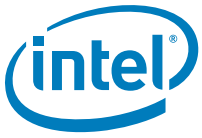
MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 000C0021h



Bit Range	Default & Access	Description
31: 16	000Ch RO	**Protocol Speed ID Mantissa (PSIM):** Reserved.
15: 9	00h RO	**Rsvd0 (Rsvd0):** Reserved.
8	0b RO	**PSI Full Duplex (PFD):** Reserved.
7: 6	0h RO	**PSI Type (PLT):** Reserved.
5: 4	2h RO	**Protocol Speed ID Exponent (PSIE):** Reserved.



Bit Range	Default & Access	Description
3: 0	1h RO	**Protocol Speed ID Value (PSIV):** Reserved.

14.7.132 XECP_SUPP_USB2_4 (Low Speed) (XECP_SUPP_USB2_4)—Offset 8014h

Access Method

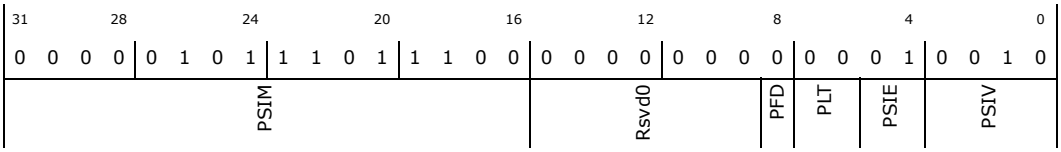
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB2_4: [MBAR] + 8014h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 05DC0012h



Bit Range	Default & Access	Description
31: 16	05DCh RO	**Protocol Speed ID Mantissa (PSIM):** Reserved.
15: 9	00h RO	**Rsvd0 (Rsvd0):** Reserved.
8	0b RO	**PSI Full Duplex (PFD):** Reserved.
7: 6	0h RO	**PSI Type (PLT):** Reserved.
5: 4	1h RO	**Protocol Speed ID Exponent (PSIE):** Reserved.
3: 0	2h RO	**Protocol Speed ID Value (PSIV):** Reserved.

14.7.133 XECP_SUPP_USB2_5 (High Speed) (XECP_SUPP_USB2_5)—Offset 8018h

Access Method

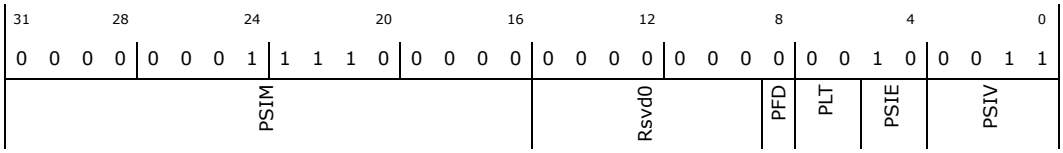
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB2_5: [MBAR] + 8018h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 01E00023h



Bit Range	Default & Access	Description
31: 16	01E0h RO	**Protocol Speed ID Mantissa (PSIM):** Reserved.
15: 9	00h RO	**Rsvd0 (Rsvd0):** Reserved.
8	0b RO	**PSI Full Duplex (PFD):** Reserved.
7: 6	0h RO	**PSI Type (PLT):** Reserved.
5: 4	2h RO	**Protocol Speed ID Exponent (PSIE):** Reserved.
3: 0	3h RO	**Protocol Speed ID Value (PSIV):** Reserved.

14.7.134 XECP_SUPP_USB3_0 (XECP_SUPP_USB3_0)—Offset 8020h

Access Method

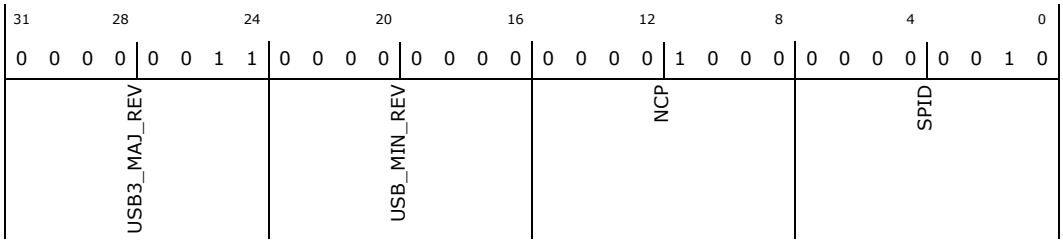
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB3_0: [MBAR] + 8020h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 03000802h



Bit Range	Default & Access	Description
31: 24	03h RO	**USB Major Revision: 3.0 (USB3_MAJ_REV):** Reserved.
23: 16	00h RO	**USB Minor Revision (USB_MIN_REV):** Reserved.
15: 8	08h RO	**Next Capability Pointer (NCP):** Reserved.
7: 0	02h RO	**Supported Protocol ID (SPID):** Reserved.

14.7.135 XECP_SUPP_USB3_1 (XECP_SUPP_USB3_1)—Offset 8024h

Access Method

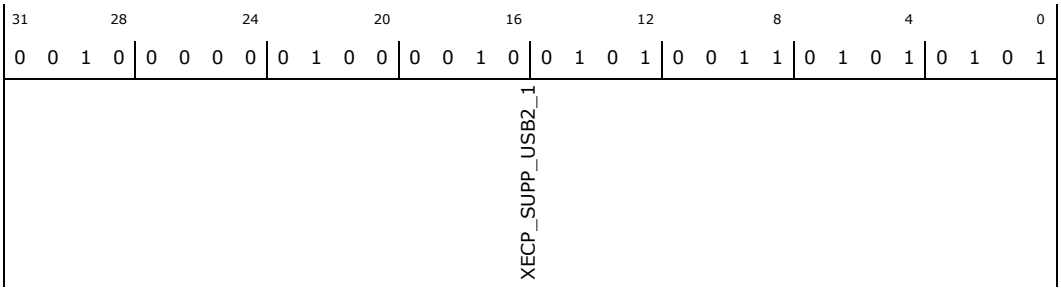
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB3_1: [MBAR] + 8024h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 20425355h



Bit Range	Default & Access	Description
31: 0	20425355h RO	**XECP_SUPP_USB2_1 (XECP_SUPP_USB2_1):** Namestring USB

14.7.136 XECP_SUPP_USB3_2 (XECP_SUPP_USB3_2)—Offset 8028h

Access Method

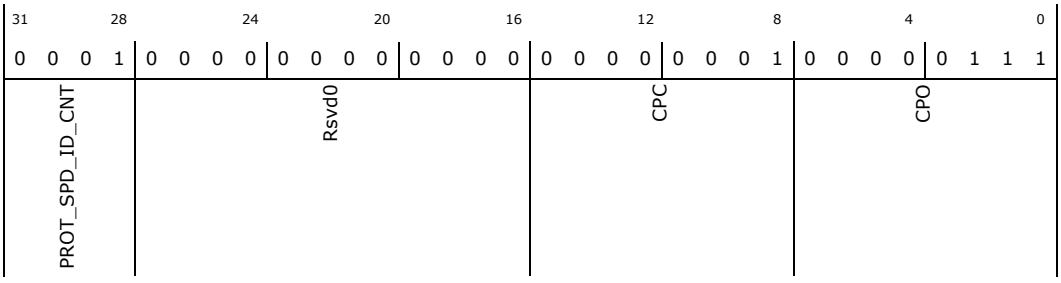
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB3_2: [MBAR] + 8028h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 10000107h



Bit Range	Default & Access	Description
31: 28	1h RO	**Protocol Speed ID Count (PROT_SPD_ID_CNT):** 1 USB 3.0 Speed (Supper Speed)

Bit Range	Default & Access	Description
27: 16	000h RO	**Rsvd0 (Rsvd0):** Reserved.
15: 8	01h RO	**Compatible Port Count (CPC):** Reserved.
7: 0	07h RO	**Compatible Port Offset (CPO):** Reserved.

14.7.137 XECP_SUPP_USB3_3 (XECP_SUPP_USB3_3)—Offset 8030h

Access Method

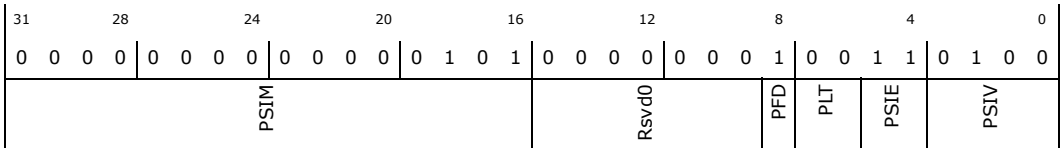
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_SUPP_USB3_3: [MBAR] + 8030h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00050134h



Bit Range	Default & Access	Description
31: 16	0005h RO	**Protocol Speed ID Mantissa (PSIM):** Reserved.
15: 9	00h RO	**Rsvd0 (Rsvd0):** Reserved.
8	1b RO	**PSI Full Duplex (PFD):** Reserved.
7: 6	0h RO	**PSI Type (PLT):** Reserved.
5: 4	3h RO	**Protocol Speed ID Exponent (PSIE):** Reserved.
3: 0	4h RO	**Protocol Speed ID Value (PSIV):** Reserved.

14.7.138 XECP_CMDM_STS0 (XECP_CMDM_STS0)—Offset 8040h

Access Method

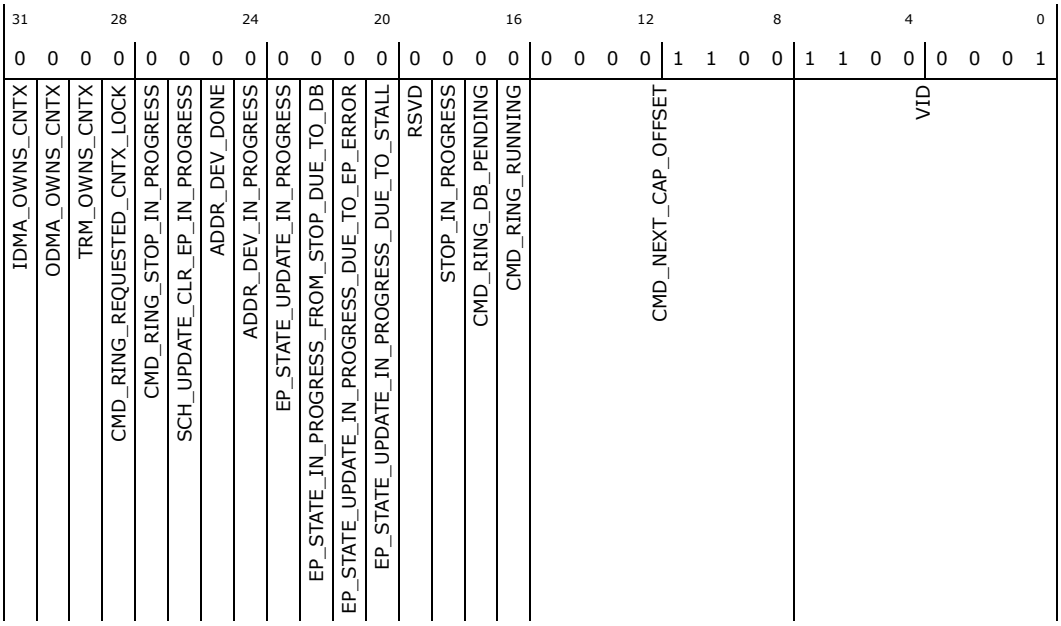
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_CMDM_STS0: [MBAR] + 8040h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000CC1h



Bit Range	Default & Access	Description
31	0h RO	**IDMA_OWNS_CNTX (IDMA_OWNS_CNTX):** Indicates that IDMA module owns the context access currently
30	0h RO	**ODMA_OWNS_CNTX (ODMA_OWNS_CNTX):** Indicates that ODMA module owns the context access currently
29	0h RO	**TRM_OWNS_CNTX (TRM_OWNS_CNTX):** Indicates that TRM modules owns the context access currently
28	0h RO	**CMD_RING_REQUESTED_CNTX_LOCK (CMD_RING_REQUESTED_CNTX_LOCK):** Indicates that Command Manager has requested a context lock
27	0h RO	**CMD_RING_STOP_IN_PROGRESS (CMD_RING_STOP_IN_PROGRESS):** Indicates that Command Ring stop command is in progress
26	0h RO	**SCH_UPDATE_CLR_EP_IN_PROGRESS (SCH_UPDATE_CLR_EP_IN_PROGRESS):** Indicates that clearing an EP out of schedule is in progress
25	0h RO	**ADDR_DEV_DONE (ADDR_DEV_DONE):** Indicates that current address device command is done by ODMA
24	0h RO	**ADDR_DEV_IN_PROGRESS (ADDR_DEV_IN_PROGRESS):** Indicates that ODMA has an address device command in progress
23	0h RO	**EP_STATE_UPDATE_IN_PROGRESS (EP_STATE_UPDATE_IN_PROGRESS):** Indicates that updating of EP state is in progress
22	0h RO	**EP_STATE_IN_PROGRESS_FROM_STOP_DUE_TO_DB (EP_STATE_IN_PROGRESS_FROM_STOP_DUE_TO_DB):** Indicates that doorbell manager is issuing and EP update due to a doorbell ring on an EP that is in stop state
21	0h RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_EP_ERROR (EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_EP_ERROR):** Indicates that transfer ring manager is isuing and EP update due to an EP error condition detected
20	0h RO	**EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_STALL (EP_STATE_UPDATE_IN_PROGRESS_DUE_TO_STALL):** Indicates that transfere ring manager is issuing an EP state update due to stall received

Bit Range	Default & Access	Description
19	0h RO	**Reserved (RSVD):** Reserved.
18	0h RO	**STOP in progress (STOP_IN_PROGRESS):** Indicates that a STOP on the Command Ring is in progress
17	0h RO	**commend ring has doorbell pending (CMD_RING_DB_PENDING):** Indicates that the commend ring has doorbell pending
16	0h RO	**commend ring running (CMD_RING_RUNNING):** Indicates that the commend ring is running
15: 8	0Ch RO	**Command next capability offset (CMD_NEXT_CAP_OFFSET):** Reserved.
7: 0	C1h RO	**Vendor defined capability ID (VID):** Reserved.

14.7.139 XECP_CMDM_STS1 (XECP_CMDM_STS1)—Offset 8044h

Access Method

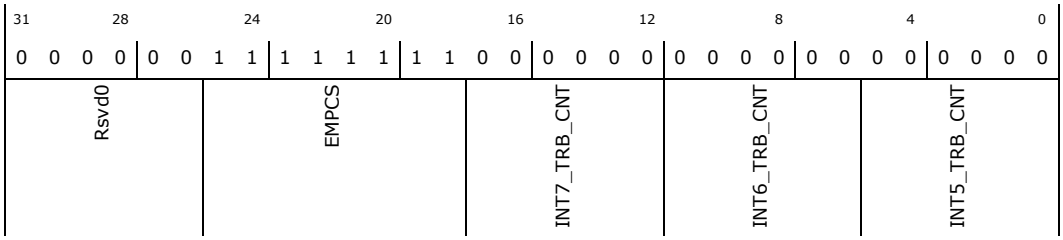
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_CMDM_STS1: [MBAR] + 8044h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 03FC0000h



Bit Range	Default & Access	Description
31: 26	00h RO	**Rsvd0 (Rsvd0):** Reserved.
25: 18	FFh RO	**Event manager Producer Cycle State (EMPCS):** Reserved.
17: 12	00h RO	**Interrupter 7 TRB Count [5:0] (INT7_TRB_CNT):** Reserved.
11: 6	00h RO	**Interrupter 6 TRB Count [5:0] (INT6_TRB_CNT):** Reserved.
5: 0	00h RO	**Interrupter 5 TRB Count [5:0] (INT5_TRB_CNT):** Reserved.

14.7.140 XECP_CMDM_STS2 (XECP_CMDM_STS2)—Offset 8048h

Access Method

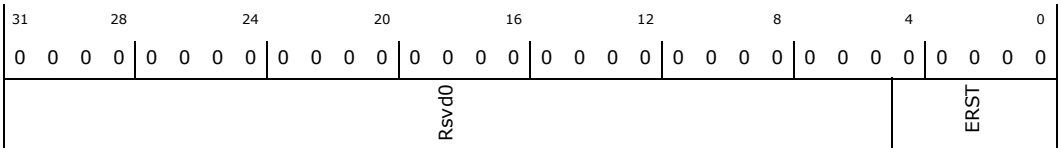
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_CMDM_STS2: [MBAR] + 8048h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 5	0000000h RO	**Rsvd0 (Rsvd0):** Reserved.
4: 0	00h RO	**Event Ring Segment Table (ERST):** count low

14.7.141 XECP_CMDM_STS3 (XECP_CMDM_STS3)—Offset 804Ch

Access Method

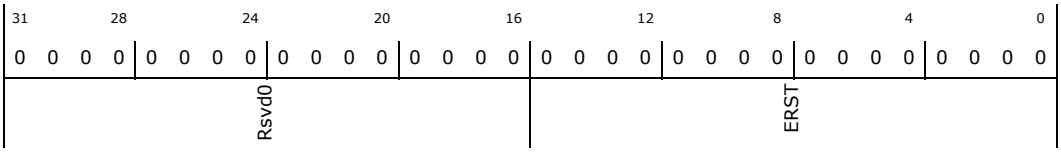
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_CMDM_STS3: [MBAR] + 804Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Rsvd0 (Rsvd0):** Reserved.
15: 0	0000h RO	**Event Ring Segment Table (ERST):** count high

14.7.142 XECP_CMDM_STS4 (XECP_CMDM_STS4)—Offset 8050h

Access Method

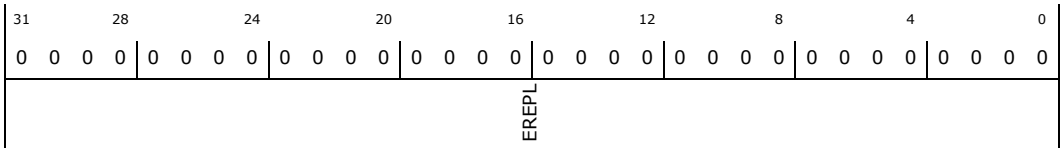
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_CMDM_STS4: [MBAR] + 8050h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RO	**Event Ring Enqueue Pointer Low (EREPL):** Reserved.

14.7.143 XECP_CMDM_STS5 (XECP_CMDM_STS5)—Offset 8054h

Access Method

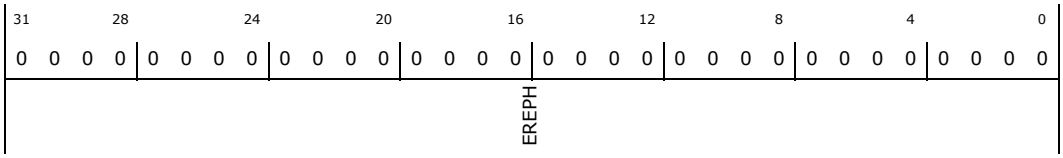
Type: Memory Mapped I/O Register (Size: 32 bits)

XECP_CMDM_STS5: [MBAR] + 8054h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RO	**Event Ring Enqueue Pointer High (EREPH):** Reserved.

14.7.144 Host Controller Capability (HOST_CTRL_CAP_REG)—Offset 8070h

This register is modified and maintained by BIOS

Access Method

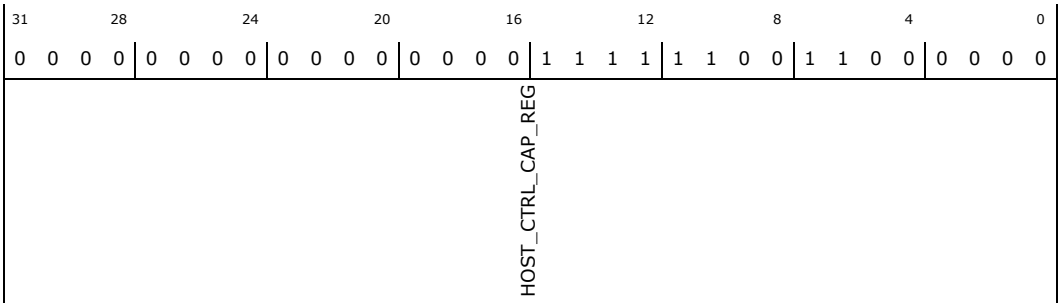
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CTRL_CAP_REG: [MBAR] + 8070h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0000FCC0h



Bit Range	Default & Access	Description
31: 0	0000FCC0h RW/L	**Host Controller Capability (HOST_CTRL_CAP_REG):** This is a register that describe the host controller the extended cap location. It includes the , XECP_HOST_NEXT_CAP_OFFSET and VEND_DEF_HOST_CAP_ID_192

14.7.145 Override EP Flow Control (HOST_CLR_MASK_REG)—Offset 8078h

Access Method

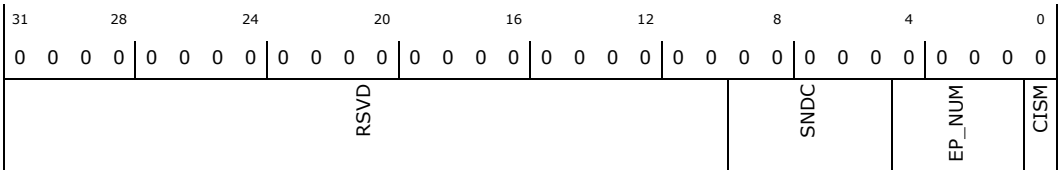
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CLR_MASK_REG: [MBAR] + 8078h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 10	000000h RO	**RESERVED (RSVD):** Reserved.

Bit Range	Default & Access	Description
9: 5	00h RW	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots
4: 1	0h RW	**EP Number (EP_NUM):** 4bits of EP number
0	0b RW	**Clear Internal Scheduler's Mask (CISM):** This is a register that is used to clear the internal scheduler's mask that is used to stop scheduling a particular EP. Bit0 indicates the direction of the EP

14.7.146 Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG)—Offset 807Ch

Access Method

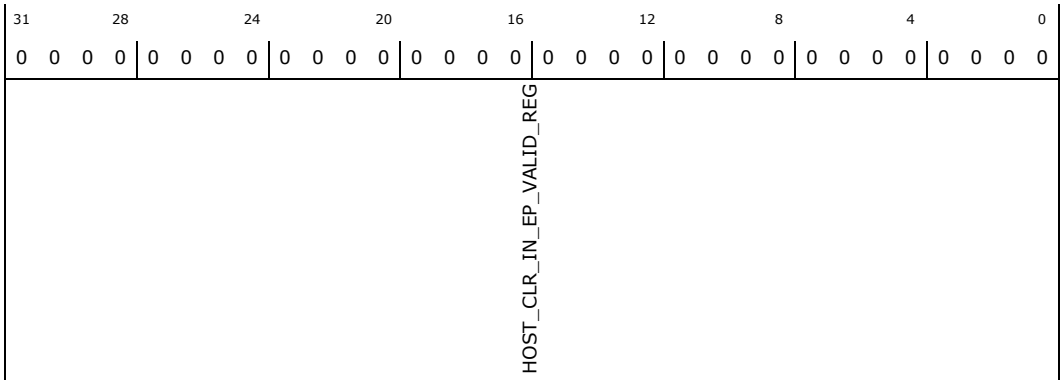
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CLR_IN_EP_VALID_REG: [MBAR] + 807Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 0	00000000h RW	**Clear Active IN EP ID Control (HOST_CLR_IN_EP_VALID_REG):** This register is used to clear the internal valid IN EP array that TRM stored in order to guarantee one IN EP per port. This register allows software to clear the valid bit of each port IN EP. This field indicates the port number. For a 2port configuration, only bit1:0 are valid. It can scale for the max number of ports that we support.

14.7.147 Clear Poll Mask Control (HOST_CLR_PMASK_REG)—Offset 8080h

Access Method

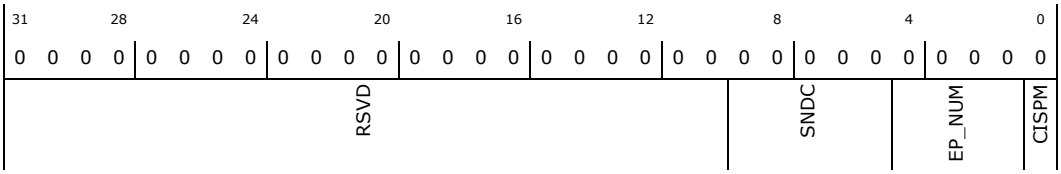
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CLR_PMASK_REG: [MBAR] + 8080h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 10	000000h RO	**RESERVED (RSVD):** Reserved.
9: 5	00h RW	**Slot Number Default Config (SNDC):** 5bits of slot number as a default configuration. It can scale to max of 128 slots
4: 1	0h RW	**EP Number (EP_NUM):** 4bits of EP number
0	0b RW	**Clear Internal Scheduler's Poll Mask (CISPM):** This is a register that is used to clear the internal scheduler's poll mask that is used to indicate whether we need to poll this EP. This is used for USB2. Bit0 indicates the direction of the EP

14.7.148 Host Control Scheduler (HOST_CTRL_SCH_REG)—Offset 8094h

Access Method

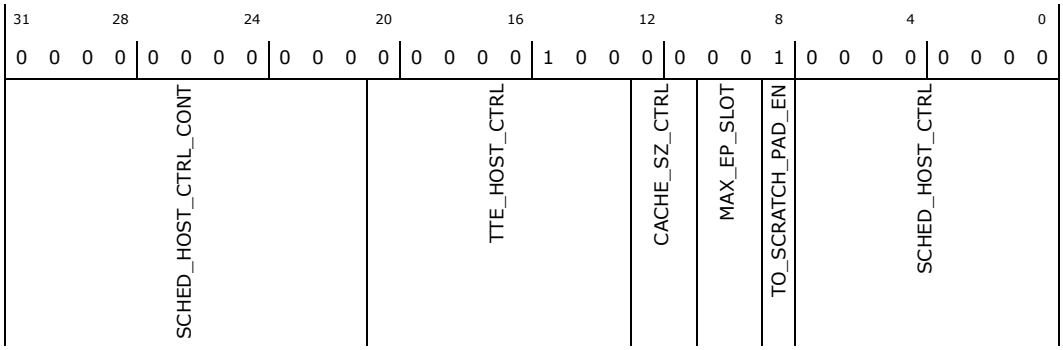
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CTRL_SCH_REG: [MBAR] + 8094h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00008100h



Bit Range	Default & Access	Description
31: 21	000h RW	**Scheduler Host Control Reg Cont (SCHED_HOST_CTRL_CONT):** method of USB2 port periodic done check (off by default)
20: 13	04h RW	**TTE Host Control (TTE_HOST_CTRL):** (0): disable interrupt complete split limit to 3 microframes (1): disable checking of missed microframes (2): disable split error request w/NULL pointer on speculative INs with data payload and no TRB. (3): disable deferred split error request on speculative IN with data payload and no TRB. (7:4): reserved
12: 11	0h RW	**Cache Size Control Reg (CACHE_SZ_CTRL):** 0: 64 1: 32 2,3: 16
10: 9	0h RW	**Maximum EP Per Slot (MAX_EP_SLOT):** 0: 32 1: 16 2: 8 3: 4
8	1b RW	**Turn on scratch_pad_en (TO_SCRATCH_PAD_EN):** Reserved.
7: 0	00h RW	**Scheduler Host Control Reg (SCHED_HOST_CTRL):** (0): disable poll delay (1): disable TRM active in EP valid check (2): enable TTE overlap prevention on interrupt IN EPs (at cost of possible service interval slip) (3) enable TTE overlap prevention on interrupt OUT EPs (at cost of possible service interval slip) (5:4) scheduler sort pattern 00 (default) search ISO ahead of interrupt within each service interval 01 - search USB2-ISO, USB3-ISO, USB2-Interrupt, USB3-Interrupt within each service interval 10 - search strictly by interval 11 - search all ISO intervals ahead interrupt intervals and within each interval, USB2 ahead of USB3 (6): disable 1 pack scheduling limit when ISO pending in present microframe (7): enable check to stop scheduling on port that are not connected

14.7.149 Global Port Control (HOST_CTRL_PORT_CTRL)—Offset 80A0h

Access Method

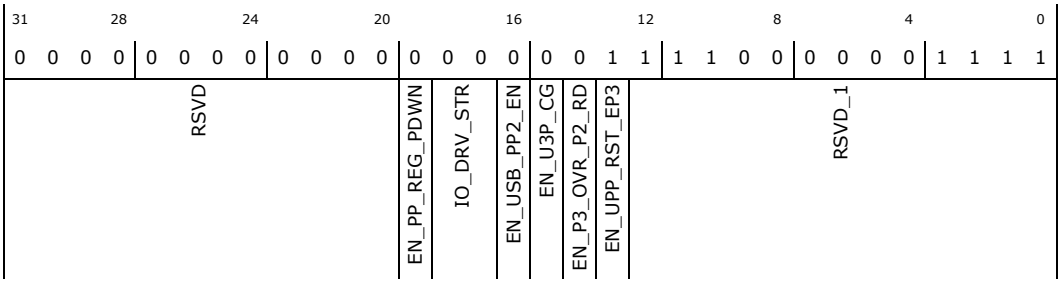
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CTRL_PORT_CTRL: [MBAR] + 80A0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00003C0Fh



Bit Range	Default & Access	Description
31: 20	000h RO	**RESERVED (RSVD):** Reserved.
19	0b RW	**Enable PCIe PHY Regulator Power Down (EN_PP_REG_PDWN):** 0: Disable PCIe PHY regulator power down mode 1: Enable PCIe PHY regulator power down mode
18: 17	0h RW	**IO Drive Strength (IO_DRV_STR):** This value defines IO drive strength
16	0b RW	**Enable USB PHY p2_EN (EN_USB_PP2_EN):** 0: Disable USB PHY P2_EN 1: Enable USB PHY P2_EN
15	0b RW	**Enable USB3 Port Clock Gate (EN_U3P_CG):** 0: Disable USB3 port clock gate 1: Enable USB3 port clock gate
14	0b RW	**Enable P3 Override P2 RxDetect (EN_P3_OVR_P2_RD):** 0: Disable P3 overriding P2 in RxDetect 1: Enable P3 overriding P2 in RxDetect
13	1b RW	**Enable USB PHY Pipe Reset Exit P3 (EN_UPP_RST_EP3):** 0: Disable a USB PHY pipe reset when exit P3 1: Enable a USB PHY pipe reset when exit P3
12: 0	1C0Fh RO	**RESERVED (RSVD_1):** Reserved.

14.7.150 AUX Reset Control (AUX_CTRL_REG)—Offset 80C0h

Access Method

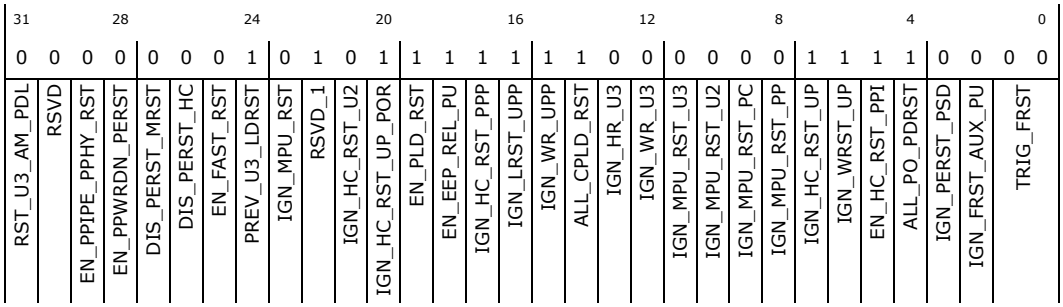
Type: Memory Mapped I/O Register (Size: 32 bits)

AUX_CTRL_REG: [MBAR] + 80C0h

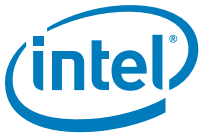
MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 015FC0F0h



Bit Range	Default & Access	Description
31	0b RW	**Reset USB3 AUX/Main PD Logic (RST_U3_AM_PDL):** A reset that is designed to reset all USB3 port AUX + Main power domain logic. This is a debug function. It is called cold reset. Write 1 to this register will issue a cold reset to USB3 ports.
30	0b RW	**RESERVED (RSVD):** Reserved.
29	0b RW	**Enable PCIe PIPE Reset As PCIe PHY Reset (EN_PPIPE_PPHY_RST):** This bit set to 1 selects the PCIe PIPE reset as a PCIe PHY power on reset. 0 selects the AUX powerup reset as a PCIe PHY powerup reset.
28	0b RW	**Ensure PIPE Powerdown On PERST# (EN_PPWRDN_PERST):** This bit ensures any PERST# being asserted will cause PIPE powerdown state transition to P1.
27	0b RW	**Disable PERST# Main RST (DIS_PERST_MRST):** There is a feature where we only allow PERST# to be treated as a main powerdown reset when it is asserted during the state that is not in D3. This bit disables this feature when it is set to 1. If this bit is set to 1, it means that any PERST# will be treated as a main power domain reset regardless of its Dstate.
26	0b RW	**Disable PCIe PERST# Host Controller (DIS_PERST_HC):** There is a feature where we can disable PCIe PERST# from reset the host controller until power management control module has done its clock switching. This is for a case where PM entered L23 and immediately PERST# asserted. This bit is designed to enable this feature when set to 1.
25	0b RW	**Enable Fast Simulation Reset Mode (EN_FAST_RST):** Enable a fast simulation mode for reset function. This is a feature for GLS
24	1b RW	**Prevent USB3 Link Down Reset (PREV_U3_LDRST):** When set to 1 prevent a reset being generated due to the USB3 port link down condition.
23	0b RW	**Ignore Main Power Up Reset (IGN_MPU_RST):** When set to 1 ignore the main power up reset for USB3 PIPE PHY reset.
22	1b RW	**RESERVED (RSVD_1):** Reserved.
21	0b RW	**Ignore HC Reset USB2 (IGN_HC_RST_U2):** When set to '1' ignore HC reset to reset the USB2 Port logic



Bit Range	Default & Access	Description
20	1b RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP_POR):** When set to '1' ignore HC reset to the USB PHY power-on reset
19	1b RW	**Enable PCIe Link-Down Reset (EN_PLD_RST):** Enable a reset due to a PCIe link-down condition. The PCIe link down condition will cause a HC reset liked. If this bit is set 1, the PCIe link down condition will only reset the PCIe core.
18	1b RW	**Enable EEPROM Reload On Power Up (EN_EEP_REL_PU):** When set to '1' enable EEPROM reload on every main power-up
17	1b RW	**Ignore HC Reset PCIe PHY PIPE (IGN_HC_RST_PPP):** When set to '1' ignore HC reset to the PCIe PHY PIPE reset
16	1b RW	**Ignore LTSSM Reset USB PHY PIPE (IGN_LRST_UPP):** When set to '1' ignore the LTSSM of USB link state transition caused reset to USB PHY PIPE reset
15	1b RW	**Ignore Warm Reset USB PHY Power (IGN_WR_UPP):** When set to '1' ignore warm reset the USB PHY power on reset
14	1b RW	**Allow Core PCIe Link Down Reset (ALL_CPLD_RST):** When set to '1' allow PCIe link down to cause a reset to the rest of the core
13	0b RW	**Ignore Hot Reset USB3 (IGN_HR_U3):** When set to '1' ignore hot reset to the USB3 port logic
12	0b RW	**Ignore Warm Reset USB3 (IGN_WR_U3):** When set to '1' ignore warm reset to the USB3 port logic
11	0b RW	**Ignore Main Power Up Reset USB3 (IGN_MPU_RST_U3):** When set to '1' ignore main power up reset to USB3 port logic
10	0b RW	**Ignore Main Power Up Reset USB2 (IGN_MPU_RST_U2):** When set to '1' ignore main power up reset to USB2 port logic
9	0b RW	**Ignore Main Power Up Reset PCIe Core (IGN_MPU_RST_PC):** When set to '1' ignore main power up reset to PCIe core
8	0b RW	**Ignore Main Power Up Reset PCIe PHY (IGN_MPU_RST_PP):** When set to '1' ignore main power up reset to PCIe PHY
7	1b RW	**Ignore HC Reset USB PHY (IGN_HC_RST_UP):** When set to '1' ignore HC reset to the USB PHY
6	1b RW	**Ignore Warm Reset USB PHY (IGN_WRST_UP):** When set to '1' ignore warm reset to the USB PHY
5	1b RW	**Enable HC Reset Per Port Isolation (EN_HC_RST_PPI):** Enables the HC reset or per port reset isolation function
4	1b RW	**Allow Power Off Power Domain Reset (ALL_PO_PDRST):** When set to '1' allow main power off condition to trigger a main power domain reset
3	0b RW	**Ignore Wait For PERST# During Power Show Down (IGN_PERST_PSD):** When set to '1' ignore waiting for PERST# deassertion during main power show down.
2	0b RW	**Ignore Fundamental Reset During AUX Power Up (IGN_FRST_AUX_PU):** When fundamental reset is asserted during AUX power up, if this bit is set, then we will ignore PERST# such that purely wait for timeout to deassert fundamental reset.
1: 0	0h RW	**Trigger Fundamental Reset (TRIG_FRST):** Writing to bit(1:0) to value of 2'b11 will cause a fundamental reset

14.7.151 Super Speed Bandwidth Overload (HOST_BW_OV_SS_REG)—Offset 80C4h

Access Method

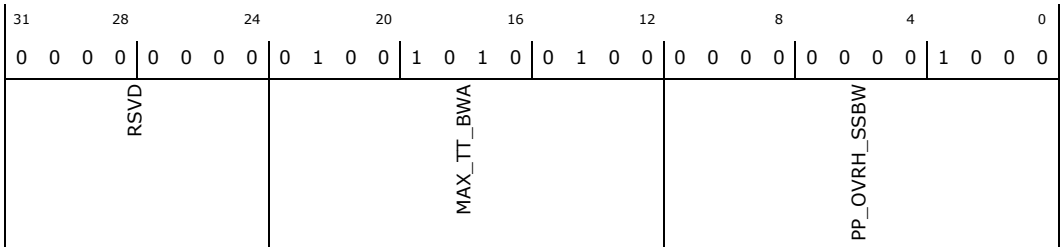
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_BW_OV_SS_REG: [MBAR] + 80C4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 004A4008h



Bit Range	Default & Access	Description
31: 24	00h RO	**RESERVED (RSVD):** Reserved.
23: 12	4A4h RW	**Max. TT BW Allowed (MAX_TT_BWA):** see white paper
11: 0	008h RW	**Per Packet Overhead SS BW (PP_OVRH_SSBW):** BW calculation: Overhead per packet for SS BW calculations. see white paper.

14.7.152 High Speed TT Bandwidth Overload (HOST_BW_OV_HS_REG)—Offset 80C8h

Access Method

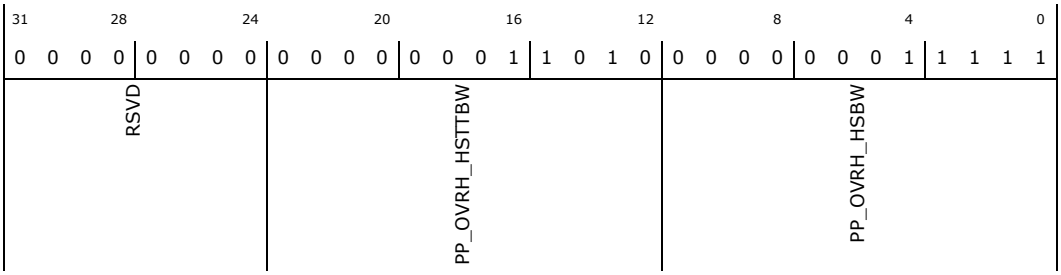
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_BW_OV_HS_REG: [MBAR] + 80C8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0001A01Fh



Bit Range	Default & Access	Description
31: 24	00h RO	**RESERVED (RSVD):** Reserved.
23: 12	01Ah RW	**Per Packet Overhead HS-TT BW (PP_OVRH_HSTTBW):** BW calculation: Overhead per packet for HS-TT BW calculations. see white paper.
11: 0	01Fh RW	**Per Packet Overhead HS BW (PP_OVRH_HSBW):** BW calculation: Overhead per packet for HS BW calculations. see white paper.

14.7.153 Bandwidth Overload Full Low Speed (HOST_BW_OV_FS_LS_REG)—Offset 80CCh

Access Method

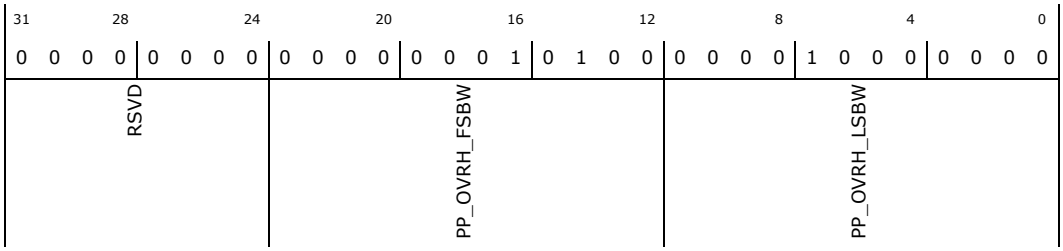
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_BW_OV_FS_LS_REG: [MBAR] + 80CCh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00014080h



Bit Range	Default & Access	Description
31: 24	00h RO	**RESERVED (RSVD):** Reserved.
23: 12	014h RW	**Per Packet Overhead FS BW (PP_OVRH_FSBW):** BW calculation: Overhead per packet for FS BW calculations. see white paper.
11: 0	080h RW	**Per Packet Overhead LS BW (PP_OVRH_LSBW):** BW calculation: Overhead per packet for LS BW calculations. see white paper.

14.7.154 System Bandwidth Overload (HOST_BW_OV_SYS_REG)—Offset 80D0h

Access Method

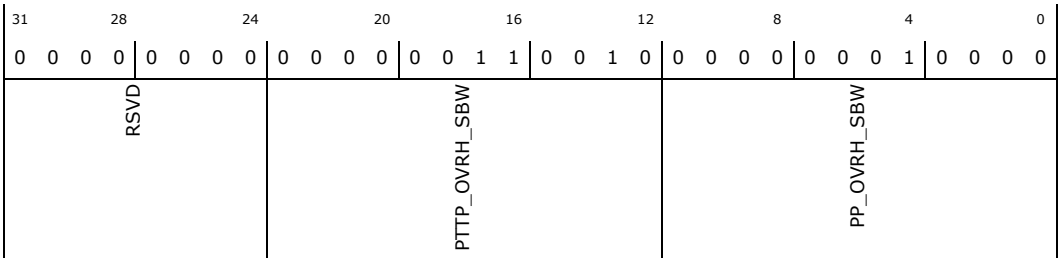
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_BW_OV_SYS_REG: [MBAR] + 80D0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00032010h



Bit Range	Default & Access	Description
31: 24	00h RO	**RESERVED (RSVD):** Reserved.
23: 12	032h RW	**Per TT Packet Overhead System BW (PTTP_OVRH_SBW):** BW calculation: Overhead per TT packet for System BW calculations. see white paper.
11: 0	010h RW	**Per Packet Overhead System BW (PP_OVRH_SBW):** BW calculation: Overhead per packet for System BW calculations. see white paper.

14.7.155 Scheduler Async Delay (HOST_CTRL_SCH_ASYNC_DELAY_REG)—Offset 80D4h

Global defaults for inserting delays between packets in the scheduler for async. types.

Access Method

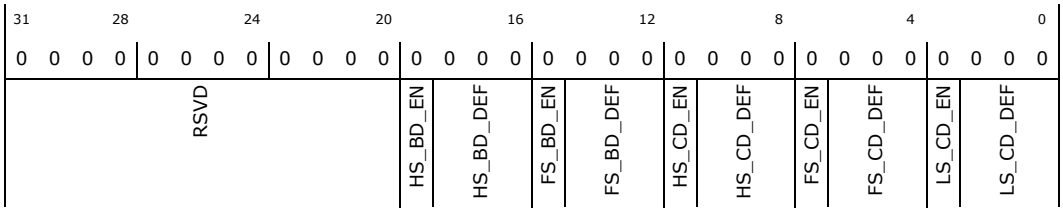
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CTRL_SCH_ASYNC_DELAY_REG: [MBAR] + 80D4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 20	000h RO	**RESERVED (RSVD):** Reserved.
19	0b RW	**High-Speed Bulk Delay Enable (HS_BD_EN):** Reserved.
18: 16	0h RW	**High-Speed Bulk Delay Default (HS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)
15	0b RW	**Full-Speed Bulk Delay Enable (FS_BD_EN):** Reserved.
14: 12	0h RW	**Full-Speed Bulk Delay Default (FS_BD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)
11	0b RW	**High-Speed Control Delay Enable (HS_CD_EN):** Reserved.
10: 8	0h RW	**High-Speed Control Delay Default (HS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)
7	0b RW	**Full-Speed Control Delay Enable (FS_CD_EN):** Reserved.
6: 4	0h RW	**Full-Speed Control Default (FS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)
3	0b RW	**Low-Speed Control Delay Enable (LS_CD_EN):** Reserved.
2: 0	0h RW	**Low-Speed Control Delay Default (LS_CD_DEF):** (0=125us,1=250us,2=500us,3=1ms,...)

14.7.156 AUX Power PHY Reset (UPORTS_PON_RST_REG)—Offset 80D8h

Access Method

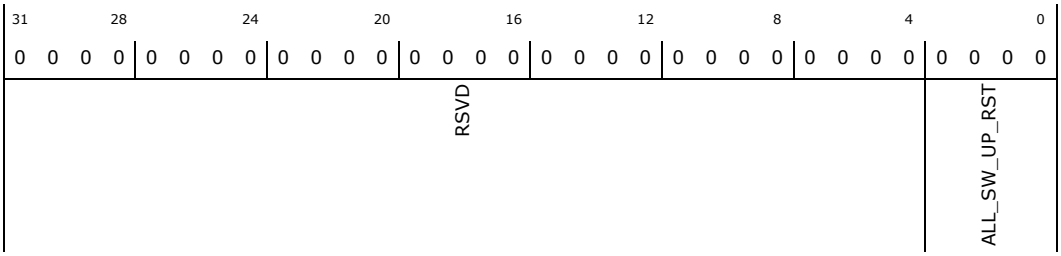
Type: Memory Mapped I/O Register (Size: 32 bits)

UPORTS_PON_RST_REG: [MBAR] + 80D8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 4	0000000h RO	**RESERVED (RSVD):** Reserved.
3: 0	0h WO	**Allow Software USB PHY RST (ALL_SW_UP_RST):** Allow a USB PHY reset being issued by software. Writing to this register with bit set to 1 will reset the USB PHY that is connected to the port. Bit3:0 indicates the port number of the USB PHY

14.7.157 AUX Power Management Control (AUX_CTRL_REG1)—Offset 80E0h

Access Method

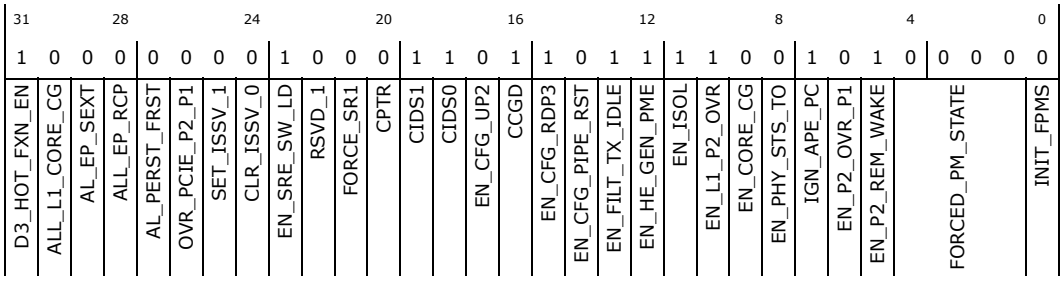
Type: Memory Mapped I/O Register (Size: 32 bits)

AUX_CTRL_REG1: [MBAR] + 80E0h

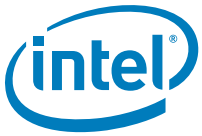
MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 808DBCA0h



Bit Range	Default & Access	Description
31	1b RW	**D3 Hot function enable register (D3_HOT_FXN_EN):** This bit is from pin input which is set 1. But we allow software to alter it if it is needed. 1: D3 hot enabled 0: D3 hot not abled.
30	0b RW	**Allow L1 Core Clock Gating (ALL_L1_CORE_CG):** When set to 1 allows core clock being gated during L1 state.
29	0b RW	**Allow Engine PHY Status Extension (AL_EP_SEXT):** When set to 1 allows the engine to extend PHY status of PCIe PIPE for one more cycle. This is due to the fact that our rate change function has a potential of not being able to sample the phystatus signal.
28	0b RW	**Allow Engine PCIe Rate Change Passing (ALL_EP_RCP):** When set to 1 allows the engine to pass PCIe rate change signal as it is from PCIe core to PCIe PHY.
27	0b RW	**Allow Engine PERST Fundamental Reset (AL_PERST_FRST):** When set to 1 allow engine to treat PERST# as a foundamental reset
26	0b RW	**Overwrite PCIe P2 to P1 (OVR_PCIE_P2_P1):** When set to 1 will overwrite a PCIe powerdown state of P2 to P1.
25	0b RW	**Set Internal SSV 1 (SET_ISSV_1):** When set to 1 set the internal SSV to 1.
24	0b RW	**Clear Internal SSV 0 (CLR_ISSV_0):** When set to 1 clear the internal SSV to 0.
23	1b RW	**Enable save_restore_enable SW Loading (EN_SRE_SW_LD):** This is a bit that enables the save_restore_enable signal being loaded when a software command has set Save bit. This is a debug function.
22	0b RW	**RESERVED (RSVD_1):** Reserved.
21	0b RW	**Force save_restore 1 (FORCE_SR1):** When set to 1, it will force the save_restore flag to 1. This flag is an bit to ensure that we have masked the update during low power state. If software write this bit to 1, it must write it to 0 in order to resume the normal save and restore function.



Bit Range	Default & Access	Description
20	0b RW	**cfg pcie txreg rd (CPTR):** Reserved.
19	1b RW	**cfg iob drivestrength[1] (CIDS1):** Reserved.
18	1b RW	**cfg iob drivestrength[0] (CIDS0):** Reserved.
17	0b RW	**Enable CFG USB P2 (EN_CFG_UP2):** When set to '1' enable cfg usb p2
16	1b RW	**cfg clk gate dis (CCGD):** Reserved.
15	1b RW	**Enable CFG RXDET P3 (EN_CFG_RDP3):** When set to '1' enable cfg rxdet p3
14	0b RW	**Enable CFG PIPE Reset (EN_CFG_PIPE_RST):** When set to '1' enable cfg pipe rst
13	1b RW	**Enable Filter TX Idle (EN_FILT_TX_IDLE):** When set to 1 enables a filter function to TX electrical idle signal at PCie PIPE. We have a filter that will set TXelecidle signal of PCIe PIPE to 1 whenever we are in isolation state or power down transition states.
12	1b RW	**Enable Host Engine Generate PME (EN_HE_GEN_PME):** This is a global switch to whether or not eable this host engine to generate PME message.
11	1b RW	**Enable Isolation (EN_ISOL):** When set to '1' enable isolation
10	1b RW	**Enable L1 Caused P2 Overwrite (EN_L1_P2_OVR):** Set 1 to enable a new feature. This new feature is designed to use L1 as a state to identify whether we should do P2 Overwrite or not. We used to use P1 state to identify whether or not to invoke P2 overwrite function.
9	0b RW	**Enable Core Clock Gating (EN_CORE_CG):** When set to '1' enable core clock gating based on low power state entered
8	0b RW	**Enable PHY Status Timeout (EN_PHY_STS_TO):** When set to '1' enable PHY status timeout function which is designed to cover the PCIePHY issue that we may have not able to detect the PHY status toggle.
7	1b RW	**Ignore aux_pm_en PCIe Core (IGN_APE_PC):** When set to '1' ignore the aux_pm_en reg from PCIe core to continue the remote wake/clock switching support
6	0b RW	**Enable P2 Overwrite P1 (EN_P2_OVR_P1):** When set to '1' enable P2 overwrite P1 when PCIe core has indicated the transition from P0 to P1. This is to enable entering the even lower power state.
5	1b RW	**Enable P2 Remote Wake (EN_P2_REM_WAKE):** When set 1 '1' enable the remote wake function by allowing P2 clock/switching and P2 entering
4: 1	0h RW	**Forced PM State (FORCED_PM_STATE):** Reserved.
0	0b RW	**Initiate Force PM State (INIT_FPMS):** When set to '1' force PM state to go to the state indicated in bit 4:1

14.7.158 Battery Charge (BATTERY_CHARGE_REG)—Offset 80E4h

Access Method

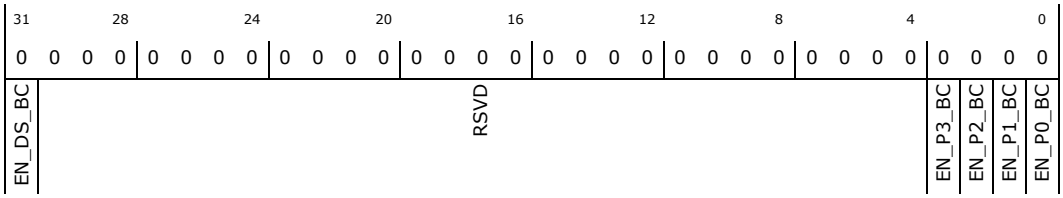
Type: Memory Mapped I/O Register (Size: 32 bits)

BATTERY_CHARGE_REG: [MBAR] + 80E4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Enable DM_SRC Battery Charge (EN_DS_BC):** 1 - Always enable battery charge DM_SRC if not connected. Don't wait for portable device detect. (spec. ver. 1.2) 0 - Battery charge spec ver. 1.1.
30: 4	0000000h RO	**RESERVED (RSVD):** Reserved.
3	0b RW	**Enable Port 3 Battery Charging (EN_P3_BC):** 0 - Battery charging disabled (Physical Port #3) 1 - Battery charging enabled (Physical Port #3)
2	0b RW	**Enable Port 2 Battery Charging (EN_P2_BC):** 0 - Battery charging disabled (Physical Port #2) 1 - Battery charging enabled (Physical Port #2)
1	0b RW	**Enable Port 1 Battery Charging (EN_P1_BC):** 0 - Battery charging disabled (Physical Port #1) 1 - Battery charging enabled (Physical Port #1)
0	0b RW	**Enable Port 0 Battery Charging (EN_P0_BC):** 0 - Battery charging disabled (Physical Port #0) 1 - Battery charging enabled (Physical Port #0)

14.7.159 Port Watermark (HOST_CTRL_WATERMARK_REG)—Offset 80E8h

Access Method

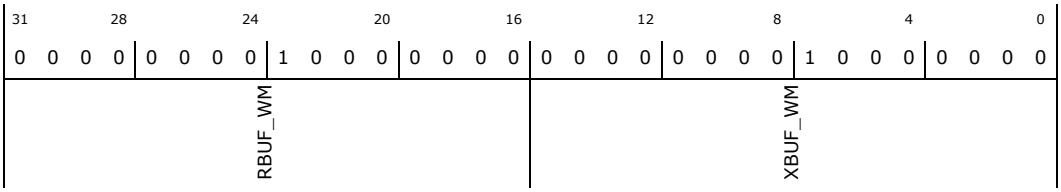
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CTRL_WATERMARK_REG: [MBAR] + 80E8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00800080h



Bit Range	Default & Access	Description
31: 16	0080h RW	**RBUF water mark (RBUF_WM):** Reserved.
15: 0	0080h RW	**XBUF water mark (XBUF_WM):** Reserved.

14.7.160 SuperSpeed Port Link Control (HOST_CTRL_PORT_LINK_REG)—Offset 80ECh

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CTRL_PORT_LINK_REG: [MBAR] + 80ECh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 18010600h

Bit Range	Default & Access	Description
31: 27	03h RW	**Force LTSSM State (FORCE_LTSSM_ST):** LTSSM state to be forced This value is for test purpose only.

Bit Range	Default & Access	Description
26	0b RW	**Direct Link LTSSM State (DL_LTSSM_ST):** 0: Normal operation mode 1: Direct link to a specific state specified by bit 31:27 This bit is for test purpose only. It shall be written 0 in normal operation mode.
25	0b RW	**Direct Link To U0 (DL_U0):** 0: Normal operation mode 1: Direct link to U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
24: 21	0h RW	**Forced Compliance Pattern (FORCED_CMP_PAT):** Compliance pattern to be forced to enter compliance mode This value is for test purpose only.
20	0b RW	**Enable Link Error Slave Count (EN_LES_CNT):** 0: Disable link error slave count 1: Enable link error slave count
19: 17	0h RW	**Debug Mode Select (DEBUG_MD_SEL):** Reserved.
16: 15	2h RW	**PHY Low Power Latency (PHY_LP_LAT):** This field defines the latency to drive the PHY to enter low power mode 0: 4 cycles 1: 8 cycles 2: 16 cycles 3: 32 cycles
14: 12	0h RW	**Link Recovery Minimum Time (LR_MIN_TM):** This value defines the minimum time for the link to stay in Recovery.Active other than from U3. The granuity is 128us.
11: 9	3h RW	**Link Polling Minimum Time (LP_MIN_TM):** This value defines the minimum time for the link to stay in Polling.Active and Recovery.Active from U3. The granuity is 128us.
8	0b RW	**Force Link Accept PM Command (FORCE_LA_PMC):** 0: Normal operation mode 1: Force link to accept power management command
7	0b RW	**Direct Link Recovery U0 (DL_REC_U0):** 0: Normal operation mode 1: Direct link to Recovery from U0
6	0b RW	**Link Fast Training Mode (LINK_FTM):** 0: Normal operation mode 1: Link fast training mode This bit should be written 0 in normal operation.
5	0b RW	**Disable Link Scrambler (DIS_LINK_SCRAM):** 0: Enable link scrambler 1: Disable link scramber
4	0b RW	**Direct Link U3 From U0 (DL_U3_U0):** 0: Normal operation mode 1: Direct link to U3 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
3	0b RW	**Direct Link U3 From U0 (DL_U2_U0):** 0: Normal operation mode 1: Direct link to U2 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
2	0b RW	**Direct Link U3 From U0 (DL_U1_U0):** 0: Normal operation mode 1: Direct link to U1 from U0 This bit is for test purpose only. It shall be written 0 in normal operation mode.
1	0b RW	**Enable Link Loopback Master Mode (EN_LINK_LB_MAST):** 0: Disable link loopback master mode 1: Enable link loopback master mode
0	0b RW	**Disable Link Compliance Mode (DIS_LINK_CM):** 0: Enable link compliance mode 1: Disable link compliance mode

14.7.161 USB2 Port Link Control 1 (USB2_LINK_MGR_CTRL_REG1)—Offset 80F0h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

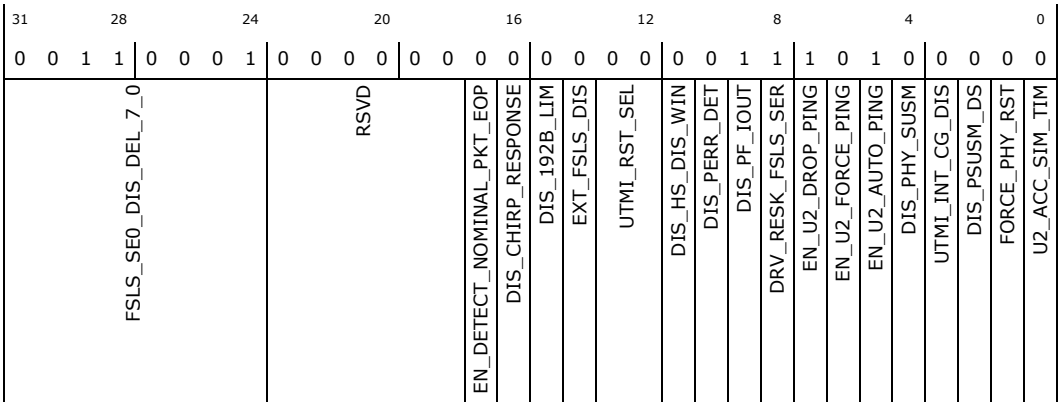
Type: Memory Mapped I/O Register (Size: 32 bits)

USB2_LINK_MGR_CTRL_REG1: [MBAR] + 80F0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 310003A0h



Bit Range	Default & Access	Description
31: 24	31h RW	**FS/LS Mode SE0 Disconnect Delay[7:0] (FSLS_SE0_DIS_DEL_7_0):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.
23: 18	00h RW	**Reserved (RSVD):** Reserved.
17	0b RW	**EN_DETECT_NOMINAL_PKT_EOP (EN_DETECT_NOMINAL_PKT_EOP):** 0: Detect minimal packet EOP. 1: Detect nominal packet EOP.
16	0b RW	**Disable Chirp Response (DIS_CHIRP_RESPONSE):** 0: Normal 1: Force full speed on host ports (disable chirp response)
15	0b RW	**Disable 192 Byte Limit Check (DIS_192B_LIM):** 0: Enforce 192 byte limit on complete-split INs. Treat any packet) 192 as babble case. 1: Disable 192 byte limit check.
14	0b RW	**External Provided FS/LS Disconnect (EXT_FSLS_DIS):** 0: Internal FS/LS Disconnect from linestate(1:0) 1: External provided FS/LS Disconnect from hostdisconnect input
13: 12	0h RW	**UTMI Reset Source Select (UTMI_RST_SEL):** Select UTMI Reset Source (FRD UTMI Reset Only) 00: HCReset or Force PHY Reset or internal reset after disconnect/suspend for restart (default) 01,11: UTMI reset = ~UTMI suspendm 10: UTMI reset = ~UTMI suspendm and synchronization to port clk.
11	0b RW	**Disable HS Disconnect Window (DIS_HS_DIS_WIN):** 0: Enable HS Disconnect Window Function 1: Disable HS Disconnect Window Function
10	0b RW	**Disable Port Error Detection (DIS_PERR_DET):** 0: Enable Port Error Detection (default) 1: Disable Port Error Detection

Bit Range	Default & Access	Description
9	1b RW	**Disable Peek Function for ISO-OUT (DIS_PF_IOUT):** 0: Enable Peek function for ISO-OUT (default) 1: Disable Peek function for ISO-OUT
8	1b RW	**Drive Resume-K FS/LS Serial Interface (DRV_RESK_FSLS_SER):** 0: Drive Resume-K on parallel Interface 1: Drive Resume-K directly on FS/LS Serial Interface (default)
7	1b RW	**Enable USB2 Drop-Ping (EN_U2_DROP_PING):** 0: Disable Drop-Ping Function in USB2 Protocol (default) 1: Enable Drop-Ping Function in USB2 Protocol
6	0b RW	**Enable USB2 Force-Ping (EN_U2_FORCE_PING):** 0: Disable Force-Ping Function in USB2 Protocol (default) 1: Enable Force-Ping Function in USB2 Protocol
5	1b RW	**Enable USB2 Auto-Ping (EN_U2_AUTO_PING):** 0: Disable Auto-Ping Function 1: Enable Auto-Ping Function in USB2 Protocol (default)
4	0b RW	**Disable PHY SuspendM (DIS_PHY_SUSM):** 0: PHY is suspend=U3,U2,disconnect (default) 1: Disable PHY SuspendM in All States
3	0b RW	**UTMI Internal Clock Gate Disable (UTMI_INT_CG_DIS):** 0: Normal operation (internal clock gated in U2,U3,disconnect) 1: UTMI Internal Clock Gate Disable
2	0b RW	**Disable PHY SuspendM in Disconnect State (DIS_PSUSM_DS):** 0: PHY is suspendM=0 in Disconnect State (default) 1: Disable PHY SuspendM in Disconnect State
1	0b RW	**Force PHY Reset (FORCE_PHY_RST):** 0: Normal Operation (default) 1: Force PHY Reset
0	0b RW	**USB2 Accelerated Simulation Timing (U2_ACC_SIM_TIM):** 0: Normal Operation (default - FPGA/ASIC) 1: USB2 Accelerated Simulation Timing (default - simulation)

14.7.162 USB2 Port Link Control 2 (USB2_LINK_MGR_CTRL_REG2)—Offset 80F4h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

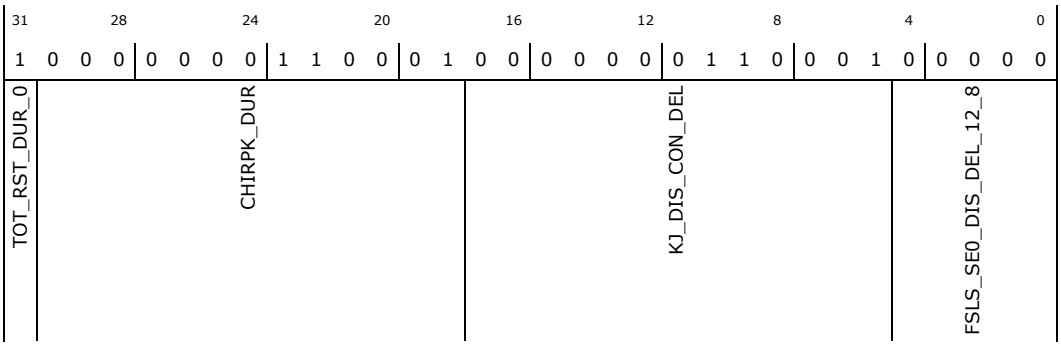
Type: Memory Mapped I/O Register (Size: 32 bits)

USB2_LINK_MGR_CTRL_REG2: [MBAR] + 80F4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 80C40620h



Bit Range	Default & Access	Description
31	1b RW	**Total Reset Duration[0] (TOT_RST_DUR_0):** # of microseconds for total reset duration
30: 18	0031h RW	**Chirp-K Duration (CHIRPK_DUR):** # of microseconds of Chirp-K to register that a device is chirping
17: 5	0031h RW	**K/J Disconnect Connect Delay (KJ_DIS_CON_DEL):** # of microseconds of K/J in disconnected state to register connect has occurred.
4: 0	00h RW	**FS/LS Mode SE0 Disconnect Delay[12:8] (FSLS_SE0_DIS_DEL_12_8):** # of microseconds of SE0 in FS/LS mode to register disconnect had occurred.

14.7.163 USB2 Port Link Control 3 (USB2_LINK_MGR_CTRL_REG3)—Offset 80F8h

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

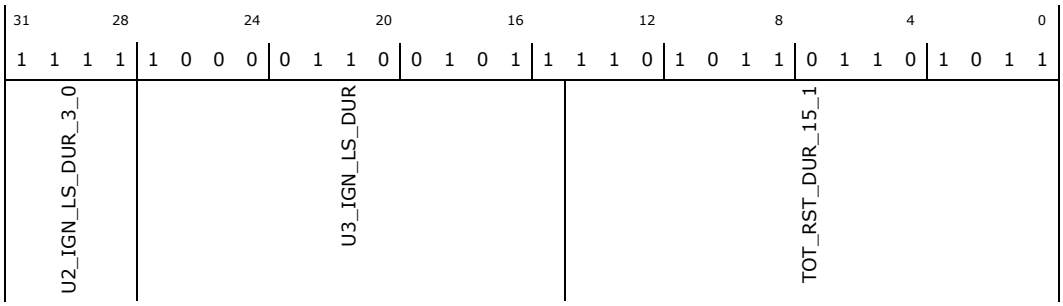
Type: Memory Mapped I/O Register (Size: 32 bits)

USB2_LINK_MGR_CTRL_REG3: [MBAR] + 80F8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: F865EB6Bh



Bit Range	Default & Access	Description
31: 28	Fh RW	**U2 Entry Ignore Linestate Changes Duration[3:0] (U2_IGN_LS_DUR_3_0):** # of microseconds after entering U2, linestate changes are ignored as bus settles
27: 15	10CBh RW	**U3 Entry Ignore Linestate Changes Duration (U3_IGN_LS_DUR):** # of microseconds after entering U3, linestate changes are ignored as bus settles
14: 0	6B6Bh RW	**Total Reset Duration[15:1] (TOT_RST_DUR_15_1):** # of microseconds for total reset duration

14.7.164 USB2 Port Link Control 4 (USB2_LINK_MGR_CTRL_REG4)—Offset 80FCh

These set of registers is used to control jey USB set of timers. They are spread over 4 registers each 32 bits wide.

Access Method

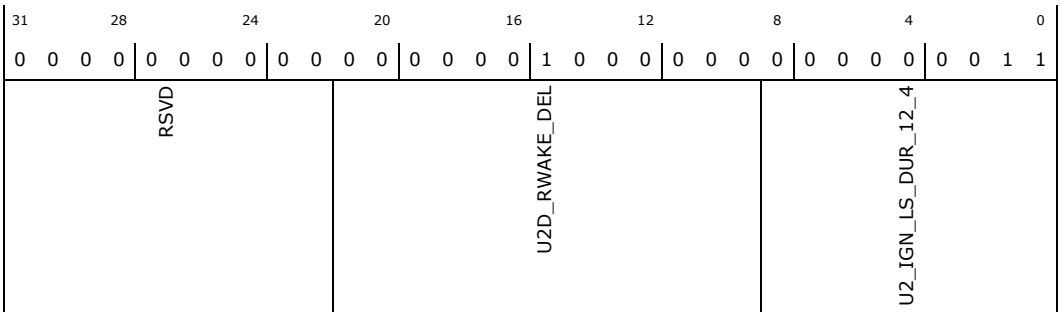
Type: Memory Mapped I/O Register (Size: 32 bits)

USB2_LINK_MGR_CTRL_REG4: [MBAR] + 80FCh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00008003h



Bit Range	Default & Access	Description
31: 22	000h RO	**RESERVED (RSVD):** Reserved.
21: 9	0040h RW	**U2 Detect Remote Wake Delay (U2D_RWAKE_DEL):** #of microseconds after detecting U2 remote wake condition to reflect K
8: 0	003h RW	**U2 Entry Ignore Linestate Changes Duration[12:4] (U2_IGN_LS_DUR_12_4):** # of microseconds after entering U2, linestate changes are ignored as bus settles

14.7.165 Bandwidth Calc Control (HOST_CTRL_BW_CTRL_REG)—Offset 8100h

Access Method

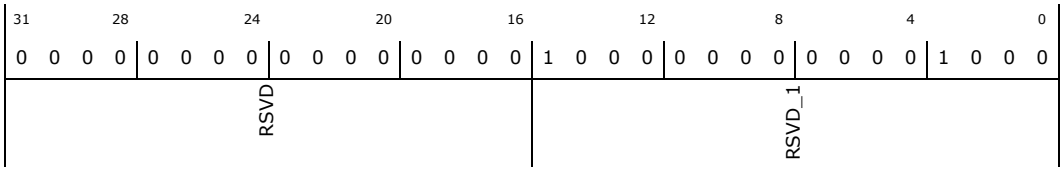
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_CTRL_BW_CTRL_REG: [MBAR] + 8100h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00008008h



Bit Range	Default & Access	Description
31: 16	0000h RO	**Reserved (RSVD):** Reserved.
15: 0	8008h RW	**Reserved (RSVD_1):** Reserved.

14.7.166 Host Interface Control (HOST_IF_CTRL_REG)—Offset 8108h

Access Method

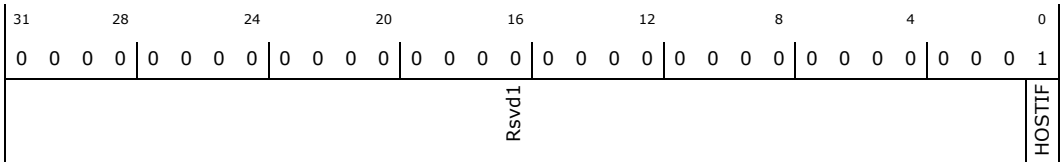
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_IF_CTRL_REG: [MBAR] + 8108h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000001h



Bit Range	Default & Access	Description
31: 1	00000000h RW	**Rsvd1 (Rsvd1):** Reserved.
0	1b RW	**Host IF (HOSTIF):** Reserved.

14.7.167 Bandwidth Overload Burst (HOST_BW_OV_BURST_REG)—Offset 810Ch

Access Method

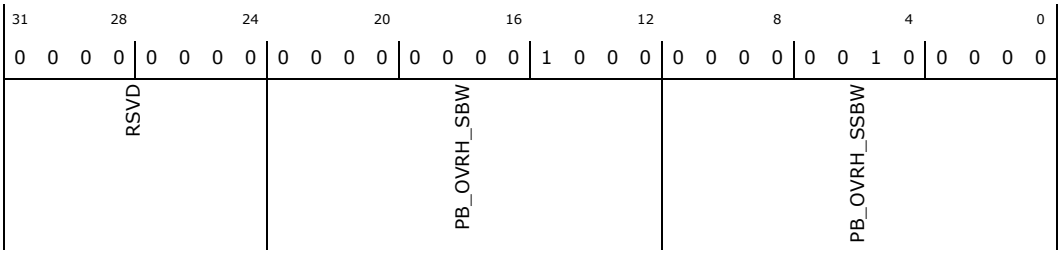
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_BW_OV_BURST_REG: [MBAR] + 810Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00008020h



Bit Range	Default & Access	Description
31: 24	00h RO	**RESERVED (RSVD):** Reserved.
23: 12	008h RW	**Per Burst Overhead System BW (PB_OVRH_SBW):** BW calculation: Overhead per burst for system BW calculations. see white paper.
11: 0	020h RW	**Per Burst Overhead System BW (PB_OVRH_SSBW):** BW calculation: Overhead per burst for SS BW calculations. see white paper.

14.7.168 USB Max Bandwidth Control 4 (HOST_CTRL_BW_MAX_REG)—Offset 8128h

Access Method

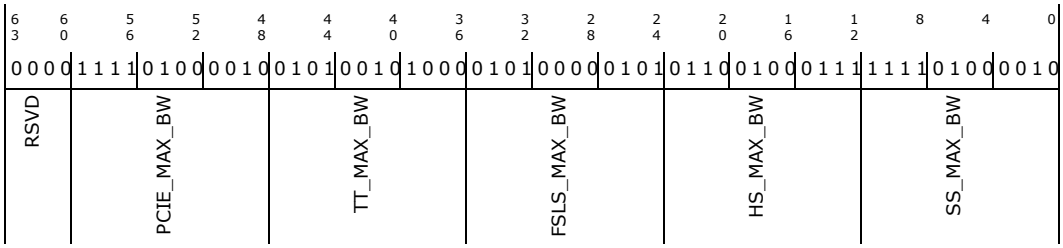
Type: Memory Mapped I/O Register (Size: 64 bits)

HOST_CTRL_BW_MAX_REG: [MBAR] + 8128h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0F42528505647F00h



Bit Range	Default & Access	Description
63: 60	0h RO	**Reserved (RSVD):** Reserved.
59: 48	F42h RW	**PCIe Max BW Units (PCIE_MAX_BW):** Max. Number of BW units for PCIe (system interface) (denominator in 90% calculation)
47: 36	528h RW	**TT Max BW Units (TT_MAX_BW):** Max. Number of BW units for TTs. (denominator in 90% calculation)
35: 24	505h RW	**FS/LS Max BW Units (FSLS_MAX_BW):** Max. Number of BW units for FS/LS ports. (denominator in 90% calculation)
23: 12	647h RW	**HS Max BW Units (HS_MAX_BW):** Max. Number of BW units for HS ports. (denominator in 80% calculation)
11: 0	F42h RW	**SS Max BW Units (SS_MAX_BW):** Max. Number of BW units for SS ports. (denominator in 90% calculation)

14.7.169 USB2 Linestate Debug (LINESTATE_DEBUG_REG)—Offset 8130h

Access Method

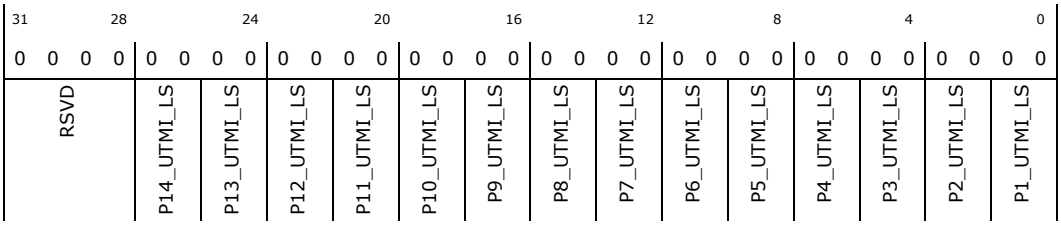
Type: Memory Mapped I/O Register (Size: 32 bits)

LINESTATE_DEBUG_REG: [MBAR] + 8130h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 28	0h RO	**RESERVED (RSVD):** Reserved.
27: 26	0h RO	**Port 14 UTMI Linestate (P14_UTMI_LS):** Reserved.
25: 24	0h RO	**Port 13 UTMI Linestate (P13_UTMI_LS):** Reserved.
23: 22	0h RO	**Port 12 UTMI Linestate (P12_UTMI_LS):** Reserved.
21: 20	0h RO	**Port 11 UTMI Linestate (P11_UTMI_LS):** Reserved.
19: 18	0h RO	**Port 10 UTMI Linestate (P10_UTMI_LS):** Reserved.
17: 16	0h RO	**Port 9 UTMI Linestate (P9_UTMI_LS):** Reserved.
15: 14	0h RO	**Port 8 UTMI Linestate (P8_UTMI_LS):** Reserved.
13: 12	0h RO	**Port 7 UTMI Linestate (P7_UTMI_LS):** Reserved.
11: 10	0h RO	**Port 6 UTMI Linestate (P6_UTMI_LS):** Reserved.
9: 8	0h RO	**Port 5 UTMI Linestate (P5_UTMI_LS):** Reserved.
7: 6	0h RO	**Port 4 UTMI Linestate (P4_UTMI_LS):** Reserved.
5: 4	0h RO	**Port 3 UTMI Linestate (P3_UTMI_LS):** Reserved.
3: 2	0h RO	**Port 2 UTMI Linestate (P2_UTMI_LS):** Reserved.
1: 0	0h RO	**Port 1 UTMI Linestate (P1_UTMI_LS):** Reserved.

14.7.170 USB2 Protocol Gap Timer (USB2_PROTOCOL_GAP_TIMER_REG)—Offset 8134h

Access Method

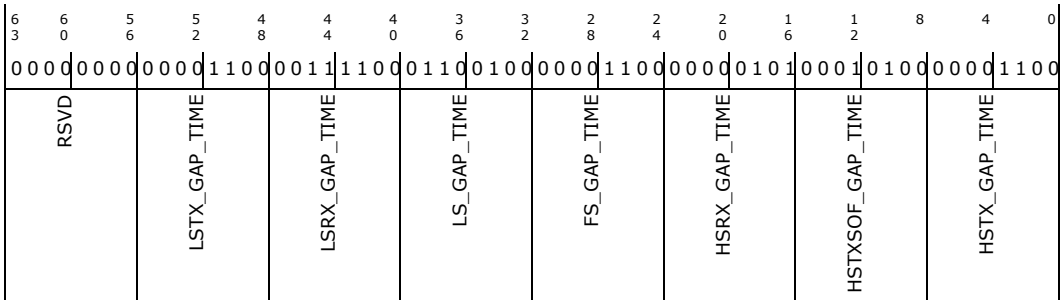
Type: Memory Mapped I/O Register (Size: 64 bits)

USB2_PROTOCOL_GAP_TIMER_REG: [MBAR] + 8134h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 000C3C640C05140Ch



Bit Range	Default & Access	Description
63: 56	00h RO	**Reserved (RSVD):** Reserved.
55: 48	0ch RW	**GAP time after LS TX thru FS hub (LSTX_GAP_TIME):** Reserved.
47: 40	3ch RW	**GAP time after LS RX thru FS hub (LSRX_GAP_TIME):** Reserved.
39: 32	64h RW	**GAP timer after LS (LS_GAP_TIME):** Reserved.
31: 24	0ch RW	**GAP time after FS (FS_GAP_TIME):** Reserved.
23: 16	05h RW	**GAP time after HS RX (HSRX_GAP_TIME):** Reserved.
15: 8	14h RW	**GAP time after HS TX SOF (HSTXSOF_GAP_TIME):** Reserved.
7: 0	0ch RW	**GAP time HS TX Packet (HSTX_GAP_TIME):** Reserved.

14.7.171 USB2 Protocol Bus Timeout Timer (USB2_PROTOCOL_BTO_TIMER_REG)—Offset 813Ch

Access Method

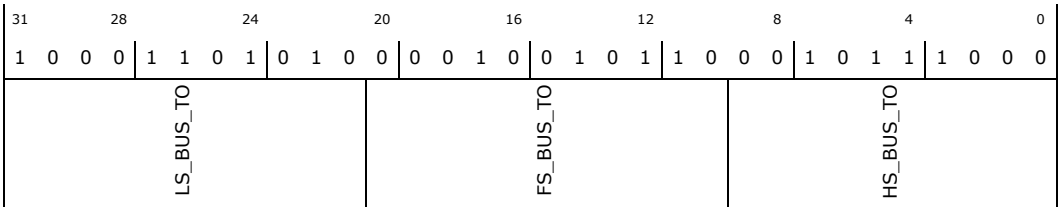
Type: Memory Mapped I/O Register (Size: 32 bits)

USB2_PROTOCOL_BTO_TIMER_REG: [MBAR] + 813Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 8D4258B8h



Bit Range	Default & Access	Description
31: 21	46ah RW	**Bus timeout count for LS (LS_BUS_TO):** Reserved.
20: 10	096h RW	**Bus timeout count for FS (FS_BUS_TO):** Reserved.
9: 0	0b8h RW	**Bus timeout count for HS (HS_BUS_TO):** Reserved.

14.7.172 Power Scheduler Control-0 (PWR_SCHED_CTRL0)—Offset 8140h

Access Method

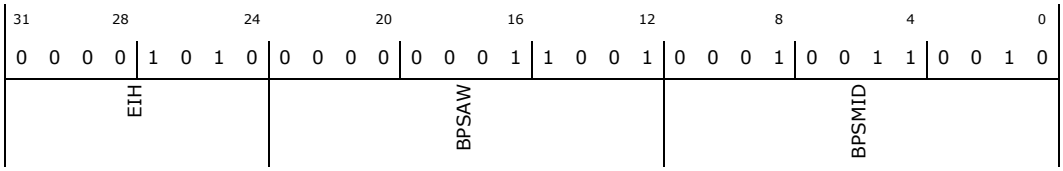
Type: Memory Mapped I/O Register (Size: 32 bits)

PWR_SCHED_CTRL0: [MBAR] + 8140h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0A019132h



Bit Range	Default & Access	Description
31: 24	0ah RW	**Engine Idle Hysteresis (EIH):** This register controls the min. idle span that has to be observed from the engine idle indicators before the power state flags (xhc_*_idle) will indicate a 1.
23: 12	019h RW	**Backbone PLL Shutdown Advance Wake (BPSAW):** This register controls the time before the next scheduled transaction where the Backbone PLL request will assert. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)
11: 0	132h RW	**Backbone PLL Shutdown Min. Idle Duration (BPSMID):** The sum of this register plus the Backbone PLL Shutdown Advance Wake form to a Total Idle time. When the next scheduled periodic transaction is after present time + Total Idle, the Backbone PLL request will de-assert, allowing the PLL to shutdwon. Register Format: Bits [11:7] # of 125us uframes Bits [6:0] # of microseconds (0-124)

14.7.173 Power Scheduler Control-2 (PWR_SCHED_CTRL2)—Offset 8144h

These bit enable by EP type those EPs classes that are considered for determining next periodic active interval for pre-wake of the periodic_active signal. EP classes that are disabled may never be observed in setting of the periodic_active signal.

Access Method

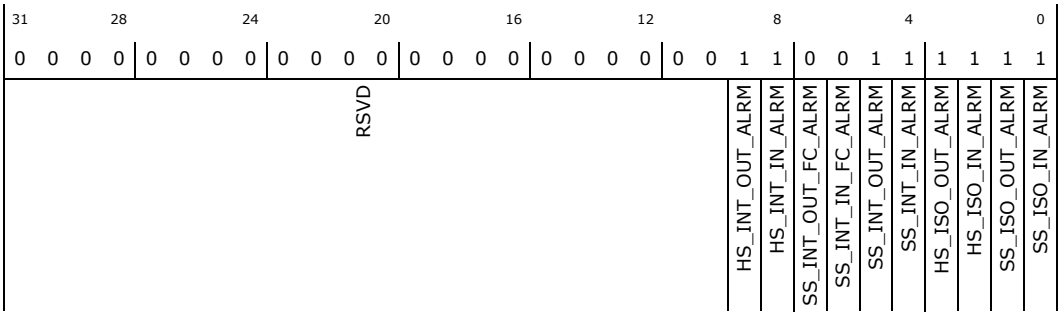
Type: Memory Mapped I/O Register (Size: 32 bits)

PWR_SCHED_CTRL2: [MBAR] + 8144h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0000033Fh



Bit Range	Default & Access	Description
31: 10	000000h RO	**Reserved (RSVD):** Reserved.
9	1b RW	**HS Interrupt-OUT Alarm (HS_INT_OUT_ALRM):** Reserved.
8	1b RW	**HS Interrupt-IN Alarm (HS_INT_IN_ALRM):** Reserved.
7	0b RW	**SS Interrupt-OUT FC Alarm (SS_INT_OUT_FC_ALRM):** Reserved.
6	0b RW	**SS Interrupt-IN Alarm (SS_INT_IN_FC_ALRM):** Reserved.
5	1b RW	**SS Interrupt-OUT & not in FC Alarm (SS_INT_OUT_ALRM):** Reserved.
4	1b RW	**SS Interrupt-IN & not in FC Alarm (SS_INT_IN_ALRM):** Reserved.
3	1b RW	**HS ISO-OUT Alarm (HS_ISO_OUT_ALRM):** Reserved.
2	1b RW	**HS ISO-IN Alarm (HS_ISO_IN_ALRM):** Reserved.
1	1b RW	**SS ISO-OUT Alarm (SS_ISO_OUT_ALRM):** Reserved.
0	1b RW	**SS ISO-IN Alarm (SS_ISO_IN_ALRM):** Reserved.

14.7.174 Latency Tolerance Control 0 (HOST_IF_LAT_TOL_CTRL_REG0)—Offset 8150h

The Latency Tolerance Control Register is used by SW to control which BELT is returned when this register is read. SW shall write to this register to program a Slot-ID, Port-ID and BELT Select to determine which BELT is selected. When this register is read the selected BELT is returned.

Access Method

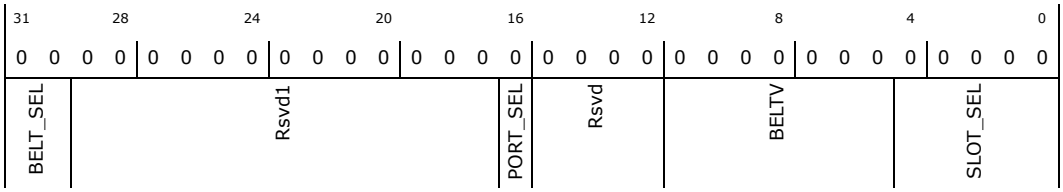
Type: Memory Mapped I/O Register (Size: 32 bits)

HOST_IF_LAT_TOL_CTRL_REG0: [MBAR] + 8150h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 30	0h WO	**BELT Select (BELT_SEL):** This field determines what value will be selected to read back from SW when reading this register 0: Returns the SW programmed Latency Tolerance Value 1: Returns the Lowest BELT in the Host 2: Returns the BELT for the requested Slot-ID (Slot Select) 3: Returns the BELT for the requested Port-ID (Port Select)
29: 17	0h RO	**Rsvd1 (Rsvd1):** Reserved.
16	0h WO	**Port Select (PORT_SEL):** Used to select the BELT for a given Port # when the BELT Select is programmed to select the Port-ID (this field is 0 based)
15: 12	0h RO	**Rsvd (Rsvd):** Reserved.
11: 5	0h RO	**BELT Value (BELTV):** Value of selected BELT is return in this field
4: 0	00h RW	**Slot Select (SLOT_SEL):** Reads will return: BELT Value (BELTV) [4:0]: Value of selected BELT is return in this field Writes will control : Slot Select (): Used to select the BELT for a given Slot # when the BELT Select is programmed to select the Slot-ID (this field is zero based)

14.7.175 AUX Power Management Control (AUX_CTRL_REG2)—Offset 8154h

Access Method

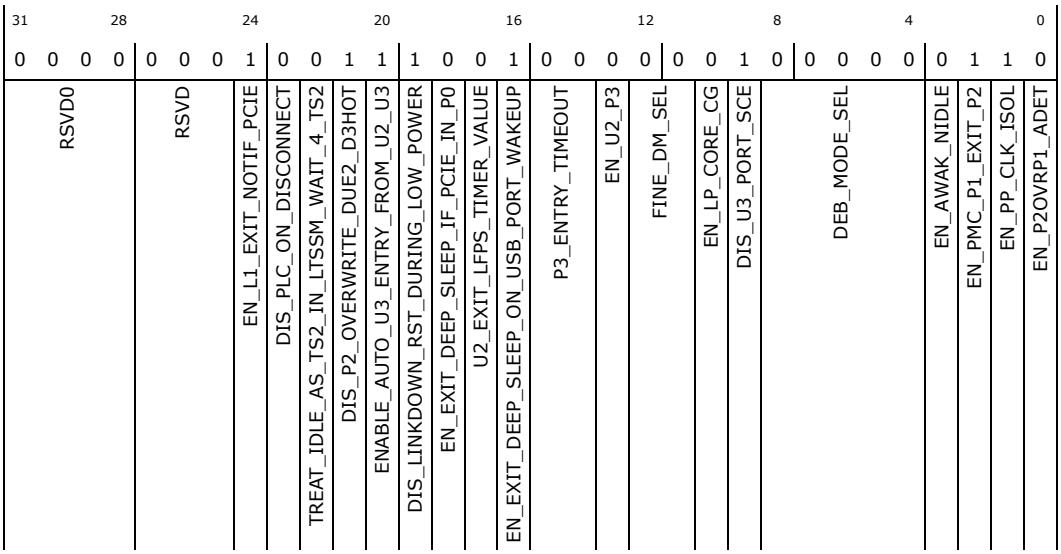
Type: Memory Mapped I/O Register (Size: 32 bits)

AUX_CTRL_REG2: [MBAR] + 8154h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 01390206h



Bit Range	Default & Access	Description
31: 28	0h RW	**RESERVED0 (RSVD0):** Reserved.
27: 25	0h RW	**RESERVED (RSVD):** Reserved.
24	1b RW	**Enable L1 exit notification to SNPS PCIe core (EN_L1_EXIT_NOTIF_PCIE):** This bit enables a L1 exit notification to SNPS PCIe core. There is a case where USB ports have waked up and AUX PM module has started the wakeup process. The AUX PM control state got into a wait for P0 state because it needs to wait until PCIe core to signal powerdown state change. Due to the fact that the core is in D3Hot, there is no run_stop bit set such that no internal interrupt will be fired. This causes the LTSSM of PCIe stayed in L1 even though AUX PM has known that it needs an L1 exit. This bit works together with bit21 of this register. 1: enables this feature 0: disables this feature.
23	0b RW	**DISABLE PLC ON DISCONNECT (DIS_PLC_ON_DISCONNECT):** 1: do not assert PLC for disconnection 0: assert PLC for disconnection
22	0b RW	**TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2 (TREAT_IDLE_AS_TS2_IN_LTSSM_WAIT_4_TS2):** This bit enables a feature in PCie core LTSSM to treat IDLE received as TS2 when LTSSM is in wait for TS2 receive state. This is a function requested from PHY where it is possible to not able to receive TS2 without error. 1: treat Logic IDLE as TS2 received when in some PCIe LTSSM state. 0: disable this feature.
21	1b RW	**Disable p2 overwrite due to the D3HOT where PCIe core enters the L1 (DIS_P2_OVERWRITE_DUE2_D3HOT):** We added a feature where if PCIe core LTSSM enters L1 due to the D3hot, the aux PM control will not start a P2 overwrite function in anticipating for the next L23 enter. 1: disables p2 overwrite due to the D3HOT where PCIe core enters the L1. 0: enables P2 overwrite even if we are in D3Hot.
20	1b RW	**Enable the port to enter U3 automatically when in U1/U2 (ENABLE_AUTO_U3_ENTRY_FROM_U2_U3):** 1: enables the port to enter U3 automatically when in U1/U2 0: disables the port to enter U3 automatically when in U1/U2
19	1b RW	**No linkdown reset is issue during low power state (DIS_LINKDOWN_RST_DURING_LOW_POWER):** No linkdown reset is issue during low power state

Bit Range	Default & Access	Description
18	0b RW	**EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0 (EN_EXIT_DEEP_SLEEP_IF_PCIE_IN_P0):** This bit enables a feature in AUX PM module where if PCIe core LTSSM is in P0 for a duration of time, we will exit the deep sleep state. This is for failure control in case. 1: enables this feature 0: disable this feature
17	0b RW	**U2_EXIT_LFPS_TIMER_VALUE (U2_EXIT_LFPS_TIMER_VALUE):** This bit selects U2 exit LFPS timer value 0: 320ns 400ns in 25MHz domain 1: 240ns 320ns in 25MHz domain
16	1b RW	**EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP (EN_EXIT_DEEP_SLEEP_ON_USB_PORT_WAKEUP):** This bit enables a function that AUX PM module exits from the deep sleep state due to the USB ports wakeup level signal. We have added this feature where USB ports will generated a wakeup level signal to wakeup the AUX PM module if it is in deep sleep state and this level signal will be cleared if the change bits are updated by software. 1: enables this function 0: disables this function which means that a wakeup pulse generated from each USB PortSC event will wake up the AUX PM module from deep sleep if the D3 state is programmed.
15: 14	0h RW	**P3_ENTRY_TIMEOUT (P3_ENTRY_TIMEOUT):** This field defines the timeout value to enter P3 mode in U2. 00: 7us 8us 01: 511us 512us 10: disables the timer (0us) 11: disables the timer (0us)
13	0b RW	**Enable U2 P3 Mode (EN_U2_P3):** 0: Disable U2 P3 mode 1: Enable U2 P3 mode
12: 11	0h RW	**Fine Debug Mode Select (FINE_DM_SEL):** Reserved.
10	0b RW	**Enable Low Power State Based Core Clock Gating (EN_LP_CORE_CG):** When set to '1' enable core clock gating based on low power state entered
9	1b RW	**Disable USB3 Port Status Changed Event (DIS_U3_PORT_SCE):** 0: Enable USB3 port status change event generation if any change bit is not cleared 1: Disable USB3 port status change event generation if any change bit is not cleared Bit 12 default 0
8: 4	00h RW	**Debug Mode Select Register (DEB_MODE_SEL):** Reserved.
3	0b RW	**Enable Auto Wakeup Non-IDLE (EN_AWAK_NIDLE):** When set to 1 enables the auto wakeup function when engine has identified non IDLE condition.
2	1b RW	**Enable PM Control P1 Exit P2 (EN_PMC_P1_EXIT_P2):** When set 1 enables the PM control module to transition to P1 instead of P0 when exit P2.
1	1b RW	**Enable PCIe PIPE CLK Isolation (EN_PP_CLK_ISOL):** When set to 1 enables the PCIe PIPE CLK to be isolated when main power is removed.
0	0b RW	**Enable P2 Overwrite P1 Allowed Detect (EN_P2OVRP1_ADET):** When set to 1 enables a function that can detect whether or not enable P2 overwrite P1 function. The condition to get to P2 overwrite is when engine is in idle conditions. This means that there is no ISO EP pending.

14.7.176 USB2 PHY Power Management Control (USB2_PHY_PMC)—Offset 8164h

Access Method

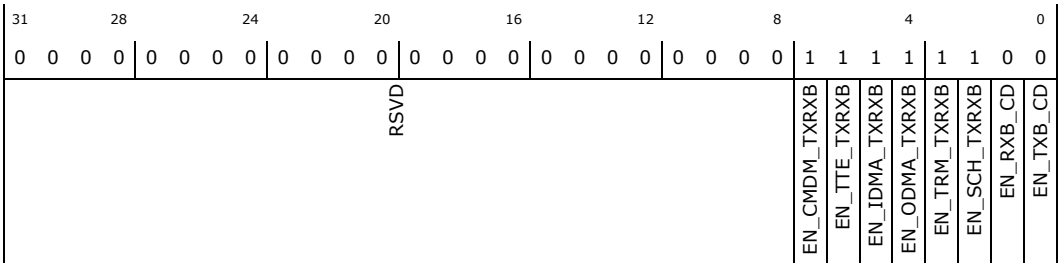
Type: Memory Mapped I/O Register (Size: 32 bits)

USB2_PHY_PMC: [MBAR] + 8164h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 000000FCh



Bit Range	Default & Access	Description
31: 8	000000h RO	**Reserved (RSVD):** Reserved.
7	1b RW	**EN_CMDM_TXRXB (EN_CMDM_TXRXB):** Enable Command Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
6	1b RW	**EN_TTE_TXRXB (EN_TTE_TXRXB):** Enable TTE Active indication for Tx/Rx Bias circuit HS Phy PM Policy
5	1b RW	**EN_IDMA_TXRXB (EN_IDMA_TXRXB):** Enable IDMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
4	1b RW	**EN_ODMA_TXRXB (EN_ODMA_TXRXB):** Enable ODMA Active indication for Tx/Rx Bias circuit HS Phy PM Policy
3	1b RW	**EN_TRM_TXRXB (EN_TRM_TXRXB):** Enable Transfer Manager Active indication for Tx/Rx Bias circuit HS Phy PM Policy
2	1b RW	**EN_SCH_TXRXB (EN_SCH_TXRXB):** Enable Scheduler Active indication for Tx/Rx Bias circuit HS Phy PM Policy
1	0b RW	**Enable Rx Bias ckt disable (EN_RXB_CD):** When set enables the Rx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)
0	0b RW	**Enable Tx Bias ckt disable (EN_TXB_CD):** When set enables the Tx bias ckt to be disabled when conditions met (as described by the HS phy PM policy bits)

14.7.177 USB Power Gating Control (USB_PGC)—Offset 8168h

Access Method

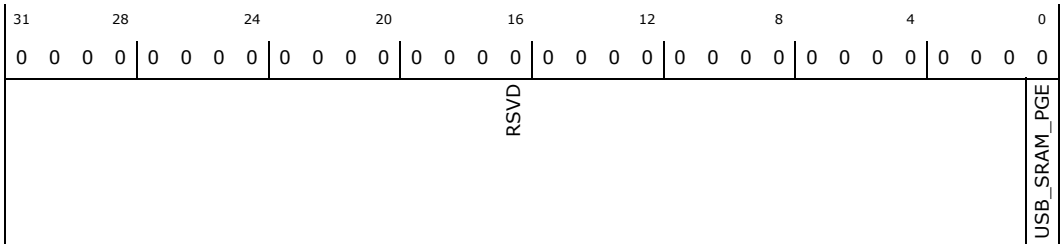
Type: Memory Mapped I/O Register (Size: 32 bits)

USB_PGC: [MBAR] + 8168h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 1	00000000h RO	**Reserved (RSVD):** Reserved.
0	0b RW	**USB SRAM power gating enable (USB_SRAM_PGE):** When set enables power gating on USB ports. Usage of this bit is further qualified with xHCI SRAM Dynamic Power Gating Disable fuse. If the fuse disables dynamic power gating, setting this bit to 1 shall not enable power gating feature. This bit always returns the value that was written to it irrespective of the setting of xHCI SRAM Dynamic Power Gating Disable fuse.

14.7.178 xHCI Aux Clock Control Register (XHCI_AUX_CCR)—Offset 816Ch

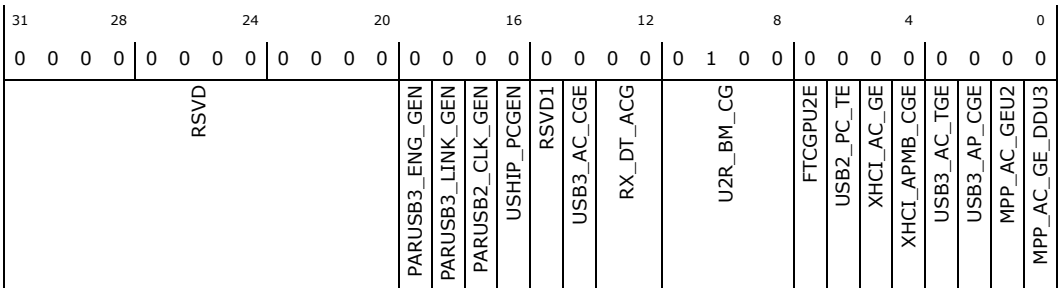
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

XHCI_AUX_CCR: [MBAR] + 816Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Default: 00000400h



Bit Range	Default & Access	Description
31: 20	000h RO	**Reserved (RSVD):** Reserved.
19	0b RW	**USB3 Partition Engine/Link trunk gating Enable (PARUSB3_ENG_GEN):** When set to 1 enables gating of the SOSC trunk to the XHCI engine and link in the PARUSB3 partition.
18	0b RW	**USB3 Partition Frame Timer trunk gating Enable (PARUSB3_LINK_GEN):** When set to 1 enables gating of the SOSC trunk to the Frame timer in the PARUSB3 partition.
17	0b RW	**USB2 link partition clock gating enable (PARUSB2_CLK_GEN):** When set to 1 enables gating of the SOSC trunk to the USB2 link and Phy logic in the PARUSB2 partition.
16	0b RW	**USB2/USHIP 12.5 MHz partition clock gating enable (USHIP_PCGEN):** When set to 1 enables gating of the 12.5 MHz SOSC trunk to the USB2 and USHIP logic in the PARUSB2 partition.
15	0b RO	**Reserved1 (RSVD1):** Reserved
14	0b RW	**USB3 Port Aux/Core clock gating enable (USB3_AC_CGE):** When set, allows the aux_cclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
13: 12	0h RW	**Rx Detect Timer when port Aux Clock is Gated (RX_DT_ACG):** This field defines the value of the timer used to perform Rx Detect when port Aux Clock has been gated. 0x0: 100ms 0x1: 12ms Others: Reserved Note: This timer shall use the Fast Training Timer Tick (about 1us tick) for simulation purposes. For Fast Training mode, the above timeouts will become about 11us and about 100us, +/- implementation uncertainty, respectively.
11: 8	4h RW	**U2 Residency Before ModPHY Clock Gating (U2R_BM_CG):** Before gating ModPHY Aux clock, Host Controller shall wait for this time in U2. This time is meant to ensure that the attached device has entered U2 as well. 0x0: 1us 0x1: 128us 0x2: 256us 0x3: 512us 0x4: 640us 0x5: 768us 0x6: 896us 0x7: 1024us Others: Reserved Note: This counter shall start counting once pipe has entered PS3 state in response to link in U2.

Bit Range	Default & Access	Description
7	0h RW	**Frame Timer Clock Gating Ports in U2 Enable (FTCGPU2E):** This bit, when set, allows Host Controller to gate the clock to the Frame Timer when ports are in U2.
6	0b RW	**USB2 port clock throttle enable (USB2_PC_TE):** When set, allows the Aux clock into the USB2 ports to be throttled when conditions allow.
5	0b RW	**XHCI Engine Aux clock gating enable (XHCI_AC_GE):** When set, allows the aux clock into the XHCI engine to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
4	0b RW	**XHCI Aux PM block clock gating enable (XHCI_APMB_CGE):** When set, allows the aux clock into the Aux PM block to be gated when idle. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
3	0b RW	**USB3 Aux Clock Trunk Gating Enable (USB3_AC_TGE):** When set, allows Aux Clock Trunk feeding to USB3.0 ports to be gated when port Aux clock is gated at all USB3.0 ports and all USB3.0 modPHY instances. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
2	0b RW	**USB3 Port Aux/Port clock gating enable (USB3_AP_CGE):** When set, allows the aux_pclk clock into the USB3 port to be gated when conditions are met. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
1	0b RW	**ModPHY port Aux clock gating enable in U2 (MPP_AC_GEU2):** When set, allows the aux clock into the ModPhy to be gated when Link is in U2 and pipe has been in PS3 for at least the time defined by U2 Residency Before ModPHY Clock Gating field. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.
0	0b RW	**ModPHY port Aux clock gating enable in Disconnected, U3 or Disabled (MPP_AC_GE_DDU3):** When set, allows the aux clock into the ModPHY to be gated when Link is in Disconnected, U3 or Disabled state. Usage of this bit is further qualified with xHC Dynamic Clock Gating Disable fuse. If the fuse disables dynamic clock gating, Aux clock gating will not be enabled either. This bit always returns the value that was written to it irrespective of the setting of xHC Dynamic Clock Gating Disable fuse.

14.7.179 USB LPM Parameters (USB_LPM_PARAM)—Offset 8170h

Access Method

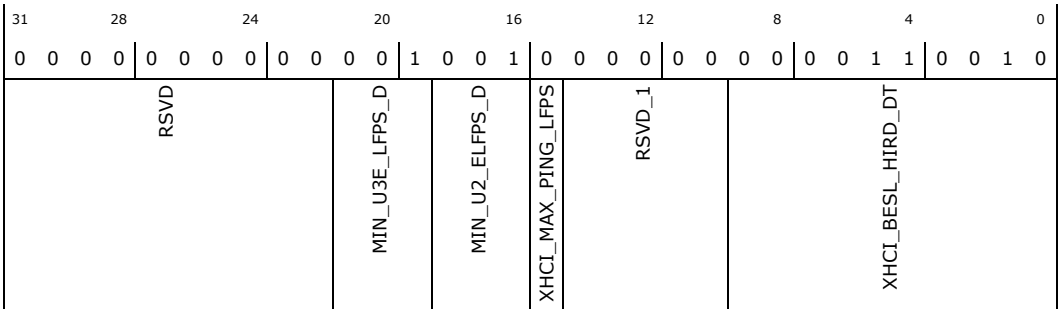
Type: Memory Mapped I/O Register (Size: 32 bits)

USB_LPM_PARAM: [MBAR] + 8170h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00090032h



Bit Range	Default & Access	Description
31: 22	000h RO	**Reserved (RSVD):** Reserved.
21: 19	001b RW	**Min U3 Exit LFPS Duration (MIN_U3E_LFPS_D):** Min U3 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U3 exit LFPS handshake. Note that theres an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000: 96us 0b001: 160us 0b010: 224us 0b011: 288us 0b100: 352us 0b101: 416us 0b110: 480us 0b111: 544us
18: 16	001b RW	**Min U2 Exit LFPS Duration (MIN_U2_ELFPS_D):** Min U2 Exit LFPS Duration This field defines the minimum duration of LFPS driven by Host Controller upon U2 exit LFPS handshake. Note that theres an uncertainty of +-16us in actual duration driven by the Host Controller. 0b000: 96us 0b001: 160us 0b010: 224us 0b011: 288us 0b100: 352us 0b101: 416us 0b110: 480us 0b111: 544us
15	0b RW	**Max PING LFPS Rx Detection (XHCI_MAX_PING_LFPS):** This field defines the maximum timing for PING LFPS. If an incoming LFPS will be considered a PING if it has a timing such that it is less than or equal to the selected value. Otherwise it will be considered for the other types of LFPS. 0b Max PING LFPS timing set to 256 ns (32 link clocks) 1b Max PING LFPS timing set to 320 ns (40 link clocks)
14: 10	00h RO	**Reserved (RSVD_1):** Reserved.
9: 0	032h RW	**xHCI BESL to HIRD Distance (XHCI_BESL_HIRD_DT):** This field defines the gap between BESL and duration of Resume signalling from Host upon Host Initiated Resume from USB2.0 LPM. Default value of this register corresponds to xHCI spec defined 50us value. Value BESL to HIRD Distance 000h 0us 001h 1us 002h 2us 3FFh 1023us

14.7.180 xHC Latency Tolerance Parameters - LTV Control (XLTP_LTV1)—Offset 8174h

Access Method

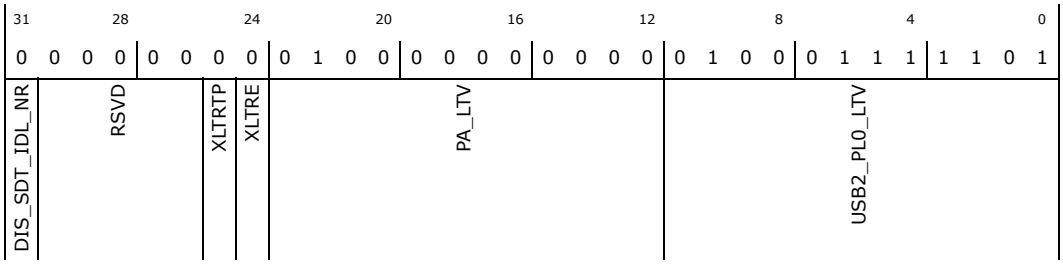
Type: Memory Mapped I/O Register (Size: 32 bits)

XLTP_LTV1: [MBAR] + 8174h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0040047Dh



Bit Range	Default & Access	Description
31	0b RW	**Disable scheduler direct transition from IDLE to NO requirement (DIS_SDT_IDL_NR):** 0: (default) allow scheduler direct transition from IDLE to NO requirement 1: Disable scheduler direct transition from IDLE to NO requirement
30: 26	00h RW	**Reserved (RSVD):** Reserved.
25	0b RW	**XHCI LTR Transition Policy (XLTRTP):** When '0', LTR messaging state machine transitions from High, Medium, or Low LTR states to Active state upon the Alarm Timer timout and stays in Active until the next service boundary. When '1', the LTR messaging state machine transitions through High ? Med ? Low ? Active states assuming enough latency is available for each transition.
24	0b RW	**XHCI LTR Enable (XLTRE):** This bit must be set to enable LTV messaging from XHCI to the PMC.
23: 12	400h RW	**Periodic Active LTV (PA_LTV):** 23:22 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 21:12 Latency Value (ns) Defaults to 0 micro seconds
11: 0	47Dh RW	**USB2 Port L0 LTV (USB2_PL0_LTV):** 11:10 Latency Scale 00b : Reserved 01b : Latency Value to be multiplied by 1024 10b : Latency Value to be multiplied by 32,768 11b : Latency Value to be multiplied by 1,048,576 9:0 Latency Value (ns) Defaults to 128 Micro Seconds

14.7.181 xHC Latency Tolerance Parameters LTV Control 2 (XLTP_LTV2)—Offset 8178h

Access Method

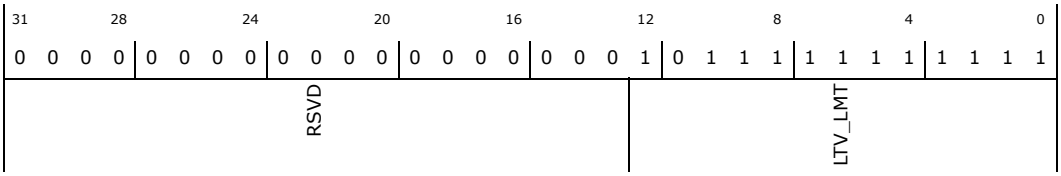
Type: Memory Mapped I/O Register (Size: 32 bits)

XLTP_LTV2: [MBAR] + 8178h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 000017FFh



Bit Range	Default & Access	Description
31: 13	00000h RO	**Reserved (RSVD):** Reserved.
12: 0	17FFh RW	**LTV Limit (LTV_LMT):** This register defines a maximum LTR value that is allowed to be advertised to the PMC. This is meant to be used as a workaround or mitigation if issues are discovered with the LTR values generated by the XHC using the defined algorithms. If the LTR value of the XHC is larger than the value in this register field, the value in this field is sent to the PMC instead. Default value is the highest possible - 101b 12:10: Latency Multiplier Field 000b - Value times 1 ns 001b - Value times 32 ns 010b - Value times 1,024 ns 011b - Value times 32,768 ns 100b - Value times 1,048,576 ns 101b - Value times 33,554,432 ns 110b-111b - Not Permitted 9:0: Latency Value Default = 3FFh

14.7.182 xHC Latency Tolerance Parameters - High Idle Time Control (XLTP_HITC)—Offset 817Ch

Access Method

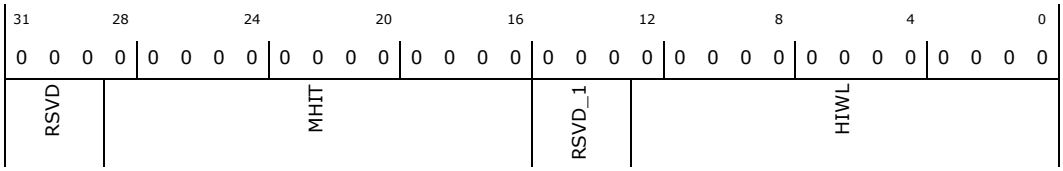
Type: Memory Mapped I/O Register (Size: 32 bits)

XLTP_HITC: [MBAR] + 817Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 29	0h RO	**Reserved (RSVD):** Reserved.
28: 16	0000h RW	**Minimum High Idle Time (MHIT):** LTR value can be indicated. This value must be larger than HIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15: 13	0h RO	**Reserved (RSVD_1):** Reserved.
12: 0	0000h RW	**High Idle Wake Latency (HIWL):** This is the latency to access memory from the High Idle Latency state. This value must be larger than MIWL and LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

14.7.183 xHC Latency Tolerance Parameters - Medium Idle Time Control (XLTP_MITC)—Offset 8180h

Access Method

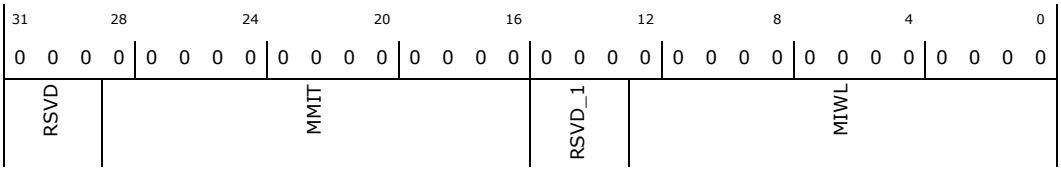
Type: Memory Mapped I/O Register (Size: 32 bits)

XLTP_MITC: [MBAR] + 8180h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 29	0h RO	**Reserved (RSVD):** Reserved.
28: 16	0000h RW	**Minimum Medium Idle Time (MMIT):** LTR value can be indicated. This value must be larger than MIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15: 13	0h RO	**Reserved (RSVD_1):** Reserved.
12: 0	0000h RW	**Medium Idle Wake Latency (MIWL):** This is the latency to access memory from the Medium Idle Latency state. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

14.7.184 xHC Latency Tolerance Parameters Low Idle Time Control (XLTP_LITC)—Offset 8184h

Access Method

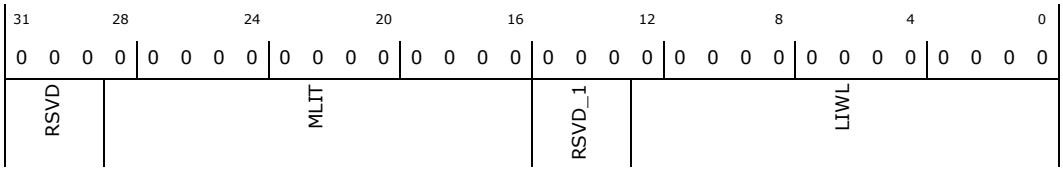
Type: Memory Mapped I/O Register (Size: 32 bits)

XLTP_LITC: [MBAR] + 8184h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 29	0h RO	**Reserved (RSVD):** Reserved.
28: 16	0000h RW	**Minimum Low Idle Time (MLIT):** LTR value can be indicated. This value must be larger than LIWL 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)
15: 13	0h RO	**Reserved (RSVD_1):** Reserved.
12: 0	0000h RW	**Low Idle Wake Latency (LIWL):** This is the latency to access memory from the Medium Idle Latency state. 12:7 - Time value in # of 125 Micro Seconds Bus Intervals (0 - 8ms) 6:0 - Fractional BI Time value in Micro Seconds (0 - 124 Micro Seconds)

14.7.185 USB EP Type Lock Policy (USB_EP_TLP)—Offset 8344h

Access Method

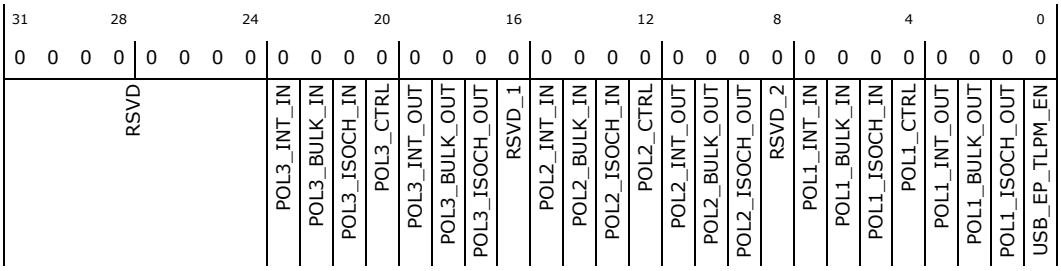
Type: Memory Mapped I/O Register (Size: 32 bits)

USB_EP_TLP: [MBAR] + 8344h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 24	00h RO	**Reserved (RSVD):** Reserved.
23	0b RW/L	**Policy 3 Interrupt IN EP Type (POL3_INT_IN):** 1 - EP Type = 7 is allowed by Policy 3 0 - EP Type = 7 is not allowed by Policy 3
22	0b RW/L	**Policy 3 Bulk IN EP Type (POL3_BULK_IN):** 1 - EP Type = 6 is allowed by Policy 3 0 - EP Type = 6 is not allowed by Policy 3
21	0b RW/L	**Policy 3 Isochronous IN EP Type (POL3_ISOCH_IN):** 1 - EP Type = 5 is allowed by Policy 3 0 - EP Type = 5 is not allowed by Policy 3
20	0b RW/L	**Policy 3 Control EP Type (POL3_CTRL):** 1 - EP Type = 4 is allowed by Policy 3 0 - EP Type = 4 is not allowed by Policy 3
19	0b RW/L	**Policy 3 Interrupt OUT EP Type (POL3_INT_OUT):** 1 - EP Type = 3 is allowed by Policy 3 0 - EP Type = 3 is not allowed by Policy 3
18	0b RW/L	**Policy 3 Bulk OUT EP Type (POL3_BULK_OUT):** 1 - EP Type = 2 is allowed by Policy 3 0 - EP Type = 2 is not allowed by Policy 3
17	0b RW/L	**Policy 3 Isochronous OUT EP Type (POL3_ISOCH_OUT):** 1 - EP Type = 1 is allowed by Policy 3 0 - EP Type = 1 is not allowed by Policy 3
16	0b RO	**Reserved (RSVD_1):** Reserved.
15	0b RW/L	**Policy 2 Interrupt IN EP Type (POL2_INT_IN):** 1 - EP Type = 7 is allowed by policy 2 0 - EP Type = 7 is not allowed by policy 2
14	0b RW/L	**Policy 2 Bulk IN EP Type (POL2_BULK_IN):** 1 - EP Type = 6 is allowed by policy 2 0 - EP Type = 6 is not allowed by policy 2
13	0b RW/L	**Policy 2 Isochronous IN EP Type (POL2_ISOCH_IN):** 1 - EP Type = 5 is allowed by policy 2 0 - EP Type = 5 is not allowed by policy 2
12	0b RW/L	**Policy 2 Control EP Type (POL2_CTRL):** 1 - EP Type = 4 is allowed by policy 2 0 - EP Type = 4 is not allowed by policy 2
11	0b RW/L	**Policy 2 Interrupt OUT EP Type (POL2_INT_OUT):** 1 - EP Type = 3 is allowed by policy 2 0 - EP Type = 3 is not allowed by policy 2

Bit Range	Default & Access	Description
10	0b RW/L	**Policy 2 Bulk OUT EP Type (POL2_BULK_OUT):** 1 - EP Type = 2 is allowed by policy 2 0 - EP Type = 2 is not allowed by policy 2
9	0b RW/L	**Policy 2 Isochronous OUT EP Type (POL2_ISOCH_OUT):** 1 - EP Type = 1 is allowed by policy 2 0 - EP Type = 1 is not allowed by policy 2
8	0b RO	**Reserved (RSVD_2):** Reserved.
7	0b RW/L	**Policy 1 Interrupt IN EP Type (POL1_INT_IN):** 1 - EP Type = 7 is allowed by policy 1 0 - EP Type = 7 is not allowed by policy 1
6	0b RW/L	**Policy 1 Bulk IN EP Type (POL1_BULK_IN):** 1 - EP Type = 6 is allowed by policy 1 0 - EP Type = 6 is not allowed by policy 1
5	0b RW/L	**Policy 1 Isochronous IN EP Type (POL1_ISOCH_IN):** 1 - EP Type = 5 is allowed by policy 1 0 - EP Type = 5 is not allowed by policy 1
4	0b RW/L	**Policy 1 Control EP Type (POL1_CTRL):** 1 - EP Type = 4 is allowed by policy 1 0 - EP Type = 4 is not allowed by policy 1
3	0b RW/L	**Policy 1 Interrupt OUT EP Type (POL1_INT_OUT):** 1 - EP Type = 3 is allowed by policy 1 0 - EP Type = 3 is not allowed by policy 1
2	0b RW/L	**Policy 1 Bulk OUT EP Type (POL1_BULK_OUT):** 1 - EP Type = 2 is allowed by policy 1 0 - EP Type = 2 is not allowed by policy 1
1	0b RW/L	**Policy 1 Isochronous OUT EP Type (POL1_ISOCH_OUT):** 1 - EP Type = 1 is allowed by policy 1 0 - EP Type = 1 is not allowed by policy 1
0	0b RW/L	**USB EP Type Lock Policy match enable (USB_EP_TLPM_EN):** Globally enable policy matching

14.7.186 USB EP Type Lock Policy - Port Control 1 (USB_EP_TLP1)—Offset 8348h

Access Method

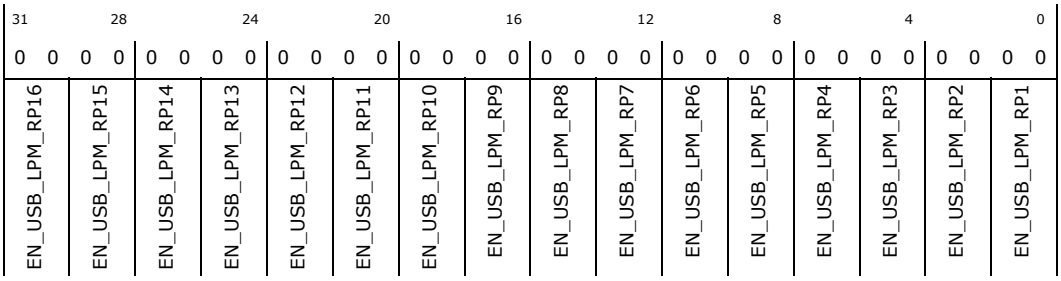
Type: Memory Mapped I/O Register (Size: 32 bits)

USB_EP_TLP1: [MBAR] + 8348h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 30	0h RW/L	**Enable USB Lock Policy match on root port number 16 (EN_USB_LPM_RP16):** 00 - policy is not enabled for root port number 16 01 - policy 1 is enabled for root port number 16 10 - policy 2 is enabled for root port number 16 11 - policy 3 is enabled for root port number 16
29: 28	0h RW/L	**Enable USB Lock Policy match on root port number 15 (EN_USB_LPM_RP15):** 00 - policy is not enabled for root port number 15 01 - policy 1 is enabled for root port number 15 10 - policy 2 is enabled for root port number 15 11 - policy 3 is enabled for root port number 15
27: 26	0h RW/L	**Enable USB Lock Policy match on root port number 14 (EN_USB_LPM_RP14):** 00 - policy is not enabled for root port number 14 01 - policy 1 is enabled for root port number 14 10 - policy 2 is enabled for root port number 14 11 - policy 3 is enabled for root port number 14
25: 24	0h RW/L	**Enable USB Lock Policy match on root port number 13 (EN_USB_LPM_RP13):** 00 - policy is not enabled for root port number 13 01 - policy 1 is enabled for root port number 13 10 - policy 2 is enabled for root port number 13 11 - policy 3 is enabled for root port number 13
23: 22	0h RW/L	**Enable USB Lock Policy match on root port number 12 (EN_USB_LPM_RP12):** 00 - policy is not enabled for root port number 12 01 - policy 1 is enabled for root port number 12 10 - policy 2 is enabled for root port number 12 11 - policy 3 is enabled for root port number 12
21: 20	0h RW/L	**Enable USB Lock Policy match on root port number 11 (EN_USB_LPM_RP11):** 00 - policy is not enabled for root port number 11 01 - policy 1 is enabled for root port number 11 10 - policy 2 is enabled for root port number 11 11 - policy 3 is enabled for root port number 11
19: 18	0h RW/L	**Enable USB Lock Policy match on root port number 10 (EN_USB_LPM_RP10):** 00 - policy is not enabled for root port number 10 01 - policy 1 is enabled for root port number 10 10 - policy 2 is enabled for root port number 10 11 - policy 3 is enabled for root port number 10
17: 16	0h RW/L	**Enable USB Lock Policy match on root port number 9 (EN_USB_LPM_RP9):** 00 - policy is not enabled for root port number 9 01 - policy 1 is enabled for root port number 9 10 - policy 2 is enabled for root port number 9 11 - policy 3 is enabled for root port number 9

Bit Range	Default & Access	Description
15: 14	0h RW/L	**Enable USB Lock Policy match on root port number 8 (EN_USB_LPM_RP8):** 00 - policy is not enabled for root port number 8 01 - policy 1 is enabled for root port number 8 10 - policy 2 is enabled for root port number 8 11 - policy 3 is enabled for root port number 8
13: 12	0h RW/L	**Enable USB Lock Policy match on root port number 7 (EN_USB_LPM_RP7):** 00 - policy is not enabled for root port number 7 01 - policy 1 is enabled for root port number 7 10 - policy 2 is enabled for root port number 7 11 - policy 3 is enabled for root port number 7
11: 10	0h RW/L	**Enable USB Lock Policy match on root port number 6 (EN_USB_LPM_RP6):** 00 - policy is not enabled for root port number 6 01 - policy 1 is enabled for root port number 6 10 - policy 2 is enabled for root port number 6 11 - policy 3 is enabled for root port number 6
9: 8	0h RW/L	**Enable USB Lock Policy match on root port number 5 (EN_USB_LPM_RP5):** 00 - policy is not enabled for root port number 5 01 - policy 1 is enabled for root port number 5 10 - policy 2 is enabled for root port number 5 11 - policy 3 is enabled for root port number 5
7: 6	0h RW/L	**Enable USB Lock Policy match on root port number 4 (EN_USB_LPM_RP4):** 00 - policy is not enabled for root port number 4 01 - policy 1 is enabled for root port number 4 10 - policy 2 is enabled for root port number 4 11 - policy 3 is enabled for root port number 4
5: 4	0h RW/L	**Enable USB Lock Policy match on root port number 3 (EN_USB_LPM_RP3):** 00 - policy is not enabled for root port number 3 01 - policy 1 is enabled for root port number 3 10 - policy 2 is enabled for root port number 3 11 - policy 3 is enabled for root port number 3
3: 2	0h RW/L	**Enable USB Lock Policy match on root port number 2 (EN_USB_LPM_RP2):** 00 - policy is not enabled for root port number 2 01 - policy 1 is enabled for root port number 2 10 - policy 2 is enabled for root port number 2 11 - policy 3 is enabled for root port number 2
1: 0	0h RW/L	**Enable USB Lock Policy match on root port number 1 (EN_USB_LPM_RP1):** 00 - policy is not enabled for root port number 1 01 - policy 1 is enabled for root port number 1 10 - policy 2 is enabled for root port number 1 11 - policy 3 is enabled for root port number 1

14.7.187 USB EP Type Lock Policy - Port Control 2 (USB_EP_TLP2)—Offset 834Ch

Access Method

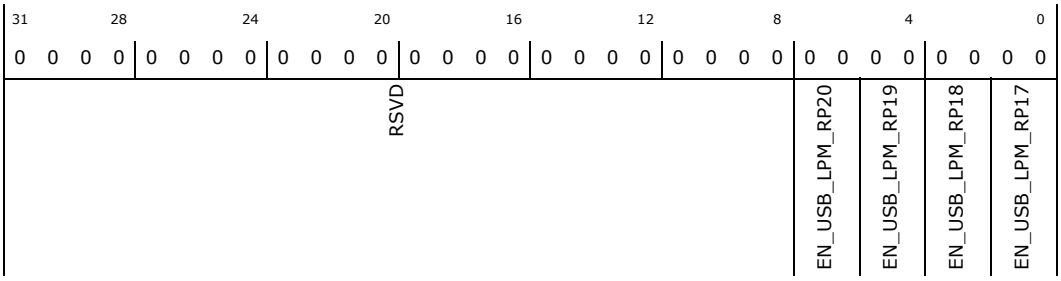
Type: Memory Mapped I/O Register (Size: 32 bits)

USB_EP_TLP2: [MBAR] + 834Ch

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 8	000000h RO	**Reserved (RSVD):** Reserved.
7: 6	0h RW/L	**Enable USB Lock Policy match on root port number 20 (EN_USB_LPM_RP20):** 00 - policy is not enabled for root port number 20 01 - policy 1 is enabled for root port number 20 10 - policy 2 is enabled for root port number 20 11 - policy 3 is enabled for root port number 20
5: 4	0h RW/L	**Enable USB Lock Policy match on root port number 19 (EN_USB_LPM_RP19):** 00 - policy is not enabled for root port number 19 01 - policy 1 is enabled for root port number 19 10 - policy 2 is enabled for root port number 19 11 - policy 3 is enabled for root port number 19
3: 2	0h RW/L	**Enable USB Lock Policy match on root port number 18 (EN_USB_LPM_RP18):** 00 - policy is not enabled for root port number 18 01 - policy 1 is enabled for root port number 18 10 - policy 2 is enabled for root port number 18 11 - policy 3 is enabled for root port number 18
1: 0	0h RW/L	**Enable USB Lock Policy match on root port number 17 (EN_USB_LPM_RP17):** 00 - policy is not enabled for root port number 17 01 - policy 1 is enabled for root port number 17 10 - policy 2 is enabled for root port number 17 11 - policy 3 is enabled for root port number 17

14.7.188 USB Legacy Support Capability (USBLEGSUP)—Offset 8460h

This register is modified and maintained by BIOS

Access Method

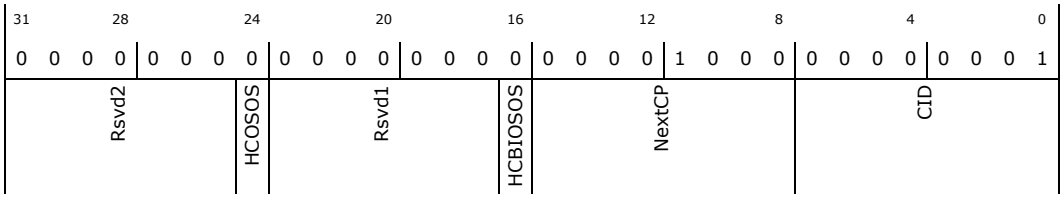
Type: Memory Mapped I/O Register (Size: 32 bits)

USBLEGSUP: [MBAR] + 8460h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000801h



Bit Range	Default & Access	Description
31: 25	00h RO	**Rsvd2 (Rsvd2):** Reserved.
24	0b RW	**HC OS Owned Semaphore (HCOSOS):** Reserved.
23: 17	00h RO	**Rsvd1 (Rsvd1):** Reserved.
16	0b RW	**HC BIOS Owned Semaphore (HCBIOSOS):** Reserved.
15: 8	08h RW/S	**Next Capability Pointer (NextCP):** Reserved.
7: 0	01h RW/L	**Capability ID (CID):** Reserved.

14.7.189 USB Legacy Support Control Status (USBLEGCTLSTS)—Offset 8464h

Access Method

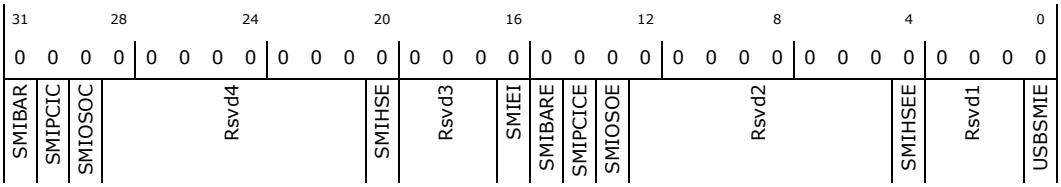
Type: Memory Mapped I/O Register (Size: 32 bits)

USBLEGCTLSTS: [MBAR] + 8464h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: SUS

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/C	**SMI on BAR (SMIBAR):** Reserved.
30	0b RW/C	**SMI on PCI Command (SMIPCIC):** Reserved.
29	0b RW/C	**SMI on OS Ownership Change (SMIOSOC):** Reserved.
28: 21	00h RO	**Rsvd4 (Rsvd4):** Reserved.
20	0b RO	**SMI on Host System Error (SMIHSE):** Reserved.
19: 17	0h RO	**Rsvd3 (Rsvd3):** Reserved.
16	0b RO	**SMI on Event Interrupt (SMIEI):** Reserved.
15	0b RW	**SMI on BAR Enable (SMIBARE):** Reserved.
14	0b RW	**SMI on PCI Command Enable (SMIPCICE):** Reserved.
13	0b RW	**SMI on OS Ownership Enable (SMIOSOE):** Reserved.
12: 5	00h RO	**Rsvd2 (Rsvd2):** Reserved.
4	0b RW	**SMI on Host System Error Enable (SMIHSEE):** Reserved.
3: 1	0h RO	**Rsvd1 (Rsvd1):** Reserved.
0	0b RW	**USB SMI Enable (USBSMIE):** Reserved.

14.7.190 Debug Capability ID Register (DCID)—Offset 8480h

This register is modified and maintained by BIOS

Access Method

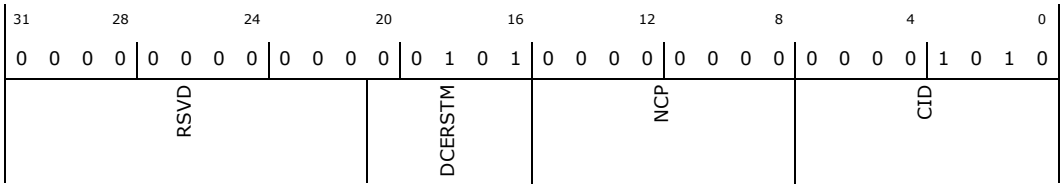
Type: Memory Mapped I/O Register (Size: 32 bits)

DCID: [MBAR] + 8480h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0005000Ah



Bit Range	Default & Access	Description
31: 21	000h RO	**Reserved (RSVD):** Reserved.
20: 16	05h RW	**Debug Capability Event Ring Segment Table Max (DCERSTM):** Note: This register is sticky.
15: 8	00h RW	**Next Capability Pointer (NCP):** Note: This register is sticky.
7: 0	0Ah RW	**Capability ID (CID):** Note: This register is sticky.

14.7.191 Debug Capability Doorbell Register (DCDB)—Offset 8484h

Access Method

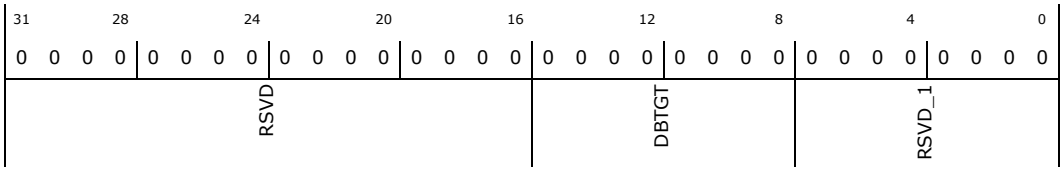
Type: Memory Mapped I/O Register (Size: 32 bits)

DCDB: [MBAR] + 8484h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	00h RW	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
15: 8	00h RW	**Doorbell Target (DBTGT):** This field defines the target of the doorbell reference. The table below defines the Debug Capability notification that is generated by ringing the doorbell. Value Definition 0 Data EP 1 OUT Enqueue Pointer Update 1 Data EP 1 IN Enqueue Pointer Update 2:255 Reserved This field returns '0' when read and the value should be treated as undefined by software.
7: 0	00h RW	**Reserved (RSVD_1):** Reserved.

14.7.192 Debug Capability Event Ring Segment Table Size Register (DCERSTSZ)—Offset 8488h

Access Method

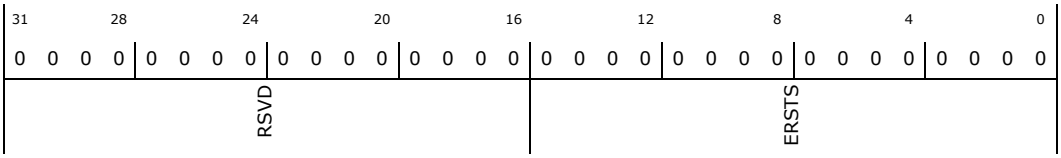
Type: Memory Mapped I/O Register (Size: 32 bits)

DCERSTSZ: [MBAR] + 8488h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Reserved (RSVD):** Reserved.
15: 0	0000h RW	**Event Ring Segment Table Size (ERSTS):** This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Debug Capability Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the DCERST Max field in the DCID register Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.

14.7.193 Debug Capability Event Ring Segment Table Base Address Register (DCERSTBA)—Offset 8490h

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

DCERSTBA: [MBAR] + 8490h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0000000000000000h

Bit Range	Default & Access	Description
63: 4	0000000000000000h RW	**Event Ring Segment Table Base Address Register (ERSTBAR):** This field defines the high order bits of the start address of the Debug Capability Event Ring Segment Table. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.
3: 0	0h RW	**Reserved (RSVD):** Reserved.

14.7.194 Debug Capability Event Ring Dequeue Pointer Register (DCERDP)—Offset 8498h

Access Method

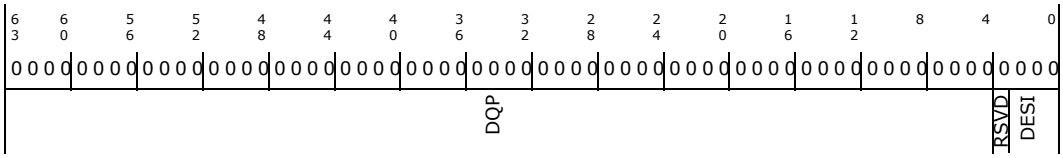
Type: Memory Mapped I/O Register (Size: 64 bits)

DCERDP: [MBAR] + 8498h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0000000000000000h



Bit Range	Default & Access	Description
63: 4	0000000000000000h RW	**Dequeue Pointer (DQP):** This field defines the high order bits of the 64-bit address of the current Debug Capability Event Ring Dequeue Pointer. Software shall initialize this register before setting the Debug Capability Enable field in the DCCTRL register to '1'.
3	0b RW	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
2: 0	0h RW	**Dequeue ERST Segment Index (DESI):** This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in.

14.7.195 Debug Capability Control Register (DCCTRL)—Offset 84A0h

Access Method

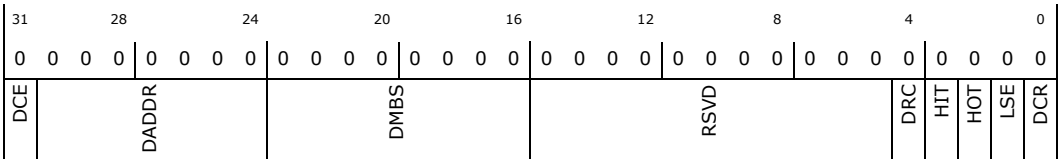
Type: Memory Mapped I/O Register (Size: 32 bits)

DCCTRL: [MBAR] + 84A0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**Debug Capability Enable (DCE):** Reserved.
30: 24	00h RO	**Device Address (DADDR):** Reserved.
23: 16	00h RO	**Debug Max Burst Size (DMBS):** LPT-LP USB Debug Device does not support bursting.
15: 5	000h RO	**Reserved (RSVD):** Reserved.
4	0b RW/C	**DbC Run Change (DRC):** Reserved.
3	0b RW/S	**Halt IN TR (HIT):** Reserved.
2	0b RW/S	**Halt OUT TR (HOT):** Reserved.
1	0b RW	**Link Status Event Enable (LSE):** Reserved.
0	0b RO	**DbC Run (DCR):** Reserved.

14.7.196 Debug Capability Status Register (DCST)—Offset 84A4h

Access Method

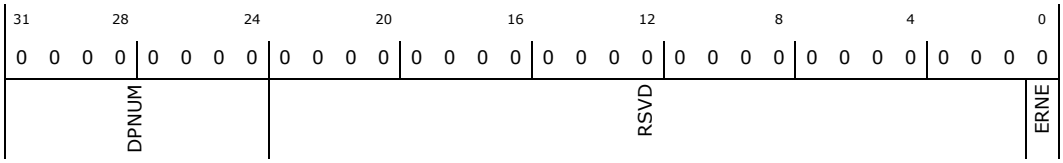
Type: Memory Mapped I/O Register (Size: 32 bits)

DCST: [MBAR] + 84A4h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 24	00h RO	**Debug Port Number (DPNUM):** This field provides the ID of the Root Hub port that the Debug Capability has been automatically attached to. The value is '0' when the Debug Capability is not attached to a Root Hub port.
23: 1	000000h RO	**Reserved (RSVD):** Reserved.
0	0b RO	**Event Ring Not Empty (ERNE):** When '1', this field indicates that the Debug Capability Event Ring has a Transfer Event on it. It is automatically cleared to '0' by the xHC when the Debug Capability Event Ring is empty, i.e. the Debug Capability Enqueue Pointer is equal to the Debug Capability Event Ring Dequeue Pointer register.

14.7.197 Debug Capability Port Status and Control Register (DCPORTSC)—Offset 84A8h

Access Method

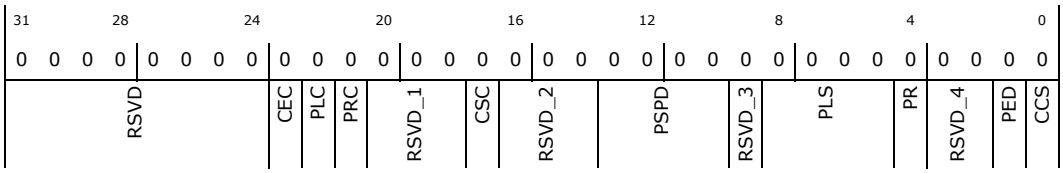
Type: Memory Mapped I/O Register (Size: 32 bits)

DCPORTSC: [MBAR] + 84A8h

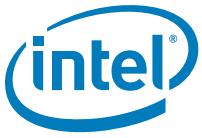
MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 24	00h RO	**Reserved (RSVD):** Reserved.
23	0b RW/C	**Port Config Error Change (CEC):** This flag indicates that the port failed to configure its link partner. 0 = No change. 1 = Port Config Error detected. Software shall clear this bit by writing a '1' to it.



Bit Range	Default & Access	Description
22	0b RW/C	**Port Link Status Change (PLC):** This flag is set to '1' due to the following PLS transitions: U0 -) U3 Suspend signaling detected from Debug Host U3 -) U0 Resume complete Polling -) Disabled Training Error Ux or Recovery -) Inactive Error Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'
21	0b RW/C	**Port Reset Change (PRC):** This bit is set when reset processing on this port is complete (i.e. a '1' to '0' transition of PR). '0' = No change. '1' = Reset complete.Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
20: 18	0h RO	**Reserved (RSVD_1):** Reserved.
17	0b RW/C	**Connect Status Change (CSC):** an already-set bit (i.e., the bit will remain '1'). Software shall clear this bit by writing a '1' to it. This field is '0' if DCE is '0'.
16: 14	0h RO	**Reserved (RSVD_2):** Reserved.
13: 10	0h RO	**Port Speed (PSPD):** This field identifies the speed of the port. This field is only relevant when a Debug Host is attached (CCS = '1') in all other cases this field shall indicate Undefined Speed. 0 Undefined Speed 1-15 Protocol Speed ID (PSI) Note: The Debug Capability onlydoes not supports LS, FS, or HS operation.
9	0b RO	**Reserved (RSVD_3):** Reserved.
8: 5	0h RO	**Port Link State (PLS):** This field reflects its current link state. This field is only relevant when a Debug Host is attached (Debug Port Number) '0'). Value Meaning 0 Link is in the U0 State 1 Link is in the U1 State 2 Link is in the U2 State 3 Link is in the U3 State (Device Suspended) 4 Link is in the Disabled State 5 Link is in the RxDetect State 6 Link is in the Inactive State 7 Link is in the Polling State 8 Link is in the Recovery State 9 Link is in the Hot Reset State 15:10 Reserved Note: Transitions between different states are not reflected until the transition is complete.
4	0b RO	**Port Reset (PR):** '1' = Port is in Reset. '0' = Port is not in Reset. This bit is set to '1' when the bus reset sequence as defined in the USB Specification is detected on the Root Hub port assigned to the Debug capability. It is cleared when the bus reset sequence is completed by the Debug Host, and the DbC shall transition to the USB Default state. A '0' to '1' transition of this bit shall clear DCPORTSC PED ('0'). This field is '0' if DCE or CCS are '0'.
3: 2	0h RO	**Reserved (RSVD_4):** Reserved.
1	0b RW	**Port Enabled/Disabled (PED):** Default = '0'. '1' = Enabled. '0' = Disabled. This flag shall be set to '1' by a '0' to '1' transition of CCS or a '1' to '0' transition of the PR. When PED transitions from '1' to '0' due to the assertion of PR, the port's link shall transition to the Rx.Detect state. This flag may be used by software to enable or disable the operation of the Root Hub port assigned to the Debug Capability. The Debug Capability Root Hub port operation may be disabled by a fault condition (disconnect event or other fault condition, e.g. a LTSSM Polling substate timeout, tPortConfiguration timeout error, etc.), the assertion of DCPORTSC PR, or by software. 0 = Debug Capability Root Hub port is disabled. 1 = Debug Capability Root Hub port is enabled. When the port is disabled (PED = '0') the port's link shall enter the SS.Disabled state and remain there until PED is reasserted ('1') or DCE is negated ('0'). Note that the Root Hub port is remains mapped to Debug Capability while PED = '0'. While PED = '0' the Debug Capability will appear to be disconnected to the Debug Host. Note, this bit is not affected by PORTSC PR bit transitions. This field is '0' if DCE or CCS are '0'.
0	0b RO	**Current Connect Status (CCS):** '1' = A Root Hub port is connected to a Debug Host and assigned to the Debug Capability. '0' = No Debug Host is present. This value reflects the current state of the port, and may not correspond to the value reported by the Connect Status Change (CSC) field in the Port Status Change Event that was generated by a '0' to '1' transition of this bit. This flag is '0' if Debug Capability Enable (DCE) is '0'.

14.7.198 Debug Capability Context Pointer Register (DCCP)—Offset 84B0h

Access Method

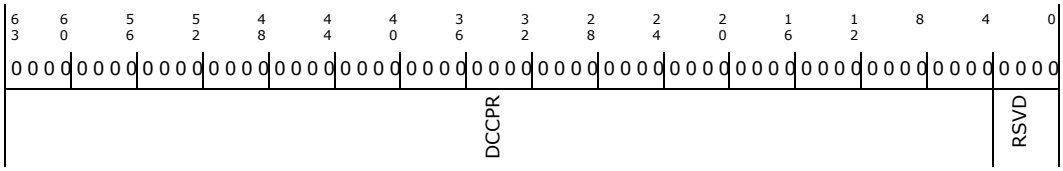
Type: Memory Mapped I/O Register (Size: 64 bits)

DCCP: [MBAR] + 84B0h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 0000000000000000h



Bit Range	Default & Access	Description
63: 4	0000000000000000h RW	**Debug Capability Context Pointer Register (DCCPR):** This field defines the high order bits of the start address of the Debug Capability Context data structure associated with the Debug Capability. Software shall initialize this register before setting the Debug Capability Enable bit in the Debug Capability Control Register to '1'.
3: 0	0h RO	**Reserved (RSVD):** Reserved.

14.7.199 Debug Capability Device Descriptor Info Register 1 (DCDDI1)—Offset 84B8h

Access Method

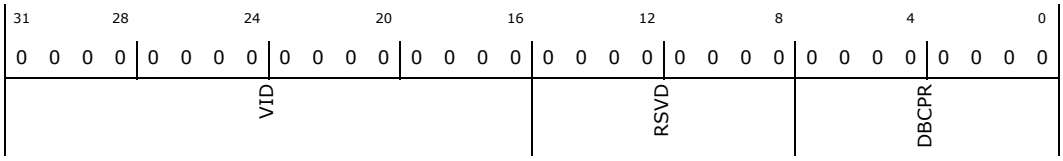
Type: Memory Mapped I/O Register (Size: 32 bits)

DCDDI1: [MBAR] + 84B8h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Vendor ID (VID):** This field is presented by the Debug Device in the USB Device Descriptor idVendor field.
15: 8	00h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
7: 0	00h RW	**DbC Protocol (DBCPR):** This field is presented by the Debug Device in the USB Interface Descriptor bInterfaceProtocol field. Value Function 0 Debug Target vendor defined. 1 GNU Remote Debug Command Set supported. 2-255 Reserved.

14.7.200 Debug Capability Device Descriptor Info Register 2 (DCDDI2)—Offset 84BCh

Access Method

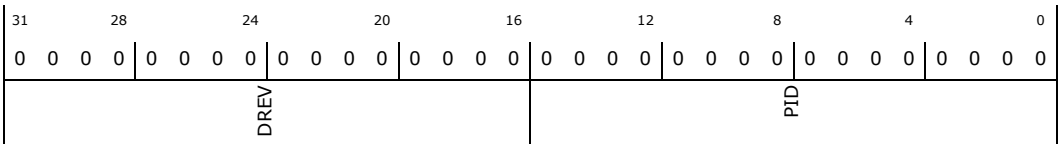
Type: Memory Mapped I/O Register (Size: 32 bits)

DCDDI2: [MBAR] + 84BCh

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 16	0000h RW	**Device Revision (DREV):** This field is presented by the Debug Device in the USB Device Descriptor bcdDevice field.
15: 0	0000h RW	**Product ID (PID):** This field is presented by the Debug Device in the USB Device Descriptor idProduct field.

14.7.201 Debug Capability Descriptor Parameters (DCDP)—Offset 8530h

Access Method

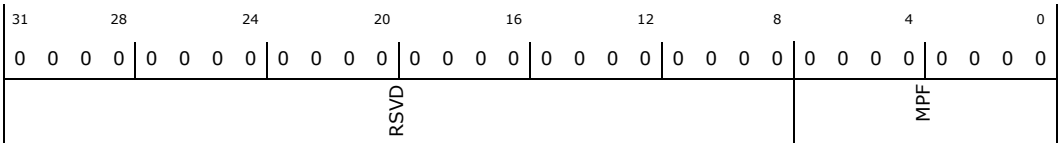
Type: Memory Mapped I/O Register (Size: 32 bits)

DCDP: [MBAR] + 8530h

MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 8	000000h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
7: 0	00h RW	**Max Power Field (MPF):** This field will be used by USB Debug Device to report maximum power consumption when the device is fully operational. This value is returned by bMaxPower field in response to Configuration Descriptor read from the debug device. Note: bU1DevExitLat and bU2DevExitLat fields returned in BOS Descriptor read will be taken from the corresponding fields from the Host Controller space.

14.7.202 Debug Device Control ODMA (DBGDEV_CTRL_ODMA_REG)—Offset 8538h

This register contains a number of fields that provide a specific level of configurability for the OUT DMA that is part of Debug Device logic. This configurability is above and beyond that defined in the xHCI specification.

Access Method

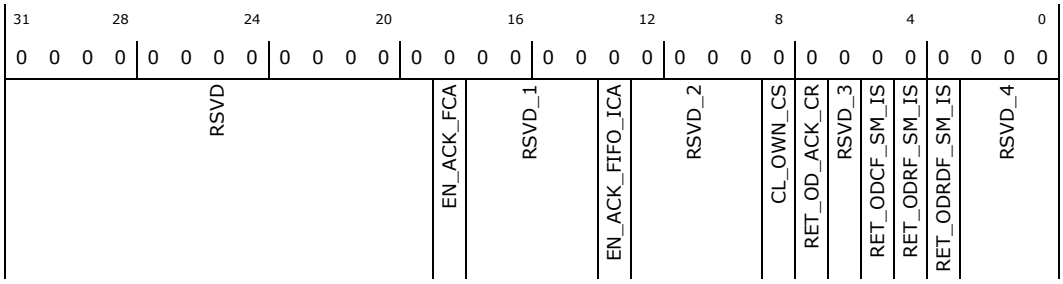
Type: Memory Mapped I/O Register (Size: 32 bits)

DBGDEV_CTRL_ODMA_REG: [MBAR] + 8538h

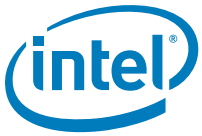
MBAR Type: PCI Configuration Register (Size: 32 bits)
MBAR Reference: [B:0, D:20, F:0] + 10h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31: 19	0000h RO	**Reserved (RSVD):** Reserved.
18	0b RW	**Enable ACK FIFO credit accounting (EN_ACK_FCA):** Setting this field will enable ACK FIFO credit accounting. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
17: 14	0h RO	**Reserved (RSVD_1):** Reserved.
13	0b RW	**Enable ACK FIFO ICA mechanisms (EN_ACK_FIFO_ICA):** Setting this field will enable ACK FIFO individual credit accounting mechanisms for Async vs. Periodic Endpoints. ODMA will ensure that ample room exists in the ACK FIFO for expected device responses prior to initiating a given DP
12: 9	0h RO	**Reserved (RSVD_2):** Reserved.
8	0b RW	**Clear ownership of context semaphore (CL_OWN_CS):** Setting this field generates a pulse that clears the ownership of the context semaphore that is shared between the Out DMA Response and Completion Finite State Machines

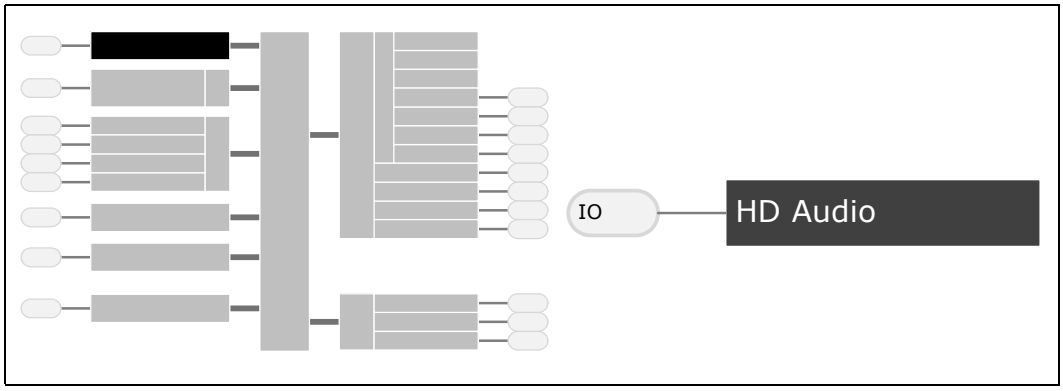


Bit Range	Default & Access	Description
7	0b RW	**Return OD ACK credits (RET_OD_ACK_CR):** Setting this field generates a pulse that implicitly returns all of the Out DMA ACK credits on all ports
6	0b RO	**Reserved (RSVD_3):** Reserved.
5	0b RW	**Return ODCF SM to idle state (RET_ODCF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Completion Finite State Machine into the IDLE state
4	0b RW	**Return ODRF SM to idle state (RET_ODRF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Response Finite State Machine into the IDLE state
3	0b RW	**Return ODRDF SM to idle state (RET_ODRDF_SM_IS):** Setting this field generates a pulse that returns the Out DMA Read Finite State Machine into the IDLE state
2: 0	0h RO	**Reserved (RSVD_4):** Reserved.

15 Intel® High Definition Audio (Intel® HD Audio)

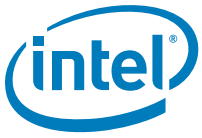
The Intel® High Definition Audio (Intel® HD Audio) is an architecture and infrastructure to support high-quality audio implementations for PCs.

Note: When High Definition Audio is active, the LPE Audio functionality is disabled.



The Intel® High Definition Audio (Intel® HD Audio) controller consists of a set of DMA engines that are used to move samples of digitally encoded data between system memory and internal/external CODECs. The controller communicates with the internal/external CODECs over the Intel® HD Audio serial link.The output DMA engines move digital data from system memory to a D-A converter in a CODEC. The processor implements a single Serial Data Output (SDO) signal that is connected to the external CODECs. The input DMA engines move digital data from the A-D converter in the CODEC to system memory. The platform supports up to two external CODECs by implementing two Serial Data Input (SDI) signals, each being dedicated to a single CODEC.

Audio software renders outbound, and processes inbound data to/from buffers in memory. The location of the individual buffers is described by a Buffer Descriptor List that is fetched and processed by the audio controller. The data in the buffers is arranged in a pre-defined format. The output DMA engines fetch the digital data from memory and reformat it based on the programmed sample rate, bits/sample and number of channels. The data from the output DMA engines is then combined and serially sent to the CODEC(s) over the Intel® HD Audio link. The input DMA engines receive data from the CODEC(s) over the Intel® HD Audio link and format the data based on the programmable attributes for that stream. The data is then written to memory in the predefined format for software to process. Each DMA engine moves one "stream" of data. A single CODEC can accept or generate multiple "streams" of data, one for each A-D or D-A converter in the CODEC. Multiple CODECs can accept the same output "stream" processed by a single DMA engine.



Codec commands and responses are also transported to and from the CODEC using DMA engines. The DMA engine dedicated to transporting commands from the Command Output Ring Buffer (CORB) in memory to the CODEC(s) is called the CORB engine. The DMA engine dedicated to transporting responses from the CODEC(s) to the Response Input Ring Buffer in memory is called the RIRB engine. Every command sent to a CODEC yields a response from that CODEC. Some commands are "broadcast" type commands in which case a response will be generated from each CODEC. A CODEC may also be programmed to generate unsolicited responses, which the RIRB engine also processes. The platform also supports Programmed IO-based Immediate Command/Response transport mechanism that can be used by BIOS prior to memory initialization.

15.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 121. Signals

Signal Name	Direction/ Type	Description
HDA_RST#	O	**Intel HD Audio Reset:** Master H/W reset to external Codecs
HDA_SYNC	O	**Intel HD Audio Sync:** 48 kHz fixed rate
HDA_CLK	O	**Intel HD Audio Bit Clock (Output):** 24 MHz serial data clock generated by the Intel HD Audio controller
HDA_SDO	O	**Intel HD Audio Data Out:** Serial TDM data output to the Codec(s). The serial output is double-pumped for a bit rate of 48 Mb/s
HDA_SDI[1:0]	I/O	**Intel HD Audio Serial Data In[1:0]:** Serial TDM data input from the CODEC(s). The serial input is single-pumped for a bit rate of 24 Mb/s.

The signals in the table above are all multiplexed and may be used by other functions.

15.2 Features

The Intel® HD Audio Controller supports the following features:

- Supports MSI and legacy interrupt delivery
- Support for ACPI D3 and D0 Device States
- Supports up to:
  - 6 streams (three input, three output)
  - 16 channels per stream
  - 32 bits/sample
  - 192 kHz sample rate
- 24 MHz HDA_CLK supports
  - SDO double pumped at 48 Mb/s
  - SDI single pumped at 24 Mb/s
- Supports 1.5V mode only
- Supports optional Immediate Command/Response mechanism

15.3 References

High Definition Audio Specification, Revision 1.0a

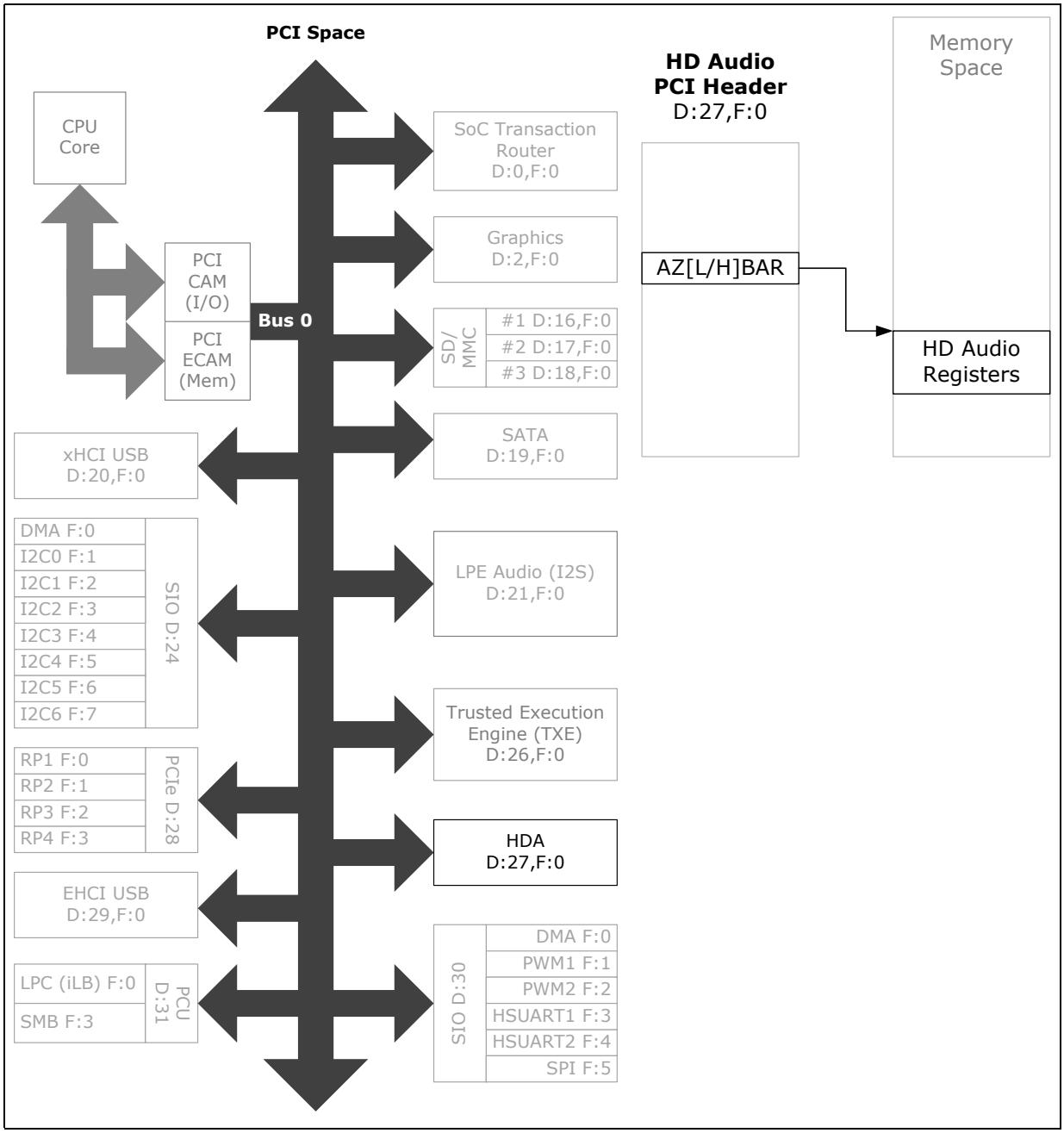
- http://www.intel.com/content/www/us/en/standards/high-definition-audio-specification.html

15.4 Register Map

See Chapters 3 and 4 for additional information.

Note: PCI mode is supported, but not PCIe mode. Must set TM1.HAPD bit to 1b for PCI mode.

Figure 20. Intel® HD Audio Register Map



15.5 HD Audio PCI Configuration Registers

Table 122. Summary of HD Audio PCI Configuration Registers—0/27/0

Offset	Size	Register ID—Description	Default Value
0h	2	"VID—Offset 0h" on page 543	8086h
2h	2	"DID—Offset 2h" on page 544	0F04h
4h	2	"CMD—Offset 4h" on page 544	0000h
6h	2	"STS—Offset 6h" on page 545	0010h
8h	1	"RID—Offset 8h" on page 546	00h
9h	1	"PI—Offset 9h" on page 546	00h
Ah	1	"SCC—Offset Ah" on page 547	03h
Bh	1	"BCC—Offset Bh" on page 547	04h
Ch	1	"CLS—Offset Ch" on page 548	00h
Dh	1	"LT—Offset Dh" on page 548	00h
Eh	1	"HTYPE—Offset Eh" on page 549	00h
Fh	1	"BIST—Offset Fh" on page 549	00h
10h	4	"AZLBAR—Offset 10h" on page 550	00000004h
14h	4	"AZUBAR—Offset 14h" on page 550	00000000h
2Ch	2	"SVID—Offset 2Ch" on page 551	0000h
2Eh	2	"SID—Offset 2Eh" on page 551	0000h
34h	1	"CAPPTR—Offset 34h" on page 552	50h
3Ch	1	"INTLN—Offset 3Ch" on page 552	00h
3Dh	1	"INTPN—Offset 3Dh" on page 553	01h
40h	1	"AZCTL—Offset 40h" on page 553	01h
42h	1	"IOBC—Offset 42h" on page 554	00h
43h	1	"TM1—Offset 43h" on page 554	57h
4Ch	1	"DCKCTL—Offset 4Ch" on page 555	00h
4Dh	1	"DCKSTS—Offset 4Dh" on page 556	80h
50h	2	"PID—Offset 50h" on page 556	6001h
52h	2	"PC—Offset 52h" on page 557	C842h
54h	4	"PCS—Offset 54h" on page 558	00000000h
60h	2	"MID—Offset 60h" on page 559	7005h
64h	4	"MMLA—Offset 64h" on page 559	00000000h
68h	4	"MMUA—Offset 68h" on page 560	00000000h
6Ch	2	"MMD—Offset 6Ch" on page 560	0000h
70h	2	"PXID—Offset 70h" on page 561	0010h
72h	2	"PXC—Offset 72h" on page 561	0091h
74h	4	"DEVCAP—Offset 74h" on page 562	10000000h
78h	2	"DEVCAP—Offset 74h" on page 562	0800h
7Ah	2	"DEVS—Offset 7Ah" on page 564	0010h

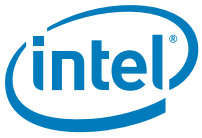


Table 122. Summary of HD Audio PCI Configuration Registers—0/27/0 (Continued)

Offset	Size	Register ID—Description	Default Value
F8h	4	"MANID—Offset F8h" on page 565	00000F00h
100h	4	"VCCAP—Offset 100h" on page 565	13010002h
104h	4	"PVCCAP1—Offset 104h" on page 566	00000001h
108h	4	"PVCCAP2—Offset 108h" on page 567	00000000h
10Ch	2	"PVCCTL—Offset 10Ch" on page 567	0000h
10Eh	2	"PVCSTS—Offset 10Eh" on page 568	0000h
110h	4	"VC0CAP—Offset 110h" on page 568	00000000h
114h	4	"VC0CTL—Offset 114h" on page 569	800000FFh
11Ah	2	"VC0STS—Offset 11Ah" on page 570	0000h
11Ch	4	"VCICAP—Offset 11Ch" on page 570	00000000h
120h	4	"VCICTL—Offset 120h" on page 571	00000000h
126h	2	"VCISTS—Offset 126h" on page 572	0000h
130h	4	"RCCAP—Offset 130h" on page 572	00010005h
134h	4	"ESD—Offset 134h" on page 573	0F000100h
140h	4	"L1DESC—Offset 140h" on page 573	00000001h
148h	4	"L1LADD—Offset 148h" on page 574	00000000h
14Ch	4	"L1UADD—Offset 14Ch" on page 574	00000000h

15.5.1 VID—Offset 0h

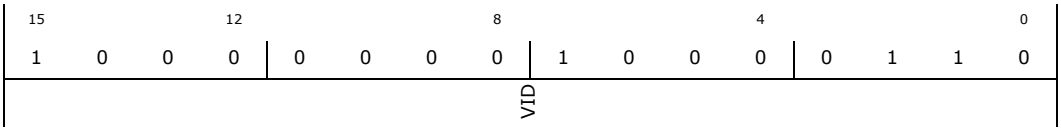
Vendor ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

VID: [B:0, D:27, F:0] + 0h

Default: 8086h



Bit Range	Default & Access	Description
15:0	8086h RO	**VID:** Vendor ID

15.5.2 DID—Offset 2h

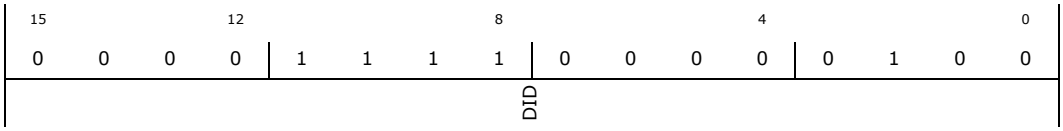
Device ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

DID: [B:0, D:27, F:0] + 2h

Default: 0F04h



Bit Range	Default & Access	Description
15:0	0f04h RO	**DID:** Device ID: This field identifies the particular device. DID[15:7] indicates processor, DID[6:1]=6'b000010 indicates HDAudio device, DID[0] comes from fuse indicates HDAudio SKU

15.5.3 CMD—Offset 4h

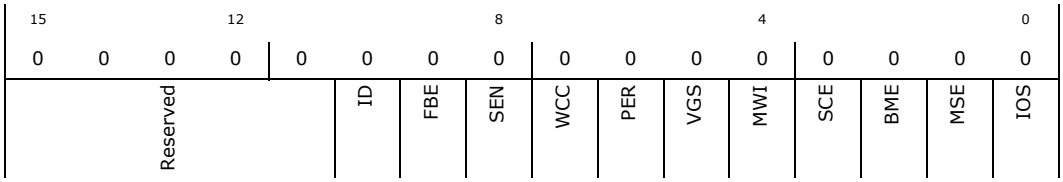
Command

Access Method

Type: PCI Configuration Register (Size: 16 bits)

CMD: [B:0, D:27, F:0] + 4h

Default: 0000h



Bit Range	Default & Access	Description
15:11	0000h RO	**Reserved:** Reserved
10	0h RW	**ID:** Interrupt Disable
9	0h RO	**FBE:** Fast back to back enable. Not implemented.
8	0h RW	**SEN:** SERR enable
7	0h RO	**WCC:** Wait Cycle Control. Not implemented.
6	0h RW	**PER:** Parity error response. Not implemented.
5	0h RO	**VGS:** VGA Pallete Snoop. Not implemented.

Bit Range	Default & Access	Description
4	0h RO	**MWI:** Memory write and invalidate enable. Not implemented.
3	0h RO	**SCE:** Special cycle enable. Not implemented.
2	0h RW	**BME:** Bus master enable
1	0h RW	**MSE:** Memory space enable
0	0h RO	**IOS:** I/O space enabled. Not implemented.

15.5.4 STS—Offset 6h

Status

Access Method

Type: PCI Configuration Register (Size: 16 bits)

STS: [B:0, D:27, F:0] + 6h

Default: 0010h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
DPE	SERRS	RMA	RTA	STA	DEVT		MDPE	FBC	Reserved	C66	CLIST	IS	Reserved_1		

Bit Range	Default & Access	Description
15	0h RO	**DPE:** Detected parity error. Not implemented.
14	0h RO	**SERRS:** SERR Status
13	0h WOC	**RMA:** Recieved master abort
12	0h RO	**RTA:** Recieved target abort. Not implemented.
11	0h RO	**STA:** Signaled target abort. Not implemented.
10:9	0h RO	**DEVT:** DEVSEL timing status. Not implemented.
8	0h RO	**MDPE:** Master data parity error. Not implemented.
7	0h RO	**FBC:** Fast back to back capable. Not implemented.
6	0h RO	**Reserved:** Reserved

Bit Range	Default & Access	Description
5	0h RO	**C66:** 66MHz capable. Not implemented.
4	1h RO	**CLIST:** Capabilities list exist
3	0h RO	**IS:** Interrupt Status. Shows legacy interrupt signal status. Doesn't apply to MSI.
2:0	0h RO	**Reserved_1:** reserved

15.5.5 RID—Offset 8h

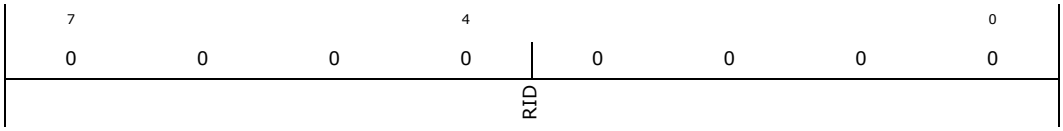
Revision ID

Access Method

Type: PCI Configuration Register (Size: 8 bits)

RID: [B:0, D:27, F:0] + 8h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**RID:** Revision ID

15.5.6 PI—Offset 9h

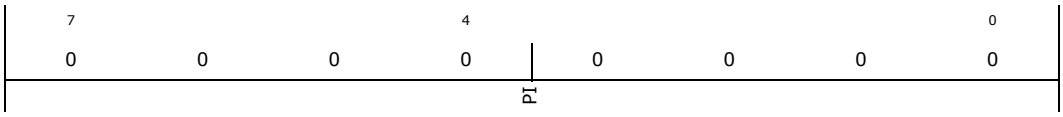
Programming Interface

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PI: [B:0, D:27, F:0] + 9h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**PI:** Programming Interface

15.5.7 SCC—Offset Ah

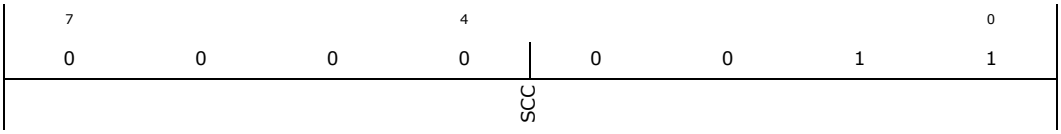
Sub Class Code

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SCC: [B:0, D:27, F:0] + Ah

Default: 03h



Bit Range	Default & Access	Description
7:0	03h RO	**SCC:** Sub Class Code

15.5.8 BCC—Offset Bh

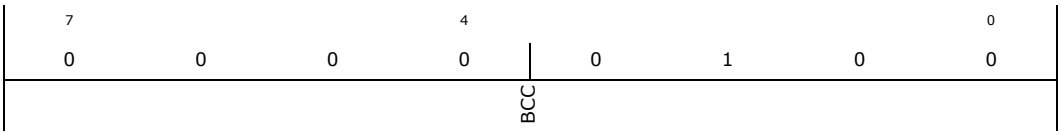
Base Class Code

Access Method

Type: PCI Configuration Register (Size: 8 bits)

BCC: [B:0, D:27, F:0] + Bh

Default: 04h



Bit Range	Default & Access	Description
7:0	04h RO	**BCC:** Base Class Code

15.5.9 CLS—Offset Ch

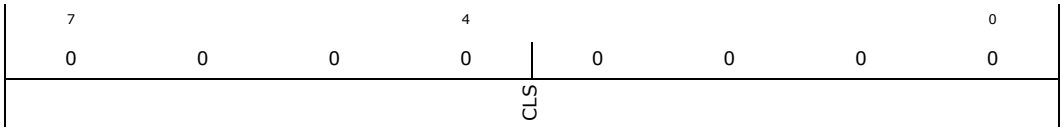
Cache line size

Access Method

Type: PCI Configuration Register (Size: 8 bits)

CLS: [B:0, D:27, F:0] + Ch

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RW	**CLS:** Cache line size

15.5.10 LT—Offset Dh

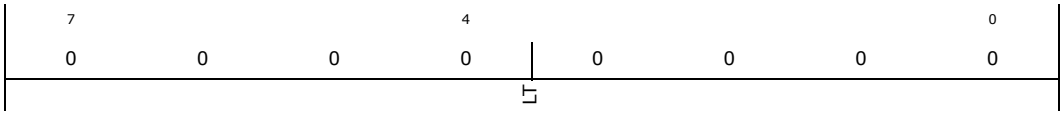
Latency timer

Access Method

Type: PCI Configuration Register (Size: 8 bits)

LT: [B:0, D:27, F:0] + Dh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**LT:** Latency timer

15.5.11 HTYPE—Offset Eh

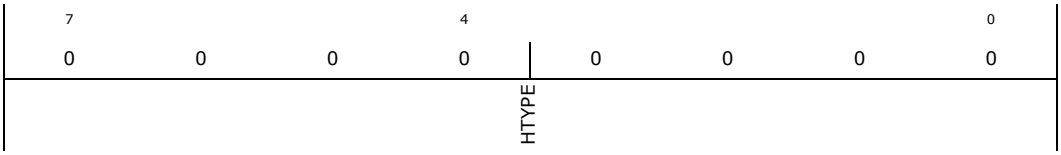
Header type

Access Method

Type: PCI Configuration Register (Size: 8 bits)

HTYPE: [B:0, D:27, F:0] + Eh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**HTYPE:** Header type

15.5.12 BIST—Offset Fh

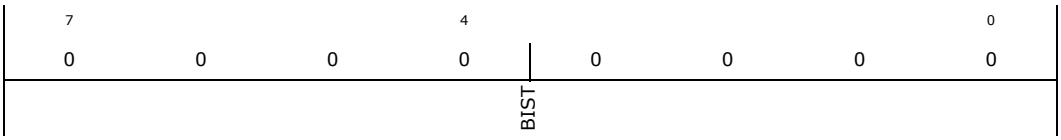
Built in self test. Not implemented.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

BIST: [B:0, D:27, F:0] + Fh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**BIST:** Built in self test. Not implemented.

15.5.13 AZLBAR—Offset 10h

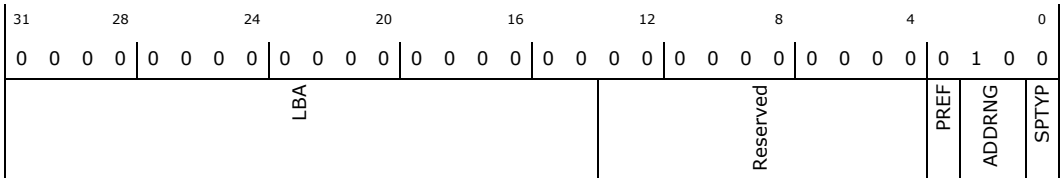
Lower Base Address (BAR)

Access Method

Type: PCI Configuration Register (Size: 32 bits)

AZLBAR: [B:0, D:27, F:0] + 10h

Default: 00000004h



Bit Range	Default & Access	Description
31:14	0h RW	**LBA:** Lower Base Address
13:4	0h RO	**Reserved:** Reserved
3	0h RO	**PREF:** Prefetchable
2:1	2h RO	**ADDRNG:** Address Range
0	0h RO	**SPTYP:** Space Type (Memory)

15.5.14 AZUBAR—Offset 14h

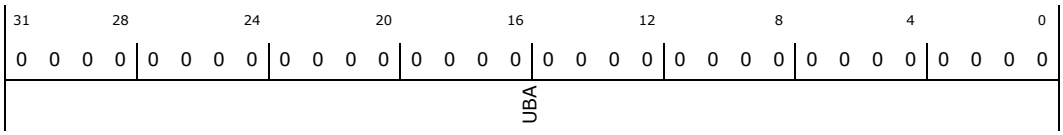
Upper Base Address (BAR)

Access Method

Type: PCI Configuration Register (Size: 32 bits)

AZUBAR: [B:0, D:27, F:0] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**UBA:** Upper Base Address

15.5.15 SVID—Offset 2Ch

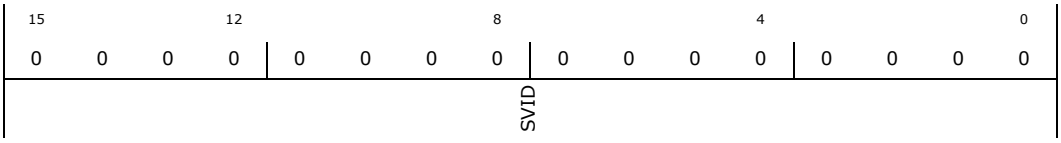
subsystem vendor ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SVID: [B:0, D:27, F:0] + 2Ch

Default: 0000h



Bit Range	Default & Access	Description
15:0	0h RWO	**SVID:** subsystem vendor ID. This field is written by BIOS. No hardware action is taken according to this register

15.5.16 SID—Offset 2Eh

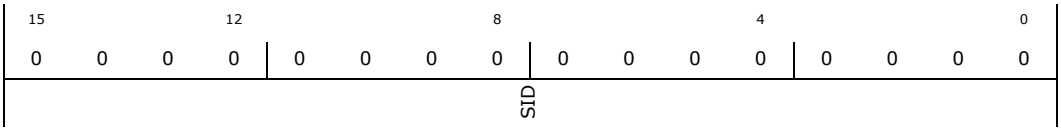
subsystem ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SID: [B:0, D:27, F:0] + 2Eh

Default: 0000h



Bit Range	Default & Access	Description
15:0	0h RWO	**SID:** subsystem ID. This field is written by BIOS. No hardware action is taken according to this register

15.5.17 CAPPTR—Offset 34h

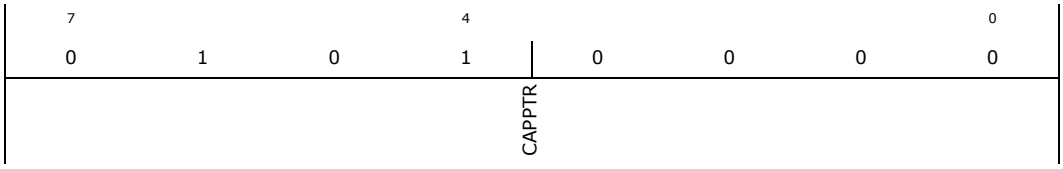
Capabilities pointer

Access Method

Type: PCI Configuration Register (Size: 8 bits)

CAPPTR: [B:0, D:27, F:0] + 34h

Default: 50h



Bit Range	Default & Access	Description
7:0	50h RO	**CAPPTR:** Capabilities pointer

15.5.18 INTLN—Offset 3Ch

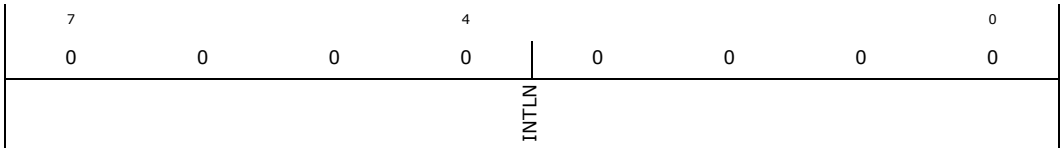
Interrupt Line

Access Method

Type: PCI Configuration Register (Size: 8 bits)

INTLN: [B:0, D:27, F:0] + 3Ch

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RW	**INTLN:** Interrupt Line

15.5.19 INTPN—Offset 3Dh

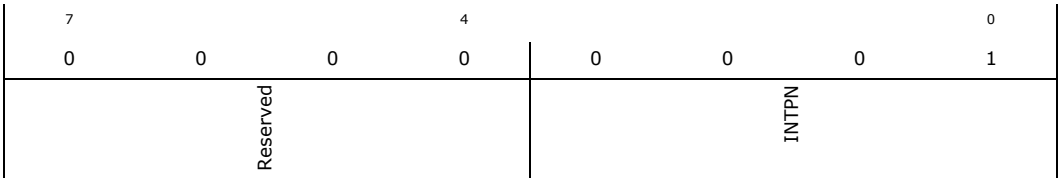
Interrupt Pin

Access Method

Type: PCI Configuration Register (Size: 8 bits)

INTPN: [B:0, D:27, F:0] + 3Dh

Default: 01h



Bit Range	Default & Access	Description
7:4	0h RO	**Reserved:** Reserved
3:0	1h RO	**IP (INTPN):** Interrupt Pin

15.5.20 AZCTL—Offset 40h

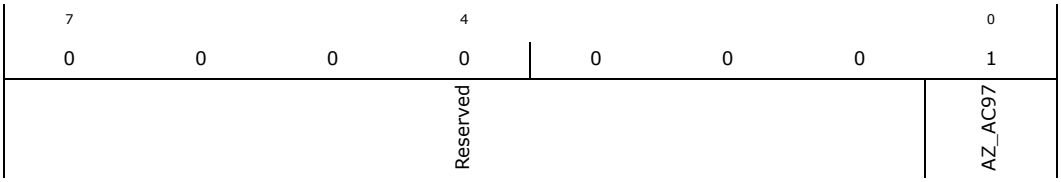
Azalia controller

Access Method

Type: PCI Configuration Register (Size: 8 bits)

AZCTL: [B:0, D:27, F:0] + 40h

Default: 01h



Bit Range	Default & Access	Description
7:1	0h RO	**Reserved:** Reserved
0	1h RO	**AZ_AC97# (AZ_AC97):** This register is always 1'b1 indicating Azalia

15.5.21 IOBC—Offset 42h

IO Buffer control

Access Method

Type: PCI Configuration Register (Size: 8 bits)

IOBC: [B:0, D:27, F:0] + 42h

Default: 00h

7				4			0
0	0	0	0	0	0	0	0
Reserved_0				ASRC	Reserved_1	AVDDIS	MVSEL	VMODE

Bit Range	Default & Access	Description
7:6	0h RO	**Reserved_0:** Reserved
5:4	0h RO	**ASRC:** Audio buffer slew rate control
3	0h RO	**Reserved_1:** Reserved
2	0h RO	**AVDDIS:** Automatic voltage detector disable
1	0h RO	**MVSEL:** Manual voltage select
0	0h RO	**VMODE:** voltage mode

15.5.22 TM1—Offset 43h

Test mode 1

Access Method

Type: PCI Configuration Register (Size: 8 bits)

TM1: [B:0, D:27, F:0] + 43h

Default: 57h

7				4			0
0	1	0	1	0	1	1	1
RSVD	RSVD	RSVD	RSVD	HAPD	RSVD	RSVD	RSVD

Bit Range	Default & Access	Description
7	0h RO	**Reserved (RSVD):** Reserved.
6	1h RO	**Reserved (RSVD):** Reserved.

Bit Range	Default & Access	Description
5	0h RO	**Reserved (RSVD):** Reserved.
4	1h RO	**Reserved (RSVD):** Reserved.
3	0h RWO	**HAPD:** HD Audio PCI/PCIe# device
2	1h RO	**Reserved (RSVD):** Reserved.
1	1h RO	**Reserved (RSVD):** Reserved.
0	1h RO	**Reserved (RSVD):** Reserved.

15.5.23 DCKCTL—Offset 4Ch

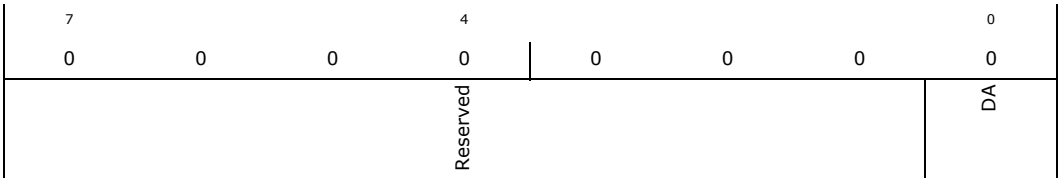
Docking control

Access Method

Type: PCI Configuration Register (Size: 8 bits)

DCKCTL: [B:0, D:27, F:0] + 4Ch

Default: 00h



Bit Range	Default & Access	Description
7:1	0h RO	**Reserved:** reserved
0	0h RW	**DA:** Dock attach

15.5.24 DCKSTS—Offset 4Dh

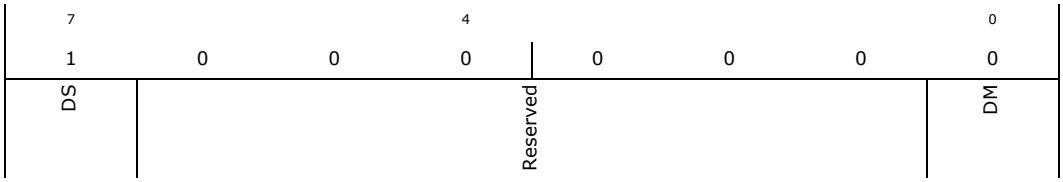
Docking status

Access Method

Type: PCI Configuration Register (Size: 8 bits)

DCKSTS: [B:0, D:27, F:0] + 4Dh

Default: 80h



Bit Range	Default & Access	Description
7	1h RWO	**DS:** Docking support
6:1	0h RO	**Reserved:** reserved
0	0h RO	**DM:** Dock Mated

15.5.25 PID—Offset 50h

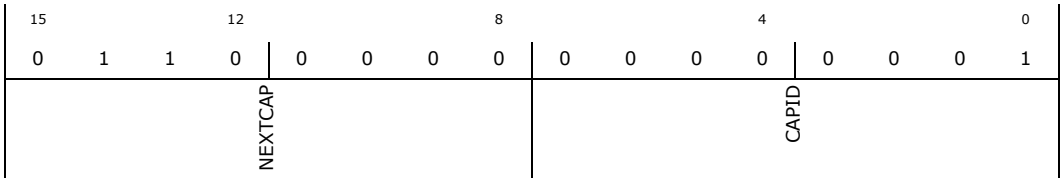
Power Management Capability ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PID: [B:0, D:27, F:0] + 50h

Default: 6001h



Bit Range	Default & Access	Description
15:8	60h RO	**NEXTCAP:** Next Capability.
7:0	01h RO	**CAPID:** Capability ID.

15.5.26 PC—Offset 52h

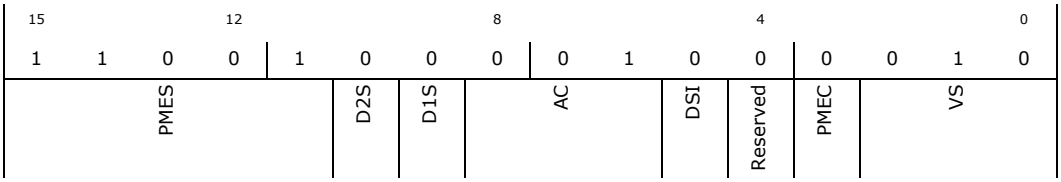
Power Management Capabilities

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PC: [B:0, D:27, F:0] + 52h

Default: C842h



Bit Range	Default & Access	Description
15:11	19h RO	**PMES:** PME_Support (PMES): Indicates PME# can be generated from D3 and D0 states.
10	0h RO	**D2S:** D2 state. Not supported.
9	0h RO	**D1S:** D1 state. Not supported.
8:6	1h RO	**AC:** Aux Current
5	0h RO	**DSI:** Device specific initialization
4	0h RO	**Reserved:** Reserved
3	0h RO	**PMEC:** PME Clock. Does not apply.
2:0	2h RO	**VS:** Version (VS): Indicates support for Revision 1.1 of the PCI Power Management Specification.

15.5.27 PCS—Offset 54h

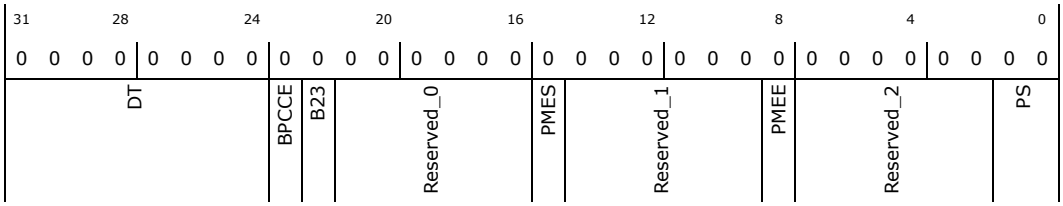
Power Management control and status

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCS: [B:0, D:27, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**DT:** Data. Does not apply.
23	0h RO	**BPCCE:** Bus power control enable. Does not apply.
22	0h RO	**B23:** Does not apply.
21:16	0h RO	**Reserved_0:** Reserved
15	0h RW1C	**PMES:** PME Status (PMES): This bit is set when the Intel HD Audio controller would normally assert the PME# signal independent of the state of the PME_En bit. This bit resides in the Suspend well. This bit is in the Suspend well and cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	0h RO	**Reserved_1:** Reserved
8	0h RW	**PMEE:** PME enable
7:2	0h RO	**Reserved_2:** reserved
1:0	0h RW	**PS:** Power State (PS): This field is used both to determine the current power state of the Intel HD Audio controller and to set a new power state. The values are: 00 D0 state 11 D3HOT state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3HOT states, the Intel HD Audio controllers configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3HOT state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.

15.5.28 MID—Offset 60h

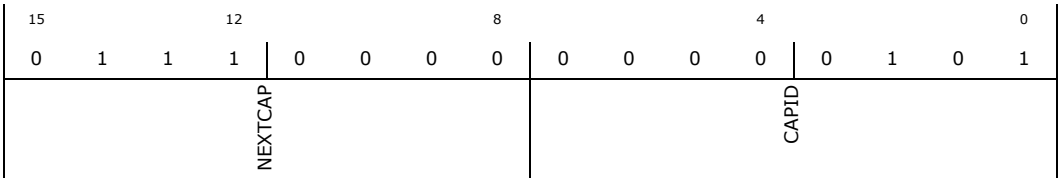
MSI Capability ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MID: [B:0, D:27, F:0] + 60h

Default: 7005h



Bit Range	Default & Access	Description
15:8	70h RO	**NEXTCAP:** Next Capability. The value of this field depends on the TM1.HAPD bit. When TM1.HAPD is 0, this field has a value of 70h where it points to the PCI Express capability structure. When TM1.HAPD bit is 1, this field has a value of 00h to indicate that this is the last capability structure in the list.
7:0	05h RO	**CAPID:** Capability ID.

15.5.29 MMLA—Offset 64h

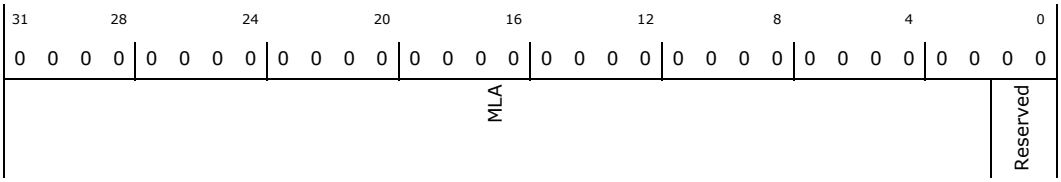
MSI Lower Address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MMLA: [B:0, D:27, F:0] + 64h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0h RW	**MLA:** MSI Lower Address
1:0	0h RO	**Reserved:** Reserved

15.5.30 MMUA—Offset 68h

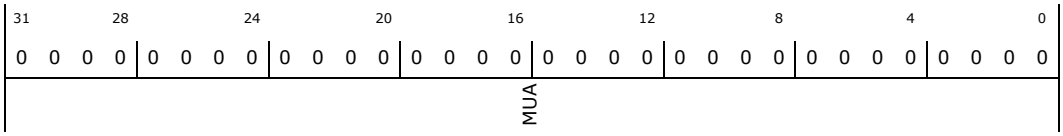
MSI Upper Address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MMUA: [B:0, D:27, F:0] + 68h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**MUA:** MSI Upper Address

15.5.31 MMD—Offset 6Ch

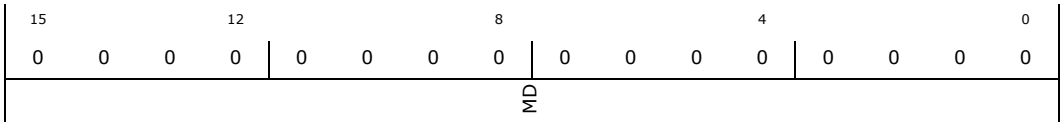
MSI Data

Access Method

Type: PCI Configuration Register (Size: 16 bits)

MMD: [B:0, D:27, F:0] + 6Ch

Default: 0000h



Bit Range	Default & Access	Description
15:0	0h RW	**MD:** MSI Data

15.5.32 PXID—Offset 70h

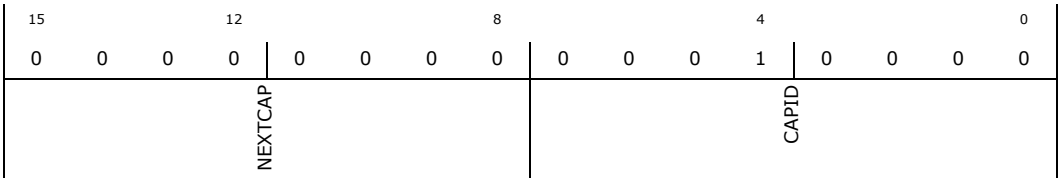
PCIe Capability ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PXID: [B:0, D:27, F:0] + 70h

Default: 0010h



Bit Range	Default & Access	Description
15:8	00h RO	**NEXTCAP:** Next Capability.
7:0	10h RO	**CAPID:** Capability ID.

15.5.33 PXC—Offset 72h

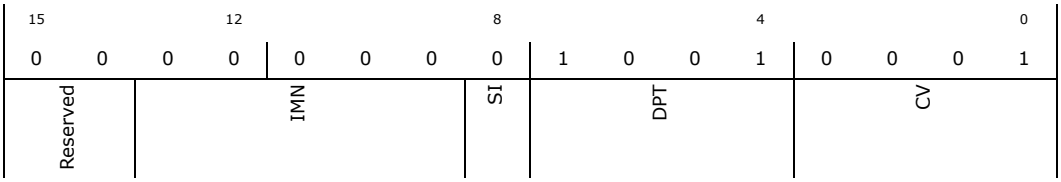
PCI express capabilities

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PXC: [B:0, D:27, F:0] + 72h

Default: 0091h



Bit Range	Default & Access	Description
15:14	0h RO	**Reserved:** reserved
13:9	0h RO	**IMN:** Interrupt message number
8	0h RO	**SI:** Slot implemented
7:4	9h RO	**DPT:** Device/port type
3:0	1h RO	**CV:** Capability version

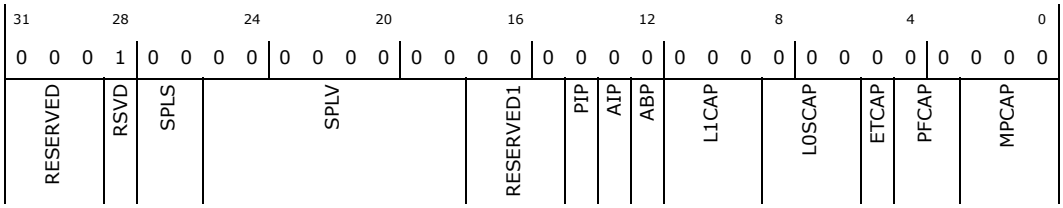
15.5.34 DEVCAP—Offset 74h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

DEVCAP: [B:0, D:27, F:0] + 74h

Default: 10000000h



Bit Range	Default & Access	Description
31:29	0h RO	**RESERVED:** reserved
28	1h RO	**Reserved (RSVD):** Reserved.
27:26	0h RO	**SPLS:** Captured Slot Power Limit Scale
25:18	0h RO	**SPLV:** Captured Slot Power Limit Value
17:15	0h RO	**RESERVED1:** reserved
14	0h RO	**PIP:** Power Indicator Present
13	0h RO	**AIP:** Attention Indicator Present
12	0h RO	**ABP:** Attention Button Present
11:9	0h RWO	**L1CAP:** Endpoint L1 Acceptable Latency
8:6	0h RWO	**L0SCAP:** Endpoint L0s Acceptable Latency
5	0h RO	**ETCAP:** Extended Tag Field Support
4:3	0h RO	**PFCAP:** Phantom Functions Supported
2:0	0h RO	**MPCAP:** Max Payload Size Supported

15.5.35 DEVC—Offset 78h

Device control

Access Method

Type: PCI Configuration Register (Size: 16 bits)

DEVC: [B:0, D:27, F:0] + 78h

Default: 0800h

15			12				8				4				0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
RSVD	MRRS			NSNPEN	AUXPEN	PEEN	ETEN	MAXPAY			ROEN	URREN	FEREN	NFEREN	CEREN

Bit Range	Default & Access	Description
15	0h RO	**Reserved (RSVD):** Reserved.
14:12	0h RO	**MRRS:** Max read request size
11	1h RW	**NSNPEN:** Enable No Snoop
10	0h RO	**AUXPEN:** Auxiliary Power PM Enable
9	0h RO	**PEEN:** Phantom Functions Enable
8	0h RO	**ETEN:** Extended Tag Field Enable
7:5	0h RO	**MAXPAY:** Max Payload Size
4	0h RO	**ROEN:** Enable Relaxed Ordering
3	0h RW	**URREN:** Unsupported Request Reporting Enable
2	0h RW	**FEREN:** Fatal Error Reporting Enable
1	0h RW	**NFEREN:** Non-Fatal Error Reporting Enable
0	0h RW	**CEREN:** Correctable Error Reporting Enable

15.5.36 DEVS—Offset 7Ah

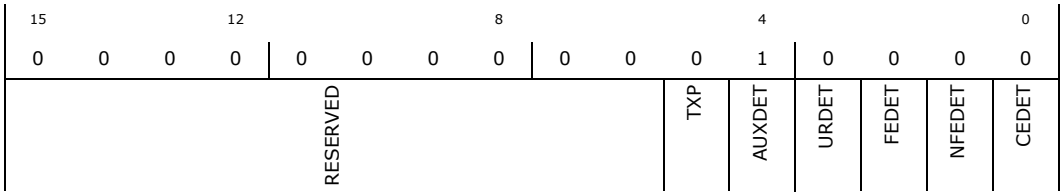
Device status

Access Method

Type: PCI Configuration Register (Size: 16 bits)

DEVS: [B:0, D:27, F:0] + 7Ah

Default: 0010h



Bit Range	Default & Access	Description
15:6	0h RO	**RESERVED:** RESERVED
5	0h RO	**TXP:** Transactions Pending
4	1h RO	**AUXDET:** AUX Power Detected
3	0h RO	**URDET:** Unsupported Request Detected
2	0h RO	**FEDET:** Fatal Error Detected
1	0h RO	**NFEDET:** Non-Fatal Error Detected
0	0h RO	**CEDET:** Correctable Error Detected

15.5.37 MANID—Offset F8h

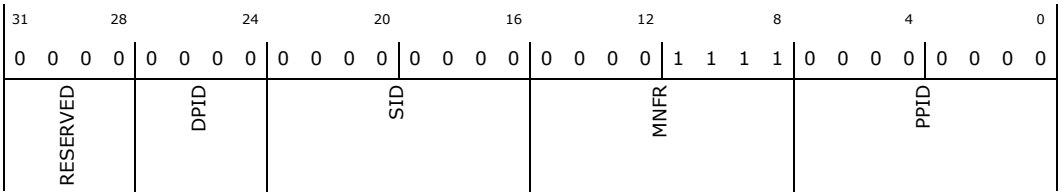
Manufacturer ID

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:27, F:0] + F8h

Default: 00000F00h



Bit Range	Default & Access	Description
31:28	0h RO	**RESERVED:** RESERVED
27:24	0h RO	**DPID:** Dot Portion Process ID
23:16	0h RO	**SID:** Stepping ID
15:8	0Fh RO	**MNFR:** Manufacturer
7:0	0h RO	**PPID:** Process Portion Process ID

15.5.38 VCCAP—Offset 100h

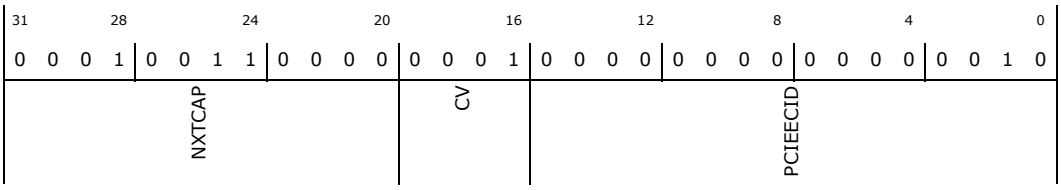
Virtual Channel Cap Header

Access Method

Type: PCI Configuration Register (Size: 32 bits)

VCCAP: [B:0, D:27, F:0] + 100h

Default: 13010002h



Bit Range	Default & Access	Description
31:20	130h RWO	**NXTCAP:** Next Capability Offset (NXTCAP): Points to the next capability header, which is the Root Complex Link Declaration Enhanced Capability Header. This register is RWO to support removing the Root Complex Topology Capability from the PCI Express Extended Capability List. For systems which support the Root Complex Topology Capability Structure, boot BIOS should write a 130h to this register, otherwise boot BIOS should write a 000h to this register.

Bit Range	Default & Access	Description
19:16	1h RWO	**CV:** Capability Version (CV): This register is RWO to support removing the PCI Express Extended Capabilities from Azalia. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 1h to this register, otherwise boot BIOS should write a 0h to this register.
15:0	2h RWO	**PCIEECID:** PCI Express Extended Capability ID (PCIEECID): This register is RWO to support removing the PCI Express Extended Capabilities from Azalia. For systems which support the PCI Express Virtual Channel capability and the Root Complex Topology Capability Structure, boot BIOS should write a 0002h to this register, otherwise boot BIOS should write a 0000h to this register.

15.5.39 PVCCAP1—Offset 104h

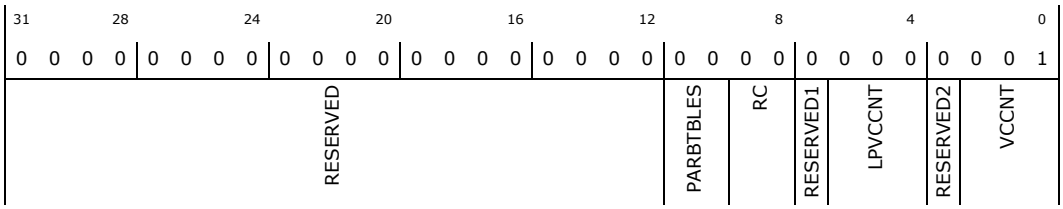
Port VC Capability

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PVCCAP1: [B:0, D:27, F:0] + 104h

Default: 00000001h



Bit Range	Default & Access	Description
31:12	0h RO	**RESERVED:** RESERVED
11:10	0h RO	**PARBTBLES:** Port Arbitration Table Entry Size
9:8	0h RO	**RC:** Reference Clock
7	0h RO	**RESERVED1:** RESERVED
6:4	0h RO	**LPVCCNT:** Low Priority Extended VC Count
3	0h RO	**RESERVED2:** RESERVED
2:0	1h RO	**VCCNT:** Extended VC Count

15.5.40 PVCCAP2—Offset 108h

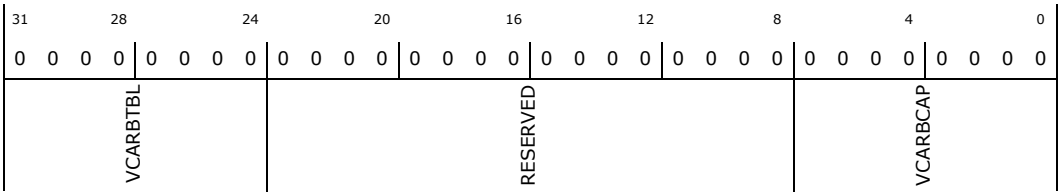
Port VC Capability 2

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PVCCAP2: [B:0, D:27, F:0] + 108h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**VCARBTBL:** VC Arbitration Table Offset
23:8	0h RO	**RESERVED:** RESERVED
7:0	0h RO	**VCARBCAP:** VC Arbitration Capability

15.5.41 PVCCTL—Offset 10Ch

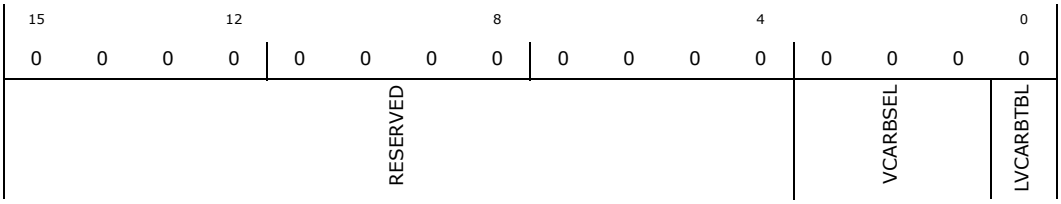
Port VC Control

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PVCCTL: [B:0, D:27, F:0] + 10Ch

Default: 0000h



Bit Range	Default & Access	Description
15:4	0h RO	**RESERVED:** RESERVED
3:1	0h RO	**VCARBSEL:** VC Arbitration Select
0	0h RO	**LVCARBTBL:** Load VC Arbitration Table

15.5.42 PVCSTS—Offset 10Eh

Port VC Status

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PVCSTS: [B:0, D:27, F:0] + 10Eh

Default: 0000h

Bit Range	Default & Access	Description
15:1	0h RO	**RESERVED:** RESERVED
0	0h RO	**VCARBTBLSTS:** VC Arbitration Table Status

15.5.43 VC0CAP—Offset 110h

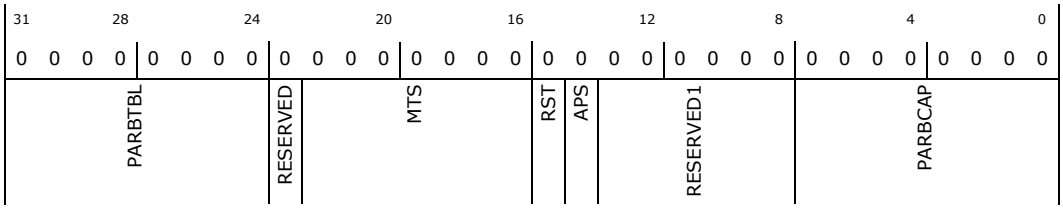
VC0 Resource Capability

Access Method

Type: PCI Configuration Register (Size: 32 bits)

VC0CAP: [B:0, D:27, F:0] + 110h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**PARBTBL:** Port Arbitration Table Offset
23	0h RO	**RESERVED:** RESERVED
22:16	0h RO	**MTS:** Maximum Time Slots
15	0h RO	**RST:** Reject Snoop Transactions

Bit Range	Default & Access	Description
14	0h RO	**APS:** Advanced Packet Switching
13:8	0h RO	**RESERVED1:** RESERVED
7:0	0h RO	**PARBCAP:** Port Arbitration Capability

15.5.44 VC0CTL—Offset 114h

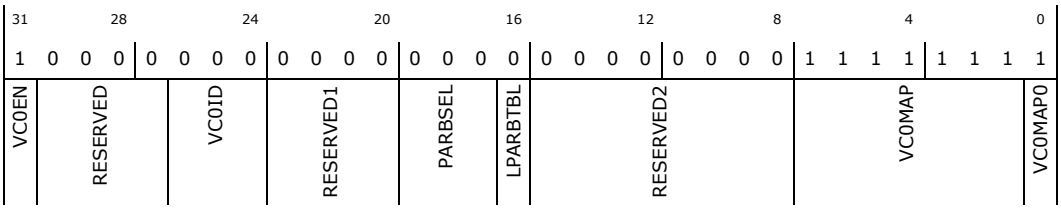
VC0 Resource Control

Access Method

Type: PCI Configuration Register (Size: 32 bits)

VC0CTL: [B:0, D:27, F:0] + 114h

Default: 800000FFh



Bit Range	Default & Access	Description
31	1h RO	**VC0EN:** VC0 Enable
30:27	0h RO	**RESERVED:** RESERVED
26:24	0h RO	**VC0ID:** VC0 ID
23:20	0h RO	**RESERVED1:** RESERVED
19:17	0h RO	**PARBSEL:** Port Arbitration Select
16	0h RO	**LPARBTBL:** Load Port Arbitration Table
15:8	0h RO	**RESERVED2:** RESERVED
7:1	7Fh RW	**VC0MAP:** TC/VC0 Map
0	1h RO	**VC0MAP0:** TC/VC0 Map

15.5.45 VC0STS—Offset 11Ah

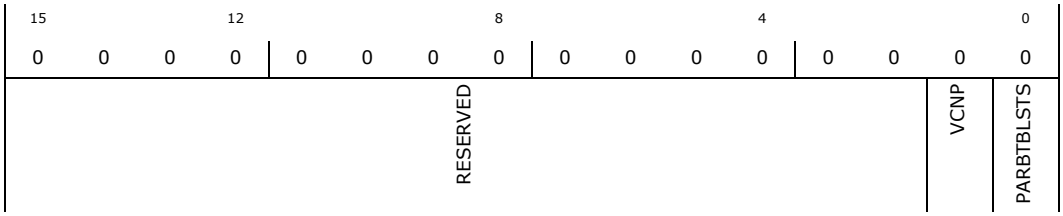
VC0 Resource Status

Access Method

Type: PCI Configuration Register (Size: 16 bits)

VC0STS: [B:0, D:27, F:0] + 11Ah

Default: 0000h



Bit Range	Default & Access	Description
15:2	0h RO	**RESERVED:** RESERVED
1	0h RO	**VCNP:** VC0 Negotiation Pending
0	0h RO	**PARBTBLSTS:** Port Arbitration Table Status

15.5.46 VCICAP—Offset 11Ch

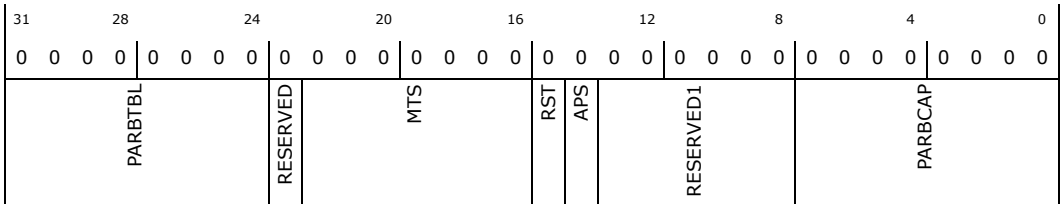
VCi Resource Capabilities

Access Method

Type: PCI Configuration Register (Size: 32 bits)

VCICAP: [B:0, D:27, F:0] + 11Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RO	**PARBTBL:** Port Arbitration Table Offset
23	0h RO	**RESERVED:** RESERVED
22:16	0h RO	**MTS:** Maximum Time Slots
15	0h RO	**RST:** Reject Snoop Transactions

Bit Range	Default & Access	Description
14	0h RO	**APS:** Advanced Packet Switching
13:8	0h RO	**RESERVED1:** RESERVED
7:0	0h RO	**PARBCAP:** Port Arbitration Capability

15.5.47 VCICTL—Offset 120h

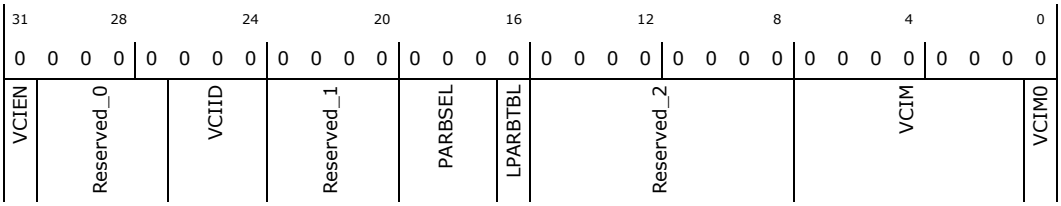
VCi control register

Access Method

Type: PCI Configuration Register (Size: 32 bits)

VCICTL: [B:0, D:27, F:0] + 120h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**VCIEN:** VCi Enable
30:27	0h RO	**Reserved_0:** Reserved
26:24	0h RW	**VCIID:** VCi ID
23:20	0h RO	**Reserved_1:** Reserved
19:17	0h RO	**PARBSEL:** Port arbitration select. Doesn't apply.
16	0h RO	**LPARBTBL:** Load port arbitration table. Dosn't apply.
15:8	0h RO	**Reserved_2:** reserved
7:1	0h RW	**VCIM:** TC/VCi map
0	0h RO	**VCIM0:** TC/VCi map bit 0. Not used.

15.5.48 VCISTS—Offset 126h

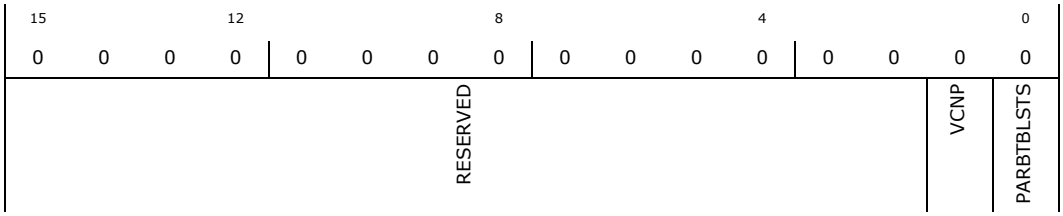
VCi Resource Status

Access Method

Type: PCI Configuration Register (Size: 16 bits)

VCISTS: [B:0, D:27, F:0] + 126h

Default: 0000h



Bit Range	Default & Access	Description
15:2	0h RO	**RESERVED:** RESERVED
1	0h RO	**VCNP:** VCi Negotiation Pending
0	0h RO	**PARBTBLSTS:** Port Arbitration Table Status

15.5.49 RCCAP—Offset 130h

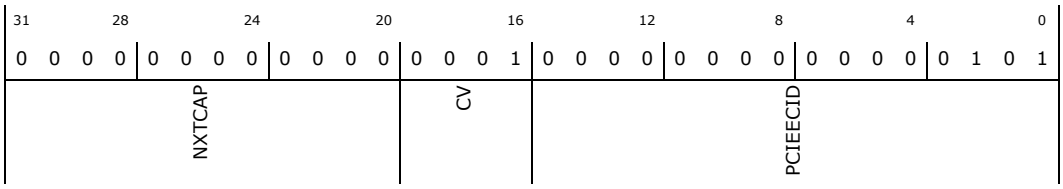
Root Complex Link Declaration Capability Header

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RCCAP: [B:0, D:27, F:0] + 130h

Default: 00010005h



Bit Range	Default & Access	Description
31:20	0h RO	**NXTCAP:** Next Capability Offset
19:16	1h RO	**CV:** Capability Version
15:0	5h RO	**PCIEECID:** PCI Express Extended Capability ID

15.5.50 ESD—Offset 134h

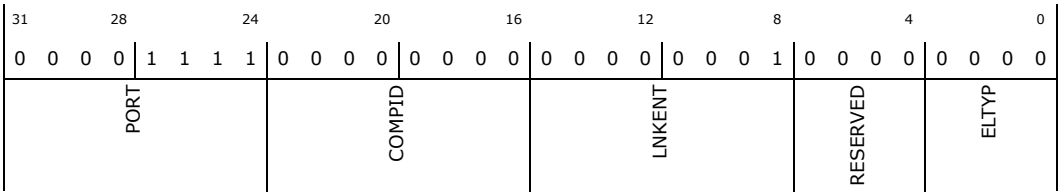
Element Self Description

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ESD: [B:0, D:27, F:0] + 134h

Default: 0F000100h



Bit Range	Default & Access	Description
31:24	0Fh RO	**PORT:** Port Number
23:16	00h RO	**COMPID:** Component ID
15:8	01h RO	**LNKENT:** Number of Link Entries
7:4	0h RO	**RESERVED:** RESERVED
3:0	0h RO	**ELTYP:** Element Type

15.5.51 L1DESC—Offset 140h

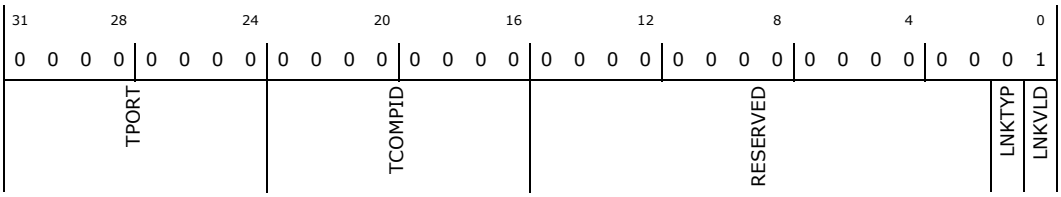
Link 1 Description

Access Method

Type: PCI Configuration Register (Size: 32 bits)

L1DESC: [B:0, D:27, F:0] + 140h

Default: 00000001h



Bit Range	Default & Access	Description
31:24	0h RO	**TPORT:** Target Port Number
23:16	0h RO	**TCOMPID:** Target Component ID

Bit Range	Default & Access	Description
15:2	0h RO	**RESERVED:** RESERVED
1	0h RO	**LNKTYP:** Link Type
0	1h RO	**LNKVLD:** Link Valid

15.5.52 L1LADD—Offset 148h

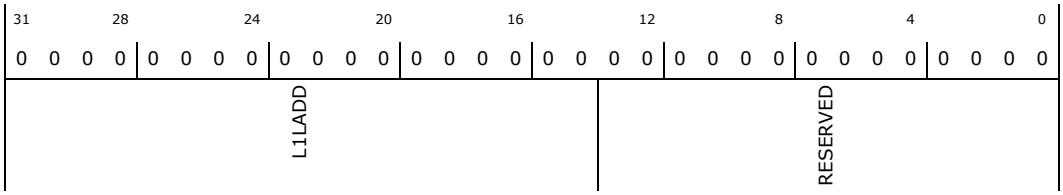
Link 1 Lower Address

Access Method

Type: PCI Configuration Register (Size: 32 bits)

L1LADD: [B:0, D:27, F:0] + 148h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0h RO	**L1LADD:** Link 1 Lower Address
13:0	0h RO	**RESERVED:** RESERVED

15.5.53 L1UADD—Offset 14Ch

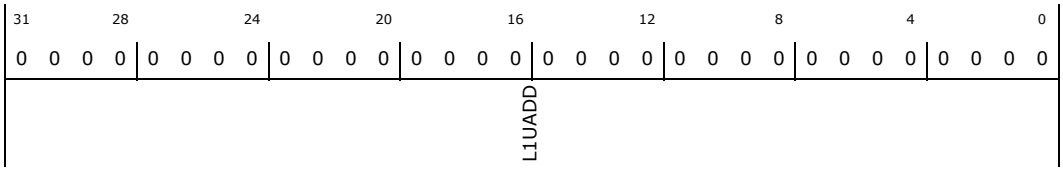
Link 1 Upper Address

Access Method

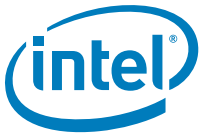
Type: PCI Configuration Register (Size: 32 bits)

L1UADD: [B:0, D:27, F:0] + 14Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**L1UADD:** Link 1 Upper Address



15.6 HD Audio Memory Mapped I/O Registers

Table 123. Summary of HD Audio Memory Mapped I/O Registers—AZLBAR

Offset	Size	Register ID—Description	Default Value
0h	2	"GCAP—Offset 0h" on page 578	4401h
2h	1	"VMIN—Offset 2h" on page 579	00h
3h	1	"VMAJ—Offset 3h" on page 579	01h
4h	2	"OUTPAY—Offset 4h" on page 580	003Ch
6h	2	"INPAY—Offset 6h" on page 581	001Dh
8h	4	"GCTL—Offset 8h" on page 581	00000000h
Ch	1	"WAKEEN—Offset Ch" on page 583	00h
Eh	1	"WAKESTS—Offset Eh" on page 584	00h
10h	2	"GSTS—Offset 10h" on page 584	0000h
18h	2	"OUTSTRMPAY—Offset 18h" on page 585	0030h
1Ah	2	"INSTRMPAY—Offset 1Ah" on page 586	0018h
20h	4	"INTCTL—Offset 20h" on page 587	00000000h
24h	4	"INTSTS—Offset 24h" on page 588	00000000h
30h	4	"WALCLK—Offset 30h" on page 589	00000000h
38h	4	"SSYNC—Offset 38h" on page 590	00000000h
40h	4	"CORBLBASE—Offset 40h" on page 591	00000000h
44h	4	"CORBUBASE—Offset 44h" on page 592	00000000h
48h	2	"CORBWP—Offset 48h" on page 592	0000h
4Ah	2	"CORBRP—Offset 4Ah" on page 593	0000h
4Ch	1	"CORBCTL—Offset 4Ch" on page 594	00h
4Dh	1	"CORBSTS—Offset 4Dh" on page 595	00h
4Eh	1	"CORBSIZE—Offset 4Eh" on page 596	42h
50h	4	"RIRBLBASE—Offset 50h" on page 597	00000000h
54h	4	"RIRBUBASE—Offset 54h" on page 598	00000000h
58h	2	"RIRBWP—Offset 58h" on page 599	0000h
5Ah	2	"RINTCNT—Offset 5Ah" on page 600	0000h
5Ch	1	"RIRBCTL—Offset 5Ch" on page 601	00h
5Dh	1	"RIRBSTS—Offset 5Dh" on page 602	00h
5Eh	1	"RIRBSIZE—Offset 5Eh" on page 603	42h
60h	4	"IC—Offset 60h" on page 604	00000000h
64h	4	"IR—Offset 64h" on page 605	00000000h
68h	2	"ICS—Offset 68h" on page 606	0000h
70h	4	"DPLBASE—Offset 70h" on page 607	00000000h
74h	4	"DPUBASE—Offset 74h" on page 608	00000000h
80h	4	"ISD0CTL_STS—Offset 80h" on page 609	00040000h
84h	4	"ISD0LPIB—Offset 84h" on page 611	00000000h
88h	4	"ISD0CBL—Offset 88h" on page 612	00000000h
8Ch	2	"ISD0LVI—Offset 8Ch" on page 613	0000h
8Eh	2	"ISD0FIFOW—Offset 8Eh" on page 614	0004h

Table 123. Summary of HD Audio Memory Mapped I/O Registers—AZLBAR (Continued)

Offset	Size	Register ID—Description	Default Value
90h	2	"ISD0FIFOS—Offset 90h" on page 614	0000h
92h	2	"ISD0FMT—Offset 92h" on page 615	0000h
98h	4	"ISD0BDLPLBA—Offset 98h" on page 616	00000000h
9Ch	4	"ISD0BDLPUBA—Offset 9Ch" on page 617	00000000h
A0h	4	"ISD1CTL_STS—Offset A0h" on page 618	00040000h
A4h	4	"ISD1LPIB—Offset A4h" on page 620	00000000h
A8h	4	"ISD1CBL—Offset A8h" on page 621	00000000h
ACh	2	"ISD1LVI—Offset ACh" on page 622	0000h
AEh	2	"ISD1FIFOW—Offset AEh" on page 623	0004h
B0h	2	"ISD1FIFOS—Offset B0h" on page 624	0000h
B2h	2	"ISD1FMT—Offset B2h" on page 625	0000h
B8h	4	"ISD1BDLPLBA—Offset B8h" on page 626	00000000h
BCh	4	"ISD1BDLPUBA—Offset BCh" on page 627	00000000h
C0h	4	"ISD2CTL_STS—Offset C0h" on page 628	00040000h
C4h	4	"ISD2LPIB—Offset C4h" on page 630	00000000h
C8h	4	"ISD2CBL—Offset C8h" on page 631	00000000h
CCh	2	"ISD2LVI—Offset CCh" on page 632	0000h
CEh	2	"ISD2FIFOW—Offset CEh" on page 633	0004h
D0h	2	"ISD2FIFOS—Offset D0h" on page 634	0000h
D2h	2	"ISD2FMT—Offset D2h" on page 635	0000h
D8h	4	"ISD2BDLPLBA—Offset D8h" on page 636	00000000h
DCh	4	"ISD2BDLPUBA—Offset DCh" on page 637	00000000h
E0h	4	"ISD3CTL_STS—Offset E0h" on page 638	00040000h
E4h	4	"ISD3LPIB—Offset E4h" on page 640	00000000h
E8h	4	"ISD3CBL—Offset E8h" on page 641	00000000h
ECh	2	"ISD3LVI—Offset ECh" on page 642	0000h
EEh	2	"ISD3FIFOW—Offset EEh" on page 643	0004h
F0h	2	"ISD3FIFOS—Offset F0h" on page 644	0000h
F2h	2	"ISD3FMT—Offset F2h" on page 645	0000h
F8h	4	"ISD3BDLPLBA—Offset F8h" on page 646	00000000h
FCh	4	"ISD3BDLPUBA—Offset FCh" on page 647	00000000h
100h	4	"OSD0CTL_STS—Offset 100h" on page 648	00040000h
104h	4	"OSD0LPIB—Offset 104h" on page 650	00000000h
108h	4	"OSD0CBL—Offset 108h" on page 651	00000000h
10Ch	2	"OSD0LVI—Offset 10Ch" on page 652	0000h
10Eh	2	"OSD0FIFOW—Offset 10Eh" on page 653	0004h
110h	2	"OSD0FIFOS—Offset 110h" on page 654	0000h
112h	2	"OSD0FMT—Offset 112h" on page 655	0000h
118h	4	"OSD0BDLPLBA—Offset 118h" on page 656	00000000h
11Ch	4	"OSD0BDLPUBA—Offset 11Ch" on page 657	00000000h
120h	4	"OSD1CTL_STS—Offset 120h" on page 658	00040000h
124h	4	"OSD1LPIB—Offset 124h" on page 660	00000000h

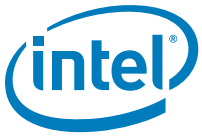


Table 123. Summary of HD Audio Memory Mapped I/O Registers—AZLBAR (Continued)

Offset	Size	Register ID—Description	Default Value
128h	4	"OSD1CBL—Offset 128h" on page 661	00000000h
12Ch	2	"OSD1LVI—Offset 12Ch" on page 662	0000h
12Eh	2	"OSD1FIFOW—Offset 12Eh" on page 663	0004h
130h	2	"OSD1FIFOS—Offset 130h" on page 664	0000h
132h	2	"OSD1FMT—Offset 132h" on page 665	0000h
138h	4	"OSD1BDLPLBA—Offset 138h" on page 666	00000000h
13Ch	4	"OSD1BDLPUBA—Offset 13Ch" on page 667	00000000h
140h	4	"OSD2CTL_STS—Offset 140h" on page 668	00040000h
144h	4	"OSD2LPIB—Offset 144h" on page 670	00000000h
148h	4	"OSD2CBL—Offset 148h" on page 671	00000000h
14Ch	2	"OSD2LVI—Offset 14Ch" on page 672	0000h
14Eh	2	"OSD2FIFOW—Offset 14Eh" on page 673	0004h
150h	2	"OSD2FIFOS—Offset 150h" on page 674	0000h
152h	2	"OSD2FMT—Offset 152h" on page 675	0000h
158h	4	"OSD2BDLPLBA—Offset 158h" on page 676	00000000h
15Ch	4	"OSD2BDLPUBA—Offset 15Ch" on page 677	00000000h
160h	4	"OSD3CTL_STS—Offset 160h" on page 678	00040000h
164h	4	"OSD3LPIB—Offset 164h" on page 680	00000000h
168h	4	"OSD3CBL—Offset 168h" on page 681	00000000h
16Ch	2	"OSD3LVI—Offset 16Ch" on page 682	0000h
16Eh	2	"OSD3FIFOW—Offset 16Eh" on page 683	0004h
170h	2	"OSD3FIFOS—Offset 170h" on page 684	0000h
172h	2	"OSD3FMT—Offset 172h" on page 685	0000h
178h	4	"OSD3BDLPLBA—Offset 178h" on page 686	00000000h
17Ch	4	"OSD3BDLPUBA—Offset 17Ch" on page 687	00000000h
2030h	4	"WLCLKA—Offset 2030h" on page 688	00000000h
2084h	4	"ISD0LPIBA—Offset 2084h" on page 689	00000000h
20A4h	4	"ISD1LPIBA—Offset 20A4h" on page 690	00000000h
20C4h	4	"ISD2LPIBA—Offset 20C4h" on page 691	00000000h
20E4h	4	"ISD3LPIBA—Offset 20E4h" on page 692	00000000h
2104h	4	"OSD0LPIBA—Offset 2104h" on page 693	00000000h
2124h	4	"OSD1LPIBA—Offset 2124h" on page 694	00000000h
2144h	4	"OSD2LPIBA—Offset 2144h" on page 695	00000000h
2164h	4	"OSD3LPIBA—Offset 2164h" on page 696	00000000h

15.6.1 GCAP—Offset 0h

Global Capabilities

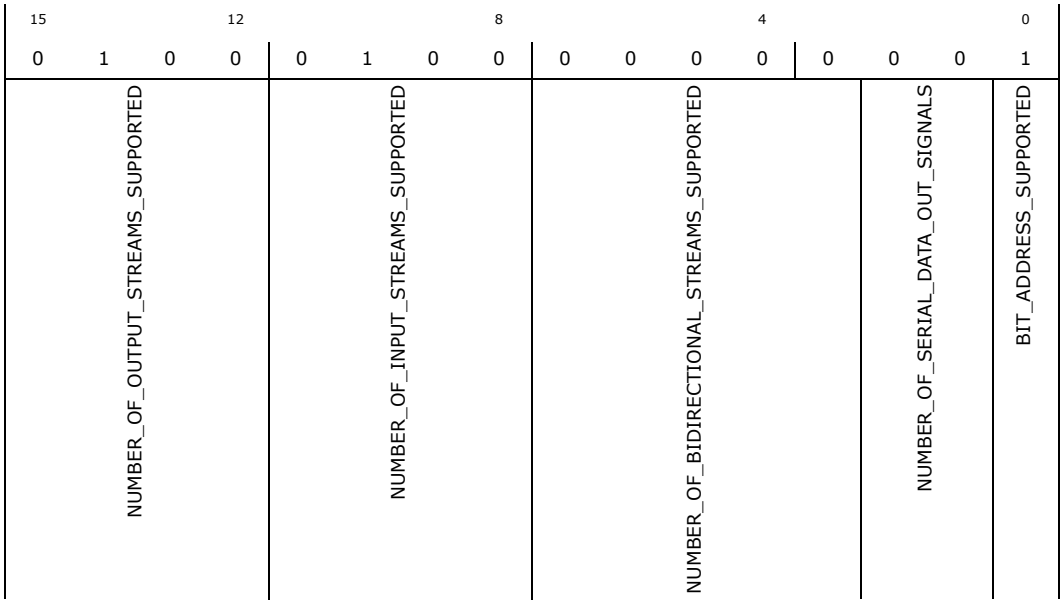
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

GCAP: [AZLBAR] + 0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 4401h



Bit Range	Default & Access	Description
15:12	4h RW	**NUMBER_OF_OUTPUT_STREAMS_SUPPORTED:** 0011b indicates that in this processor, Intel HD Audio controller supports three output streams.
11:8	4h RW	**NUMBER_OF_INPUT_STREAMS_SUPPORTED:** 0011b indicates that in this processor, Intel HD Audio controller supports three output streams.
7:3	00h RO	**NUMBER_OF_BIDIRECTIONAL_STREAMS_SUPPORTED:** 00000b indicates that the Intel HD Audio controller supports 0 bidirectional streams.
2:1	0h RO	**NUMBER_OF_SERIAL_DATA_OUT_SIGNALS:** 00b indicates that the Intel HD Audio controller supports one Serial Data Output signal.
0	01h RW	**BIT_ADDRESS_SUPPORTED:** A 1 indicates that the Intel HD Audio controller supports 64 bit addressing for BDL addresses data buffer addresses and command buffer addresses.

15.6.2 VMIN—Offset 2h

Minor Version

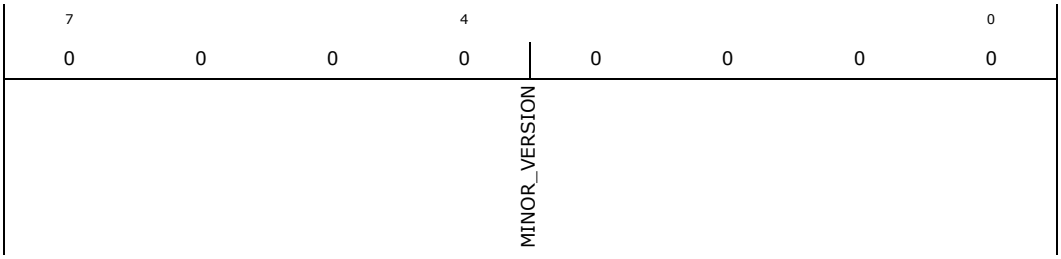
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

VMIN: [AZLBAR] + 2h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**MINOR_VERSION:** Indicates processor supports minor revision number 00h of the Intel HD Audio specification.

15.6.3 VMAJ—Offset 3h

Major Version

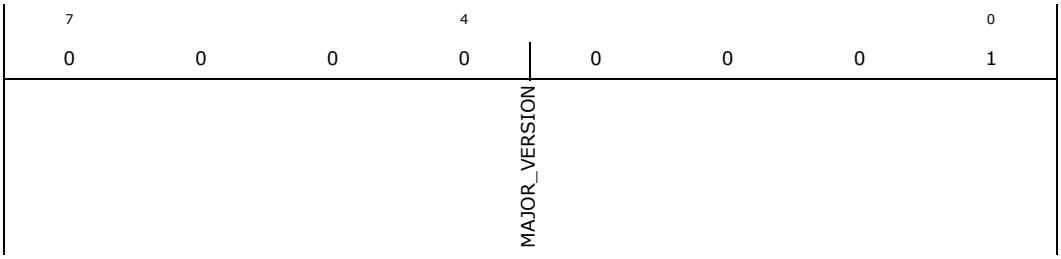
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

VMAJ: [AZLBAR] + 3h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 01h



Bit Range	Default & Access	Description
7:0	01h RO	**MAJOR_VERSION:** Indicates processor supports major revision number 1 of the Intel HD Audio specification.

15.6.4 OUTPAY—Offset 4h

Output Payload Capability

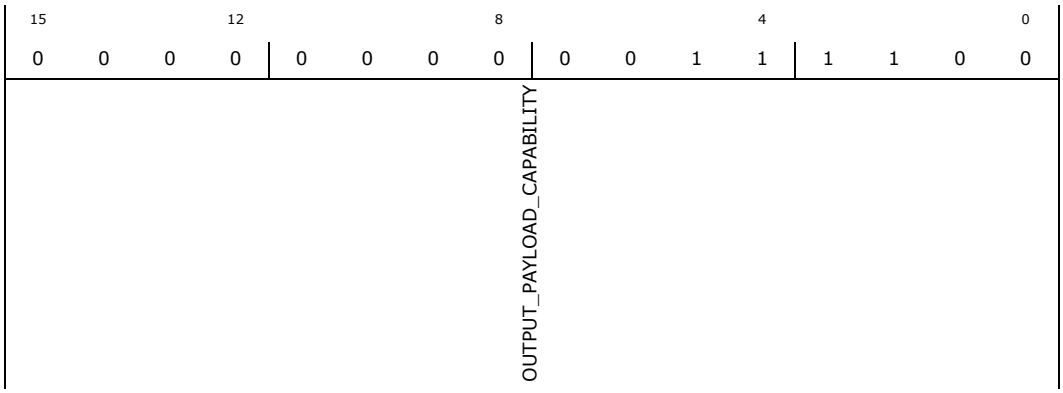
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OUTPAY: [AZLBAR] + 4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 003Ch



Bit Range	Default & Access	Description
15:0	003Ch RO	**OUTPUT_PAYLOAD_CAPABILITY:** Indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16 bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz the data is double pumped provides 1000 bits per frame or 62.5 words in total. 40 bits are used for command and control leaving 60 words available for data payload. 00h 0 words 01h 1 word payload FFh 255h word payload

15.6.5 INPAY—Offset 6h

Input Payload Capability

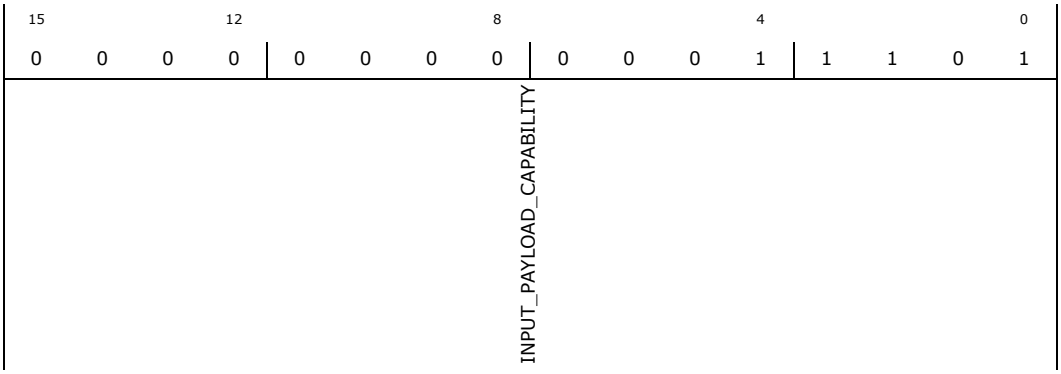
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

INPAY: [AZLBAR] + 6h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 001Dh



Bit Range	Default & Access	Description
15:0	001Dh RO	**INPUT_PAYLOAD_CAPABILITY:** Indicates the total input payload available on the link. This does not include bandwidth used for response. This measurement is in 16 bit word quantities per 48 kHz frame. The default link clock speed of 24.000 MHz provides 500 bits per frame or 31.25 words in total. 36 bits are used for response leaving 29 words for data payload. 00h 0 words 01h 1 word payload FFh 255h word payload

15.6.6 GCTL—Offset 8h

Global Control

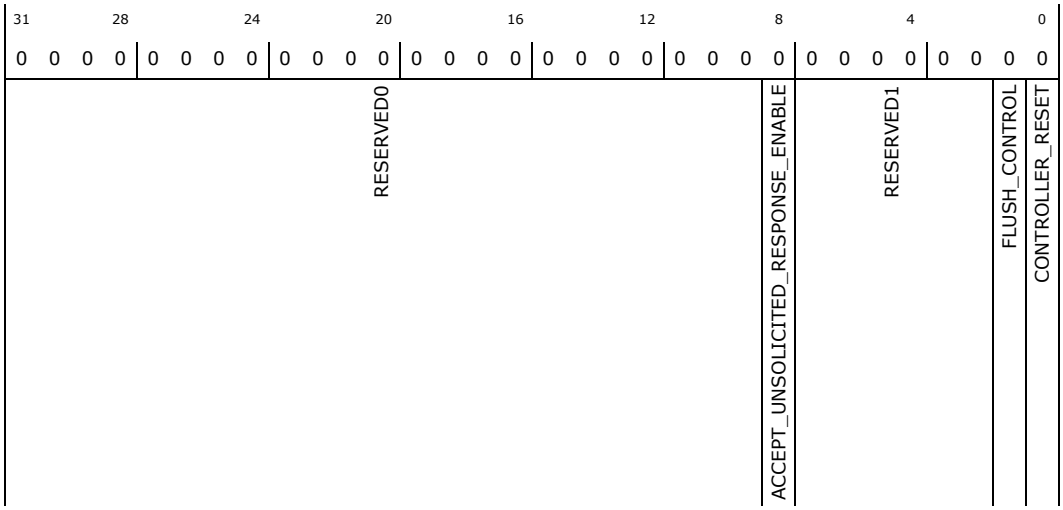
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GCTL: [AZLBAR] + 8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0h RO	**RESERVED0:** reserved
8	0h RW	**ACCEPT_UNSOLICITED_RESPONSE_ENABLE:** If UNSOL is a 1 Unsolicited Responses from the codecs are accepted by the controller and placed into the Response Input Ring Buffer. If UNSOL is a 0 unsolicited responses are not accepted and dropped on the floor.
7:2	00h RO	**RESERVED1:** reserved
1	0h RW	**FLUSH_CONTROL:** Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated the DMA Position Buffer must be programmed with a valid memory address by software but the DMA Position Buffer bit 0 need not be set to enable the position reporting mechanism. Also all streams must be stopped the associated RUN bit must be 0 . When the flush is initiated the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.
0	0h RW	**CONTROLLER_RESET:** Writing a 0 to this bit causes the Intel HD Audio controller to be reset. All state machines FIFO s and non Suspend well memory mapped configuration registers except ECAP and PCI Configuration Registers in the controller will be reset. The Intel HD Audio link RESET signal will be asserted and all other link signals will be driven to their reset values. After the hardware has completed sequencing into the reset state it will report a 0 in this bit. Software must read a 0 from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit its reset state and de assert the Intel HD Audio link RESET signal. Software is responsible forsetting clearing this bit such that the minimum Intel HD Audio link RESET signal assertion pulse width specification is met. When the controller hardware is ready to begin operation it will report a1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST bit defaults to a 0 after hardware reset therefore software needs to write a 1 to this bit to begin operation. Note thatthe CORB RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST is written to 0 asserted in order to assure a clean re start. When setting or clearing CRST software must ensure that minimum link timing requirements minimum RESET assertion time etc. are met. When CRST is 0 indicating that the controller is in reset writes to all Intel HD Audio memory mapped registers are ignored as if the device is not present. The only exception is the Global Control register containing the CRST bit itself. The Global Control register is write able as a DWord Word or Byte even when CRST is 0 if the byte enable for the byte containing the CRST bit Byte Enable 0 is active. If Byte Enable 0 is not active writes to the Global Control register will be ignored when CRST is 0. When CRST is 0 reads to Intel HD Audio memory mapped registers will return their default value except for registers that are not reset with PLTRST or on a D3hot gt D0 transition.

15.6.7 WAKEEN—Offset Ch

Wake Enable

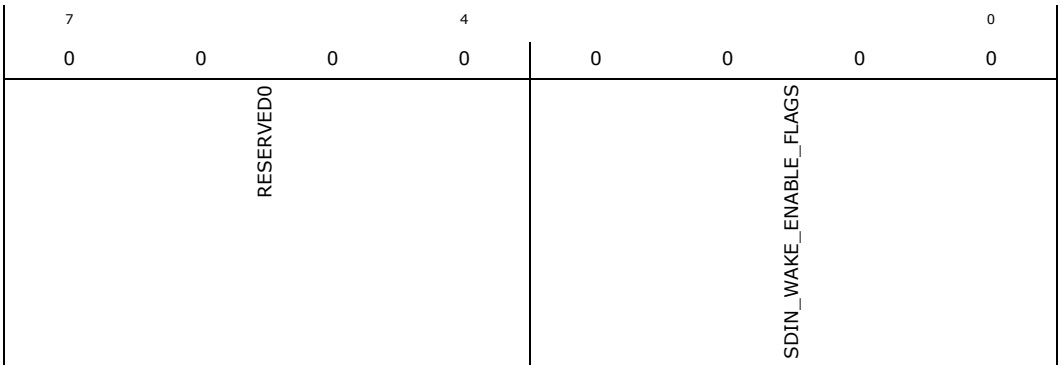
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

WAKEEN: [AZLBAR] + Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:4	0h RO	**RESERVED0:** reserved
3:0	0h RW	**SDIN_WAKE_ENABLE_FLAGS:** Bits which control which SDI signal s may generate a wake event. A 1 bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake.

15.6.8 WAKESTS—Offset Eh

Wake Status

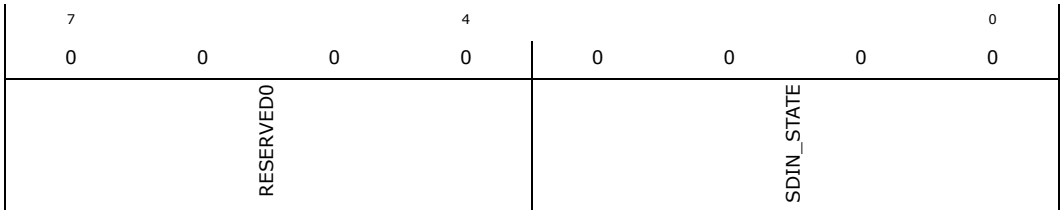
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

WAKESTS: [AZLBAR] + Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:4	0h RO	**RESERVED0:** reserved
3:0	0h RO	**SDIN_STATE:** Flag bits that indicate which SDI signal s received a State Change event. The bits are cleared by writing 1 s to them.

15.6.9 GSTS—Offset 10h

Global Status

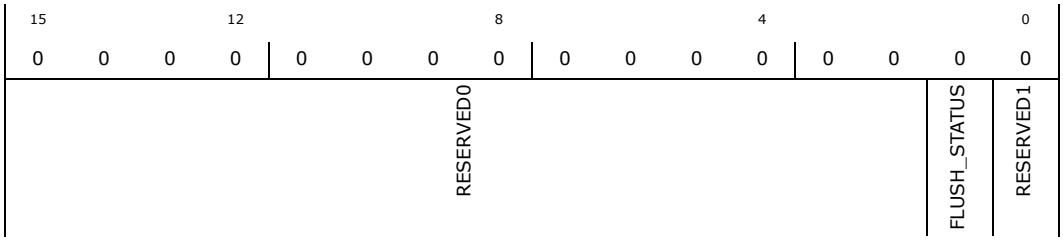
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

GSTS: [AZLBAR] + 10h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:2	0000h RO	**RESERVED0:** reserved
1	0h RW	**FLUSH_STATUS:** This bit is set to a 1 by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a 1to clear this bit before the next time FCNTRL is set.
0	0h RO	**RESERVED1:** reserved

15.6.10 OUTSTRMPAY—Offset 18h

Output Stream Payload Capability

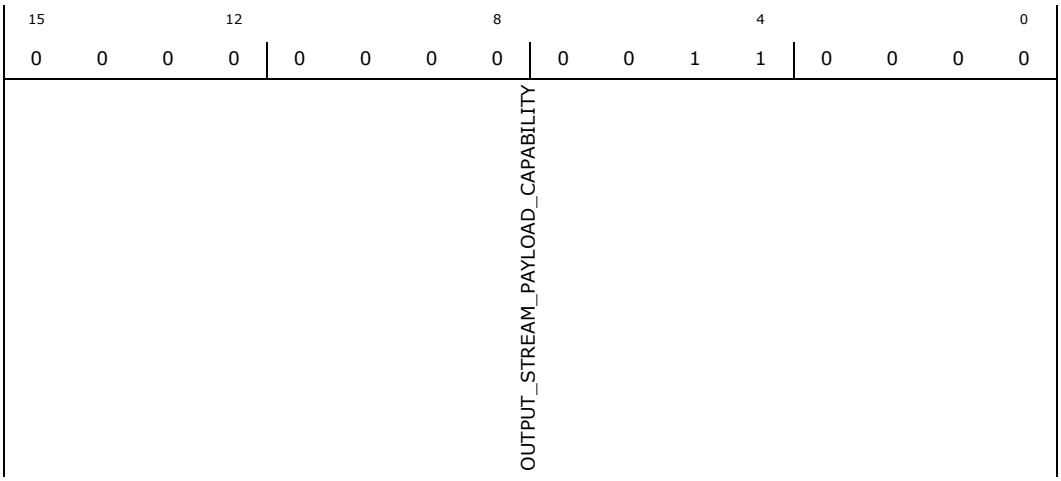
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OUTSTRMPAY: [AZLBAR] + 18h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0030h



Bit Range	Default & Access	Description
15:0	0030h RO	**OUTPUT_STREAM_PAYLOAD_CAPABILITY:** Indicates maximum number of words per frame for any single output stream. This measurement is in 16 bit word quantities per 48 kHz frame. 48 Words 96B is the maximum supported therefore a value of 30h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h 0 words 01h 1 word payload FFh 255h word payload

15.6.11 INSTRMPAY—Offset 1Ah

Input Stream Payload Capability

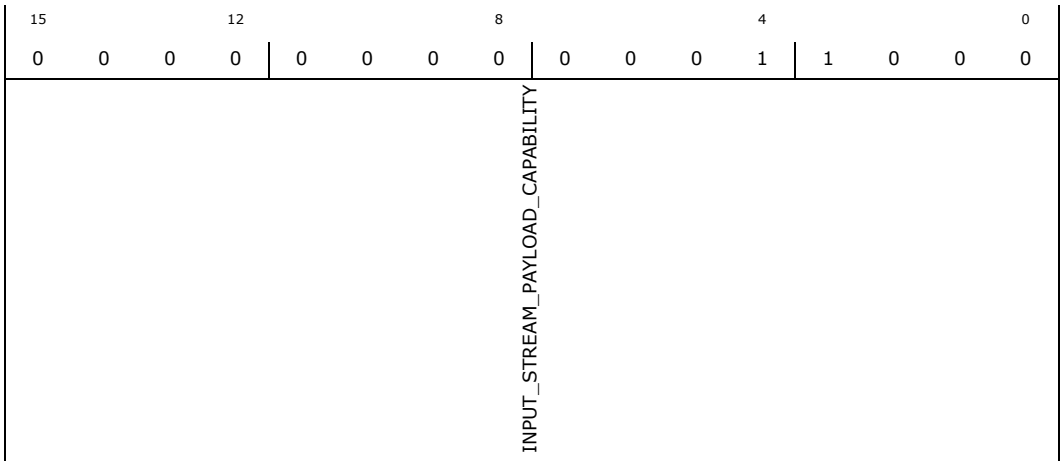
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

INSTRMPAY: [AZLBAR] + 1Ah

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0018h



Bit Range	Default & Access	Description
15:0	0018h RO	**INPUT_STREAM_PAYLOAD_CAPABILITY:** Indicates maximum number of words per frame for any single input stream. This measurement is in 16 bit word quantities per 48 kHz frame. 24 Words 48B is the maximum supported therefore a value of 18h is reported in this register. Software must ensure that a format which would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h 0 words 01h 1 word payload FFh 255h word payload

15.6.12 INTCTL—Offset 20h

Interrupt Control

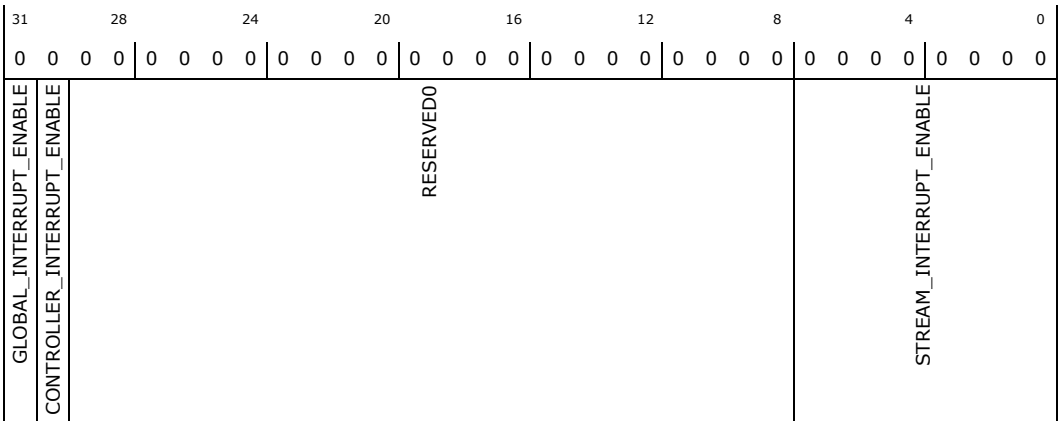
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

INTCTL: [AZLBAR] + 20h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**GLOBAL_INTERRUPT_ENABLE:** Global bit to enable device interrupt generation. When set to 1 the Intel HD Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space such as the Interrupt Enable bit in the PCI Configuration Space. This bit is not affected by controller reset.
30	0h RW	**CONTROLLER_INTERRUPT_ENABLE:** Enables the general interrupt for controller functions. When set to 1 and GIE is enabled the controller generates an interrupt when the CIS bit gets set. This bit is not affected by controller reset.
29:8	0h RO	**RESERVED0:** reserved
7:0	00h RW	**STREAM_INTERRUPT_ENABLE:** When set to 1 the individual Streams are enabled to generate an interrupt when the corresponding stream status bits get set. A stream interrupt will be caused as a result of a buffer with IOC 1 in the BDL entry being completed or as a result of a FIFO error underrun or overrun occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially based on their order in the register set. Bit 0 Input Stream 1 Bit 1 Input Stream 2 Bit 2 Input Stream 3 Bit 3 Input Stream 4 Bit 4 Output Stream 1 Bit 5 Output Stream 2 Bit 6 Output Stream 3 Bit 7 Output Stream 4

15.6.13 INTSTS—Offset 24h

Interrupt Status

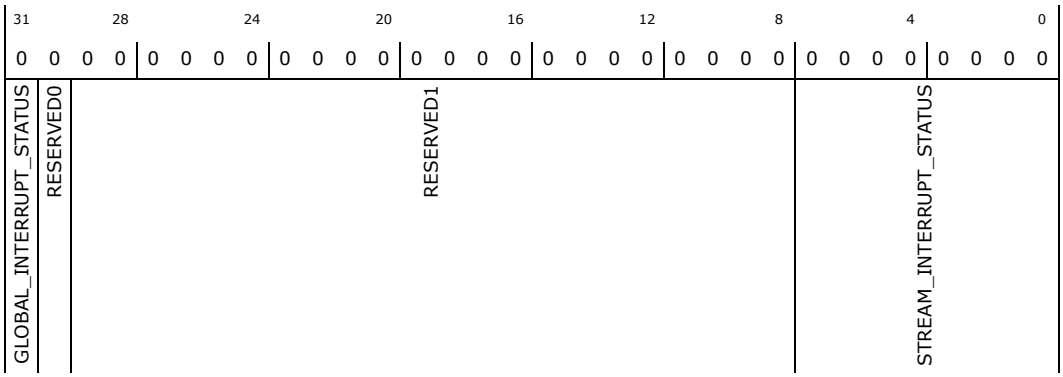
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

INTSTS: [AZLBAR] + 24h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RO	**GLOBAL_INTERRUPT_STATUS:** This bit is an OR of all of the interrupt status bits in this register.
30	0h RO	**RESERVED0:** Status of general controller interrupt. A 1 indicates that an interrupt condition occurred due to a Response Interrupt a Response Buffer Overrun Interrupt CORB Memory Error Interrupt Error Present Interrupt Intel Reserved or a SDIN State Change event. The exact cause can be determined by interrogating other registers. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of the stated interrupt status bits for this register.
29:8	0h RO	**RESERVED1:** reserved
7:0	00h RW	**STREAM_INTERRUPT_STATUS:** A 1 indicates that an interrupt condition occurred on the corresponding Stream. Note that a HW interrupt will not be generated unless the corresponding enable bit is set. This bit is an OR of all of an individual stream s interrupt status bits. The streams are numbered and the SIS bits assigned sequentially based on their order in the register set. Bit 0 Input Stream 1 Bit 1 Input Stream 2 Bit 2 Input Stream 3 Bit 3 Input Stream 4 Bit 4 Output Stream 1 Bit 5 Output Stream 2 Bit 6 Output Stream 3 Bit 7 Output Stream 4

15.6.14 WALCLK—Offset 30h

Wall Clock Counter

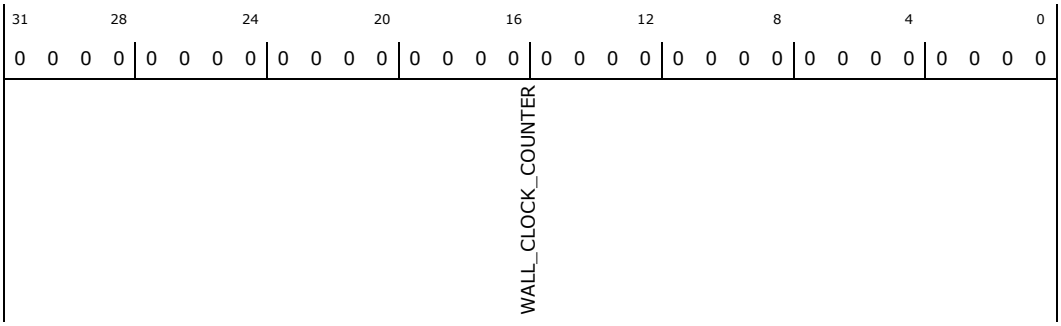
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

WALCLK: [AZLBAR] + 30h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**WALL_CLOCK_COUNTER:** 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

15.6.15 SSYNC—Offset 38h

Stream Synchronization

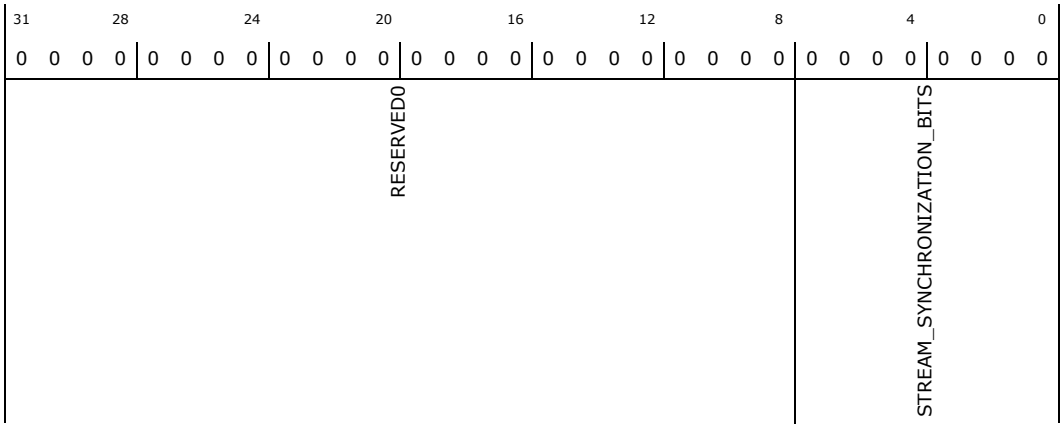
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SSYNC: [AZLBAR] + 38h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0h RO	**RESERVED0:** reserved
7:0	00h RW	**STREAM_SYNCHRONIZATION_BITS:** The Stream Synchronization bits when set to 1 block data from being sent on or received from the link. Each bit controls the associated Stream Descriptor bit 0 corresponds to the first Stream Descriptor etc. To synchronously start a set of DMA engines the bits in the SSYNC register are first set to a 1. The RUN bits for the associated Stream Descriptors are then set to a 1 to start the DMA engines. When all streams are ready FIFORDY 1 the associated SSYNC bits can all be set to 0 at the same time and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams first the bits are set in the SSYNC register and then the individual RUN bits in the Stream Descriptors are cleared by software. The streams are numbered and the SSYNC bits assigned sequentially based on their order in the register set. Bit 0 Input Stream 1 Bit 1 Input Stream 2 Bit 2 Input Stream 3 Bit 3 Input Stream 4 Bit 4 Output Stream 1 Bit 5 Output Stream 2 Bit 6 Output Stream 3 Bit 7 Output Stream 4 Each bit can be reset by their respective stream reset.

15.6.16 CORBLBASE—Offset 40h

CORB Lower Base Address

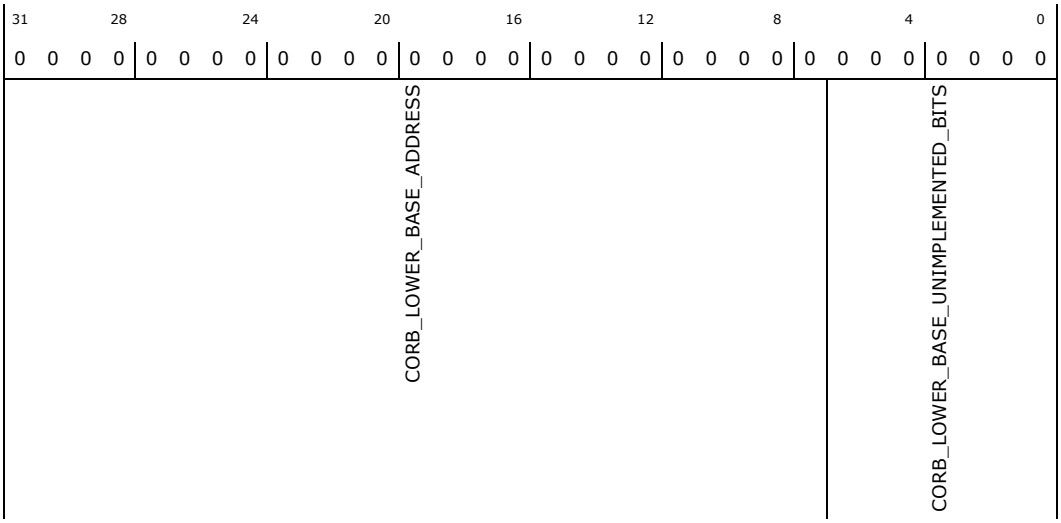
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CORBLBASE: [AZLBAR] + 40h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**CORB_LOWER_BASE_ADDRESS:** Lower address of the Command Output Ring Buffer allowing the CORB Base Address to be assigned on any 64 B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	00h RO	**CORB_LOWER_BASE_UNIMPLEMENTED_BITS:** Hardwired to 0. This requires the CORB to be allocated with 128 byte granularity to allow for cache line fetch optimizations.

15.6.17 CORBUBASE—Offset 44h

CORB Upper Base Address

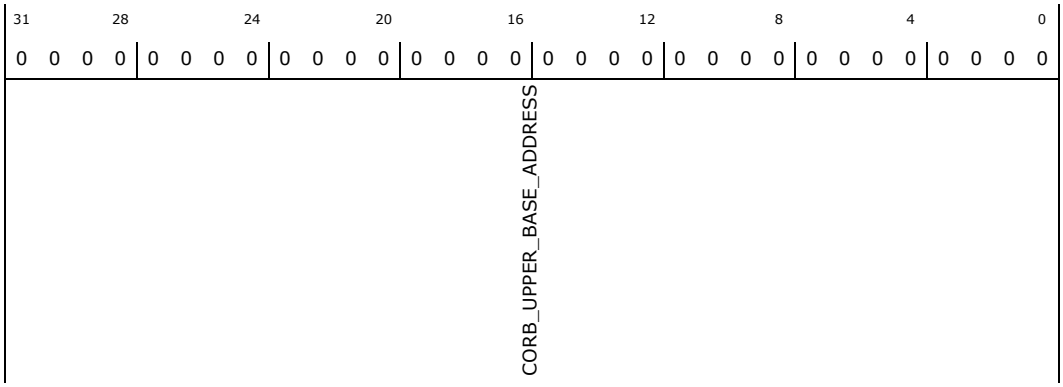
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CORBUBASE: [AZLBAR] + 44h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CORB_UPPER_BASE_ADDRESS:** Upper 32 bits of address of the Command Output Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

15.6.18 CORBWP—Offset 48h

CORB Write Pointer

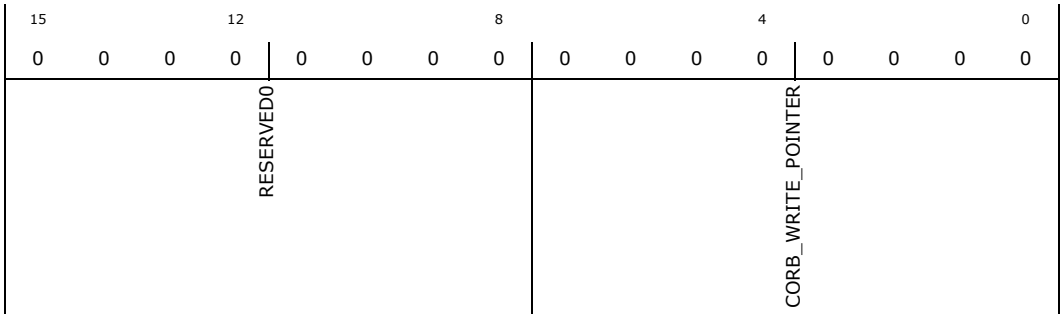
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CORBWP: [AZLBAR] + 48h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**CORB_WRITE_POINTER:** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the Read Pointer matches the Write Pointer. Supports 256 CORB entries 256 x 4B 1KB . This field may be written while the DMA engine is running.

15.6.19 CORBRP—Offset 4Ah

CORB Read Pointer

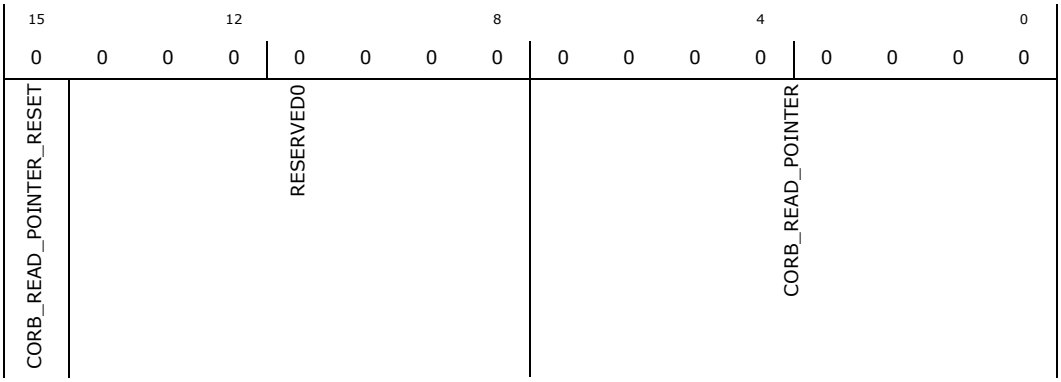
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

CORBRP: [AZLBAR] + 4Ah

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RW	**CORB_READ_POINTER_RESET:** Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual pre fetched commands in the CORB hardware buffer within the Intel Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	00h RO	**RESERVED0:** reserved
7:0	00h RO	**CORB_READ_POINTER:** Software reads this field to determine how many commands it can write to the CORB without over running. The value read indicates the CORB Read Pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over written by software. Supports 256 CORB entries 256 x 4B 1KB . This field may be read while the DMA engine is running.

15.6.20 CORBCTL—Offset 4Ch

CORB Control

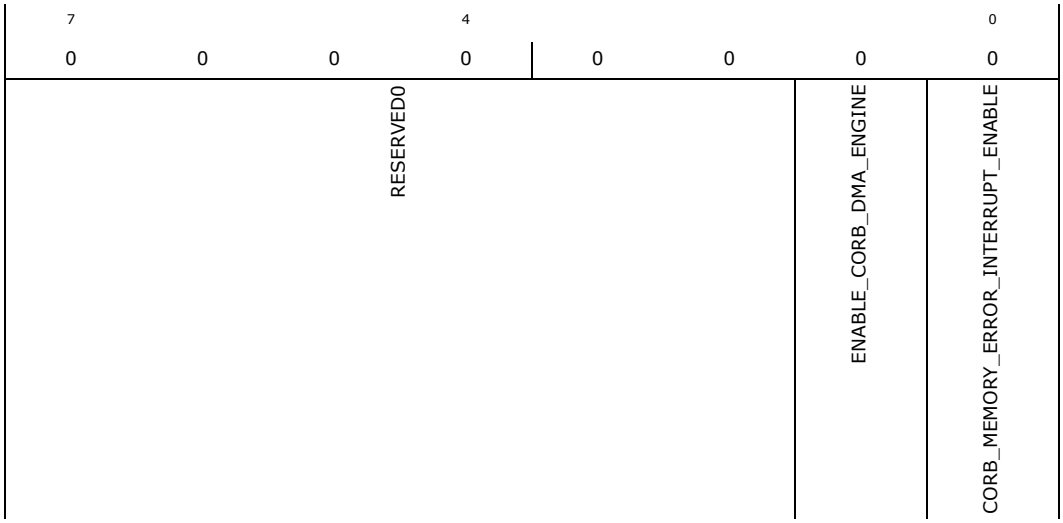
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

CORBCTL: [AZLBAR] + 4Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:2	00h RO	**RESERVED0:** reserved
1	0h RW	**ENABLE_CORB_DMA_ENGINE:** 0 DMA Stop 1 DMA Run After SW writes a 0 to this bit the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**CORB_MEMORY_ERROR_INTERRUPT_ENABLE:** If this bit is set and GIE and CIE are enabled the controller will generate an interrupt if the MEI status bit is set.

15.6.21 CORBSTS—Offset 4Dh

CORB Status

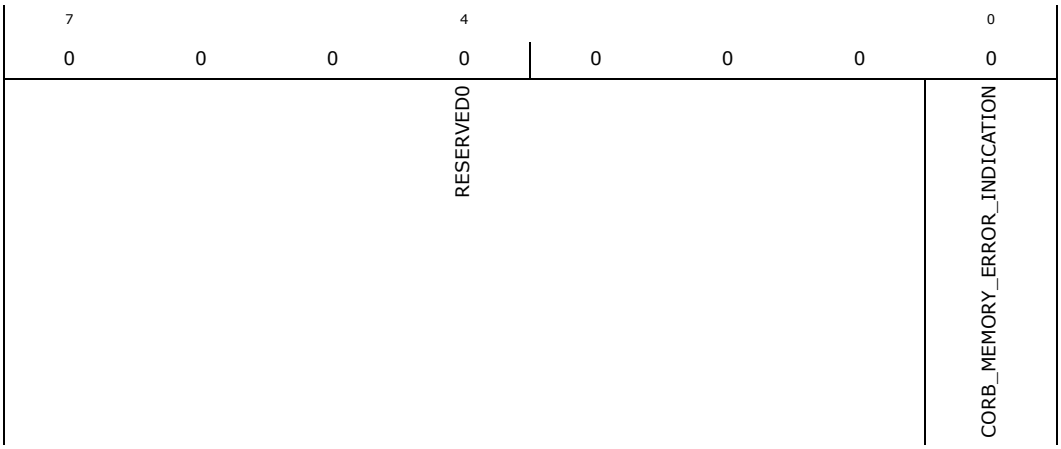
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

CORBSTS: [AZLBAR] + 4Dh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:1	00h RO	**RESERVED0:** reserved
0	0h RW	**CORB_MEMORY_ERROR_INDICATION:** If this status bit is set the controller has detected an error in the pathway between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However this type of error leaves the audio subsystem in an unviable state and typically requires CRST .

15.6.22 CORBSIZE—Offset 4Eh

CORB Size

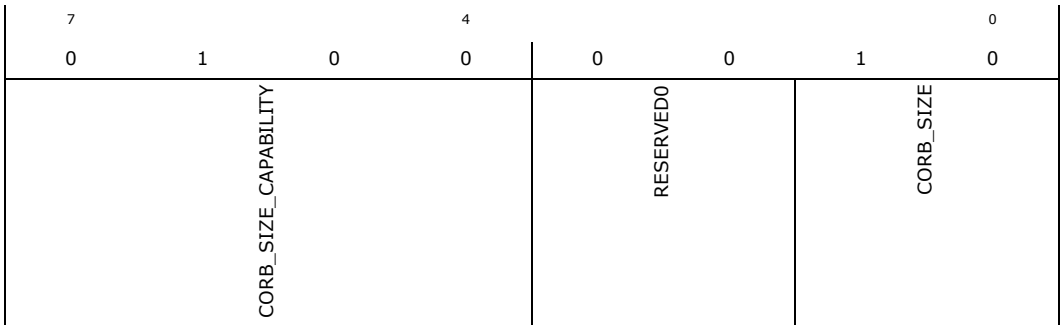
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

CORBSIZE: [AZLBAR] + 4Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 42h



Bit Range	Default & Access	Description
7:4	4h RO	**CORB_SIZE_CAPABILITY:** 0100b indicates that the HD Audio controller only supports a CORB size of 256 CORB entries 1024B .
3:2	0h RO	**RESERVED0:** reserved
1:0	02h RO	**CORB_SIZE:** Hardwired to 10b which sets the CORB size to 256 entries 1024B .

15.6.23 RIRBLBASE—Offset 50h

RIRB Lower Base Address

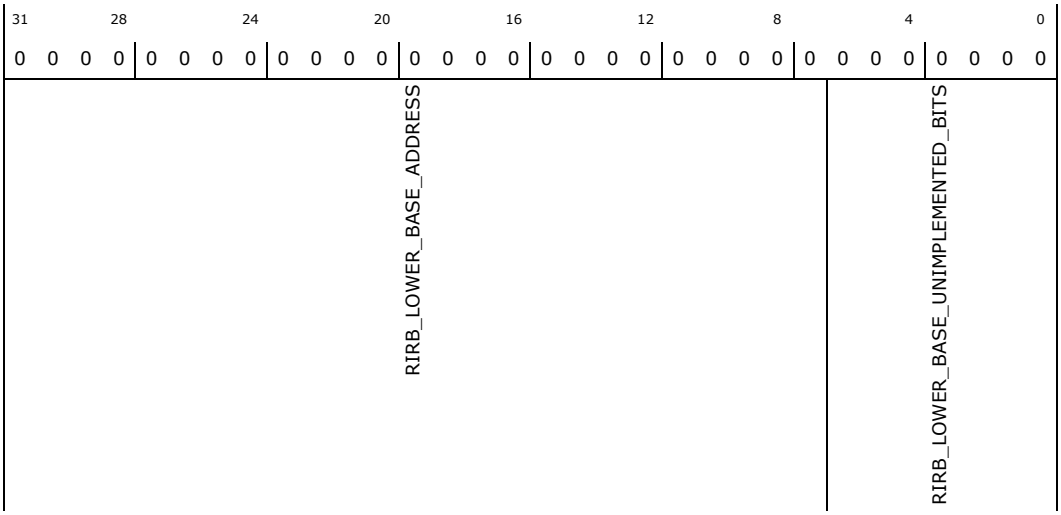
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RIRBLBASE: [AZLBAR] + 50h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**RIRB_LOWER_BASE_ADDRESS:** Lower address of the Response Input Ring Buffer allowing the RIRB Base Address to be assigned on any 64 B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	00h RO	**RIRB_LOWER_BASE_UNIMPLEMENTED_BITS:** Hardwired to 0 to force 128 byte buffer alignment for cache line fetch optimizations.

15.6.24 RIRBUBASE—Offset 54h

RIRB Upper Base Address

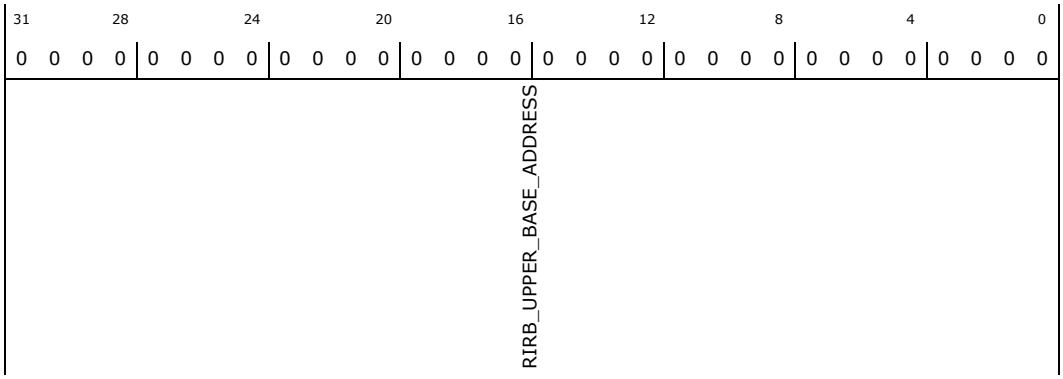
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

RIRBUBASE: [AZLBAR] + 54h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**RIRB_UPPER_BASE_ADDRESS:** Upper 32 bits of address of the Response Input Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

15.6.25 RIRBWP—Offset 58h

RIRB Write Pointer

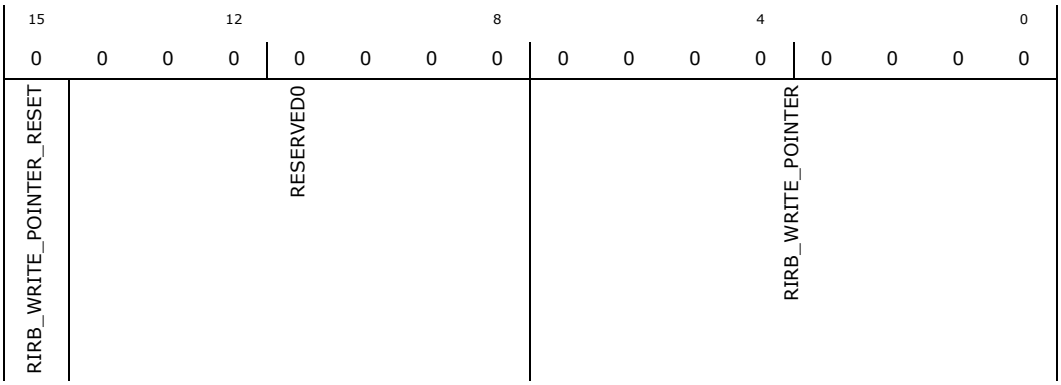
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

RIRBWP: [AZLBAR] + 58h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h WO	**RIRB_WRITE_POINTER_RESET:** Software writes a 1 to this bit to reset the RIRB Write Pointer to 0 s. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0.
14:8	00h RO	**RESERVED0:** reserved
7:0	00h RO	**RIRB_WRITE_POINTER:** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword RIRB entry units since each RIRB entry is 2 Dwords long . Supports up to 256 RIRB entries 256 x 8B 2KB . This field may be read while the DMA engine is running.

15.6.26 RINTCNT—Offset 5Ah

Response Interrupt Count

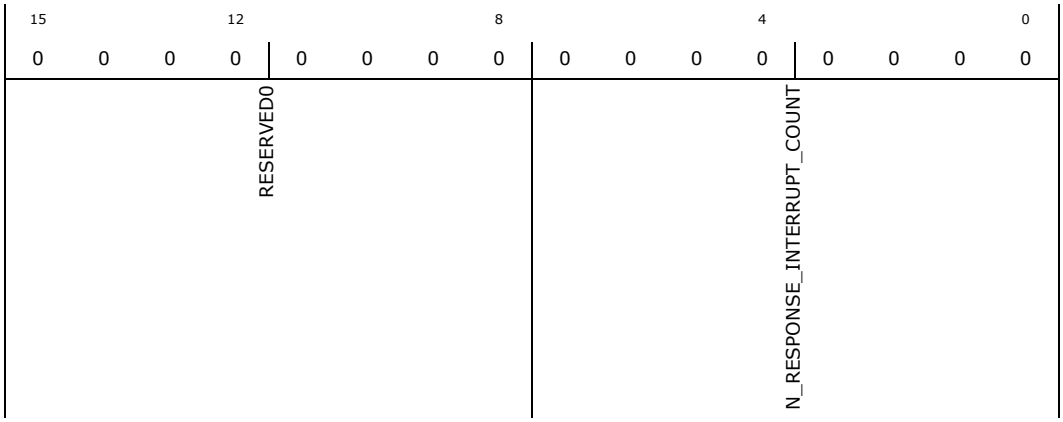
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

RINTCNT: [AZLBAR] + 5Ah

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**N_RESPONSE_INTERRUPT_COUNT:** 0000_0001b 1 Response sent to RIRB 1111_1111b 255 Responses sent to RIRB 0000_0000b 256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned as opposed to the number of frames in which there were responses. If more than one codec responds in one frame then the count is increased by the number of responses received in the frame.

15.6.27 RIRBCTL—Offset 5Ch

RIRB Control

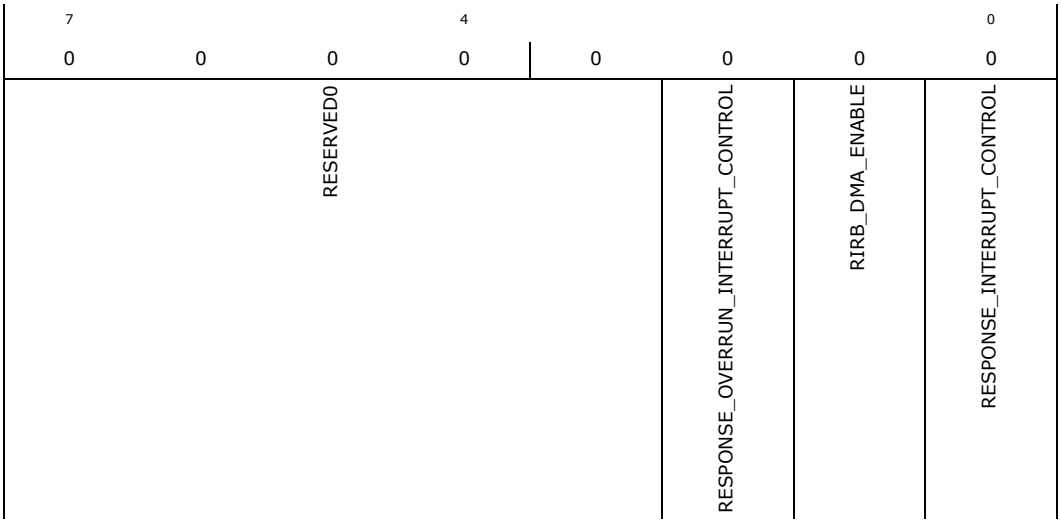
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

RIRBCTL: [AZLBAR] + 5Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	00h RO	**RESERVED0:** reserved
2	0h RW	**RESPONSE_OVERRUN_INTERRUPT_CONTROL:** If this bit is set and GIE and CIE are enabled the hardware will generate an interrupt when the Response Overrun Interrupt Status bit is set.
1	0h RW	**RIRB_DMA_ENABLE:** 0 DMA Stop 1 DMA Run After SW writes a 0 to this bit the HW may not stop immediately. The hardware will physically update the bit to a 0 when the DMA engine is truly stopped. SW must read a 0 from this bit to verify that the DMA is truly stopped.
0	0h RW	**RESPONSE_INTERRUPT_CONTROL:** 0 Disable Interrupt 1 Generate an interrupt if GIE and CIE are enabled after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI_x inputs whichever occurs first . The N counter is reset when the interrupt is generated.

15.6.28 RIRBSTS—Offset 5Dh

RIRB Status

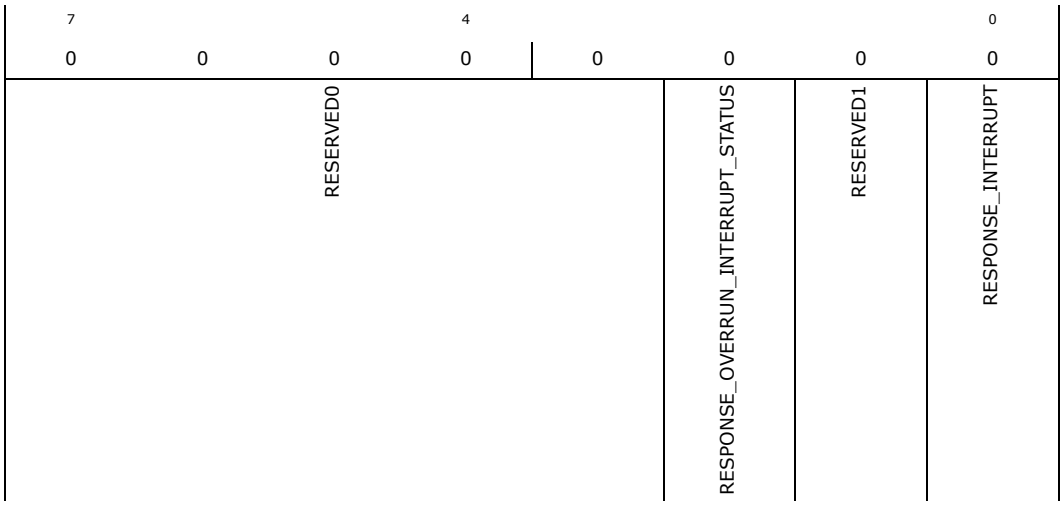
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

RIRBSTS: [AZLBAR] + 5Dh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	00h RO	**RESERVED0:** reserved
2	0h RW	**RESPONSE_OVERRUN_INTERRUPT_STATUS:** Hardware sets this bit to a 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.
1	0h RO	**RESERVED1:** reserved
0	0h RW	**RESPONSE_INTERRUPT:** Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI x inputs whichever occurs first . Note that this status bit is set even if an interrupt is not enabled for this event. Software clears this flag by writing a 1 to this bit.

15.6.29 RIRBSIZE—Offset 5Eh

RIRB Size

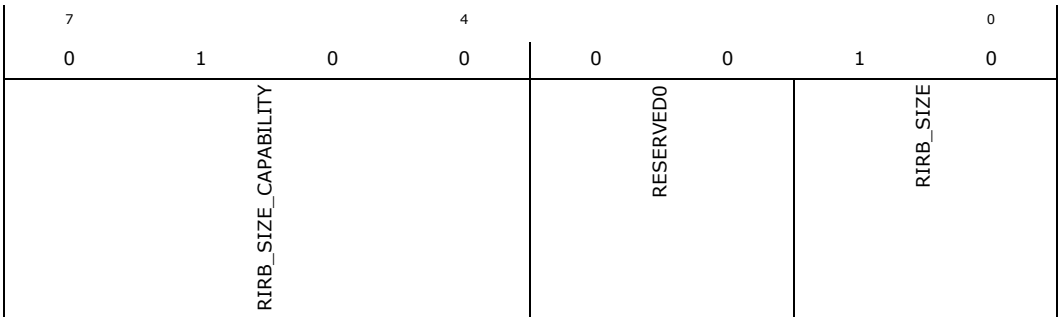
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

RIRBSIZE: [AZLBAR] + 5Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 42h



Bit Range	Default & Access	Description
7:4	4h RO	**RIRB_SIZE_CAPABILITY:** 0100b indicates that the HD Audio controller only supports a RIRB size of 256 RIRB entries 2048B .
3:2	0h RO	**RESERVED0:** reserved
1:0	02h RO	**RIRB_SIZE:** Hardwired to 10b which sets the RIRB size to 256 entries 2048B .

15.6.30 IC—Offset 60h

Immediate Command

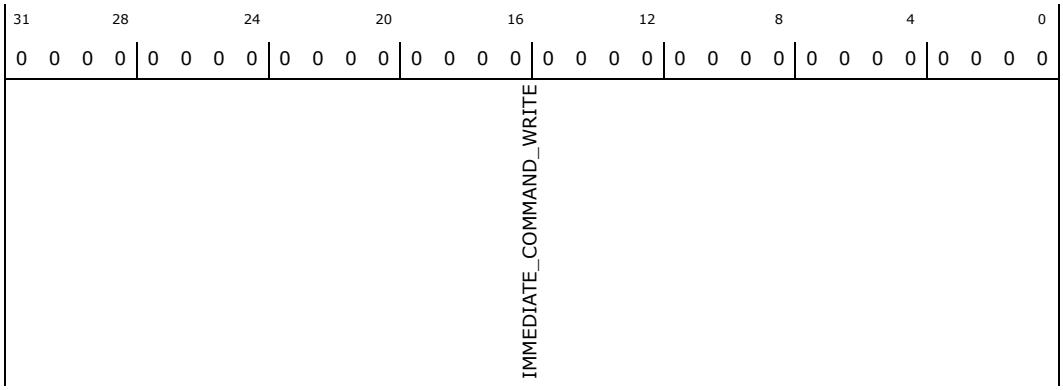
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IC: [AZLBAR] + 60h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**IMMEDIATE_COMMAND_WRITE:** The command to be sent to the codec via the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit.

15.6.31 IR—Offset 64h

Immediate Response

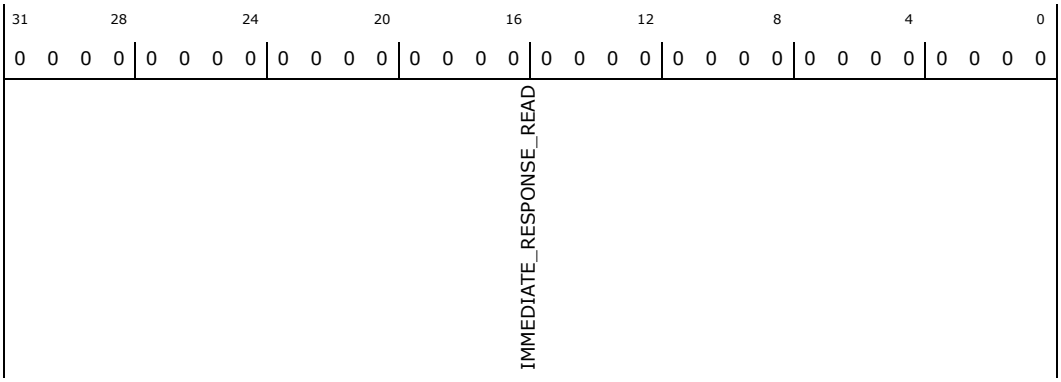
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IR: [AZLBAR] + 64h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**IMMEDIATE_RESPONSE_READ:** This register contains the response received from a codec resulting from a command sent via the Immediate Command mechanism. If multiple codecs responded in the same frame there is no guarantee as to which response will be latched. Therefore broadcast type commands must not be issued via the Immediate Command mechanism.

15.6.32 ICS—Offset 68h

Immediate Command Status

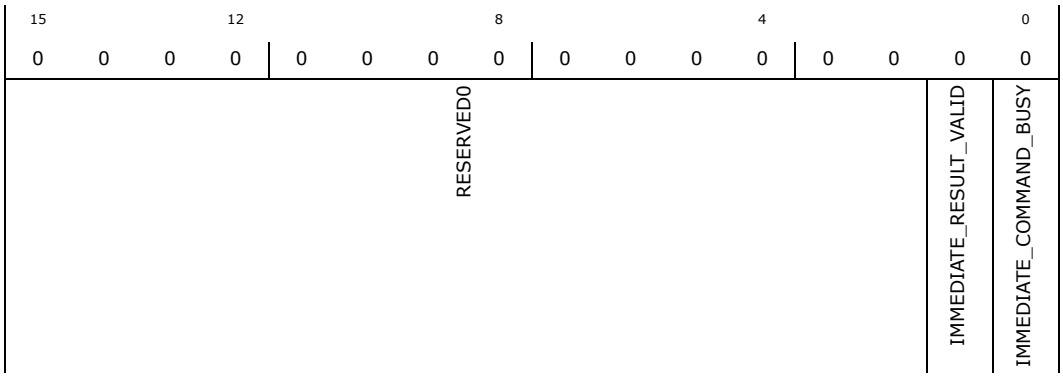
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ICS: [AZLBAR] + 68h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:2	0000h RO	**RESERVED0:** reserved
1	0h RW	**IMMEDIATE_RESULT_VALID:** This bit is set to a 1 by hardware when a new response is latched into the IRR register. This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit by writing a one to it before issuing a new command so that the software may determine when a new response has arrived.
0	0h RW	**IMMEDIATE_COMMAND_BUSY:** When this bit as read as a 0 it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 via software writing a 1 the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register the controller hardware sets the IRV flag and clears the ICB bit back to 0. SW may write this bit to a 0 if the bit fails to return to 0 after a reasonable timeout period. Note that an Immediate Command must not be issued while the CORB RIRB mechanism is operating otherwise the responses conflict. This must be enforced by software.

15.6.33 DPLBASE—Offset 70h

DMA Position Lower Base Address

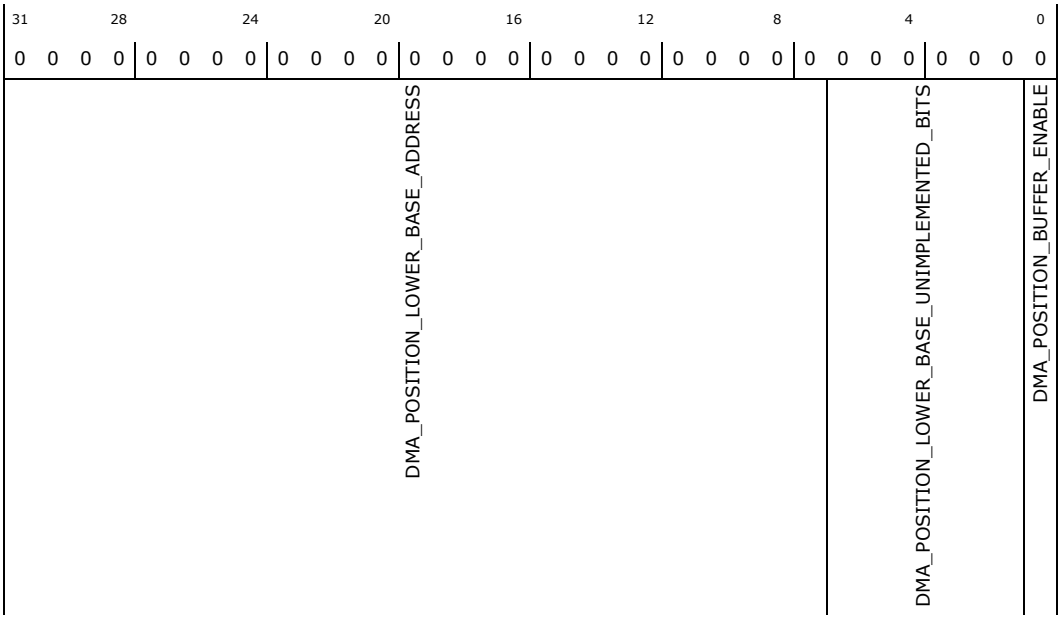
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPLBASE: [AZLBAR] + 70h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**DMA_POSITION_LOWER_BASE_ADDRESS:** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	00h RO	**DMA_POSITION_LOWER_BASE_UNIMPLEMENTED_BITS:** Hardwired to 0 to force 128 byte buffer alignment for cache line write optimizations.
0	0h RW	**DMA_POSITION_BUFFER_ENABLE:** When this bit is set to a 1 the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically typically once frame . Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream s DMA buffer. This has particular relevance in systems which support isochronous transfer the stream positions in the software visible memory buffer must represent stream data which has reached the Global Observation point.

15.6.34 DPUBASE—Offset 74h

DMA position Upper Base Address

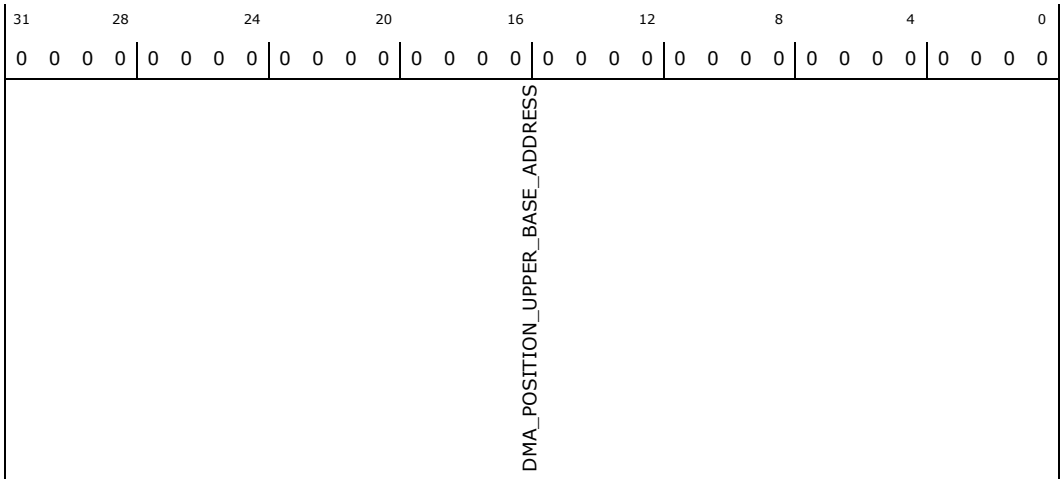
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

DPUBASE: [AZLBAR] + 74h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**DMA_POSITION_UPPER_BASE_ADDRESS:** Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

15.6.35 ISD0CTL_STS—Offset 80h

Input Stream Descriptor 0 Control and status

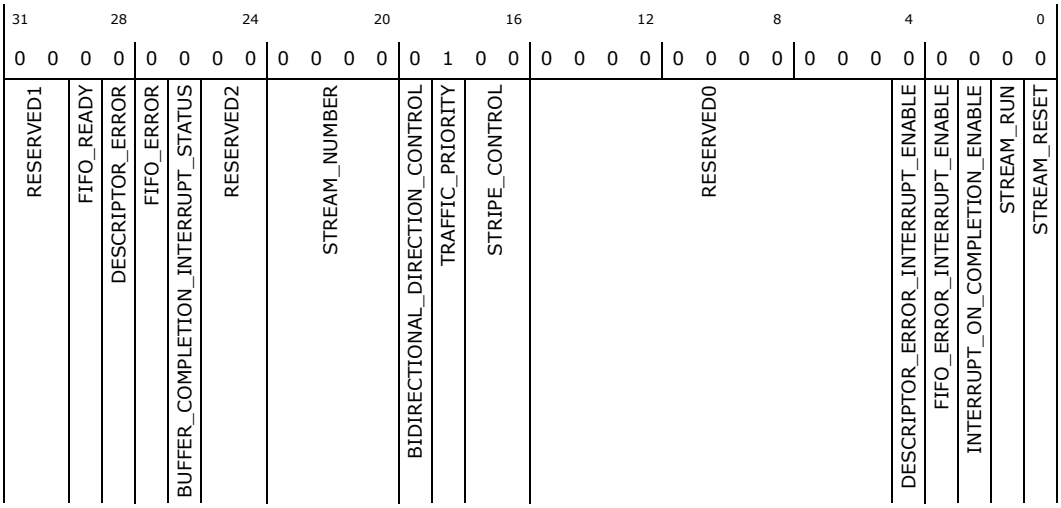
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD0CTL_STS: [AZLBAR] + 80h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h



Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For input streams the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an input stream this indicates a FIFO overrun occurring while the RUN bit is set. When this happens the FIFO pointers don t increment and the incoming data is not written into the FIFO thereby being lost.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved

Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When an input stream is detected on any of the SDIx signals that match this value the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number two different SDIx inputs may not be configured with the same stream number. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** This field is meaningless for input streams.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error overrun for input will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

15.6.36 ISD0LPIB—Offset 84h

Input Stream Descriptor 0 Link Position in Buffer

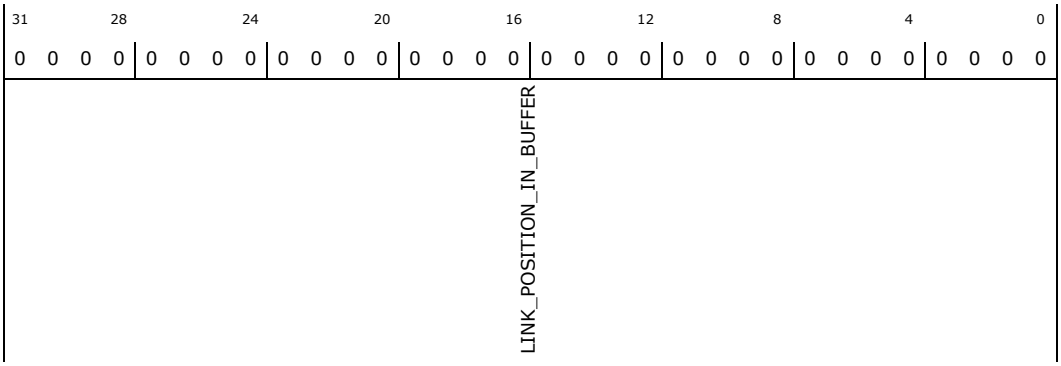
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD0LPIB: [AZLBAR] + 84h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.37 ISD0CBL—Offset 88h

Input Stream Descriptor 0 Cyclic Buffer Length

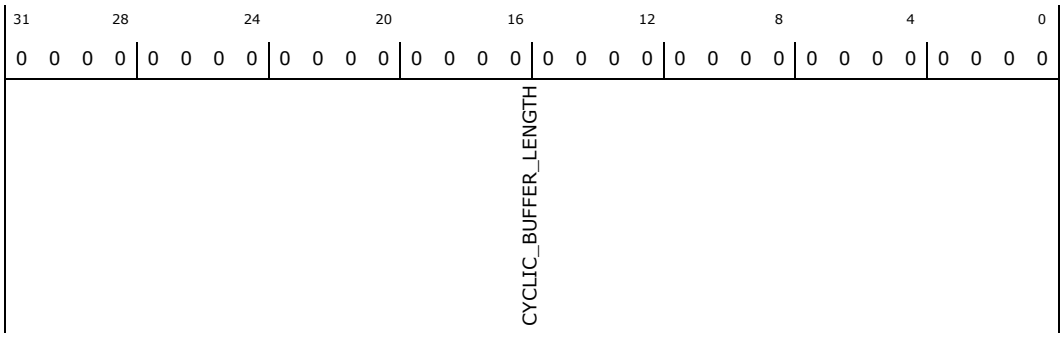
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD0CBL: [AZLBAR] + 88h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

15.6.38 ISD0LVI—Offset 8Ch

Input Stream Descriptor 0 Last Valid Index

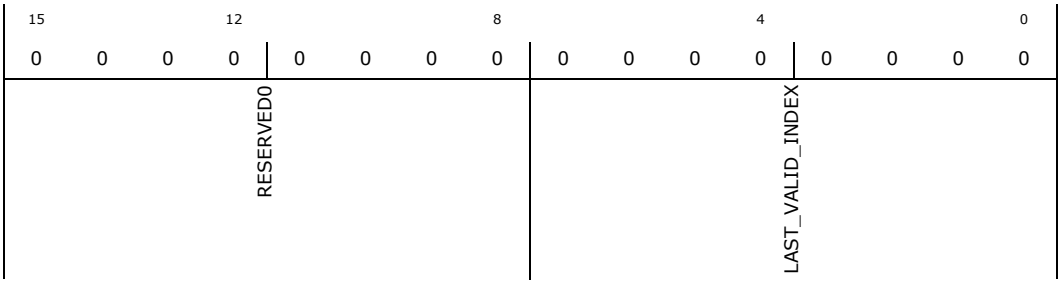
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD0LVI: [AZLBAR] + 8Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1; that is, there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

15.6.39 ISD0FIFOW—Offset 8Eh

Input Stream Descriptor 0 FIFO Eviction Watermark

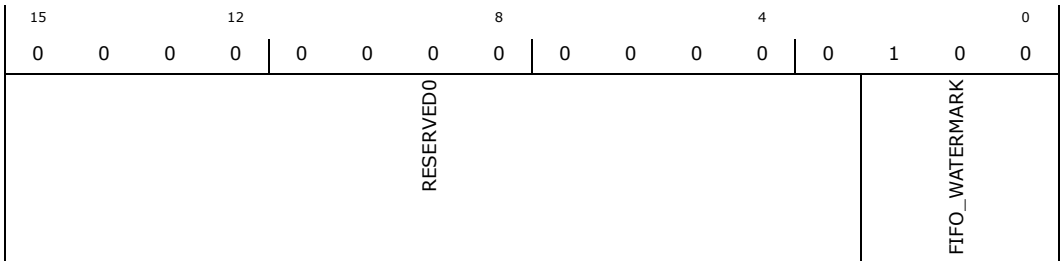
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD0FIFOW: [AZLBAR] + 8Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h



Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes accumulated in the FIFO before the controller will start an eviction of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For input streams the FIFOW value is determined by the EM3.ISRWS SEM3.ISRWS field.

15.6.40 ISD0FIFOS—Offset 90h

Input Stream Descriptor 0 FIFO Size

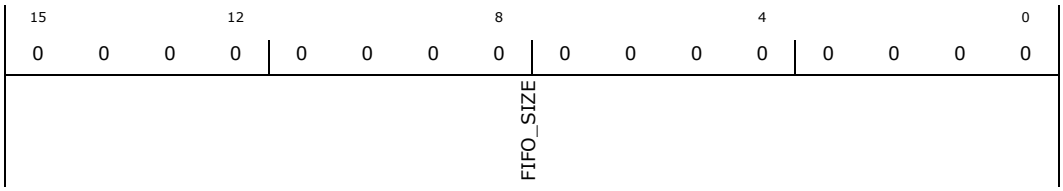
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD0FIFOS: [AZLBAR] + 90h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be received by the controller at one time. This is the maximum number of bytes that may have been received from the link but not yet DMA d into memory and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in ISD0FMT register. As the default value is zero, SW must write to the respective ISD0FMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

15.6.41 ISD0FMT—Offset 92h

Input Stream Descriptor 0 Format

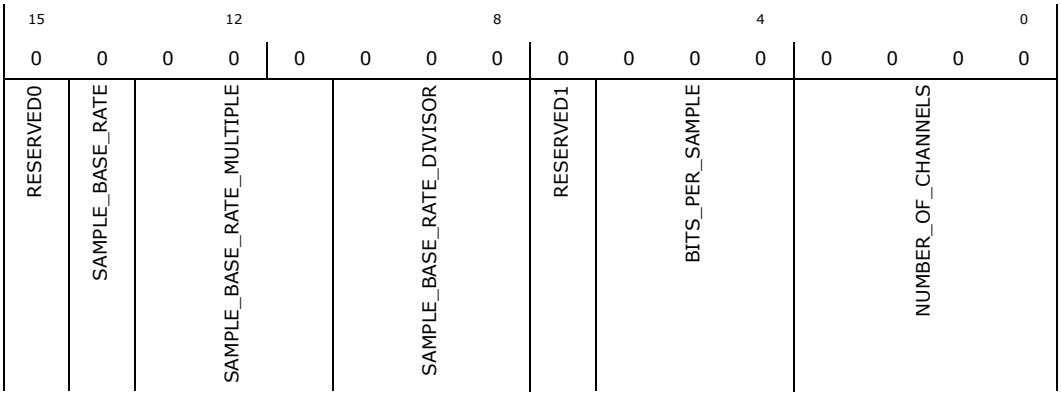
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD0FMT: [AZLBAR] + 92h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

15.6.42 ISD0BDLPLBA—Offset 98h

Input Stream Descriptor 0 Buffer Descriptor List Pointer Lower Base Address

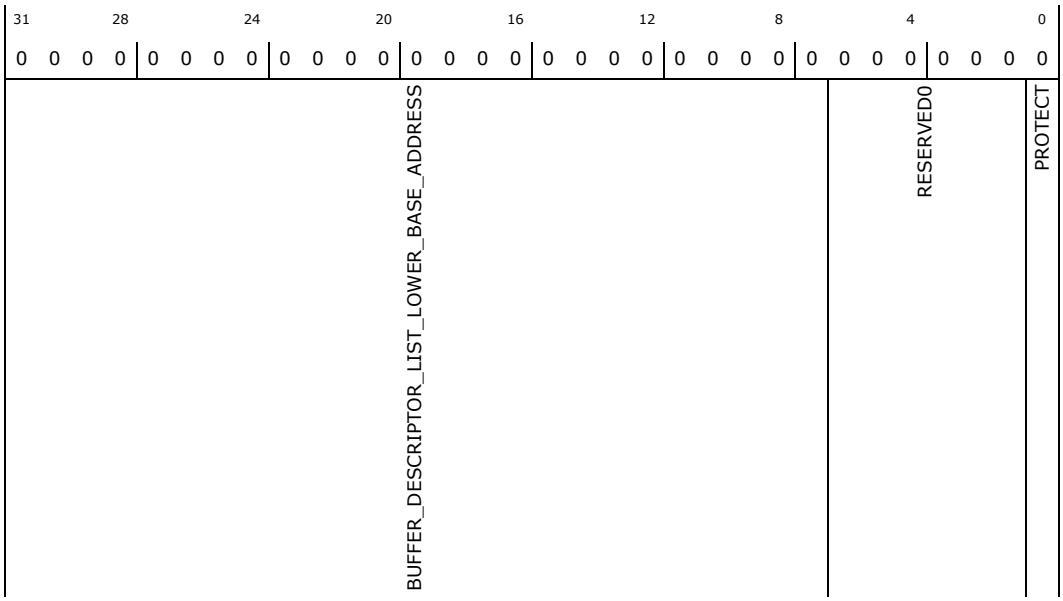
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD0BDLPLBA: [AZLBAR] + 98h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

15.6.43 ISD0BDLPUBA—Offset 9Ch

Input Stream Descriptor 0 Buffer Descriptor List Pointer Upper Base Address

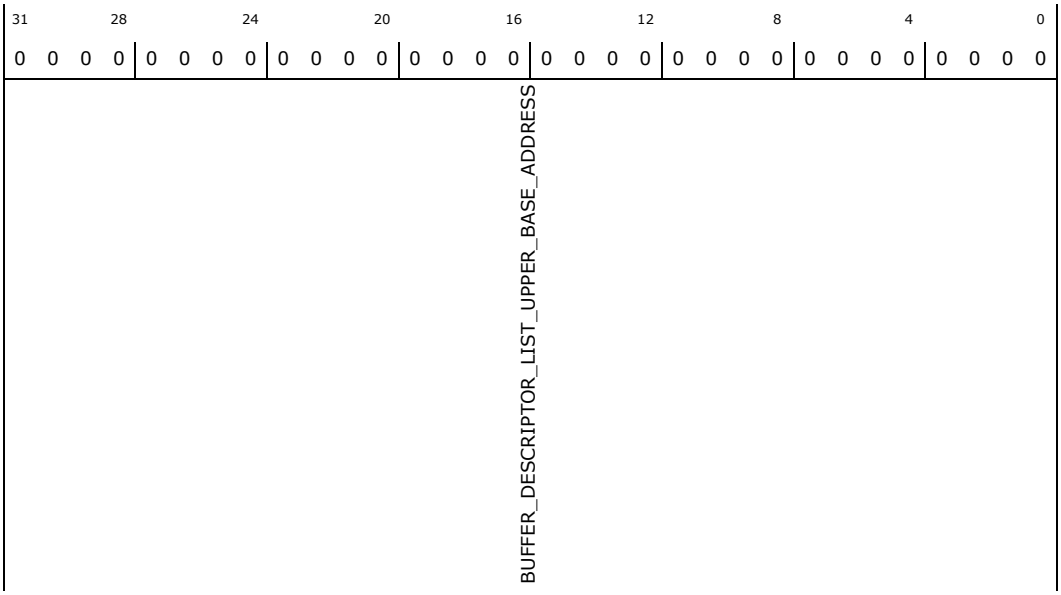
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD0BDLPUBA: [AZLBAR] + 9Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

15.6.44 ISD1CTL_STS—Offset A0h

Input Stream Descriptor 1 Control and status

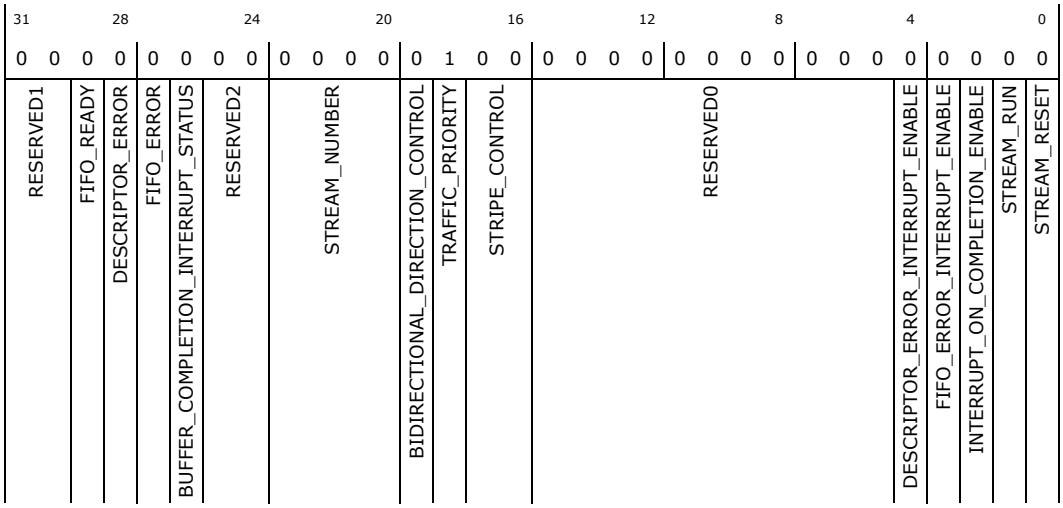
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

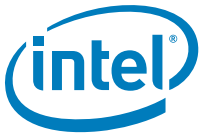
ISD1CTL_STS: [AZLBAR] + A0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h



Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For input streams the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an input stream this indicates a FIFO overrun occurring while the RUN bit is set. When this happens the FIFO pointers don t increment and the incoming data is not written into the FIFO thereby being lost.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved



Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When an input stream is detected on any of the SDIx signals that match this value the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number two different SDIx inputs may not be configured with the same stream number. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** This field is meaningless for input streams.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error overrun for input will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

15.6.45 ISD1LPIB—Offset A4h

Input Stream Descriptor 1 Link Position in Buffer

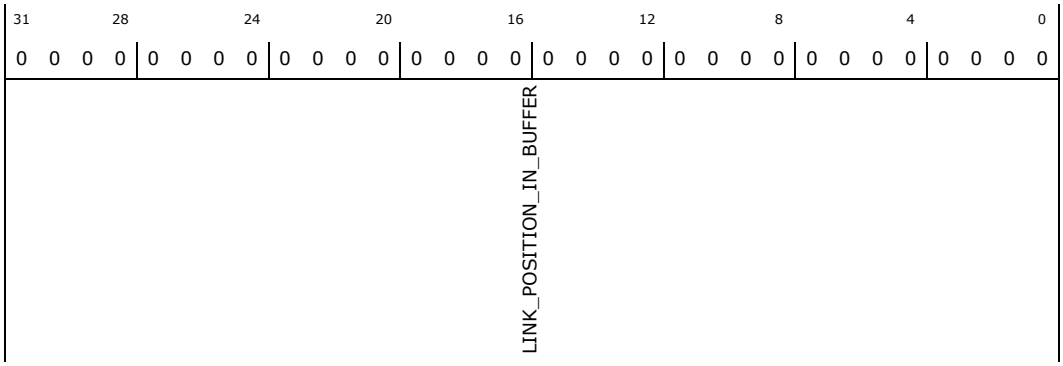
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD1LPIB: [AZLBAR] + A4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.46 ISD1CBL—Offset A8h

Input Stream Descriptor 1 Cyclic Buffer Length

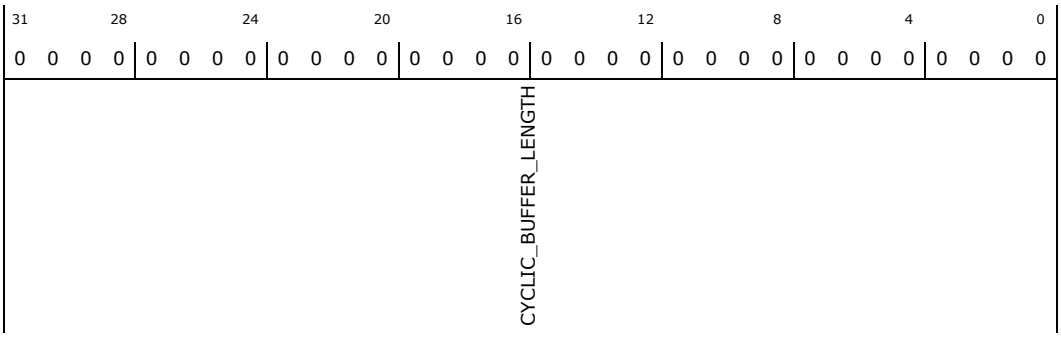
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD1CBL: [AZLBAR] + A8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

15.6.47 ISD1LVI—Offset ACh

Input Stream Descriptor 1 Last Valid Index

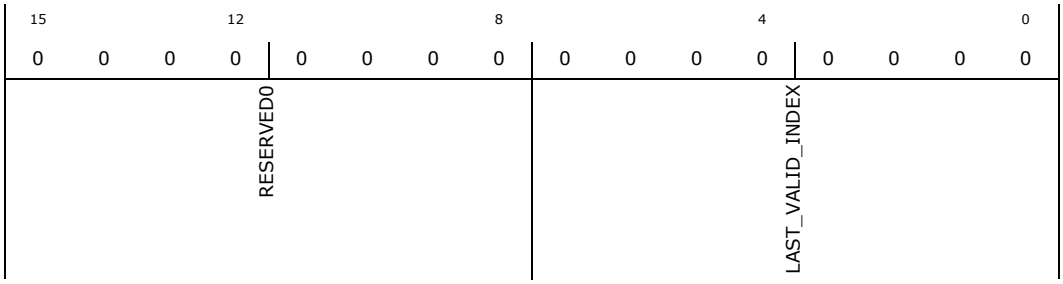
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD1LVI: [AZLBAR] + ACh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1; that is, there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

15.6.48 ISD1FIFOW—Offset AEh

Input Stream Descriptor 1 FIFO Eviction Watermark

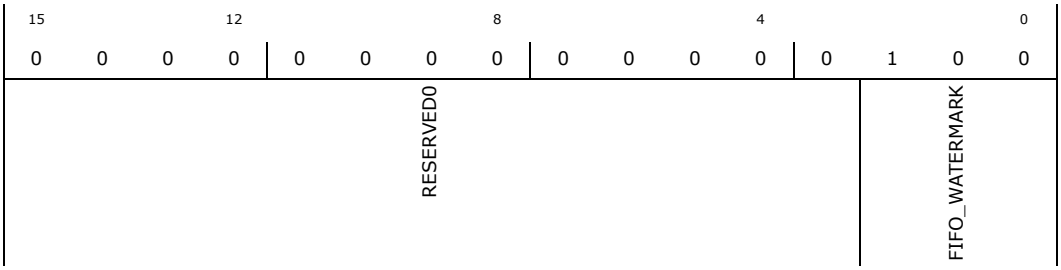
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD1FIFOW: [AZLBAR] + AEh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h



Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes accumulated in the FIFO before the controller will start an eviction of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For input streams the FIFOW value is determined by the EM3.ISRWS SEM3.ISRWS field.

15.6.49 ISD1FIFOS—Offset B0h

Input Stream Descriptor 1 FIFO Size

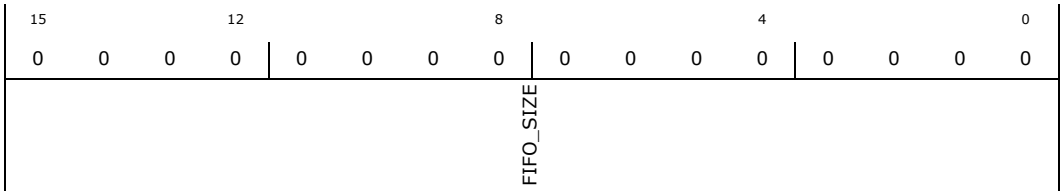
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD1FIFOS: [AZLBAR] + B0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be received by the controller at one time. This is the maximum number of bytes that may have been received from the link but not yet DMA d into memory and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in ISD1FMT register. As the default value is zero, SW must write to the respective ISD1FMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

15.6.50 ISD1FMT—Offset B2h

Input Stream Descriptor 1 Format

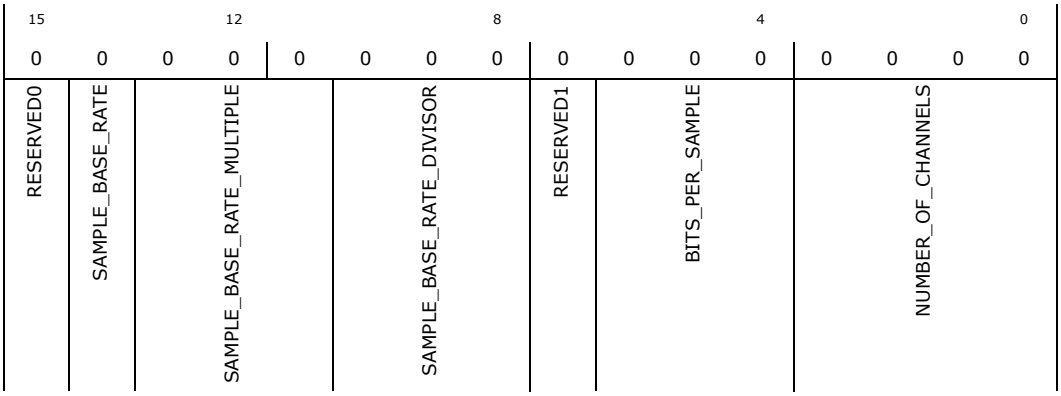
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD1FMT: [AZLBAR] + B2h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

15.6.51 ISD1BDLPLBA—Offset B8h

Input Stream Descriptor 1 Buffer Descriptor List Pointer Lower Base Address

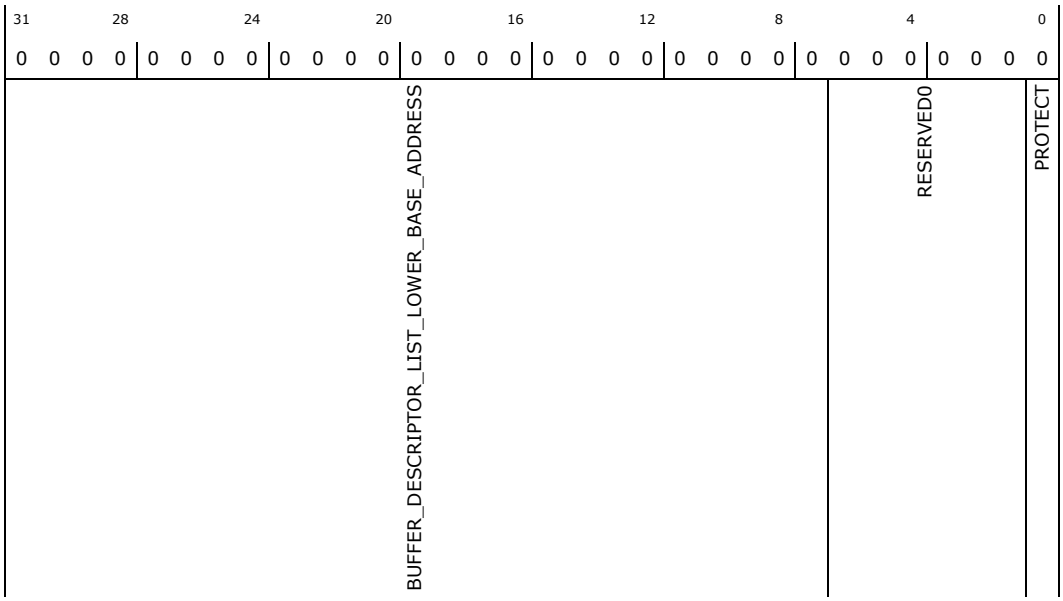
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD1BDLPLBA: [AZLBAR] + B8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

15.6.52 ISD1BDLPUBA—Offset BCh

Input Stream Descriptor 1 Buffer Descriptor List Pointer Upper Base Address

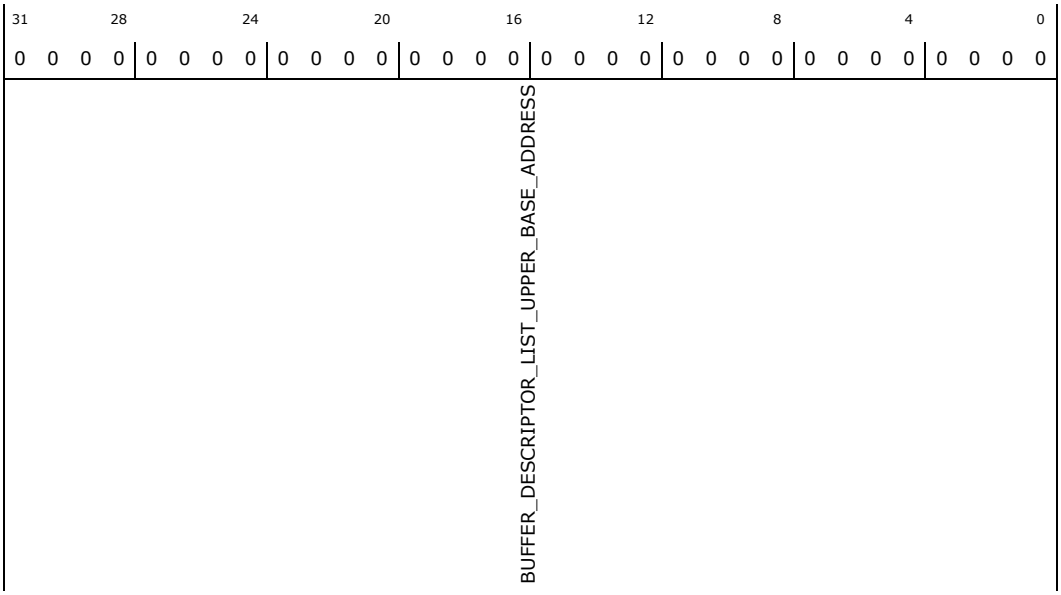
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD1BDLPUBA: [AZLBAR] + BCh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

15.6.53 ISD2CTL_STS—Offset C0h

Input Stream Descriptor 2 Control and status

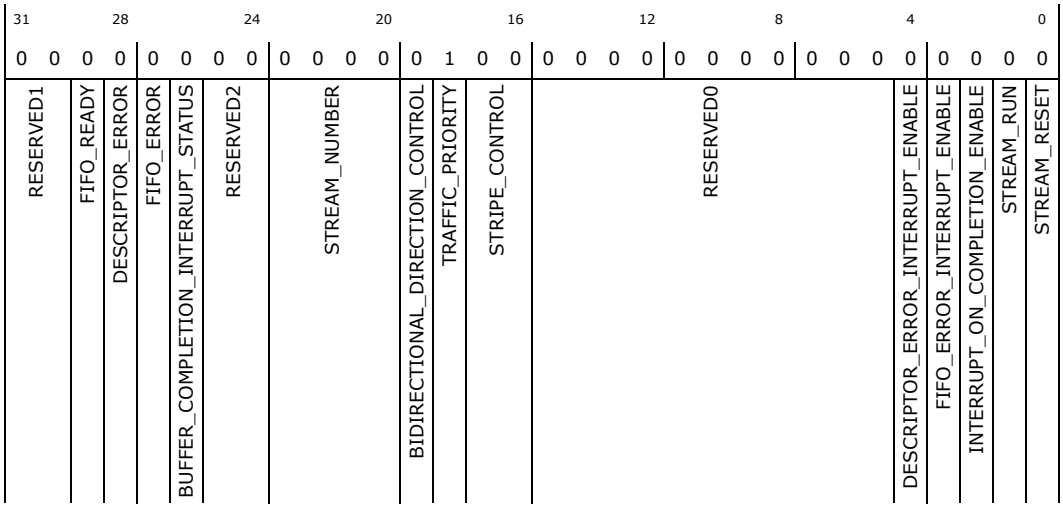
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

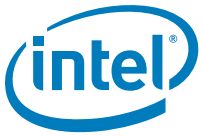
ISD2CTL_STS: [AZLBAR] + C0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h



Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For input streams the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an input stream this indicates a FIFO overrun occurring while the RUN bit is set. When this happens the FIFO pointers don t increment and the incoming data is not written into the FIFO thereby being lost.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved



Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When an input stream is detected on any of the SDIx signals that match this value the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number two different SDIx inputs may not be configured with the same stream number. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** This field is meaningless for input streams.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error overrun for input will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

15.6.54 ISD2LPIB—Offset C4h

Input Stream Descriptor 2 Link Position in Buffer

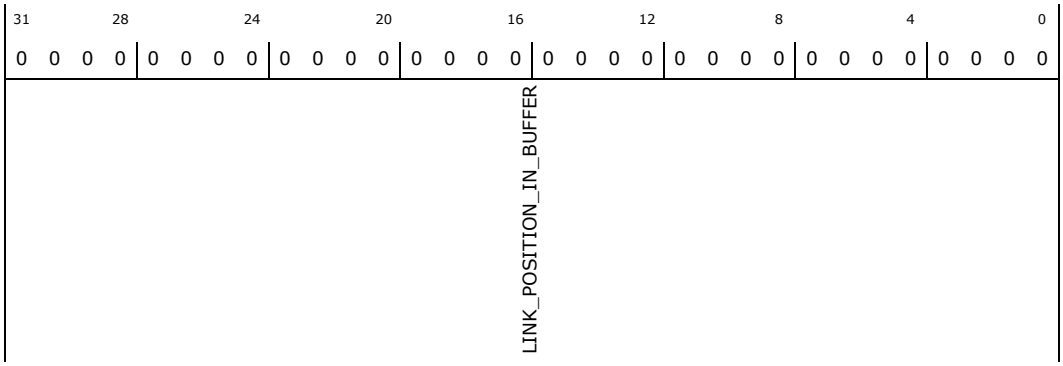
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD2LPIB: [AZLBAR] + C4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.55 ISD2CBL—Offset C8h

Input Stream Descriptor 2 Cyclic Buffer Length

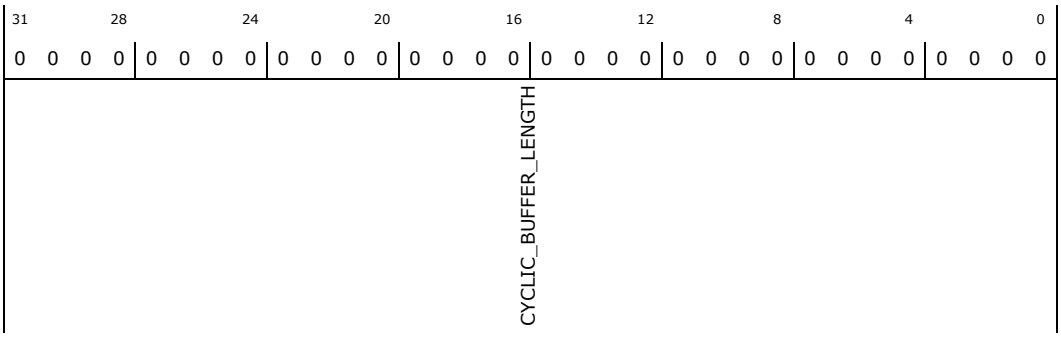
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD2CBL: [AZLBAR] + C8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

15.6.56 ISD2LVI—Offset CCh

Input Stream Descriptor 2 Last Valid Index

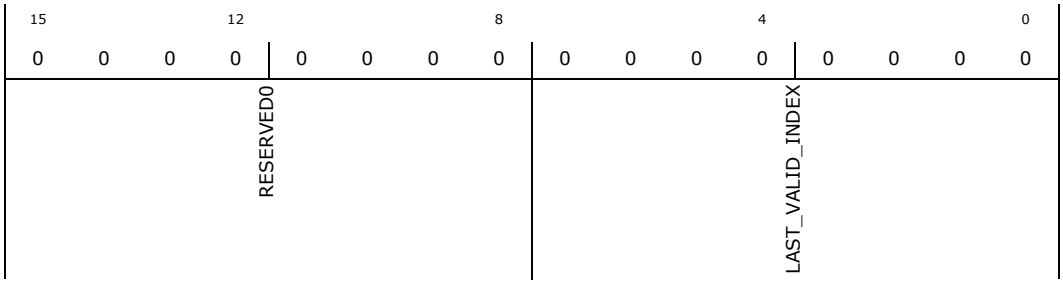
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD2LVI: [AZLBAR] + CCh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, that is, there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

15.6.57 ISD2FIFOW—Offset CEh

Input Stream Descriptor 2 FIFO Eviction Watermark

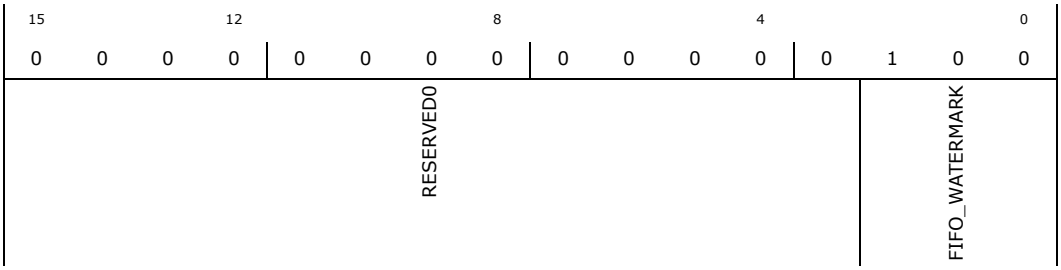
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD2FIFOW: [AZLBAR] + CEh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h



Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes accumulated in the FIFO before the controller will start an eviction of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For input streams the FIFOW value is determined by the EM3.ISRWS SEM3.ISRWS field.

15.6.58 ISD2FIFOS—Offset D0h

Input Stream Descriptor 2 FIFO Size

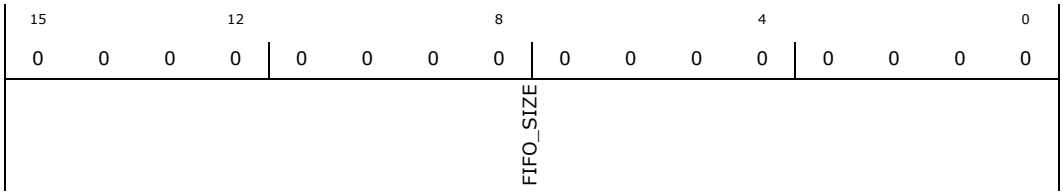
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD2FIFOS: [AZLBAR] + D0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be revicted by the controller at one time. This is the maximum number of bytes that may have been received from the link but not yet DMA d into memory and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in ISD2FMT register. As the default value is zero, SW must write to the respective ISD2FMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

15.6.59 ISD2FMT—Offset D2h

Input Stream Descriptor 2 Format

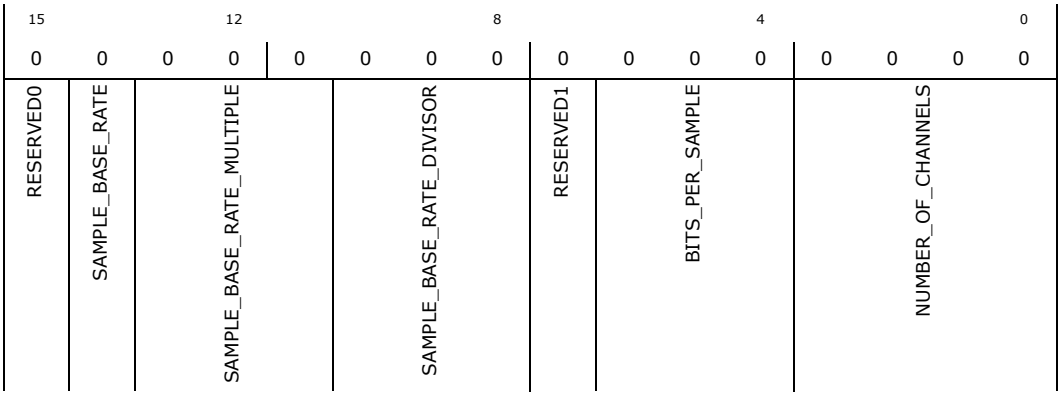
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD2FMT: [AZLBAR] + D2h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

15.6.60 ISD2BDLPLBA—Offset D8h

Input Stream Descriptor 2 Buffer Descriptor List Pointer Lower Base Address

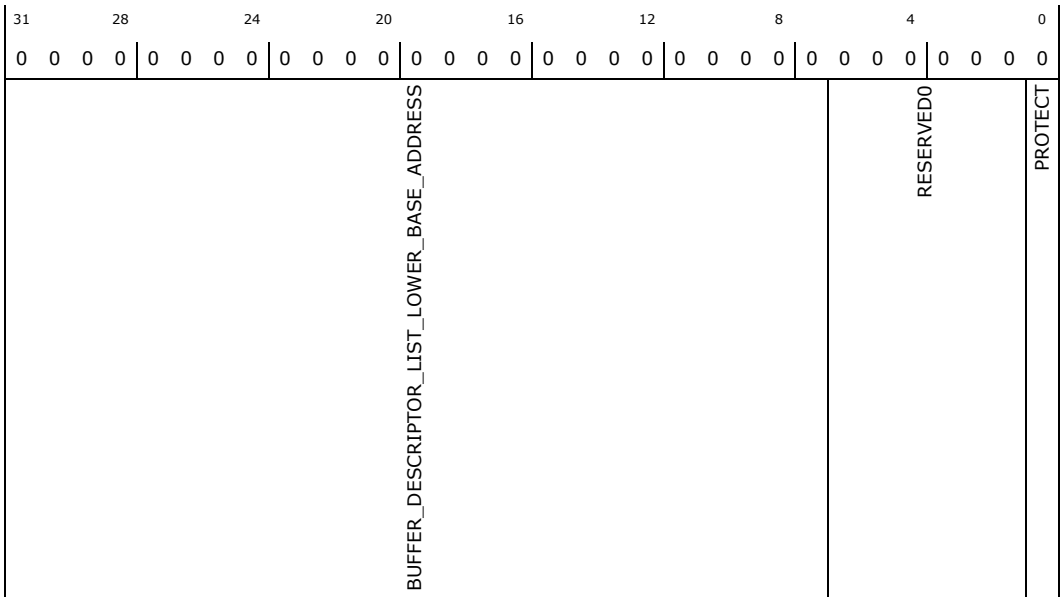
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD2BDLPLBA: [AZLBAR] + D8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

15.6.61 ISD2BDLPUBA—Offset DCh

Input Stream Descriptor 2 Buffer Descriptor List Pointer Upper Base Address

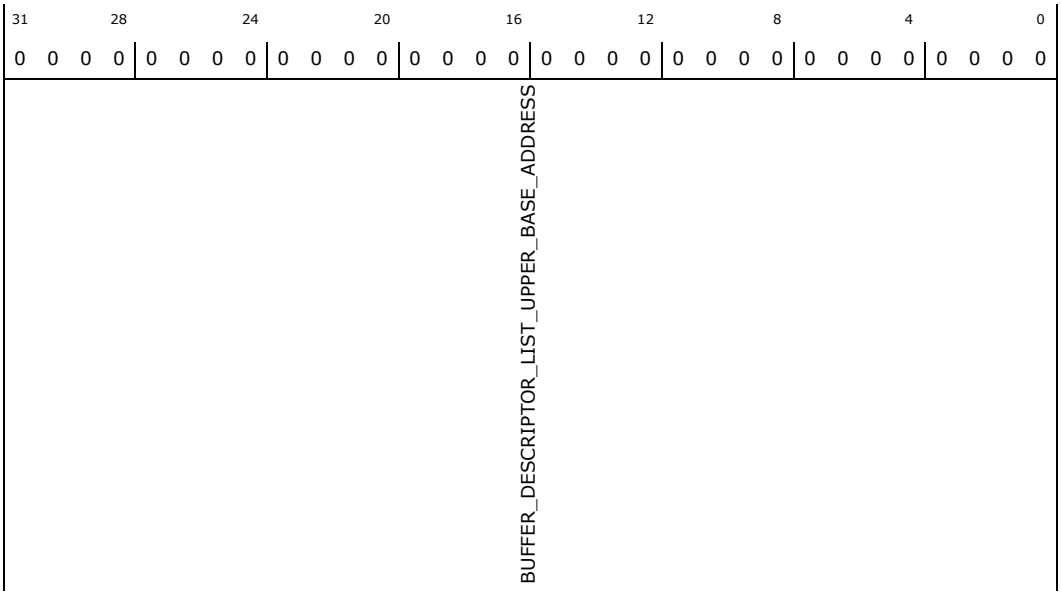
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD2BDLPUBA: [AZLBAR] + DCh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

15.6.62 ISD3CTL_STS—Offset E0h

Input Stream Descriptor 3 Control and status

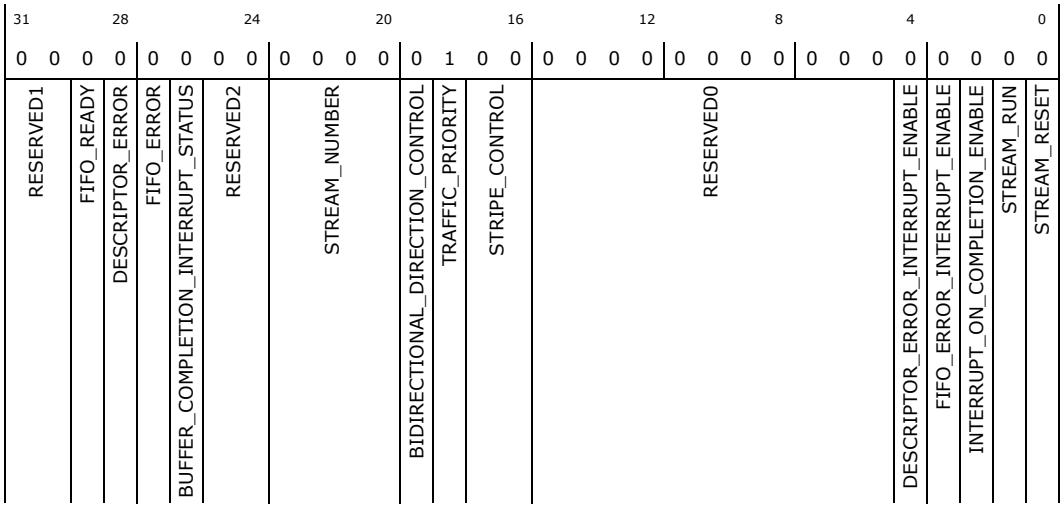
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

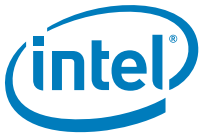
ISD3CTL_STS: [AZLBAR] + E0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h



Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For input streams the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an input stream this indicates a FIFO overrun occurring while the RUN bit is set. When this happens the FIFO pointers don t increment and the incoming data is not written into the FIFO thereby being lost.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved



Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When an input stream is detected on any of the SDIx signals that match this value the data samples are loaded into the FIFO associated with this descriptor. Note that while a single SDIx input may contain data from more than one stream number two different SDIx inputs may not be configured with the same stream number. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** This field is meaningless for input streams.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error overrun for input will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. When cleared to 0 the DMA engine associated with this input stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

15.6.63 ISD3LPIB—Offset E4h

Input Stream Descriptor 3 Link Position in Buffer

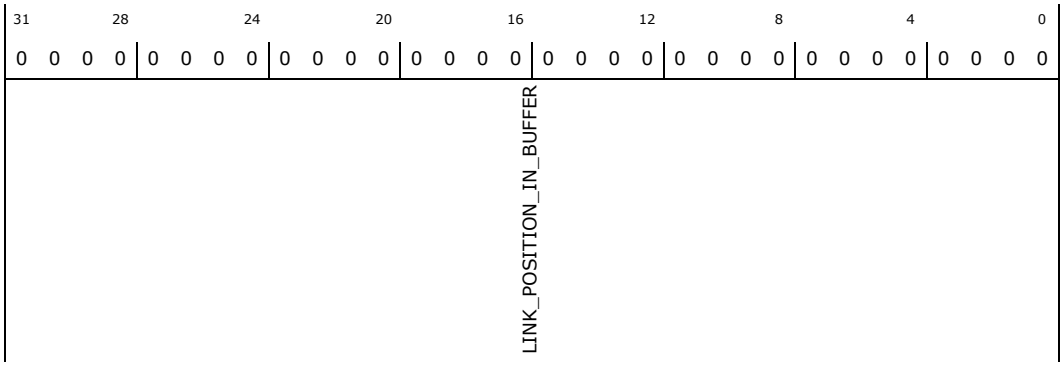
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD3LPIB: [AZLBAR] + E4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.64 ISD3CBL—Offset E8h

Input Stream Descriptor 3 Cyclic Buffer Length

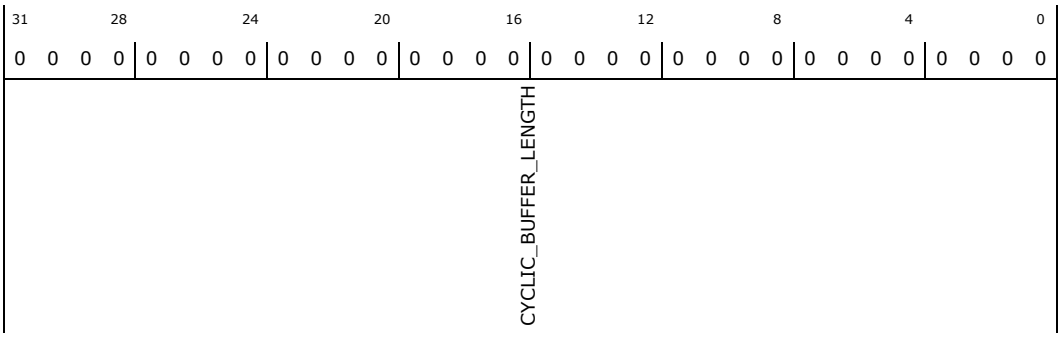
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD3CBL: [AZLBAR] + E8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

15.6.65 ISD3LVI—Offset ECh

Input Stream Descriptor 3 Last Valid Index

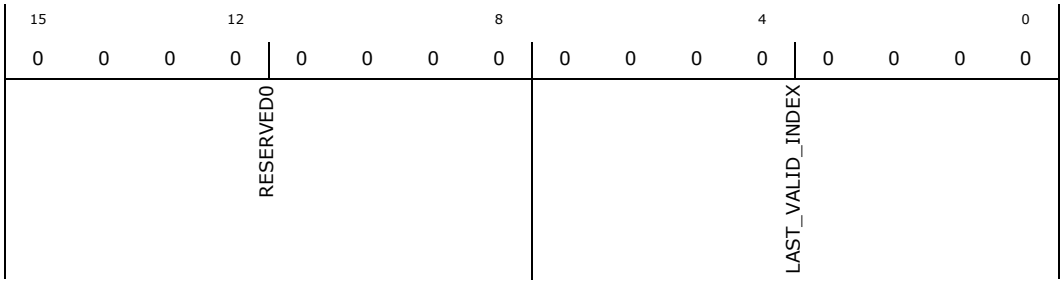
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD3LVI: [AZLBAR] + ECh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, that is, there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

15.6.66 ISD3FIFOW—Offset EEh

Input Stream Descriptor 3 FIFO Eviction Watermark

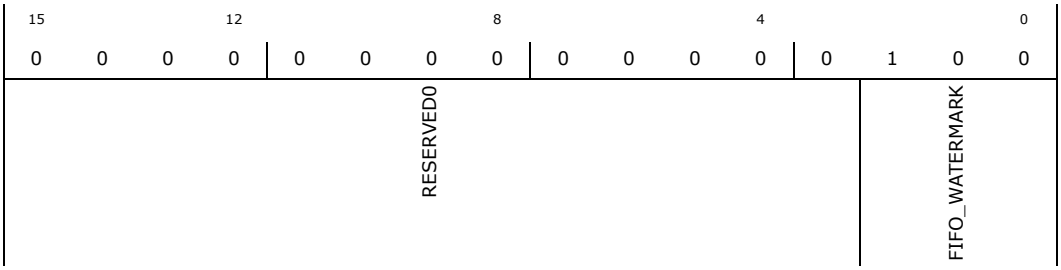
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD3FIFOW: [AZLBAR] + EEh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h



Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes accumulated in the FIFO before the controller will start an eviction of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For input streams the FIFOW value is determined by the EM3.ISRWS SEM3.ISRWS field.

15.6.67 ISD3FIFOS—Offset F0h

Input Stream Descriptor 3 FIFO Size

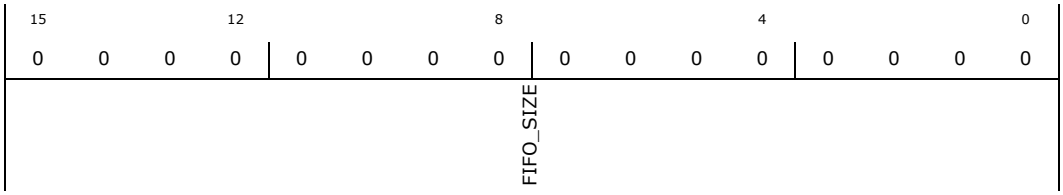
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD3FIFOS: [AZLBAR] + F0h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be revicted by the controller at one time. This is the maximum number of bytes that may have been received from the link but not yet DMA d into memory and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in ISD3FMT register. As the default value is zero, SW must write to the respective ISD3FMT register to kick of the FIFO size calculation, and read back to find out the HW allocated FIFO size.

15.6.68 ISD3FMT—Offset F2h

Input Stream Descriptor 3 Format

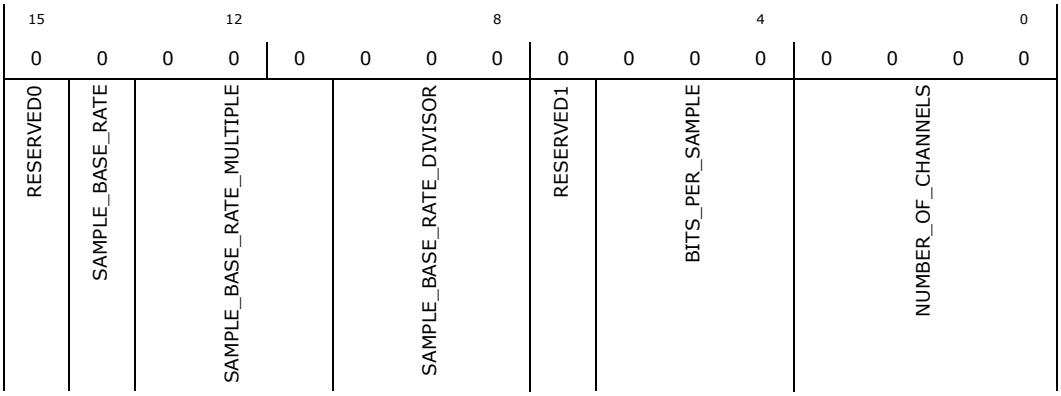
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

ISD3FMT: [AZLBAR] + F2h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** 0 48 kHz 1 44.1 kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

15.6.69 ISD3BDLPLBA—Offset F8h

Input Stream Descriptor 3 Buffer Descriptor List Pointer Lower Base Address

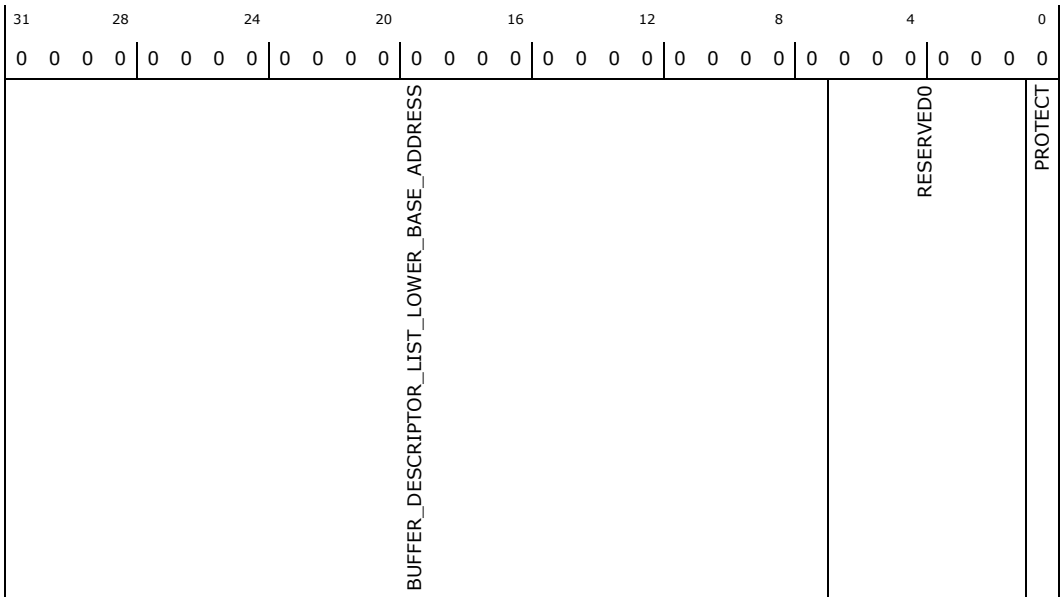
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD3BDLPLBA: [AZLBAR] + F8h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

15.6.70 ISD3BDLPUBA—Offset FCh

Input Stream Descriptor 3 Buffer Descriptor List Pointer Upper Base Address

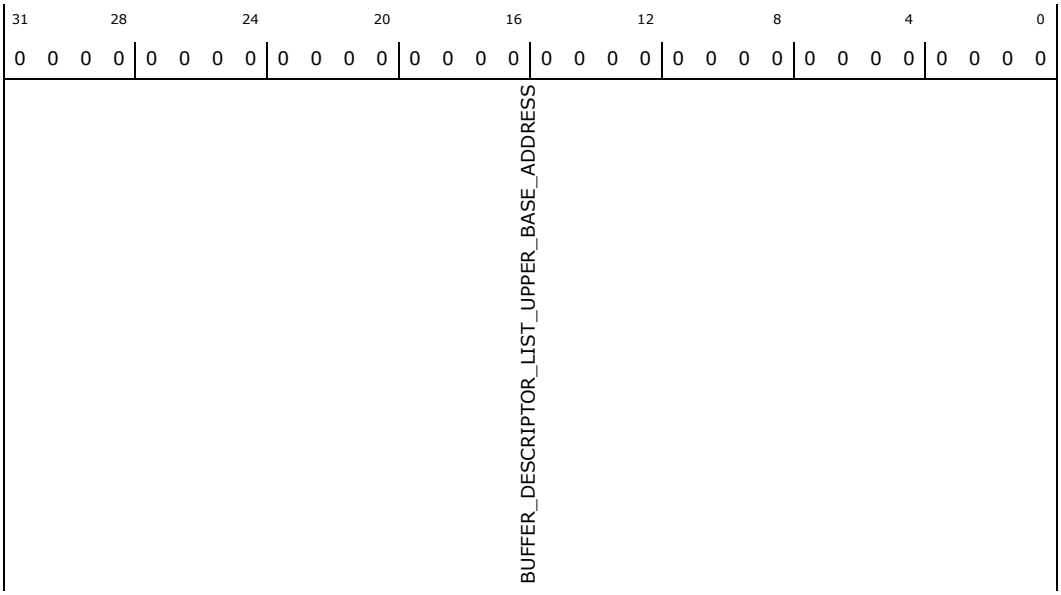
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD3BDLPUBA: [AZLBAR] + FCh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

15.6.71 OSD0CTL_STS—Offset 100h

Output Stream Descriptor 0 Control and status

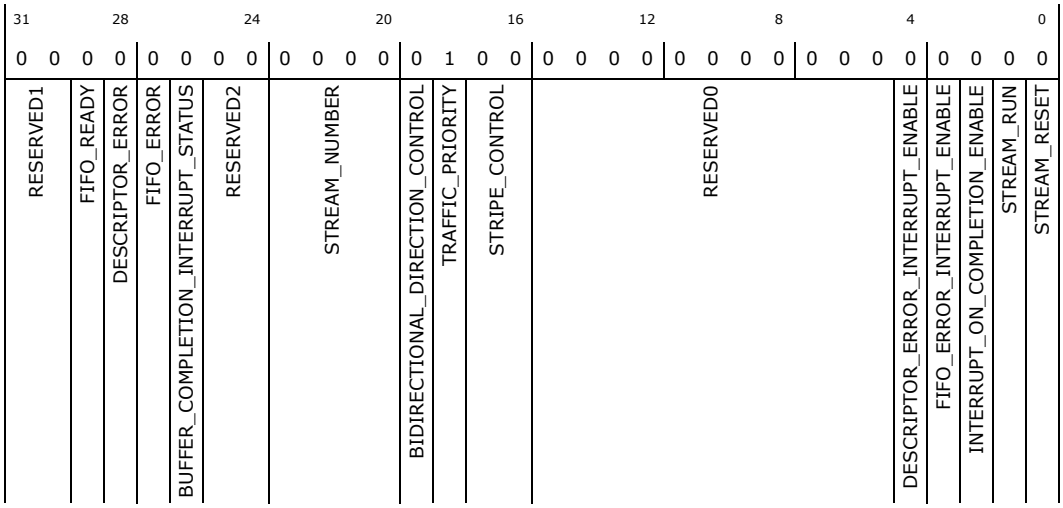
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

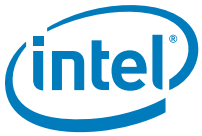
OSD0CTL_STS: [AZLBAR] + 100h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h



Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For output streams the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an output stream this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved



Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link it will have this stream number encoded on the SYNC signal. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in the HD Audio controller. Therefore it is hardwired to 0 s.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error under run for output will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

15.6.72 OSD0LPIB—Offset 104h

Output Stream Descriptor 0 Link Position in Buffer

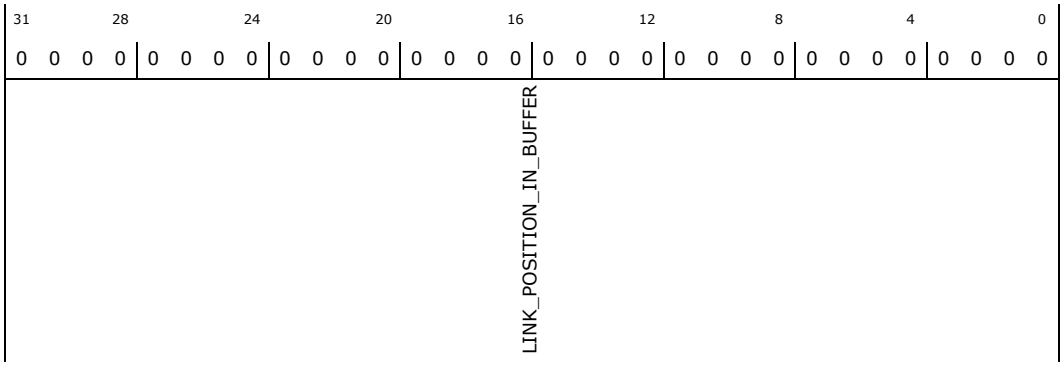
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD0LPIB: [AZLBAR] + 104h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.73 OSD0CBL—Offset 108h

Output Stream Descriptor 0 Cyclic Buffer Length

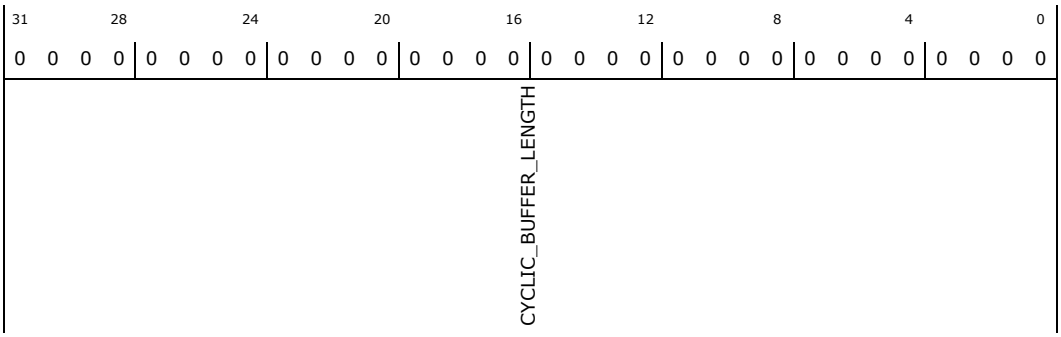
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD0CBL: [AZLBAR] + 108h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

15.6.74 OSD0LVI—Offset 10Ch

Output Stream Descriptor 0 Last Valid Index

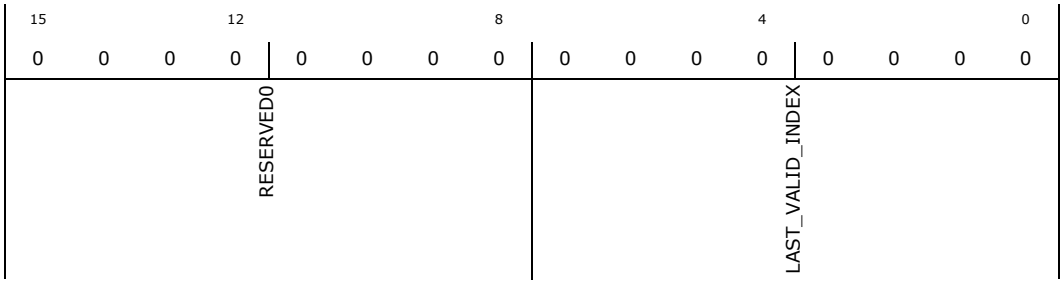
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD0LVI: [AZLBAR] + 10Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, that is, there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

15.6.75 OSD0FIFOW—Offset 10Eh

Output Stream Descriptor 0 FIFO Fetch Watermark

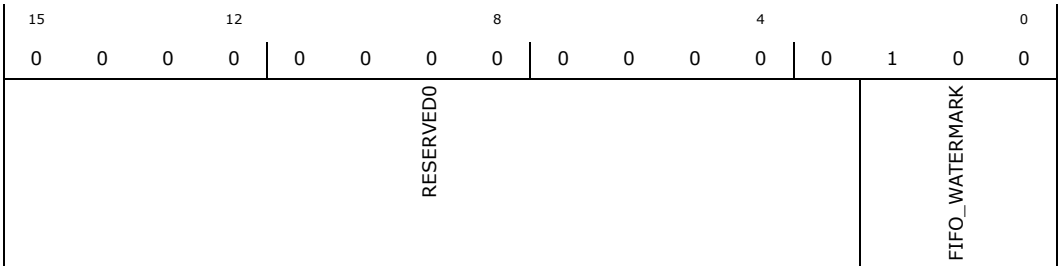
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD0FIFOW: [AZLBAR] + 10Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h



Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes free in the FIFO before the controller will start a fetch of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For output streams the FIFOW value is determined by the EM4.OSRWS SEM4.OSRWS field.

15.6.76 OSD0FIFOS—Offset 110h

Output Stream Descriptor 0 FIFO Size

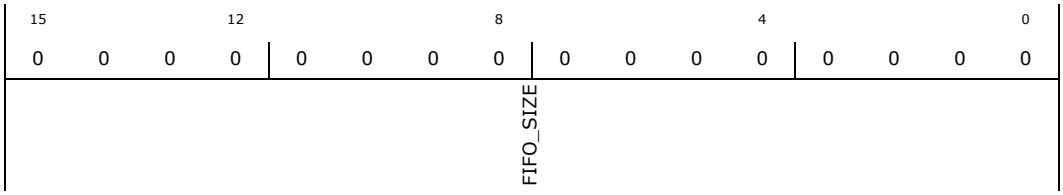
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD0FIFOS: [AZLBAR] + 110h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA d into memory but not yet transmitted on the link and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in OSD0FMT register. As the default value is zero, SW must write to the OSD0FMT register to kick of the FIFO size calculation and read back to find out the HW allocated FIFO size.

15.6.77 OSD0FMT—Offset 112h

Output Stream Descriptor 0 Format

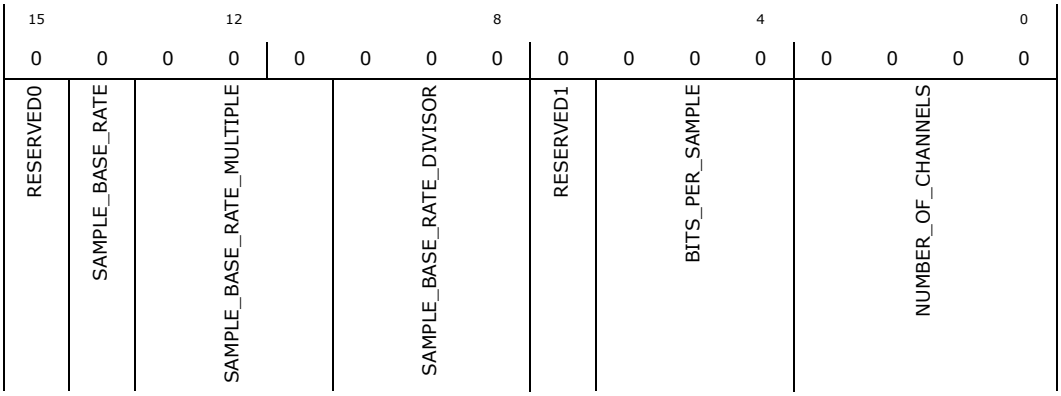
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD0FMT: [AZLBAR] + 112h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

15.6.78 OSD0BDLPLBA—Offset 118h

Output Stream Descriptor 0 Buffer Descriptor List Pointer Lower Base Address

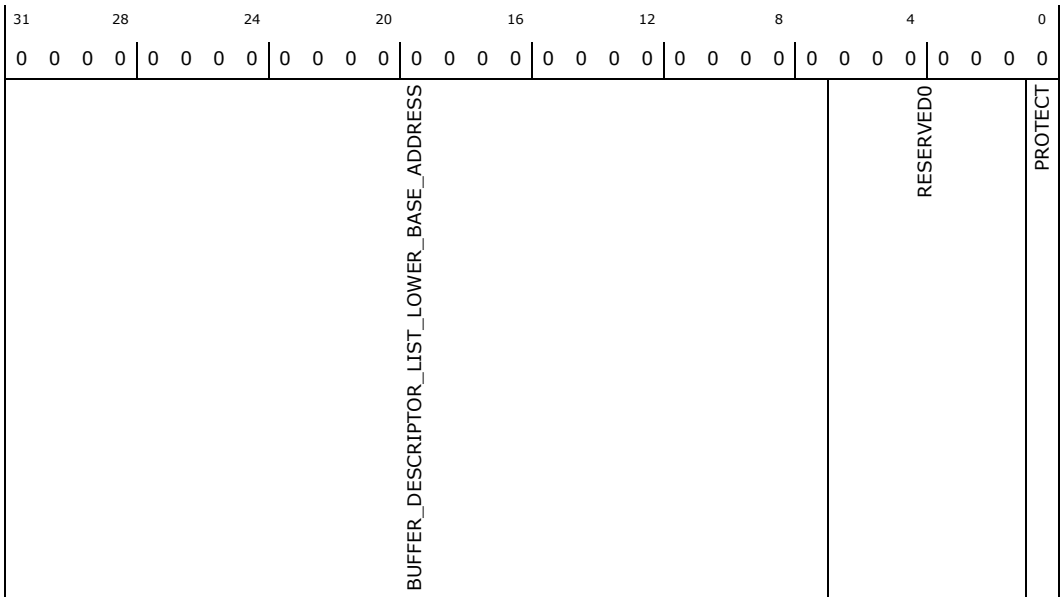
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD0BDLPLBA: [AZLBAR] + 118h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

15.6.79 OSD0BDLPUBA—Offset 11Ch

Output Stream Descriptor 0 Buffer Descriptor List Pointer Upper Base Address

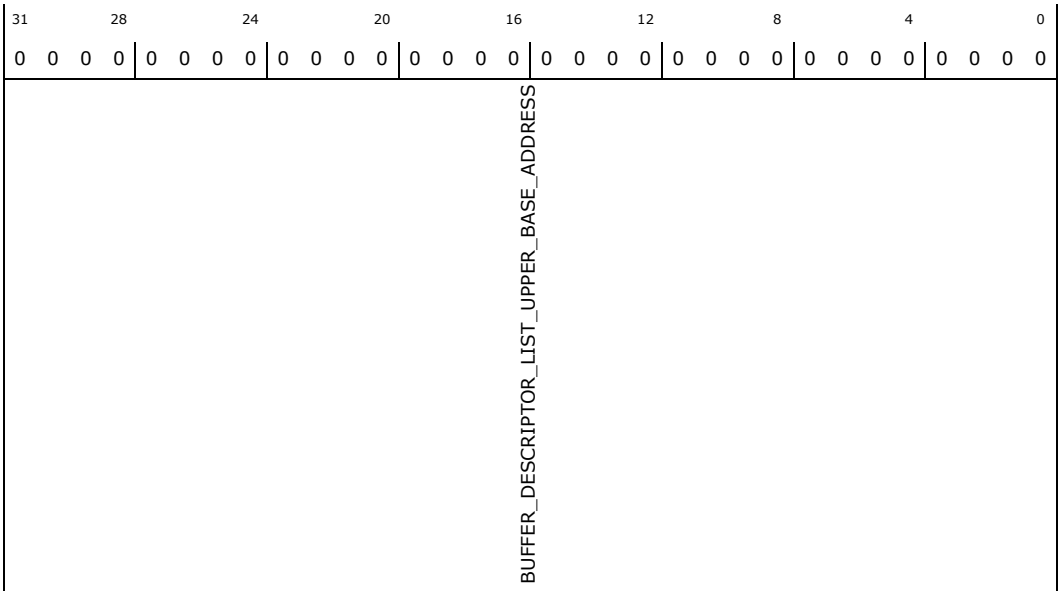
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD0BDLPUBA: [AZLBAR] + 11Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

15.6.80 OSD1CTL_STS—Offset 120h

Output Stream Descriptor 1 Control and status

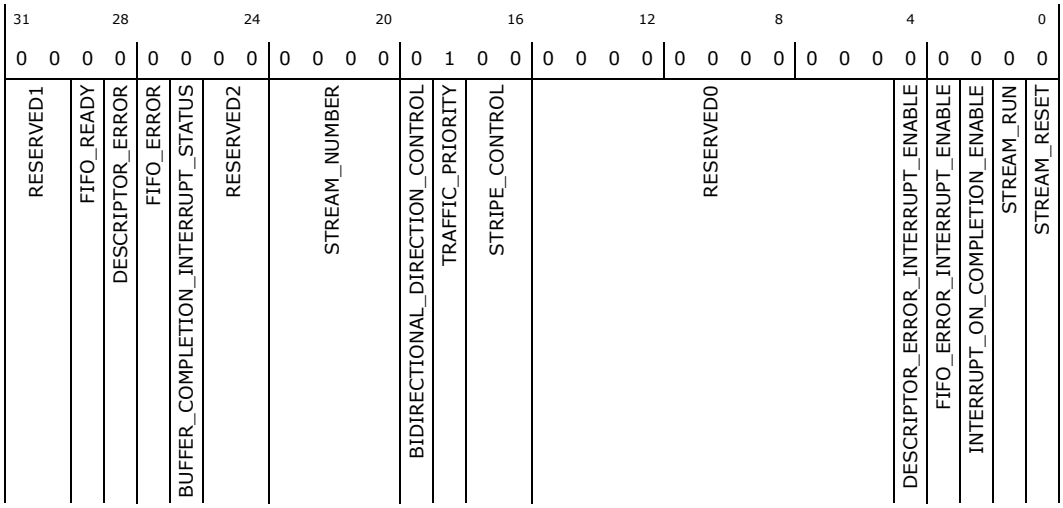
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

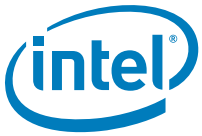
OSD1CTL_STS: [AZLBAR] + 120h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h



Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For output streams the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an output stream this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved



Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link it will have this stream number encoded on the SYNC signal. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in the HD Audio controller. Therefore it is hardwired to 0 s.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error under run for output will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

15.6.81 OSD1LPIB—Offset 124h

Output Stream Descriptor 1 Link Position in Buffer

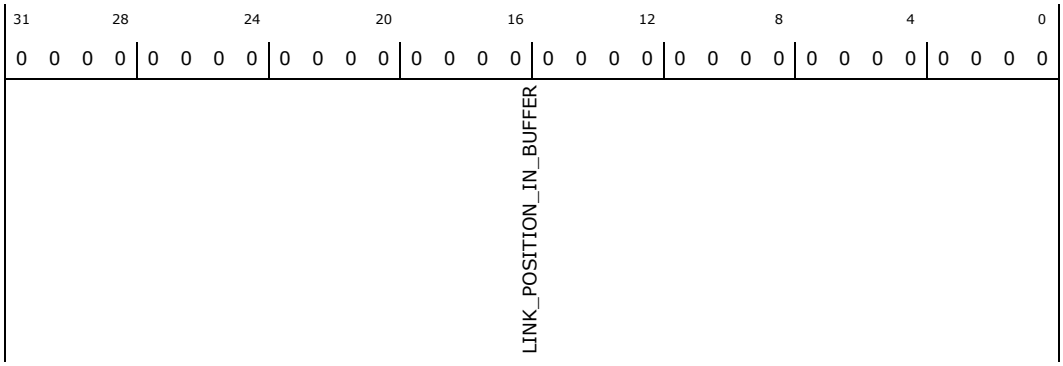
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD1LPIB: [AZLBAR] + 124h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.82 OSD1CBL—Offset 128h

Output Stream Descriptor 1 Cyclic Buffer Length

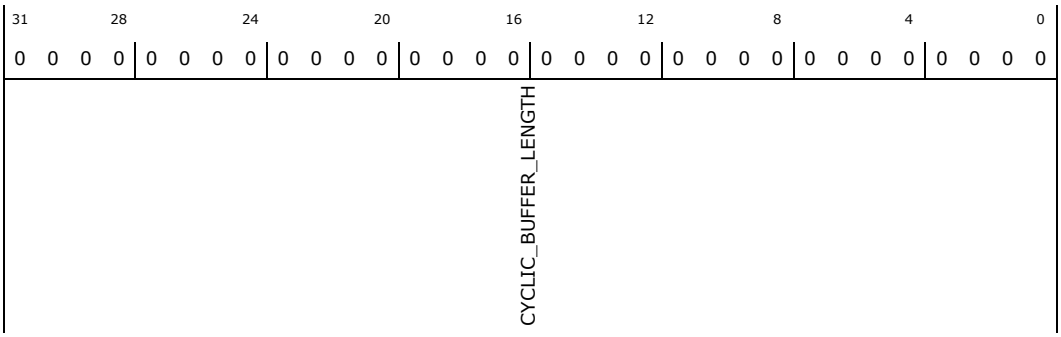
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD1CBL: [AZLBAR] + 128h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

15.6.83 OSD1LVI—Offset 12Ch

Output Stream Descriptor 1 Last Valid Index

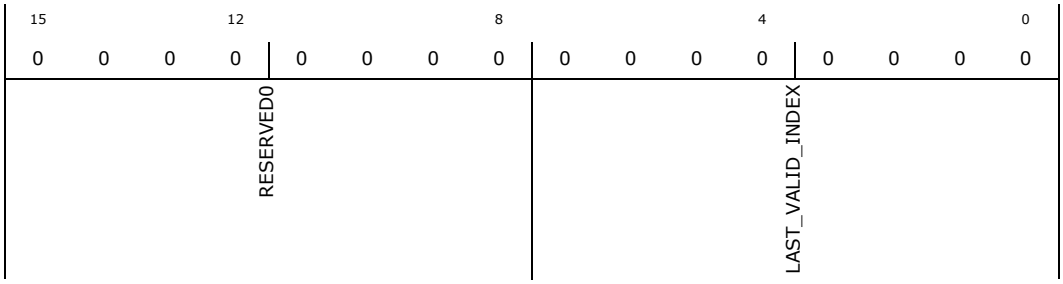
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD1LVI: [AZLBAR] + 12Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, that is, there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

15.6.84 OSD1FIFOW—Offset 12Eh

Output Stream Descriptor 1 FIFO Fetch Watermark

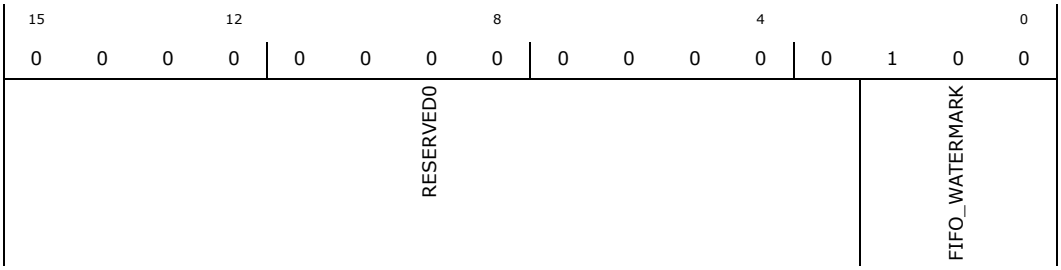
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD1FIFOW: [AZLBAR] + 12Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h



Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes free in the FIFO before the controller will start a fetch of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For output streams the FIFOW value is determined by the EM4.OSRWS SEM4.OSRWS field.

15.6.85 OSD1FIFOS—Offset 130h

Output Stream Descriptor 1 FIFO Size

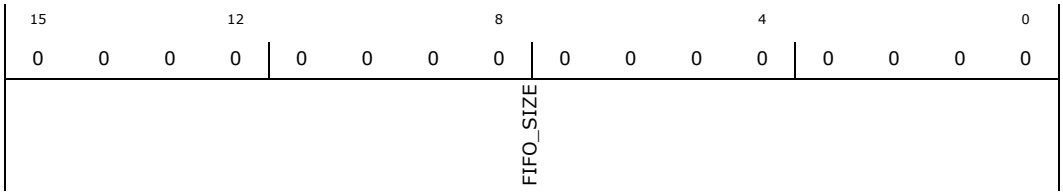
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD1FIFOS: [AZLBAR] + 130h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA d into memory but not yet transmitted on the link and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in OSD1FMT register. As the default value is zero, SW must write to the OSD1FMT register to kick of the FIFO size calculation and read back to find out the HW allocated FIFO size.

15.6.86 OSD1FMT—Offset 132h

Output Stream Descriptor 1 Format

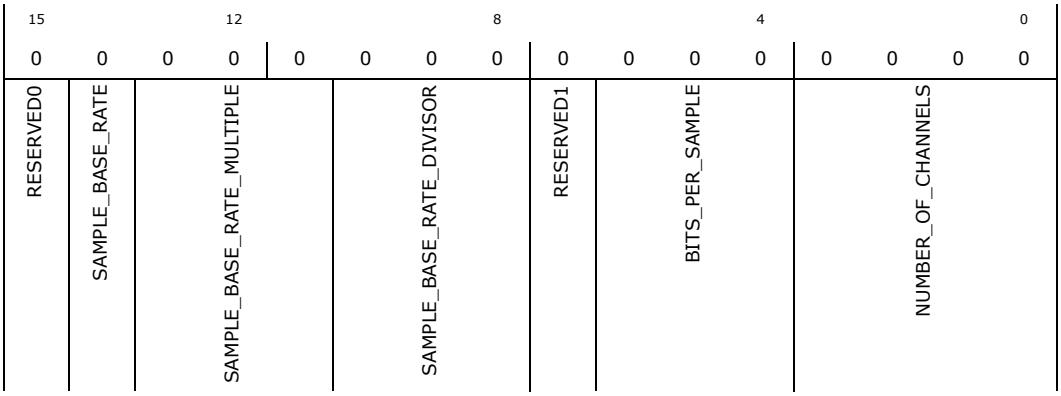
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD1FMT: [AZLBAR] + 132h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

15.6.87 OSD1BDLPLBA—Offset 138h

Output Stream Descriptor 1 Buffer Descriptor List Pointer Lower Base Address

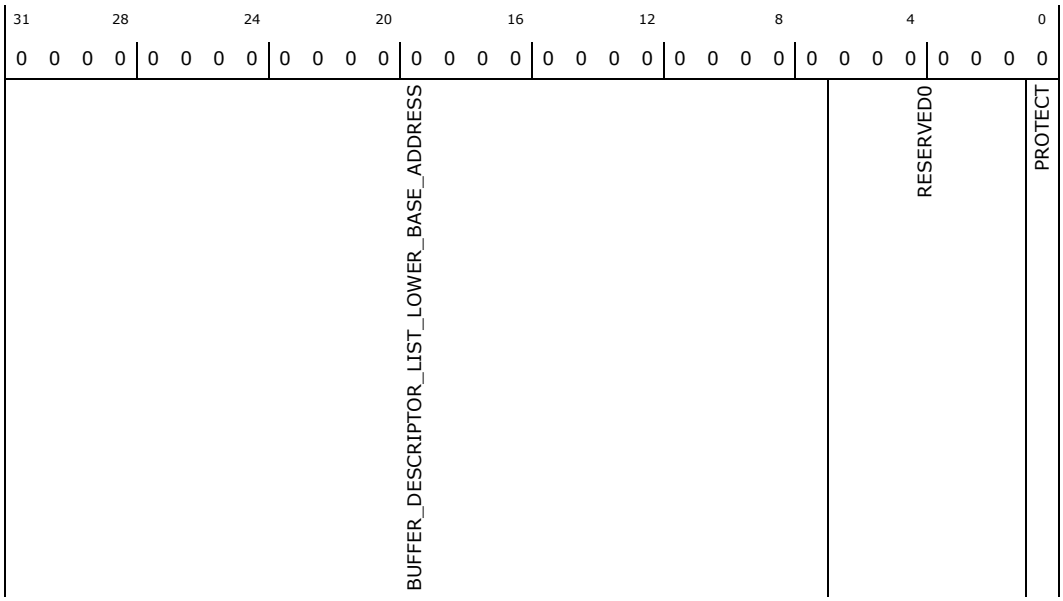
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD1BDLPLBA: [AZLBAR] + 138h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

15.6.88 OSD1BDLPUBA—Offset 13Ch

Output Stream Descriptor 1 Buffer Descriptor List Pointer Upper Base Address

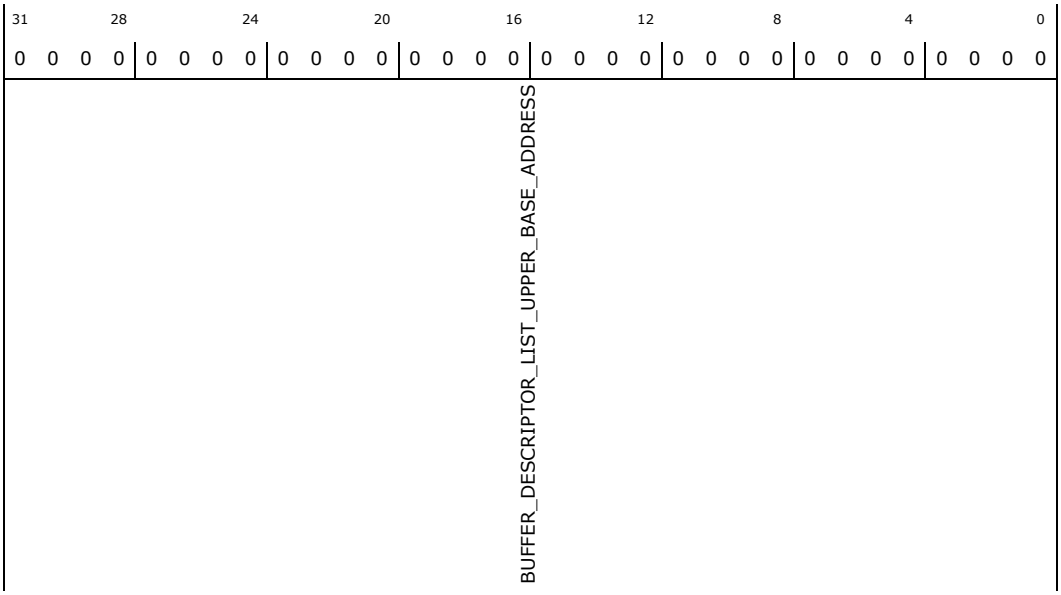
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD1BDLPUBA: [AZLBAR] + 13Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

15.6.89 OSD2CTL_STS—Offset 140h

Output Stream Descriptor 2 Control and status

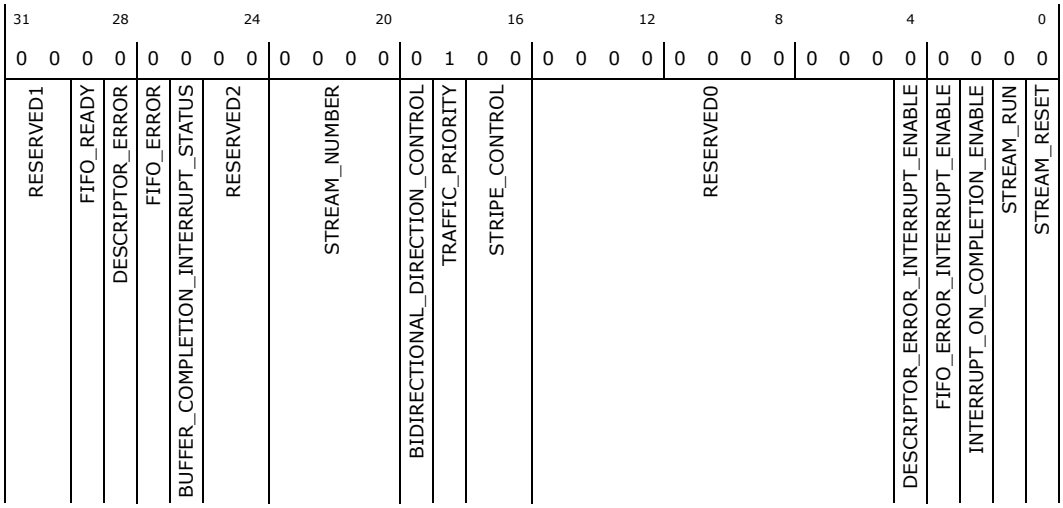
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

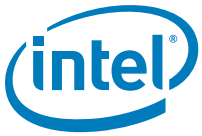
OSD2CTL_STS: [AZLBAR] + 140h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h



Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For output streams the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an output stream this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved



Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link it will have this stream number encoded on the SYNC signal. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in the HD Audio controller. Therefore it is hardwired to 0 s.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error under run for output will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

15.6.90 OSD2LPIB—Offset 144h

Output Stream Descriptor 2 Link Position in Buffer

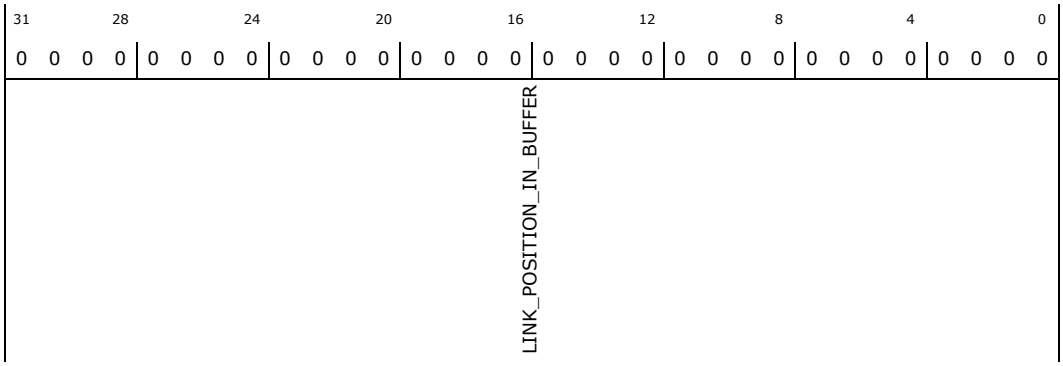
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD2LPIB: [AZLBAR] + 144h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.91 OSD2CBL—Offset 148h

Output Stream Descriptor 2 Cyclic Buffer Length

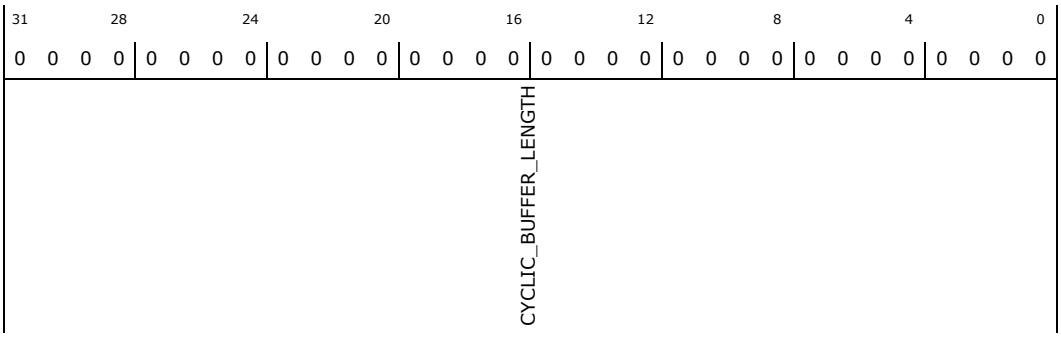
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD2CBL: [AZLBAR] + 148h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

15.6.92 OSD2LVI—Offset 14Ch

Output Stream Descriptor 2 Last Valid Index

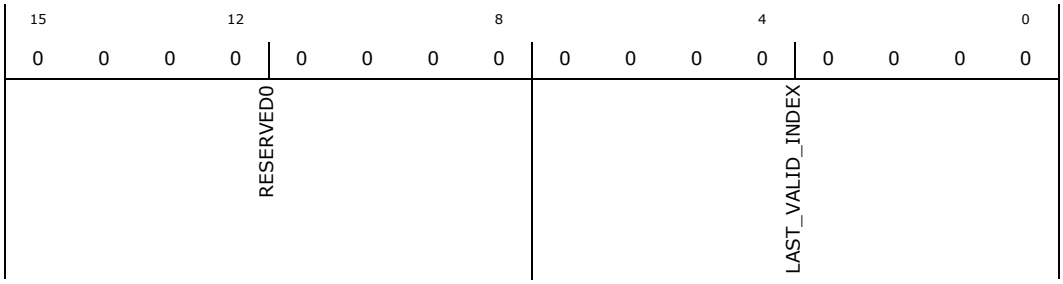
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD2LVI: [AZLBAR] + 14Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, that is, there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

15.6.93 OSD2FIFOW—Offset 14Eh

Output Stream Descriptor 2 FIFO Fetch Watermark

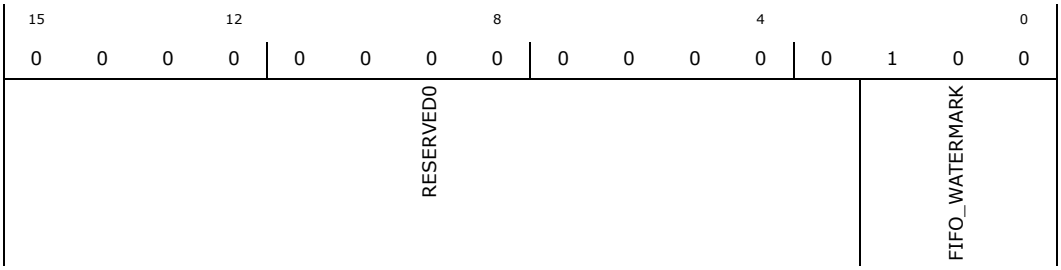
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD2FIFOW: [AZLBAR] + 14Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h



Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes free in the FIFO before the controller will start a fetch of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For output streams the FIFOW value is determined by the EM4.OSRWS SEM4.OSRWS field.

15.6.94 OSD2FIFOS—Offset 150h

Output Stream Descriptor 2 FIFO Size

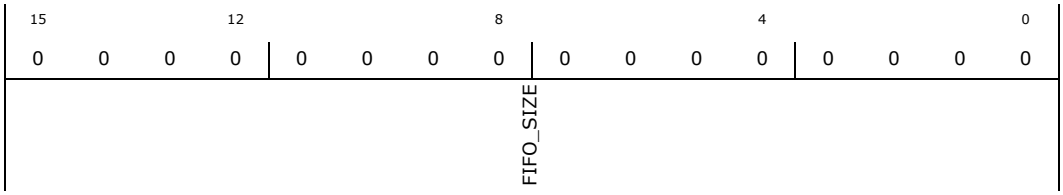
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD2FIFOS: [AZLBAR] + 150h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA d into memory but not yet transmitted on the link and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in OSD2FMT register. As the default value is zero, SW must write to the OSD2FMT register to kick of the FIFO size calculation and read back to find out the HW allocated FIFO size.

15.6.95 OSD2FMT—Offset 152h

Output Stream Descriptor 2 Format

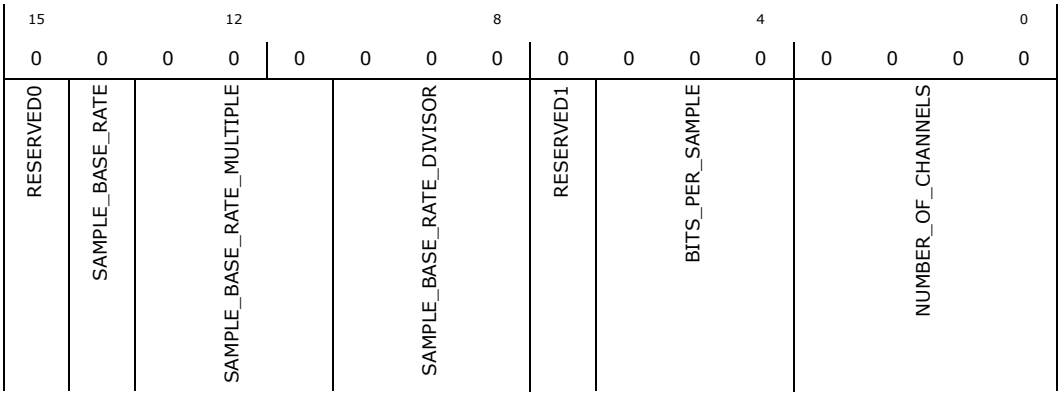
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD2FMT: [AZLBAR] + 152h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

15.6.96 OSD2BDLPLBA—Offset 158h

Output Stream Descriptor 2 Buffer Descriptor List Pointer Lower Base Address

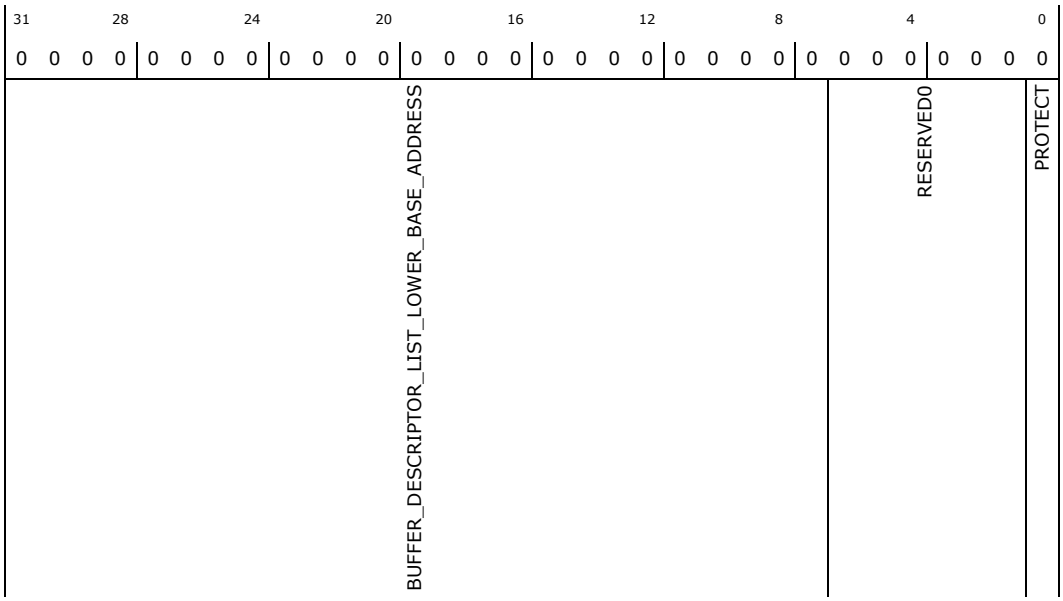
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD2BDLPLBA: [AZLBAR] + 158h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

15.6.97 OSD2BDLPUBA—Offset 15Ch

Output Stream Descriptor 2 Buffer Descriptor List Pointer Upper Base Address

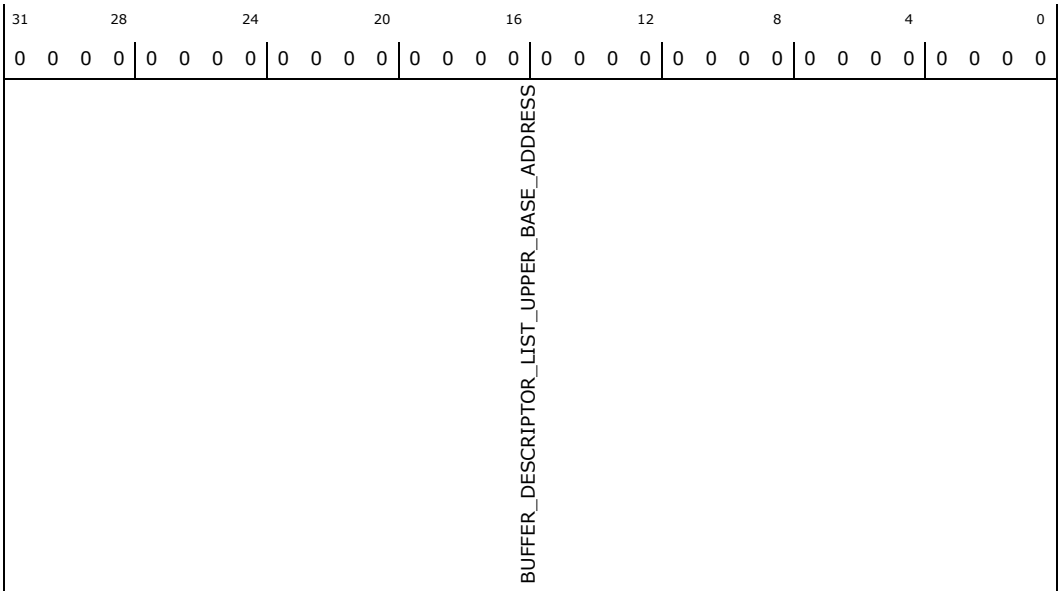
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD2BDLPUBA: [AZLBAR] + 15Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

15.6.98 OSD3CTL_STS—Offset 160h

Output Stream Descriptor 3 Control and status

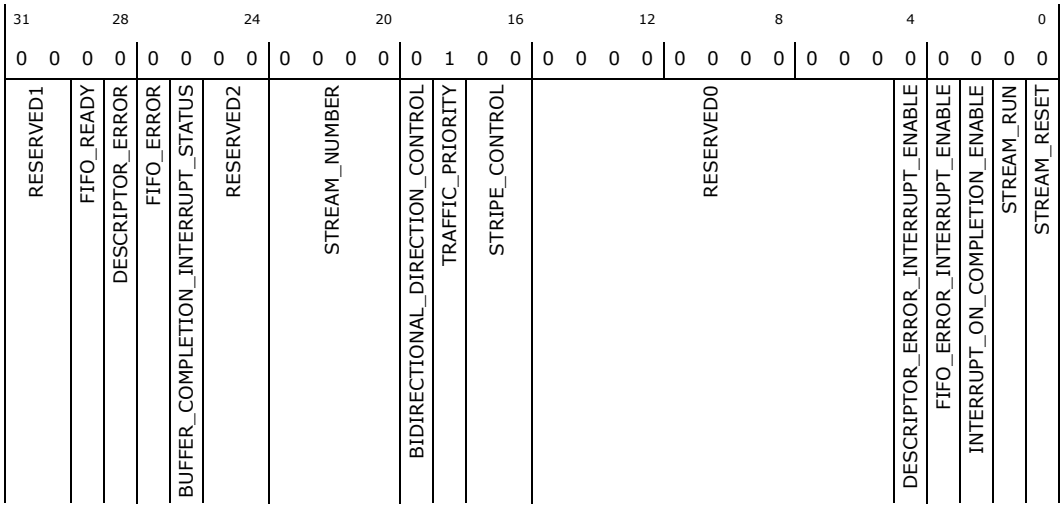
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

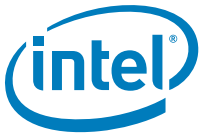
OSD3CTL_STS: [AZLBAR] + 160h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00040000h



Bit Range	Default & Access	Description
31:30	0h RO	**RESERVED1:** reserved
29	0h RO	**FIFO_READY:** For output streams the controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset.
28	0h RW	**DESCRIPTOR_ERROR:** Indicates that a serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort a Parity or ECC error on the bus or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
27	0h RW	**FIFO_ERROR:** Set when a FIFO error occurs. Bit is cleared by writing a 1 to this bit position. This bit is set even if an interrupt is not enabled. For an output stream this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
26	0h RW	**BUFFER_COMPLETION_INTERRUPT_STATUS:** This bit is set to 1 by the hardware after the last sample of a buffer has been processed AND if the Interrupt on Completion IOC bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit position.
25:24	0h RO	**RESERVED2:** reserved



Bit Range	Default & Access	Description
23:20	0h RW	**STREAM_NUMBER:** This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link it will have this stream number encoded on the SYNC signal. 0000 Reserved Indicates Unused 0001 Stream 1 1110 Stream 14 1111 Stream 15
19	0h RO	**BIDIRECTIONAL_DIRECTION_CONTROL:** This bit is only meaningful for Bidirectional streams. Therefore this bit is hardwired to 0.
18	01h RO	**TRAFFIC_PRIORITY:** Hardwired to 1 indicating that all streams will use VC1 if it is enabled throughout the PCI Express registers.
17:16	0h RO	**STRIPE_CONTROL:** For output streams it controls the number of SDO signals to stripe data across. Only one SDO is supported in the HD Audio controller. Therefore it is hardwired to 0 s.
15:5	000h RO	**RESERVED0:** reserved
4	0h RW	**DESCRIPTOR_ERROR_INTERRUPT_ENABLE:** Controls whether an interrupt is generated when the Descriptor Error Status DESE bit is set.
3	0h RW	**FIFO_ERROR_INTERRUPT_ENABLE:** This bit controls whether the occurrence of a FIFO error under run for output will cause an interrupt or not. If this bit is not set bit 3 in the Status register will be set but the interrupt will not occur. Either way the samples will be dropped.
2	0h RW	**INTERRUPT_ON_COMPLETION_ENABLE:** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set bit 2 in the Status register will be set but the interrupt will not occur.
1	0h RW	**STREAM_RUN:** When set to 1 the DMA engine associated with this output stream will be enabled to transfer data in the main memory to FIFO. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams the cadence generator is reset whenever the RUN bit is set. When cleared to 0 the DMA engine associated with this output stream will be disabled. Hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine.
0	0h RW	**STREAM_RESET:** Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers except the SRST bit itself and FIFO s for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation it will report a0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

15.6.99 OSD3LPIB—Offset 164h

Output Stream Descriptor 3 Link Position in Buffer

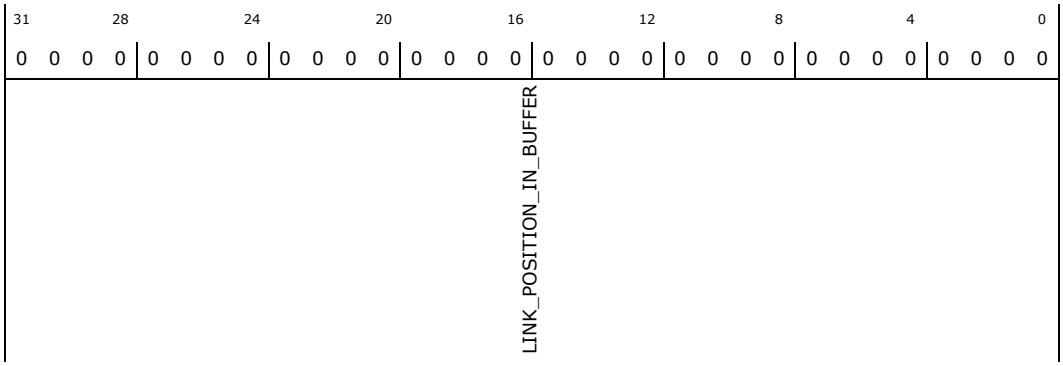
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD3LPIB: [AZLBAR] + 164h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER:** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.100 OSD3CBL—Offset 168h

Output Stream Descriptor 3 Cyclic Buffer Length

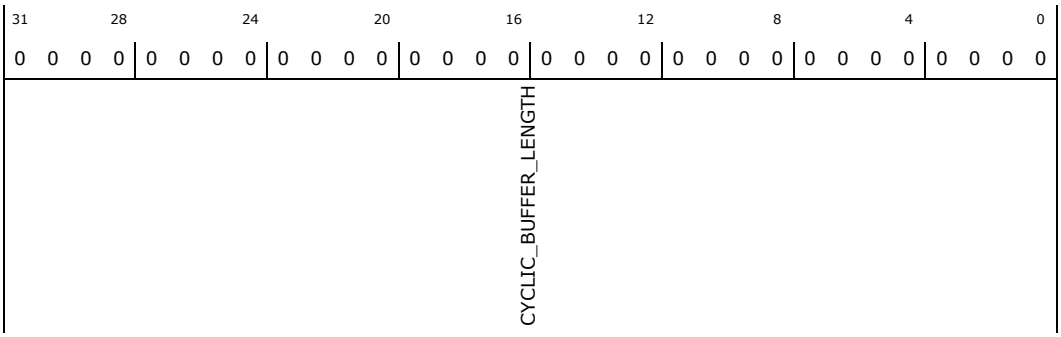
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD3CBL: [AZLBAR] + 168h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**CYCLIC_BUFFER_LENGTH:** Indicates the number of bytes in the complete cyclic buffer. CBL must represent an integer number of samples. Link Position in Buffer LPIB will be reset when it reaches this value. Software may only write to this register after Global Reset Controller Reset or Stream Reset has occurred. This value should only be modified when the RUN bit is 0 . Once the RUN bit has been set to enable the engine software must not write to this register until after the next reset is asserted or transfers may be corrupted.

15.6.101 OSD3LVI—Offset 16Ch

Output Stream Descriptor 3 Last Valid Index

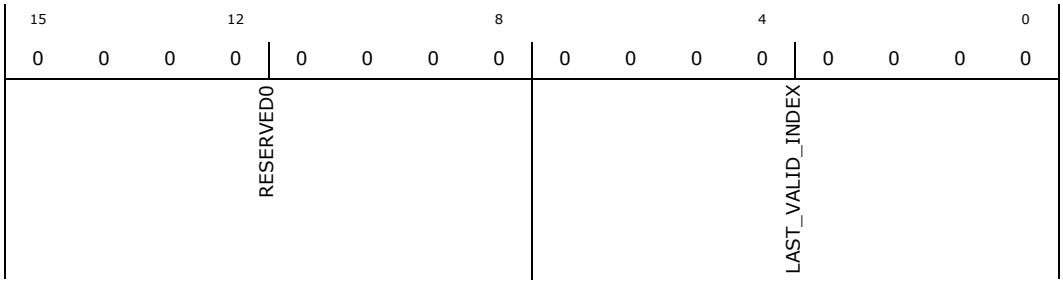
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD3LVI: [AZLBAR] + 16Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RO	**RESERVED0:** reserved
7:0	00h RW	**LAST_VALID_INDEX:** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor it will wrap back to the first descriptor in the list and continue processing. LVI must be at least 1, that is, there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0

15.6.102 OSD3FIFOW—Offset 16Eh

Output Stream Descriptor 3 FIFO Fetch Watermark

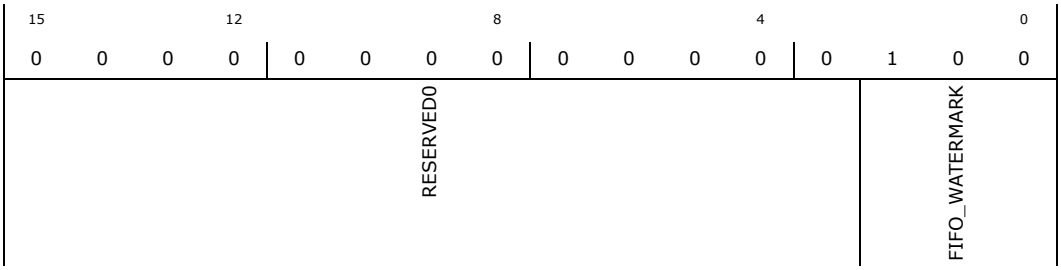
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD3FIFOW: [AZLBAR] + 16Eh

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0004h



Bit Range	Default & Access	Description
15:3	0000h RO	**RESERVED0:** reserved
2:0	04h RO	**FIFO_WATERMARK:** Indicates the minimum number of bytes free in the FIFO before the controller will start a fetch of data. The HD Audio controller hardwires the FIFO Watermark either 32B or 64B based on the following. For output streams the FIFOW value is determined by the EM4.OSRWS SEM4.OSRWS field.

15.6.103 OSD3FIFOS—Offset 170h

Output Stream Descriptor 3 FIFO Size

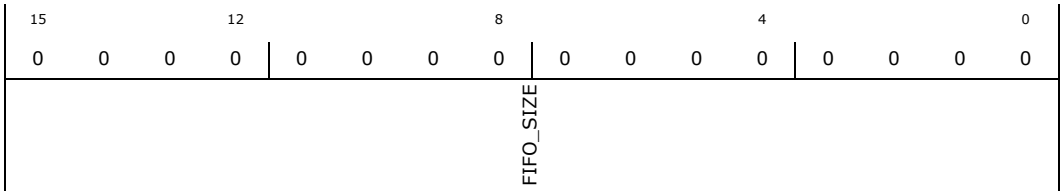
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD3FIFOS: [AZLBAR] + 170h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15:0	00h RW	**FIFO_SIZE:** Indicates the maximum number of bytes that could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA d into memory but not yet transmitted on the link and is also the maximum possible value that the PICB count will increase by at one time. The FIFO size is calculated based on factors including the stream format programmed in OSD3FMT register. As the default value is zero, SW must write to the OSD3FMT register to kick of the FIFO size calculation and read back to find out the HW allocated FIFO size.

15.6.104 OSD3FMT—Offset 172h

Output Stream Descriptor 3 Format

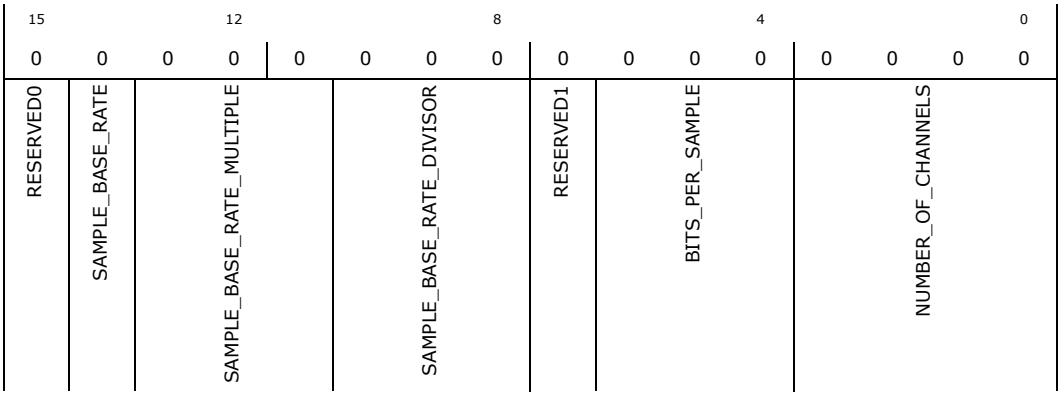
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

OSD3FMT: [AZLBAR] + 172h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 0000h



Bit Range	Default & Access	Description
15	0h RO	**RESERVED0:** reserved
14	0h RW	**SAMPLE_BASE_RATE:** Sample Base Rate (BASE): 0=48kHz 1=44.1kHz
13:11	0h RW	**SAMPLE_BASE_RATE_MULTIPLE:** Sample Base Rate Multiple (MULT): 000=48kHz/ 44.1kHz or less 001=x2 96kHz 88.2kHz 32kHz 010=x3 144kHz 011=x4 192kHz 176.4kHz 100-111 Reserved
10:8	0h RW	**SAMPLE_BASE_RATE_DIVISOR:** Sample Base Rate Divisor (DIV): 000 Divide by 1, 48kHz 44.1kHz 001 Divide by 2, 24kHz 22.05kHz 010 Divide by 3, 16kHz 32kHz 011 Divide by 4, 11.025kHz 100 Divide by 5, 9.6kHz 101 Divide by 6, 8kHz 110 Divide by 7 111 Divide by 8, 6kHz
7	0h RO	**RESERVED1:** reserved
6:4	0h RW	**BITS_PER_SAMPLE:** Bits per Sample (BITS): 000=8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001=16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 010=20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011=24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 100=32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101-111 Reserved
3:0	0h RW	**NUMBER_OF_CHANNELS:** Number of channels in each frame of the stream 0000=1 0001=2 1111=16

15.6.105 OSD3BDLPLBA—Offset 178h

Output Stream Descriptor 3 Buffer Descriptor List Pointer Lower Base Address

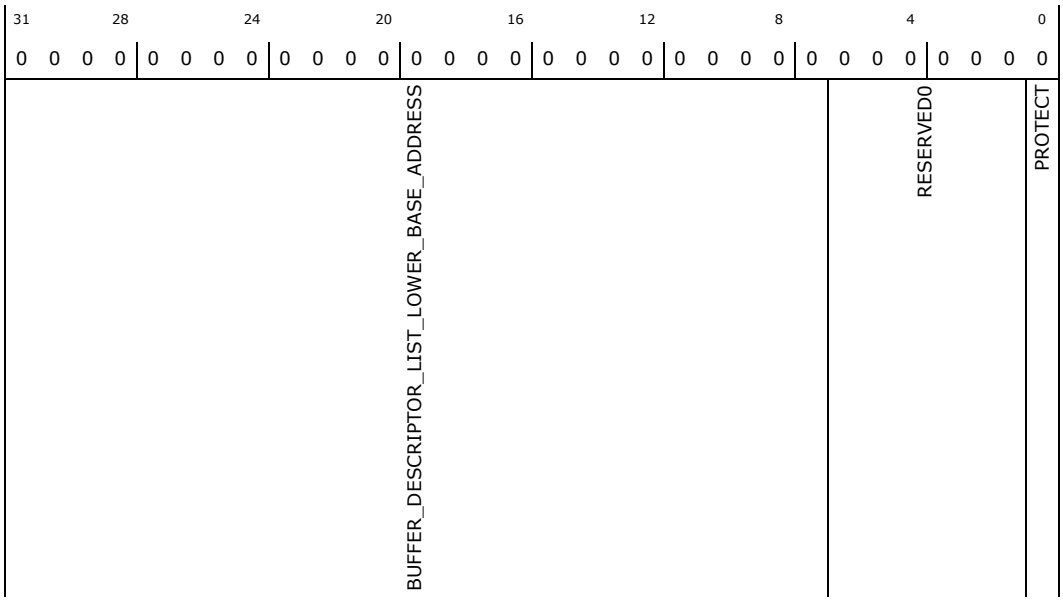
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD3BDLPLBA: [AZLBAR] + 178h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0h RW	**BUFFER_DESCRIPTOR_LIST_LOWER_BASE_ADDRESS:** Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or DMA transfers may be corrupted. Intel Reserved comment This field becomes WO and 0 s will be read when the Protect bit is set to 1.
6:1	00h RO	**RESERVED0:** reserved
0	0h RW	**PROTECT:** When this bit is set to 1 bits 31 7 0 of this register are WO and will return 0 s when read. When this bit is cleared to 0 bits 31 7 0 are RW. Note that this bit can only be changed when all four bytes of this register are written in a single write operation. If less than four bytes are written this bit retains its previous value. This bit is Intel Reserved.

15.6.106 OSD3BDLPUBA—Offset 17Ch

Output Stream Descriptor 3 Buffer Descriptor List Pointer Upper Base Address

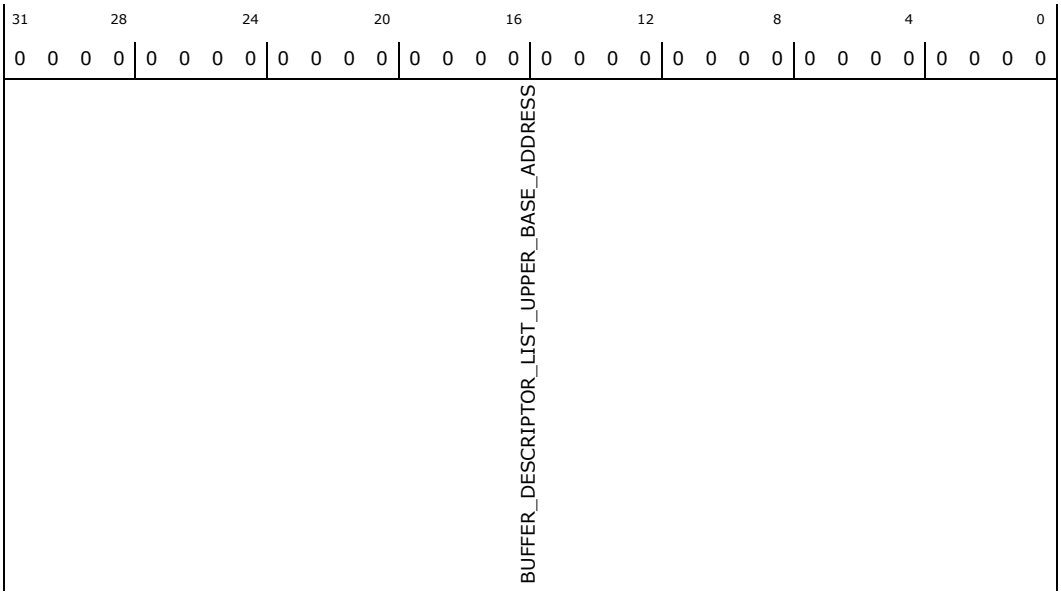
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD3BDLPUBA: [AZLBAR] + 17Ch

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**BUFFER_DESCRIPTOR_LIST_UPPER_BASE_ADDRESS:** Upper 32 bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0 or the DMA transfer may be corrupted.

15.6.107 WLCLKA—Offset 2030h

Wall Clock Alias

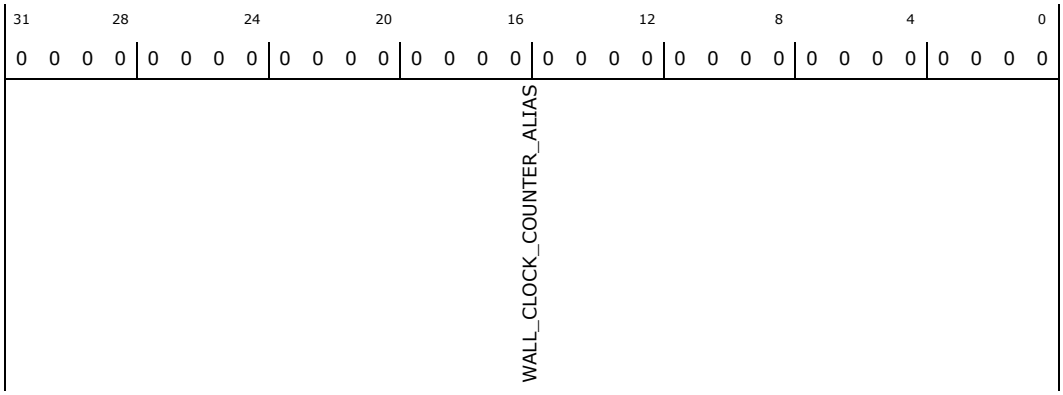
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

WLCLKA: [AZLBAR] + 2030h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**WALL_CLOCK_COUNTER_ALIAS:** This is an alias of the WALCK register. 32 bit counter that is incremented on each link BCLK period and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.

15.6.108 ISD0LPIBA—Offset 2084h

Input Stream Descriptor 0 Link Position in Buffer Alias

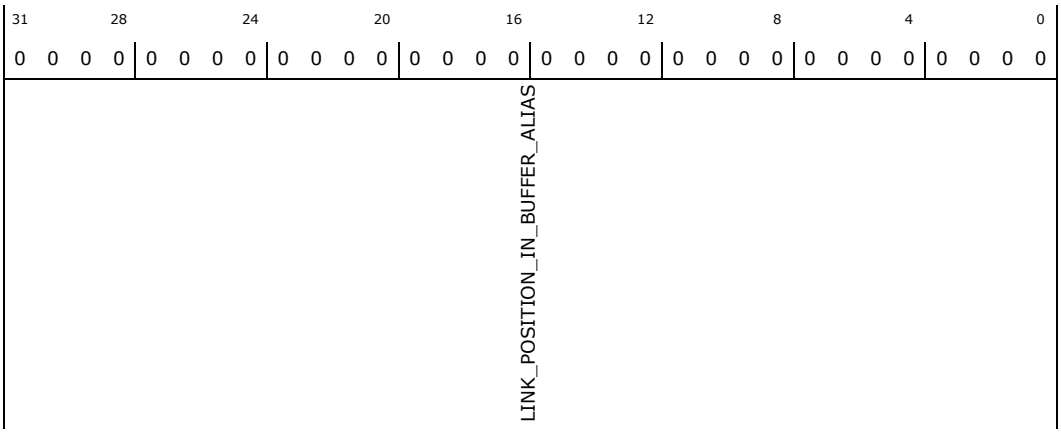
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD0LPIBA: [AZLBAR] + 2084h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.109 ISD1LPIBA—Offset 20A4h

Input Stream Descriptor 1 Link Position in Buffer Alias

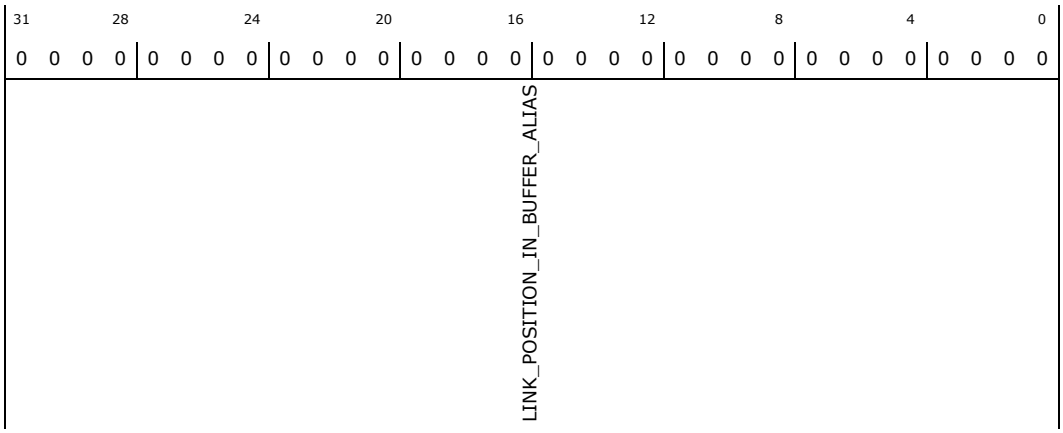
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD1LPIBA: [AZLBAR] + 20A4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.110 ISD2LPIBA—Offset 20C4h

Input Stream Descriptor 2 Link Position in Buffer Alias

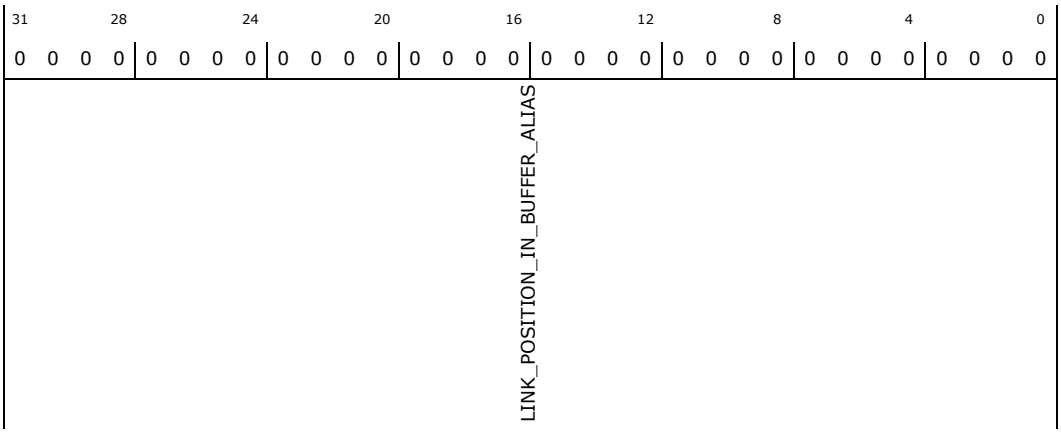
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD2LPIBA: [AZLBAR] + 20C4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.111 ISD3LPIBA—Offset 20E4h

Input Stream Descriptor 3 Link Position in Buffer Alias

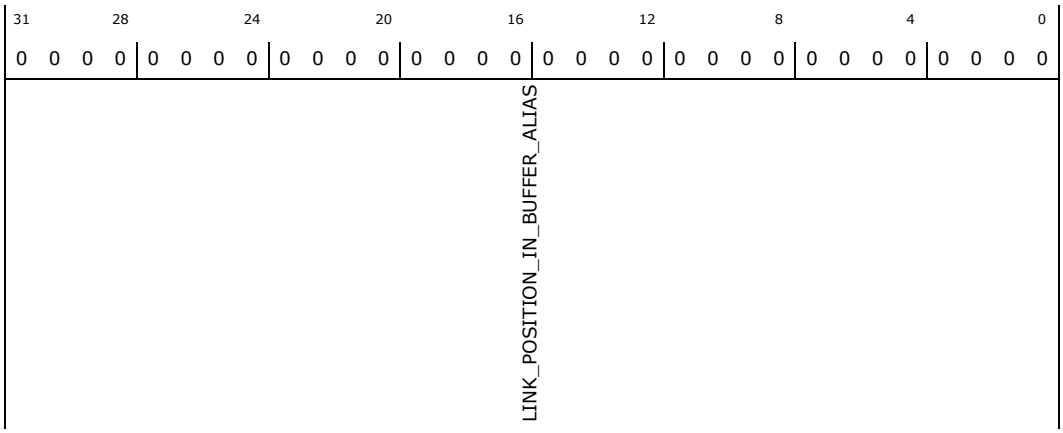
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

ISD3LPIBA: [AZLBAR] + 20E4h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.112 OSD0LPIBA—Offset 2104h

Output Stream Descriptor 0 Link Position in Buffer Alias

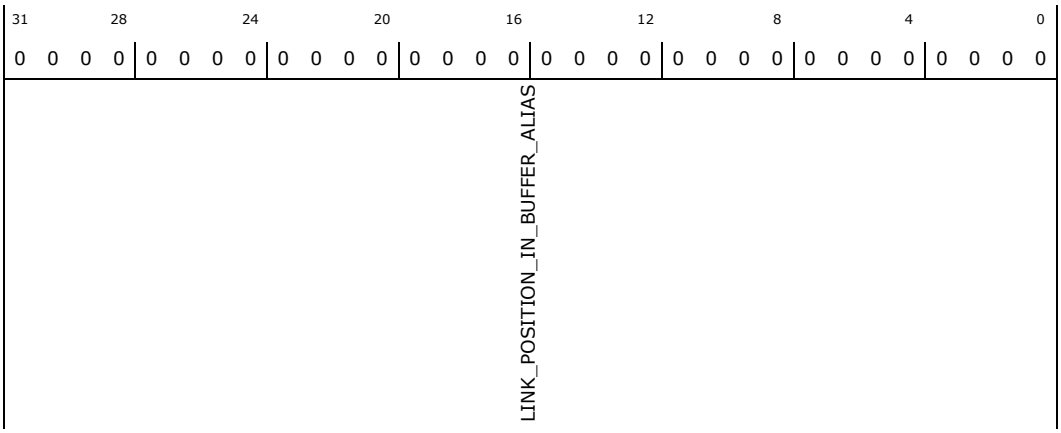
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD0LPIBA: [AZLBAR] + 2104h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.113 OSD1LPIBA—Offset 2124h

Output Stream Descriptor 1 Link Position in Buffer Alias

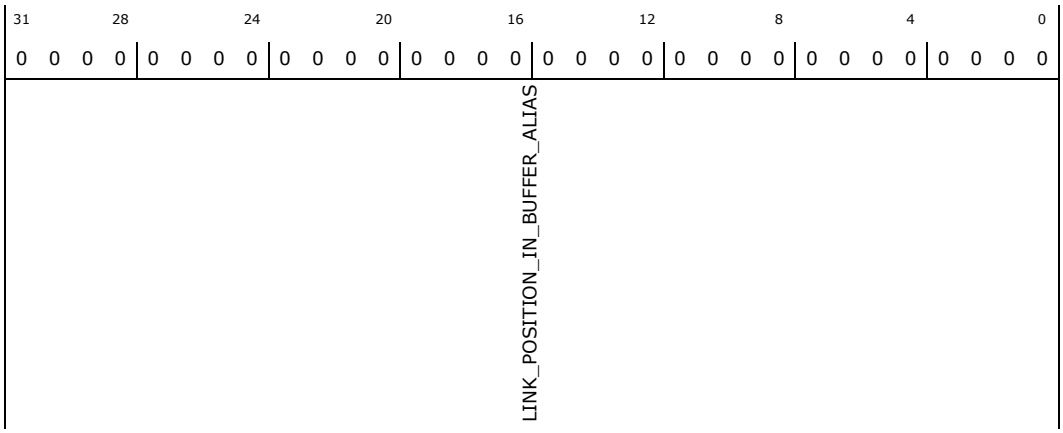
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD1LPIBA: [AZLBAR] + 2124h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.114 OSD2LPIBA—Offset 2144h

Output Stream Descriptor 2 Link Position in Buffer Alias

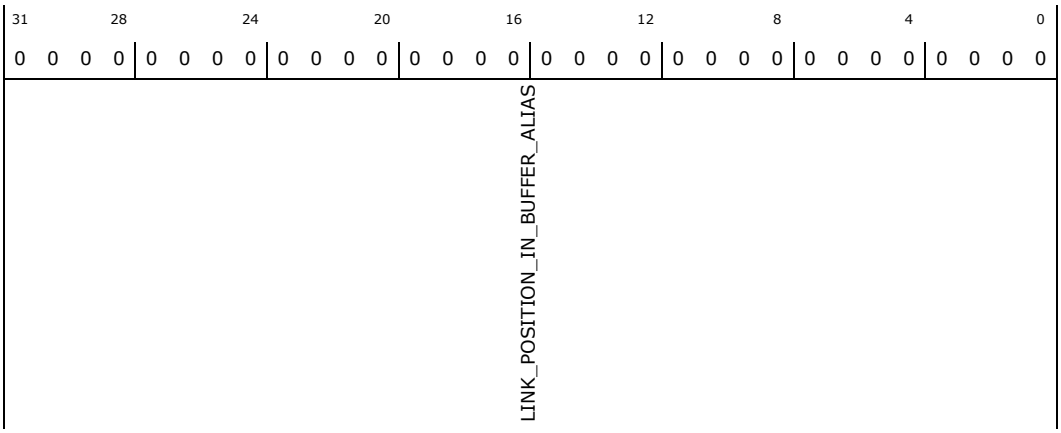
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD2LPIBA: [AZLBAR] + 2144h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

15.6.115 OSD3LPIBA—Offset 2164h

Output Stream Descriptor 3 Link Position in Buffer Alias

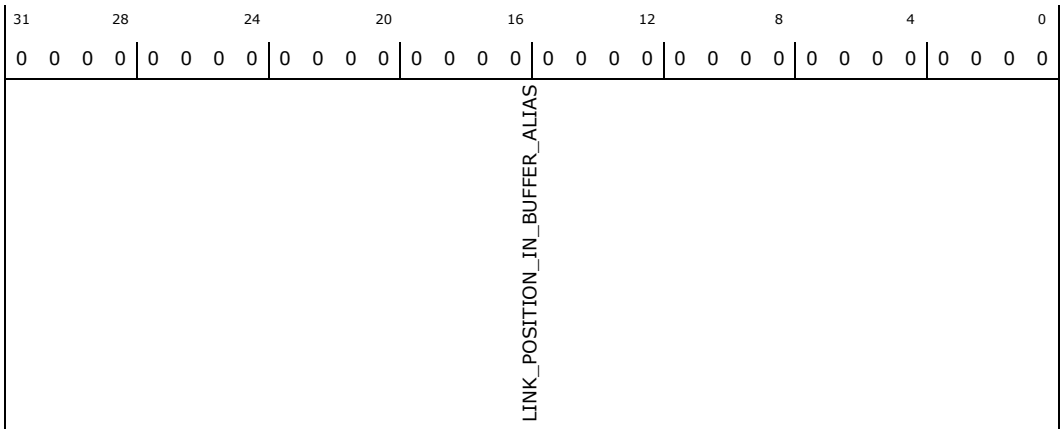
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

OSD3LPIBA: [AZLBAR] + 2164h

AZLBAR Type: PCI Configuration Register (Size: 32 bits)
AZLBAR Reference: [B:0, D:27, F:0] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RO	**LINK_POSITION_IN_BUFFER_ALIAS:** This is an alias of the corresponding LPIB register. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

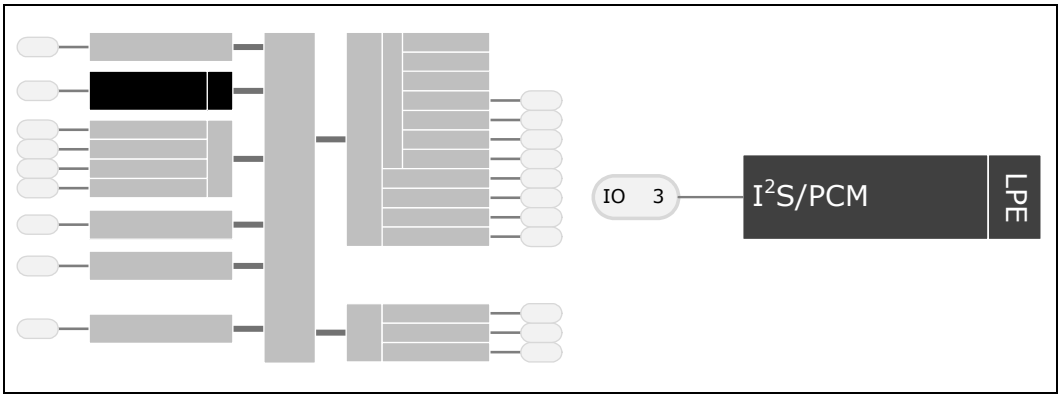
§ §

16 Low Power Engine (LPE) for Audio (I^2S)

The Low Power Engine for Audio provides acceleration for common audio and voice functions. The voice and audio engine provides a mechanism for rendering audio and voice streams and tones from the operating system, applications to an audio or voice codec, and ultimately to the speaker, headphones, or Bluetooth headsets.

Audio streams in the processor can be encoded and decoded by the Low Power Engine (LPE) in the Audio subsystem.

LPE Audio provides three external I^2S audio interfaces.



Note: LPE/I^2S interfaces are not planned to be supported by the processor on Windows 8 Non Connected Standby.

Table 124. Processor Software POR for LPE/I^2S Interfaces

OS/SW Component	Supported?	Notes
Windows 8 Non Connected Standby	No	

16.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 125. LPE Signals

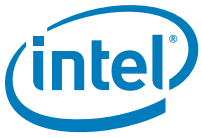
Signal Name	Direction /Type	Description
LPE_I2S2[0:2]_CLK	I/O	Clock signal for I^2S
LPE_I2S2[0:2]_FRM	I/O	Frame select signal for I^2S
LPE_I2S2[0:2]_DATAIN	I/O	RX data for I^2S
LPE_I2S2[0:2]_DATAOUT	I/O	TX data for I^2S

† All LPE signals are multiplexed and may be used by other functions.

16.2 Features

The LPE Audio Subsystem consists of the following:

- Integrated, power-efficient 32-bit architecture core with 24-bit audio processing instructions
- Core processing speeds up to 343 MHz
- Closely Coupled Memories (CCMs)
  - 80KB Instruction RAM
  - 160KB Data RAM
  - 48KB Instruction Cache
  - 96KB Data Cache
- Very low-power consumption coupled with high-fidelity 24-bit audio
- Dual-issue, static, super-scalar VLIW processing engine
- Mode-less switching between 16-, 24-, and 64-bit dual-issue instructions
- Dual MACs which can operate with 32 x 16-bit and/or 24 x 24-bit operands
- Inter-Process Communication (IPC) mechanism to communicate with the processor Core including 4KB mailbox memory
- Flexible audio interfaces include three SSPs with I^2S port functionality for I-directional audio transfers
  - I^2S mode supports PCM payloads
  - Frame counters for all I^2S ports
- PWM (Pulse Width Modulation) function
- High Performance DMA
  - DMA IP to support multiple outstanding transactions
  - Interleaved scatter-gather support for Audio DMA transfers
- Clock switching logic including new frequency increments
- External timer function with an always running clock.



The LPE core runs at a peak clock frequency of 343 MHz and has dedicated on-chip program and data memories and caches. The LPE core can access shared SRAM blocks, and external DRAM through OCP fabric. It communicates with audio peripherals using the audio sub-fabric, and employs Inter-Processor Communication (IPC) mechanism to communicate with the processor Core.

The Audio subsystem includes two OCP-based DMA engines. These DMA engines support single and multi-block transfers. They can be configured to transfer data between DRAM and audio CCMs or transfer data between CCMs and the audio peripheral interfaces

All these interfaces are peripherals in the Audio subsystem. LPE, LPE DMA, or the processor core may access the peripherals during normal operation. The PMC may access all peripherals during specific tasks such as at boot time or during power state changes.A complete audio solution based on an internal audio processing engine which includes several I^2S-based output ports.

The audio core used is a dedicated audio DSP core designed specifically for audio processing (decoding, post-processing, mixing, etc.)

Note: LPE requires systems with more than 512MB memory. This is required since the LPE firmware must reside at a stolen memory location on 512MB boundaries below 3 GiB. The LPE firmware itself is ~1MB, and is reserved by BIOS for LPE use.

16.2.1 Audio Capabilities

16.2.1.1 Audio Decode

The Audio core supports decoding of the following formats:

- MP3
- AAC-LC
- HE-AAC v1/2
- WMA9,10, PRO, Lossless, Voice
- MPEG layer 2
- RealAudio
- OggVorbis
- FLAC
- DD/DD+

16.2.1.2 Audio Encode

The Audio core supports encoding of the following formats:

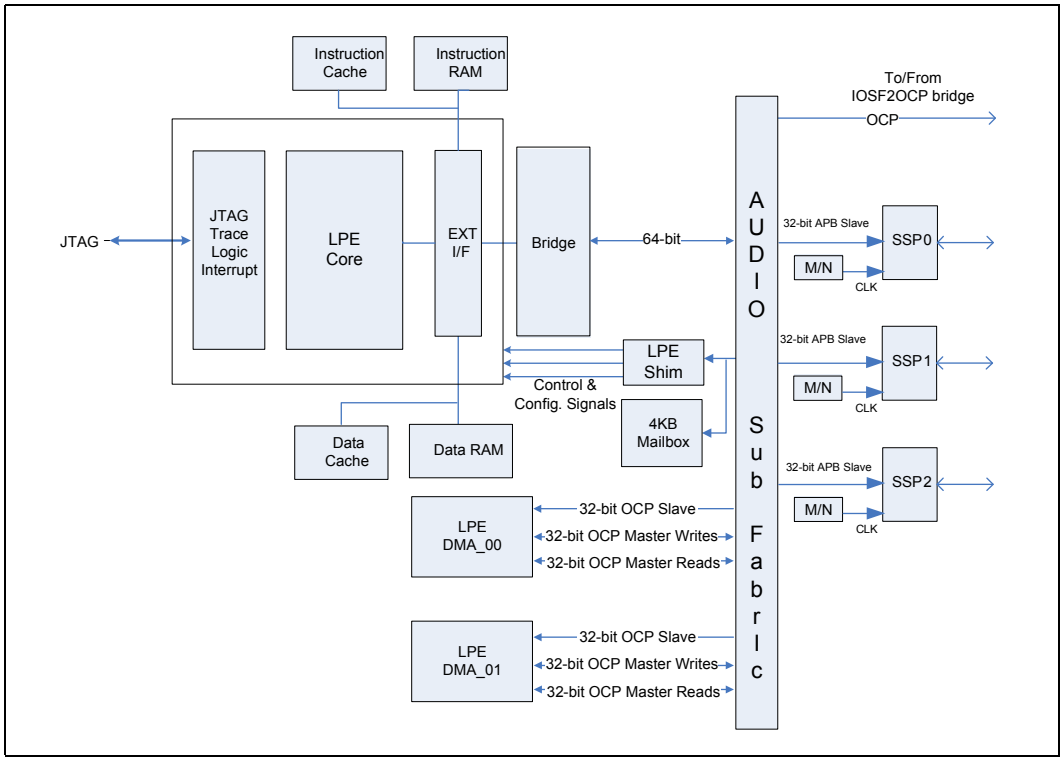
- MP3
- AAC-LC
- WMA
- DD-2channel

16.3 Detailed Block Level Description

16.3.1 LPE Core

The LPE core in the processor runs at maximum frequency of 343 MHz and interfaces with the rest of the processor system through the OCP bus. It is one of the masters on the Audio Sub-Fabric The IA-32 CPU and LPE DMA engines are the other masters on the fabric. The following figure shows the LPE core and its interfaces.

Figure 21. Audio Cluster Block Diagram



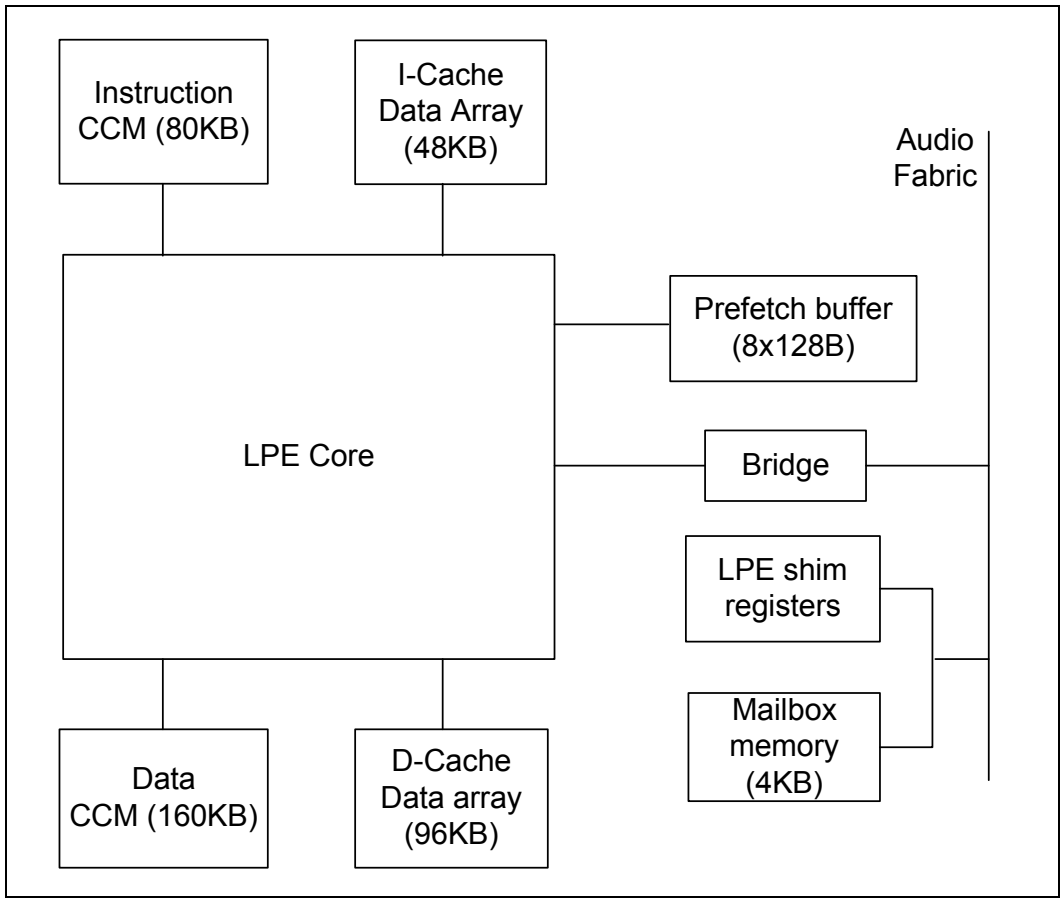
The main DSP hardware is a two-multiplier, multiply/accumulate unit, a register file LPE_PR to hold pairs of 24-bit data items, a register file LPE-OR to hold 56-bit accumulator values, an arithmetic/logic unit to operate on the LPE_PR and LPE_OR values, and a shift unit to operate on the LPE_PR and LPE_OR values. The multiply/

accumulate unit also supports multiplication of 32-bit values from LPE_OR registers by 16-bit values from LPE_PR registers, with the 48-bit result written or accumulated in the LPE_OR register. The instructions for the DSP subsystems are built from operations that are divided into two sets: the slot 0 set and the slot 1 set. In each execution cycle, zero or one operations from each set can be executed independently according to the static bundling expressed in the machine code.

16.3.2 Memory Architecture

The LPE core is configured to use local memory and local caches. It has 80KB of Instruction Closely Coupled Memory (CCM), 160KB of Data CCM, 48KB of Instruction Cache and 96KB of Data Cache. The LPE core also has access to 4KB of mailbox memory and external DRAM.

Figure 22. Memory Connections for LPE



16.3.3 Instruction Closely Coupled Memory (CCM)

Instruction CCM for the core is used for loading commonly used routines as well as time-critical processing. Examples of time critical processing are acoustic echo cancellation and noise cancellation during voice calls.

Instruction CCM is initialized after reset by an external DMA controller. Runtime update of instruction CCM can be done either using explicit instructions or using an external DMA controller with inbound access.

16.3.4 Data Closely Coupled Memory (CCM)

Data CCM can be initialized after reset by an external DMA controller using inbound access. Runtime update of data CCM can be done either using stores to Data CCM or using an external DMA controller with inbound access.

16.3.5 Mailbox Memory and Data Exchange

The mailbox memory is a shared memory region in LPE address space that is accessible by the processor Core, PMC, and LPE. It is used when Doorbell registers cannot hold all the information that one processor wishes to communicate to the other. A typical example of such data blocks are audio stream related parameters when starting a new stream. The structures of data communicated through the mailbox are not defined in hardware so that software may partition the mailbox memory in any desired way and create any meaningful structures required.

16.4 Software Implementation Considerations

16.4.1 Processor Core Cache Coherence

Traffic generated by the LPE core is considered non-cacheable and non-coherent with respect to the processor Core cache. DMA traffic is considered cacheable and checked for coherency with the processor Core cache.

Implications of this implementation are as follows:

- All code and tables for the LPE core need to be explicitly flushed from the processor Core cache if they are ever accessed.
- If the LPE core directly accesses data buffers in system DDR, the driver must explicitly flush the buffer from the processor Core cache
- If DMA accesses data buffers from system DRAM, the driver need not flush the data buffer from the processor Core cache.

16.4.2 Interrupts

16.4.2.1 LPE Peripheral Interrupts

Each of the LPE peripherals generates its own interrupts. SSP0, SSP1, and SSP2 have one interrupt each. Each of the DMA channels have individual interrupt lines. These interrupts are connected to the LPE core through the PISR register. The same interrupts are routed to IOAPIC through the ISRX register. The LPE core and processor Core have individual masks to enable these interrupts.

16.4.2.2 Interrupts Between Processor Core and the LPE

The interrupts between the processor Core and the LPE are handled through the inter-processor communication registers. Whenever the processor Core writes to the IPCX communication register an interrupt is generated to the LPE. The LPE firmware sees there is a message waiting from the processor Core, and reads the IPCX register for the data. This data is a pre-configured message, where the message structure has been decided beforehand between the processor Core and the LPE. Similarly we have the IPCD register for the communication between the LPE and processor Core. Once the LPE writes to the IPCD register, an interrupt should be generated for the processor Core and the processor Core should read the message from the IPCD register and act accordingly. From a software viewpoint, the mechanism remains the same as before. From a hardware view point, the interrupt to IA-32 gets routed by means of the IOAPIC block. The IPC from Audio to IA-32 gets a dedicated interrupt line to the IOAPIC.

16.4.2.3 Interrupts between PMC and LPE

The interrupts between PMC and LPE are also handled using Inter Process Communication registers.

16.4.3 Power Management Options for the LPE Core

- WAITI
  - — Allows the LPE core to suspend operation until an interrupt occurs by executing the optional WAITI instruction.
- External Run/Stall Control Signal
  - — This processor input allows external logic to stall large portions of the LPE pipeline by shutting off the clock to much of the processor's logic to reduce operating power when the LPE computational capabilities are not immediately needed by the system.

Note: Using the WAITI instruction to power down the processor will save more power than use of the external run/stall signal because the WAITI instruction disables more of the LPE's internal clocks.

16.4.3.1 Audio S0ix Low Power Mode Entry

- S0i1 and S0i2 entry are identical from the audio subsystem perspective. The choice between S0i1 and S0i2 is decided by the latency that can be tolerated. For MP3 codec playback the system uses S0i2.
- As part of S0ix entry decision making, SCU firmware needs to comprehend the frequency requirements of the audio core and the latency tolerance (LTR) as reported by audio firmware to SCU firmware (by means of the IPC). The audio core frequency requirement has to be either 19.2 or 38.4 MHz for the system to enter into S0ix with audio ON. Similarly the LTR reported earlier by audio firmware has to allow S0ix entry.

16.4.4 External Timer

This timer always runs from SSP clock (before M/N divider) at 19.2/25MHz. The timer starts running once the run bit (refer to the External timer register definition for details) is set and the clear bit is cleared.

The timer generates an Interrupt pulse when the counter value matches the “match” value. The interrupt does not get generated if the match value is set to “0”. The timer runs in free running mode and rolls over after all 32 bits have become all 1’s.

The timer continues to run as long as the run bit is set. Once the run bit is cleared the timer holds the current value. The clear bit needs to be set to restart the timer from “0”.

16.5 Clocks

16.5.1 Clock Frequencies

Table 126 shows the clock frequency options for the Audio functional blocks.

Table 126. Clock Frequencies

Clock	Frequency	Notes
Audio core	343/250/200 MHz/100/ 50 MHz/2x Osc/Osc	Audio input clock trunk. CCU drives one of several frequencies as noted.
DMA 0	50/OSC	DMA clock
DMA1	50/OSC	DMA clock
Audio fabric clock	50/OSC	Fabric clock derived from audio core clock

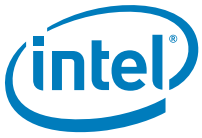


Table 126. Clock Frequencies

Clock	Frequency	Notes
SSP0 Clock	Fabric side: 50/OSC Link side: Up to 19.2 MHz	SSP0 clock domains
SSP1 Clock	Fabric side: 50/OSC Link side: Up to 19.2 MHz	SSP1 clock domains
SSP2 Clock	Fabric side: 50/OSC Link side: Up to 19.2 MHz	SSP2 clock domains

16.5.2 50 MHz Clock for LPE

50 MHz, the 2X OSC clock, is added to increase MIPS for low power MP3 mode. This frequency will be supplied by the clock doubler internal to the processor's Clock Control Unit.

16.5.3 Cache and CCM Clocking

Data CCM, Data cache, Instruction CCM, and Instruction Cache run off of the LPE clock. These memories are in a single clock domain.

Note: All Data CCM and Instruction CCM run in the same clock domain.

16.5.4 SSP Clocking

SSP could be used as either clock masters or clock slaves. Consequently, theses IP have dual clock domains.

The first clock domain is clocked from an internal clock (e.g., fabric clock) and is used for generic logic like interrupt generation and register access.

The second clock domain drives the serial shift register (either driven internally or externally). When driven internally, this clock can be sourced from XTAL clock 25 MHz or PLL 19.2 MHz. These clocks are then divided down within the serial interface IP to generate the final bit clock for the interface.

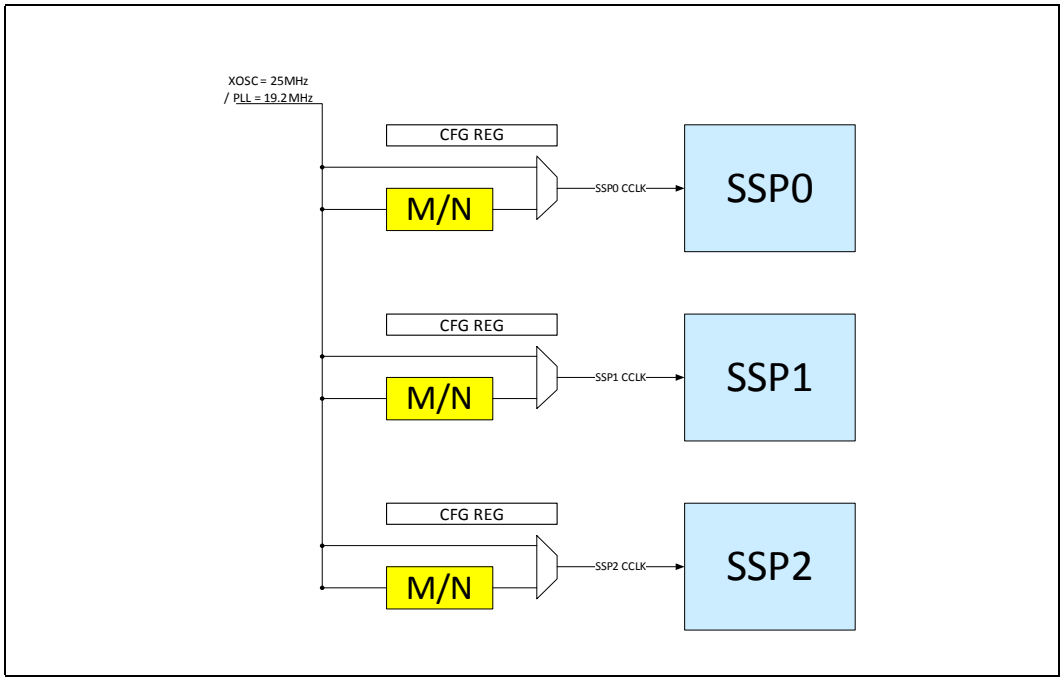
After power on, if the SSP input IO clock is in high state, first transition of the clock from high to low may be missing due to the processor clock gating logic.

Note: "Frame Master" mode cannot be used when operating as clock slave and "Frame Slave" mode cannot be used when operating as clock master.

16.5.5 M/N Divider

LPE SSP in master mode uses the SSP CCLK to drive the serial clock. It has very limited option to divide CCLK. An M/N divider is added between the 25 MHz clock (XOSC) from CCU to each SSP CCLK input as shown in following diagram:

Figure 23. SSP CCLK Structure



Note: The M/N divider has bypass option so VLV could be configured to act same as TNG.

The LPE M/N divider is designed to produce a clock signal for the SSP block used in master mode. The divider is based on a generic NOM/DENOM divider. The supplied Master clock is 25 MHz (XTAL) or 19.2 MHz (LPPLL), but usually be used by the 25 MHz clock.

This mechanism is good for a wide spectrum of generated clocks. Two registers must be configured to get the target SSP clock. The values for the Nominator and Denominator registers are the smallest divider of:

$$\frac{Nominator}{Denominator} = \frac{Source\_clock}{Target\_clock}$$

16.5.5.1 Example

If we want to generate 17.64 MHz (=400x44.1 KHz) output clock out of 25 MHz clock, we need to program "NOM = 441" and "DENOM = 625":

17.64 MHz = (441/625) x 25 MHz

In general the M over N can generate fractional devisor that could be used for generating the required clocks for Audio codec. Table 127 describes some configuration options of this generic divider:

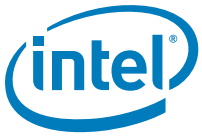


Table 127. M/N Values, Examples

Source Clock Frequency	Requested Clock	M/N Value
25 MHz	48 KHz	6/3125
	48K x 24 = 1.152 MHz	1152/25000
	48K x32 = 1.536 MHz	1536/25000
	48K x 64 = 3.072 MHz	3072/25000
	44.1 KHz	441/250000
	48K x 400 = 19.2 MHz	96/125
	44.1K x 400 = 17.64 MHz	441/625

16.5.5.2 Accuracy and Jitter

The output of the M/N is equal to the desired clock in average with Jitter of 20nTXE for 25 MHz input clock.

16.5.5.3 Configuration

Following configurable fields per M/N divider/SSP are in LPE shim registers:

Table 128. M/N Configurable Fields

Field	Width	Description
Bypass	1 bit	When set M/N divider is bypass. Clock from CCU is connected directly to SSP CCLK
EN	1 bit	Enable the divider
Update	1 bit	Update divider parameters
M Value	20 bits	Nominator value
N Value	20 bits	Denominator value

16.6 SSP (I^2S)

The processor audio subsystem consists of the LPE Audio Engine and three Synchronous Serial Protocol (SSP) ports. These ports are used in PCM mode and enable simultaneous support of voice and audio streams over I^2S. The processor audio subsystem also includes two DMA controllers dedicated to the LPE. The LPE DMA controllers are used for transferring data between external memory and CCMs, between CCMs and the SSP ports, and between CCMs. All peripheral ports can operate simultaneously.

16.6.1 Introduction

The Enhanced SSP Serial Ports are full-duplex synchronous serial interfaces. They can connect to a variety of external analog-to-digital (A/D) converters, audio, and telecommunication codecs, and many other devices which use serial protocols for

transferring data. Formats supported include National* Microwire, Texas Instruments* Synchronous Serial Protocol (SSP), Motorola* Serial Peripheral Interface (SPI) protocol and a flexible Programmable Serial Port protocol (PSP).

The Enhanced SSPs operate in master mode (the attached peripheral functions as a slave) or slave mode (the attached peripheral functions as a master), and support serial bit rates from 0 to 25 Mbps, dependent on the input clock. Serial data formats range from 4 to 32-bits in length. Two on-chip register blocks function as independent FIFOs for transmit and receive data.

FIFOs may be loaded or emptied by the system processor using single transfers or DMA burst transfers of up to the FIFO depth. Each 32-bit word from the bus fills one entry in a FIFO using the lower significant bits of a 32-bit word.

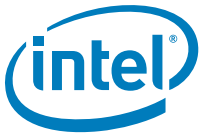
16.6.2 SSP Features

The SSP port features are:

- Inter-IC Sound (I^2S) protocols, are supported by programming the Programmable Serial Protocol (PSP).
- One FIFO for transmit data (TXFIFO) and a second, independent, FIFO for receive data (RXFIFO), where each FIFO is 16 samples deep x 32 bits wide
- Data sample sizes from 8, 16, 18, or 32 bits
- 12.5 Mbps maximum serial bit-rate in both modes: master and slave.
- Clock master or slave mode operations
- Receive-without-transmit operation
- Network mode with up to eight time slots for PSP formats, and independent transmit/receive in any/all/none of the time slots.
- After updating SSP configuration, for example active slot count, the SSP will need to be disabled and enabled again. In other words, a SSP will not function correctly if a user changes the configuration setting on the fly.

16.6.3 Operation

Serial data is transferred between the LPE core or the processor Core and an external peripheral through FIFOs in one of the SSP ports. Data transfers between an SSP port and memory are initiated by either the LPE core or the processor Core using programmed I/O, or by DMA bursts. Although it is possible to initiate transfers directly from the processor Core, current driver design uses LPE for all PCM operations. Separate transmit and receive FIFOs and serial data paths permit simultaneous transfers in both directions to and from the external peripheral, depending on the protocols chosen.



Programmed I/O can transfer data between:

- The LPE core and the FIFO Data register for the TXFIFO
- The processor Core and the FIFO Data register for the TXFIFO
- The LPE core and the FIFO Data register for the RXFIFO
- The processor Core and the FIFO Data register for the RXFIFO
- The processor Core and the control or status registers
- The LPE core and the control or status registers

DMA bursts can transfer data between:

- Universal memory and the FIFO Data register for the TXFIFO
- Universal memory and the FIFO Data register for the RXFIFO
- Universal memory and the sequentially addressed control or status registers

16.6.4 LPE and DMA FIFO Access

The LPE or DMA access data through the Enhanced SSP Port's Transmit and Receive FIFOs. An LPE access takes the form of programmed I/O, transferring one FIFO entry per access. LPE accesses would normally be triggered off of an SSSR Interrupt and must always be 32 bits wide. LPE Writes to the FIFOs are 32 bits wide, but the serializing logic will ignore all bits beyond the programmed FIFO data size (EDSS/DSS value). LPE Reads to the FIFOs are also 32 bits wide, but the Receive data written into the RX FIFO (from the RXD line) is stored with zeroes in the MSBs down to the programmed data size. The FIFOs can also be accessed by DMA bursts, which must be in multiples of 1, 2 or 4 bytes, depending upon the EDSS value, and must also transfer one FIFO entry per access. When the SSCR0.EDSS bit is set, DMA bursts must be in multiples of 4 bytes (the DMA must have the Enhanced SSP configured as a 32-bit peripheral).The DMA's width register must be at least the SSP data size programmed into the SSP control registers EDSS and DSS. The FIFO is seen as one 32-bit location by the processor. For Writes, the Enhanced SSP port takes the data from the Transmit FIFO, serializes it, and sends it over the serial wire (I2S[2:0]_DATAOUT) to the external peripheral. Receive data from the external peripheral (on I2S[2:0]_DATAIN) is converted to parallel words and stored in the Receive FIFO.

A programmable FIFO trigger threshold, when exceeded, generates an Interrupt or DMA service request that, if enabled, signals the CPU or DMA respectively to empty the Receive FIFO or to refill the Transmit FIFO.

The Transmit and Receive FIFOs are differentiated by whether the access is a Read or a Write transfer. Reads automatically target the Receive FIFO, while Writes will write data to the Transmit FIFO. From a memory-map perspective, they are at the same address. FIFOs are 16 samples deep by 32 bits wide. Each read or write is to 1 SSP sample.

16.6.5 Supported Formats

The SSP consists of four pins that are used to transfer data between the processor and external Audio codecs, modems, or other peripherals. Although four serial-data formats exist, each has the same basic structure, and in all cases the following pins are used in the following manner:

- I2Sx_CLK—Defines the bit rate at which serial data is driven onto and sampled from the port
- I2Sx_FRM—Defines the boundaries of a basic data "unit," comprised of multiple serial bits
- I2Sx_DATAIN—The serial data path for transmitted data, from system to peripheral
- I2Sx_DATAOUT—The serial data path for received data, from peripheral to system

A data frame can contain from 4 to 32 bits, depending on the selected format. Serial data is transmitted most significant bit first. The Programmable Serial Protocol (PSP) format is used to implement I^2S.

Master and Slave modes are supported. When driven by the Enhanced SSP, the I2Sx_CLK only toggles during active transfers (not continuously) unless ECRA/ECRB functions are used. When the I2Sx_CLK is driven by another device, it is allowed to be either continuous or only driven during transfers, but certain restrictions on PSP parameters apply.

Normally, the serial clock (I2Sx_CLK), if driven by the Enhanced SSP Port, only toggles while an active data transfer is underway. There are several conditions, however, that may cause the clock to run continuously. If the Receive With Out Transmit mode is enabled by setting the SSCR1.RWOT bit to 1, the I2Sx_CLK will toggle regardless of whether Transmit data exists within the Transmit FIFO. The I2Sx_CLK will also toggle continuously if the Enhanced SSP is in Network mode, or if ECRA, or ECRB is enabled. At other times, I2Sx_CLK will be held in an inactiveI2Sx_FRM or idle state, as defined by the specified protocol under which it operates.

16.6.5.1 Programmable Serial Protocol (PSP)

There are many variations of the frame behavior for different codecs and protocol formats. To allow flexibility the PSP format allows I2Sx_FRM to be programmable in direction, delay, polarity, and width. Master and Slave modes are supported. PSP can be programmed to be either full or half duplex.

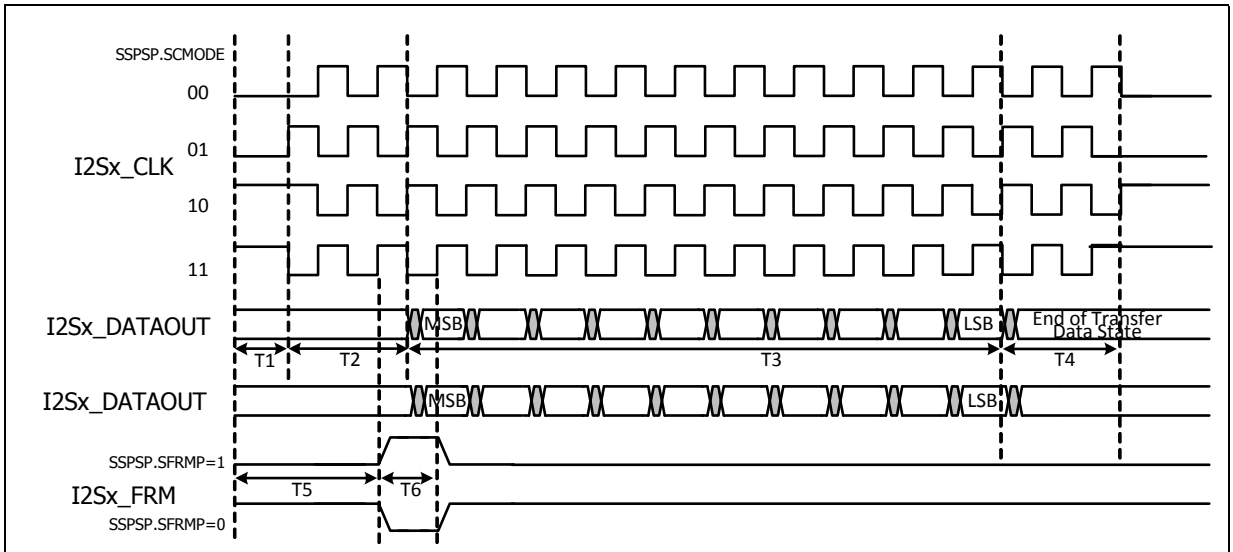
The I2Sx_CLK function behavior varies between each format. PSP lets programmers choose which edge of I2Sx_CLK to use for switching Transmit data, and for sampling Receive data. In addition, programmers can control the idle state for I2Sx_CLK and the number of active clocks that precede and follow the data transmission.

The PSP format provides programmability for several parameters that determine the transfer timings between data samples. There are four possible serial clock sub-modes, depending on the I2Sx_CLK edges selected for driving data and sampling received data, and the selection of idle state of the clock.

For the PSP format, the Idle and Disable modes of the I2Sx_DATAOUT, I2Sx_CLK, and I2Sx_FRM are programmable by means of the SSPSP.ETDS, SSPSP.SCMODE and SSPSP.SFRMP bits. When Transmit data is ready, the I2Sx_CLK will remain in its Idle state for the number of serial clock (I2Sx_CLK) clock periods programmed within the Start Delay (SSPSP.STRTDLY) field. I2Sx_CLK will then start toggling, I2Sx_DATAOUT will remain in the idle state for the number of cycles programmed within the Dummy Start (SSPSP.DMYSTRT) field. The I2Sx_FRM signal will be asserted after the number of half-clocks programmed in the SSPSP.SFRDLY field. The I2Sx_FRM signal will remain asserted for the number of clocks programmed within the SSPSP.SFRMWDTH then de-assert. Four to 32 bits can be transferred per frame. Once the last bit (LSB) is transferred, the I2Sx_CLK will continue toggling based off the Dummy Stop (SSPSP.DMYSTOP) field. I2Sx_DATAOUT either retains the last value transmitted or is forced to zero, depending on the value programmed within the End of Transfer Data State (SSPSP.ETDS) field, when the controller goes into Idle mode, unless the Enhanced SSP port is disabled or reset (which forces I2Sx_DATAOUT to zero).

With the assertion of I2Sx_FRM, Receive data is simultaneously driven from the peripheral on I2Sx_DATAIN, most significant bit first. Data transitions on I2Sx_CLK based on the Serial Clock Mode selected and is sampled by the controller on the opposite edge. When the Enhanced SSP is a master to the frame synch (I2Sx_FRM) and a slave to the clock (I2Sx_CLK), then at least three extra clocks (I2Sx_CLKs) will be needed at the beginning and end of each block of transfers to synchronize control signals from the APB clock domain into the SSP clock domain (a block of transfers is a group of back-to-back continuous transfers).

Figure 24. Programmable Serial Protocol Format



NOTE: When in PSP format, if the SSP is the master of the clock (I2Sx_CLK is an output) and the SSPSP.ETDS bit is cleared, the End of Transfer Data State for the I2Sx_DATAOUT line is 0. If the SSP is the master of the clock, and the SSPSP.ETDS bit is set, the I2Sx_DATAOUT line remains at the last bit transmitted (LSB). If the SSP is a slave to the clock (I2Sx_CLK is an input), and modes 1 or 3 are used, the ETDS can only change from the LSB if more clocks (I2Sx_CLK) are sent to the SSP (that is, dummy stop clocks or slave clock is free running.

Figure 25. Programmable Serial Protocol Format (Consecutive Transfers)

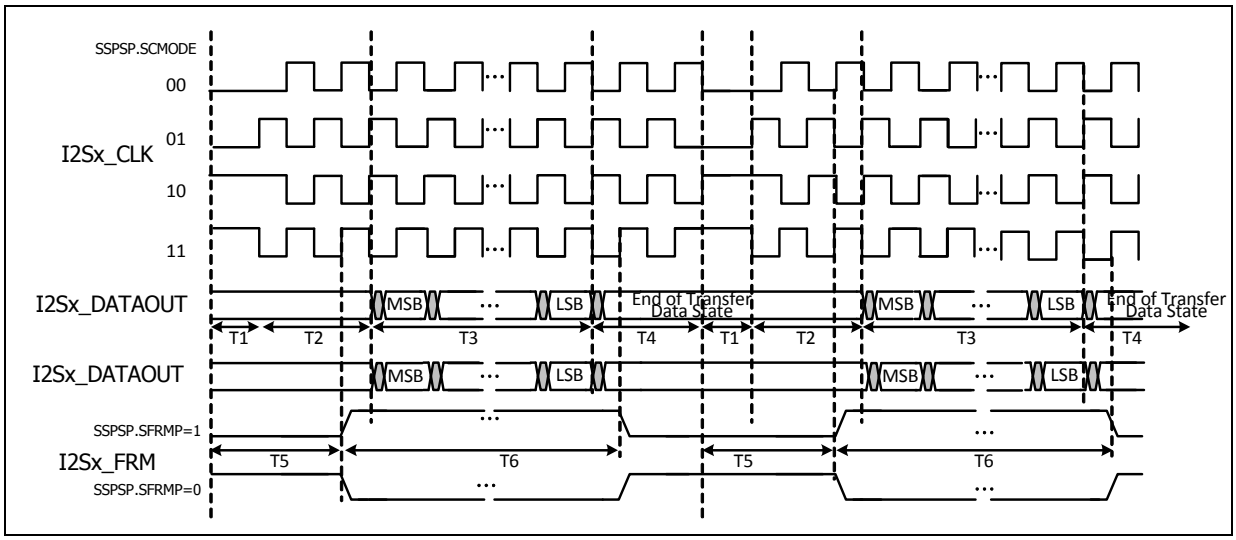
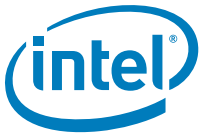


Table 129. Programmable Protocol Parameters

Symbol	Definition (Register.Bit Field)	Range	Units
	Serial Clock Mode (SSPSP.SCMODE)	(Drive, Sample, I2Sx_CLK Idle) 0 = Fall, Rise, Low 1 = Rise, Fall, Low 2 = Rise, Fall, High 3 = Fall, Rise, High	
	Serial Frame Polarity (SSPSP.SFRMP)	High or Low	
T1	Start Delay (SSPSP.STRTDLY)	0–7	Clock Period
T2	Dummy Start (SSPSP.DMYSTRT)	0–3	Clock Period
T3	Data Size (SSCRO.EDSS AND SSCRO.DSS)	4–32	Clock Period
T4	Dummy Stop (SSPSP.DMYSTOP)	0–3	Clock Period
T5	I2Sx_FRM Delay (SPSP.SFRMDLY)	0–88	Half Clock Period
T6	I2Sx_FRM Width (SSPSP.SFRMWDTH)	1–44	Clock Period
	End of Transfer Data State (SSPSP.ETDS)	Low or [bit 0]	

Note: The I2Sx_FRM Delay must not extend beyond the end of T4. I2Sx_FRM Width must be asserted for at least 1 I2Sx_CLK, and should be de-asserted before the end of the T4 cycle (for example, in terms of time, not bit values, (T5 + T6) <= (T1 + T2 + T3 + T4),



1<= T6 < (T2 + T3 + T4), and (T5 + T6) >= (T1 + 1) to ensure that I2Sx_FRM is asserted for at least 2 edges of the I2Sx_CLK). The T1 Start Delay value should be programmed to 0 when the I2Sx_CLK is enabled by either of the SSCR1.ECRA or SSCR1.ECRB bits. While the PSP can be programmed to generate the assertion of I2Sx_FRM during the middle of the data transfer (after the MSB was sent), the Enhanced SSP will not be able to receive data in Frame slave mode (SSCR1SFRMDIR = 1) if the assertion of Frame is not before the MSB is sent (that is, T5 ≤ T2 if SSCR1.SFRMDIR =1). Transmit Data will transition from the "End of Transfer Data State" to the next MSB value upon the assertion of Frame. The Start Delay field should be programmed to 0 whenever I2Sx_CLK or I2Sx_FRM is configured as an input. Clock state is not defined between two active frame periods. Clock can be active or inactive between two active frame periods.

16.7 Programming Model

The CPU or DMA access data through the Enhanced SSP Port's Transmit and Receive FIFOs. A CPU access takes the form of programmed I/O, transferring one FIFO entry per access. CPU accesses would normally be triggered off of an SSSR Interrupt and must always be 32 bits wide. The CPU Writes to the FIFOs are 32 bits wide, but the serializing logic will ignore all bits beyond the programmed FIFO data size (EDSS/DSS value). CPU Reads to the FIFOs are also 32 bits wide, but the Receive data written into the RX FIFO (from the RXD line) is stored with zeroes in the MSBs down to the programmed data size. The FIFOs can also be accessed by DMA bursts, which must be in multiples of 1, 2, or 4 bytes, depending upon the EDSS value, and must also transfer one FIFO entry per access. When the SSCR0.EDSS bit is set, DMA bursts must be in multiples of 4 bytes (the DMA must have the Enhanced SSP configured as a 32-bit peripheral). The DMA DCMD.width register must be at least the SSP data size programmed into the SSP control registers EDSS and DSS. The FIFO is seen as one 32-bit location by the processor. For Writes, the Enhanced SSP port takes the data from the Transmit FIFO, serializes it, and sends it over the serial wire (I2Sx_DATAOUT) to the external peripheral. Receive data from the external peripheral (on I2Sx_DATAIN) is converted to parallel words and stored in the Receive FIFO.

A programmable FIFO trigger threshold, when exceeded, generates an Interrupt or DMA service request that, if enabled, signals the IA-32 CPU or DMA respectively to empty the Receive FIFO or to refill the Transmit FIFO. The Transmit and Receive FIFOs are differentiated by whether the access is a Read or a Write transfer. Reads automatically target the Receive FIFO, while Writes will write data to the Transmit FIFO. From a memory-map perspective, they are at the same address. Each read or write is 1 SSP sample.

16.7.1 PIO and DMA Programming Considerations

All CPU and DMA accesses transfer one FIFO entry per access. Data in the FIFOs is always stored with one 32-bit value per data sample, regardless of the format data word length. Within each 32-bit field, the stored data sample is right-justified, with the least significant bit of the word in bit 0. In the Receive FIFO, unused bits are packed as zeroes above the most significant bit. In the Transmit FIFO, unused don't-care bits are

above the most significant bit (that is, DMA and CPU access do not have to write to the unused bit locations). Logic in the Enhanced SSP automatically formats data in the Transmit FIFO so that the sample is properly transmitted on I2Sx_DATAOUT in the selected frame format.

Two separate and independent FIFOs are present for Transmit (to peripheral) and Receive (from peripheral) serial data. FIFOs are filled or emptied by programmed I/O or DMA bursts.

16.7.1.1 Programmed IO Considerations

FIFO filling and emptying can be performed by the processor in response to an Interrupt from the FIFO logic. Each FIFO has a programmable FIFO trigger threshold at which an Interrupt is triggered. When the number of entries in the Receive FIFO exceeds the SSCR1.RFT value, an interrupt is generated (if enabled), which signals the CPU to empty the Receive FIFO. When the number of entries in the Transmit FIFO is less than or equal to the SSCR1.TFT value plus 1, an Interrupt is generated (if enabled), which signals the CPU to refill the Transmit FIFO.

Users can also poll the Enhanced SSP Status register to determine how many samples are in a FIFO, and whether the FIFO is full or empty. Software is responsible for ensuring that the proper RFT and TFT values are chosen to prevent ROR and TUR error conditions.

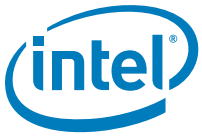
Note: If the software attempts to read from an empty Receive FIFO, it will receive a duplicate of the previously read value.

16.7.1.2 DMA Considerations

The DMA controller can also be programmed to transfer data to and from the Enhanced SSP FIFOs. To prevent over-runs of the Transmit FIFO or under-runs of the Receive FIFO when using the DMA, be careful when setting the Transmit and Receive FIFO trigger threshold levels.

There are restrictions on how the DMA can be programmed when used with the SSP Controller.

- The DMA Transfer Width must be greater than or equal to the SSP data size. For example if the SSP Data Size is 16b then the DMA Transfer Width should be 16b.
- The DMA may not support the DMA Transfer Width of the SSP Data Size and therefore the DMA Transfer Width must be larger than the SSP Data Size. If this is the case then software must manage any extra data bits.
- The DMA Burst Transaction Length for RX must be less than or equal to the RX Threshold.
- The DMA Burst Transaction Length for TX must be less than or equal to the number of empty locations in the TX FIFO. A safe value is the Total TX FIFO Size - TX Threshold.
- DMA must be in Fixed Address mode to read or write the SSP Data Register.



In full-duplex formats where the Enhanced SSP always receives the same number of data samples as it transmits, the DMA should be set up to transmit and receive the same number of bytes.

Note: A TFT value of 0 means that there is one sample left in the TX FIFO.

Because the Enhanced SSP is not flow controlled, software must program the TX FIFO Threshold (TFT), RX FIFO Threshold (RFT), and the DMA burst size to ensure that a TX FIFO overflow or RX FIFO underflow does not occur. Software must also ensure that the Enhanced SSP DMA requests are properly prioritized in the system to prevent fatal overruns and under-runs.

The programming model for using the DMA is as follows:

- Program the total number of Transmit/Receive byte lengths, DMA burst, and DMA Width in the DMA.
- Set the preferred values in the Enhanced SSP Control registers.
- Enable the Enhanced SSP by setting SSCR0.SSE.
- Set the run bit in DMA Command Register.
- The DMA will wait for either the Transmit or Receive Service requests.
- If the Transmit/Receive byte length is not an even multiple of the transfer burst size, a trailing byte condition may occur.

16.7.2 Trailing Bytes in the Receive FIFO

When the number of samples in the Receive FIFO is less than its FIFO trigger threshold level, and no additional data is received, the remaining bytes are called trailing bytes. Trailing bytes can be handled by either the DMA or the processor, as indicated by the SSCR1.TRAIL bit. Trailing bytes are identified by means of a timeout mechanism and the existence of data within the Receive FIFO.

16.7.2.1 Timeout

A timeout condition exists when the Receive FIFO has been idle for a period of time (in APB clocks) defined by the value programmed within the Timeout register (SSTO). When a timeout occurs, the receiver timeout interrupt SSSR.TINT bit will be set to a 1, and if the Timeout Interrupt is enabled SSCR1.TINTE=1, a Timeout Interrupt will occur to signal the processor that a timeout condition has occurred. The timeout timer is reset after a new sample is received. Once the SSSR.TINT bit is set it must be cleared by software by writing a 1 to it. Clearing this bit also causes the Timeout Interrupt, if enabled, to be de-asserted.

16.7.2.2 Peripheral Trailing Byte Interrupt

It is possible for the DMA to reach the end of its Descriptor chain while removing Receive FIFO data. When this happens, the processor is forced to take over because the DMA can no longer service the Enhanced SSP request until a new chain is linked. When the DMA has reached the end of its Descriptor chain, and there is data in the receive FIFO, the Enhanced SSP will do the following:

- Sets the peripheral trailing byte interrupt SSSR.PINT bit to 1
- Asserts the Enhanced SSP Interrupt to signal to the processor that a Peripheral Trailing Byte Interrupt condition has occurred (if SSCR1.PINTE=1 to enable the interrupt).
- Sets the SSSR.EOC status bit which must be cleared by software. If more data is received after the EOC bit was set (and EOC bit is still set), then the SSSR.PINT bit will be set to a 1.

Once the SSSR.PINT bit is set, it must be cleared by software by writing a 1 to it. Clearing the SSSR.PINT bit also de-asserts the Peripheral Interrupt if it has been enabled (SSCR1.PINTE=1).

The remaining bytes must then be removed by means of a processor I/O as described in the processor-based method below, or by reprogramming a new Descriptor chain and restarting the DMA. Programmers need to be aware of this possibility. Refer to the DMA chapter for details on Descriptor programming and “end of chain” events.

16.7.2.3 Removing Trailing Bytes (Processor Based SSCR1.TRAIL=0)

This is the default method indicated by a zero in the SSCR1.TRAIL bit. In this case, no Receive DMA service request is generated. To read out the trailing bytes, software should wait for the timeout Interrupt and then read all remaining entries as indicated by the SSSR.RFL and SSSR.RNE bits within the Enhanced SSP Status register (SSSR).

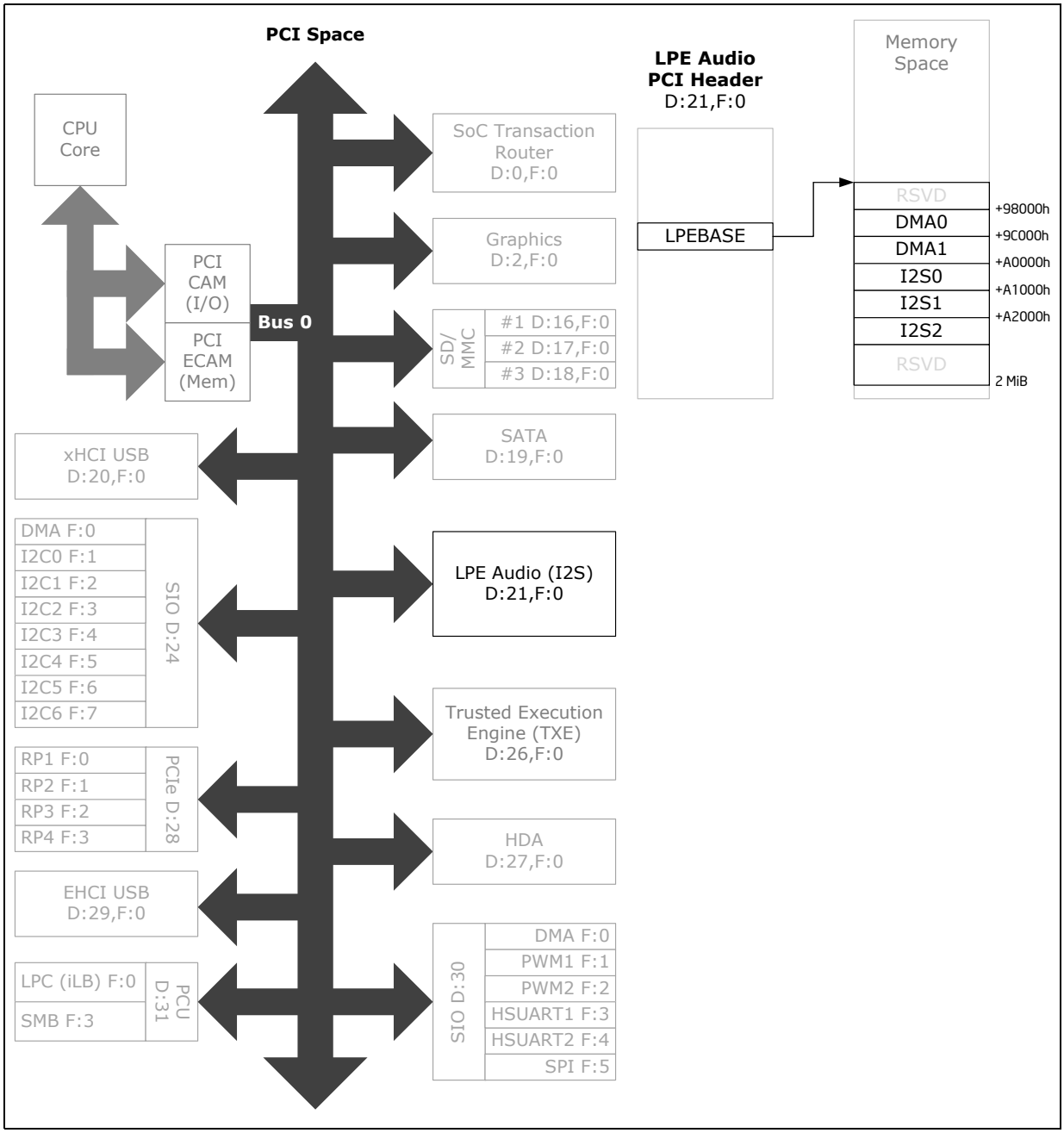
Note: To use the Trailing bytes feature through the CPU, the Timeout Interrupt must be enabled by setting SSCR1.TINTE=1 (to enable the interrupt).

16.7.2.4 Removing Trailing Bytes (DMA Based SSCR1.TRAIL=1)

When the DMA is to handle trailing bytes (SSCR1.TRAIL = 1) a DMA service request is automatically issued for the remaining number of samples left in the Receive buffer. The DMA will then empty the contents of the Receive buffer unless the DMA reaches the end of its Descriptor chain. If a timeout occurs, the processor is only interrupted by means of a Timeout Interrupt if it has been enabled by setting SSCR1.TINTE=1. When handling trailing bytes by means of the DMA, if a timeout occurs and the receive FIFO is empty, an End-of-Receive (EOR) will be sent to the DMA Controller. If an EOC occurs at the time that the last sample is read out of the FIFO (the DMA descriptor chain was just exactly long enough), and the timeout counter is still running (that is, a time out has not occurred and the SSTO register is non-zero), then, when the time out does occur, the Enhanced SSP will generate a DMA request which will create an RAS interrupt from the DMA. When this occurs, software must re-program the DMA registers and re-enable the channel for the Enhanced SSP to send its EOR to the DMA controller.

16.8 Register Map

Figure 26. Low Power Engine for Audio Register Map



§

17 Intel® Trusted Execution Engine (Intel® TXE)

This section describes the security components and capabilities. The security system contains an Intel® TXE and additional hardware security feature that enable a secure and robust platform.

Note: TXE firmware is required on the Platform as part of the PCU SPI flash image.

17.1 Features

17.1.1 Security Feature

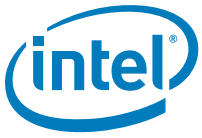
The Intel® TXE in the processor is responsible for supporting and handling security related features.

Intel TXE features:

- 32-bit RISC processor
- 256KB Data/Code RAM accessible only to the Intel® TXE
- 128KB On Chip Mask ROM for storage of Intel® TXE code
- Common Timer 1-100 µS granularity, configurable interrupt (under FW control)
- Inter-Processor Communication for message passing between the Host CPU and Intel® TXE
- 64 byte input and output command buffers
- 256 byte shared payload (enables 2048-bit keys to be exchanged as part of the command)
- No Host CPU address domain access to the Intel® TXE address domain by any Host CPU address domain units
- Security controller has direct access to Host CPU address domain (Some Restrictions Apply). Multiple context DMA engine to transfer data between Host CPU address domain (System memory) and the Intel® TXE; programmable by the Intel® TXE CPU only.
- One multi-tiered FW Key Ladder and one Intel Key ladder.
- Paging DMA operations includes encryption/decryption and integrity check value (ICV) calculation. Auxiliary GPIOs to support input alert and two GP Outputs.

17.1.1.1 HW Accelerators

- DES/3DES (ECB, CBC) – 128b ABA key for 3DES Key Ladder Operations
- Three AES engines - Two fast -128 and one slow- 128/256



- Exponentiation Acceleration Unit (EAU) for modular exponentiation, modular reduction, large number addition, subtraction, and multiplication
- SHA1, SHA256/384/512, MD5

17.1.1.2 FW Utilities and Ciphers

- RSA (with EAU acceleration)
- Flash Write Enable/Disable
- Comprehensive IPC Command Set
- Chip Unique Key encryption key wrapping of other platform keys (Flash)

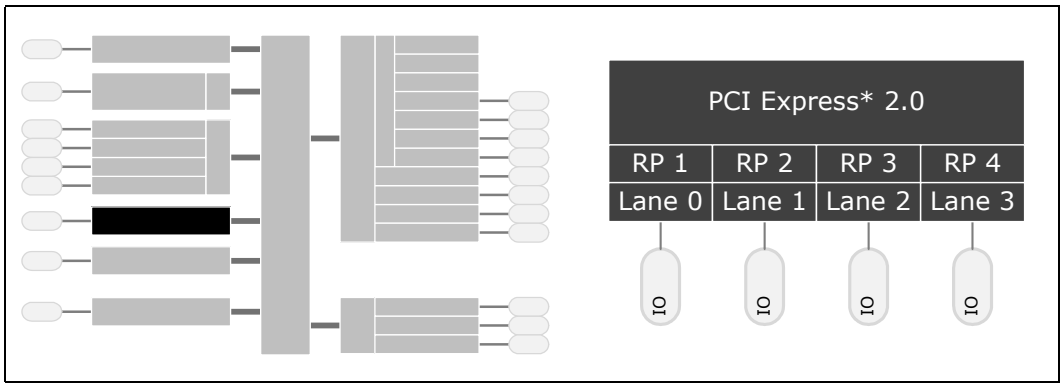
17.1.1.3 Downloadable FW Utilities and Ciphers

- One Time Programmable (OTP)

§

18 PCI Express* 2.0

There are four lanes and up to four PCI Express root ports, each supporting the *PCI Express* Base Specification*, Rev. 2.0 at a maximum 5 GT/s signaling rate. The root ports can be configured to support a diverse set of lane assignments.



18.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

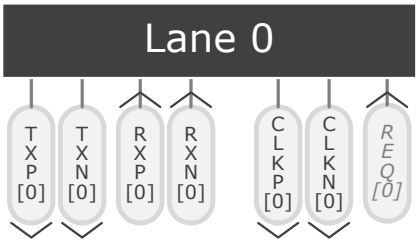
- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Note: PMC_WAKE_PCIE[3:0]# are not listed, but can be used by PCI Express* devices. Please see Section 20, "PCU – Power Management Controller (PMC)" on page 978 for details.

Table 130. Signals

Signal Name	Direction/ Type	Description
PCIE_TXP[3:0] PCIE_TXN[3:0]	O PCIe	PCI Express* Transmit PCI Express* Ports 3:0 transmit pair (P and N) signals. Each pair makes up the transmit half of a lane.
PCIE_RXP[3:0] PCIE_RXN[3:0]	I PCIe	PCI Express* Receive: PCI Express* Ports 3:0 receive pair (P and N) signals. Each pair makes up the receive half of lane.
PCIE_CLKP[3:0] PCIE_CLKN[3:0]	O PCIe	PCI Express* Output Clock 100-MHz differential clock signals.
PCIE_CLKREQ[3:0]#	I CMOS_1P8	PCI Express* Clock Request Used for devices that need to request one of the four output clocks. Each clock request maps to the matching clock output (e.g., PCI_CLKREQ[0] maps to PCIE_CLKP/N[0]). *These signals are muxed and may be used by other functions.*
PCIE_RCOMP_P PCIE_RCOMP_N	I/O	These pins are used to connect the external resistors used for Rcomp.

Figure 27. PCIe* 2.0 Lane 0 Signal Example



18.2 Features

- Conforms to *PCI Express* Base Specification*, Rev. 2.0
- 5.0 or 2.5 GT/s operation per root port
- Virtual Channel support for VC0
- x1, x2 and x4 link widths (auto negotiated)
- Flexible Root Port (1-4) configuration options
  - — (4) x1's
  - — (2) x2's
  - — (1) x2 plus (2) x1's
  - — (1) x4
- Interrupts and Events
  - — Legacy (INT*x*) and MSI Interrupts
  - — General Purpose Events

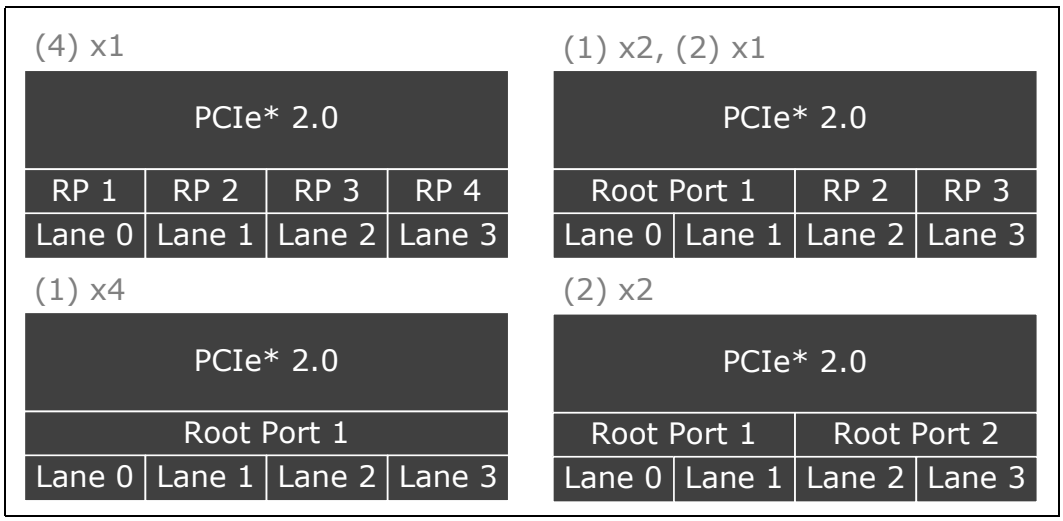
- Express Card Hot Plug Events
- System Error Events

- Power Management
  - Link State support for L0s, L1 and L2
  - Powered down in ACPI S3 state - L3

18.2.1 Root Port Configurations

Depending on SKU, there are up to four possible lane assignments for root ports 1-4.

Figure 28. Root Port Configuration Options



Root port configurations are set by SoftStraps stored in SPI flash, and the default option is "(4) x1". Links for each root port will train automatically to the maximum possible for each port.

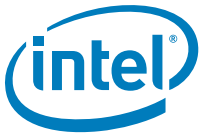
Note: x2 link widths are not common. Most devices will only train to x1 or x4.

Note: PCI functions in PCI configuration space are disabled for root ports not available.

18.2.2 Interrupts and Events

A root port is capable of handling interrupts and events from an end point device. A root port can also generate its own interrupts for some events, including power management and hot plug events, but also including error events.

There are two interrupt types a root port will receive from an end point device: INTx (legacy), and MSI. MSI's are automatically passed upstream by the root port, just as other memory writes would be. INTx messages are delivered to the Legacy block's interrupt router/controller by the root port.



Events and interrupts that are handled by the root port are shown with the possible interrupts they can deliver to the interrupt decoder/router.

Table 131. Possible Interrupts Generated From Events/Packets

Packet/Event	Type	INTx	MSI	SERR	SCI	SMI	GPE
INTx	Packet	X	X				
PM_PME	Packet	X	X				
Power Management (PM)	Event	X	X		X	X	
Hot Plug (HP)	Event	X	X		X	X	
ERR_CORR	Packet			X			
ERR_NONFATAL	Packet			X			
ERR_FATAL	Packet			X			
Internal Error	Event			X			
VDM	Packet						X

Note: Table 131 lists the possible interrupts and events generated based on Packets received, or events generated in the root port. Configuration needed by software to enable the different interrupts as applicable.

When INTx interrupts are received by an end point, they are mapped to the following interrupts and sent to the interrupt decoder/router in the iLB:

Table 132. Interrupt Generated for INT[A-D] Interrupts

	INTA	INTB	INTC	INTD
Root Port 1	INTA#	INTB#	INTC#	INTD#
Root Port 2	INTD#	INTA#	INTB#	INTC#
Root Port 3	INTC#	INTD#	INTA#	INTB#
Root Port 4	INTB#	INTC#	INTD#	INTA#

Note: Interrupts generated from events within the root port are not swizzled.

18.2.2.1 Express Card Hot Plug Events

Express Card Hot Plug is available based on Presence Detection for each root port.

Note: A full Hot Plug Controller is not implemented.

Presence detection occurs when a PCI Express* device is plugged in and power is supplied. The physical layer will detect the presence of the device, and the root port will set the SLSTS.PDS and SLSTS.PDC bits.

When a device is removed and detected by the physical layer, the root port will clear the SLSTS.PDS bit, and set the SLSTS.PDC bit.

Interrupts can be generated by the root port when a hot plug event occurs. A hot plug event is defined as the transition of the SLSTS.PDC bit from 0 to 1. Software can set the SLCTL.PDE and SLTCTL.HPE bits to allow hot plug events to generate an interrupt.

If SLCTL.PDE and SLTCTL.HPE are both set, and STSTS.PDC transitions from 0 to 1, an interrupt will be generated.

18.2.2.2 System Error (SERR)

System Error events are support by both internal and external sources. See the PCI Express* Base Specification, Revision 2.0 for details.

18.2.3 Power Management

Each root port's link supports L0s, L1, and L2/3 link states per PCI Express* Base Specification, Revision 2.0. L2/3 is entered on entry to S3.

18.3 References

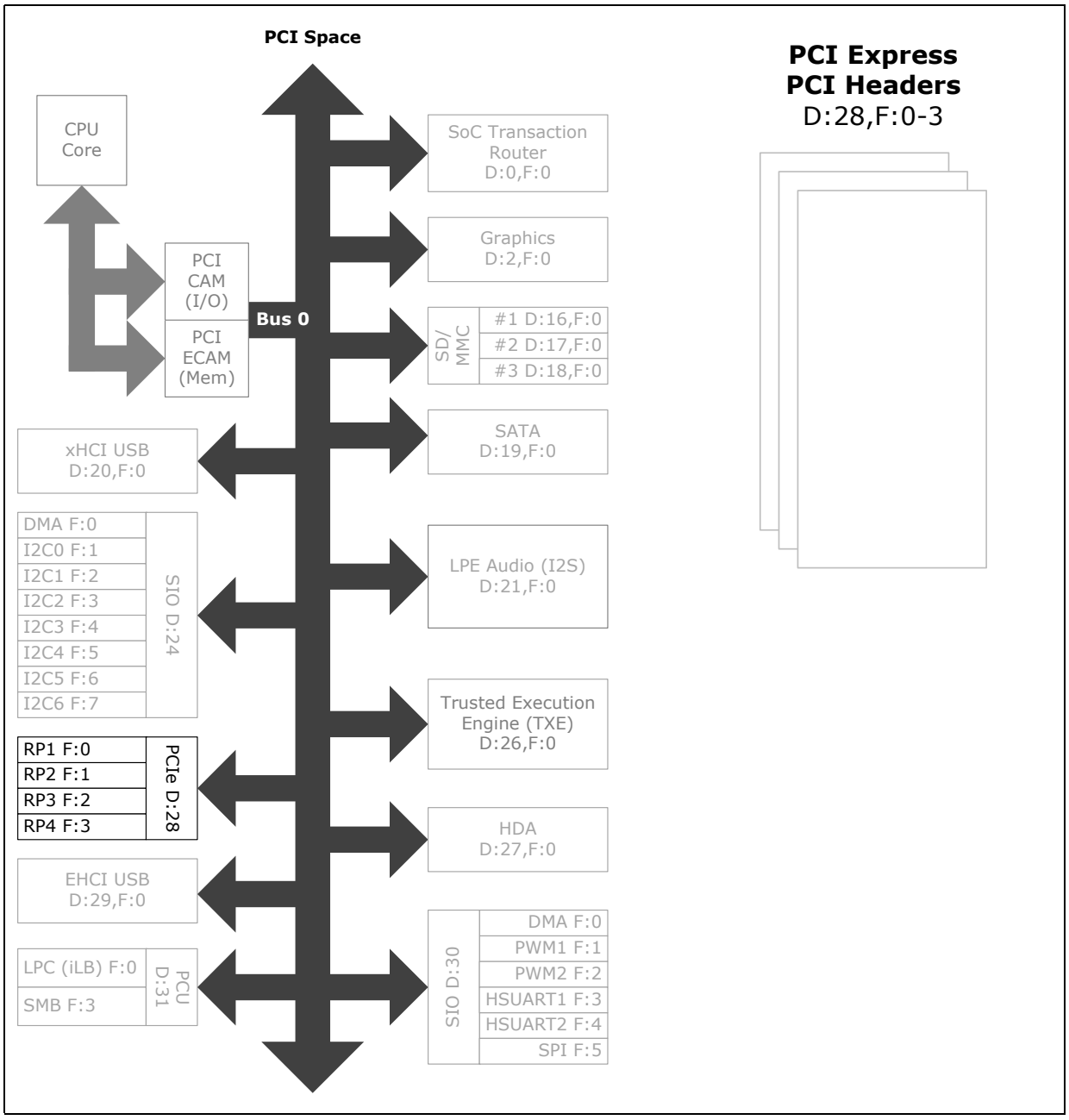
PCI Express Base Specification*, Rev. 2.0

18.4 Register Map

Each root port supports its own extended PCI bridge header in PCI configuration space. These headers are located on PCI bus 0, device 28, functions 0-32 as shown below. There are no other registers implemented by the root ports or their controller.

See Chapters 3 and 4 for additional information.

Figure 29. PCI Express Register Map



18.5 PCI Configuration Registers

Registers listed are for function 0 (root port 1). All other root ports contain the same registers. Differences for other root ports (functions 1-32) will be noted in individual registers.

18.6 PCI Express* PCI Configuration Registers

Table 133. Summary of PCI Express* PCI Configuration Registers—0/28/0

Offset	Size	Register ID—Description	Default Value
0h	4	"Identifiers (ID)—Offset 0h" on page 727	00008086h
4h	4	"Device Command; Primary Status (CMD_PSTS)—Offset 4h" on page 728	00100000h
8h	4	"Revision ID;Class Code (RID_CC)—Offset 8h" on page 730	06040000h
Ch	4	"Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch" on page 730	00810000h
18h	4	"Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h" on page 731	00000000h
1Ch	4	"I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch" on page 732	00000000h
20h	4	"Memory Base and Limit (MBL)—Offset 20h" on page 733	00000000h
24h	4	"Prefetchable Memory Base and Limit (PMBL)—Offset 24h" on page 734	00010001h
28h	4	"Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h" on page 735	00000000h
2Ch	4	"Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch" on page 735	00000000h
34h	4	"Capabilities List Pointer (CAPP)—Offset 34h" on page 736	00000040h
3Ch	4	"Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch" on page 737	00000000h
40h	4	"Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h" on page 738	00428010h
44h	4	"Device Capabilities (DCAP)—Offset 44h" on page 739	00008000h
48h	4	"Device Control; Device Status (DCTL_DSTS)—Offset 48h" on page 740	00100000h
4Ch	4	"Link Capabilities (LCAP)—Offset 4Ch" on page 741	00310C02h
50h	4	"Link Control; Link Status (LCTL_LSTS)—Offset 50h" on page 743	00010000h
54h	4	"Slot Capabilities (SLCAP)—Offset 54h" on page 745	00040060h
58h	4	"Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h" on page 746	00000000h
5Ch	4	"Root Control (RCTL)—Offset 5Ch" on page 747	00000000h
60h	4	"Root Status (RSTS)—Offset 60h" on page 748	00000000h
64h	4	"Device Capabilities 2 (DCAP2)—Offset 64h" on page 748	00080816h
68h	4	"Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h" on page 749	00000000h
6Ch	4	"Link Capabilities 2 (LCAP2)—Offset 6Ch" on page 750	00000000h
70h	4	"Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h" on page 751	00000000h
74h	4	"Slot Capabilities 2 (SLCAP2)—Offset 74h" on page 752	00000000h
78h	4	"Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h" on page 753	00000000h
80h	4	"Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h" on page 753	00009005h
84h	4	"Message Signaled Interrupt Message Address (MA)—Offset 84h" on page 754	00000000h
88h	4	"Message Signaled Interrupt Message Data (MD)—Offset 88h" on page 754	00000000h
90h	4	"Subsystem Vendor Capability (SVCAP)—Offset 90h" on page 755	0000A00Dh
94h	4	"Subsystem Vendor IDs (SVID)—Offset 94h" on page 755	00000000h
A0h	4	"Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h" on page 756	C8030001h
A4h	4	"PCI Power Management Control And Status (PMCS)—Offset A4h" on page 757	00000000h

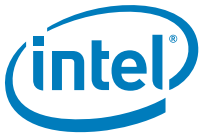


Table 133. Summary of PCI Express* PCI Configuration Registers—0/28/0 (Continued)

Offset	Size	Register ID—Description	Default Value
F8h	4	"Manufacturer's ID (MANID)—Offset F8h" on page 758	00000F00h
100h	4	"Advanced Error Reporting Capability Header (AECH)—Offset 100h" on page 758	00000000h
104h	4	"Uncorrectable Error Status (UES)—Offset 104h" on page 759	00000000h
108h	4	"Uncorrectable Error Mask (UEM)—Offset 108h" on page 760	00000000h
10Ch	4	"Uncorrectable Error Severity (UEV)—Offset 10Ch" on page 761	00060011h
110h	4	"Correctable Error Status (CES)—Offset 110h" on page 762	00000000h
114h	4	"Correctable Error Mask (CEM)—Offset 114h" on page 763	00002000h
118h	4	"Advanced Error Capabilities and Control (AECC)—Offset 118h" on page 764	00000000h
11Ch	4	"Header Log DW1 (HL_DW1)—Offset 11Ch" on page 765	00000000h
120h	4	"Header Log DW2 (HL_DW2)—Offset 120h" on page 765	00000000h
124h	4	"Header Log DW3 (HL_DW3)—Offset 124h" on page 766	00000000h
128h	4	"Header Log DW4 (HL_DW4)—Offset 128h" on page 766	00000000h
12Ch	4	"Root Error Command (REC)—Offset 12Ch" on page 767	00000000h
130h	4	"Root Error Status (RES)—Offset 130h" on page 767	00000000h
134h	4	"Error Source Identification (ESID)—Offset 134h" on page 768	00000000h
328h	4	"PCI Express Status 1 (PCIESTS1)—Offset 328h" on page 769	00000000h
32Ch	4	"PCI Express Status 2 (PCIESTS2)—Offset 32Ch" on page 770	00000000h
330h	4	"PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h" on page 771	28000016h
334h	4	"PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h" on page 772	4ABCB5BCh

18.6.1 Identifiers (ID)—Offset 0h

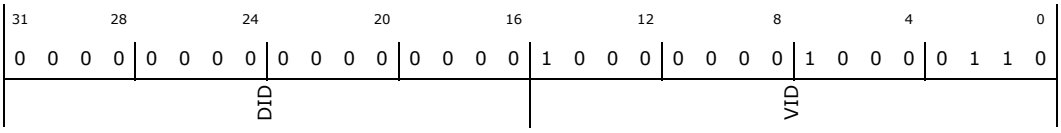
Access Method

Type: PCI Configuration Register (Size: 32 bits)

ID: [B:0, D:28, F:0] + 0h

Power Well: Core

Default: 00008086h



Bit Range	Default & Access	Description
31:16	0000h RO/V	**Device Identification (DID):** The value of this ID is product specific.
15:0	8086h RO	**Vendor Identification (VID):** Indicates Intel

18.6.2 Device Command; Primary Status (CMD_PSTS)—Offset 4h

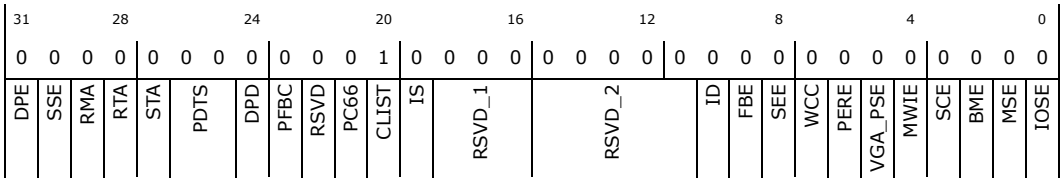
Access Method

Type: PCI Configuration Register (Size: 32 bits)

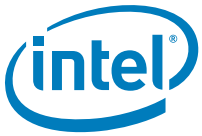
CMD_PSTS: [B:0, D:28, F:0] + 4h

Power Well: Core

Default: 00100000h



Bit Range	Default & Access	Description
31	0b RW/C	**DPE Detected Parity Error (DPE):** Set when the root port receives a command or data from the backbone with a parity error. This is set even if CMD.PERE is not set.
30	0b RW/C	**Signaled System Error (SSE):** Set when the root port signals a system error to the internal SERR# logic.
29	0b RW/C	**Received Master Abort (RMA):** Set when the root port receives a completion with unsupported request status from the backbone.
28	0b RW/C	**Received Target Abort (RTA):** Set when the root port receives a completion with completer abort from the backbone.
27	0b RW/C	**Signaled Target Abort (STA):** Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
26:25	00b RO	**Primary DEVSEL# Timing Status (PDTS):** Reserved per PCI-Express spec
24	0b RW/C	**Master Data Parity Error Detected (DPD):** Set when the root port receives a completion with a data parity error on the backbone and CMD.PERE is set.
23	0b RO	**Primary Fast Back to Back Capable (PFBC):** Reserved per PCI-Express spec.
22	0b RO	**Reserved (RSVD):** Reserved
21	0b RO	**Primary 66 MHz Capable (PC66):** Reserved per PCI-Express spec.
20	1b RO	**Capabilities List (CLIST):** Indicates the presence of a capabilities list.
19	0b RO/V	**Interrupt Status (IS):** Indicates status of hot plug and power management interrupts on the root port that result in INTx# message generation. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of CMD.ID.
18:16	000b RO	**Reserved (RSVD_1):** Reserved
15:11	00h RO	**Reserved (RSVD_2):** Reserved



Bit Range	Default & Access	Description
10	0b RW/V	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts on enabled hot plug and power management events. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt for hot plug or power management and MSI is not enabled. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set. For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register is RO and returns a value of 0 when read, else it is RW with the functionality described above.
9	0b RO	**Fast Back to Back Enable (FBE):** Reserved per PCI-Express spec.
8	0b RW	**SERR# Enable (SEE):** When set, enables the root port to generate an SERR# message when PSTS.SSE is set.
7	0b RO	**Wait Cycle Control (WCC):** Reserved per PCI-Express spec.
6	0b RW	**Parity Error Response Enable (PERE):** Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	0b RO	**VGA Palette Snoop (VGA_PSE):** Reserved per PCI-Express spec.
4	0b RO	**Memory Write and Invalidate Enable (MWIE):** Reserved per PCI-Express spec.
3	0b RO	**Special Cycle Enable (SCE):** Reserved per PCI-Express and PCI bridge spec.
2	0b RW	**Bus Master Enable (BME):** When set, allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI-Express device. When this bit is 0b, Memory and I/O requests received at a Root Port must be handled as Unsupported Requests (UR). This bit does not affect forwarding of Completions in either the Upstream or Downstream direction. The forwarding of Requests other than Memory or I/O requests is not controlled by this bit.
1	0b RW	**Memory Space Enable (MSE):** When set, memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI-Express device. When cleared, these memory cycles are master aborted on the backbone.
0	0b RW	**I/O Space Enable (IOSE):** When set, I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI-Express device. When cleared, these cycles are master aborted on the backbone..

18.6.3 Revision ID;Class Code (RID_CC)—Offset 8h

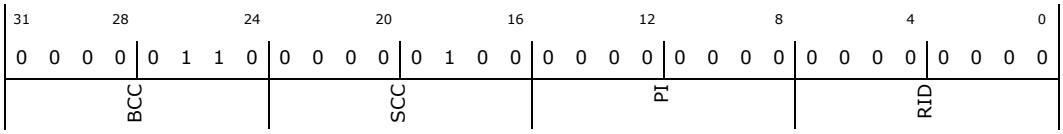
Access Method

Type: PCI Configuration Register (Size: 32 bits)

RID_CC: [B:0, D:28, F:0] + 8h

Power Well: Core

Default: 06040000h



Bit Range	Default & Access	Description
31:24	06h RO	**Base Class Code (BCC):** Indicates the device is a bridge device.
23:16	04h RO/V	**Sub-Class Code (SCC):** The default indicates the device is a PCI-to-PCI bridge.
15:8	00h RO/V	**Programming Interface (PI):** The value reported in this register is a function of the Decode Control.Subtractive Decode Enable (SDE) register. SDE Value reported in this register 0: 00h 1: 01h
7:0	00h RO/V	**Revision ID (RID):** Indicates the revision of the bridge.

18.6.4 Cache Line Size; Primary Latency Timer; Header Type (CLS_PLT_HTYPE)—Offset Ch

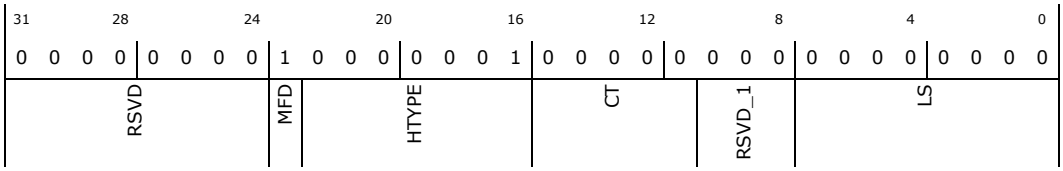
Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLS_PLT_HTYPE: [B:0, D:28, F:0] + Ch

Power Well: Core

Default: 00810000h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved (RSVD):** Reserved
23	1b RO	**Multi-function Device (MFD):** This bit is '1' to indicate a multi-function device.
22:16	01h RO/V	**Header Type (HTYPE):** The default mode identifies the header layout of the configuration space, which is a PCI-to-PCI bridge.
15:11	00h RO	**Latency Count (CT):** Reserved per PCI-Express spec

Bit Range	Default & Access	Description
10:8	000b RO	**Reserved (RSVD_1):** Reserved
7:0	00h RW	**Line Size (LS):** This is read/write but contains no functionality, per PCI-Express spec

18.6.5 Bus Numbers; Secondary Latency Timer (BNUM_SLT)—Offset 18h

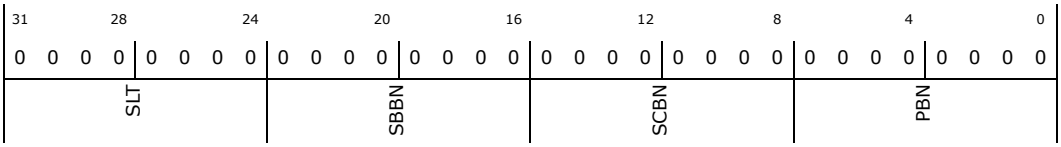
Access Method

Type: PCI Configuration Register (Size: 32 bits)

BNUM_SLT: [B:0, D:28, F:0] + 18h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RW/V	**Secodary Latency Timer (SLT):** For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is a RW register; else this register is RO and returns 0. This register does not affect the behavior of any HW logic.
23:16	00h RW	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.
15:8	00h RW	**Secondary Bus Number (SCBN):** Indicates the bus number the port.
7:0	00h RW	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

18.6.6 I/O Base and Limit; Secondary Status (IOBL_SSTS)—Offset 1Ch

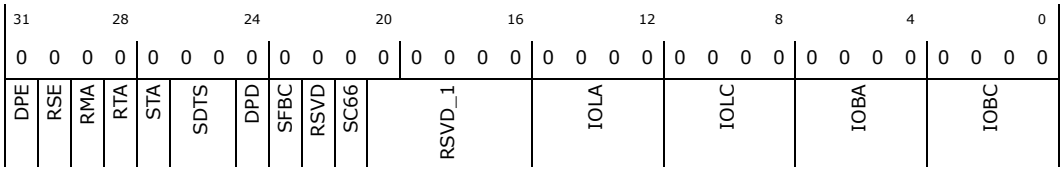
Access Method

Type: PCI Configuration Register (Size: 32 bits)

IOBL_SSTS: [B:0, D:28, F:0] + 1Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/C	**Detected Parity Error (DPE):** Set when the port receives a poisoned TLP.
30	0b RW/C	**Received System Error (RSE):** Set when the port receives an ERR_FATAL or ERR_NONFATAL message from the device.
29	0b RW/C	**Received Master Abort (RMA):** Set when the port receives a completion with 'Unsupported Request' status from the device.
28	0b RW/C	**Received Target Abort (RTA):** Set when the port receives a completion with 'Completion Abort' status from the device.
27	0b RW/C	**Signaled Target Abort (STA):** Set when the port generates a completion with 'Completion Abort' status to the device.
26:25	00b RO/V	**Secondary DEVSEL# Timing Status (SDTS):** Reserved per PCI-Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 01b when read, else this register returns a value of 00b.
24	0b RW/C	**Data Parity Error Detected (DPD):** Set when the BCTRL.PERE, and either of the following two conditions occurs: Port receives completion marked poisoned. Port poisons a write request to the secondary side.
23	0b RO/V	**Secondary Fast Back to Back Capable (SFBC):** Reserved per PCI Express spec For PCI Bus Emulation Mode compatibility, if the PCIBEM register is set, this register returns a value of 1b when read, else this register returns a value of 0b.
22	0b RO	**Reserved (RSVD):** Reserved
21	0b RO	**Secondary 66 MHz Capable (SC66):** Reserved per PCI Express spec
20:16	00h RO	**Reserved (RSVD_1):** Reserved
15:12	0h RW	**I/O Address Limit (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	0h RO	**I/O Limit Address Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.
7:4	0h RW	**I/O Base Address (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	0h RO	**I/O Base Address Capability (IOBC):** Indicates that the bridge does not support 32-bit I/O addressing.

18.6.7 Memory Base and Limit (MBL)—Offset 20h

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is MB [gt]= AD[lb]31:20[rb] [lt]= ML.

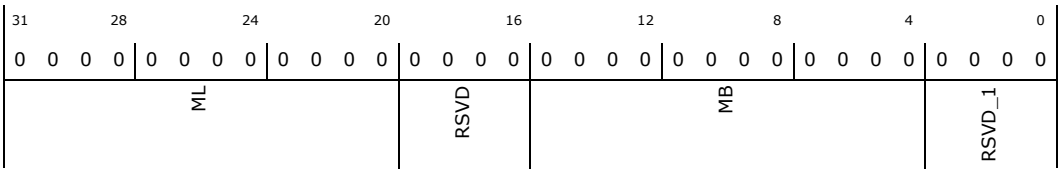
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MBL: [B:0, D:28, F:0] + 20h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:20	000h RW	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	0h RO	**Reserved (RSVD):** Reserved
15:4	000h RW	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	0h RO	**Reserved (RSVD_1):** Reserved

18.6.8 Prefetchable Memory Base and Limit (PMBL)—Offset 24h

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME is set. The comparison performed is PMBU32:PMB [gt]= AD[lb]63:32[rb]:AD[lb]31:20[rb] [lt]= PMLU32:PML.

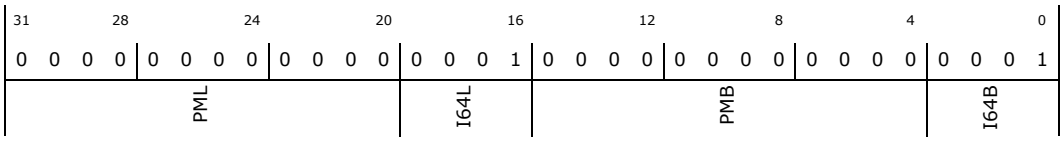
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMBL: [B:0, D:28, F:0] + 24h

Power Well: Core

Default: 00010001h



Bit Range	Default & Access	Description
31:20	000h RW	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	1h RO	**64-bit Indicator (I64L):** Indicates support for 64-bit addressing.
15:4	000h RW	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	1h RO	**64-bit Indicator (I64B):** Indicates support for 64-bit addressing.

18.6.9 Prefetchable Memory Base Upper 32 Bits (PMBU32)—Offset 28h

Size:32 bits

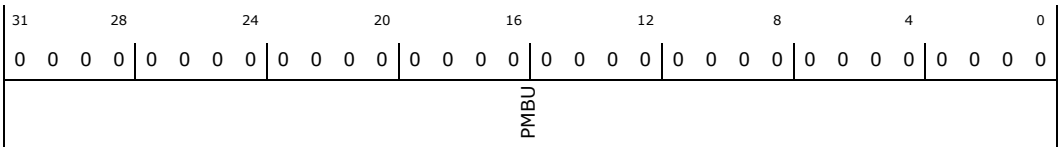
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMBU32: [B:0, D:28, F:0] + 28h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

18.6.10 Prefetchable Memory Limit Upper 32 Bits (PMLU32)—Offset 2Ch

Size:32 bits

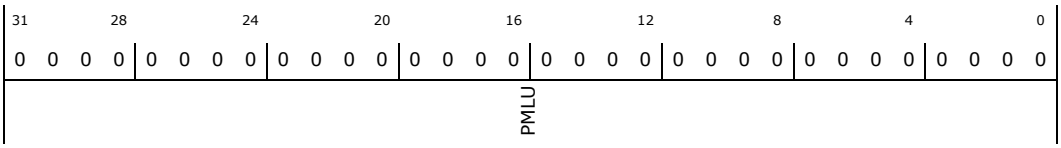
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMLU32: [B:0, D:28, F:0] + 2Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

18.6.11 Capabilities List Pointer (CAPP)—Offset 34h

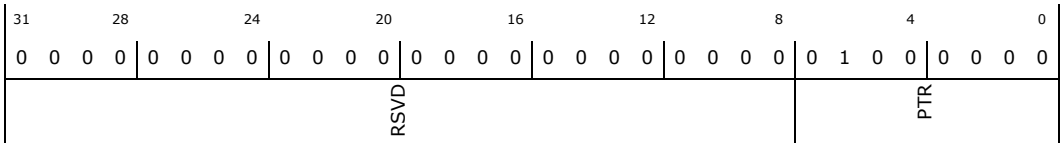
Access Method

Type: PCI Configuration Register (Size: 32 bits)

CAPP: [B:0, D:28, F:0] + 34h

Power Well: Core

Default: 00000040h



Bit Range	Default & Access	Description
31:8	000000h RO	**Reserved (RSVD):** Reserved
7:0	40h RW/O	**Capabilities Pointer (PTR):** Indicates that the pointer for the first entry in the capabilities list. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value. Capability Linked List (Default Settings) Offset Capability Next Pointer 40h PCI Express 80h 80h Message Signaled Interrupt (MSI) 90h 90h Subsystem Vendor A0h A0h PCI Power Management 00h Extended PCIe Capability Linked List Offset Capability Next Pointer 100h Advanced Error Reporting 000h

18.6.12 Interrupt Information; Bridge Control (INTR_BCTRL)—Offset 3Ch

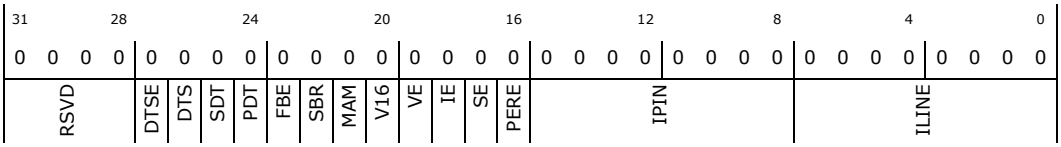
Access Method

Type: PCI Configuration Register (Size: 32 bits)

INTR_BCTRL: [B:0, D:28, F:0] + 3Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27	0b RW/V	**Discard Timer SERR# Enable (DTSE):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
26	0b RO	**Discard Timer Status (DTS):** Reserved per PCI-Express spec. For PCI Bus Emulation Mode compatibility, this register can remain RO as no secondary discard timer exists that will ever cause it to be set.
25	0b RW/V	**Secondary Discard Timer (SDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
24	0b RW/V	**Primary Discard Timer (PDT):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
23	0b RO	**Fast Back to Back Enable (FBE):** Reserved per Express spec.
22	0b RW	**Secondary Bus Reset (SBR):** Triggers a Hot Reset on the PCI-Express port.
21	0b RW/V	**Master Abort Mode (MAM):** Reserved per Express spec. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register is RW else it is RO. This register is only maintained for SW compatibility and has no functionality within the port.
20	0b RW	**VGA 16-Bit Decode (V16):** When set, indicates that the I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled. 0: Execute 10-bit address decode on VGA I/O accesses. 1: Execute 16-bit address decode on VGA I/O accesses.
19	0b RW	**VGA Enable (VE):** When set, the following ranges will be claimed off the backbone by the root port: Memory ranges A0000h-BFFFFh I/O ranges 3B0h 3BBh and 3C0h 3DFh, and all aliases of bits 15:10 in any combination of 1's
18	0b RW	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. If this bit is set, the root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
17	0b RW	**SERR# Enable (SE):** When set, ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone. When cleared, they are not.
16	0b RW	**Parity Error Response Enable (PERE):** When set, poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD.

Bit Range	Default & Access	Description
15:8	00h RO/V	**Interrupt Pin (IPIN):** Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values, which reflect the reset state of the STRPFUSECFG register in chipset config space: Port Bits[lb]15:12[rb] Bits[lb]11:08[rb] 1 0h STRPFUSECFG.P1IP 2 0h STRPFUSECFG.P2IP 3 0h STRPFUSECFG.P3IP 4 0h STRPFUSECFG.P4IP 5 0h STRPFUSECFG.P5IP 6 0h STRPFUSECFG.P6IP 7 0h STRPFUSECFG.P7IP 8 0h STRPFUSECFG.P8IP The value that is programmed into STRPFUSECFG is always reflected in this register. For PCI Bus Emulation Mode compatibility, if the DC.PCIBEM register is set, this register returns a value of 00h when read, else this register returns the value from the table above.
7:0	00h RW	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

18.6.13 Capabilities List; PCI Express Capabilities (CLIST_XCAP)—Offset 40h

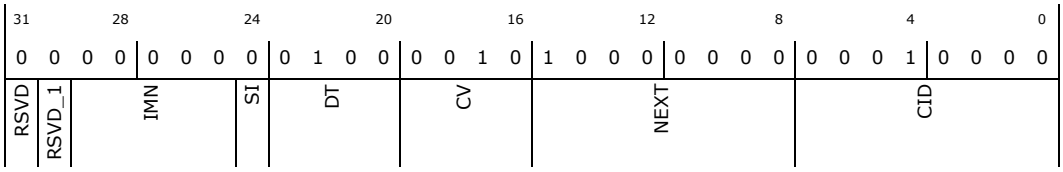
Access Method

Type: PCI Configuration Register (Size: 32 bits)

CLIST_XCAP: [B:0, D:28, F:0] + 40h

Power Well: Core

Default: 00428010h



Bit Range	Default & Access	Description
31	0b RO	**Reserved (RSVD):** Reserved
30	0b RO	**Reserved (RSVD_1):** Reserved. This register at one time was for TCS Routing but that was later removed from the PCIe 2.0 spec
29:25	00h RO	**Interrupt Message Number (IMN):** The root port does not have multiple MSI interrupt numbers.
24	0b RW/O	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
23:20	4h RO	**Device / Port Type (DT):** Indicates this is a PCI-Express root port
19:16	2h RO	**Capability Version (CV):** Version 2.0 indicates devices compliant to the PCI Express 2.0 specification which incorporates the Register Expansion ECN.
15:8	80h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability. The default value of this register is 80h which points to the MSI Capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	10h RO	**Capability ID (CID):** Indicates this is a PCI Express capability

18.6.14 Device Capabilities (DCAP)—Offset 44h

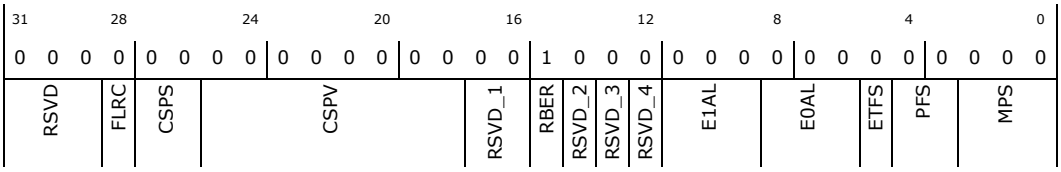
Access Method

Type: PCI Configuration Register (Size: 32 bits)

DCAP: [B:0, D:28, F:0] + 44h

Power Well: Core

Default: 00008000h



Bit Range	Default & Access	Description
31:29	000b RO	**Reserved (RSVD):** Reserved
28	0b RO	**Function Level Reset Capable (FLRC):** Not supported in Root Ports
27:26	00b RO	**Captured Slot Power Limit Scale (CSPS):** Not supported
25:18	00h RO	**Captured Slot Power Limit Value (CSPV):** Not supported
17:16	00b RO	**Reserved (RSVD_1):** Reserved
15	1b RO	**Role Based Error Reporting (RBER):** When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. This bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1., or subsequent PCI Express Base Specification revisions.
14	0b RO	**Reserved (RSVD_2):** Reserved. On previous version of the specification this was Power Indicator Present (PIP)
13	0b RO	**Reserved (RSVD_3):** Reserved. On previous version of the specification this was Attention Indicator Present (AIP)
12	0b RO	**Reserved (RSVD_4):** Reserved. On previous version of the specification this was Attention Button Present (ABP)
11:9	000b RO	**Endpoint L1 Acceptable Latency (E1AL):** Reserved for root ports.
8:6	000b RO	**Endpoint L0 Acceptable Latency (E0AL):** Reserved for Root port.
5	0b RO	**Extended Tag Field Supported (ETFS):** The root port never needs to initiate a transaction as a Requester with the Extended Tag bits being set. This bit does not affect the root port's ability to forward requests as a bridge as the root port always supports forwarding requests with extended tags.
4:3	00b RO	**Phantom Functions Supported (PFS):** No phantom functions supported

Bit Range	Default & Access	Description
2:0	000b RW/O	**Max Payload Size Supported (MPS):** BIOS should write to this field during system initialization. Only Max Payload Size of 128B is supported. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface.

18.6.15 Device Control; Device Status (DCTL_DSTS)—Offset 48h

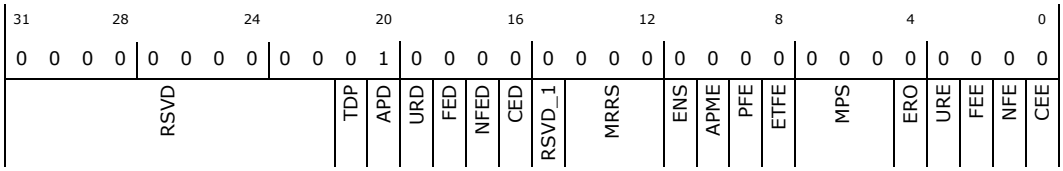
Access Method

Type: PCI Configuration Register (Size: 32 bits)

DCTL_DSTS: [B:0, D:28, F:0] + 48h

Power Well: Core

Default: 00100000h



Bit Range	Default & Access	Description
31:22	000h RO	**Reserved (RSVD):** Reserved
21	0b RO	**Transactions Pending (TDP):** This bit has no meaning for the root port since it never initiates a non-posted request with its own Requester ID.
20	1b RO	**AUX Power Detected (APD):** The root port contains AUX power for wakeup
19	0b RW/C	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
18	0b RW/C	**Fatal Error Detected (FED):** Indicates a fatal error was detected. Set when a fatal error occurred on from a data link protocol error, buffer overflow, or malformed tlp
17	0b RW/C	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. Set when an received a non-fatal error occurred from a poisoned tlp, unexpected completions, unsupported requests, completor abort, or completer timeout
16	0b RW/C	**Correctable Error Detected (CED):** Indicates a correctable error was detected. Set when received an internal correctable error from receiver errors / framing errors, tlp crc error, dllp crc error, replay num rollover, replay timeout.
15	0b RO	**Reserved (RSVD_1):** Reserved
14:12	000b RO	**Max Read Request Size (MRRS):** Hardwired to 0. This field applies only to the PCIe link interface.
11	0b RO	**Enable No Snoop (ENS):** Not supported. The root port will never issue non-snoop requests.
10	0b RW/P	**Aux Power PM Enable (APME):** The OS will set this bit to '1' if the device connected has detected aux power.

Bit Range	Default & Access	Description
9	0b RO	**Phantom Functions Enable (PFE):** Not supported
8	0b RO	**Extended Tag Field Enable (ETFE):** Not supported
7:5	000b RW	**Max Payload Size (MPS):** The root port only supports 128B max payload. Programming this field to any values other than 128B max payload size will result in aliasing to 128B max payload size. If the DCAP.MPS indicates 128B max payload size support, programming this field to any values other than 128B will result in aliasing to 128B max payload size. 000b: 128 bytes max payload size. 001b: 256 bytes max payload size. 010b: 512 bytes max payload size. 011b: 1024 bytes max payload size. 100b: 2048 bytes max payload size. 101b: 4096 bytes max payload size. 110b: Reserved. 111b: Reserved. This field applies only to the PCIe link interface. Note: Software should ensure that the system is quiescent and no TLP is in progress prior to changing this field. BIOS should program this field prior to enabling BME.
4	0b RO	**Enable Relaxed Ordering (ERO):** Not supported
3	0b RW	**Unsupported Request Reporting Enable (URE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	0b RW	**Fatal Error Reporting Enable (FEE):** enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	0b RW	**Non-Fatal Error Reporting Enable (NFE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	0b RW	**Correctable Error Reporting Enable (CEE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

18.6.16 Link Capabilities (LCAP)—Offset 4Ch

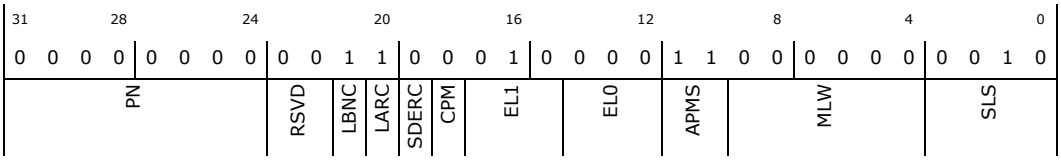
Access Method

Type: PCI Configuration Register (Size: 32 bits)

LCAP: [B:0, D:28, F:0] + 4Ch

Power Well: Core

Default: 00310C02h



Bit Range	Default & Access	Description
31:24	00h RO/V	**Port Number (PN):** Indicates the port number for the root port. This value is different for each implemented port: Port # Value of PN field 1 01h 2 02h 3 03h 4 04h

Bit Range	Default & Access	Description
23:22	00b RO	**Reserved (RSVD):** Reserved
21	1b RO	**Link Bandwidth Notification Capability (LBNC):** This port supports Link Bandwidth Notification status and interrupt mechanisms.
20	1b RO	**Link Active Reporting Capable (LARC):** This port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	0b RO	**Surprise Down Error Reporting Capable (SDERC):** Set to '0' to indicate the root port does not support Surprise Down Error Reporting
18	0b RO	**Clock Power Management (CPM):** '0' Indicates that root ports do not support the CLKREQ# mechanism.
17:15	010b RW/O	**L1 Exit Latency (EL1):** Indicates an exit latency of 2us to 4us. 000b - Less than 1 us 001b - 1 us to less than 2 us 010b - 2 us to less than 4 us 011b - 4 us to less than 8 us 100b - 8 us to less than 16 us 101b - 16 us to less than 32 us 110b - 32 us to 64 us 111b - More than 64 us Note: If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.
14:12	000b RO/V	**L0s Exit Latency (EL0):** Indicates an exit latency based upon common-clock configuration.
11:10	11b RW/O	**Active State Link PM Support (APMS):** Indicates the level of active state power management on this link Bits Definition 00 (Reserved) 01 L0s Entry supported 10 Reserved 11 Both L0s and L1 supported Note: If STRPFUSECFG.ASPMDIS is 1, the default of this field is '01'. Otherwise, the default of this field is '11'. If STRPFUSECFG.ASPMDIS is 1, BIOS writing '11' to this field will have the same effect as writing '01'. '01' will be reflected on this register when read and the register will turn to Read-Only once written once.
9:4	000000b RO/V	**Maximum Link Width (MLW):** For the root ports, several values can be taken, based upon the value of the chipset configuration register field RPC.PC1 for ports 1-4: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h
3:0	2h RO/V	**Supported Link Speeds (SLS):** Indicates the supported link speeds of the Root Port. 0001b 2.5 GT/s Link speed supported 0010b 5.0 GT/s and 2.5GT/s Link speeds supported This register reports a value of 0001b if the Root Port Gen2 Disable Fuse is set, else this register reports a value of 0010b.

18.6.17 Link Control; Link Status (LCTL_LSTS)—Offset 50h

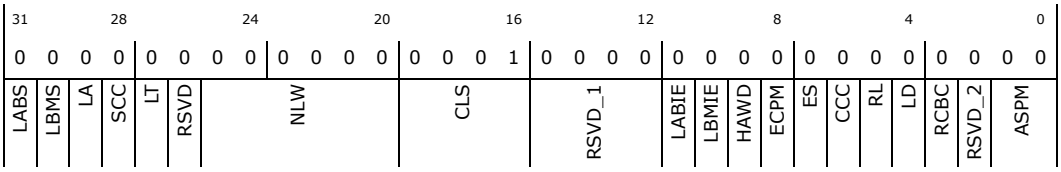
Access Method

Type: PCI Configuration Register (Size: 32 bits)

LCTL_LSTS: [B:0, D:28, F:0] + 50h

Power Well: Core

Default: 00010000h



Bit Range	Default & Access	Description
31	0b RW/C	**Link Autonomous Bandwidth Status (LABS):** This bit is Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation. This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was indicated as an autonomous change. The default value of this bit is 0b.
30	0b RW/C	**Link Bandwidth Management Status (LBMS):** This bit is Set by hardware to indicate that either of the following has occurred without the Port transitioning through DL_Down status: - A Link retraining has completed following a write of 1b to the Retrain Link bit Note: This bit is Set following any write of 1b to the Retrain Link bit, including when the Link is in the process of retraining for some other reason. - Hardware has changed Link speed or width to attempt to correct unreliable Link operation, either through an LTSSM timeout or a higher level process This bit must be set if the Physical Layer reports a speed or width change was initiated by the Downstream component that was not indicated as an autonomous change. The default value of this bit is 0b.
29	0b RO/V	**Link Active (LA):** Set to 1b when the Data Link Control and Management State Machine is in the DL_Active state, 0b otherwise.
28	0b RO/V	**Slot Clock Configuration (SCC):** In normal mode, root port uses the same reference clock as on the platform and does not generate its own clock. Note: The default of this register bit is dependent on the 'PCIe Non-Common Clock With SSC Mode Enable Strap'. If the strap enables non-common clock with SSC support, this bit shall default to '0'. Otherwise, this bit shall default to '1'.
27	0b RO/V	**Link Training (LT):** The root port sets this bit whenever link training is occurring, or that 1b was written to the Retrain Link bit but Link training has not yet begun. It clears the bit upon completion of link training.
26	0b RO	**Reserved (RSVD):** Reserved. Previously this was defined as Link Training Error (LTE) but support for this bit was removed from subsequent versions of the PCI Express specification.
25:20	00h RO/V	**Negotiated Link Width (NLW):** For the root ports, this register could take on several values: Port # Value of PN field RPC.PC1 00 01 10 11 1 01h 02h 02h 04h 2 01h 01h 01h 01h 3 01h 01h 02h 01h 4 01h 01h 01h 01h The value of this register is undefined if the link has not successfully trained.
19:16	1h RO/V	**Current Link Speed (CLS):** 0001b Link is 2.5Gb/s Link 0010b 5.0 GT/s Link The value of this field is undefined if the link is not up.
15:12	0h RO	**Reserved (RSVD_1):** Reserved
11	0b RW	**Link Autonomous Bandwidth Interrupt Enable (LABIE):** Link Autonomous Bandwidth Interrupt Enable - When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit has been Set.

Bit Range	Default & Access	Description
10	0b RW	**Link Bandwidth Management Interrupt Enable (LBMIE):** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit has been Set. This bit is not applicable and is reserved for Endpoints, PCI Express-to-PCI/PCI-X bridges, and Upstream Ports of Switches. Functions that do not implement the Link Bandwidth Notification Capability must hardwire this bit to 0b. Default value of this bit is 0b.
9	0b RW	**Hardware Autonomous Width Disable (HAWD):** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Default value of this bit is 0b.
8	0b RO	**Enable Clock Power Management (ECPM):** Reserved. Not supported on Root Ports.
7	0b RW	**Extended Synch (ES):** When set, forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	0b RW	**Common Clock Configuration (CCC):** When set, indicates that the root port and device are operating with a distributed common reference clock.
5	0b WO	**Retrain Link (RL):** When set, the root port will train its downstream link. This bit always returns '0' when read. Software uses LSTS.LT to check the status of training. It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that's already in progress.
4	0b RW	**Link Disable (LD):** When set, the root port will disable the link by directing the LTSSM to the Disabled state.
3	0b RW/O	**Read Completion Boundary Control (RCBC):** Indicates the read completion boundary is 64 bytes.
2	0b RO	**Reserved (RSVD_2):** Reserved
1:0	00b RW	**Active State Link PM Control (ASPM):** Indicates whether the root port should enter L0s or L1 or both. Bits Definition 00 Disabled 01 L0s Entry Enabled 10 L1 Entry Enabled 11 L0s and L1 Entry Enabled The value of this register is used unless the Root Port ASPM Control Override Enable register is set, in which case the Root Port ASPM Control Override value is used. Note: If STRPFUSECFG.ASPMDIS is '1', hardware will always see '00' as an output from this register. BIOS reading this register should always return the correct value.

18.6.18 Slot Capabilities (SLCAP)—Offset 54h

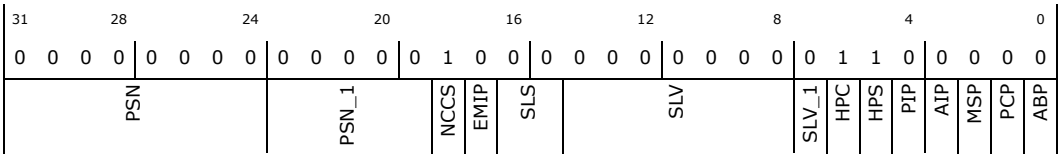
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SLCAP: [B:0, D:28, F:0] + 54h

Power Well: Core

Default: 00040060h



Bit Range	Default & Access	Description
31:24	00h RW/O	**Physical Slot Number (PSN):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
23:19	00h RW/O	**Physical Slot Number (PSN_1):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18	1b RO	**No Command Completed Support (NCCS):** Set to '1' as this port does not implement a Hot Plug controller and can handle back-2-back writes to all fields of the slot control register without delay between successive writes.
17	0b RO	**Electromechanical Interlock Present (EMIP):** Set to 0 to indicate that no electro-mechanical interlock is implemented.
16:15	00b RW/O	**Slot Power Limit Scale (SLS):** specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:8	00h RW/O	**Slot Power Limit Value (SLV):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
7	0b RW/O	**Slot Power Limit Value (SLV_1):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	1b RW/O	**Hot Plug Capable (HPC):** When set, Indicates that hot plug is supported.
5	1b RW/O	**Hot Plug Surprise (HPS):** When set, indicates the device may be removed from the slot without prior notification.
4	0b RO	**Power Indicator Present (PIP):** Indicates that a power indicator LED is not present for this slot.
3	0b RO	**Attention Indicator Present (AIP):** Indicates that an attention indicator LED is not present for this slot.
2	0b RO	**MRL Sensor Present (MSP):** Indicates that an MRL sensor is not present
1	0b RO	**Power Controller Present (PCP):** Indicates that a power controller is not implemented for this slot
0	0b RO	**Attention Button Present (ABP):** Indicates that an attention button is not implemented for this slot.

18.6.19 Slot Control; Slot Status (SLCTL_SLSTS)—Offset 58h

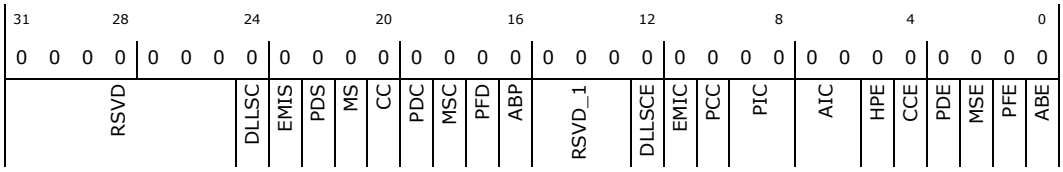
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SLCTL_SLSTS: [B:0, D:28, F:0] + 58h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:25	00h RO	**Reserved (RSVD):** Reserved
24	0b RW/C	**Data Link Layer State Changed (DLLSC):** This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	0b RO	**Electromechanical Interlock Status (EMIS):** Reserved as this port does not support and electromechanical interlock.
22	0b RO/V	**Presence Detect State (PDS):** If XCAP.SI is set (indicating that this root port spawns a slot), then this bit indicates whether a device is connected ('1') or empty ('0'). If XCAP.SI is cleared, this bit is a '1'.
21	0b RO	**MRL Sensor State (MS):** Reserved as the MRL sensor is not implemented.
20	0b RO	**Command Completed (CC):** This register is RO as this port does not implement a Hot Plug Controller..
19	0b RW/C	**Presence Detect Changed (PDC):** This bit is set by the root port when the SLSTS.PDS bit changes state.
18	0b RO	**MRL Sensor Changed (MSC):** Reserved as the MRL sensor is not implemented.
17	0b RO	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
16	0b RO	**Attention Button Pressed (ABP):** This register is RO as this port does not implement an attention button
15:13	000b RO	**Reserved (RSVD_1):** Reserved
12	0b RW	**Data Link Layer State Changed Enable (DLLSCE):** When set, this field enables generation of a hot plug interrupt when the Data Link Layer Link Active field is changed
11	0b RO	**Electromechanical Interlock Control (EMIC):** Reserved as this port does not support an Electromechanical Interlock.
10	0b RO	**Power Controller Control (PCC):** This bit has no meaning for module based hot plug.
9:8	00b RO	**Power Indicator Control (PIC):** This register is RO as this port does not implement a Hot Plug Controller..

Bit Range	Default & Access	Description
7:6	00b RO	**Attention Indicator Control (AIC):** This register is RO as this port does not implement a Hot Plug Controller..
5	0b RW	**Hot Plug Interrupt Enable (HPE):** When set, enables generation of a hot plug interrupt on enabled hot plug events.
4	0b RO	**Command Completed Interrupt Enable (CCE):** This register is RO as this port does not implement a Hot Plug Controller..
3	0b RW	**Presence Detect Changed Enable (PDE):** When set, enables the generation of a hot plug interrupt or wake message when the presence detect logic changes state.
2	0b RO	**MRL Sensor Changed Enable (MSE):** This register is RO as this port does not implement a Hot Plug Controller..
1	0b RO	**Power Fault Detected Enable (PFE):** This register is RO as this port does not implement a Hot Plug Controller...
0	0b RO	**Attention Button Pressed Enable (ABE):** This register is RO as this port does not implement a Hot Plug Controller..

18.6.20 Root Control (RCTL)—Offset 5Ch

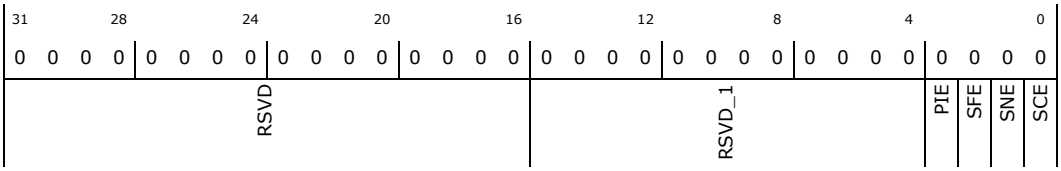
Access Method

Type: PCI Configuration Register (Size: 32 bits)

RCTL: [B:0, D:28, F:0] + 5Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15:4	000h RO	**Reserved (RSVD_1):** Reserved
3	0b RW	**PME Interrupt Enable (PIE):** When set, enables interrupt generation when RSTS.PS is in a set state (either due to a '0' to '1' transition, or due to this bit being set with RSTS.PS already set).
2	0b RW	**System Error on Fatal Error Enable (SFE):** When set, an SERR# will be generated if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port. This register is not dependent on CMD.SEE being set.
1	0b RW	**System Error on Non-Fatal Error Enable (SNE):** When set, an SERR# will be generated if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port. This register is not dependent on CMD.SEE being set.
0	0b RW	**System Error on Correctable Error Enable (SCE):** When set, an SERR# will be generated if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port. This register is not dependent on CMD.SEE being set.

18.6.21 Root Status (RSTS)—Offset 60h

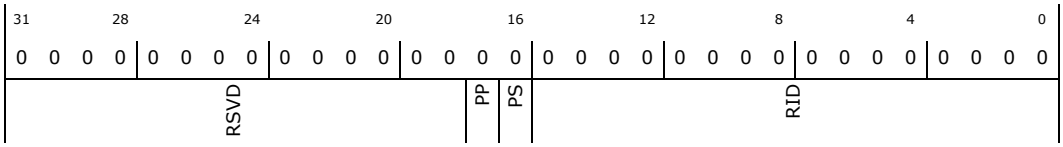
Access Method

Type: PCI Configuration Register (Size: 32 bits)

RSTS: [B:0, D:28, F:0] + 60h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:18	0000h RO	**Reserved (RSVD):** Reserved
17	0b RO/V	**PME Pending (PP):** Indicates another PME is pending when the PME status bit is set. When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. Root ports have a one deep PME pending queue.
16	0b RW/C	**PME Status (PS):** Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	0000h RO/V	**PME Requestor ID (RID):** Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set. Root ports are capable of storing the requester ID for two PM_PME messages, with one active (this register) and a one deep pending queue. Subsequent PM_PME messages will be dropped.

18.6.22 Device Capabilities 2 (DCAP2)—Offset 64h

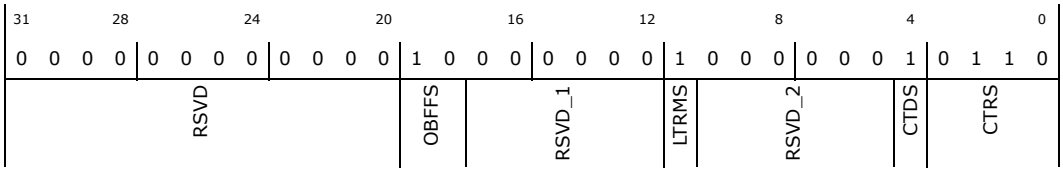
Access Method

Type: PCI Configuration Register (Size: 32 bits)

DCAP2: [B:0, D:28, F:0] + 64h

Power Well: Core

Default: 00080816h



Bit Range	Default & Access	Description
31:20	000h RO	**Reserved (RSVD):** Reserved
19:18	10b RW/O	**Optimized Buffer Flush/Fill Supported (OBFFS):** 00b - OBFF is not supported. 01b - OBFF is supported using Message signaling only. 10b - OBFF is supported using WAKE# signaling only. 11b - OBFF is supported using WAKE# and Message signaling. BIOS should program this field to 00b or 10b during system initialization to advertise the level of hardware OBFF support to software. BIOS should never program this field to 01b or 11b since OBFF messaging is not supported.

Bit Range	Default & Access	Description
17:12	00h RO	**Reserved (RSVD_1):** Reserved
11	1b RW/O	**LTR Mechanism Supported (LTRMS):** A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write to this register with either a '1' or a '0' to enable/disable the root port from declaring support for the LTR capability.
10:5	00h RO	**Reserved (RSVD_2):** Reserved
4	1b RO	**Completion Timeout Disable Supported (CTDS):** A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	6h RO	**Completion Timeout Ranges Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. Four time value ranges are defined: Range A: 50us to 10ms Range B: 10ms to 250ms Range C: 250ms to 4s Range D: 4s to 64s Bits are set according to the table below to show timeout value ranges supported. 0000b Completion Timeout programming not supported. 0001b Range A 0010b Range B 0011b Ranges A [amp] B 0110b Ranges B [amp] C [lt]-- This is supported 0111b Ranges A, B [amp] C 1110b Ranges B, C [amp] D 1111b Ranges A, B, C [amp] D All other values are reserved.

18.6.23 Device Control 2; Device Status 2 (DCTL2_DSTS2)—Offset 68h

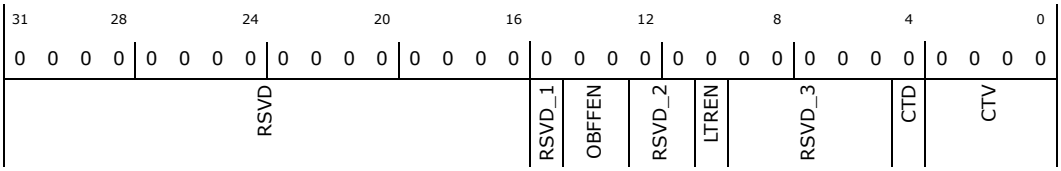
Access Method

Type: PCI Configuration Register (Size: 32 bits)

DCTL2_DSTS2: [B:0, D:28, F:0] + 68h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15	0b RO	**Reserved (RSVD_1):** Reserved
14:13	00b RW	**Optimized Buffer Flush/Fill Enable (OBFFEN):** 00b Disable OBFF mechanism. 01b Enable OBFF mechanism using Message signaling (Variation A). 10b Enable OBFF mechanism using Message signaling (Variation B). 11b Enable OBFF using WAKE# signaling. Note: Only encoding 00b and 11b are supported. The encoding of 01b or 10b would be aliased to 00b. If DCAP2.OBFFS is clear, programming this field to any non-zero values will have no effect.
12:11	00b RO	**Reserved (RSVD_2):** Reserved

Bit Range	Default & Access	Description
10	0b RW	**LTR Mechanism Enable (LTREN):** When Set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. For Downstream Ports, this bit must be reset to the default value if the Port goes to DL_Down status. If DCAP2.LTRMS is clear, programming this field to any non-zero values will have no effect.
9:5	00h RO	**Reserved (RSVD_3):** Reserved
4	0b RW	**Completion Timeout Disable (CTD):** When set to 1b, this bit disables the Completion Timeout mechanism. This field is required for all devices that support the Completion Timeout Disable Capability. Software is permitted to set or clear this bit at any time. When set, the Completion Timeout detection mechanism is disabled. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is done, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	0h RW	**Completion Timeout Value (CTV):** In Devices that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. This field is applicable to Root Ports, Endpoints that issue requests on their own behalf, and PCI Express to PCI/PCI-X Bridges that take ownership of requests issued on PCI Express. For all other devices this field is reserved and must be hardwired to 0000b. A Device that does not support this optional capability must hardwire this field to 0000b and is required to implement a timeout value in the range 50us to 50ms. Devices that support Completion Timeout programmability must support the values given below corresponding to the programmability ranges indicated in the Completion Timeout Values Supported field. The root port targeted configurable ranges are listed below, along with the range allowed by the PCI Express 2.0 specification. Defined encodings: 0000b Default range: 40-50ms (spec range 50us to 50ms) Values available if Range B (10ms to 250ms) programmability range is supported: 0101b 40-50ms (spec range is 16ms to 55ms) 0110b 160-170ms (spec range is 65ms to 210ms) Values available if Range C (250ms to 4s) programmability range is supported: 1001b 400-500ms (spec range is 260ms to 900ms) 1010b 1.6-1.7s (spec range is 1s to 3.5s) Values not defined above are Reserved. Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either when this value was changed or when each request was issued.

18.6.24 Link Capabilities 2 (LCAP2)—Offset 6Ch

Size:32 bits

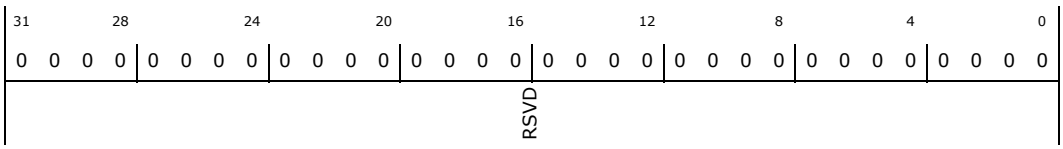
Access Method

Type: PCI Configuration Register (Size: 32 bits)

LCAP2: [B:0, D:28, F:0] + 6Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Reserved (RSVD):** Reserved

18.6.25 Link Control 2; Link Status 2 (LCTL2_LSTS2)—Offset 70h

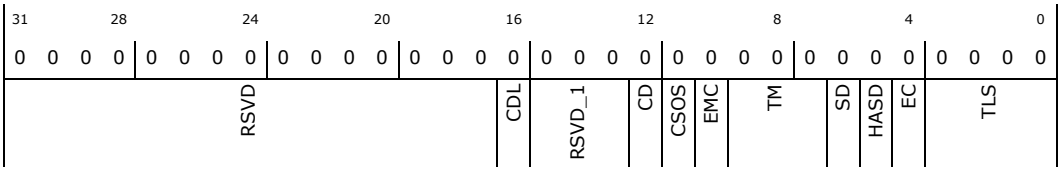
Access Method

Type: PCI Configuration Register (Size: 32 bits)

LCTL2_LSTS2: [B:0, D:28, F:0] + 70h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:17	0000h RO	**Reserved (RSVD):** Reserved
16	0b RO/V	**Current De-emphasis Level (CDL):** When the Link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB The value in this bit is undefined when the Link is operating at 2.5 GT/s speed.
15:13	000b RO	**Reserved (RSVD_1):** Reserved
12	0b RW/P	**Compliance De-emphasis (CD):** This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 1b-3.5 dB 0b-6 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. The default value of this bit is 0b. This bit is intended for debug, compliance testing purposes. System firmware and software is allowed to modify this bit only during debug or compliance testing.
11	0b RW/P	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b.
10	0b RW/P	**Enter Modified Compliance (EMC):** When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substate. Default value of this bit is 0b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
9:7	000b RW/P	**Transmit Margin (TM):** This field controls the value of the nondeemphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate (see PCI Express Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: 000b Normal operating range 001b 800-1200 mV for full swing and 400-700 mV for half-swing 010b - (n-1) Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n : 200-400 mV for full-swing and 100-200 mV for half-swing n - 111b reserved For a Multi-Function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type RsvdP. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hardwire this bit to 000b. This register is intended for debug, compliance testing purposes only. System firmware and software is allowed to modify this register only during debug or compliance testing. In all other cases, the system must ensure that this register is set to the default value.
6	0b RW/P	**Selectable De-emphasis (SD):** When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	0b RO	**Hardware Autonomous Speed Disable (HASD):** Reserved. This port cannot autonomously change speeds.

Bit Range	Default & Access	Description
4	0b RW/P	**Enter Compliance (EC):** Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link. Default value of this bit following Fundamental Reset is 0b.
3:0	0h RW/P	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. For root port, the allowed value is: 0001b 2.5 GT/s Target Link Speed 0010b 5.0 GT/s and 2.5GT/s Link speeds supported If a value is written to this field that does not correspond to a speed included in the Supported Link Speeds field, the result is undefined. The default value of this field is the highest Link speed supported by the component (as reported in the Supported Link Speeds field of the Link Capabilities register).

18.6.26 Slot Capabilities 2 (SLCAP2)—Offset 74h

Size:32 bits

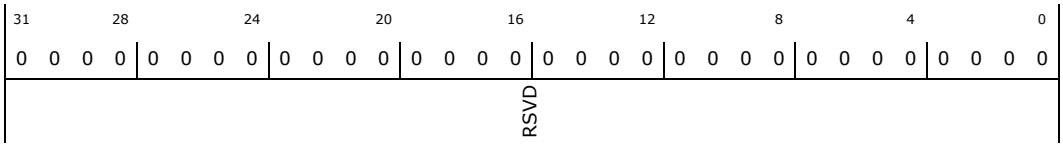
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SLCAP2: [B:0, D:28, F:0] + 74h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Reserved (RSVD):** Reserved

18.6.27 Slot Control 2; Slot Status 2 (SLCTL2_SLSTS2)—Offset 78h

Size:32 bits

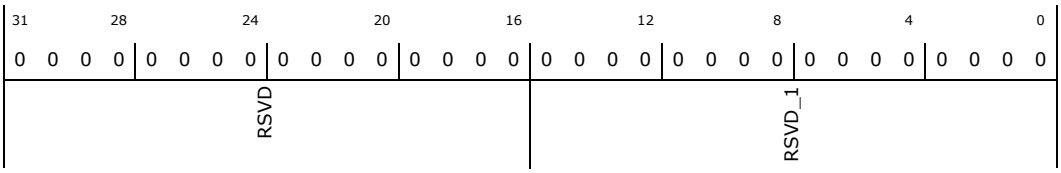
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SLCTL2_SLSTS2: [B:0, D:28, F:0] + 78h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15:0	0000h RO	**Reserved (RSVD_1):** Reserved

18.6.28 Message Signaled Interrupt Identifiers; Message Signaled Interrupt Message Control (MID_MC)—Offset 80h

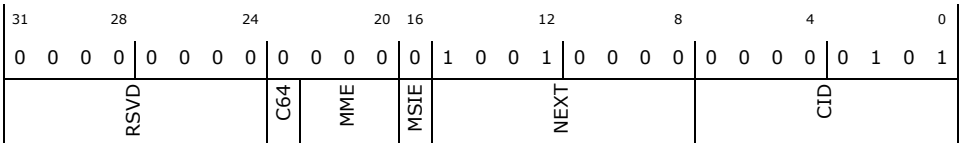
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MID_MC: [B:0, D:28, F:0] + 80h

Power Well: Core

Default: 00009005h



Bit Range	Default & Access	Description
31:24	00h RO	**Reserved (RSVD):** Reserved
23	0b RO	**64-Bit Address Capable (C64):** Capable of generating a 32-bit message only.
22:20	000b RW	**Multiple Message Enable (MME):** These bits are RW for software compatibility, but only one message is ever sent by the root port.
16	0b RW	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. CMD.BME must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

Bit Range	Default & Access	Description
15:8	90h RW/O	**Next Pointer (NEXT):** Indicates the location of the next capability in the list. The default value of this register is 90h which points to the Subsystem Vendor capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	05h RO	**Capability ID (CID):** Capabilities ID indicates MSI.

18.6.29 Message Signaled Interrupt Message Address (MA)—Offset 84h

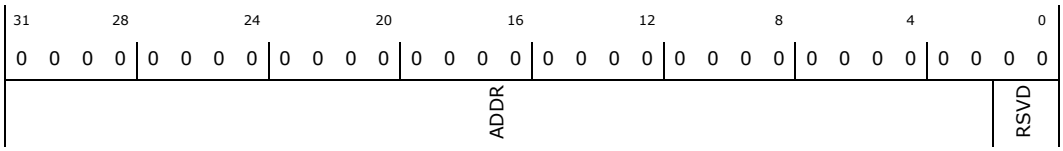
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MA: [B:0, D:28, F:0] + 84h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:2	00000000h RW	**Address (ADDR):** Lower 32 bits of the system specified message address, always DW aligned.
1:0	00b RO	**Reserved (RSVD):** Reserved

18.6.30 Message Signaled Interrupt Message Data (MD)—Offset 88h

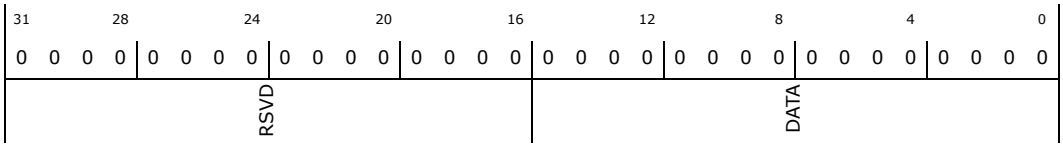
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MD: [B:0, D:28, F:0] + 88h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15:0	0000h RW	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[lb]15:0[rb]) during the data phase of the MSI memory write transaction.

18.6.31 Subsystem Vendor Capability (SVCAP)—Offset 90h

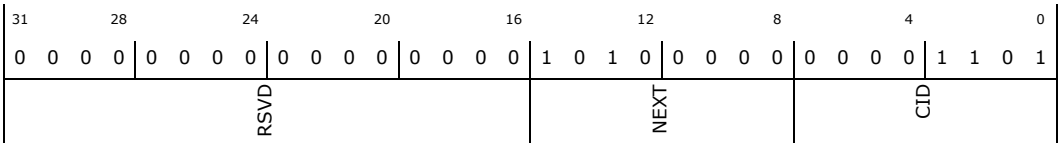
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SVCAP: [B:0, D:28, F:0] + 90h

Power Well: Core

Default: 0000A00Dh



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSVD):** Reserved
15:8	A0h RW/O	**Next Capability (NEXT):** Indicates the location of the next capability in the list. The default value of this register is A0h which points to the PCI Power Management capability structure. BIOS can determine which capabilities will be exposed by including or removing them from the capability linked list. As this register is RWO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	0Dh RO	**Capability Identifier (CID):** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

18.6.32 Subsystem Vendor IDs (SVID)—Offset 94h

Size:32 bits

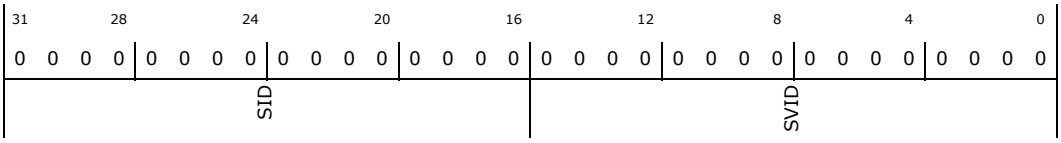
Access Method

Type: PCI Configuration Register (Size: 32 bits)

SVID: [B:0, D:28, F:0] + 94h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW/O	**Subsystem Identifier (SID):** Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	0000h RW/O	**Subsystem Vendor Identifier (SVID):** Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

18.6.33 Power Management Capability; PCI Power Management Capabilities (PMCAP_PMC)—Offset A0h

Size:32 bits

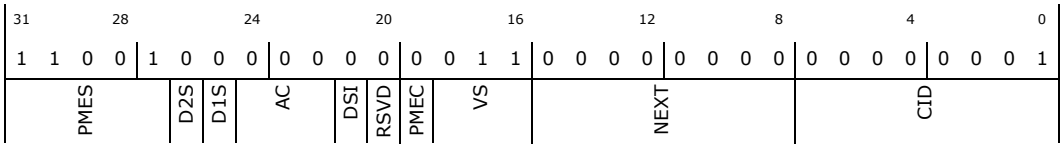
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCAP_PMC: [B:0, D:28, F:0] + A0h

Power Well: Core

Default: C8030001h



Bit Range	Default & Access	Description
31:27	11001b RO	**PME Support (PMES):** Indicates PME# is supported for states D0, D3HOT and D3COLD. The root port does not generate PME#, but reporting that it does is necessary for legacy Microsoft operating systems to enable PME# in devices connected behind this root port.
26	0b RO	**D2_Support (D2S):** The D2 state is not supported.
25	0b RO	**D1_Support (D1S):** The D1 state is not supported.
24:22	000b RO	**Aux_Current (AC):** Reports 0mA (self-powered), as use of this controller does not add to suspend well power consumption.
21	0b RO	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
20	0b RO	**Reserved (RSVD):** Reserved
19	0b RO	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
18:16	011b RO	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.
15:8	00h RO	**Next Capability (NEXT):** Indicates this is the last item in the list.
7:0	01h RO	**Capability Identifier (CID):** Value of 01h indicates this is a PCI power management capability.

18.6.34 PCI Power Management Control And Status (PMCS)—Offset A4h

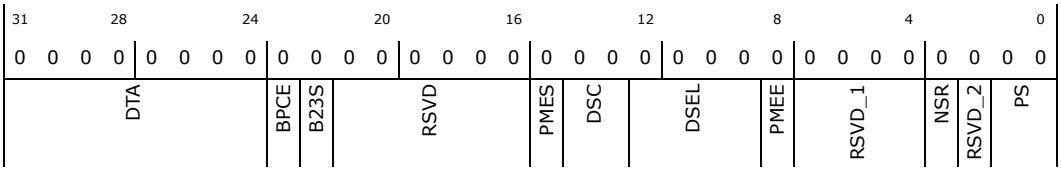
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMCS: [B:0, D:28, F:0] + A4h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO	**Data (DTA):** Reserved
23	0b RO	**Bus Power / Clock Control Enable (BPCE):** Reserved per PCI Express specification
22	0b RO	**B2/B3 Support (B23S):** Reserved per PCI Express specification.
21:16	00h RO	**Reserved (RSVD):** Reserved
15	0b RO	**PME Status (PMES):** Indicates a PME was received on the downstream link.
14:13	00b RO	**Data Scale (DSC):** Reserved
12:9	0h RO	**Data Select (DSEL):** Reserved
8	0b RW/P	**PME Enable (PMEE):** Indicates PME is enabled. This register maintains its value through S3/4/5 states.
7:4	0h RO	**Reserved (RSVD_1):** Reserved
3	0b RO	**No Soft Reset (NSR):** When set to 1 this bit indicates that devices transitioning from D3hot to D0 because of Power State commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the Power State bits. When clear, devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the Power State bits. Configuration Context is lost when performing the soft reset. Upon transition from D3hot to D0 state, full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 Uninitialized with only PME context preserved if PME is supported and enabled.
2	0b RO	**Reserved (RSVD_2):** Reserved
1:0	00b RW	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 D0 state 11 D3HOT state When in the D3HOT state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3HOT. If software attempts to write a '10' or '01' to these bits, the write will be ignored.

18.6.35 Manufacturer's ID (MANID)—Offset F8h

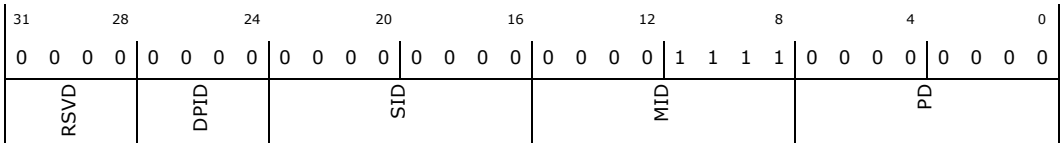
Access Method

Type: PCI Configuration Register (Size: 32 bits)

MANID: [B:0, D:28, F:0] + F8h

Power Well: Core

Default: 00000F00h



Bit Range	Default & Access	Description
31:28	0h RO	**Reserved (RSVD):** Reserved
27:24	0h RO/V	**Dot portion of Process ID (DPID):** The value of this field is processor specific. Example: Process/Dot (PD) is 1265.8. Indicates the dot as .8.
23:16	00h RO/V	**Stepping Identifier (SID):** This field is incremented for each stepping of the part. Note that this field can be used by software to differentiate steppings when the Revision ID may not change. A single Manufacturing Stepping ID can be implemented that is readable from all functions in the chip because all of them are incremented in lock-step.
15:8	0Fh RO	**Manufacturing Identifier (MID):** 0Fh = Intel
7:0	00h RO/V	**Process/Dot (PD):** Indicates the current process. The value of this field is processor specific. Example: Process/Dot (PD) is 1265.8. Indicates the Process (1265).

18.6.36 Advanced Error Reporting Capability Header (AECH)—Offset 100h

The AER capability can optionally be included or excluded from the capabilities list. The full AER is supported.

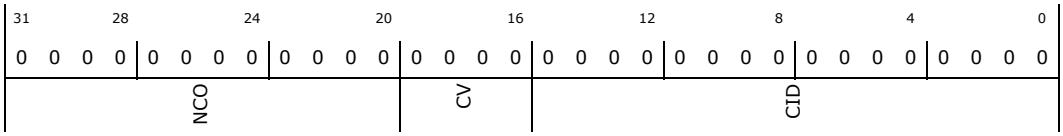
Access Method

Type: PCI Configuration Register (Size: 32 bits)

AECH: [B:0, D:28, F:0] + 100h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:20	000h RO	**Next Capability Offset (NCO):** Set to 000h as this is the last capability in the list.

Bit Range	Default & Access	Description
19:16	0h RW/O	**Capability Version (CV):** For systems that support AER, BIOS should write a 1h to this register else it should write 0
15:0	0000h RW/O	**Capability ID (CID):** For systems that support AER, BIOS should write a 0001h to this register else it should write 0

18.6.37 Uncorrectable Error Status (UES)—Offset 104h

This register must maintain its state through a platform reset. It loses its state upon loss of core power.

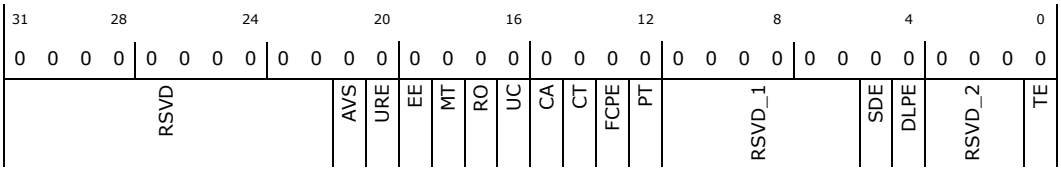
Access Method

Type: PCI Configuration Register (Size: 32 bits)

UES: [B:0, D:28, F:0] + 104h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:22	000h RO	**Reserved (RSVD):** Reserved
21	0b RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0b RW/1C/P	**Unsupported Request Error Status (URE):** Indicates an unsupported request was received.
19	0b RO	**ECRC Error Status (EE):** ECRC is not supported.
18	0b RW/1C/P	**Malformed TLP Status (MT):** Indicates a malformed TLP was received.
17	0b RW/1C/P	**Receiver Overflow Status (RO):** Indicates a receiver overflow occurred.
16	0b RW/1C/P	**Unexpected Completion Status (UC):** Indicates an unexpected completion was received.
15	0b RW/1C/P	**Completor Abort Status (CA):** Indicates a completer abort was received
14	0b RW/1C/P	**Completion Timeout Status (CT):** Indicates a completion timed out. This is signaled if Completion Timeout is enabled and a completion fails to return within the amount of time specified by the Completion Timeout Value
13	0b RO	**Flow Control Protocol Error Status (FCPE):** Not supported.
12	0b RW/1C/P	**Poisoned TLP Status (PT):** Indicates a poisoned TLP was received.

Bit Range	Default & Access	Description
11:6	00h RO	**Reserved (RSVD_1):** Reserved
5	0b RO	**Surprise Down Error Status (SDE):** Surprise Down is not supported.
4	0b RW/1C/P	**Data Link Protocol Error Status (DLPE):** Indicates a data link protocol error occurred.
3:1	000b RO	**Reserved (RSVD_2):** Reserved
0	0b RO	**Training Error Status (TE):** Not supported.

18.6.38 Uncorrectable Error Mask (UEM)—Offset 108h

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

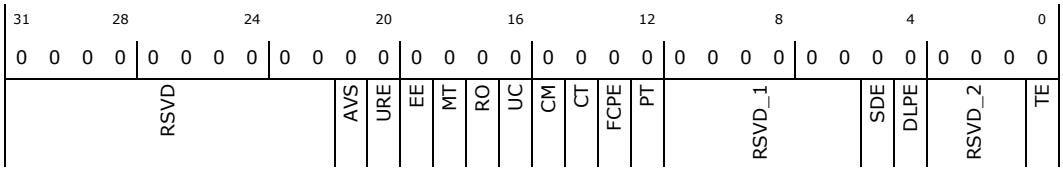
Access Method

Type: PCI Configuration Register (Size: 32 bits)

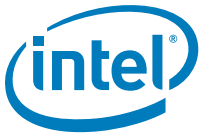
UEM: [B:0, D:28, F:0] + 108h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:22	000h RO	**Reserved (RSVD):** Reserved
21	0b RO	**ACS Violation Status (AVS):** Reserved. Access Control Services are not supported
20	0b RW/P	**Unsupported Request Error Mask (URE):** Mask for uncorrectable errors.
19	0b RO	**ECRC Error Mask (EE):** ECRC is not supported.
18	0b RW/P	**Malformed TLP Mask (MT):** Mask for malformed TLPs
17	0b RW/P	**Receiver Overflow Mask (RO):** Mask for receiver overflows.
16	0b RW/P	**Unexpected Completion Mask (UC):** Mask for unexpected completions.
15	0b RW/P	**Completor Abort Mask (CM):** Mask for completer abort.



Bit Range	Default & Access	Description
14	0b RW/P	**Completion Timeout Mask (CT):** Mask for completion timeouts.
13	0b RO	**Flow Control Protocol Error Mask (FCPE):** Not supported.
12	0b RW/P	**Poisoned TLP Mask (PT):** Mask for poisoned TLPs.
11:6	00h RO	**Reserved (RSVD_1):** Reserved
5	0b RO	**Surprise Down Error Mask (SDE):** Surprise Down is not supported.
4	0b RW/P	**Data Link Protocol Error Mask (DLPE):** Mask for data link protocol errors.
3:1	000b RO	**Reserved (RSVD_2):** Reserved
0	0b RO	**Training Error Mask (TE):** Not supported.

18.6.39 Uncorrectable Error Severity (UEV)—Offset 10Ch

This register gives the option to make an uncorrectable error fatal or non-fatal. An error is fatal if the bit is set. An error is non-fatal if the bit is cleared. This register is only reset by a loss of core power.

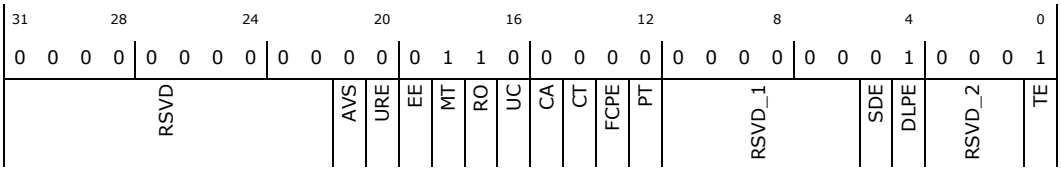
Access Method

Type: PCI Configuration Register (Size: 32 bits)

UEV: [B:0, D:28, F:0] + 10Ch

Power Well: Core

Default: 00060011h



Bit Range	Default & Access	Description
31:22	000h RO	**Reserved (RSVD):** Reserved
21	0b RO	**ACS Violation Severity (AVS):** Reserved. Access Control Services are not supported
20	0b RW/P	**Unsupported Request Error Severity (URE):** Severity for unsupported request reception.
19	0b RO	**ECRC Error Severity (EE):** ECRC is not supported.
18	1b RW/P	**Malformed TLP Severity (MT):** Severity for malformed TLP reception.

Bit Range	Default & Access	Description
17	1b RW/P	**Receiver Overflow Severity (RO):** Severity for receiver overflow occurrences.
16	0b RW/P	**Unexpected Completion Severity (UC):** Severity for unexpected completion reception.
15	0b RW/P	**Completor Abort Severity (CA):** Severity for completer abort.
14	0b RW/P	**Completion Timeout Severity (CT):** Severity for completion timeout.
13	0b RO	**Flow Control Protocol Error Severity (FCPE):** Not supported.
12	0b RW/P	**Poisoned TLP Severity (PT):** Severity for poisoned TLP reception.
11:6	00h RO	**Reserved (RSVD_1):** Reserved
5	0b RO	**Surprise Down Error Severity (SDE):** Surprise Down is not supported.
4	1b RW/P	**Data Link Protocol Error Severity (DLPE):** Severity for data link protocol errors.
3:1	000b RO	**Reserved (RSVD_2):** Reserved
0	1b RO	**Training Error Severity (TE):** TE not supported. This bit is left as RO='1' for ease of implementation..

18.6.40 Correctable Error Status (CES)—Offset 110h

This register is only reset by a loss of core power

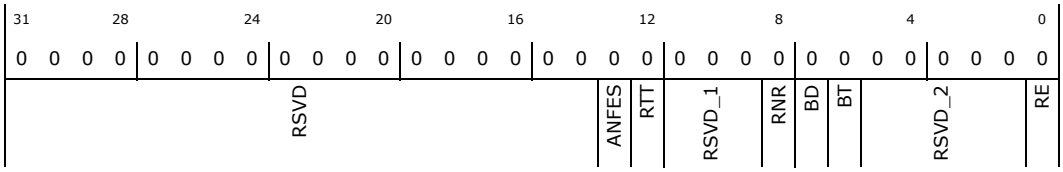
Access Method

Type: PCI Configuration Register (Size: 32 bits)

CES: [B:0, D:28, F:0] + 110h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:14	00000h RO	**Reserved (RSVD):** Reserved
13	0b RW/1C/P	**Advisory Non-Fatal Error Status (ANFES):** When set, indicates that a Advisory Non-Fatal Error occured.
12	0b RW/1C/P	**Replay Timer Timeout Status (RTT):** Indicates the replay timer timed out.

Bit Range	Default & Access	Description
11:9	000b RO	**Reserved (RSVD_1):** Reserved
8	0b RW/1C/P	**Replay Number Rollover Status (RNR):** Indicates the replay number rolled over.
7	0b RW/1C/P	**Bad DLLP Status (BD):** Indicates a bad DLLP was received.
6	0b RW/1C/P	**Bad TLP Status (BT):** Indicates a bad TLP was received.
5:1	00h RO	**Reserved (RSVD_2):** Reserved
0	0b RW/1C/P	**Receiver Error Status (RE):** Indicates a receiver error occurred.

18.6.41 Correctable Error Mask (CEM)—Offset 114h

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled. This register is only reset by a loss of core power.

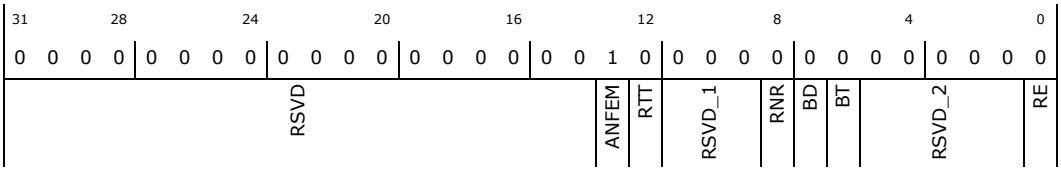
Access Method

Type: PCI Configuration Register (Size: 32 bits)

CEM: [B:0, D:28, F:0] + 114h

Power Well: Core

Default: 00002000h



Bit Range	Default & Access	Description
31:14	00000h RO	**Reserved (RSVD):** Reserved
13	1b RW/P	**Advisory Non-Fatal Error Mask (ANFEM):** When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
12	0b RW/P	**Replay Timer Timeout Mask (RTT):** Mask for replay timer timeout.
11:9	000b RO	**Reserved (RSVD_1):** Reserved
8	0b RW/P	**Replay Number Rollover Mask (RNR):** Mask for replay number rollover.
7	0b RW/P	**Bad DLLP Mask (BD):** Mask for bad DLLP reception.

Bit Range	Default & Access	Description
6	0b RW/P	**Bad TLP Mask (BT):** Mask for bad TLP reception.
5:1	00h RO	**Reserved (RSVD_2):** Reserved
0	0b RW/P	**Receiver Error Mask (RE):** Mask for receiver errors.

18.6.42 Advanced Error Capabilities and Control (AECC)—Offset 118h

This register is only reset by a loss of core power.

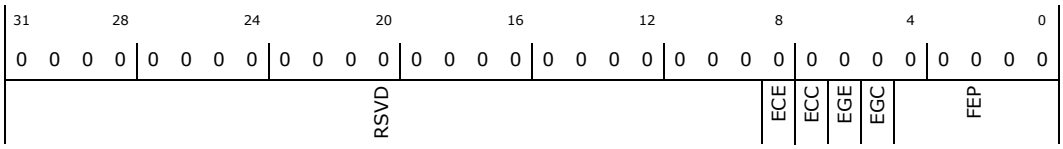
Access Method

Type: PCI Configuration Register (Size: 32 bits)

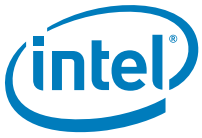
AECC: [B:0, D:28, F:0] + 118h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:9	000000h RO	**Reserved (RSVD):** Reserved
8	0b RO	**ECRC Check Enable (ECE):** ECRC is not supported.
7	0b RO	**ECRC Check Capable (ECC):** ECRC is not supported.
6	0b RO	**ECRC Generation Enable (EGE):** ECRC is not supported.
5	0b RO	**ECRC Generation Capabile (EGC):** ECRC is not supported.
4:0	00000b RO/V/P	**First Error Pointer (FEP):** Identifies the bit position of the first error reported in the Uncorrectable Error Status Register.



18.6.43 Header Log DW1 (HL_DW1)—Offset 11Ch

Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

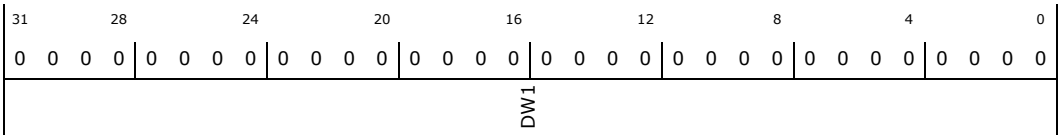
Access Method

Type: PCI Configuration Register (Size: 32 bits)

HL_DW1: [B:0, D:28, F:0] + 11Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO/V/P	**1st dWord of TLP (DW1):** Byte0 [amp][amp] Byte1 [amp][amp] Byte2 [amp][amp] Byte3

18.6.44 Header Log DW2 (HL_DW2)—Offset 120h

Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

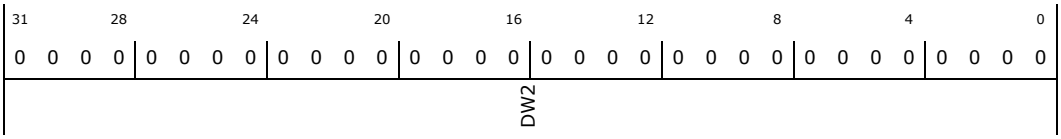
Access Method

Type: PCI Configuration Register (Size: 32 bits)

HL_DW2: [B:0, D:28, F:0] + 120h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO/V/P	**2nd dWord of TLP (DW2):** Byte4 [amp][amp] Byte5 [amp][amp] Byte6 [amp][amp] Byte7

18.6.45 Header Log DW3 (HL_DW3)—Offset 124h

Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

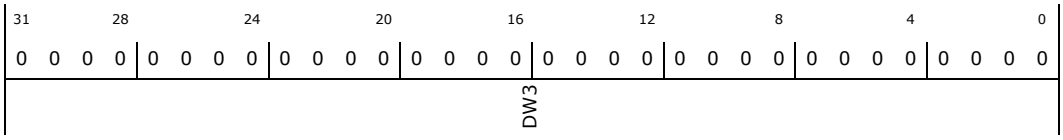
Access Method

Type: PCI Configuration Register (Size: 32 bits)

HL_DW3: [B:0, D:28, F:0] + 124h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO/V/P	**3rd dWord of TLP (DW3):** Byte8 [amp][amp] Byte9 [amp][amp] Byte10 [amp][amp] Byte11

18.6.46 Header Log DW4 (HL_DW4)—Offset 128h

Size:32 bits These registers report the header for the TLP corresponding to a detected error. This register is only reset by a loss of core power.

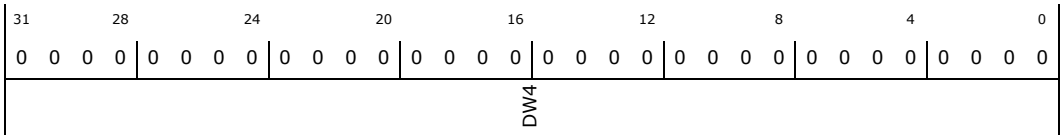
Access Method

Type: PCI Configuration Register (Size: 32 bits)

HL_DW4: [B:0, D:28, F:0] + 128h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO/V/P	**4th dWord of TLP (DW4):** Byte12 [amp][amp] Byte13 [amp][amp] Byte14 [amp][amp] Byte15

18.6.47 Root Error Command (REC)—Offset 12Ch

This register allows errors to generate interrupts.

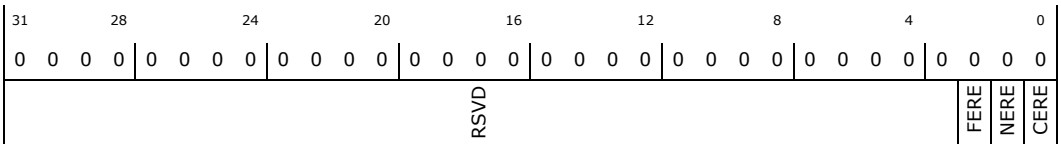
Access Method

Type: PCI Configuration Register (Size: 32 bits)

REC: [B:0, D:28, F:0] + 12Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:3	00000000h RO	**Reserved (RSVD):** Reserved
2	0b RW	**Fatal Error Reporting Enable (FERE):** When set, the root port will generate an interrupt when a fatal error is reported by the attached device.
1	0b RW	**Non-fatal Error Reporting Enable (NERE):** When set, the root port will generate an interrupt when a non-fatal error is reported by the attached device.
0	0b RW	**Correctable Error Reporting Enable (CERE):** When set, the root port will generate an interrupt when a correctable error is reported by the attached device.

18.6.48 Root Error Status (RES)—Offset 130h

This register can track more than one error and set the 'multiple' bits if a second or subsequent error occurs and the first has not been serviced. This register is only reset by a loss of core power.

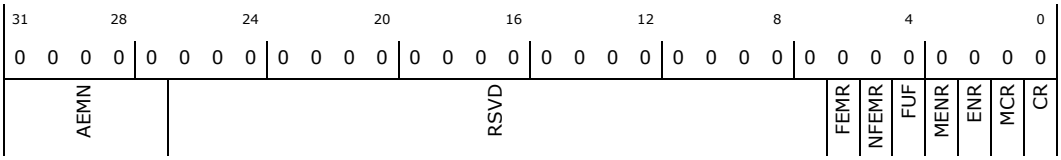
Access Method

Type: PCI Configuration Register (Size: 32 bits)

RES: [B:0, D:28, F:0] + 130h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:27	00h RO	**Advanced Error Interrupt Message Number (AEMN):** Reserved. There is only one error interrupt allocated.
26:7	00000h RO	**Reserved (RSVD):** Reserved

Bit Range	Default & Access	Description
6	0b RW/1C/P	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	0b RW/1C/P	**Non-Fatal Error Messages Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received
4	0b RW/1C/P	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	0b RW/1C/P	**Multiple ERR_FATAL/NONFATAL Received (MENR):** Set when either a fatal or a non-fatal error is received and the ENR bit is already set.
2	0b RW/1C/P	**ERR_FATAL/NONFATAL Received (ENR):** Set when either a fatal or a non-fatal error message is received.
1	0b RW/1C/P	**Multiple ERR_COR Received (MCR):** Set when a correctable error message is received and the CR bit is already set.
0	0b RW/1C/P	**ERR_COR Received (CR):** Set when a correctable error message is received.

18.6.49 Error Source Identification (ESID)—Offset 134h

Size:32 bits Identifies the source (Requester ID) of the first correctable and uncorrectable (Non-Fatal / Fatal) errors reported in the Root Error Status register. This register is only reset by a loss of core power.

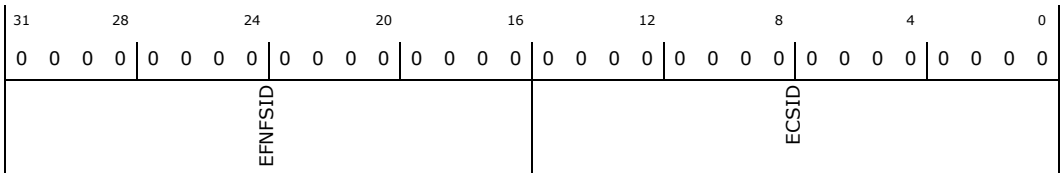
Access Method

Type: PCI Configuration Register (Size: 32 bits)

ESID: [B:0, D:28, F:0] + 134h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RO/V/P	**ERR_FATAL/NONFATAL Source Identification (EFNFSID):** Loaded with the Requester ID indicated in the received ERR_FATAL or ERR_NONFATAL Message with the ERR_FATAL/NONFATAL Received register is not already set.
15:0	0000h RO/V/P	**ERR_COR Source Identification (ECSID):** Loaded with the Requester ID indicated in the received ERR_COR Message with the ERR_COR Received register is not already set.

18.6.50 PCI Express Status 1 (PCIESTS1)—Offset 328h

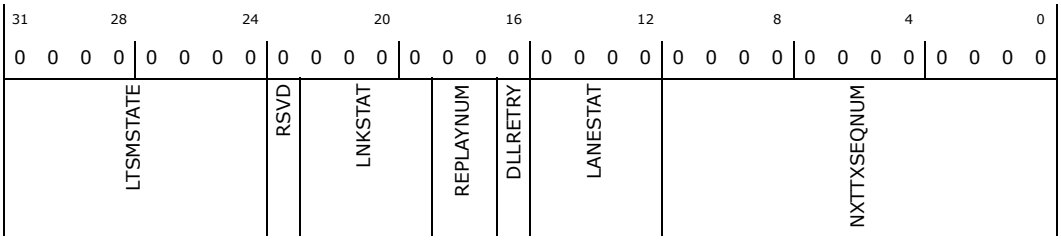
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIESTS1: [B:0, D:28, F:0] + 328h

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RO/V	**LTSM State (LTSMSTATE):** Indicates the LTSM present state. 00000: DETECTQUIET 00001: DETECTACTIVE 00010: POLLINGACTIVE 00011: POLLINGCOMPLIANCE 00100: POLLINGCONFIGURATION 00101: POLLINGSPEED 00110: CONFIGRCVRCFG 00111: CONFIGRCVRCFGLPBK 01000: CONFIGIDLE 01001: L0 01010: L0WAIT 01011: RECOVERYRCVRLOCK 01100: RECOVERYRCVRCFG 01101: RECOVERYIDLE 01110: RECOVERYIDLELPBK 01111: L1ENTRY 10000: L1IDLE 10001: L2IDLE 10010: LINKCONTROLRESET 10011: LOOPBACKENTRY 10100: LOOPBACKACTIVE 10101: LOOPBACKEXITM 10110: LOOPBACKEXITS 10111: DISABLED Note: This register field could be used by REUT software to monitor the link LTSSM substates.
23	0b RO	**Reserved (RSVD):** Reserved
22:19	0000b RO/V	**Link Status (LNKSTAT):** During Link initialization the Link will always traverse this list of state from the top (0000) to the bottom of the list (0111). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000 Link Down 0001 : Link Retrain 0011 : L1 0100 : L2 0101 : L3 0111 : L0 (Link Up) 1000 : L0s (Transmit [amp] Receive) 1001 : L0s (Transmit only) 1010 : L0s (Receive only) All others reserved
18:17	00b RO/V	**Replay Number (REPLAYNUM):** Number of times the Retry Buffer has been replayed since the last Link initialization / re-training. When the Data Link Layer has replayed the contents of the Retry Buffer four times a Link re-training will be initiated which will reset this value back to zero.
16	0b RO/V	**Data Link Layer Retry (DLLRETRY):** Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number will be the sequence number associated with the corrupted packet.
15:12	0h RO/V	**Lane Status (LANESTAT):** Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (that is, bit 0 = '1' means lane 0 is trained).
11:0	000h RO/V	**Next Transmitted Sequence Number (NXTTXSEQNUM):** This is the sequence number to be applied to and pre-pended to the next outgoing TLP.

18.6.51 PCI Express Status 2 (PCIESTS2)—Offset 32Ch

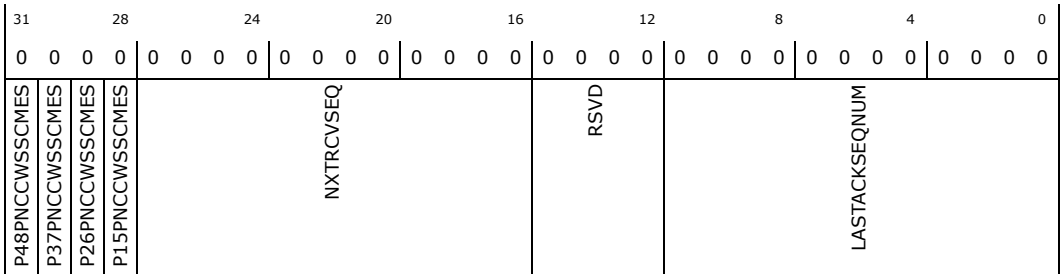
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIESTS2: [B:0, D:28, F:0] + 32Ch

Power Well: Core

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO/V	**PCIe Port 4 Non-Common Clock With SSC Mode Enable Strap (P48PNCCWSSCMES):** '0': PCIe port 4/8 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 4/8 is enabled to operate in non-common clock mode with SSC enabled.
30	0b RO/V	**PCIe Port 3 Non-Common Clock With SSC Mode Enable Strap (P37PNCCWSSCMES):** '0': PCIe port 3 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 3 is enabled to operate in non-common clock mode with SSC enabled.
29	0b RO/V	**PCIe Port 2 Non-Common Clock With SSC Mode Enable Strap (P26PNCCWSSCMES):** '0': PCIe port 2 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 2 is enabled to operate in non-common clock mode with SSC enabled.
28	0b RO/V	**PCIe Port 1 Non-Common Clock With SSC Mode Enable Strap (P15PNCCWSSCMES):** '0': PCIe port 1 is not enabled to operate in non-common clock mode with SSC enabled. '1': PCIe port 1 is enabled to operate in non-common clock mode with SSC enabled.
27:16	000h RO/V	**Next Receive Sequence Number (NXTRCVSEQ):** This is the sequence number associated with the TLP that is expected to be received next.
15:12	0h RO	**Reserved (RSVD):** Reserved
11:0	000h RO/V	**Last Acknowledged Sequence Number (LASTACKSEQNUM):** This is the sequence number associated with the last acknowledged TLP.

18.6.52 PCI Express Compliance Measurement Mode (CMM) Port Control (PCIECMMPC)—Offset 330h

Note that selecting a lane number that does not exist for a port may result in undefined behavior.

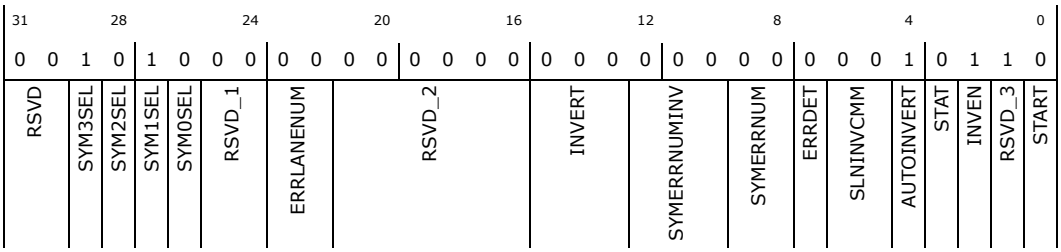
Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIECMMPC: [B:0, D:28, F:0] + 330h

Power Well: Core

Default: 28000016h



Bit Range	Default & Access	Description
31:30	00b RO	**Reserved (RSVD):** Reserved
29	1b RW	**CMM Symbol[3] Select (SYM3SEL):** 0: selects CMM Symbol [lb]3[rb] to a control character 1: selects CMM Symbol [lb]3[rb] as a data character
28	0b RW	**CMM Symbol[2] Select (SYM2SEL):** 0: selects CMM Symbol [lb]2[rb] to a control character 1: selects CMM Symbol [lb]2[rb] as a data character
27	1b RW	**CMM Symbol[1] Select (SYM1SEL):** 0: selects CMM Symbol [lb]1[rb] to a control character 1: selects CMM Symbol [lb]1[rb] as a data character
26	0b RW	**CMM Symbol[0] Select (SYM0SEL):** 0: selects CMM Symbol [lb]0[rb] to a control character 1: selects CMM Symbol [lb]0[rb] as a data character
25:24	00b RO	**Reserved (RSVD_1):** Reserved
23:22	00b RO/V	**CMM Error Lane Number (ERRLANENUM):** This field contains the lane number of the failing lane. Only valid when CMM Error Detected is 1.
21:16	00h RO	**Reserved (RSVD_2):** Reserved
15:13	000b RO/V	**CMM Invert (INVERT):** Indicates which lanes are inverted 000: No inversion 001: Lanes 0 010: Lanes 1 011: Lanes 2 100: Lanes 3 This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated)
12:10	000b RO/V	**CMM Symbol Error Number Invert (SYMERRNUMINV):** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. 000: CMM Data D0 001: CMM Data D0 010: CMM Data D0 011: CMM Data D1 100: CMM Data D2 101: CMM Data D3 110: CMM Data D0 111: CMM Data D0
9:8	00b RO/V	**CMM Symbol Error Number (SYMERRNUM):** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. 00: CMM Data 0 01: CMM Data 1 10: CMM Data 2 11: CMM Data 3

Bit Range	Default & Access	Description
7	0b RW/C	**CMM Error Detected (ERRDET):** 1: An error was detected 0: No error detected Note: This bit will be shadowed to an observability pin that can be used for IRQ generation.
6:5	00b RW	**Select Lane Number to be inverted for CMM (SLNINVCMM):** Select Lane Number to be inverted for CMM
4	1b RW	**CMM AutoInvert (AUTOINVERT):** 1: CMM autosequences through the inversion 0: CMM does not sequence inversion
3	0b RO/V	**CMM Status (STAT):** This bit is set when the CMM Start bit is set and cleared when the CMM mode has been entered successfully. 0: Compliance Measurement Mode is not active or CMM mode has been entered successfully. 1: Set as a result of CMM Start bit being set.
2	1b RW	**CMM Invert Enable (INVEN):** 1: Enables the Inversion of the lane 0: Lane not inverted
1	1b RW	**Reserved (RSVD_3):** Reserved
0	0b RW	**CMM Start (START):** 1: Start CMM 0: Stop CMM

18.6.53 PCI Express Compliance Measurement Mode Symbol Buffer (PCIECMMSB)—Offset 334h

Size:32 bits

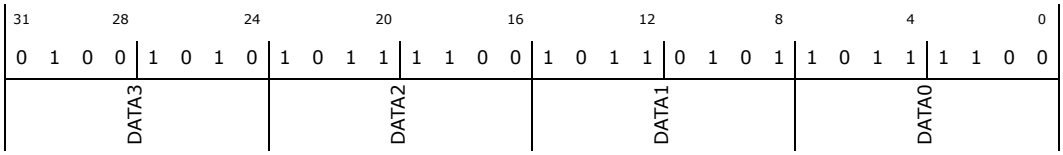
Access Method

Type: PCI Configuration Register (Size: 32 bits)

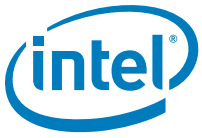
PCIECMMSB: [B:0, D:28, F:0] + 334h

Power Well: Core

Default: 4ABCB5BCh



Bit Range	Default & Access	Description
31:24	4Ah RW	**CMM Data [3] (DATA3):** This character contains CMM Data [lb]3[rb] that will be transmitted on the link.
23:16	BCh RW	**CMM Data [2] (DATA2):** This character contains CMM Data [lb]2[rb] that will be transmitted on the link.
15:8	B5h RW	**CMM Data [1] (DATA1):** This character contains CMM Data [lb]1[rb] that will be transmitted on the link.
7:0	BCh RW	**CMM Data [0] (DATA0):** This character contains CMM Data [lb]0[rb] that will be transmitted on the link.



18.7 PCI Express* Lane 0 Electrical Address Map

Table 134. Summary of PCI Express* Lane 0 Electrical Message Bus Registers—0xA6 (Global Offset 200h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 774	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 776	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 777	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 778	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 779	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 780	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 782	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 783	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 784	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 785	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 787	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 788	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 790	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 791	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 792	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 793	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 795	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 796	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 798	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 799	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 800	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 801	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 802	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 803	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 803	0001C020h

18.7.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

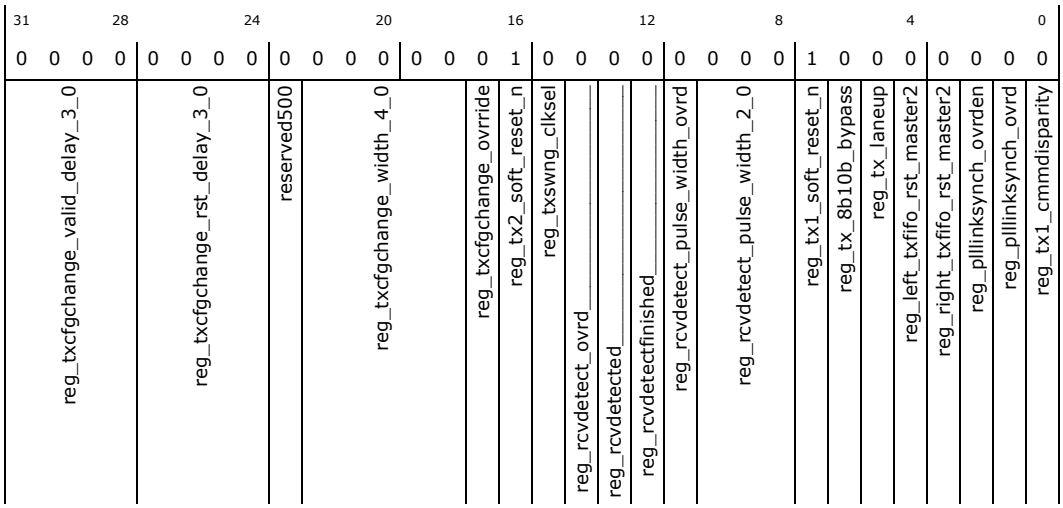
Type: Message Bus Register (Size: 32 bits)

pcs_dword0: [Port: 0xA6] + (200h + 0h)

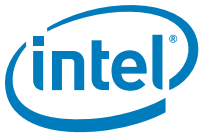
Op Codes:

0h - Read, 1h - Write

Default: 00010080h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd_____:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected_____:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished_____:** override for rcvdetectfinished



Bit Range	Default & Access	Description
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

18.7.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

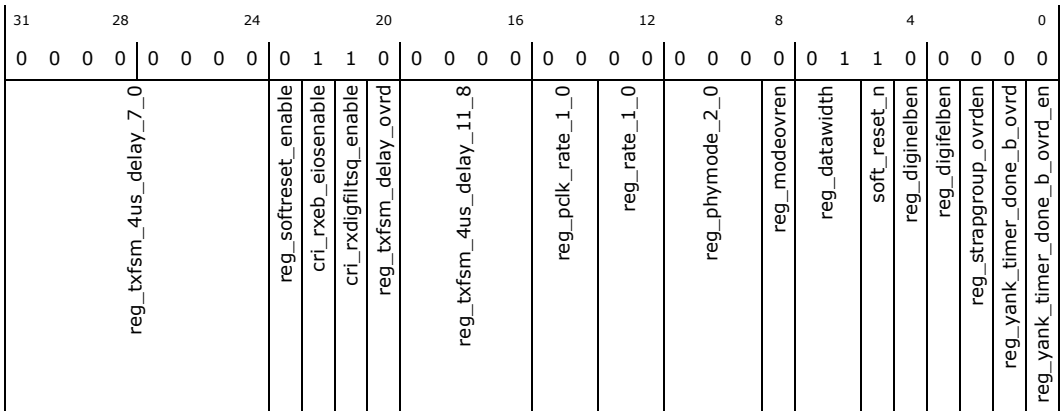
Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA6] + (200h + 4h)

Op Codes:

0h - Read, 1h - Write

Default: 00600060h



Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width

Bit Range	Default & Access	Description
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

18.7.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

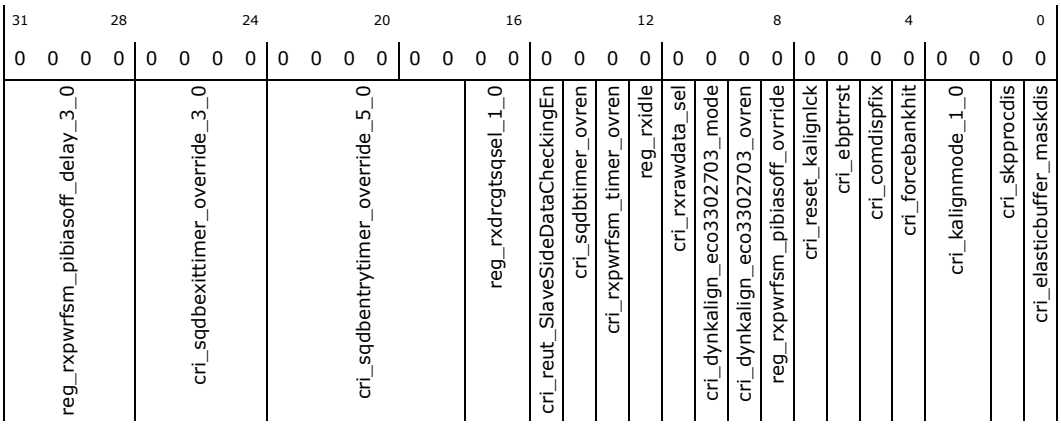
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword2: [Port: 0xA6] + (200h + 8h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave

Bit Range	Default & Access	Description
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

18.7.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

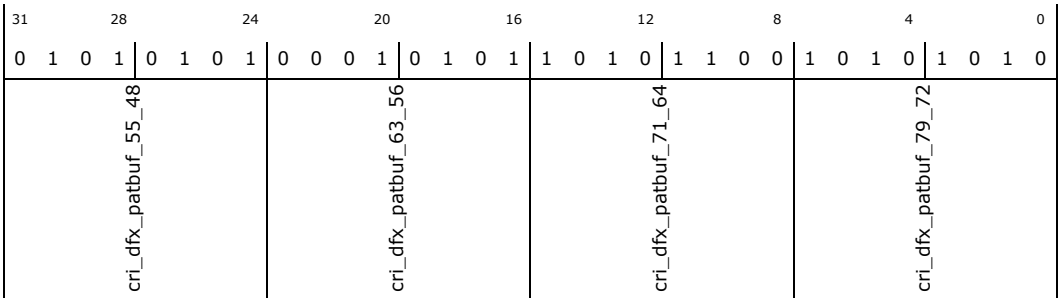
Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA6] + (200h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 5515ACAAh



Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.7.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword4: [Port: 0xA6] + (200h + 10h)

Op Codes:

0h - Read, 1h - Write

Default: 575555C1h

Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

Bit Range	Default & Access	Description
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.7.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

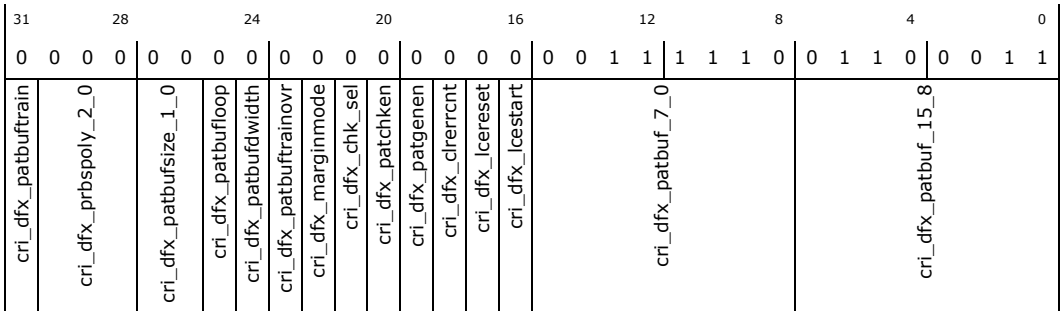
Type: Message Bus Register (Size: 32 bits)

pcs_dword5: [Port: 0xA6] + (200h + 14h)

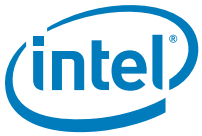
Op Codes:

0h - Read, 1h - Write

Default: 00003E63h



Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training



Bit Range	Default & Access	Description
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass multiplexes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.7.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

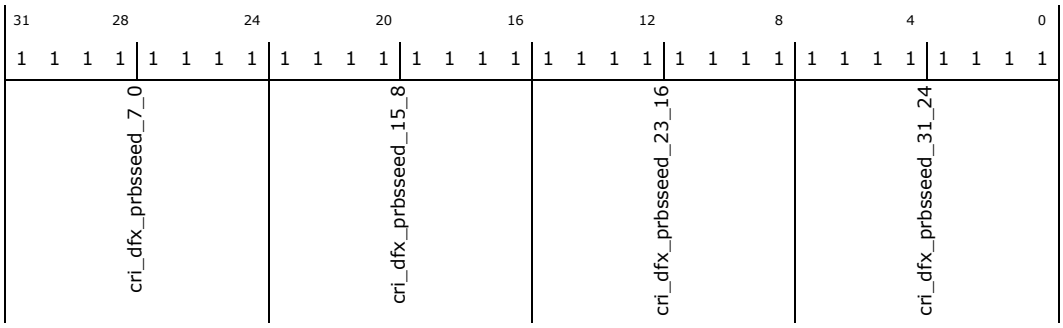
Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA6] + (200h + 18h)

Op Codes:

0h - Read, 1h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

18.7.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

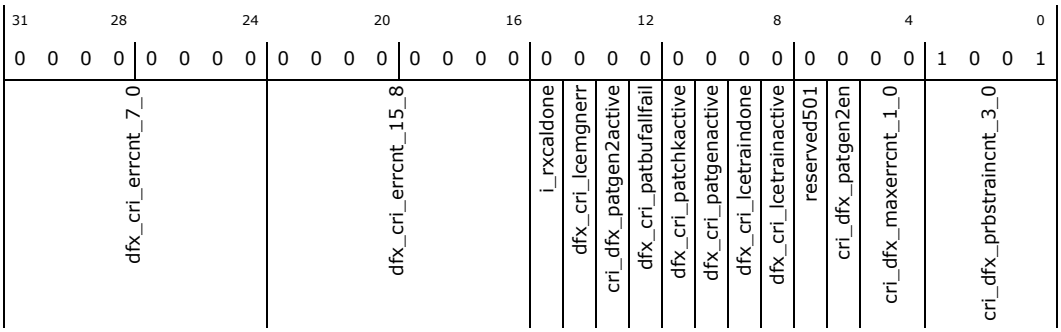
Type: Message Bus Register (Size: 32 bits)

pcs_dword7: [Port: 0xA6] + (200h + 1Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000009h



Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator

Bit Range	Default & Access	Description
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

18.7.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

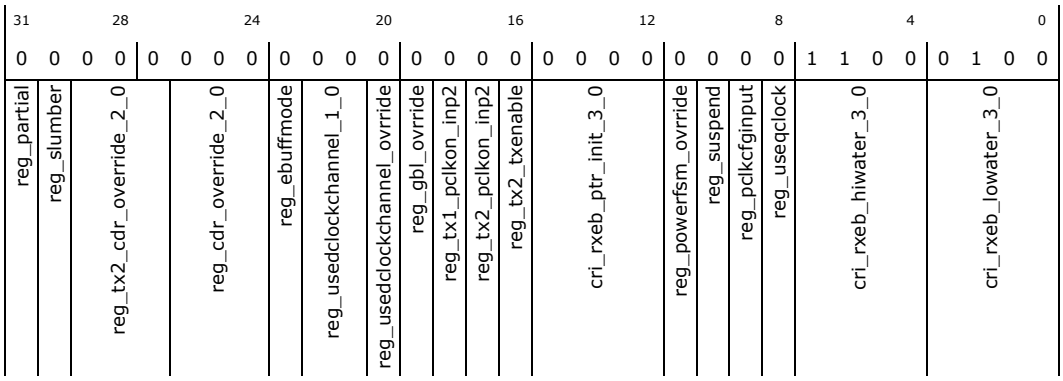
Type: Message Bus Register (Size: 32 bits)

pcs_dword8: [Port: 0xA6] + (200h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 000000C4h



Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1

Bit Range	Default & Access	Description
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

18.7.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

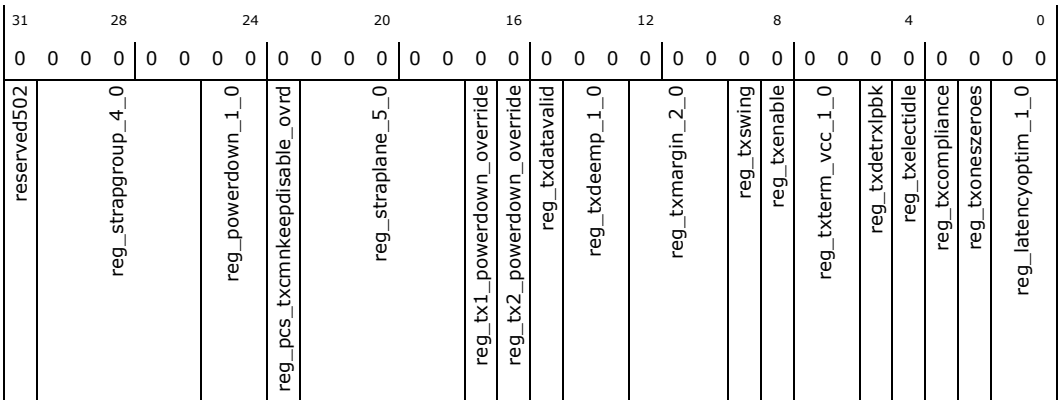
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword9: [Port: 0xA6] + (200h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup

Bit Range	Default & Access	Description
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

18.7.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

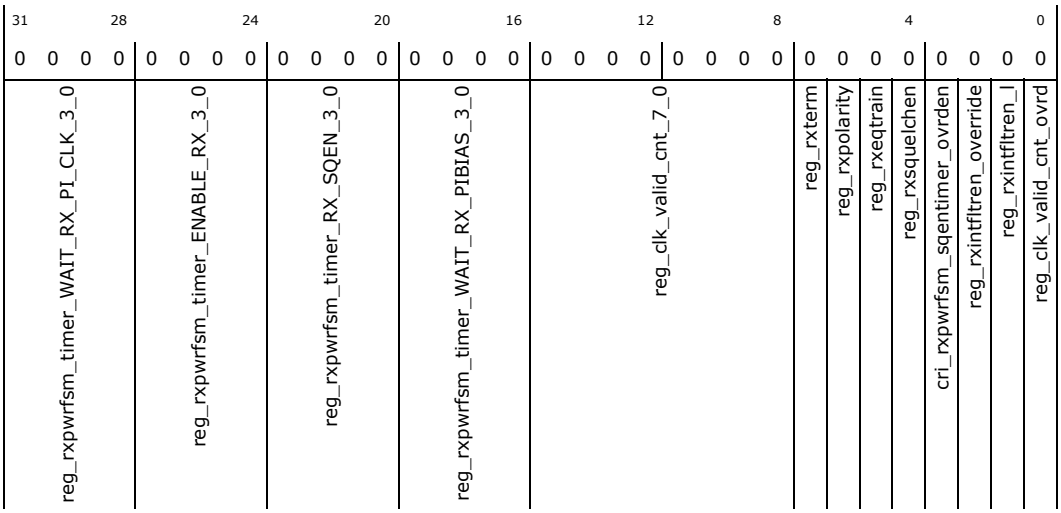
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword10: [Port: 0xA6] + (200h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).

Bit Range	Default & Access	Description
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

18.7.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

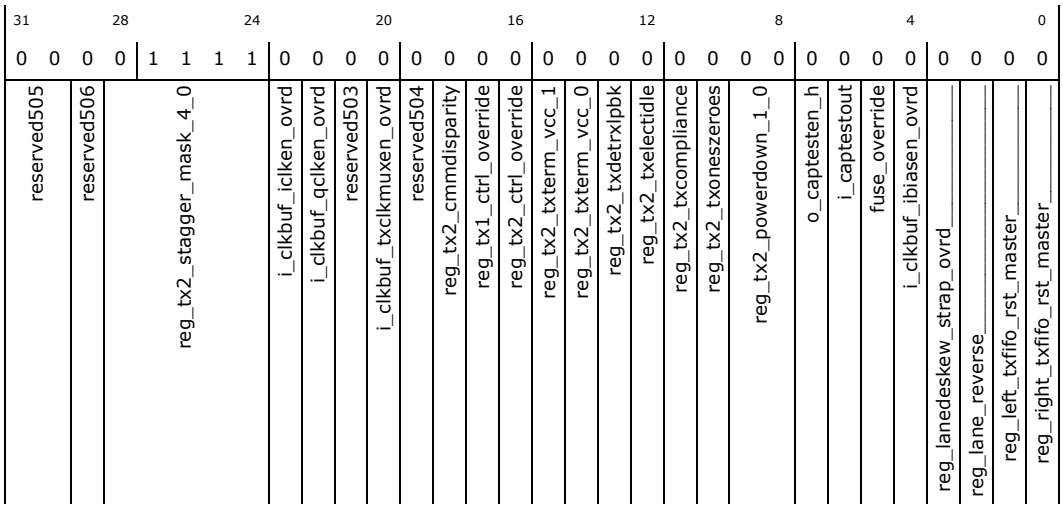
Type: Message Bus Register (Size: 32 bits)

pcs_dword11: [Port: 0xA6] + (200h + 2Ch)

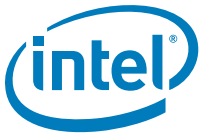
Op Codes:

0h - Read, 1h - Write

Default: 0F000000h



Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved



Bit Range	Default & Access	Description
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd_____:** reserved
2	0h RW	**reg_lane_reverse_____:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____:** reserved
0	0h RW	**reg_right_txfifo_rst_master_____:** reserved

18.7.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

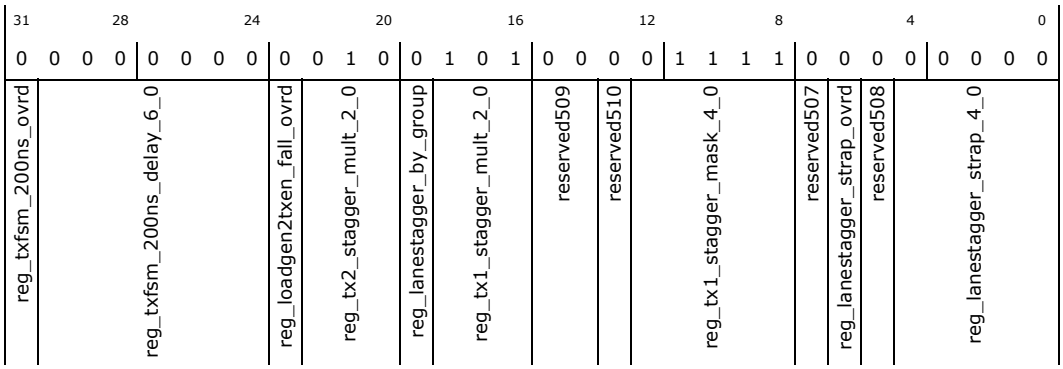
Type: Message Bus Register (Size: 32 bits)

pcs_dword12: [Port: 0xA6] + (200h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00250F00h



Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

18.7.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

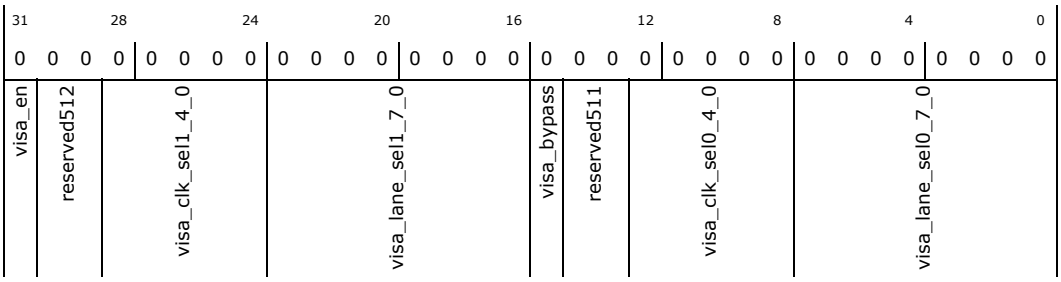
Type: Message Bus Register (Size: 32 bits)

pcs_dword13: [Port: 0xA6] + (200h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

18.7.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

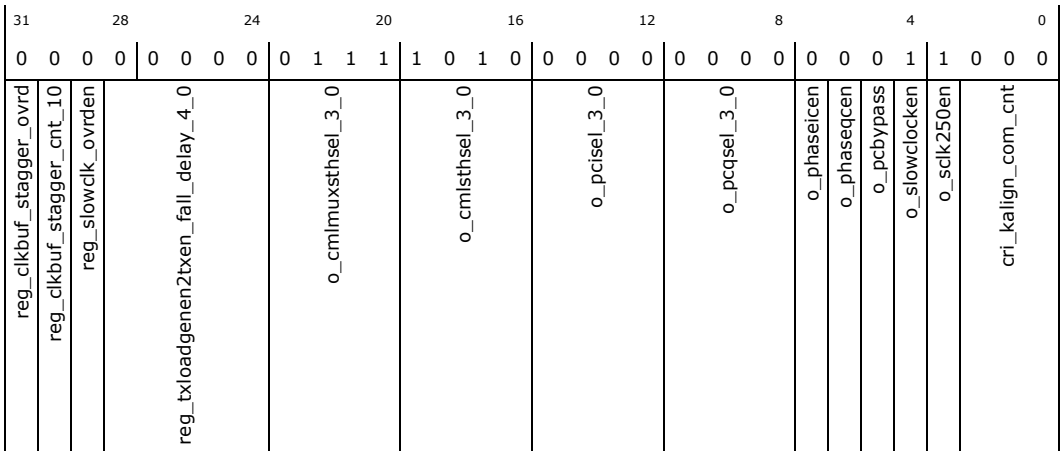
Type: Message Bus Register (Size: 32 bits)

pcs_dword14: [Port: 0xA6] + (200h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 007A0018h



Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.

Bit Range	Default & Access	Description
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

18.7.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

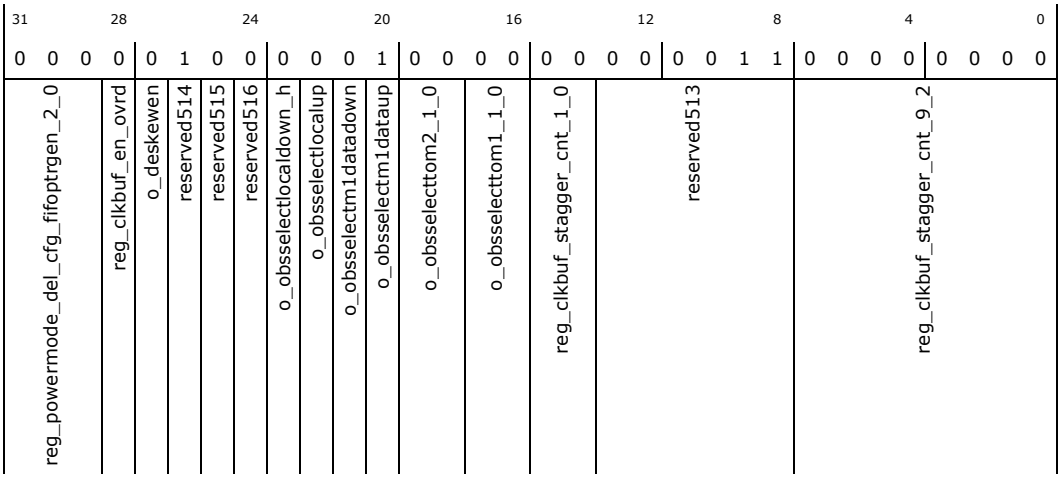
Type: Message Bus Register (Size: 32 bits)

pcs_dword15: [Port: 0xA6] + (200h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 04100300h



Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved

Bit Range	Default & Access	Description
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

18.7.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

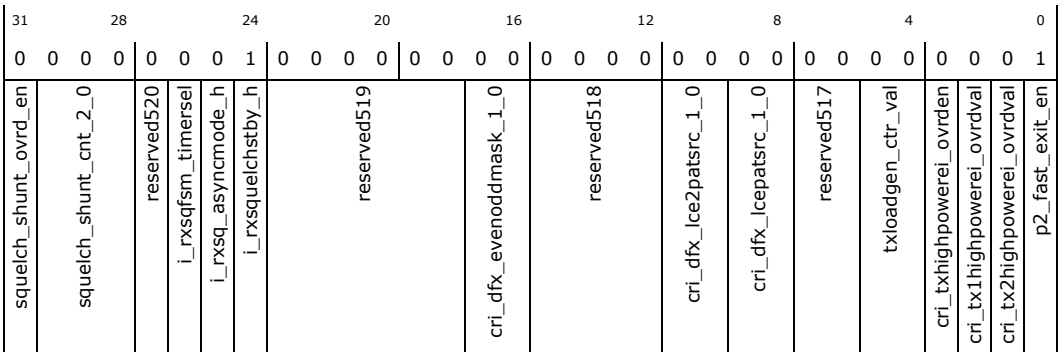
Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA6] + (200h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved

Bit Range	Default & Access	Description
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

18.7.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

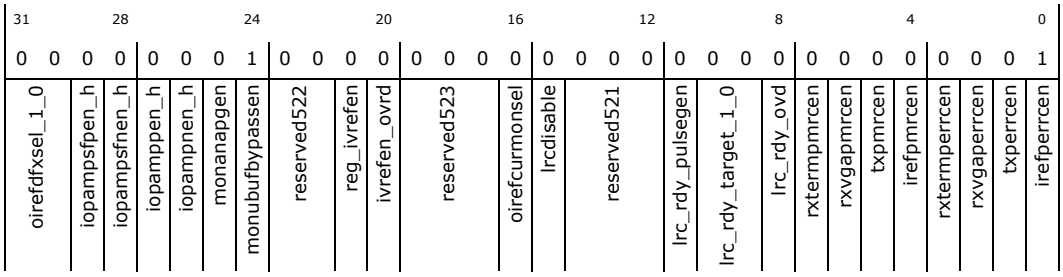
Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA6] + (200h + 44h)

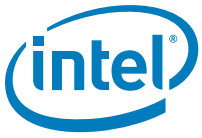
Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)



Bit Range	Default & Access	Description
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

Bit Range	Default & Access	Description
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

18.7.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

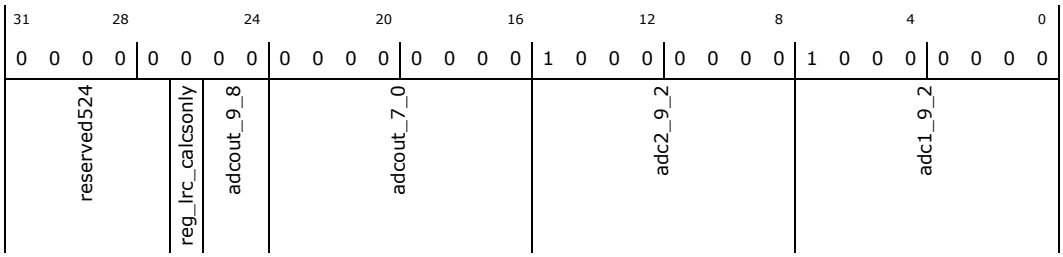
Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA6] + (200h + 48h)

Op Codes:

0h - Read, 1h - Write

Default: 00008080h



Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimation filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimation filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

18.7.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

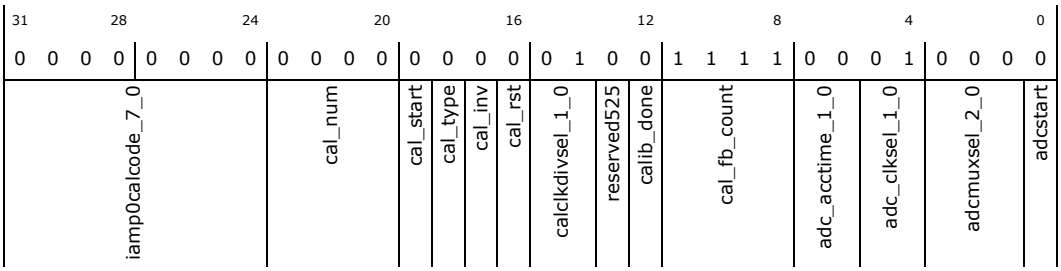
Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA6] + (200h + 4Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00004F10h



Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [Iyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.

Bit Range	Default & Access	Description
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

18.7.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

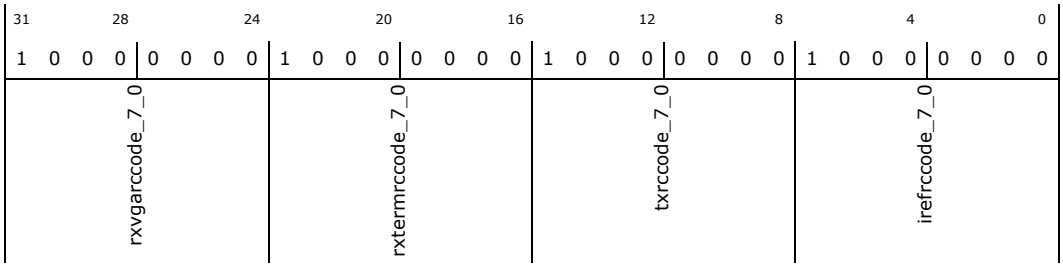
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA6] + (200h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

18.7.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

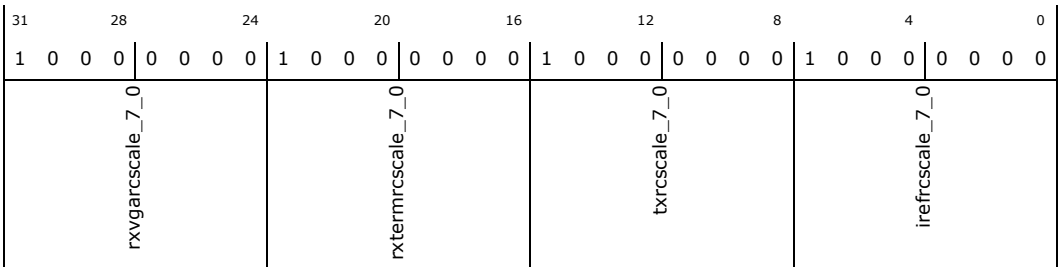
Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA6] + (200h + 54h)

Op Codes:

0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

18.7.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

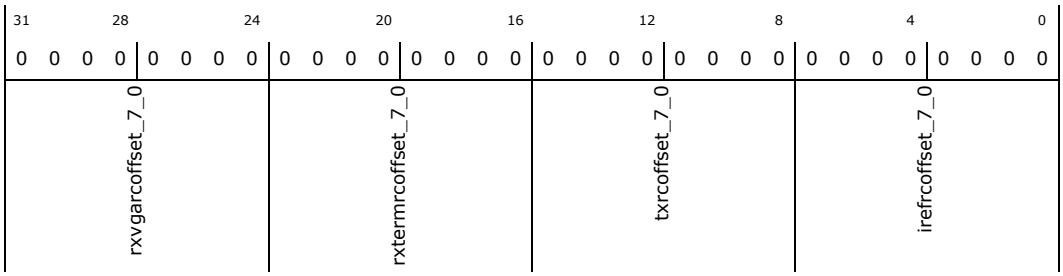
Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA6] + (200h + 58h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

18.7.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

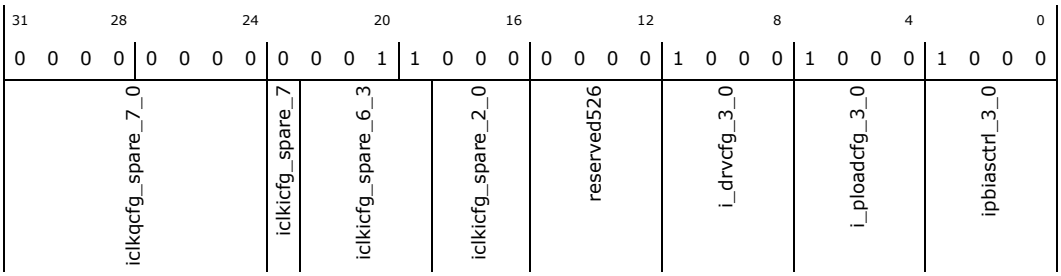
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA6] + (200h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h



Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

18.7.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

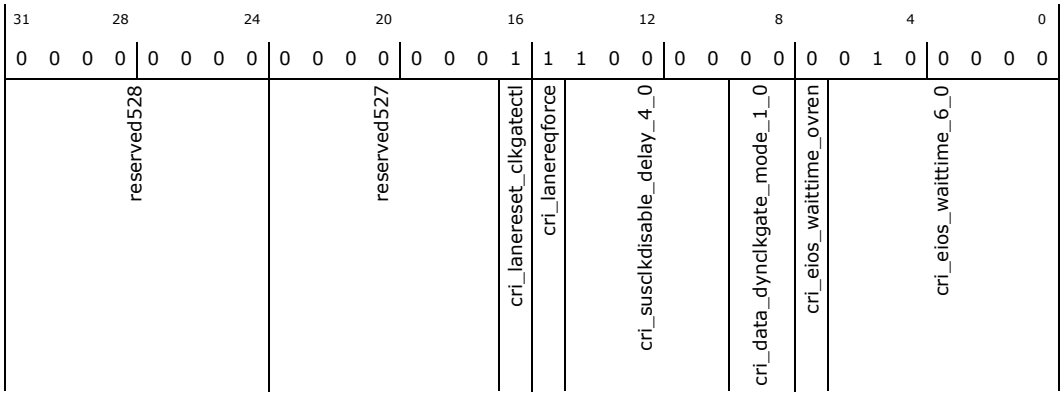
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword24: [Port: 0xA6] + (200h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h



Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (that is, 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay ..... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

18.8 PCI Express* Lane 0 Electrical Address Map

Table 135. Summary of PCI Express* Lane 0 Electrical Message Bus Registers—0xA6 (Global Offset 280h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 805	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 806	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 807	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 808	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 809	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 809	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 810	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 811	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 812	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 813	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 814	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 815	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 817	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 818	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 819	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 820	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 821	00008A00h

18.8.1 TX_DWORD0 (tx_dword0)—Offset 0h

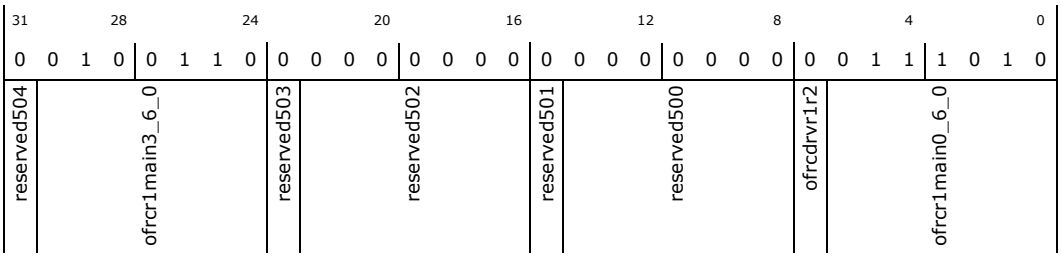
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword0: [Port: 0xA6] + (280h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah



Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

18.8.2 TX_DWORD1 (tx_dword1)—Offset 4h

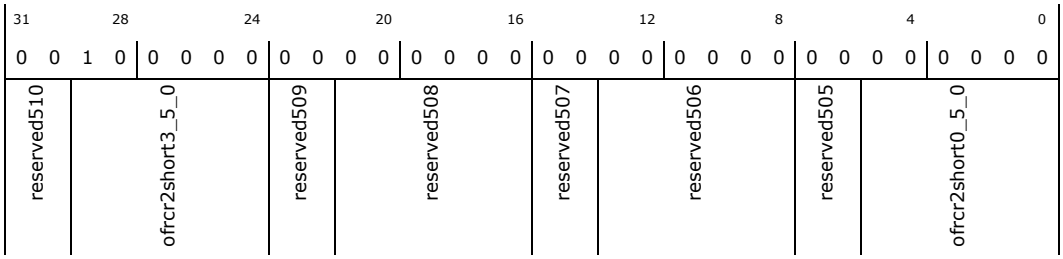
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword1: [Port: 0xA6] + (280h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

18.8.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

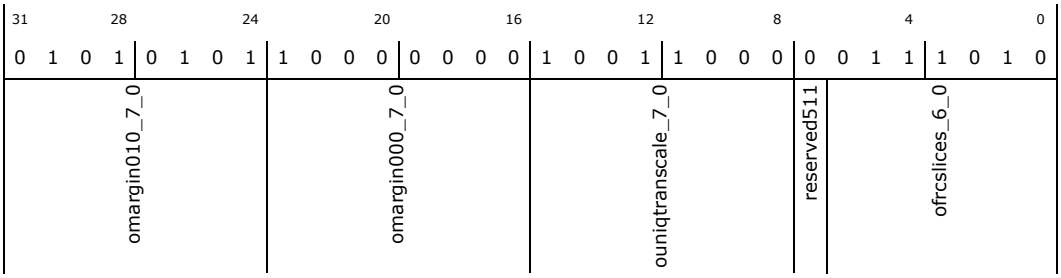
Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA6] + (280h + 8h)

Op Codes:

0h - Read, 1h - Write

Default: 5580983Ah



Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on dataratefit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

18.8.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

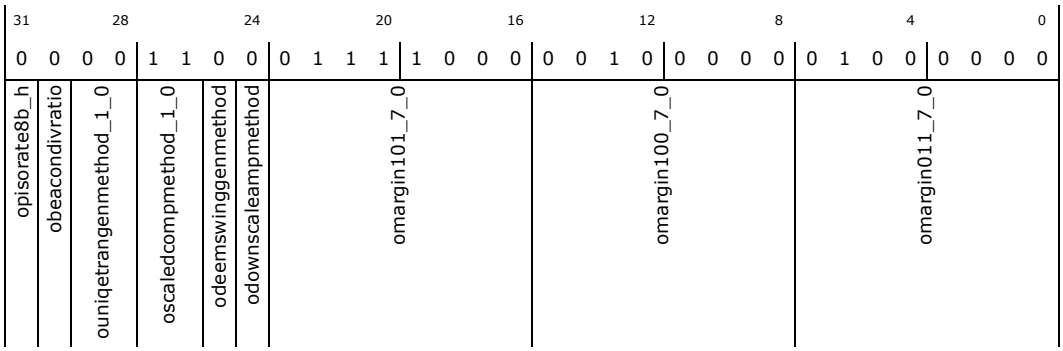
Type: Message Bus Register (Size: 32 bits)

tx_dword3: [Port: 0xA6] + (280h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0C782040h



Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

18.8.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

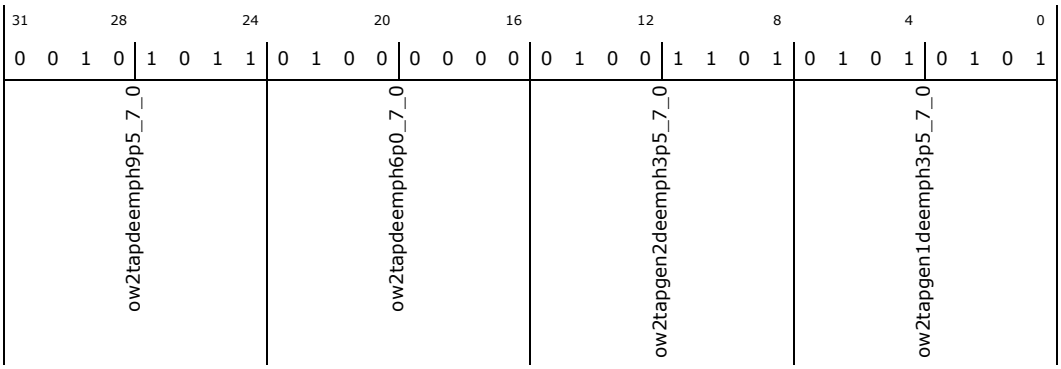
Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA6] + (280h + 10h)

Op Codes:

0h - Read, 1h - Write

Default: 2B404D55h



Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

18.8.6 TX_DWORD5 (tx_dword5)—Offset 14h

Access Method

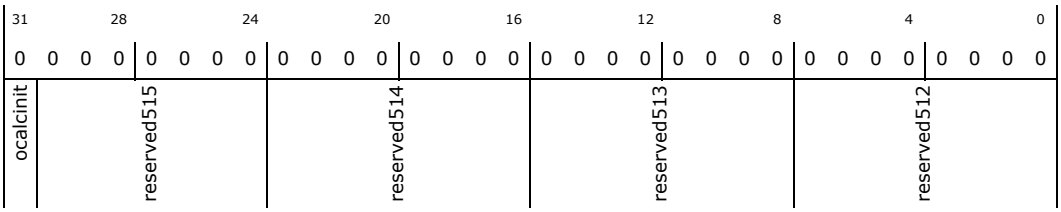
Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA6] + (280h + 14h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

18.8.7 TX_DWORD6 (tx_dword6)—Offset 18h

Access Method

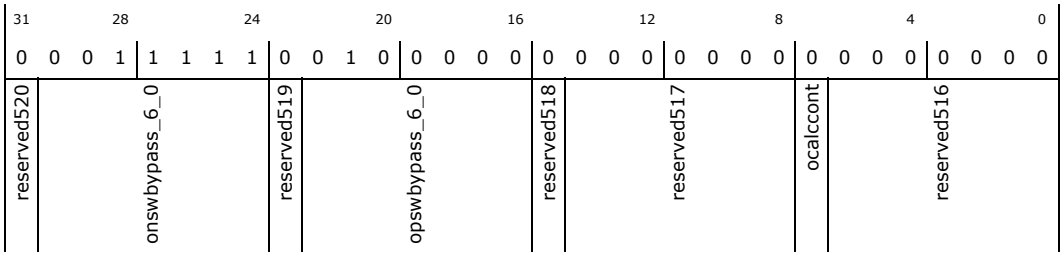
Type: Message Bus Register (Size: 32 bits)

tx_dword6: [Port: 0xA6] + (280h + 18h)

Op Codes:

0h - Read, 1h - Write

Default: 1F200000h



Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively
6:0	0h RO	**reserved516:** reserved

18.8.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

Access Method

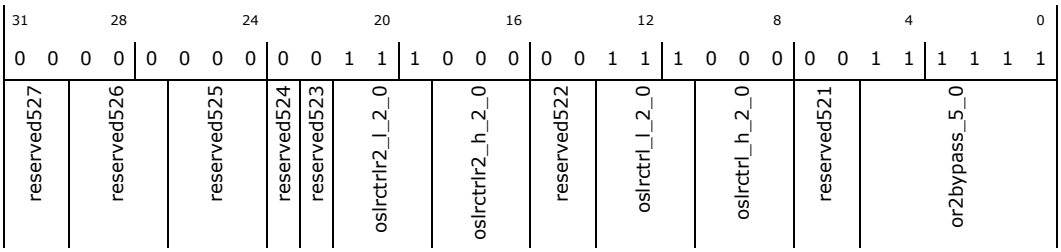
Type: Message Bus Register (Size: 32 bits)

tx_dword7: [Port: 0xA6] + (280h + 1Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0038383Fh



Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

18.8.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

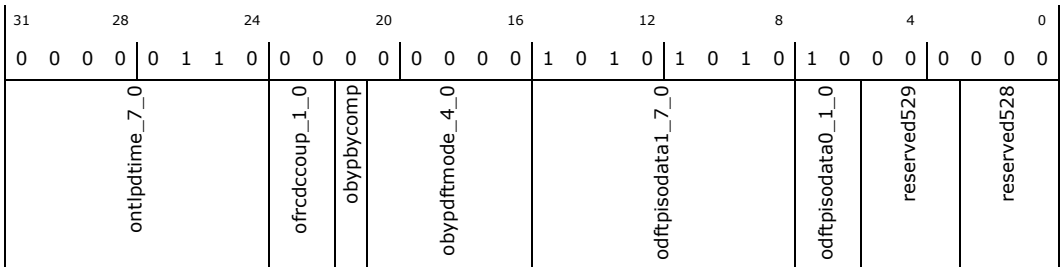
Type: Message Bus Register (Size: 32 bits)

tx_dword8: [Port: 0xA6] + (280h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 0600AA80h



Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

18.8.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

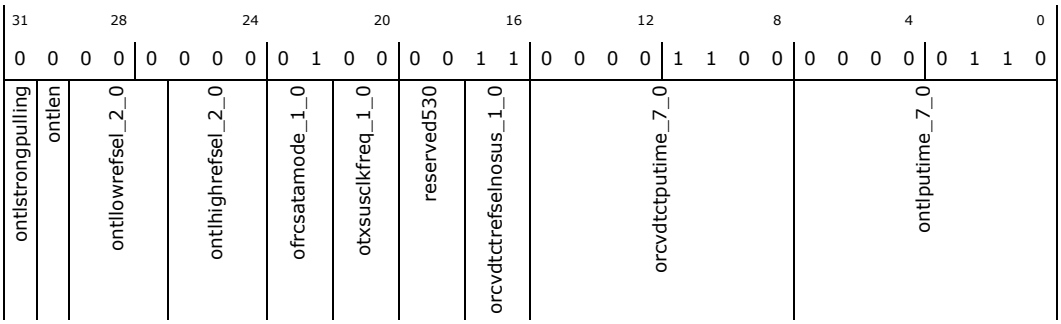
Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA6] + (280h + 24h)

Op Codes:

0h - Read, 1h - Write

Default: 00430C06h



Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

18.8.11 TX_DWORD10 (tx_dword10)—Offset 28h

Access Method

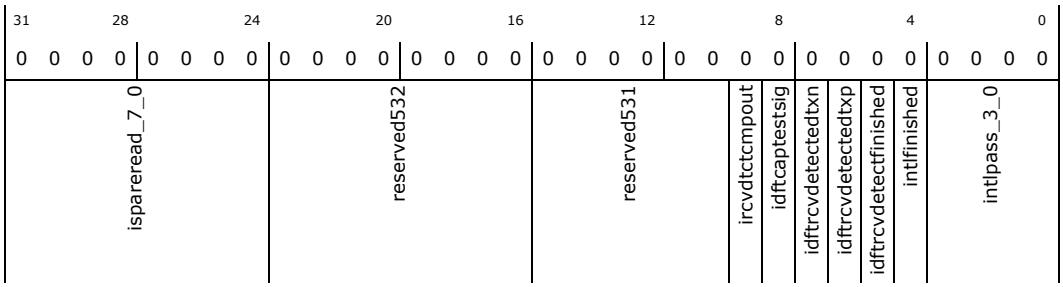
Type: Message Bus Register (Size: 32 bits)

tx_dword10: [Port: 0xA6] + (280h + 28h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

18.8.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

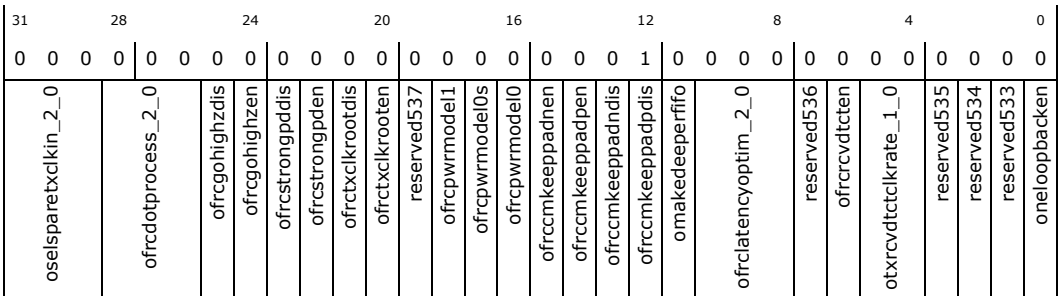
Type: Message Bus Register (Size: 32 bits)

tx_dword11: [Port: 0xA6] + (280h + 2Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00001000h



Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN

Bit Range	Default & Access	Description
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

18.8.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

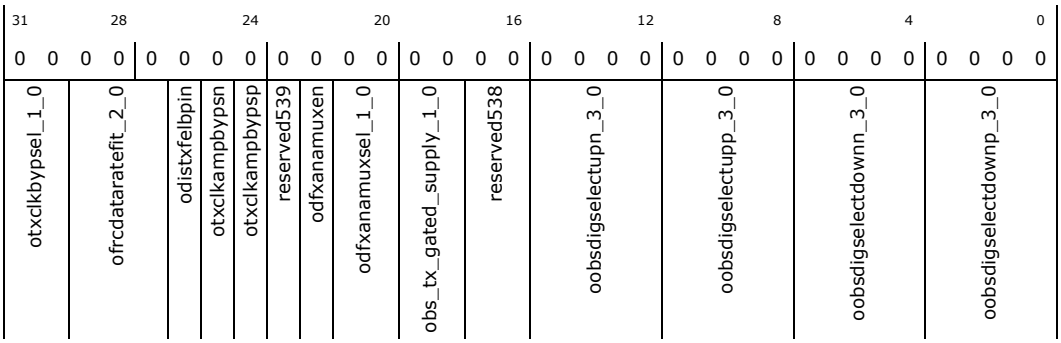
Type: Message Bus Register (Size: 32 bits)

tx_dword12: [Port: 0xA6] + (280h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - dataratefit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - dataratefit must be '11'
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]

Bit Range	Default & Access	Description
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

18.8.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

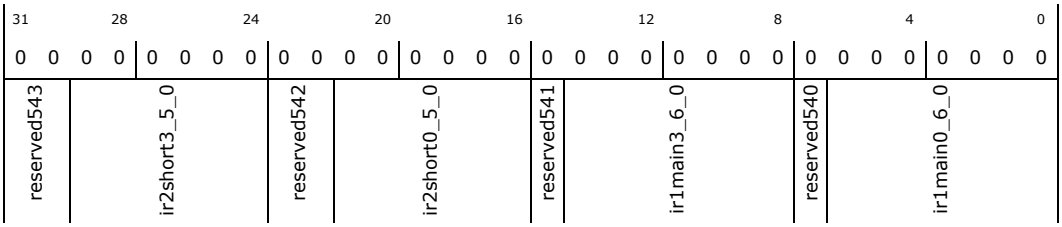
Type: Message Bus Register (Size: 32 bits)

tx_dword13: [Port: 0xA6] + (280h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

18.8.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

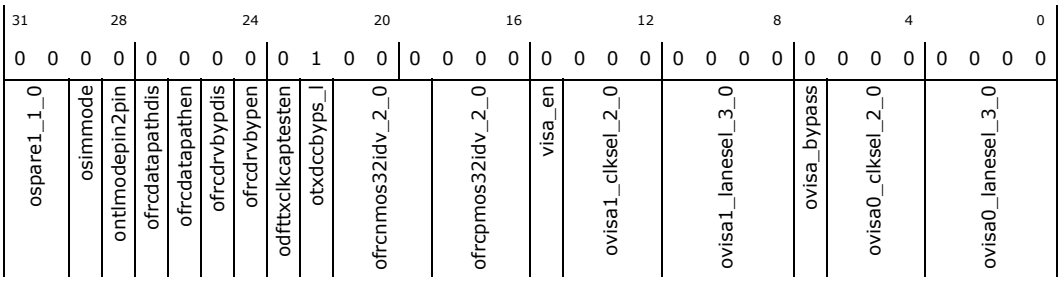
Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA6] + (280h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 00400000h



Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.

Bit Range	Default & Access	Description
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

18.8.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

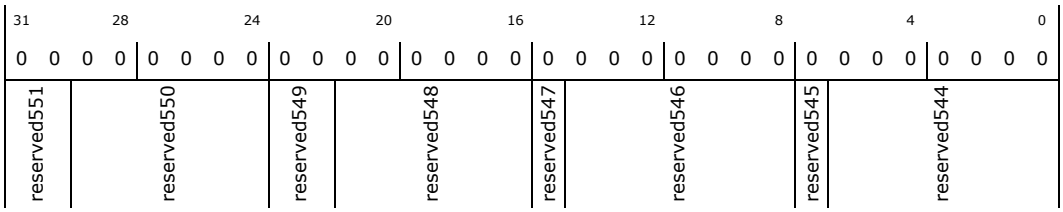
Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA6] + (280h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

18.8.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

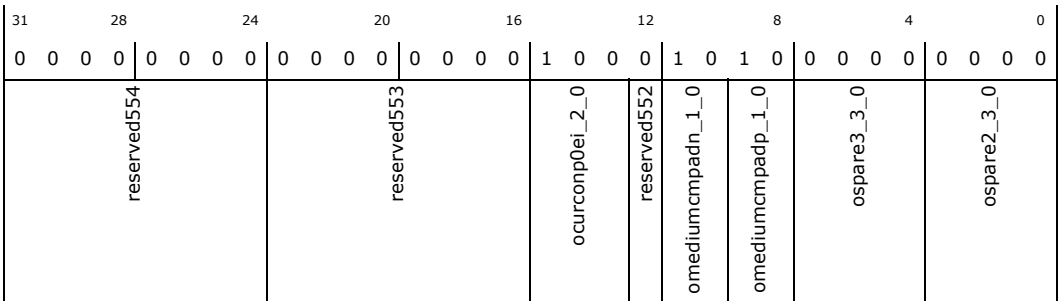
Type: Message Bus Register (Size: 32 bits)

tx_dword16: [Port: 0xA6] + (280h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 00008A00h



Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

18.9 PCI Express* Lane 1 Electrical Address Map

Table 136. Summary of PCI Express* Lane 1 Electrical Message Bus Registers—0xA6 (Global Offset 400h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 823	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 825	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 826	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 827	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 828	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 829	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 830	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 831	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 832	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 833	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 835	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 836	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 838	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 839	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 840	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 841	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 843	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 844	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 846	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 847	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 848	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 849	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 850	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 851	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 851	0001C020h

18.9.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

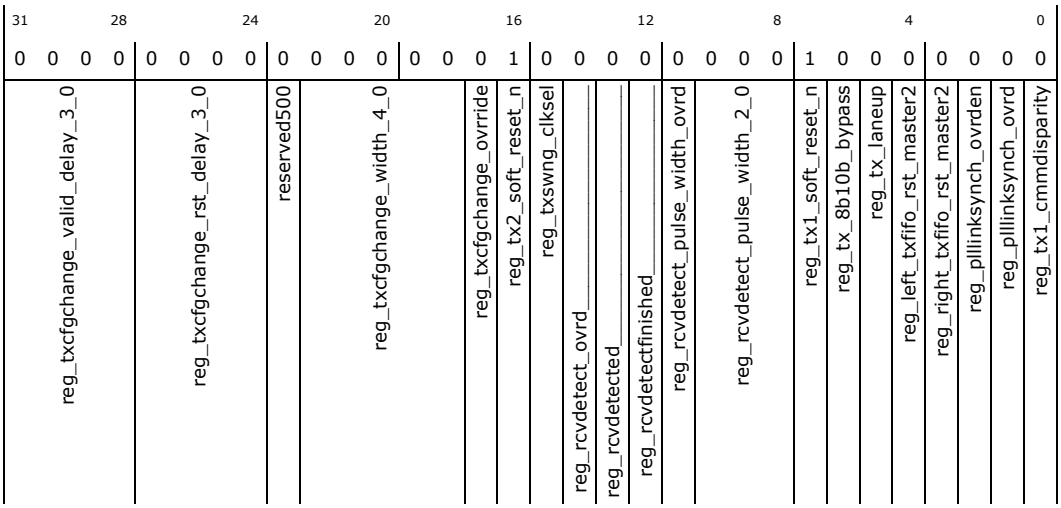
Type: Message Bus Register (Size: 32 bits)

pcs_dword0: [Port: 0xA6] + (400h + 0h)

Op Codes:

0h - Read, 1h - Write

Default: 00010080h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd_____:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected_____:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished_____:** override for rcvdetectfinished

Bit Range	Default & Access	Description
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

18.9.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

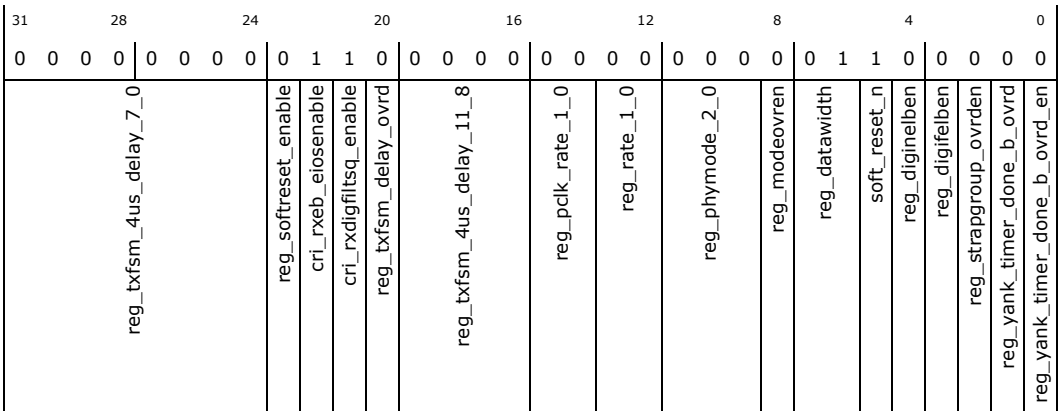
Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA6] + (400h + 4h)

Op Codes:

0h - Read, 1h - Write

Default: 00600060h



Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width

Bit Range	Default & Access	Description
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

18.9.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword2: [Port: 0xA6] + (400h + 8h)

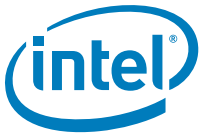
Op Codes:

0h - Read, 1h - Write

Default: 00000000h

31	28	24	20	16	12	8	4	0
0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0
reg_rxpwrfsm_pibiasoff_delay_3_0	cri_sqdbexittimer_override_3_0	cri_sqdbentrytimer_override_5_0	reg_rxdrcgtsqsel_1_0	cri_reut_SlaveSideDataCheckingEn	cri_sqdbtimer_ovren	cri_rxpwrfsm_timer_ovren	reg_rxidle	cri_rxrawdata_sel
cri_dynkalign_eco3302703_mode	cri_dynkalign_eco3302703_ovren	reg_rxpwrfsm_pibiasoff_ovrride	cri_reset_kalignlck	cri_ebptrrst	cri_comdispfix	cri_forcebankhit	cri_kalignmode_1_0	cri_skpprocdis
cri_elasticbuffer_maskdis								

Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select



Bit Range	Default & Access	Description
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

18.9.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

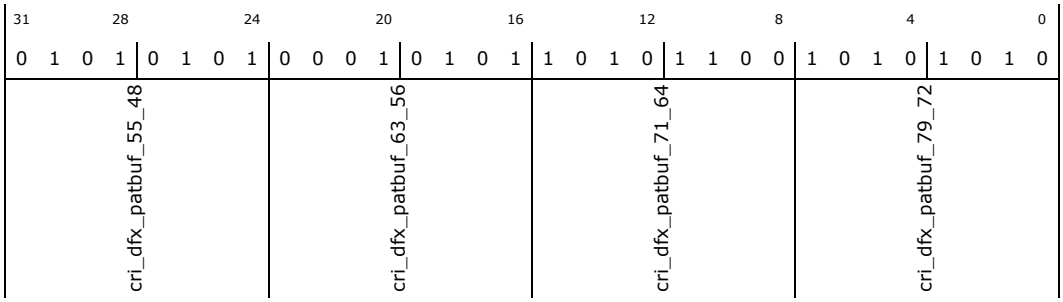
Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA6] + (400h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 5515ACAAh



Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.9.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

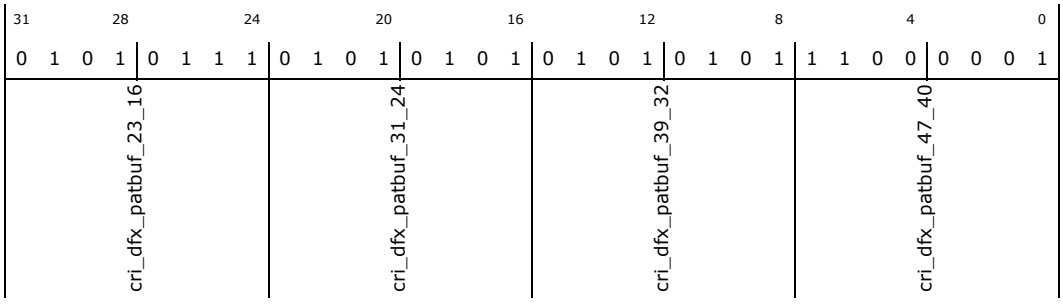
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword4: [Port: 0xA6] + (400h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 575555C1h



Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.9.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

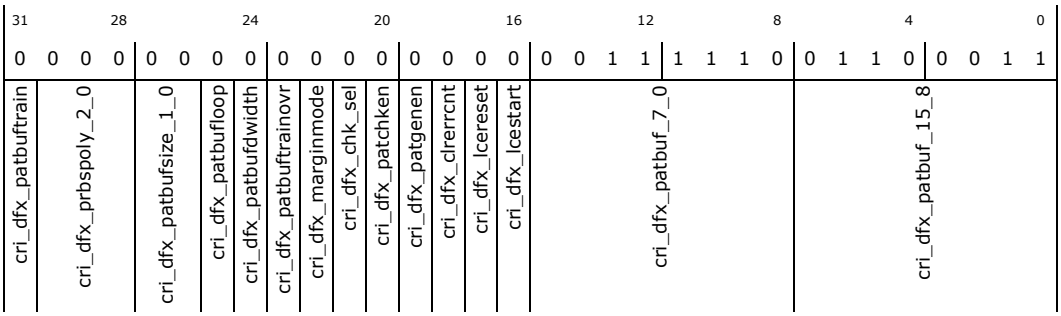
Type: Message Bus Register (Size: 32 bits)

pcs_dword5: [Port: 0xA6] + (400h + 14h)

Op Codes:

0h - Read, 1h - Write

Default: 00003E63h



Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker

Bit Range	Default & Access	Description
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.9.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

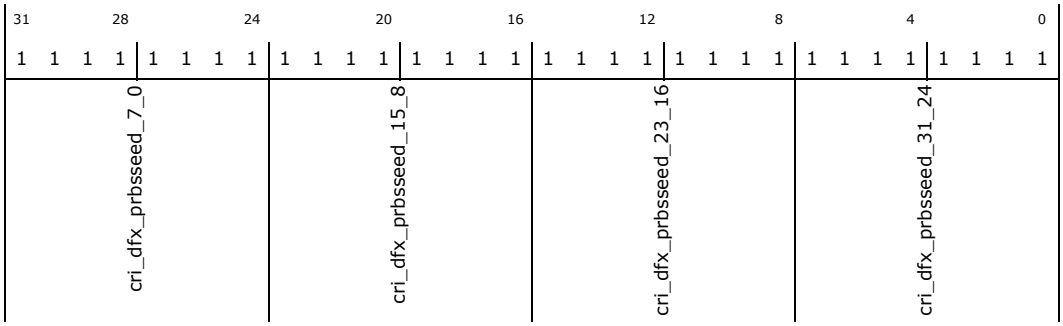
Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA6] + (400h + 18h)

Op Codes:

0h - Read, 1h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

18.9.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

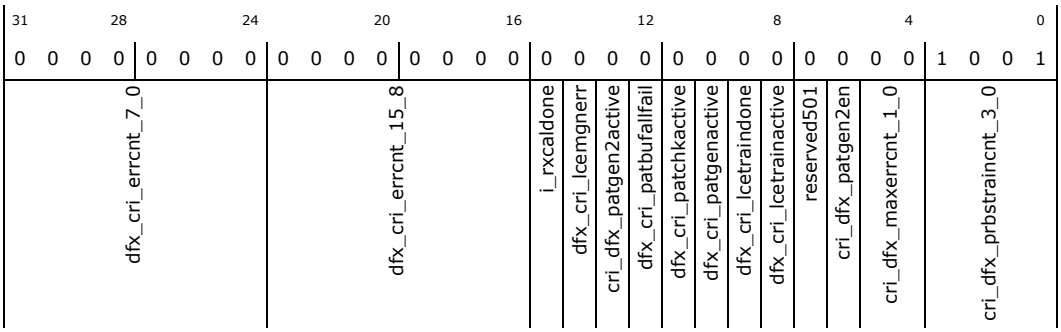
Type: Message Bus Register (Size: 32 bits)

pcs_dword7: [Port: 0xA6] + (400h + 1Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000009h



Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator

Bit Range	Default & Access	Description
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

18.9.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

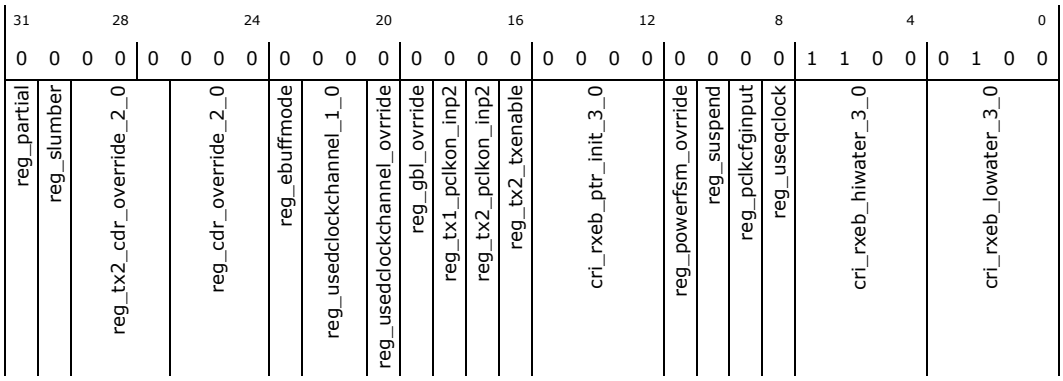
Type: Message Bus Register (Size: 32 bits)

pcs_dword8: [Port: 0xA6] + (400h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 000000C4h



Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1

Bit Range	Default & Access	Description
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

18.9.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

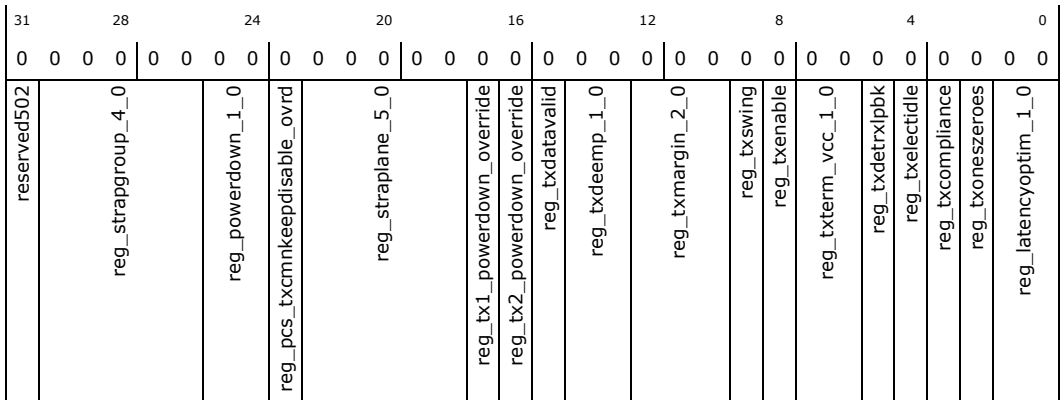
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword9: [Port: 0xA6] + (400h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup

Bit Range	Default & Access	Description
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

18.9.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

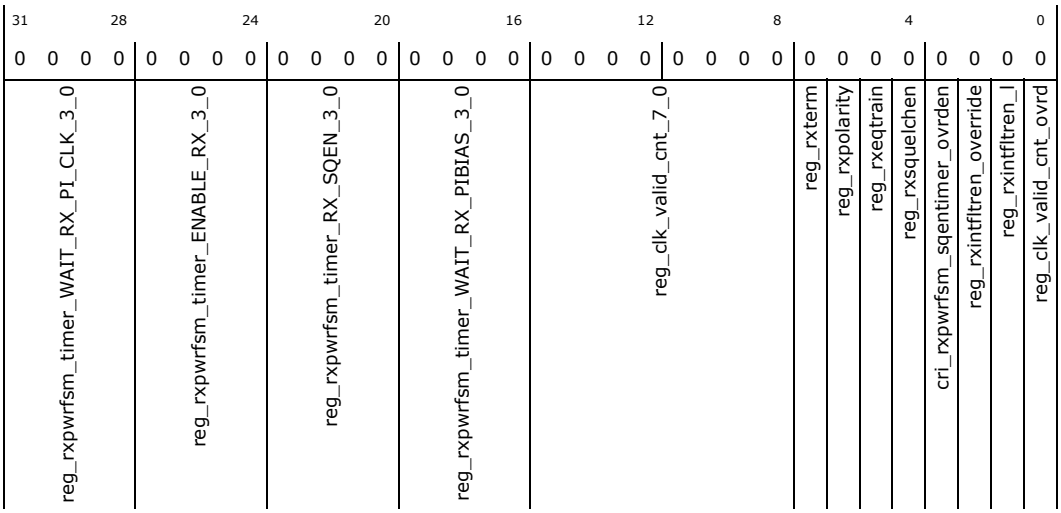
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword10: [Port: 0xA6] + (400h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).

Bit Range	Default & Access	Description
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

18.9.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

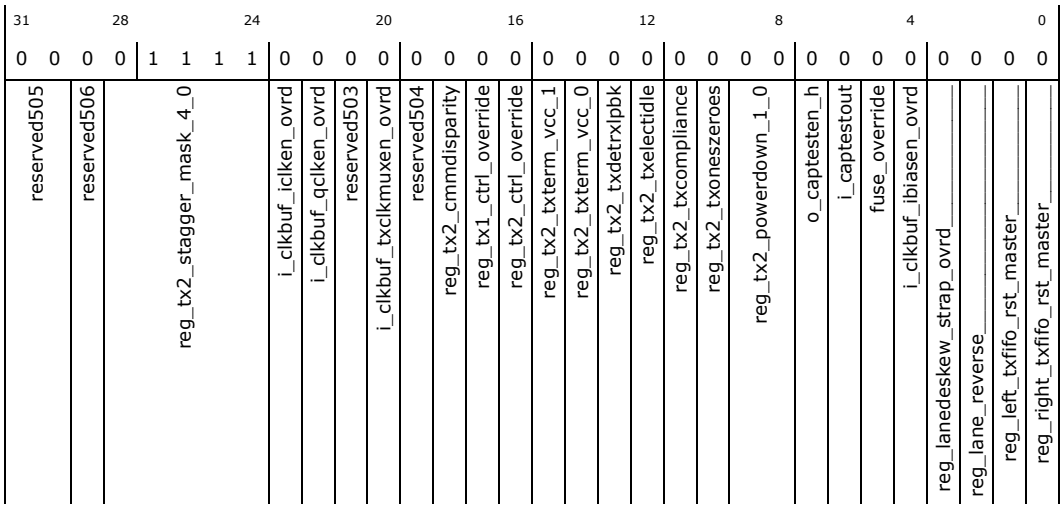
Type: Message Bus Register (Size: 32 bits)

pcs_dword11: [Port: 0xA6] + (400h + 2Ch)

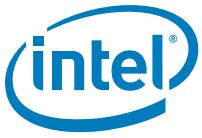
Op Codes:

0h - Read, 1h - Write

Default: 0F000000h



Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved



Bit Range	Default & Access	Description
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd_____:** reserved
2	0h RW	**reg_lane_reverse_____:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____:** reserved
0	0h RW	**reg_right_txfifo_rst_master_____:** reserved

18.9.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

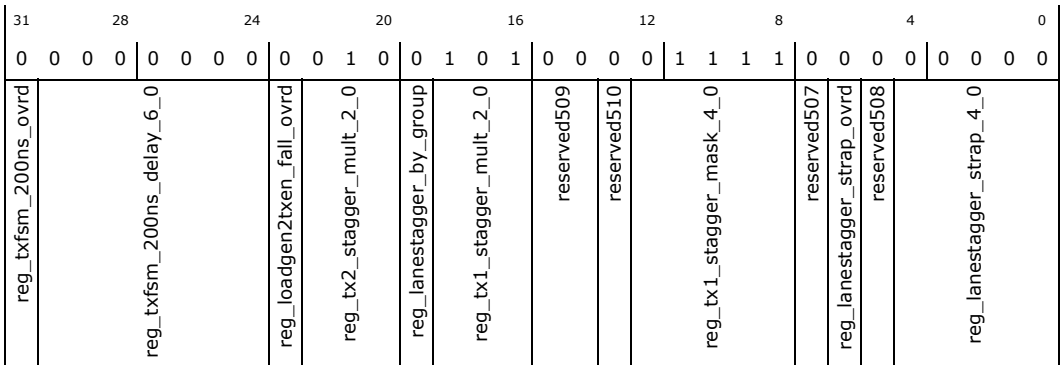
Type: Message Bus Register (Size: 32 bits)

pcs_dword12: [Port: 0xA6] + (400h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00250F00h



Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved

Bit Range	Default & Access	Description
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

18.9.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

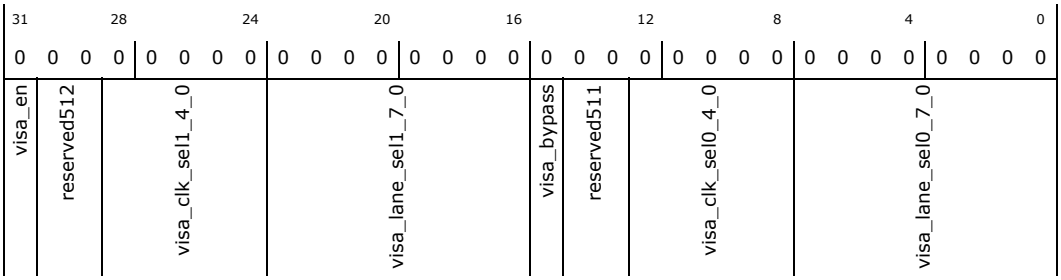
Type: Message Bus Register (Size: 32 bits)

pcs_dword13: [Port: 0xA6] + (400h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

18.9.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

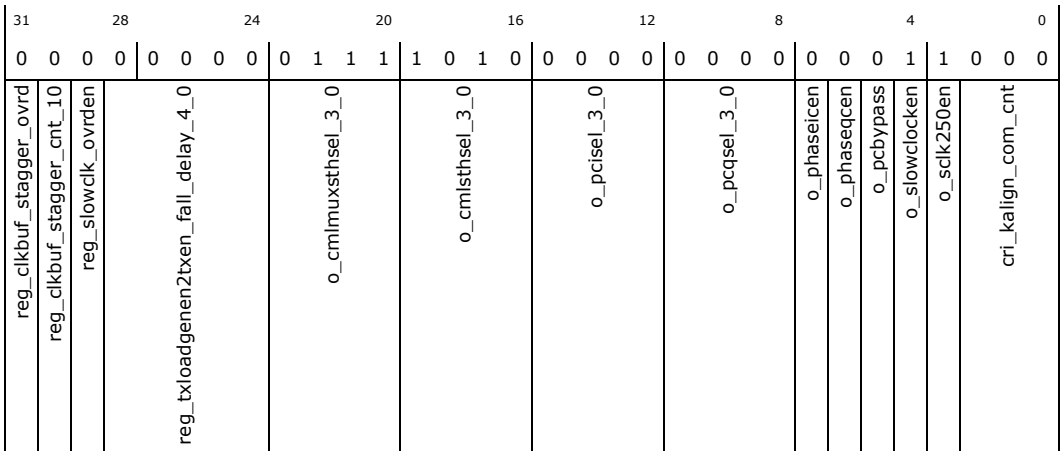
Type: Message Bus Register (Size: 32 bits)

pcs_dword14: [Port: 0xA6] + (400h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 007A0018h



Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.

Bit Range	Default & Access	Description
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

18.9.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

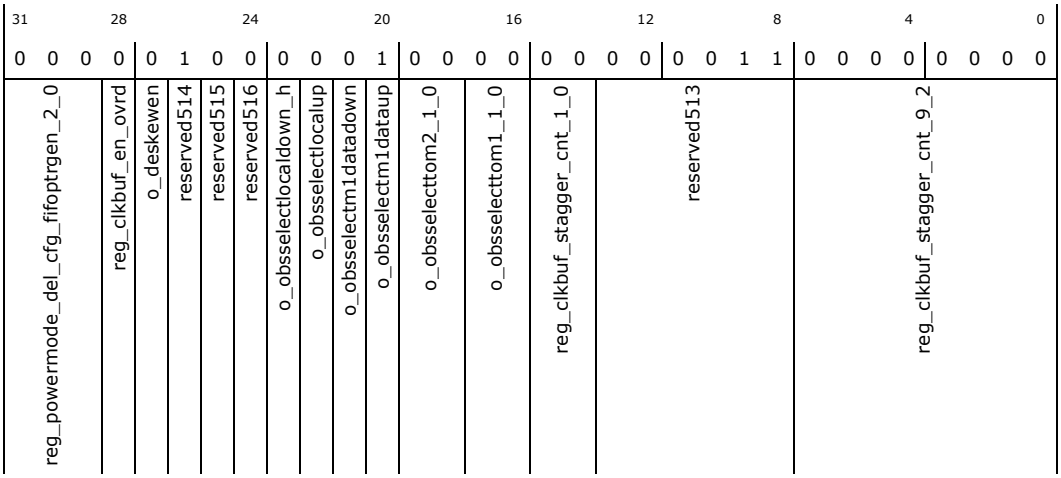
Type: Message Bus Register (Size: 32 bits)

pcs_dword15: [Port: 0xA6] + (400h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 04100300h



Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved

Bit Range	Default & Access	Description
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

18.9.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

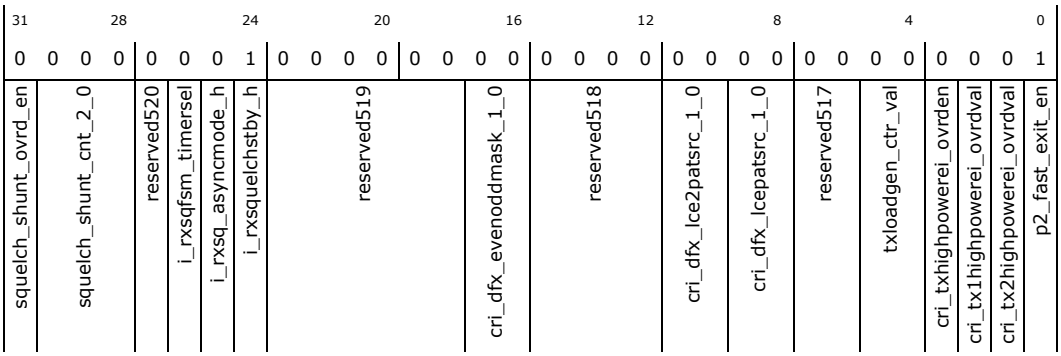
Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA6] + (400h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved

Bit Range	Default & Access	Description
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

18.9.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

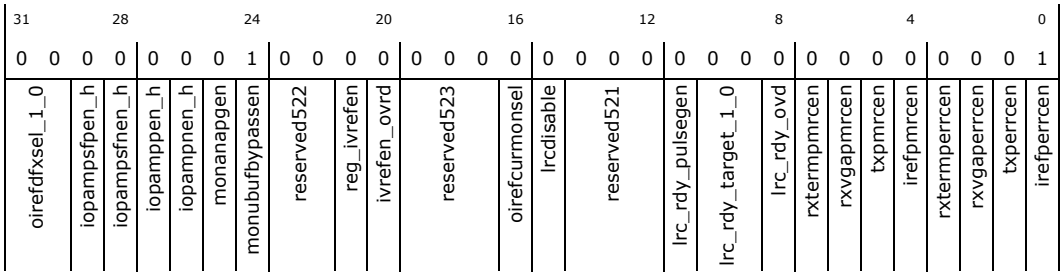
Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA6] + (400h + 44h)

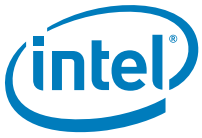
Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)



Bit Range	Default & Access	Description
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

Bit Range	Default & Access	Description
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

18.9.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

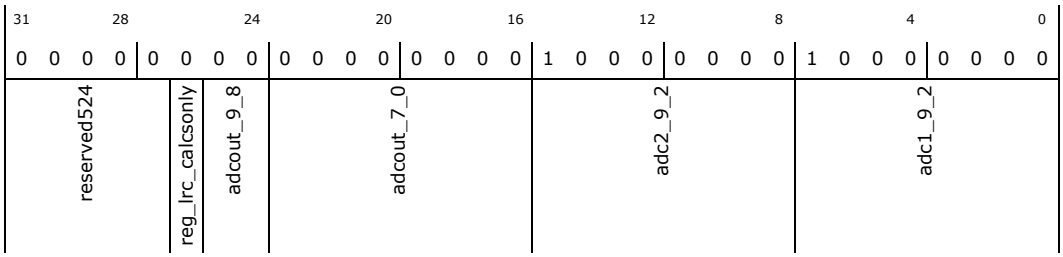
Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA6] + (400h + 48h)

Op Codes:

0h - Read, 1h - Write

Default: 00008080h



Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimation filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimation filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

18.9.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

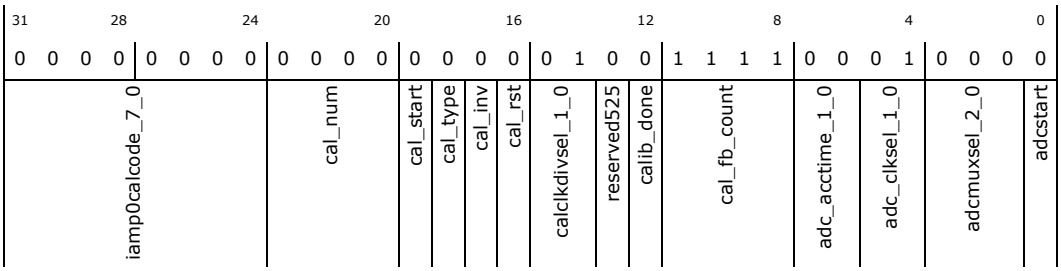
Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA6] + (400h + 4Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00004F10h



Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [Iyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.

Bit Range	Default & Access	Description
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

18.9.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

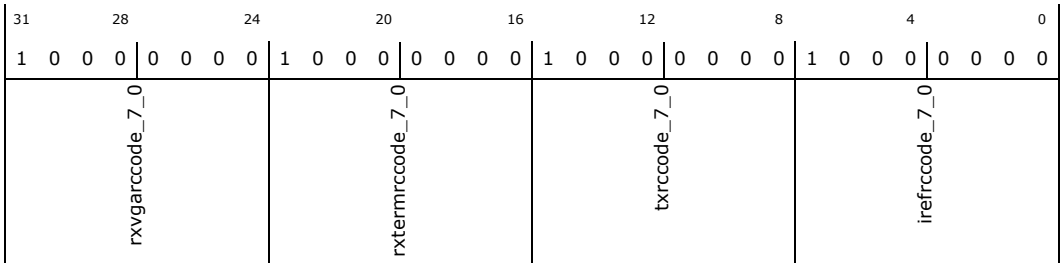
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA6] + (400h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

18.9.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

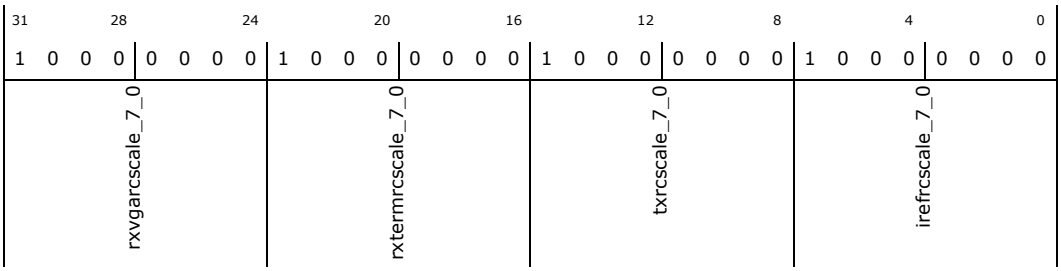
Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA6] + (400h + 54h)

Op Codes:

0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

18.9.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

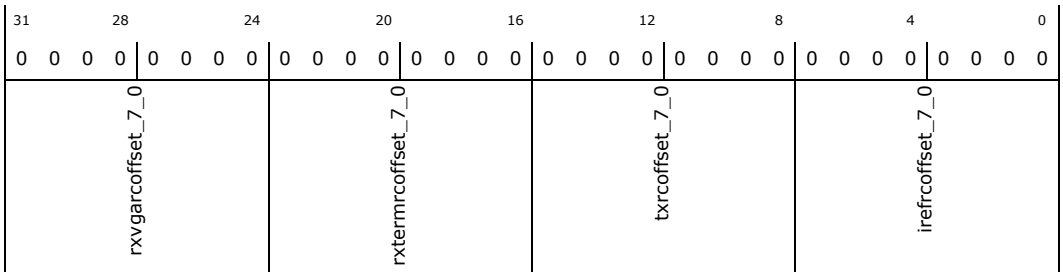
Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA6] + (400h + 58h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

18.9.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

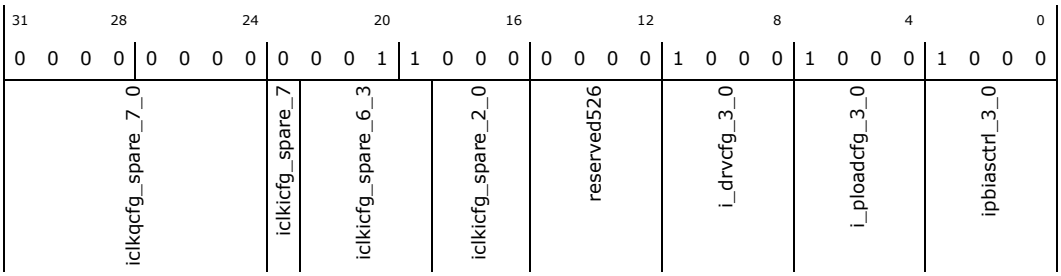
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA6] + (400h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h



Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

18.9.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

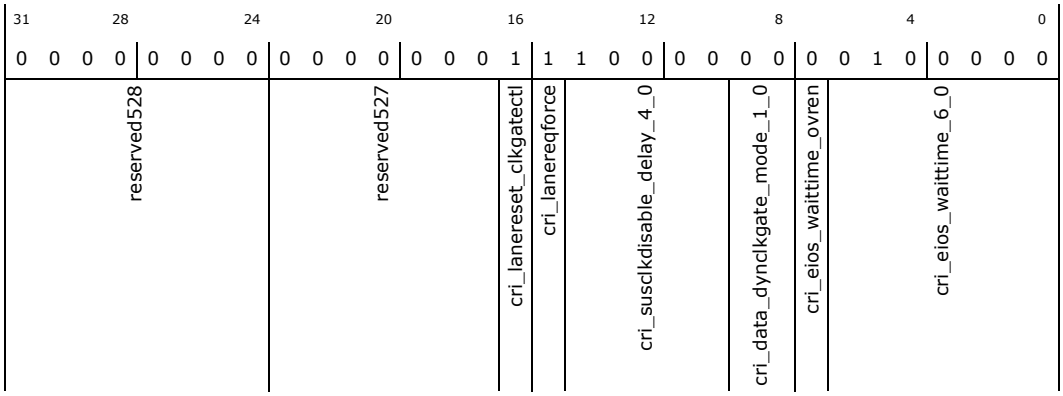
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword24: [Port: 0xA6] + (400h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h



Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (that is, 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay ..... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

18.10 PCI Express* Lane 1 Electrical Address Map

Table 137. Summary of PCI Express* Lane 1 Electrical Message Bus Registers—0xA6 (Global Offset 480h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 853	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 854	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 855	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 856	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 857	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 858	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 858	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 859	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 860	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 861	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 862	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 863	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 865	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 866	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 867	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 868	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 869	00008A00h

18.10.1 TX_DWORD0 (tx_dword0)—Offset 0h

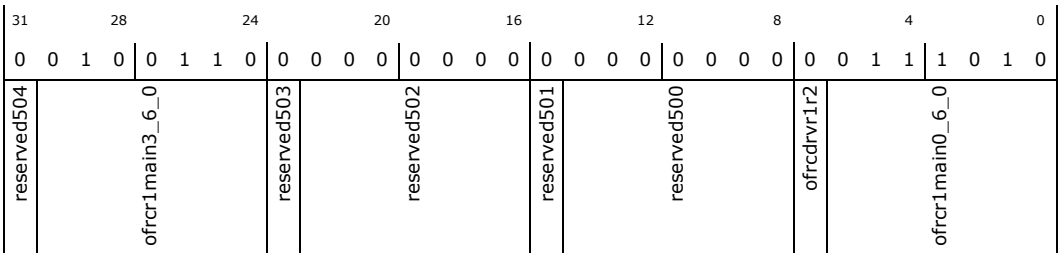
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword0: [Port: 0xA6] + (480h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah



Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

18.10.2 TX_DWORD1 (tx_dword1)—Offset 4h

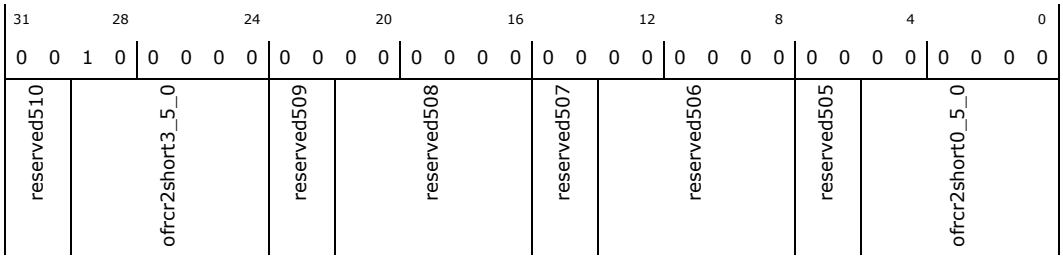
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword1: [Port: 0xA6] + (480h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

18.10.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

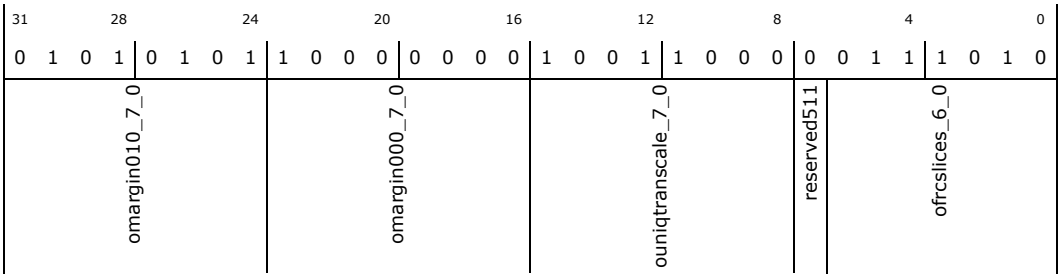
Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA6] + (480h + 8h)

Op Codes:

0h - Read, 1h - Write

Default: 5580983Ah



Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on dataratefit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

18.10.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

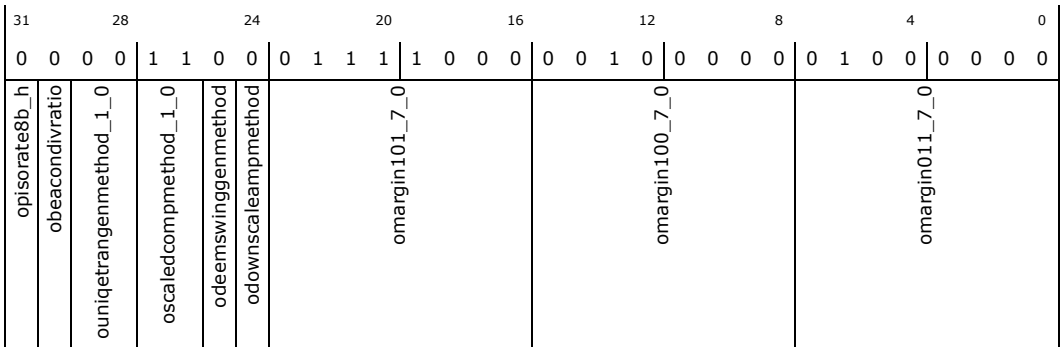
Type: Message Bus Register (Size: 32 bits)

tx_dword3: [Port: 0xA6] + (480h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0C782040h



Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p

Bit Range	Default & Access	Description
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

18.10.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

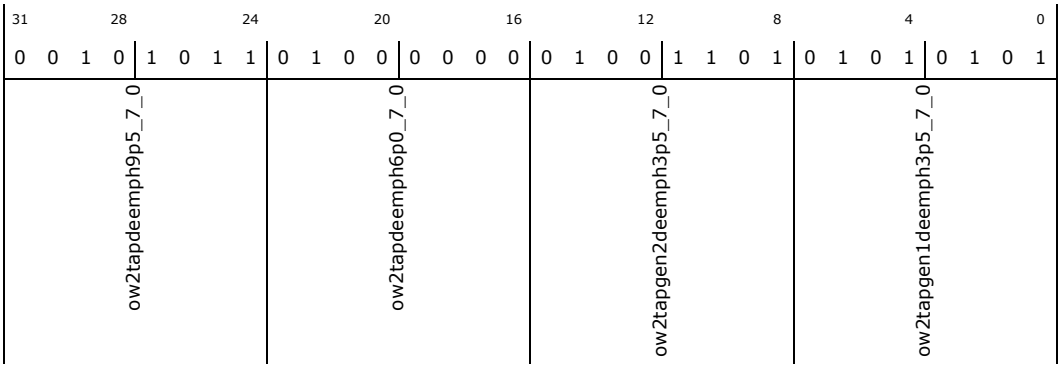
Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA6] + (480h + 10h)

Op Codes:

0h - Read, 1h - Write

Default: 2B404D55h



Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

18.10.6 TX_DWORD5 (tx_dword5)—Offset 14h

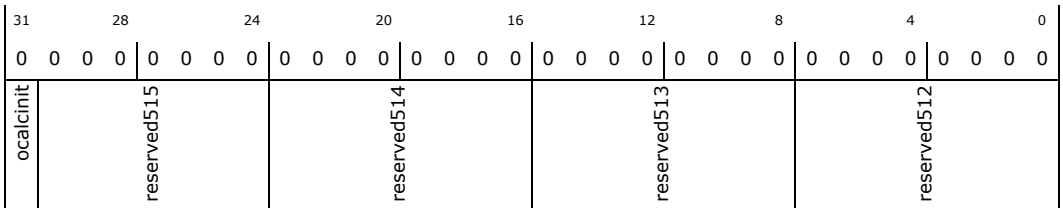
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA6] + (480h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

18.10.7 TX_DWORD6 (tx_dword6)—Offset 18h

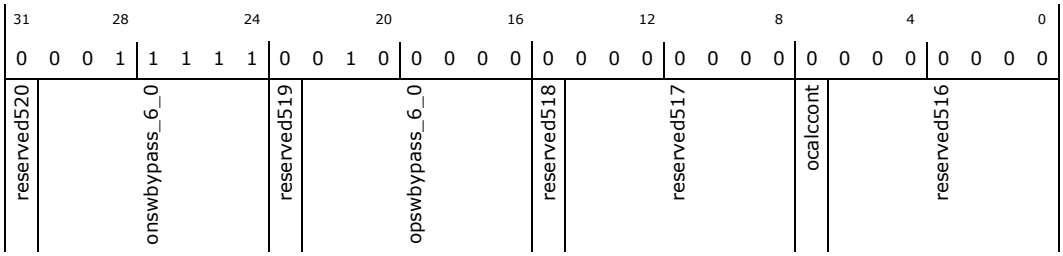
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword6: [Port: 0xA6] + (480h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h



Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved

Bit Range	Default & Access	Description
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively
6:0	0h RO	**reserved516:** reserved

18.10.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

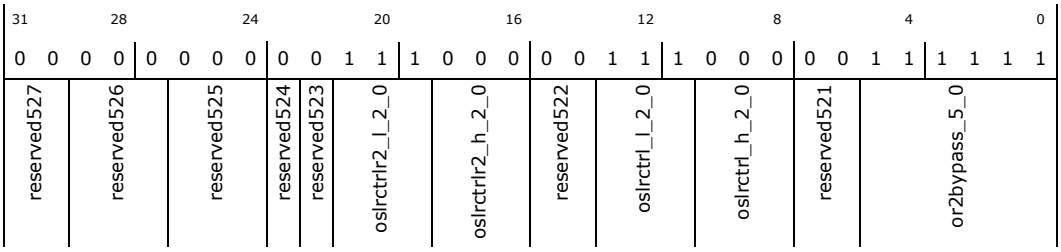
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword7: [Port: 0xA6] + (480h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh



Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved

Bit Range	Default & Access	Description
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

18.10.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

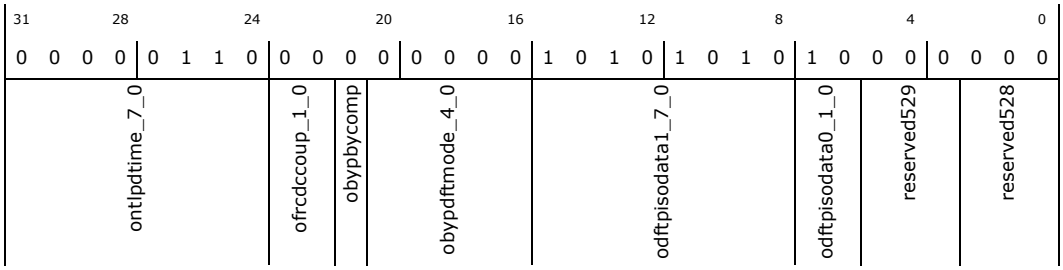
Type: Message Bus Register (Size: 32 bits)

tx_dword8: [Port: 0xA6] + (480h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 0600AA80h



Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG

Bit Range	Default & Access	Description
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

18.10.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

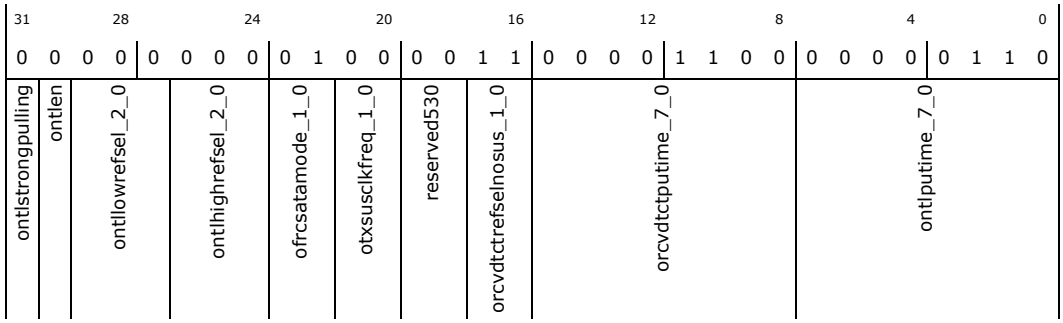
Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA6] + (480h + 24h)

Op Codes:

0h - Read, 1h - Write

Default: 00430C06h



Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active

Bit Range	Default & Access	Description
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

18.10.11 TX_DWORD10 (tx_dword10)—Offset 28h

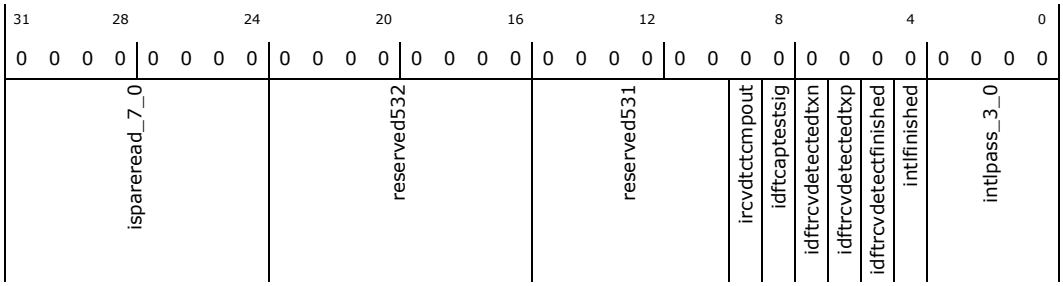
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword10: [Port: 0xA6] + (480h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

18.10.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

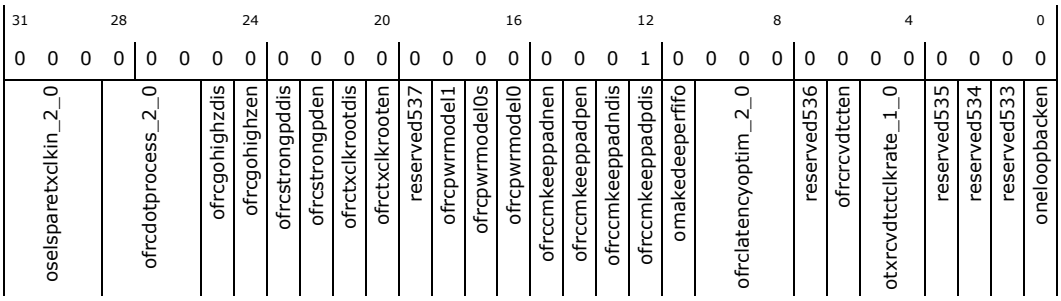
Type: Message Bus Register (Size: 32 bits)

tx_dword11: [Port: 0xA6] + (480h + 2Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00001000h



Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN

Bit Range	Default & Access	Description
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

18.10.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

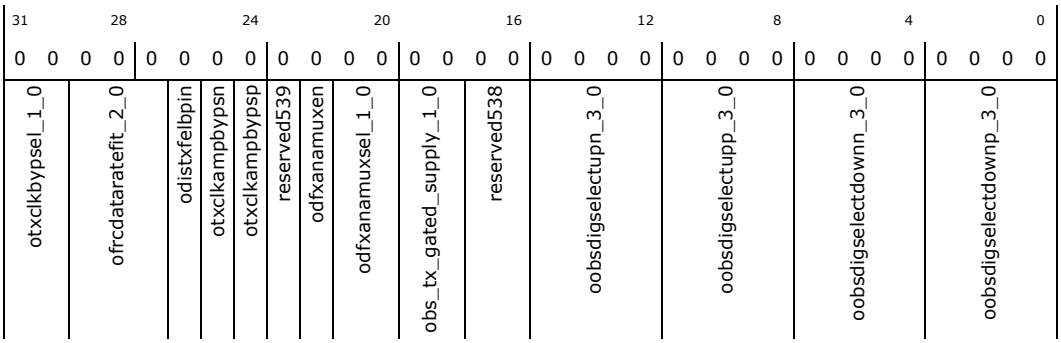
Type: Message Bus Register (Size: 32 bits)

tx_dword12: [Port: 0xA6] + (480h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - datarate fit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - datarate fit must be '11'
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]

Bit Range	Default & Access	Description
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

18.10.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

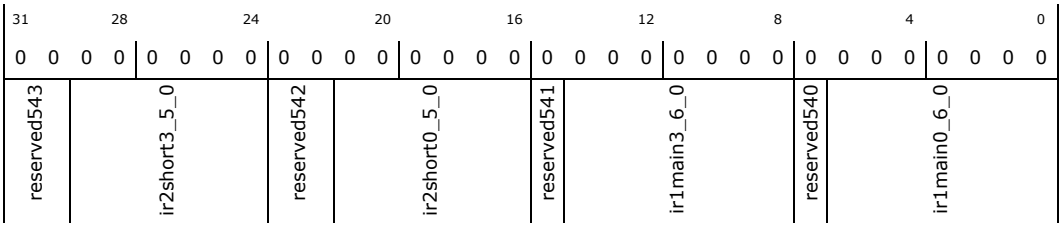
Type: Message Bus Register (Size: 32 bits)

tx_dword13: [Port: 0xA6] + (480h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

18.10.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

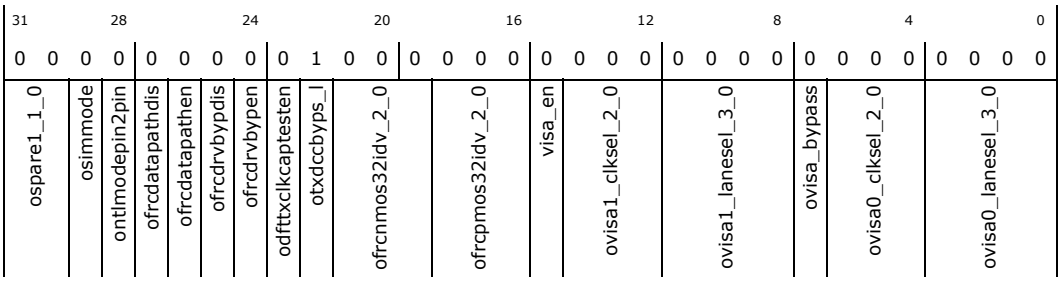
Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA6] + (480h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 00400000h



Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.

Bit Range	Default & Access	Description
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

18.10.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

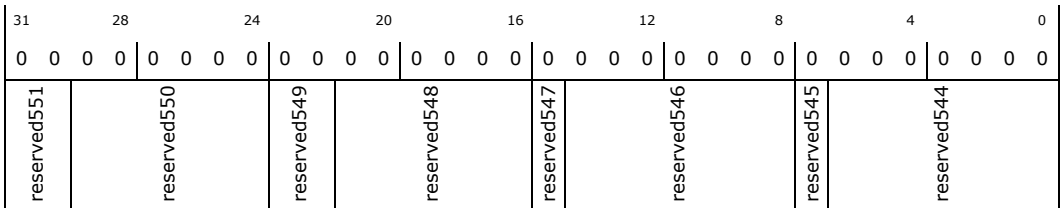
Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA6] + (480h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

18.10.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

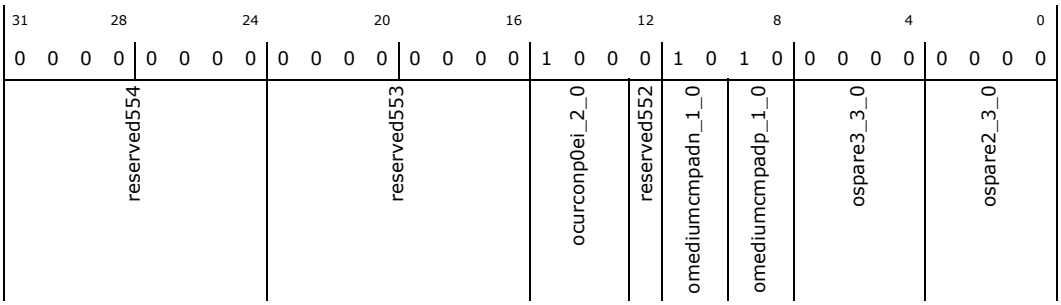
Type: Message Bus Register (Size: 32 bits)

tx_dword16: [Port: 0xA6] + (480h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 00008A00h



Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

18.11 PCI Express* Lane 2 Electrical Address Map

Table 138. Summary of PCI Express* Lane 2 Electrical Message Bus Registers—0xA6 (Global Offset 600h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 871	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 873	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 874	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 875	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 876	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 877	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 878	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 879	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 880	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 881	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 883	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 884	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 886	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 887	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 888	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 889	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 891	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 892	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 894	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 895	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 896	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 897	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 898	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 899	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 899	0001C020h

18.11.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

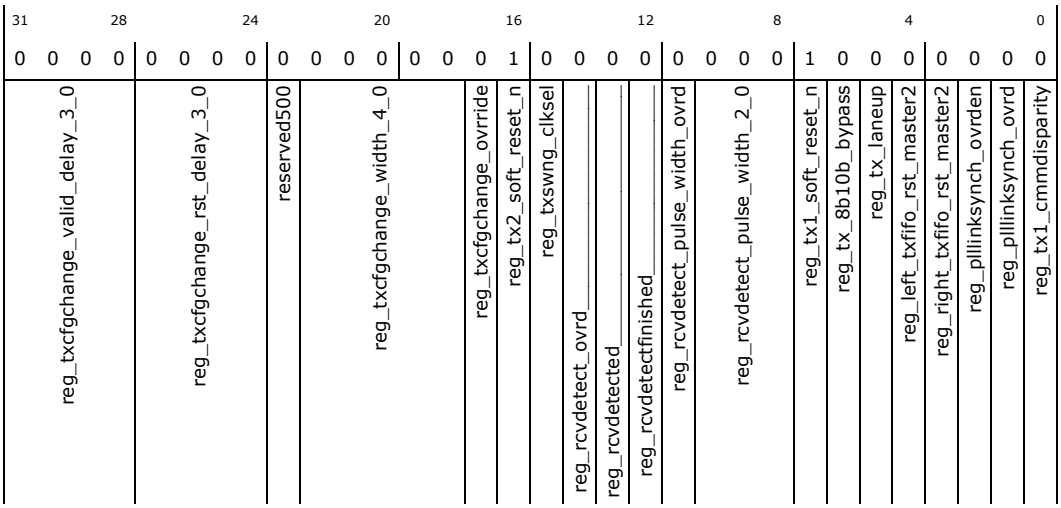
Type: Message Bus Register (Size: 32 bits)

pcs_dword0: [Port: 0xA6] + (600h + 0h)

Op Codes:

0h - Read, 1h - Write

Default: 00010080h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd_____:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected_____:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished_____:** override for rcvdetectfinished

Bit Range	Default & Access	Description
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

18.11.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

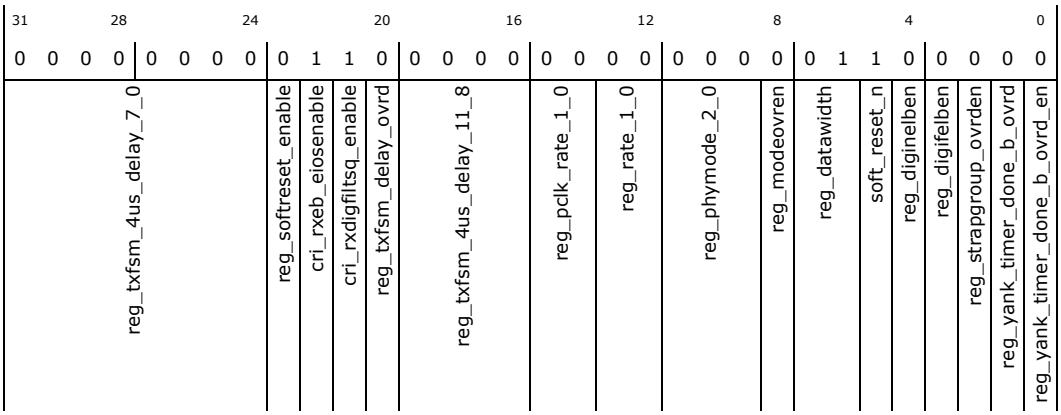
Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA6] + (600h + 4h)

Op Codes:

0h - Read, 1h - Write

Default: 00600060h



Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width

Bit Range	Default & Access	Description
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

18.11.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

Access Method

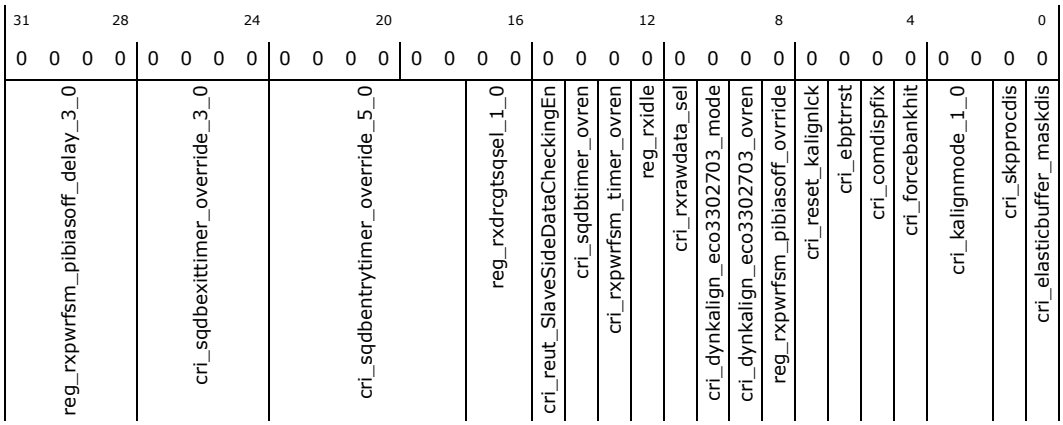
Type: Message Bus Register (Size: 32 bits)

pcs_dword2: [Port: 0xA6] + (600h + 8h)

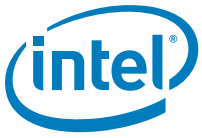
Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select



Bit Range	Default & Access	Description
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

18.11.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

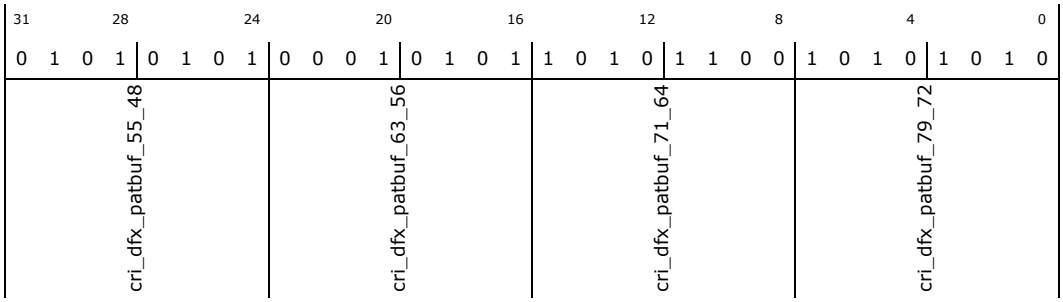
Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA6] + (600h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 5515ACAAh



Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.11.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

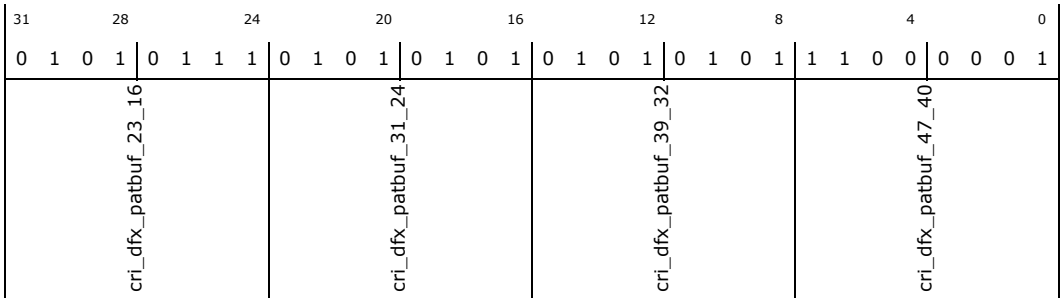
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword4: [Port: 0xA6] + (600h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 575555C1h



Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.11.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

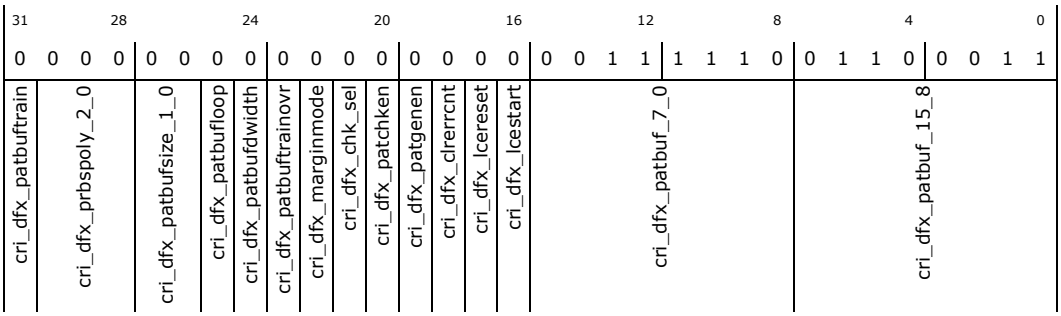
Type: Message Bus Register (Size: 32 bits)

pcs_dword5: [Port: 0xA6] + (600h + 14h)

Op Codes:

0h - Read, 1h - Write

Default: 00003E63h



Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker

Bit Range	Default & Access	Description
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.11.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

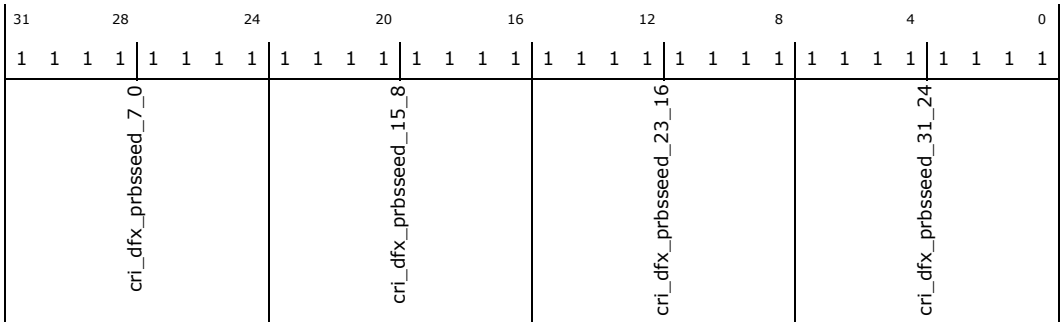
Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA6] + (600h + 18h)

Op Codes:

0h - Read, 1h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

18.11.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

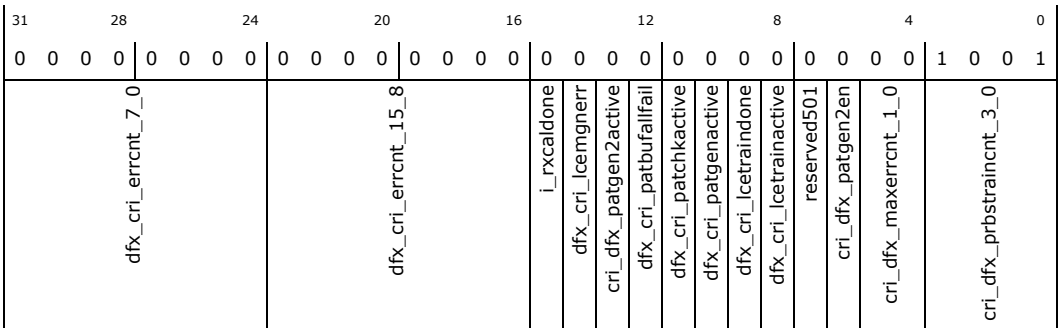
Type: Message Bus Register (Size: 32 bits)

pcs_dword7: [Port: 0xA6] + (600h + 1Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000009h



Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator

Bit Range	Default & Access	Description
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

18.11.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

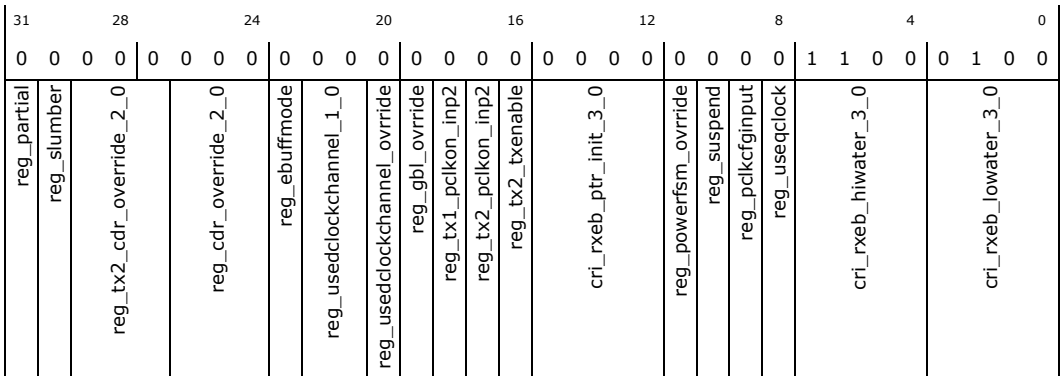
Type: Message Bus Register (Size: 32 bits)

pcs_dword8: [Port: 0xA6] + (600h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 000000C4h



Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1

Bit Range	Default & Access	Description
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

18.11.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

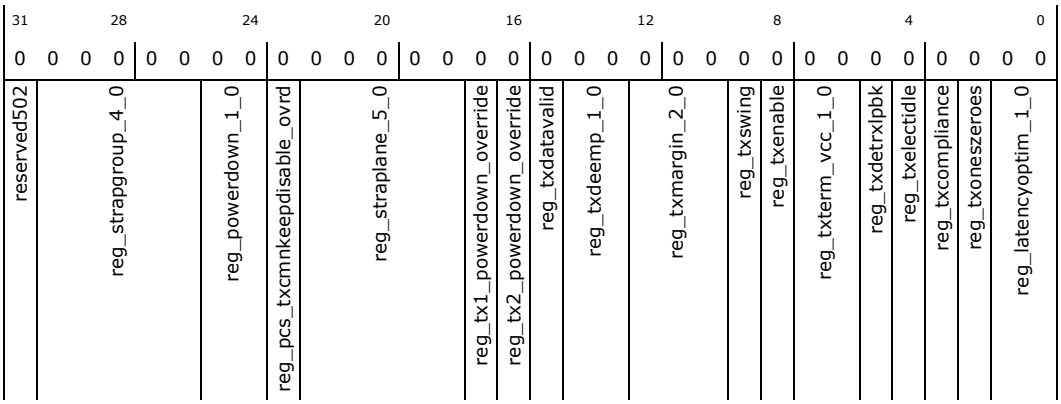
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword9: [Port: 0xA6] + (600h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup

Bit Range	Default & Access	Description
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

18.11.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

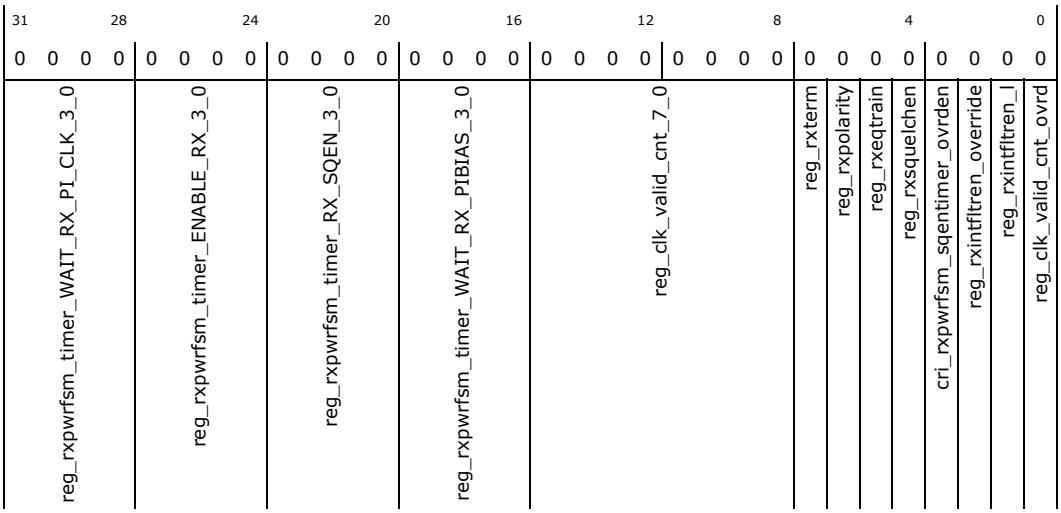
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword10: [Port: 0xA6] + (600h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).

Bit Range	Default & Access	Description
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

18.11.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

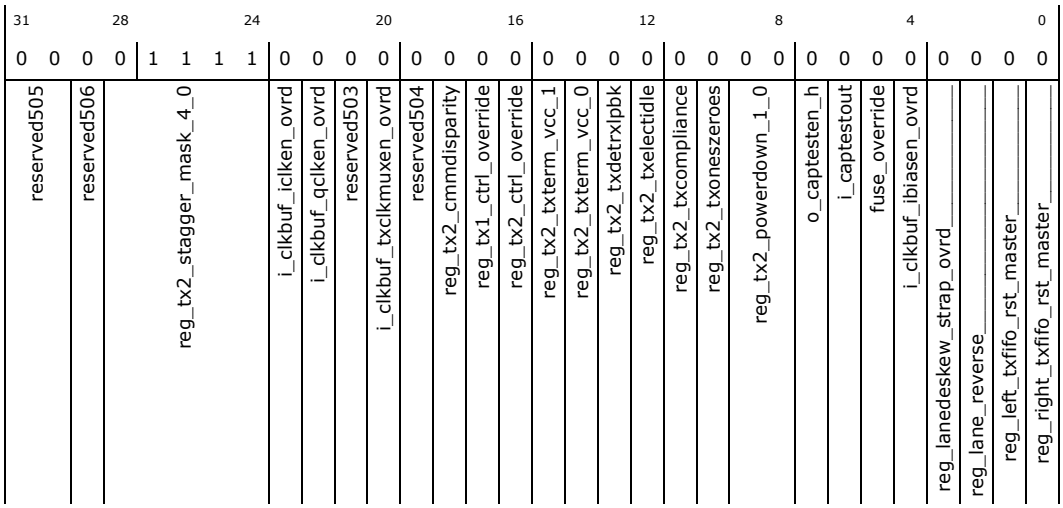
Type: Message Bus Register (Size: 32 bits)

pcs_dword11: [Port: 0xA6] + (600h + 2Ch)

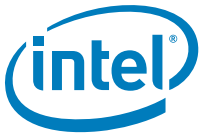
Op Codes:

0h - Read, 1h - Write

Default: 0F000000h



Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved



Bit Range	Default & Access	Description
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd_____:** reserved
2	0h RW	**reg_lane_reverse_____:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____:** reserved
0	0h RW	**reg_right_txfifo_rst_master_____:** reserved

18.11.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

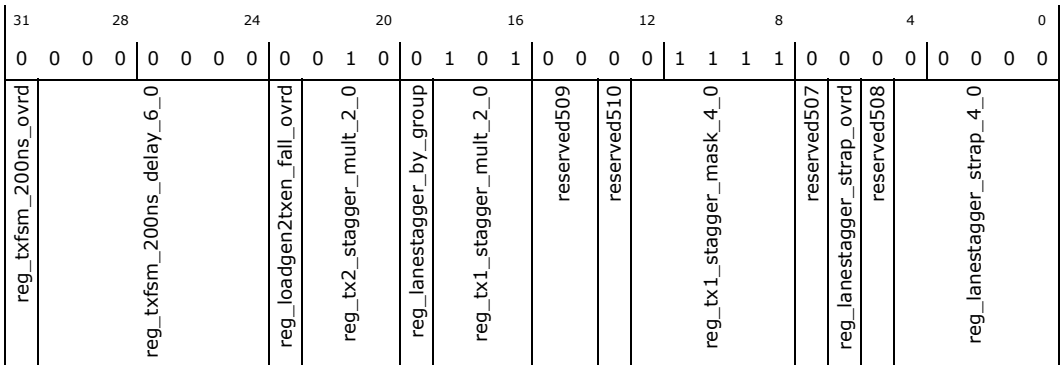
Type: Message Bus Register (Size: 32 bits)

pcs_dword12: [Port: 0xA6] + (600h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00250F00h



Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved

Bit Range	Default & Access	Description
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

18.11.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

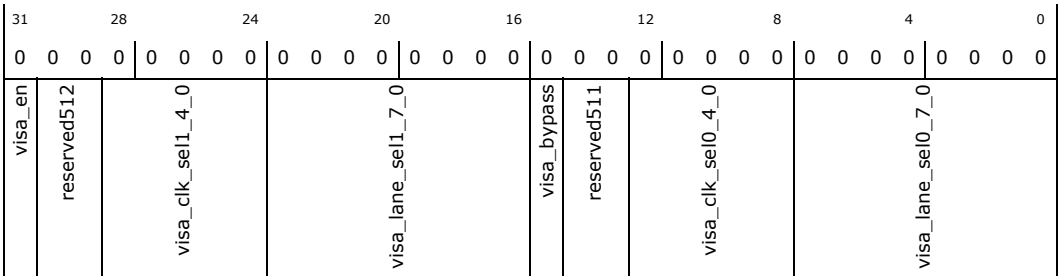
Type: Message Bus Register (Size: 32 bits)

pcs_dword13: [Port: 0xA6] + (600h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

18.11.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

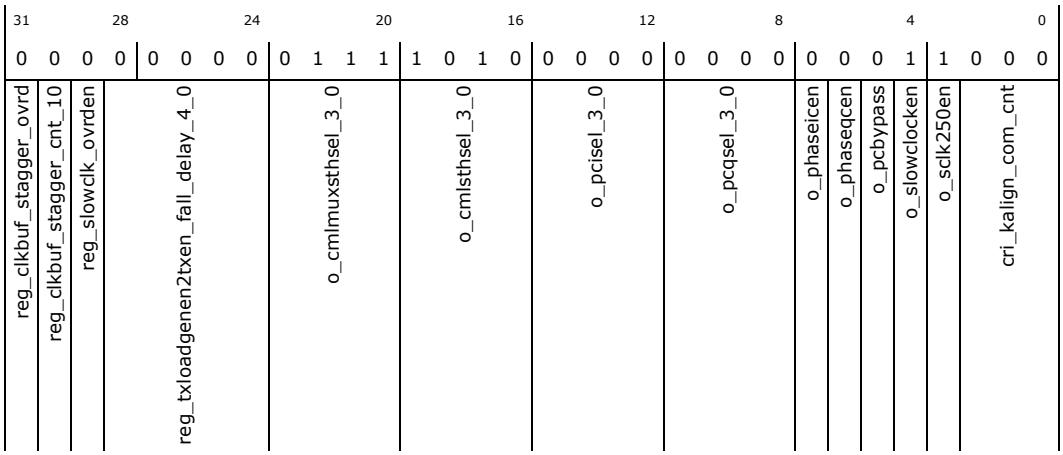
Type: Message Bus Register (Size: 32 bits)

pcs_dword14: [Port: 0xA6] + (600h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 007A0018h



Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.

Bit Range	Default & Access	Description
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

18.11.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

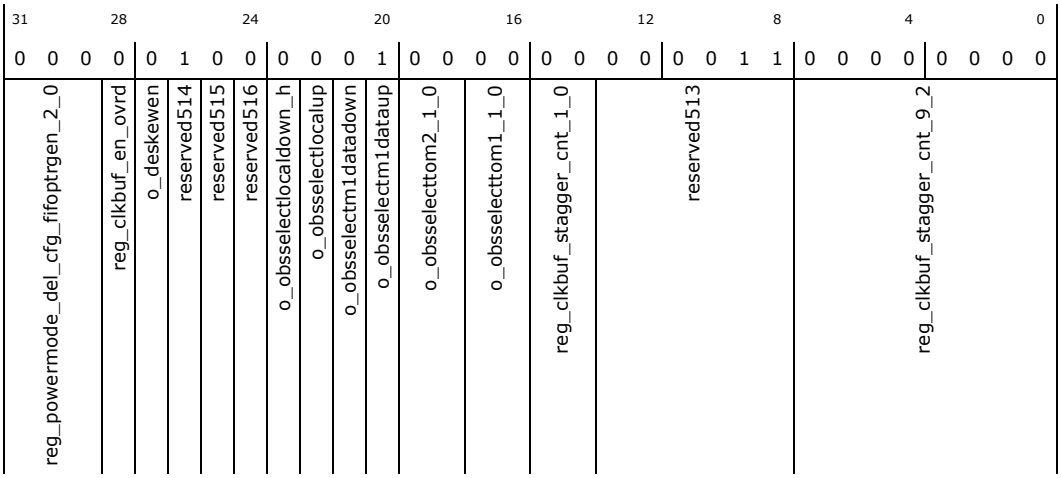
Type: Message Bus Register (Size: 32 bits)

pcs_dword15: [Port: 0xA6] + (600h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 04100300h



Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved

Bit Range	Default & Access	Description
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

18.11.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

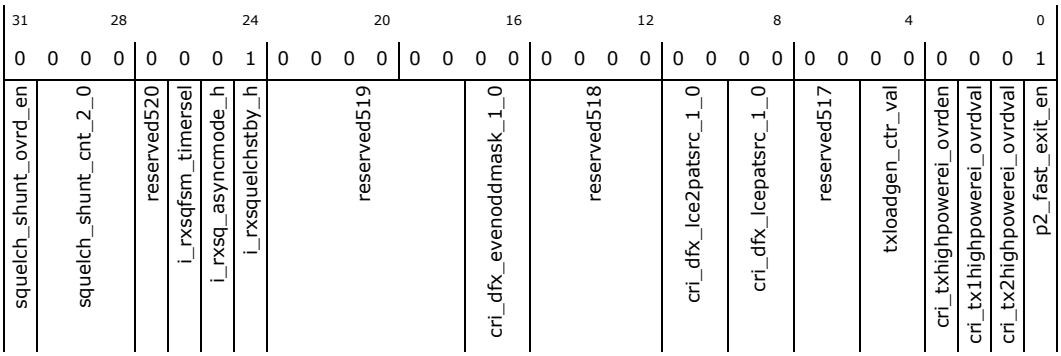
Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA6] + (600h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved

Bit Range	Default & Access	Description
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

18.11.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

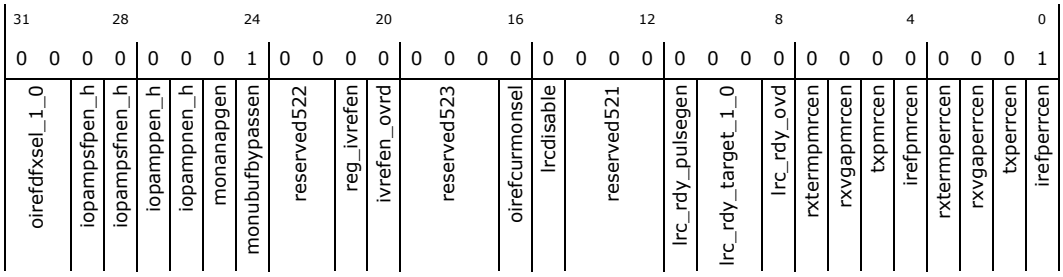
Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA6] + (600h + 44h)

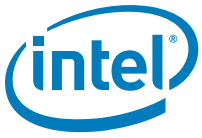
Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)



Bit Range	Default & Access	Description
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

Bit Range	Default & Access	Description
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

18.11.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

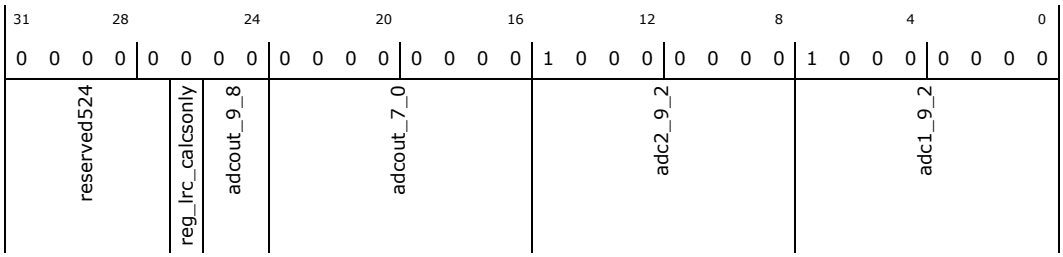
Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA6] + (600h + 48h)

Op Codes:

0h - Read, 1h - Write

Default: 00008080h



Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimation filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimation filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

18.11.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

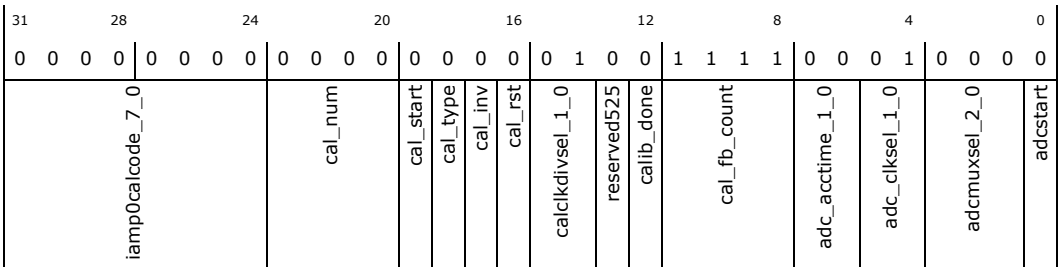
Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA6] + (600h + 4Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00004F10h



Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [Iyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.

Bit Range	Default & Access	Description
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

18.11.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

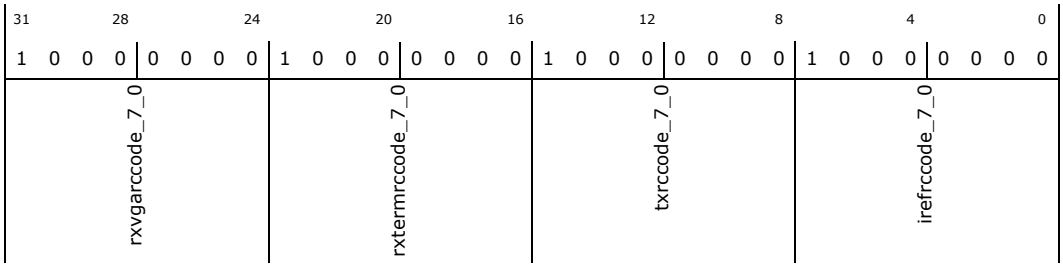
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA6] + (600h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

18.11.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

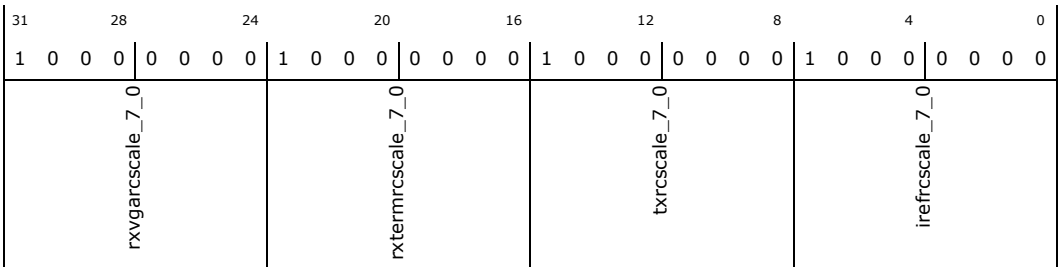
Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA6] + (600h + 54h)

Op Codes:

0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

18.11.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

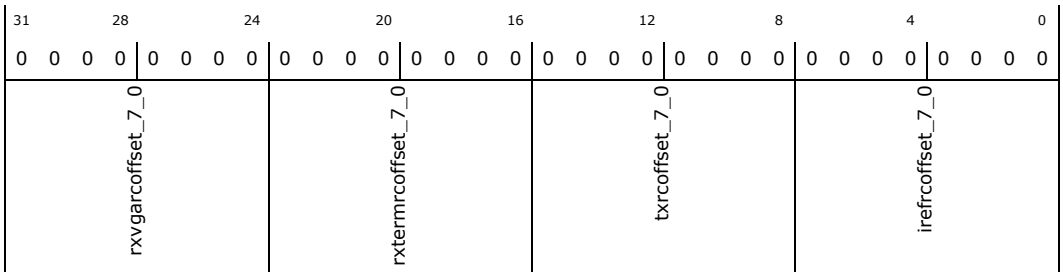
Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA6] + (600h + 58h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

18.11.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

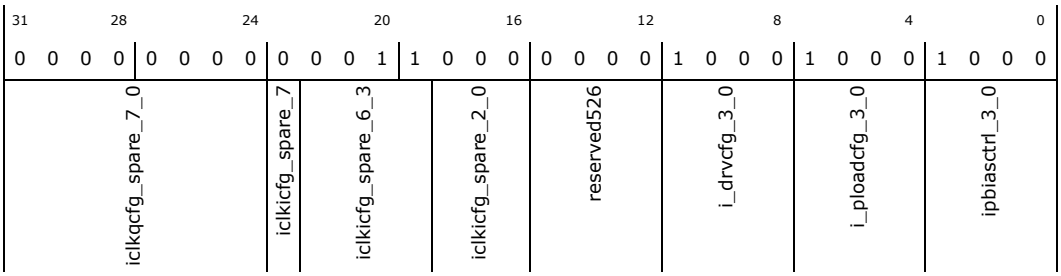
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA6] + (600h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h



Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

18.11.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

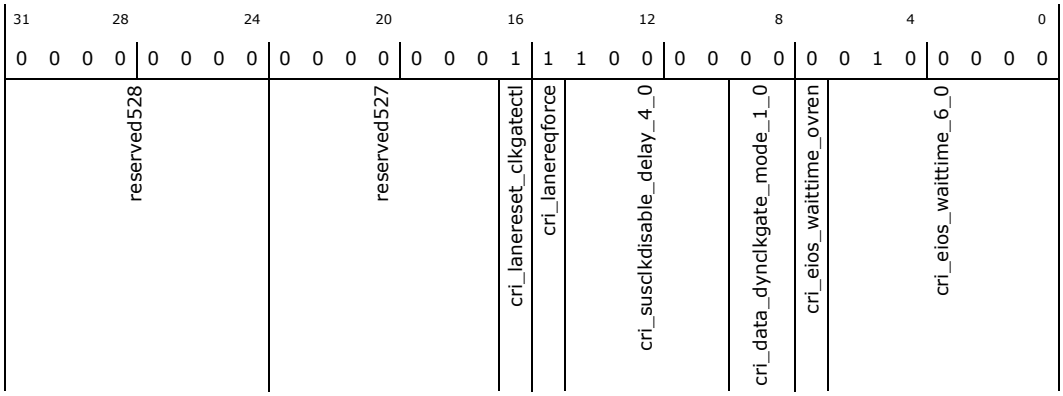
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword24: [Port: 0xA6] + (600h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h



Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (that is, 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay ..... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

18.12 PCI Express* Lane 2 Electrical Address Map

Table 139. Summary of PCI Express* Lane 2 Electrical Message Bus Registers—0xA6 (Global Offset 680h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 901	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 902	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 903	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 904	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 905	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 906	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 906	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 907	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 908	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 909	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 910	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 911	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 913	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 914	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 915	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 916	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 917	00008A00h

18.12.1 TX_DWORD0 (tx_dword0)—Offset 0h

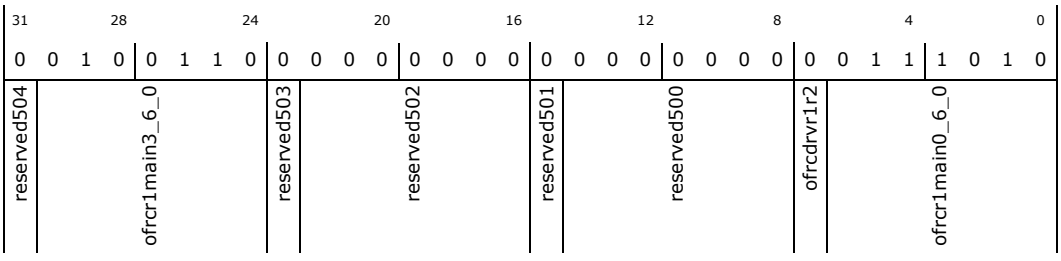
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword0: [Port: 0xA6] + (680h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah



Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

18.12.2 TX_DWORD1 (tx_dword1)—Offset 4h

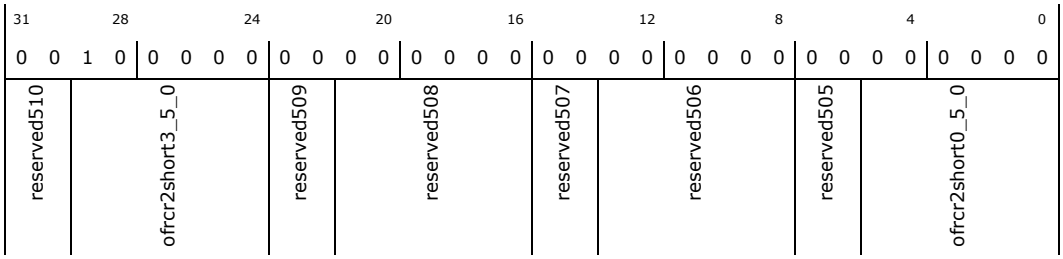
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword1: [Port: 0xA6] + (680h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

18.12.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

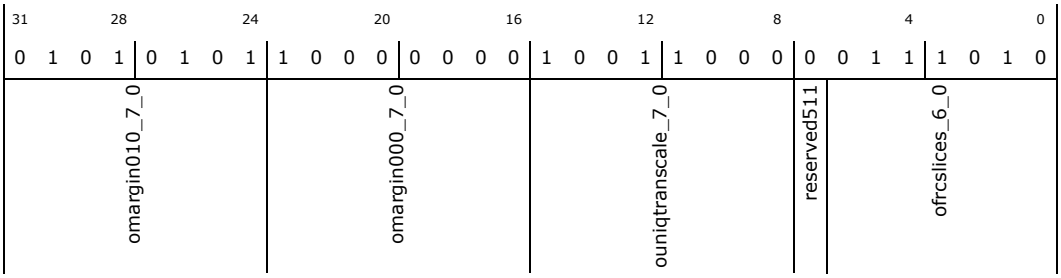
Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA6] + (680h + 8h)

Op Codes:

0h - Read, 1h - Write

Default: 5580983Ah



Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on datarateﬁt and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

18.12.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

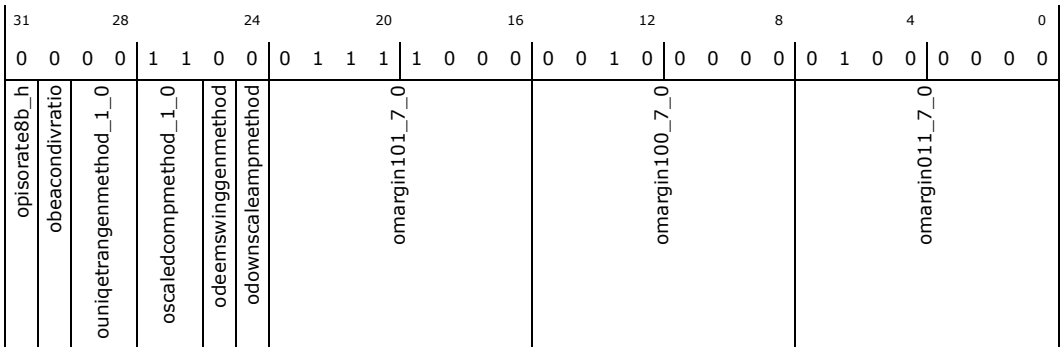
Type: Message Bus Register (Size: 32 bits)

tx_dword3: [Port: 0xA6] + (680h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0C782040h



Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p

Bit Range	Default & Access	Description
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

18.12.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

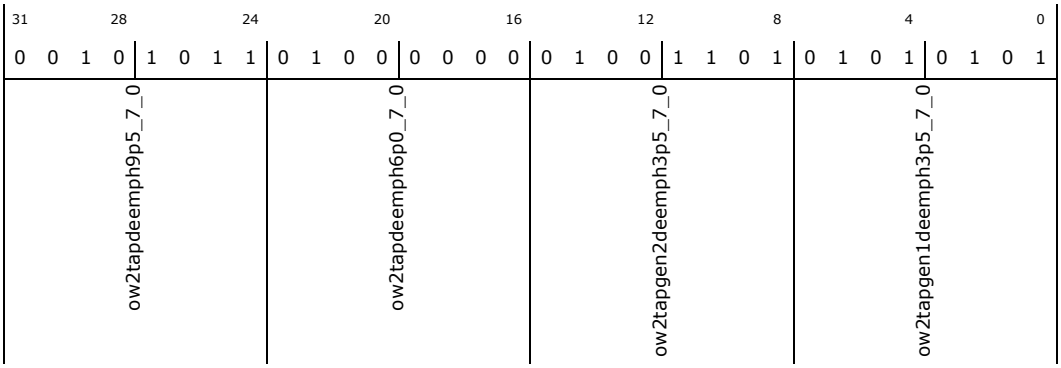
Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA6] + (680h + 10h)

Op Codes:

0h - Read, 1h - Write

Default: 2B404D55h



Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

18.12.6 TX_DWORD5 (tx_dword5)—Offset 14h

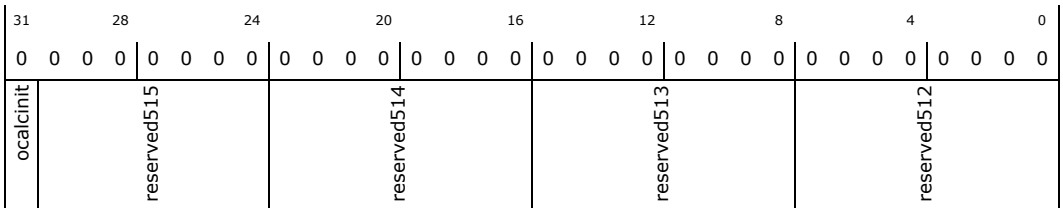
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA6] + (680h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

18.12.7 TX_DWORD6 (tx_dword6)—Offset 18h

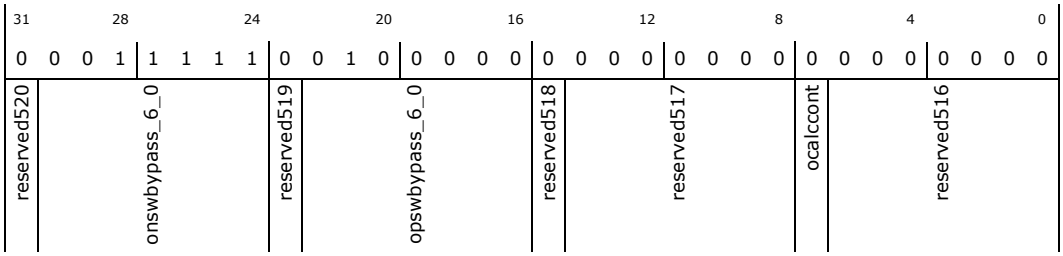
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword6: [Port: 0xA6] + (680h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h



Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved

Bit Range	Default & Access	Description
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively
6:0	0h RO	**reserved516:** reserved

18.12.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

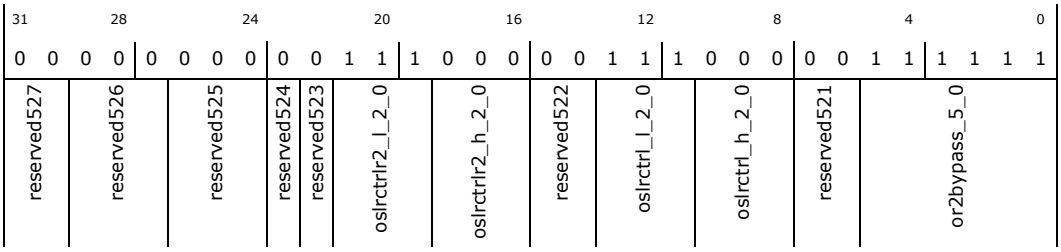
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword7: [Port: 0xA6] + (680h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh



Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved

Bit Range	Default & Access	Description
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

18.12.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

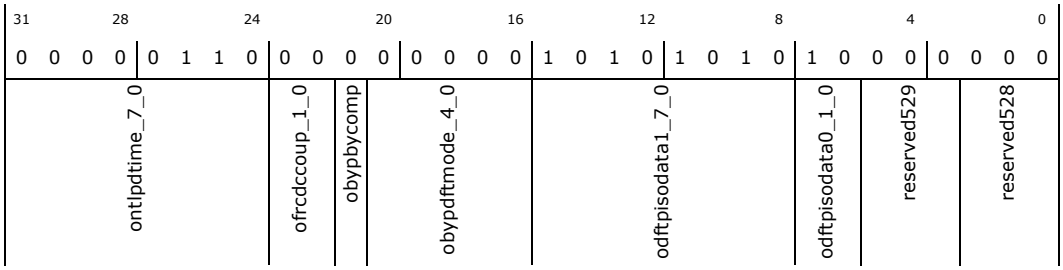
Type: Message Bus Register (Size: 32 bits)

tx_dword8: [Port: 0xA6] + (680h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 0600AA80h



Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG

Bit Range	Default & Access	Description
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

18.12.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

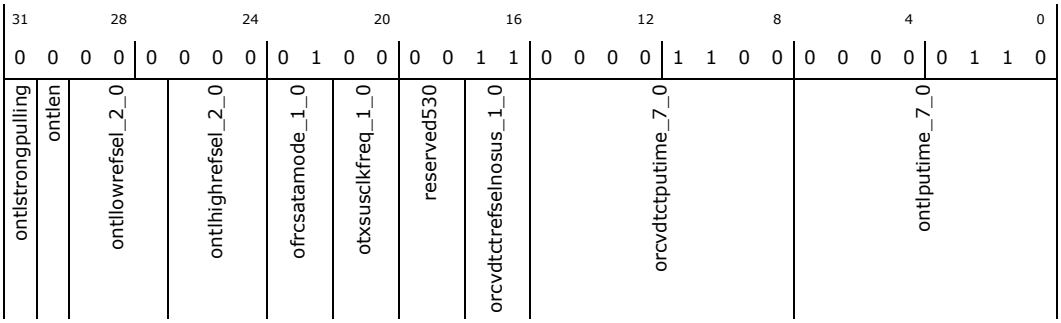
Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA6] + (680h + 24h)

Op Codes:

0h - Read, 1h - Write

Default: 00430C06h



Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active

Bit Range	Default & Access	Description
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

18.12.11 TX_DWORD10 (tx_dword10)—Offset 28h

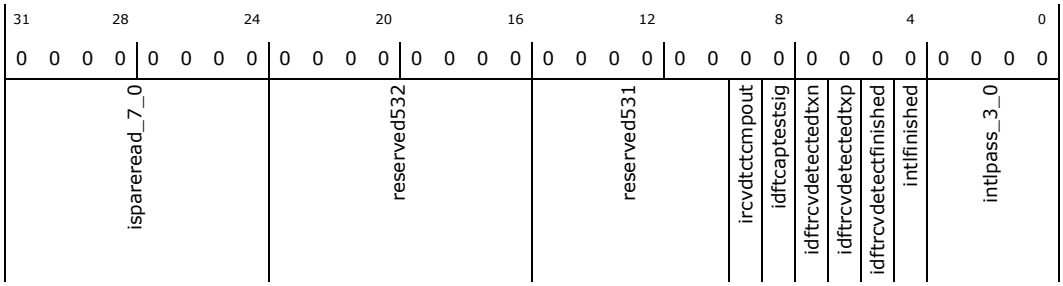
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword10: [Port: 0xA6] + (680h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

18.12.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

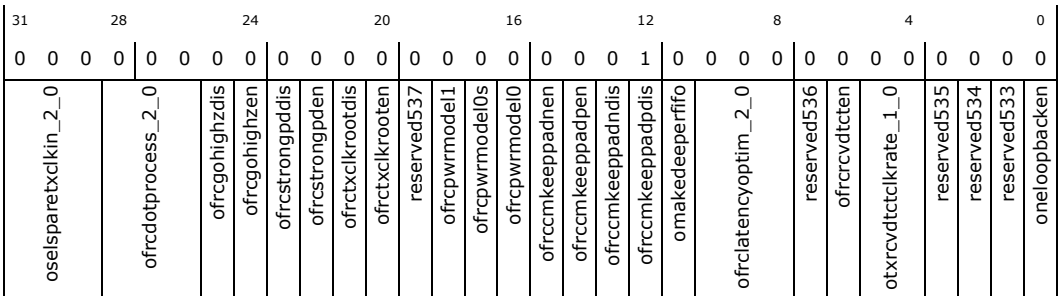
Type: Message Bus Register (Size: 32 bits)

tx_dword11: [Port: 0xA6] + (680h + 2Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00001000h



Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN

Bit Range	Default & Access	Description
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

18.12.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

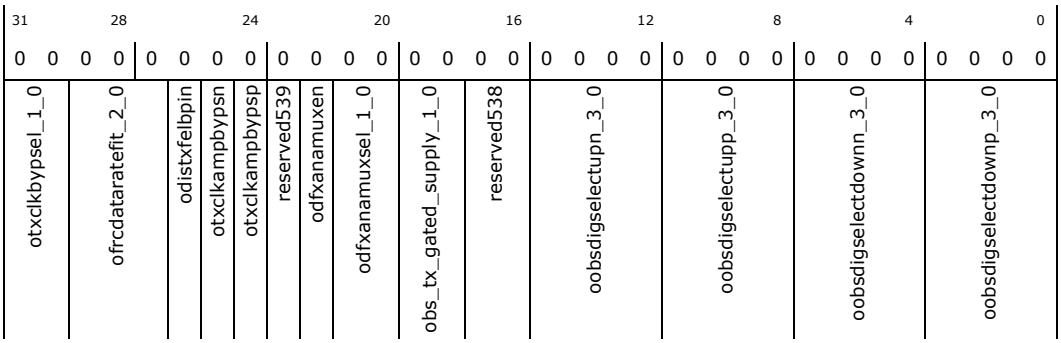
Type: Message Bus Register (Size: 32 bits)

tx_dword12: [Port: 0xA6] + (680h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - datarateﬁt must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - datarateﬁt must be '11'
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]

Bit Range	Default & Access	Description
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

18.12.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

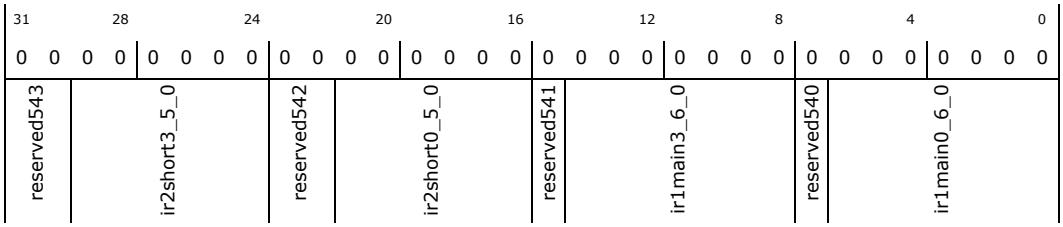
Type: Message Bus Register (Size: 32 bits)

tx_dword13: [Port: 0xA6] + (680h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

18.12.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

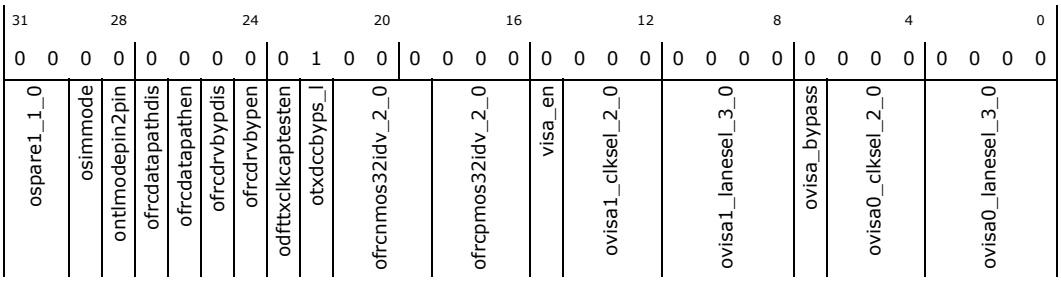
Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA6] + (680h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 00400000h



Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.

Bit Range	Default & Access	Description
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

18.12.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

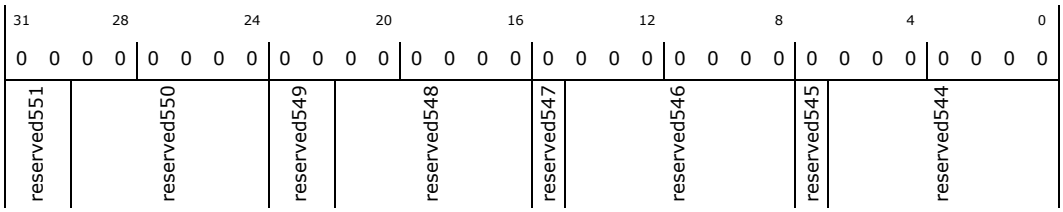
Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA6] + (680h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

18.12.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

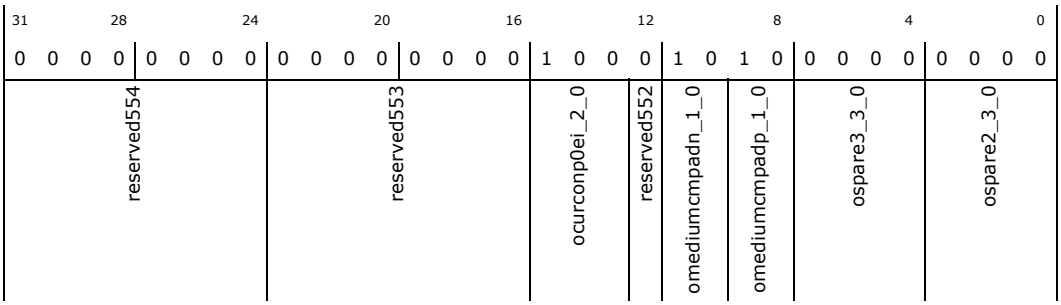
Type: Message Bus Register (Size: 32 bits)

tx_dword16: [Port: 0xA6] + (680h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 00008A00h



Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

18.13 PCI Express* Lane 3 Electrical Address Map

Table 140. Summary of PCI Express* Lane 3 Electrical Message Bus Registers—0xA6 (Global Offset 800h)

Offset	Register ID—Description	Default Value
0h	"PCS_DWORD0 (pcs_dword0)—Offset 0h" on page 919	00010080h
4h	"PCS_DWORD1 (pcs_dword1)—Offset 4h" on page 921	00600060h
8h	"PCS_DWORD2 (pcs_dword2)—Offset 8h" on page 922	00000000h
Ch	"PCS_DWORD3 (pcs_dword3)—Offset Ch" on page 923	5515ACAAh
10h	"PCS_DWORD4 (pcs_dword4)—Offset 10h" on page 924	575555C1h
14h	"PCS_DWORD5 (pcs_dword5)—Offset 14h" on page 925	00003E63h
18h	"PCS_DWORD6 (pcs_dword6)—Offset 18h" on page 926	FFFFFFFFh
1Ch	"PCS_DWORD7 (pcs_dword7)—Offset 1Ch" on page 927	00000009h
20h	"PCS_DWORD8 (pcs_dword8)—Offset 20h" on page 928	000000C4h
24h	"PCS_DWORD9 (pcs_dword9)—Offset 24h" on page 929	00000000h
28h	"PCS_DWORD10 (pcs_dword10)—Offset 28h" on page 931	00000000h
2Ch	"PCS_DWORD11 (pcs_dword11)—Offset 2Ch" on page 932	0F000000h
30h	"PCS_DWORD12 (pcs_dword12)—Offset 30h" on page 934	00250F00h
34h	"PCS_DWORD13 (pcs_dword13)—Offset 34h" on page 935	00000000h
38h	"PCS_DWORD14 (pcs_dword14)—Offset 38h" on page 936	007A0018h
3Ch	"PCS_DWORD15 (pcs_dword15)—Offset 3Ch" on page 937	04100300h
40h	"PCS_DWORD16 (pcs_dword16)—Offset 40h" on page 939	01000001h
44h	"PCS_DWORD17 (pcs_dword17)—Offset 44h" on page 940	01000001h
48h	"PCS_DWORD18 (pcs_dword18)—Offset 48h" on page 942	00008080h
4Ch	"PCS_DWORD19 (pcs_dword19)—Offset 4Ch" on page 943	00004F10h
50h	"PCS_DWORD20 (pcs_dword20)—Offset 50h" on page 944	80808080h
54h	"PCS_DWORD21 (pcs_dword21)—Offset 54h" on page 945	80808080h
58h	"PCS_DWORD22 (pcs_dword22)—Offset 58h" on page 946	00000000h
5Ch	"PCS_DWORD23 (pcs_dword23)—Offset 5Ch" on page 947	00180888h
60h	"PCS_DWORD24 (pcs_dword24)—Offset 60h" on page 947	0001C020h

18.13.1 PCS_DWORD0 (pcs_dword0)—Offset 0h

Access Method

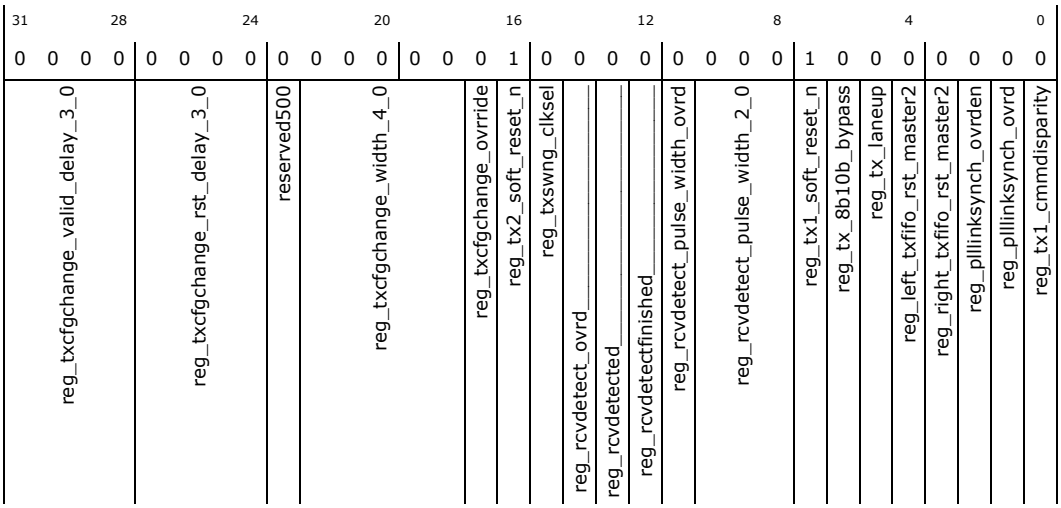
Type: Message Bus Register (Size: 32 bits)

pcs_dword0: [Port: 0xA6] + (800h + 0h)

Op Codes:

0h - Read, 1h - Write

Default: 00010080h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_txcfgchange_valid_delay_3_0:** Controls counter to wait 128ns after txcfgchange asserts when coming out of reset. This will control phystatus de-assertion after reset. Note: Minimum value when programmed has to be 4'b0100 or greater.
27:24	0h RW	**reg_txcfgchange_rst_delay_3_0:** Counter value to delay txcfgchange toggle after coming out of reset.
23	0h RW	**reserved500:** reserved
22:18	0h RW	**reg_txcfgchange_width_4_0:** Tx power fsm output - divider ratio
17	0h RW	**reg_txcfgchange_ovrride:** Override txchfchange related counters. (reg_txcfgchange_width, reg_txcfgchange_valid_delay, reg_txcfgchange_rst_delay)
16	1h RW	**reg_tx2_soft_reset_n:** Active low reset to independently reset Tx lane2 in Display Port
15	0h RW	**reg_txswng_clksel:** When 0 selects divide by 2 version of the ick_plllink clock for Tx swing control logic When 1 selects ick_plllink clock for Tx swing control logic.
14	0h RW	**reg_rcvdetect_ovrd_____:** override enable for rcvdetected and rcvdetectfinished
13	0h RW	**reg_rcvdetected_____:** override for rcvdetected
12	0h RW	**reg_rcvdetectfinished_____:** override for rcvdetectfinished

Bit Range	Default & Access	Description
11	0h RW	**reg_rcvdetect_pulse_width_ovrd:** override enable for rcvdetect_pulse_width
10:8	0h RW	**reg_rcvdetect_pulse_width_2_0:** override value for rcvdetect_pusle_width
7	1h RW	**reg_tx1_soft_reset_n:** Active low reset to independently reset Tx lane1 in Display Port 0: Lane 1 reset 1: Lane 1 active
6	0h RW	**reg_tx_8b10b_bypass:** Bypass 8b10b encoder (for SAPIS etc interface.) 0 = Disable 8b/10b encoder bypass 1 = Enable 8b/10b encoder bypass
5	0h RW	**reg_tx_laneup:** Unused in Tx
4	0h RW	**reg_left_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
3	0h RW	**reg_right_txfifo_rst_master2:** override enable = reg_lanedeskew_strap_ovrd
2	0h RW	**reg_plllinksynch_ovrden:** Override enable for reg_plllinsync_ovrd 0 = Use default delay in hardware 1 = Use reg_plllinksynch_ovrd
1	0h RW	**reg_plllinksynch_ovrd:** override value for plllinksynch
0	0h RW	**reg_tx1_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. 0 = set negative disparity 1 = set positive disparity

18.13.2 PCS_DWORD1 (pcs_dword1)—Offset 4h

Access Method

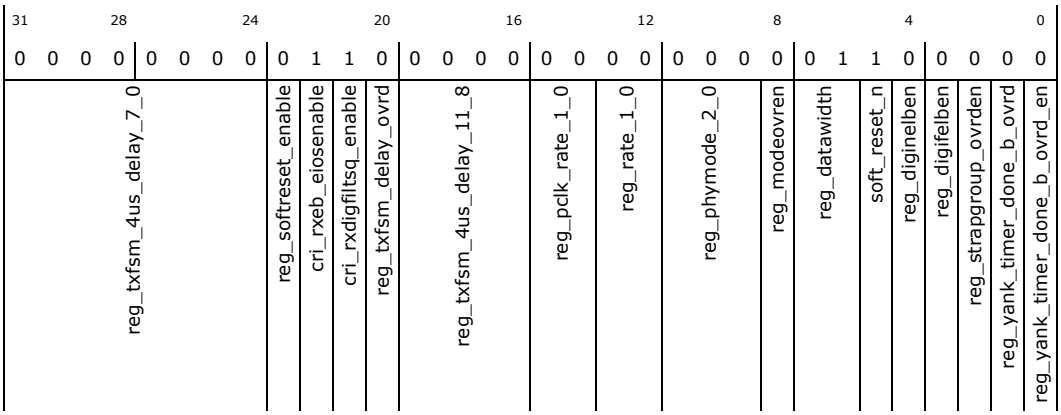
Type: Message Bus Register (Size: 32 bits)

pcs_dword1: [Port: 0xA6] + (800h + 4h)

Op Codes:

0h - Read, 1h - Write

Default: 00600060h



Bit Range	Default & Access	Description
31:24	0h RW	**reg_txfsm_4us_delay_7_0:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
23	0h RW	**reg_softreset_enable:** When '1' the soft_reset_n bit will contol the lane reset When '0' the hardware reset will control the lane reset Note for DP: In addition to soft_reset_n,which will reset both TX0 and TX 1 in the lane, the reg_tx1_soft_reset_n bit can be used to reset only TX1 in the lane and reg_tx2_soft_reset_n bit can be used to reset only TX2
22	1h RW	**cri_rxeb_eiosenable:** When 1 enables EIOS based Rx power down
21	1h RW	**cri_rxdigfiltsq_enable:** When 1 enables unsquelch based Rx power up in P0 or P0s
20	0h RW	**reg_txfsm_delay_ovrd:** Override enable bit for reg_txfsm_4us_delay
19:16	0h RW	**reg_txfsm_4us_delay_11_8:** Override counter value for 4 us delay in txfsm lane reset to txbiasen delay
15:14	0h RW	**reg_pclk_rate_1_0:** Override for pclk_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
13:12	0h RW	**reg_rate_1_0:** Override for i_rate 00 = gen1 01 = gen2 10 = gen3 11 = GbE
11:9	0h RW	**reg_phymode_2_0:** Override for PHY Mode Selection 000 = PCIE 001 = USB3 010 = GbE 011 = SATA/SAPIS 100 = Display 101 = DMI 110 = CIO 111 =Reserved
8	0h RW	**reg_modeovren:** When asserted selects register override bits for phymode, datawidth etc
7:6	1h RW	**reg_datawidth:** Override for Tx data interface width. 00 - Unused 01 - x8/x10 width (default) 10 - x16/x20 width 11 - x32/x40 width

Bit Range	Default & Access	Description
5	1h RW	**soft_reset_n:** Active low soft reset override
4	0h RW	**reg_diginelben:** Override for near end digital loopback.
3	0h RW	**reg_digifelben:** Override for far end digital loopback
2	0h RW	**reg_strapgroup_ovrden:** Override Enable for Strap Group
1	0h RW	**reg_yank_timer_done_b_ovrd:** Override for yank_timer_done_b
0	0h RW	**reg_yank_timer_done_b_ovrd_en:** Override Enable for yank_timer_done_b

18.13.3 PCS_DWORD2 (pcs_dword2)—Offset 8h

Access Method

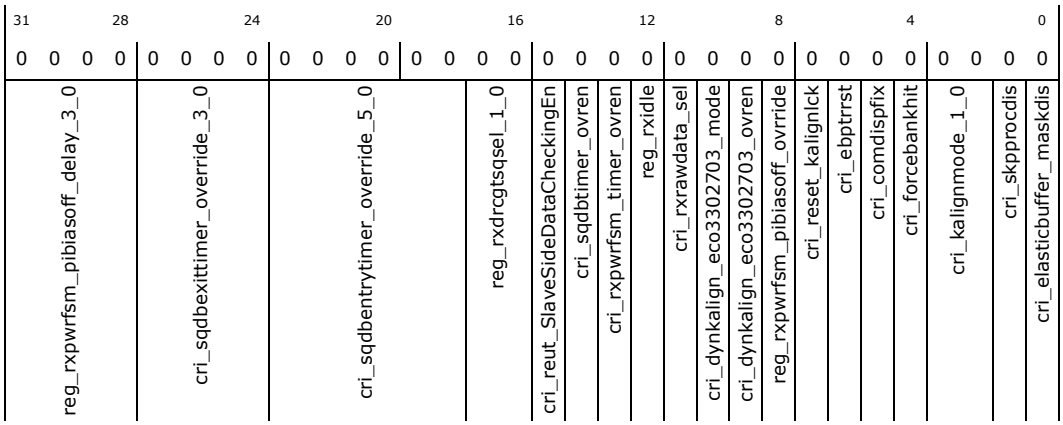
Type: Message Bus Register (Size: 32 bits)

pcs_dword2: [Port: 0xA6] + (800h + 8h)

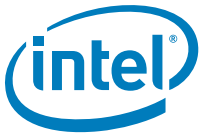
Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_pibiasoff_delay_3_0:** Override value for delay (in 2ns increments) between deassertion of opianclkbufen and opibiasen
27:24	0h RW	**cri_sqdbexittimer_override_3_0:** Rx squelch exit debounce timer
23:18	0h RW	**cri_sqdbentrytimer_override_5_0:** Rx squelch entry debounce timer
17:16	0h RW	**reg_rxdrcgtsqsel_1_0:** Squelch output select



Bit Range	Default & Access	Description
15	0h RW	**cri_reut_SlaveSideDataCheckingEn:** Enable REUT slave side checking while in loopback slave
14	0h RW	**cri_sqdbtimer_ovren:** Squelch debounce timer override enable
13	0h RW	**cri_rxpwrfsm_timer_ovren:** Rx power management fsm timer override enable
12	0h RW	**reg_rxidle:** Chicken bit to override i_rxidle from controller and keep Rx in P0 or P0s
11	0h RW	**cri_rxrawdata_sel:** When asserted bypass K-align, 10b/8b decoder and Elastic buffer
10	0h RW	**cri_dynkalign_eco3302703_mode:** Kalign Mode Override Value When cri_dynkalign_eco3302703_ovren is set, this value selects kalignmode 0 - use register bits cri_kalignmode[1:0] to select kalignmode 1 - select the 4 COM kalign mode'
9	0h RW	**cri_dynkalign_eco3302703_ovren:** Kalign Mode Override Enable Overrides kalign mode select pin, allowing config bit kalignmode_override_val to select kalignmode.
8	0h RW	**reg_rxpwrfsm_pibiasoff_ovrride:** When asserted selects reg_rxpwrfsm_pibiasoff_delay[3:0]
7	0h RW	**cri_reset_kalignlck:** When asserted resets Kalign lock indication and Kalign is performed again. The conditions when this would assert includes and is not restricted to any power management states (L0s, L1) or polling quiet states etc.
6	0h RW	**cri_ebptrrst:** Global broadcast to all lanes that the Elastic Buffer pointers should be reset. This is a pulse and will be generated when we need to reset the pointers because of collision or various other reasons.
5	0h RW	**cri_comdispfix:** Chicken bit to force disparity in dynamic K-align mode
4	0h RW	**cri_forcebankhit:** Chicken bit to enable data appear on NOA post k-align lock although k-align block is not achieving lock. This is only for NOA observeability and not for other purpose
3:2	0h RW	**cri_kalignmode_1_0:** KALIGN Mode Select 00 = dynamic kalign all the time. Accounts for bit slips on incoming stream which can cause symbol to be detected on different bank 10 = dynamic kalign up to L0 x1 = static kalign (same as GDG). Assumes symbol always detected on same data bank
1	0h RW	**cri_skpprocdis:** SKIP Ordered-Set Processing Disable When this configuration bit is asserted, then SKIP ordered=sets will be ignored (in EB block). Used in Elastic buffer block. 0 = Normal operation. SKIP ordered=sets will be processed by the Elastic Buffer 1 = SKIP processing disabled.
0	0h RW	**cri_elasticbuffer_maskdis:** Config bit (chicken bit) to disable the masking logic after elec idle ordered set is seen

18.13.4 PCS_DWORD3 (pcs_dword3)—Offset Ch

Access Method

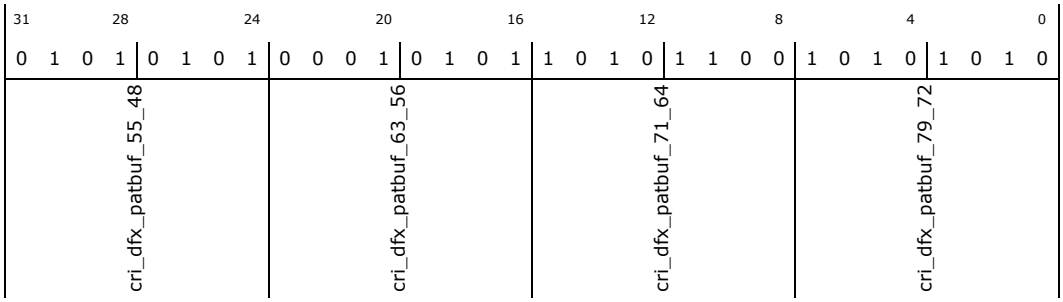
Type: Message Bus Register (Size: 32 bits)

pcs_dword3: [Port: 0xA6] + (800h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 5515ACAAh



Bit Range	Default & Access	Description
31:24	55h RW	**cri_dfx_patbuf_55_48:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	15h RW	**cri_dfx_patbuf_63_56:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	ACh RW	**cri_dfx_patbuf_71_64:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	AAh RW	**cri_dfx_patbuf_79_72:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.13.5 PCS_DWORD4 (pcs_dword4)—Offset 10h

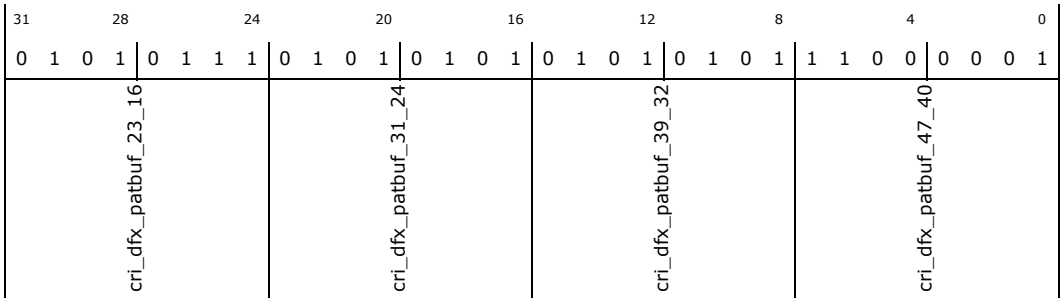
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword4: [Port: 0xA6] + (800h + 10h)

Op Codes:
0h - Read, 1h - Write

Default: 575555C1h



Bit Range	Default & Access	Description
31:24	57h RW	**cri_dfx_patbuf_23_16:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
23:16	55h RW	**cri_dfx_patbuf_31_24:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
15:8	55h RW	**cri_dfx_patbuf_39_32:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.
7:0	C1h RW	**cri_dfx_patbuf_47_40:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.13.6 PCS_DWORD5 (pcs_dword5)—Offset 14h

Access Method

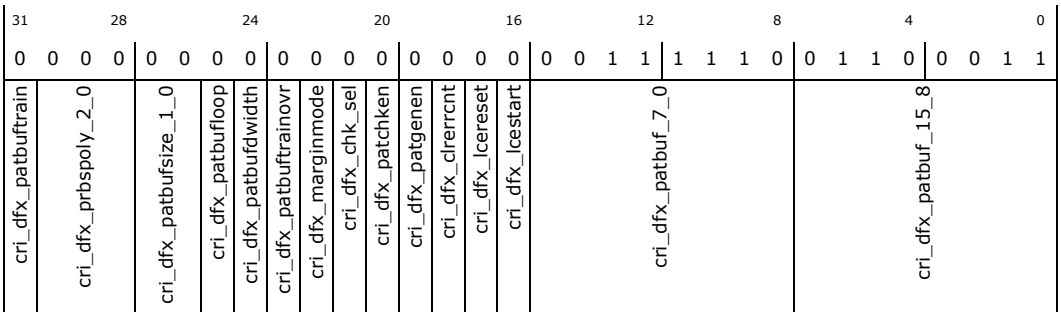
Type: Message Bus Register (Size: 32 bits)

pcs_dword5: [Port: 0xA6] + (800h + 14h)

Op Codes:

0h - Read, 1h - Write

Default: 00003E63h



Bit Range	Default & Access	Description
31	0h RW	**cri_dfx_patbuftrain:** Pattern Buffer Manual Training When DFXPATBUFTRAINOVR and DFXLCESTART are asserted, this manually controls whether the Pattern Buffers are in training or have completed training. 0 : Send training patterns (default) 1 : Send contents of DFXPATBUF
30:28	0h RW	**cri_dfx_prbspoly_2_0:** PRBS Polynomial Select the polynomial to be used by the PRBS in the Pattern Generator and Pattern Checker. PRBS support 10b or 8b, which is indicated by the msb. 000 - x^16 + x^5 + x^4 + x^3 + 1 (USB3/PCIe Scrambler) (8b) 001 - x^16 + x^15 + x^13 + x^4 + 1 (SATA scrambler) (8b) 010 - x^31 + x^28 + 1 (8b) 011 - x^7 + x^6 + 1 (8b) 100 - x^15 + x^14 + 1 (10b) 101 - x^23 + x^18 + 1 (10b) 110 - x^31 + x^28 + 1 (10b) 111 - x^7 + x^6 + 1 (10b)
27:26	0h RW	**cri_dfx_patbufsize_1_0:** Pattern Buffer Size Select the size of the Pattern Buffer to use. The MSB will always be bit 79. The LSB will depend on this select and the DFXLCEDATAWIDTH (10b or 8b mode). 00 : full 80b buffer (Default) 01 : 70b (while in 10b mode), 56b (while in 8b mode) 10 : 40b (while in 10b mode), 32b (while in 8b mode) 11 : 10b (while in 10b mode), 8b (while in 8b mode)
25	0h RW	**cri_dfx_patbufloop:** Pattern Buffer Looping Enable Enables looping of the Patter Buffer. By default, the contents of Pattern Buffer will be used once and stop. Alternatively, the Pattern Buffer will continue to loop until the DFXLCESTART is de-asserted. 0 : Run Pattern Buffer only once (default) 1 : Loop Pattern Buffer until stopped
24	0h RW	**cri_dfx_patbufdwidth:** Pattern Buffer Data Width Selects between 10 bit or 8 bit data width for the Pattern Buffer. Determines where in the Tx/Rx path the data is inserted/ retrieved. 0 : 10b (default) 1 : 8b
23	0h RW	**cri_dfx_patbuftrainovr:** Pattern Buffer Training Override Enables manual training of the Pattern Buffer instead of the automated coordination between the Pattern Checker and Patter Generator. When asserted, the DFXPATBUFTRAIN bit will be used to force when training is active and when it is complete. 0 : Automatic Training (default) 1 : Enable Manual Training
22	0h RW	**cri_dfx_marginmode:** Margin mode Overrides standard setup configurations for use with Eye Width Margining. 0 : Standard Mode (default) 1 : Margin Mode enabled
21	0h RW	**cri_dfx_chk_sel:** Pattern Checker 8b10b Select This determines where Rx data is compared, either in the 10-bit domain before decode or after 10b-)8b decoding. 0: 10b domain 1: 8b domain
20	0h RW	**cri_dfx_patchken:** Pattern Checker Enable 0 : Disable Pattern Checker (default) 1 : Enable Pattern Checker

Bit Range	Default & Access	Description
19	0h RW	**cri_dfx_patgenen:** Pattern Generator Enable This will activate the DFx bypass muxes in the PCS Tx path. 0 : Disable Pattern Generator (default) 1 : Enable Pattern Generator
18	0h RW	**cri_dfx_clrerrcnt:** Clear Error Counter Resets the Pattern Checker's error counter. 0 : Error Counter allowed to run (default) 1 : Error Counter held in reset
17	0h RW	**cri_dfx_lcereset:** Local Compare Engine Reset Resets all components of the Local Compare Engine in both the Pattern Generator and the Pattern Checker. 0 : LCE not in reset (default) 1 : LCE in reset
16	0h RW	**cri_dfx_lcestart:** Local Compare Engine Start Controls the starting and stopping of the LCE. Allows for simultaneous or independent start across lanes. Once stopped, a DFXLCERESET is usually required. 0 : LCE stopped (default) 1 : LCE running
15:8	3Eh RW	**cri_dfx_patbuf_7_0:** Pattern Buffer Storage In 10b mode, the buffer is read as eight 10b chunks. The first 10 bits should not equal the Comma Symbol: '0011111010' (or its inversion '1100000101'). In 8b mode, the buffer is read as eight 10b chunks, where the 10th bit is unused and the 9th bit is the K-bit indicator. The first 10 bits should not equal the Comma Symbol: 'xx10111100'. DFXPATBUF[78] should not = '1'.
7:0	63h RW	**cri_dfx_patbuf_15_8:** Pattern Buffer Storage See cri_dfx_patbuf[7:0] description.

18.13.7 PCS_DWORD6 (pcs_dword6)—Offset 18h

Access Method

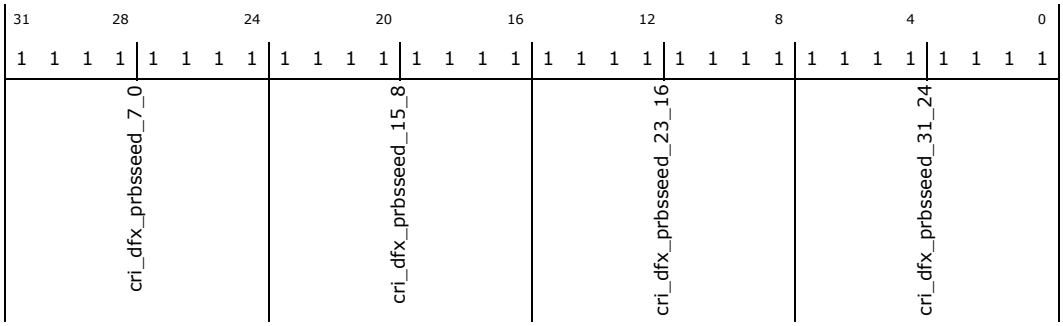
Type: Message Bus Register (Size: 32 bits)

pcs_dword6: [Port: 0xA6] + (800h + 18h)

Op Codes:

0h - Read, 1h - Write

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:24	FFh RW	**cri_dfx_prbsseed_7_0:** PRBS Seed Can be used for HVM determinism. The use of all zeroes can result in lockup.
23:16	FFh RW	**cri_dfx_prbsseed_15_8:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
15:8	FFh RW	**cri_dfx_prbsseed_23_16:** PRBS Seed See cri_dfx_prbsseed[7:0] description.
7:0	FFh RW	**cri_dfx_prbsseed_31_24:** PRBS Seed See cri_dfx_prbsseed[7:0] description.

18.13.8 PCS_DWORD7 (pcs_dword7)—Offset 1Ch

Access Method

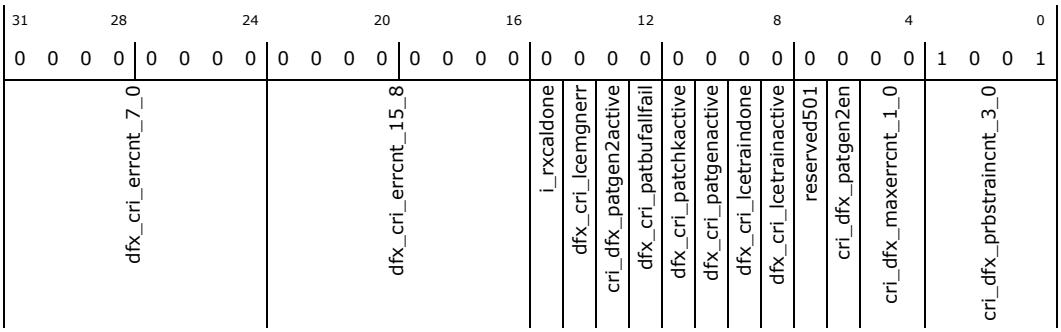
Type: Message Bus Register (Size: 32 bits)

pcs_dword7: [Port: 0xA6] + (800h + 1Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000009h



Bit Range	Default & Access	Description
31:24	X RO	**dfx_cri_errcnt_7_0:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
23:16	X RO	**dfx_cri_errcnt_15_8:** Error Counter Tracks how many bit errors the Pattern Checker has detected. Can be cleared using DFXCLRERRCNT or DFXLCERESET.
15	X RO	**i_rxcaldone:** RX Calibration Cycles Complete Indicator
14	X RO	**dfx_cri_lcemgnerr:** Local Compare Engine Margin Error Indicates that the error counter has reached its max value. This can be used by the Rx upartition during Margin Mode to determine when the eye width has closed.
13	X RO	**cri_dfx_patgen2active:** Pattern Generator 2 Active status indicator In a lane with two Tx paths, this indicates that the second Pattern Generator is in progress. The DFXPATGENACTIVE will only indicate that the first Pattern Generator is in progress.
12	X RO	**dfx_cri_patbufallfail:** Pattern Buffer All Fail status indicator Indicates that there has not been a single matching Pattern Buffer pattern. This could signify that an error occured during training.
11	X RO	**dfx_cri_patchkactive:** Pattern Checker Active status indicator Indicates that the Pattern Checker is in progress (either Pattern Buffer or PRBS).
10	X RO	**dfx_cri_patgenactive:** Pattern Generator Active status indicator Indicates that the Pattern Generator is in progress (either Pattern Buffer or PRBS).
9	X RO	**dfx_cri_lcetraindone:** Local Compare Engine Training Done status indicator Indicates that the Pattern Checker training is completed (either Pattern Buffer or PRBS). The Pattern Checker is now synchronized to the Pattern Generator.
8	X RO	**dfx_cri_lcetrainactive:** Local Compare Engine Training Active status indicator Indicates that the Pattern Checker training is in progress (either Pattern Buffer or PRBS).
7	0h RW	**reserved501:** reserved
6	0h RW	**cri_dfx_patgen2en:** Pattern Generator 2 Enable In a lane with two Tx paths, this enables the second Pattern Generator. The DFXPATGENEN will enable the first Pattern Generator. 0 : Disable second Pattern Generator (default) 1 : Enable second Pattern Generator

Bit Range	Default & Access	Description
5:4	0h RW	**cri_dfx_maxerrcnt_1_0:** Maximum Error Count Selectable maximum value that the DFXERRCNT can reach before the Local Compare Engine is automatically stopped. 00 : 2^16 (default) 01 : 2^10 10 : 2^8 11 : 2^4
3:0	9h RW	**cri_dfx_prbstraincnt_3_0:** PRBS Training Count The number of consecutive cycles that the Pattern Checker's PRBS must be error free before it is considered synchronized. Default is 9.

18.13.9 PCS_DWORD8 (pcs_dword8)—Offset 20h

Access Method

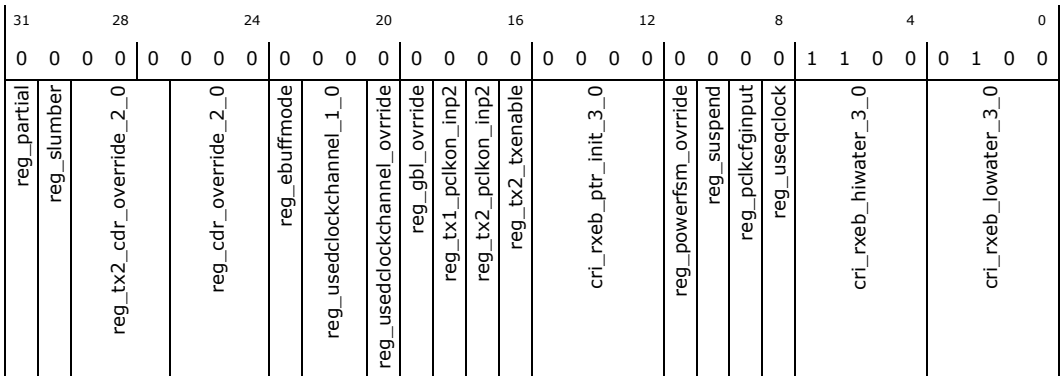
Type: Message Bus Register (Size: 32 bits)

pcs_dword8: [Port: 0xA6] + (800h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 000000C4h



Bit Range	Default & Access	Description
31	0h RW	**reg_partial:** Override for i_partial
30	0h RW	**reg_slumber:** Override for i_slumber
29:27	0h RW	**reg_tx2_cdr_override_2_0:** Override for cdr_override strap for second tx2
26:24	0h RW	**reg_cdr_override_2_0:** Override for cdr_override strap
23	0h RW	**reg_ebuffmode:** Override for ebuffmode (no functionality in p1271 phase1 design)
22:21	0h RW	**reg_usedclockchannel_1_0:** Selects the active clock channel
20	0h RW	**reg_usedclockchannel_ovrride:** When asserted selects reg_usedclockchannel[1:0]
19	0h RW	**reg_gbl_ovrride:** Global override select
18	0h RW	**reg_tx1_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. For DP this is used for Lane1

Bit Range	Default & Access	Description
17	0h RW	**reg_tx2_pclkon_inp2:** When asserted keeps PCLK running in P2 mode. This is reserved (no impact) for PCIe/DMI and used for DP Lane2
16	0h RW	**reg_tx2_txenable:** Override for i_txenable for tx2
15:12	0h RW	**cri_rxeb_ptr_init_3_0:** Config override for initial value of Rx elastic buffer read pointer
11	0h RW	**reg_powerfsm_ovrride:** When asserted overrides for Tx power fsm are selected
10	0h RW	**reg_suspend:** Override for suspend
9	0h RW	**reg_pclkcfginput:** Override for pclkcfginput strap
8	0h RW	**reg_useqclock:** Override for useqclock; MUX select for I or Q clk for TX clocking
7:4	Ch RW	**cri_rxeb_hiwater_3_0:** Elastic buffer high watermark based on which SKP is removed
3:0	4h RW	**cri_rxeb_lowater_3_0:** Elastic buffer low watermark based on which SKP is added

18.13.10 PCS_DWORD9 (pcs_dword9)—Offset 24h

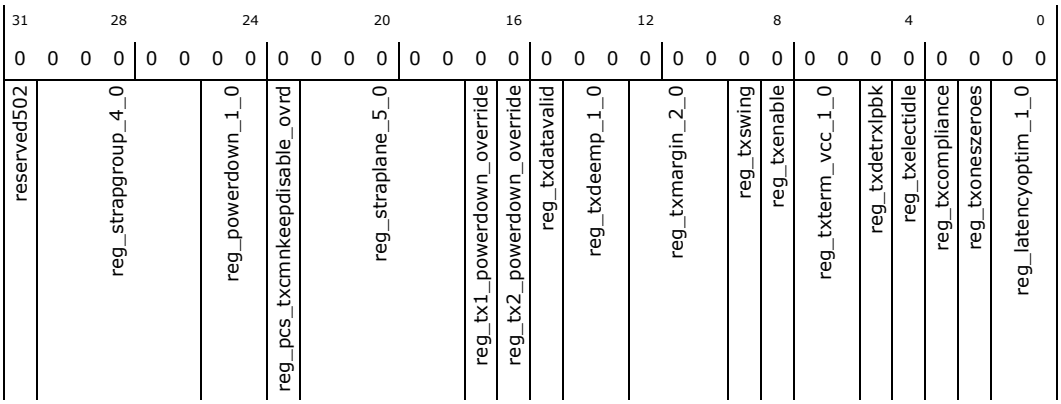
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword9: [Port: 0xA6] + (800h + 24h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**reserved502:** reserved
30:26	0h RW	**reg_strapgroup_4_0:** Override for i_strapgroup

Bit Range	Default & Access	Description
25:24	0h RW	**reg_powerdown_1_0:** Override for i_powerdown
23	0h RW	**reg_pcs_txcmnkeepdisable_ovrd:** Override for ipcs_txcmnkeepdisable input 0: Use value on ipcs_txcmnkeepdisable input pin to determine o_txgohighz state in P2/ slumber 1: Force pcs_txcmnkeepdisable to 0
22:18	0h RW	**reg_straplane_5_0:** Override for i_straplane
17	0h RW	**reg_tx1_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx1 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
16	0h RW	**reg_tx2_powerdown_override:** Overrides i_powerdown[1:0] indication from MAC for Tx2 1 : selects reg_powerdown[1:0] 0 : selects i_powerdown[1:0]
15	0h RW	**reg_txdatavalid:** Override for i_txdatavalid (register is NOT used)
14:13	0h RW	**reg_txdeemp_1_0:** Override for i_txdeemph
12:10	0h RW	**reg_txmargin_2_0:** Override for i_txmargin
9	0h RW	**reg_txswing:** Override for i_txswing
8	0h RW	**reg_txenable:** Override for i_txenable
7:6	0h RW	**reg_txterm_vcc_1_0:** Override for txterm_vcc strap
5	0h RW	**reg_txdetrxlpbk:** Override for i_txdetrxlpbk
4	0h RW	**reg_txelectidle:** Override for i_txelectidle
3	0h RW	**reg_txcompliance:** Override for i_txcompliance
2	0h RW	**reg_txoneszeroes:** Override for i_txoneszeroes
1:0	0h RW	**reg_latencyoptim_1_0:** Override for i_latencyoptim

18.13.11 PCS_DWORD10 (pcs_dword10)—Offset 28h

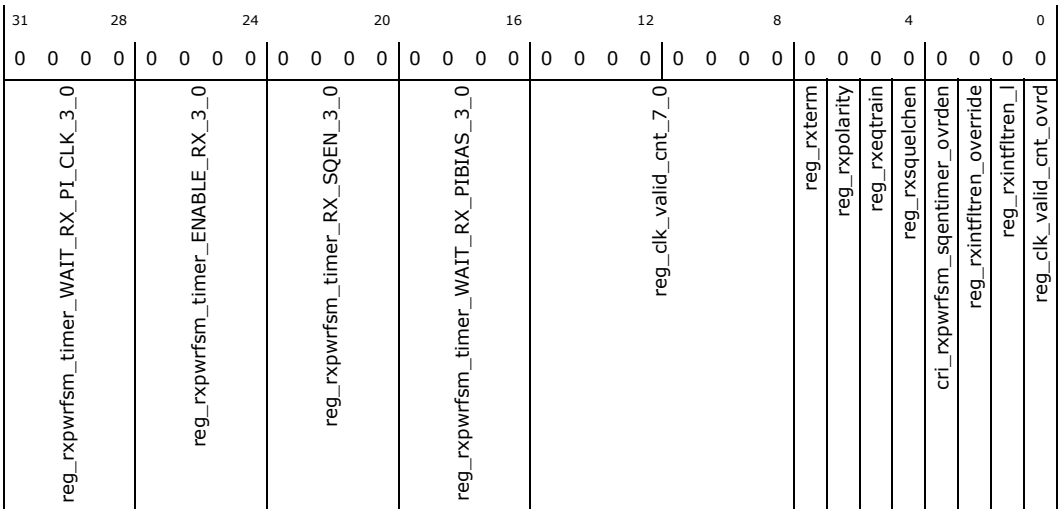
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword10: [Port: 0xA6] + (800h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:28	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PI_CLK_3_0:** Rx Power state m/c timer value used to enable PI clock
27:24	0h RW	**reg_rxpwrfsm_timer_ENABLE_RX_3_0:** Rx Power state m/c timer value used to enable receivers
23:20	0h RW	**reg_rxpwrfsm_timer_RX_SQEN_3_0:** Rx Power FSM Rx Squelch Enable Timer Override Value Affect squelch enable startup sequence during 'synchronous' squelch startup mode. 0000 - Invalid 0001 - 1 susclk period ... 1111 - 15 susclk period
19:16	0h RW	**reg_rxpwrfsm_timer_WAIT_RX_PIBIAS_3_0:** Rx Power state m/c timer value used to enable PI BIAS
15:8	0h RW	**reg_clk_valid_cnt_7_0:** Over ride value for clock valid delay in clock top block before toggling phystatus.
7	0h RW	**reg_rxterm:** Override for i_rxterm
6	0h RW	**reg_rxpolarity:** Override for i_rxpolarity
5	0h RW	**reg_rxeqtrain:** Override for i_rxeqtrain
4	0h RW	**reg_rxsquelchen:** Override for i_rxsquelchen
3	0h RW	**cri_rxpwrfsm_sqentimer_ovrden:** Squelch Enable Timer Override Enable Used to override the squelch enable timer in PCS with the timer value set by the Rx Squelch Enable timer register (reg_rxpwrfsm_timer_RX_SQEN[3:0]).

Bit Range	Default & Access	Description
2	0h RW	**reg_rxintfltren_override:** Rx Integral Filter Override Select 0: selects i_rxintfltren_l input pin. 1: selects reg_rxintfltren_l register
1	0h RW	**reg_rxintfltren_l:** Override for Rx integral filter enable i_rxintfltren_l
0	0h RW	**reg_clk_valid_cnt_ovrd:** Override enable for reg_clk_valid_cnt

18.13.12 PCS_DWORD11 (pcs_dword11)—Offset 2Ch

Access Method

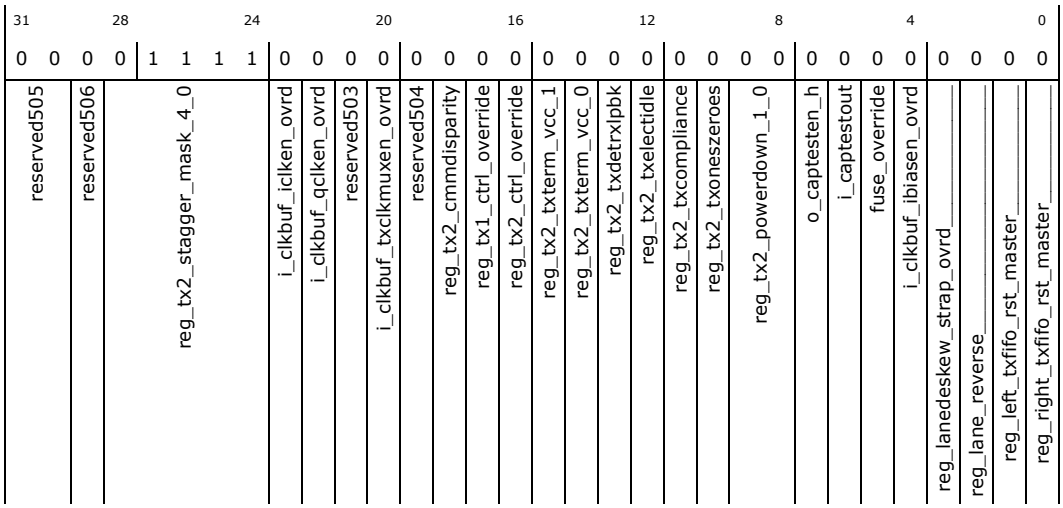
Type: Message Bus Register (Size: 32 bits)

pcs_dword11: [Port: 0xA6] + (800h + 2Ch)

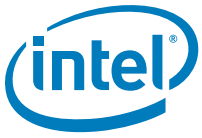
Op Codes:

0h - Read, 1h - Write

Default: 0F000000h



Bit Range	Default & Access	Description
31:30	0h RW	**reserved505:** reserved
29	0h RW	**reserved506:** reserved
28:24	Fh RW	**reg_tx2_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering. for tx2
23	0h RW	**i_clkbuf_iclken_ovrd:** I-Clock Override for the DataLane
22	0h RW	**i_clkbuf_qclken_ovrd:** Q-Clock Override for the DataLane
21	0h RW	**reserved503:** reserved



Bit Range	Default & Access	Description
20	0h RW	**i_clkbuf_txclkmuxen_ovrd:** TX Clock Selection Mux Override
19	0h RW	**reserved504:** reserved
18	0h RW	**reg_tx2_cmmdisparity:** Sets the initial disparity during Compliance Measurement Mode, used together with pcs_txcompliance pulse. For TX2 0 = set negative disparity 1 = set positive disparity
17	0h RW	**reg_tx1_ctrl_override:** overrides input parameter/controls for tx1
16	0h RW	**reg_tx2_ctrl_override:** overrides input parameter/controls for tx2
15	0h RW	**reg_tx2_txterm_vcc_1:** Override for txterm_vcc strap[1] for tx2 in DP family. Override enable for inspeccmm for non-DP families (reg_inspeccmm_ovrd_enable).
14	0h RW	**reg_tx2_txterm_vcc_0:** Override for txterm_vcc strap[0] for tx2 in DP family. Override value for inspeccmm for non-DP families (reg_inspeccmm_ovrd_value).
13	0h RW	**reg_tx2_txdetrxlpbk:** Override for i_txdetrxlpbk for tx2
12	0h RW	**reg_tx2_txelectidle:** Override for i_txelectidle for tx2
11	0h RW	**reg_tx2_txcompliance:** Override for i_txcompliance for tx2
10	0h RW	**reg_tx2_txoneszeroes:** Override for i_txoneszeroes for tx2
9:8	0h RW	**reg_tx2_powerdown_1_0:** Override for i_powerdown for tx2
7	0h RW	**o_captesten_h:** Enable testing of capacitors
6	X RO	**i_captestout:** Capacitor test result
5	0h RW	**fuse_override:** Overrides Lane fuses 1: override txterm_vcc, latencyoptim, cdr_override, rxterm_vcc 0: fuses not overridden
4	0h RW	**i_clkbuf_ibiasen_ovrd:** Override i_clkbuf_ibiasen value RX CML driver bias enable
3	0h RW	**reg_lanedeskew_strap_ovrd_____:** reserved
2	0h RW	**reg_lane_reverse_____:** reserved
1	0h RW	**reg_left_txfifo_rst_master_____:** reserved
0	0h RW	**reg_right_txfifo_rst_master_____:** reserved

18.13.13 PCS_DWORD12 (pcs_dword12)—Offset 30h

Access Method

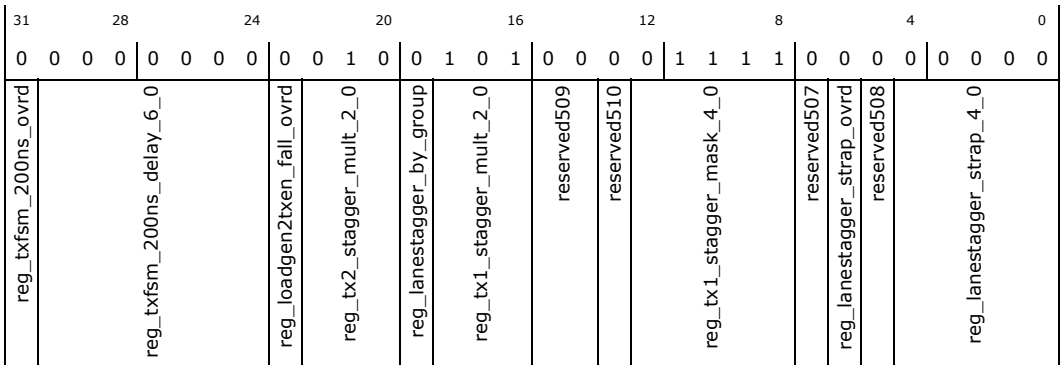
Type: Message Bus Register (Size: 32 bits)

pcs_dword12: [Port: 0xA6] + (800h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00250F00h



Bit Range	Default & Access	Description
31	0h RW	**reg_txfsm_200ns_ovrd:** Override reg_txfsm_200ns_delay+G2
30:24	0h RW	**reg_txfsm_200ns_delay_6_0:** Override value of counter for 200ns delay between txen and txloadgenen
23	0h RW	**reg_loadgen2txen_fall_ovrd:** reserved
22:20	2h RW	**reg_tx2_stagger_mult_2_0:** Stagger multiplier for Rx (or Tx1) (Same decoding as tx1_stagger_mult[2:0]) For Display, this multiplier applies to Tx2. For non-Display PHYs, this multiplier applies to the Rx. The multiplier limit for the Rx is 8x (3'b100); anything beyond that is invalid.
19	0h RW	**reg_lanestagger_by_group:** When = 1, uses group number for lane staggering, by devalues lane number is used.
18:16	5h RW	**reg_tx1_stagger_mult_2_0:** Stagger multiplier for Tx (or Tx1) These bits set the lane staggering multiplier for the transmitter based on the 'linkclk' period. 000 - 0x 001 - 1x 010 - 2x 011 - 4x 100 - 8x 101 - 16x 110 - 32x 111 - 64x For Display, this multiplier applies to Tx1.
15:14	0h RW	**reserved509:** reserved
13	0h RW	**reserved510:** reserved
12:8	Fh RW	**reg_tx1_stagger_mask_4_0:** Mask bit for lane number. Used to group lanes for staggering
7	0h RW	**reserved507:** reserved
6	0h RW	**reg_lanestagger_strap_ovrd:** When 1 config override for lane stagger strap (bits [4:0] of this register) is selected
5	0h RW	**reserved508:** reserved

Bit Range	Default & Access	Description
4:0	0h RW	**reg_lanestagger_strap_4_0:** Override for lane stagger strap

18.13.14 PCS_DWORD13 (pcs_dword13)—Offset 34h

Access Method

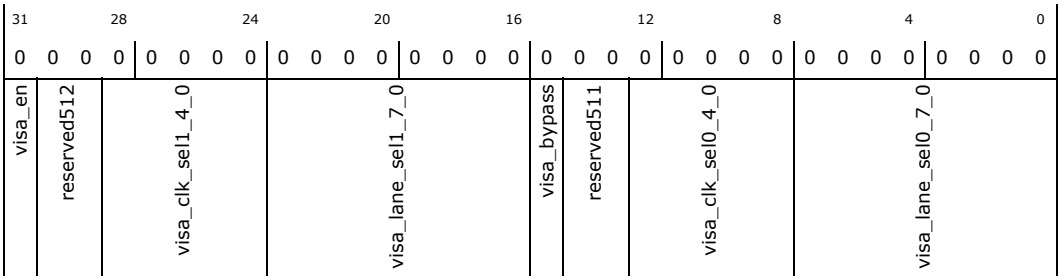
Type: Message Bus Register (Size: 32 bits)

pcs_dword13: [Port: 0xA6] + (800h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**visa_en:** VISA Enable for PCS VISA logic
30:29	0h RW	**reserved512:** reserved
28:24	0h RW	**visa_clk_sel1_4_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.
23:16	0h RW	**visa_lane_sel1_7_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane0.
15	0h RW	**visa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
14:13	0h RW	**reserved511:** reserved
12:8	0h RW	**visa_clk_sel0_4_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
7:0	0h RW	**visa_lane_sel0_7_0:** VISA Lane Select for Lane0. Selects the byte of data to be sent out on lane0.

18.13.15 PCS_DWORD14 (pcs_dword14)—Offset 38h

Access Method

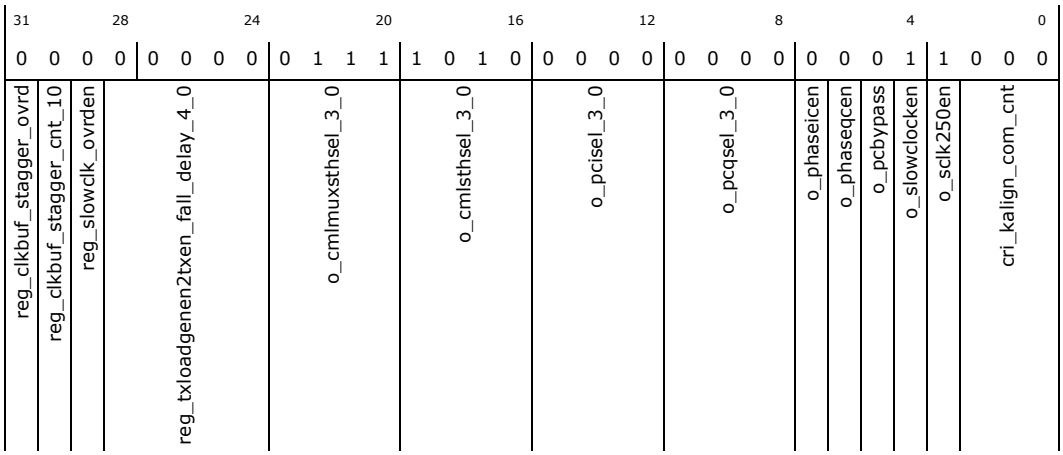
Type: Message Bus Register (Size: 32 bits)

pcs_dword14: [Port: 0xA6] + (800h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 007A0018h



Bit Range	Default & Access	Description
31	0h RW	**reg_clkbuf_stagger_ovrd:** Override enable for reg_clkbuf_stagger_cnt
30	0h RW	**reg_clkbuf_stagger_cnt_10:** Counter override value for staggering delay of clock buffer control signals.
29	0h RW	**reg_slowclk_ovrden:** Slow Clock Override Enable When set 1'b1, reg_slowclocken and reg_sclk250en are valid. When cleared 1'b0, output of FSM will drive slow clock enable.
28:24	0h RW	**reg_txloadgenen2txen_fall_delay_4_0:** reserved
23:20	7h RW	**o_cmlmuxsthsel_3_0:** CML Mux strength control
19:16	Ah RW	**o_cmlsthsel_3_0:** RX CML driver strength
15:12	0h RW	**o_pcisel_3_0:** I clk phase correction control
11:8	0h RW	**o_pcqsel_3_0:** Q clk phase correction control
7	0h RW	**o_phaseicen:** Iclk phase correction enable.
6	0h RW	**o_phaseqcen:** Qclk phase correction enabled.
5	0h RW	**o_pcbypass:** Phase correction bypass.

Bit Range	Default & Access	Description
4	1h RW	**o_slowclocken:** Slow clock 1 enable Only valid if slow clock override enable is set 1'b1
3	1h RW	**o_sclk250en:** Slow clock 2 enable Only valid if slow clock override enable is set 1'b1
2:0	0h RW	**cri_kalign_com_cnt:** Upper 3 bits of a 7-bit counter that counts number of COM characters found. Used for special SAPIS mode where spread spectrum clocking can be utilized. Note: This register is used in conjunction with another PCS register cri_kalignmode[1:0] = 10 Register value Minimum COM count to achieve symbol lock 000 - 18 001 - 34 010 - 50 011 - 66 100 - 82 101 - 98 110 - 114 111 - 130

18.13.16 PCS_DWORD15 (pcs_dword15)—Offset 3Ch

Access Method

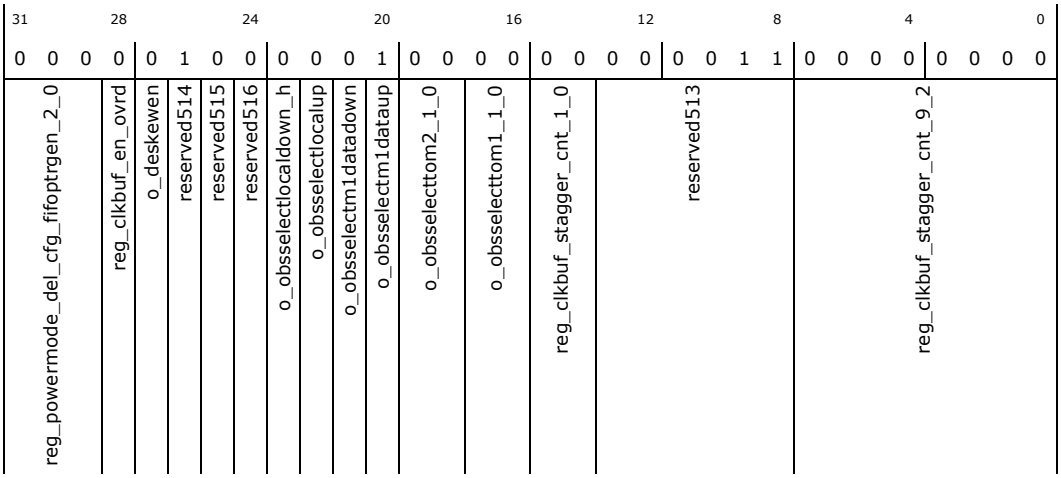
Type: Message Bus Register (Size: 32 bits)

pcs_dword15: [Port: 0xA6] + (800h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 04100300h



Bit Range	Default & Access	Description
31:29	0h RW	**reg_powermode_del_cfg_fifoptrgen_2_0:** Controls the delay from powermode change to Tx PCS data fifo pointer de-assertion 000 = 'd280 001 = 'd20 010 = 'd48 011 = 'd80 100 = 'd144 101 = 'd538 110 = 'd800 111 = 'd1023
28	0h RW	**reg_clkbuf_en_ovrd:** ClkBuf Override Enable When asserted, the overrides for the CLKBUF (i_clkbuf_*_ovrd) are selected. Enable TX clock selection MUX
27	0h RW	**o_deskewen:** DFT output deskew enable
26	1h RW	**reserved514:** reserved
25	0h RW	**reserved515:** reserved

Bit Range	Default & Access	Description
24	0h RW	**reserved516:** reserved
23	0h RW	**o_obsselectlocaldown_h:** N/N+1 Abut Obs-UP output control Selects local 'down' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsup inputs to be driven on oabut_obsup outputs. 0: select signals from the iabut_obsup inputs 1: select 'down' signals from the current lane
22	0h RW	**o_obsselectlocalup:** N/N+1 Abut Obs DOWN output control Selects local 'up' signals from current lane Tx1 (M1) and Rx/Tx2 (M2) or the iabut_obsdown inputs to be driven on oabut_obsdown outputs and to the current lane's Tx1 or Tx2. 0: select signals from the iabut_obsdown inputs 1: select 'up' signals from the current lane
21	0h RW	**o_obsselectm1datadown:** N/N+1 M1-M2 Down data control Selects local 'down' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocaldown muxes that are controlled by bit 7. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
20	1h RW	**o_obsselectm1dataup:** N/N+1 M1-M2 Up data control Selects local 'up' data input signals from M1 (Tx1) or M2 (Tx2 or Rx) to be sent to the obsselectlocalup muxes that are controlled by bit 6. 0: select M2 (Tx2 or Rx) 1. select M1 (Tx1)
19:18	0h RW	**o_obsselecttom2_1_0:** N/N+1 M2 Output Select This controls which signals are sent to Tx2. These outputs are not used when M2 is a Receiver. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
17:16	0h RW	**o_obsselecttom1_1_0:** N/N+1 M1 Output Select This controls which signals are sent to Tx1. 00: iabut_obsdown 01: iabut_obsup 10: output of local 'up' select muxes that are controlled by bit 6 11: GND
15:14	0h RW	**reg_clkbuf_stagger_cnt_1_0:** Counter override value for staggering delay of clock buffer control signals.
13:8	3h RW	**reserved513:** reserved
7:0	0h RW	**reg_clkbuf_stagger_cnt_9_2:** Counter override value for staggering delay of clock buffer control signals.

18.13.17 PCS_DWORD16 (pcs_dword16)—Offset 40h

Access Method

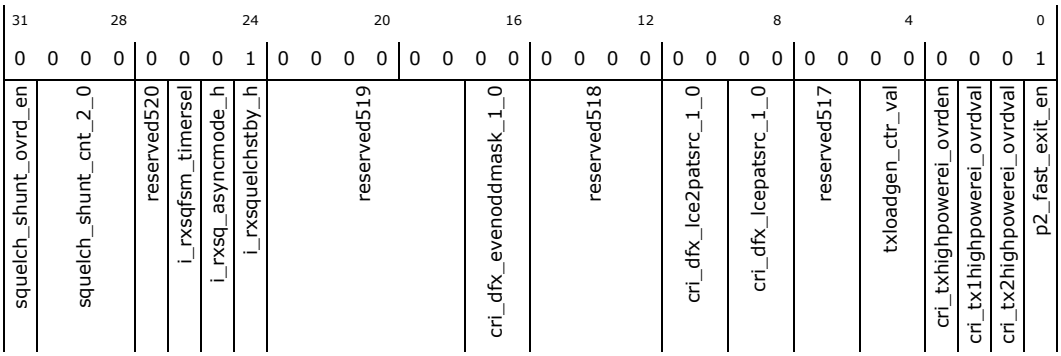
Type: Message Bus Register (Size: 32 bits)

pcs_dword16: [Port: 0xA6] + (800h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31	0h RW	**squelch_shunt_ovrd_en:** Squelch Shunt Pulse Duration Override Enable Overrides the hardware default shunt pulse duration value 1: Shunt Pulse Duration Override Enable 0: Shunt Pulse Duration Override Disable
30:28	0h RW	**squelch_shunt_cnt_2_0:** Squelch Shunt Pulse Duration Override Value 000 = No shunt pulse generated 001 = 1 susclk cycles ... 111 = 7 susclk cycles
27	0h RW	**reserved520:** reserved
26	0h RW	**i_rxsqfsm_timersel:** Squelch FSM Timer Select 0 - Selects 25Mhz values for squelch timer and shunt pulse generation . 1 - Selects 100Mhz values for squelch timer and shunt pulse generation. This register is applicable to synchronous squelch startup mode.
25	0h RW	**i_rxsq_asyncmode_h:** Squelch Async Startup Mode This squelch startup mode is power state independent. When enabled, the squelchen signal sent to Modphy will asynchronously enable the squelch detector circuit. Once enabled, the squelch detector circuit will asynchronously send an unfiltered/unqualified squelch indication signal out of Modphy. The squelch indication signal will initially be unstable, so it is up to the consumer of this signal to filter/qualfiy it accordingly. The asynchronous squelch startup mode is beneficial because it significantly reduces the squelch startup latency. This decrease in latency does come at the cost of slightly higher power when squelch is not enabled as the IREF and Squelch Keeper circuits must remain enabled. When disabled, the squelch startup sequence is synchronous in nature and the squelch indication signal sent out of Modphy is stable/filtered.
24	1h RW	**i_rxsquelchstby_h:** Fast Squelch Enable Mode Bit to keep the IREF (ivrefen) on during P2 and reduce squelch startup time.
23:18	0h RW	**reserved519:** reserved
17:16	0h RW	**cri_dfx_evenoddmask_1_0:** Pattern Checker Even/Odd Bit Error Mask Select 00 : no masking; all errors will be counted 01: select odd path, mask even path; only errors on bits [1,3,5,7,9] are counted 10: select even path, mask odd path; only errors on bits [0,2,4,6,8] are counted 11: reserved;
15:12	0h RW	**reserved518:** reserved

Bit Range	Default & Access	Description
11:10	0h RW	**cri_dfx_lce2patsrc_1_0:** Local Compare Engine 2 Pattern Source In a lane with two Tx paths, this selects between using Pattern Buffer or PRBS as source of LCE patterns for the second LCE. The DFXLCEPATSRC selects for the first LCE. 0 : Pattern Buffer (default) 1 : PRBS
9:8	0h RW	**cri_dfx_lcepatsrc_1_0:** Local Compare Engine Pattern Source. Selects between using Pattern Buffer or PRBS as source of LCE patterns. 00 : Pattern Buffer; use LCE default training pattern; 01: Pattern Buffer; use the first 40b of pattern buffer for training. 10: PRBS; use LCE default training pattern; 11: PRBS; use the first 40b of pattern buffer for training.
7:6	0h RW	**reserved517:** reserved
5:4	0h RW	**txloadgen_ctr_val:** TxLoadGen Pulse Width Control Controls the pulse width of txloadgenen from PCS to Tx upar. This is used in MAC inititated digital far end loopback mode in PCIE family. 00 - txloadgenen pulse width is 4 symbol clocks (default) 01- txloadgenen pulse width is 2 symbol clocks 10 - txloadgenen pulse not generated 11 - txloadgenen pulse width is 6 symbol clocks
3	0h RW	**cri_txhighpowerei_ovrden:** TxHighPowerEI Override Mode Enable 0 - TxHighPowerEI to TxuPAR driven by Logic 1 - TxHighPowerEI to TxuPAR driven by override register value(s).
2	0h RW	**cri_tx1highpowerei_ovrdval:** Tx1HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx1HighPowerEI disabled 1 - Tx1HighPowerEI enabled
1	0h RW	**cri_tx2highpowerei_ovrdval:** Tx2HighPowerEI Override Value Valid when cri_txhighpowerei_ovrden = 1'b1. 0 - Tx2HighPowerEI disabled 1 - Tx2HighPowerEI enabled
0	1h RW	**p2_fast_exit_en:** P2 Fast Exit Mode Enable Common Mode sustainer will be enabled during P2 when this bit is asserted. 1: P2 Fast Exit Mode Enable 0: P2 Fast Exit Mode Disable

18.13.18 PCS_DWORD17 (pcs_dword17)—Offset 44h

Access Method

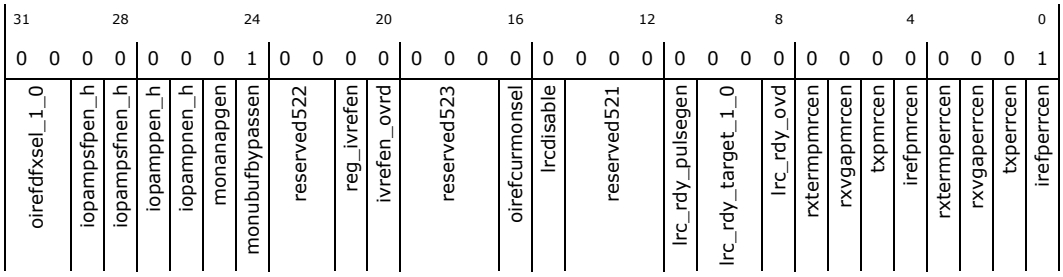
Type: Message Bus Register (Size: 32 bits)

pcs_dword17: [Port: 0xA6] + (800h + 44h)

Op Codes:

0h - Read, 1h - Write

Default: 01000001h



Bit Range	Default & Access	Description
31:30	0h RW	**oirefdfxsel_1_0:** IREF Voltage Monitor Select Selects voltage to monitor within the IREF block. 00 - vref 01 - pgate 10 - vbc 11 - vref loop
29	0h RW	**iopampsfpen_h:** (NOT USED - noconned)

Bit Range	Default & Access	Description
28	0h RW	**iopampsfnen_h:** (NOT USED - noconned)
27	0h RW	**iopamppen_h:** DC Monitor Unity-Gain Buffer Enable 0: disable (default) 1: enable
26	0h RW	**iopampnen_h:** (NOT USED - noconned)
25	0h RW	**monanapgen:** DC Monitor to Monitor Port Enable Enables DC monitor passgate to monitor port via analog observability abutment.
24	1h RW	**monubufbypassen:** DC Monitor Unity-Gain Buffer Bypass 0: no bypass 1: bypass (default - required for LRC)
23:22	0h RW	**reserved522:** reserved
21	0h RW	**reg_ivrefen:** IvrefEn Override Value Register is valid when override mode is enabled (ivrefen_ovrd). During this mode, this register will have direct control to enable/disable the ivref opamp. 0 - Disable ivref opamp 1 - Enable ivref opamp
20	0h RW	**ivrefen_ovrd:** IvrefEn Override Select 0 - the enable for the ivref opamp (ivrefen) is driven by the FSM. 1 - the ivrefen is driven by the register (reg_ivrefen).
19:17	0h RW	**reserved523:** reserved
16	0h RW	**oirefcurmonsel:** IREF Current Monitor Select Enables current mirror from the IREF block to the 'shared' analog monitor port.
15	0h RW	**lrcdisable:** LRC Disable This bit disables the LRC. Any token received is passed to the next lane.
14:12	0h RW	**reserved521:** reserved
11	0h RW	**lrc_rdy_pulsegen:** LRC Ready PulseGen Generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal to all four targets; does not recompute local Rcomp code. Values in DWD 0x14 (*rccodes[7:0]) will be latched into targets. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
10:9	0h RW	**lrc_rdy_target_1_0:** LRC Ready Pulse Target Indicates which lrc target to recompute when lrc_rdy_ovd is strobed 00: irefrccode 01: txrccode 10: rxtermrccode 11: rxvgarccode
8	0h RW	**lrc_rdy_ovd:** LRC Ready Override Recomputes the selected local rcomp code and generates a pulse 1 cal_clk cycle wide on the lrc_rdy signal that is selected in bits [2:1]. User must clear this bit before generating another pulse. Note: User should disable PM and PER. FSM can take control and codes can be overriden.
7	0h RW	**rxtermpmrcen:** PM RCOMP Enable for Rx Termination 1 - Enables the RCOMP update to occur while RX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
6	0h RW	**rxvgapmrcen:** PM RCOMP Enable for Rx VGA (Same description as the RxTerm PM Rcomp Enable.)
5	0h RW	**txpmrcen:** PM RCOMP Enable for Tx 1 - Enables the RCOMP update to occur while TX is in power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
4	0h RW	**irefpmrcen:** IREF PM RCOMP Enable 1 - Enables the RCOMP update to occur while TX/RX is in the P1 or P2 (partial or slumber) power management state if periodic RCOMP is enabled. If this bit is set and the PHY is not in a power management state, no update will occur. 0 - Disables power management qualifier to the RCOMP update; therefore RCOMP updates will be based on the state of the target periodic bit.
3	0h RW	**rxtermperrcen:** Periodic RCOMP Enable for Rx Termination 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

Bit Range	Default & Access	Description
2	0h RW	**rxvgaperrcen:** Periodic RCOMP Enable for Rx VGA 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
1	0h RW	**txperrcen:** Periodic RCOMP Enable for Tx 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.
0	1h RW	**irefperrcen:** Periodic RCOMP Enable for Iref 1 - Enables the periodic RCOMP update for specified block. 0 - Disables periodic RCOMP update for specified block.

18.13.19 PCS_DWORD18 (pcs_dword18)—Offset 48h

Access Method

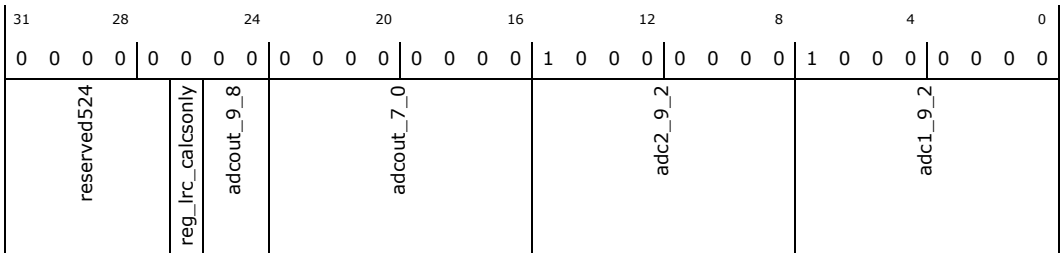
Type: Message Bus Register (Size: 32 bits)

pcs_dword18: [Port: 0xA6] + (800h + 48h)

Op Codes:

0h - Read, 1h - Write

Default: 00008080h



Bit Range	Default & Access	Description
31:27	0h RW	**reserved524:** reserved
26	0h RW	**reg_lrc_calcsonly:** Determines whether LRC ADC1/2 sequence will be bypassed when crireset_l goes from asserted to de-asserted state 0: Full LRC sequence will run (both ADC1/2 and calculations) 1: Do not run LRC ADC1/2. Only LRC calculations sequence will run. It is expected that ADC1/2 config registers will be overridden with desired values when using this mode
25:24	X RO	**adcout_9_8:** ADC Output Value2 Output of the ADC decimation filter; 2 upper bits out of 10.
23:16	X RO	**adcout_7_0:** ADC Output Value1 Output of the ADC decimation filter; 8 lower bits out of 10.
15:8	80h RW	**adc2_9_2:** LRC ADC2 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.
7:0	80h RW	**adc1_9_2:** LRC ADC1 Value Values in this register will be used by LRC_FSM to compute and cancel out IR drop. If register is written prior to LRC cycle, values will be overridden by FSM. If registers are written after LRC cycle, the original values are overridden and the new values will be applicable and will be used for subsequent cycle.

18.13.20 PCS_DWORD19 (pcs_dword19)—Offset 4Ch

Access Method

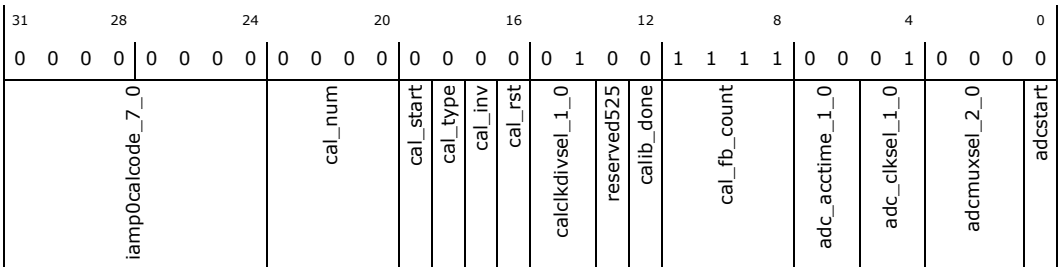
Type: Message Bus Register (Size: 32 bits)

pcs_dword19: [Port: 0xA6] + (800h + 4Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00004F10h



Bit Range	Default & Access	Description
31:24	0h RW	**iamp0calcode_7_0:** IREF Opamp Calibration Codes These bits are written by the calibration state machine. Bit7 - Calibration enable that configures the target into a calibration mode Bit6 - Calibration sign bit Bit[5:0] - Calibration magnitude [Iyonel to check bit7 functionality].
23:20	0h RW	**cal_num:** Calibration Number or Address numbers of cal targets or address for specific cal target if cal_type = 1
19	0h RW	**cal_start:** Calibration Start This bit is used to start a Cal cycle vias IOSF-SB. The cal cycle will follow the normal cal cycle as set by cal_num, cal_type, cal_inv and cal_rst. The Cal cycle starts when this bit transitions 0 1 1 = Run Cal. 0 = wait (default)
18	0h RW	**cal_type:** Calibration Type Enable calibration of one cal target defined by cal_num 0 = multi 1 = single
17	0h RW	**cal_inv:** Calibration Feedback Invert Inverse the logic of counter increment decrement depends on the FB
16	0h RW	**cal_rst:** Calibration Reset Reset state machine
15:14	1h RW	**calclkdivsel_1_0:** Calibration Clock Divider Select 00 - div2 of CRICLK 01 - div4 of CRICLK 10 - div8 of CRICLK 11 - div16 of CRICLK Note: Calibration clock period target is 160nS
13	0h RO	**reserved525:** reserved
12	0h RO	**calib_done:** Calibration Completion Indicator
11:8	Fh RW	**cal_fb_count:** Calibration Cycle Count Limit per target Each calibration target is clocked for 16 * cal_fb_count clock cycles. Max is 240 clock cycles (default)
7:6	0h RW	**adc_acctime_1_0:** ADC Accumulation Time Select This selects the conversion time for the Analog to Digital Converter. ADC clock frequency is set by bits [5:4] in this register. 00: 1024 ADC clocks (default) 01: 512 ADC clocks 10: 256 ADC clocks 11: Infinite (ADC in continuous accumulation) Note: If LRC mode and set to '11', then adctime = 1024cycles.
5:4	1h RW	**adc_clksel_1_0:** ADC Clock Frequency Select This selects the input clock frequency to the Analog to Digital Converter. 00: CRI clock div2 01: CRI clock div1 10: CRI clock div4 11: CRI clock div8 NOTE: Target is 50Mhz.

Bit Range	Default & Access	Description
3:1	0h RW	**adcmuxsel_2_0:** ADC Analog Mux Select This selects the analog voltage input to the Analog to Digital Converter. 000: Vss 001: Vcc 010: LRC R1 voltage divider 011: LRC sense net 100: input from Tx 101: input from Rx (or Tx #2) 110: input from Clock 111: input from reference generator Note: Mux select is controlled by the FSM during LRC.
0	0h RW	**adcstart:** ADC start This bit resets the ADC counter and starts a new acquisition. This bit should remain 1'b1 while the ADC is active and acquiring data. 0: Disable ADC logic and analog circuitry 1: Enable ADC and start A2D conversion.

18.13.21 PCS_DWORD20 (pcs_dword20)—Offset 50h

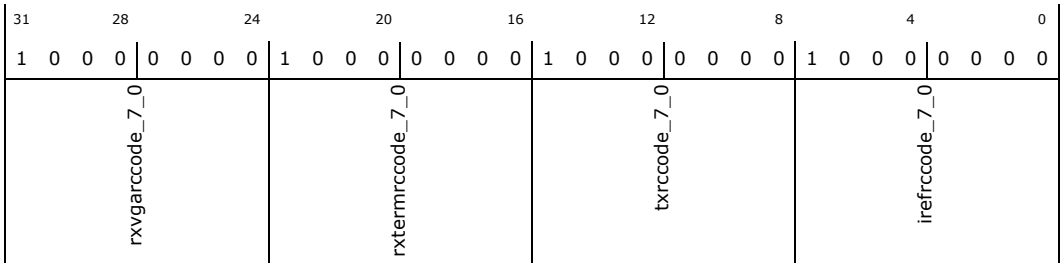
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword20: [Port: 0xA6] + (800h + 50h)

Op Codes:
0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarccode_7_0:** Rx VGA Rcomp Codes These bits are the final binary code used by the Rx VGA. This block only uses the X upper MSBs of this value. Writing to this register will override the rcomp code to the Rx VGA. An LRC Ready pulse must be generated to the Rx VGA target for this value to take effect. [7:n] - compensation code sent to Iref [n-1:0] - remaining LSBs from scaling and offset calculation
23:16	80h RW	**rxtermrccode_7_0:** Rx Termination Rcomp Codes These bits are the final binary code used by the Rx termination. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to Rxterm. An LRC Ready pulse must be generated to the Rxterm target for this value to take effect. [7:1] - compensation code sent to Rxterm [0] - remaining LSB from scaling and offset calculation
15:8	80h RW	**txrccode_7_0:** Tx Rcomp Codes These bits are the final binary code used by the Tx. This block only uses the 7 upper MSBs of this value. Writing to this register will override the rcomp code to the Tx. An LRC Ready pulse must be generated to the Tx target for this value to take effect. [7:1] - compensation code sent to Tx [0] - remaining LSB from scaling and offset calculation
7:0	80h RW	**irefrccode_7_0:** Iref Rcomp Codes These bits are the final binary code used by the Iref block. This block only uses the 6 upper MSBs of this value. Writing to this register will override the rcomp code to the Iref block. An LRC Ready pulse must be generated to the Iref target for this value to take effect. [7:2] - compensation code sent to Iref [1:0] - remaining LSBs from scaling and offset calculation

18.13.22 PCS_DWORD21 (pcs_dword21)—Offset 54h

Access Method

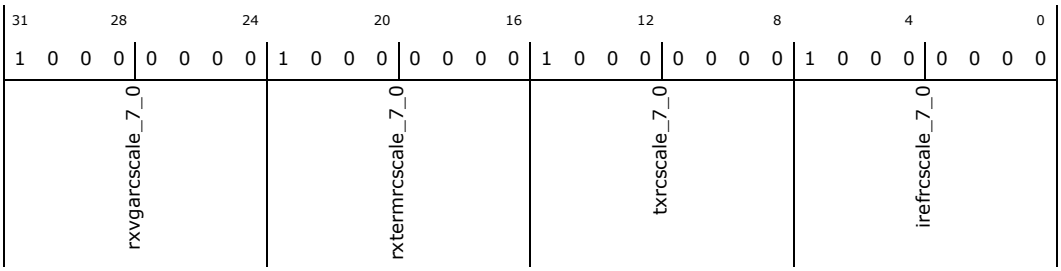
Type: Message Bus Register (Size: 32 bits)

pcs_dword21: [Port: 0xA6] + (800h + 54h)

Op Codes:

0h - Read, 1h - Write

Default: 80808080h



Bit Range	Default & Access	Description
31:24	80h RW	**rxvgarcscale_7_0:** Rx VGA Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxvgarccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
23:16	80h RW	**rxtermrcscale_7_0:** Rx Termination Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final rxtermrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
15:8	80h RW	**txrcscale_7_0:** Tx Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final txrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0
7:0	80h RW	**irefrcscale_7_0:** Iref Rcomp Scale Multiplier The LRC code is multiplied by this value before applying the offset to generate the final irefrccode. 0xFF: Scale=1.99219 0xC0: Scale=1.5 0x80: Scale=1.0 0x40: Scale=0.5 0x00: Scale=0

18.13.23 PCS_DWORD22 (pcs_dword22)—Offset 58h

Access Method

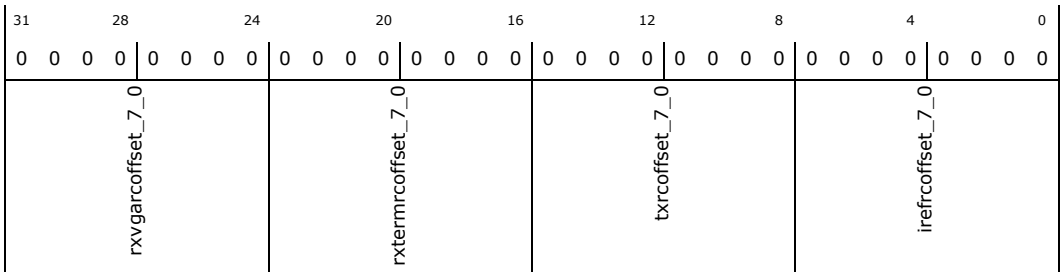
Type: Message Bus Register (Size: 32 bits)

pcs_dword22: [Port: 0xA6] + (800h + 58h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0h RW	**rxvgarcoffset_7_0:** Rx VGA Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxVGA Rcomp.
23:16	0h RW	**rxtermrcoffset_7_0:** Rx Termination Rcomp Offset Same description as IREF Rcomp Offset, but applies to RxTerm Rcomp.
15:8	0h RW	**txrcoffset_7_0:** Tx Rcomp Offset Same description as IREF Rcomp Offset, but applies to Tx Rcomp.
7:0	0h RW	**irefrcoffset_7_0:** Iref Rcomp Offset This value is added to the scaled LRC code to determine the final calibration code used by the Iref block. 2's complement format. The full 8-bit offset is used with the scale multiplier to determine the final 8-bit value, but the Iref target only uses the upper MSBs of the final value. 0x00: Offset = 0 0x01: Offset = +1 0x7F: Offset = +127 0xFF: Offset = -1 0x80: Offset = -128 Note: The final rcomp code has rollover protection so the final rcomp code + offset will not exceed the min/max range.

18.13.24 PCS_DWORD23 (pcs_dword23)—Offset 5Ch

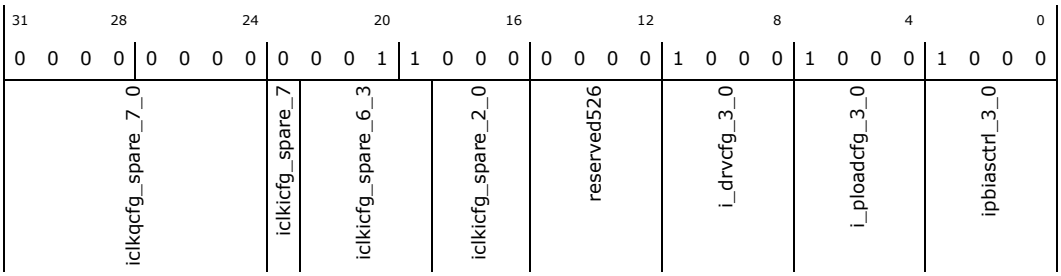
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword23: [Port: 0xA6] + (800h + 5Ch)

Op Codes:
0h - Read, 1h - Write

Default: 00180888h



Bit Range	Default & Access	Description
31:24	0h RW	**iclkqcfg_spare_7_0:** (Bonus bits for Data Lane Clk Distrubtion block)
23	0h RW	**iclkicfg_spare_7:** Repurposed for IREF backup mode in DL Select bit to enable diode based IREF in DL 0 - functional mode, use IREFGEN loop output 1 - bypass IREF loop, use diode connected PMOS output Ensure IREF loop amp is enabled by forcing reg_ivrefen and ivrefen_ovrd to 1
22:19	3h RW	**iclkicfg_spare_6_3:** TX MUX tail current strength setting
18:16	0h RW	**iclkicfg_spare_2_0:** CLK Distribution Monitor MUX Select
15:12	0h RW	**reserved526:** reserved
11:8	8h RW	**i_drvcfg_3_0:** CLK: Driver Tail Current Control
7:4	8h RW	**i_ploadcfg_3_0:** CLK: Pbias Ref Current Selection
3:0	8h RW	**ipbiasctrl_3_0:** CLK: Pmos-Load Pbias Voltage Control

18.13.25 PCS_DWORD24 (pcs_dword24)—Offset 60h

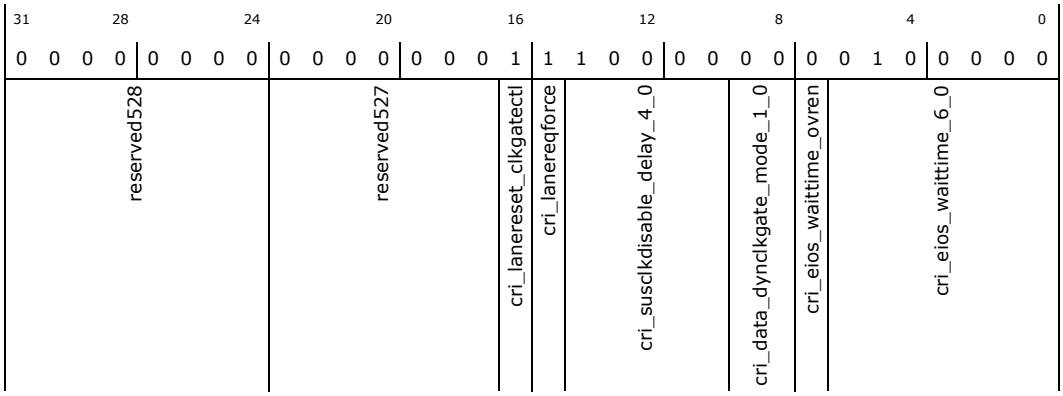
Access Method

Type: Message Bus Register (Size: 32 bits)

pcs_dword24: [Port: 0xA6] + (800h + 60h)

Op Codes:
0h - Read, 1h - Write

Default: 0001C020h



Bit Range	Default & Access	Description
31:24	0h RW	**reserved528:** reserved
23:17	0h RW	**reserved527:** reserved
16	1h RW	**cri_lanereset_clkgatectl:** 1: The assertion of lane reset will have the effect of gating the susclk and de-asserting the internal laneclkreq. This mode is only valid when the data lane dynamic clock gating mode is set to a non-zero value (that is, 01, 10, and 11). 0: The assertion of lane reset will have no effect on the gating of susclk and state of the internal laneclkreq signal.
15	1h RW	**cri_lanereqforce:** Controls whether the internal laneclkreq will be forced to 1 or 0 when cfg_data_dynclkgate_mode is set to 00 or 10. 1: force laneclkreq high 0: force laneclkreq low. This mode will likely be used when one of the lanes is disabled while other lanes in the family are enabled. In this case the internal laneclkreq of the disabled lane should be de-asserted (not influencing the clk gating decision)
14:10	10h RW	**cri_susclkdisable_delay_4_0:** This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the laneclkreq signal sent out of the datalane. The susclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 - 0 Cycle Delay 5'b00001 - 1 Cycle Delay 5'b00010 - 2 Cycle Delay ..... 5'b11110 - 30 Cycle Delay 5'b11111 - 31 Cycle Delay
9:8	0h RW	**cri_data_dynclkgate_mode_1_0:** Controls the dynamic clock gating behavior in the data lane. 00 - susclk gating and laneclkreq disabled (Forced to configured value). In this mode the susclk will not be gated under any circumstances and the laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 01 - susclk gating disabled, laneclkreq enabled . In this mode the susclk will not be gated under any circumstances. The laneclkreq sent out of the data lane will toggle based on whether the lane power state, susclk need and the previous lane's laneclkreq signal. 10 - susclk gating enabled, laneclkreq disabled (forced to configured value) - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the lane will be forced to a programmed value (can be forced high or low) 11 - susclk gating and laneclkreq enabled - In this mode the susclk will be gated during P2/Slumber when there are no requests to change the TX common mode. The laneclkreq sent out of the data lane will toggle based on the lane power state, susclk need and the previous lane's laneclkreq signal.
7	0h RW	**cri_eios_waittime_ovren:** EIOS Wait Time Override Enable for Rx Turn OFF 0: hardware value for EIOS wait timer is selected. 1: selects cri_eios_waittime[6:0]
6:0	20h RW	**cri_eios_waittime_6_0:** EIOS Wait Time for Rx Turn OFF Represents override value timer in PCS that comes into play during EIOS based turn off Rx (Rx L0s) 0000000 - Timer is bypassed 0000001 - 1 PLL link clock period delay (2ns) 0000010 - 2 PLL link clock period delay (4ns) ... 0100000 - 32 PLL link clock periods delay (64ns) - default

18.14 PCI Express* Lane 3 Electrical Address Map

Table 141. Summary of PCI Express* Lane 3 Electrical Message Bus Registers—0xA6 (Global Offset 880h)

Offset	Register ID—Description	Default Value
0h	"TX_DWORD0 (tx_dword0)—Offset 0h" on page 949	2600003Ah
4h	"TX_DWORD1 (tx_dword1)—Offset 4h" on page 950	20000000h
8h	"TX_DWORD2 (tx_dword2)—Offset 8h" on page 951	5580983Ah
Ch	"TX_DWORD3 (tx_dword3)—Offset Ch" on page 952	0C782040h
10h	"TX_DWORD4 (tx_dword4)—Offset 10h" on page 953	2B404D55h
14h	"TX_DWORD5 (tx_dword5)—Offset 14h" on page 954	00000000h
18h	"TX_DWORD6 (tx_dword6)—Offset 18h" on page 954	1F200000h
1Ch	"TX_DWORD7 (tx_dword7)—Offset 1Ch" on page 955	0038383Fh
20h	"TX_DWORD8 (tx_dword8)—Offset 20h" on page 956	0600AA80h
24h	"TX_DWORD9 (tx_dword9)—Offset 24h" on page 957	00430C06h
28h	"TX_DWORD10 (tx_dword10)—Offset 28h" on page 958	00000000h
2Ch	"TX_DWORD11 (tx_dword11)—Offset 2Ch" on page 959	00001000h
30h	"TX_DWORD12 (tx_dword12)—Offset 30h" on page 961	00000000h
34h	"TX_DWORD13 (tx_dword13)—Offset 34h" on page 962	00000000h
38h	"TX_DWORD14 (tx_dword14)—Offset 38h" on page 963	00400000h
3Ch	"TX_DWORD15 (tx_dword15)—Offset 3Ch" on page 964	00000000h
40h	"TX_DWORD16 (tx_dword16)—Offset 40h" on page 965	00008A00h

18.14.1 TX_DWORD0 (tx_dword0)—Offset 0h

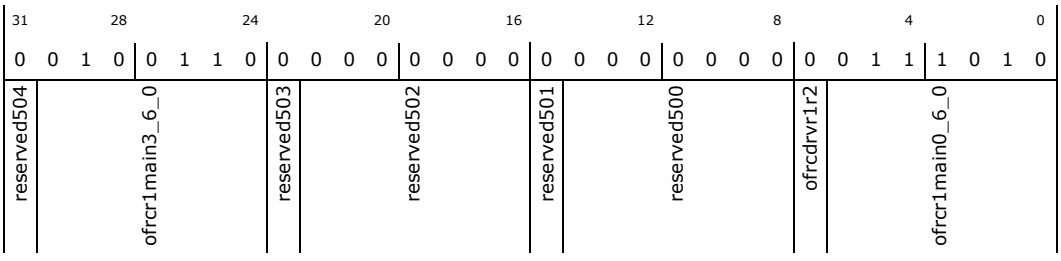
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword0: [Port: 0xA6] + (880h + 0h)

Op Codes:
0h - Read, 1h - Write

Default: 2600003Ah



Bit Range	Default & Access	Description
31	0h RO	**reserved504:** reserved

Bit Range	Default & Access	Description
30:24	26h RW	**ofrcr1main3_6_0:** number of slices in active R1 for swing 3 (DE)
23	0h RO	**reserved503:** reserved
22:16	0h RO	**reserved502:** reserved
15	0h RO	**reserved501:** reserved
14:8	0h RO	**reserved500:** reserved
7	0h RW	**ofrcdrvr1r2:** enable forcing number of used slices in all fir levels.
6:0	3Ah RW	**ofrcr1main0_6_0:** number of slices in active R1 for swing 0 (FS)

18.14.2 TX_DWORD1 (tx_dword1)—Offset 4h

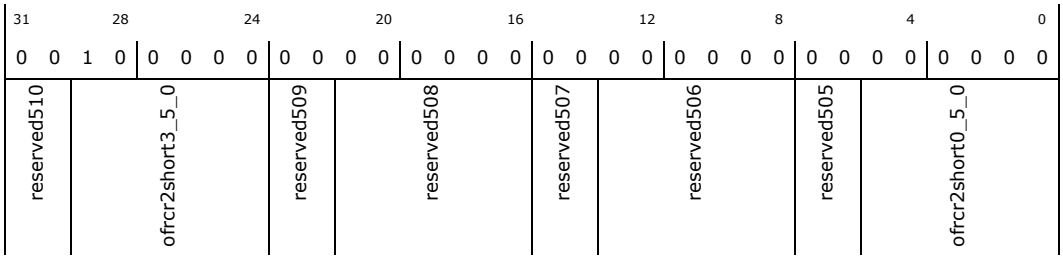
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword1: [Port: 0xA6] + (880h + 4h)

Op Codes:
0h - Read, 1h - Write

Default: 20000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved510:** reserved
29:24	20h RW	**ofrcr2short3_5_0:** number of slices in R2 for swing 3 (DE) MSB has no effect.
23:22	0h RO	**reserved509:** reserved
21:16	0h RO	**reserved508:** reserved
15:14	0h RO	**reserved507:** reserved
13:8	0h RO	**reserved506:** reserved

Bit Range	Default & Access	Description
7:6	0h RO	**reserved505:** reserved
5:0	0h RW	**ofrcr2short0_5_0:** number of slices in R2 for swing 0 (FS) MSB has no effect.

18.14.3 TX_DWORD2 (tx_dword2)—Offset 8h

Access Method

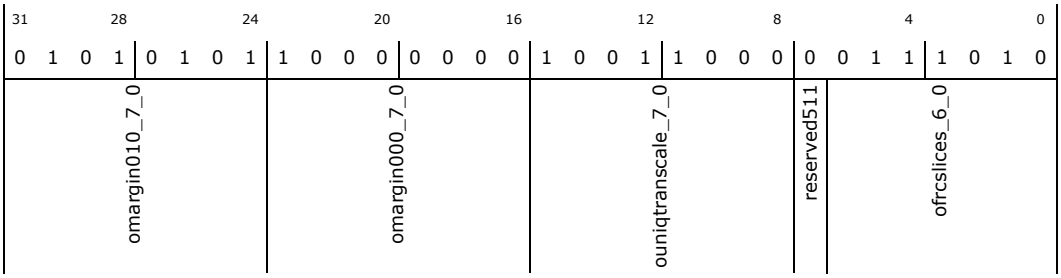
Type: Message Bus Register (Size: 32 bits)

tx_dword2: [Port: 0xA6] + (880h + 8h)

Op Codes:

0h - Read, 1h - Write

Default: 5580983Ah



Bit Range	Default & Access	Description
31:24	55h RW	**omargin010_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~2/3Vp2p
23:16	80h RW	**omargin000_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p. To be used in Gen2 mode (Gen1/Gen2 depend on datarategit and downscaleamp register)
15:8	98h RW	**ouniqtranscale_7_0:** scales the number of slices defined the ref circuit (or R-comp circuit) by factor of ouniqtranscale[7:0]/128 The scaled amount of slices might be used in the full-swing Uis according to ouniqetrangenmethod[1:0] The scaled amount of slices might be used in the full-swing Uis according to oscaledcompmethod[1:0]
7	0h RO	**reserved511:** reserved
6:0	3Ah RW	**ofrcslices_6_0:** number of used slices if forced Used in compensated GPIO mode

18.14.4 TX_DWORD3 (tx_dword3)—Offset Ch

Access Method

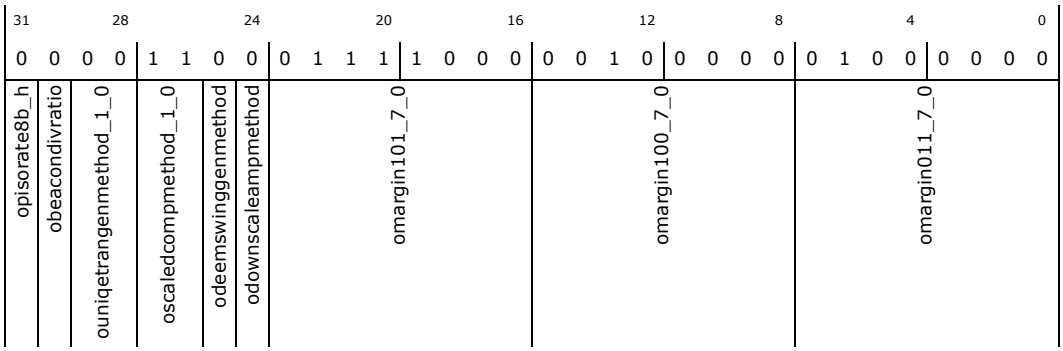
Type: Message Bus Register (Size: 32 bits)

tx_dword3: [Port: 0xA6] + (880h + Ch)

Op Codes:

0h - Read, 1h - Write

Default: 0C782040h



Bit Range	Default & Access	Description
31	0h RW	**opisorate8b_h:** if '0' the PISO is of 10 bits (the whole bus) if '1' the PISO is of 8 bits (The LSBs) It's relevant both in normal Tx and in loopback mode. Use: '1' in PCI-E gen 3 and CIO (if supported) '0' for all other interfaces
30	0h RW	**obeacondivratio:** Div ration of beacon signal from ick_suslow clock '0' - Beacon freq will be as sus clock freq '1' - Beacon freq will be 1/4 of sus clock freq (note LFPS spec is 10-50MHz)
29:28	0h RW	**ouniqetrangenmethod_1_0:** Used to define if we use uniq-transition-bit scaling or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't activate uniq-transition-bit When '01' - if fast-clock is not divided (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. When '10' - if fast-clock is not divided or divided by 2 (gen2?) activate uniq-transition-bit otherwise (gen1?) don't. (will probably be down-scaling amount of slices) When '11' - activate uniq-transition-bit
27:26	3h RW	**oscaledcompmethod_1_0:** Used to define if we use scaling of the compansation values or not. The purpose is to have gen dependant scaling / non-scaling When '00' - don't used scaled comp When '01' - if fast-clock is not divided (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp When '10' - if fast-clock is not divided or divided by 2 (gen2?) don't scale-comp otherwise (gen1?) use scaled-comp (will probably be down-scaling amount of slices) When '11' - if fast-clock is not divided (gen2?) use scaled-comp otherwise (gen1?) don't use scaled-comp (will probably be up-scaling amount of slices)
25	0h RW	**odeemswinggenmethod:** Used to select scaling of -3.5dB deemphasis either ow2tapgen1deemph3p5[7:0] or ow2tapgen2deemph3p5[7:0] When '0' - if fast-clock is not divided use gen2 otherwise use gen1 When '1' - if fast-clock is not divided or divided by 2 use gen2 otherwise use gen1
24	0h RW	**odownscaleampmethod:** when margin='001', this bit with dataratefit are used to select between margin000 (for gen2) and margin101 (for gen1) when '0' - if fast-clock is not divided use margin000 (gen2) otherwise use margin101 (gen1) when '1' - if fast-clock is not divided or divided by 2 use margin000 (gen2) otherwise use margin101 (gen1)
23:16	78h RW	**omargin101_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1V p2p to be used in Gen1 mode (Gen1/Gen2 depends on dataratefit and downscaleamp register)
15:8	20h RW	**omargin100_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/4Vp2p

Bit Range	Default & Access	Description
7:0	40h RW	**omargin011_7_0:** factor (X/128) of slices to use in main-R1 for full swing level. Used for ~1/2Vp2p

18.14.5 TX_DWORD4 (tx_dword4)—Offset 10h

Access Method

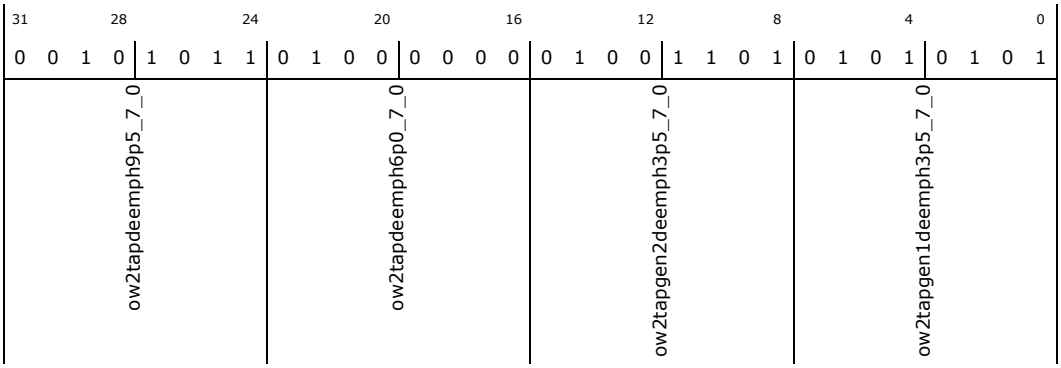
Type: Message Bus Register (Size: 32 bits)

tx_dword4: [Port: 0xA6] + (880h + 10h)

Op Codes:

0h - Read, 1h - Write

Default: 2B404D55h



Bit Range	Default & Access	Description
31:24	2Bh RW	**ow2tapdeemph9p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 9.5dB deemphais
23:16	40h RW	**ow2tapdeemph6p0_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 6.0dB deemphais
15:8	4Dh RW	**ow2tapgen2deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais
7:0	55h RW	**ow2tapgen1deemph3p5_7_0:** factor (X/128) of slices to use in main-R1 out of the slices in main-R1 in full-swing. Normally - in order to have 3.5dB deemphais

18.14.6 TX_DWORD5 (tx_dword5)—Offset 14h

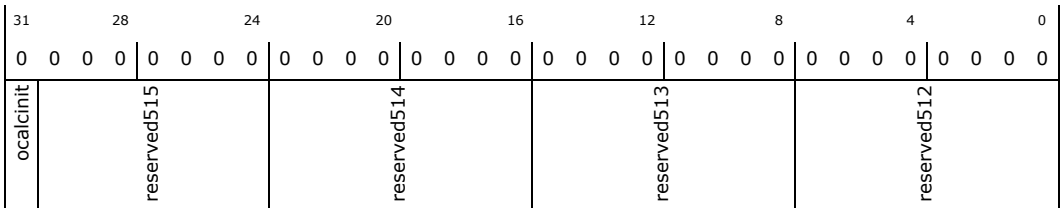
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword5: [Port: 0xA6] + (880h + 14h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31	0h RW	**ocalcinit:** initiate calculation of swing-cotrol circuit. rewrite to '0' and '1' to reinitiate the calculation
30:24	0h RO	**reserved515:** reserved
23:16	0h RO	**reserved514:** reserved
15:8	0h RO	**reserved513:** reserved
7:0	0h RO	**reserved512:** reserved

18.14.7 TX_DWORD6 (tx_dword6)—Offset 18h

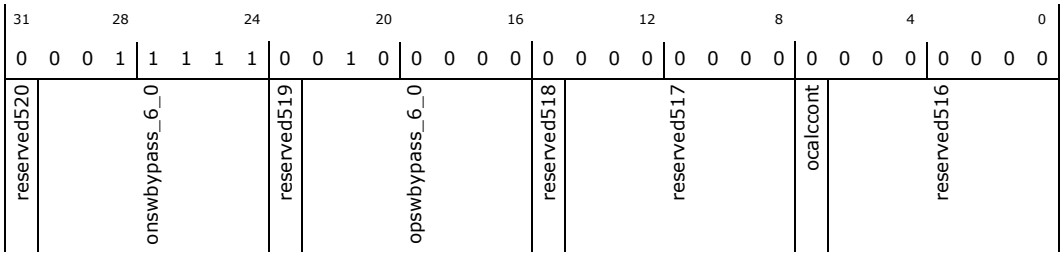
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword6: [Port: 0xA6] + (880h + 18h)

Op Codes:
0h - Read, 1h - Write

Default: 1F200000h



Bit Range	Default & Access	Description
31	0h RO	**reserved520:** reserved

Bit Range	Default & Access	Description
30:24	1Fh RW	**onswbypass_6_0:** Determines # of slices activated in N-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) same slices canot be opend for P-drv and for N-drv. Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted. In these DFT modes pswpass can be set to the same value as nswbypass
23	0h RO	**reserved519:** reserved
22:16	20h RW	**opswbypass_6_0:** Determines # of slices activated in P-drv when in strong pulling to CM (after Rx-dtct/ gohighz / stongPD) Determines # of slices for P-drv in All1/All0 DFTs when bypbycomp is not asserted.
15	0h RO	**reserved518:** reserved
14:8	0h RO	**reserved517:** reserved
7	0h RW	**ocalccont:** initiate calculation of swing-cotrol circuit. While this signal is '1' the calculation is beeing done consecutively
6:0	0h RO	**reserved516:** reserved

18.14.8 TX_DWORD7 (tx_dword7)—Offset 1Ch

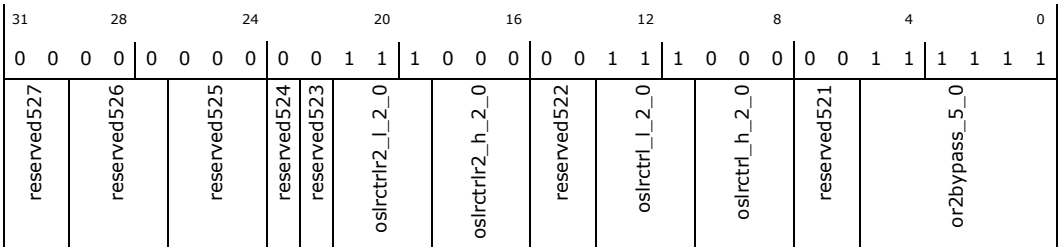
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword7: [Port: 0xA6] + (880h + 1Ch)

Op Codes:
0h - Read, 1h - Write

Default: 0038383Fh



Bit Range	Default & Access	Description
31:30	0h RO	**reserved527:** reserved
29:27	0h RO	**reserved526:** reserved
26:24	0h RO	**reserved525:** reserved
23	0h RO	**reserved524:** reserved
22	0h RO	**reserved523:** reserved

Bit Range	Default & Access	Description
21:19	7h RW	**oslrctrlr2_l_2_0:** Slew rate trimming of driver in R2 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
18:16	0h RW	**oslrctrlr2_h_2_0:** Slew rate trimming of driver in R2 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
15:14	0h RO	**reserved522:** reserved
13:11	7h RW	**oslrctrl_l_2_0:** Slew rate trimming of driver in R1 resistor for gen1. '000' - disabled '001' - slowest '111' - fastest
10:8	0h RW	**oslrctrl_h_2_0:** Slew rate trimming of driver in R1 resistor for gen1 '111' - disabled (emulates suspend mode) '110' - slowest '000' - fastest
7:6	0h RO	**reserved521:** reserved
5:0	3Fh RW	**or2bypass_5_0:** Number of open R2s in normal EI (electrical idle) Used in DFTs with other values (leg connectivity scan all power of 2s) read also notes on obypbycomp. MSB has no effect.

18.14.9 TX_DWORD8 (tx_dword8)—Offset 20h

Access Method

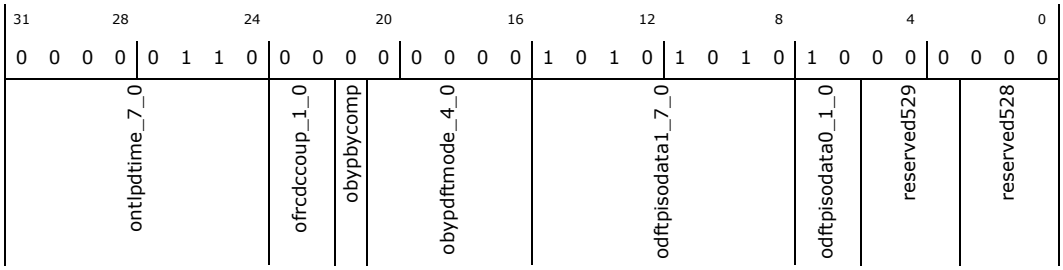
Type: Message Bus Register (Size: 32 bits)

tx_dword8: [Port: 0xA6] + (880h + 20h)

Op Codes:

0h - Read, 1h - Write

Default: 0600AA80h



Bit Range	Default & Access	Description
31:24	6h RW	**ontlpdtime_7_0:** [after step 1 of pullup] time (ick_susslow cycles) to wait (step 2) and let the pads leak downwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.
23:22	0h RW	**ofrcdccoup_1_0:** 00
21	0h RW	**obypbycomp:** 0' the amount of slices used in dftbypmode is by 'nswbypass', 'pswbypass' and 'r2bypass' registers '1' the amount of slices used is by 'slices' from swing-control block. Number of slices in R2 in EI - is also affected by this bit
20:16	0h RW	**obypdftmode_4_0:** selects the DFT mode. 5'h00 - DFT_OFF 5'h01 - DFTHIZ 5'h02 - DFTEI 5'h03 - DFTFELB 5'h04 - DFTALL1DIF 5'h05 - DFTALL0DIF 5'h06 - DFTALL1SE 5'h07 - DFTALL0SE 5'h08 - DFTDAC 5'h09 - DFTFRCBEAC 5'h0a - DFTOBS 5'h0c - DFT ASYNC MODE OFF 5'h0d - DFT ASYNC MODE Tx (output) 5'h0e - DFT ASYNC MODE Rx (input) 5'h0f - DFT ASYNC MODE Both (inout) 5'h10 - DFTPISOLOAD 5'h12 - DFTEISTRNG

Bit Range	Default & Access	Description
15:8	AAh RW	**odftpisodata1_7_0:** 8 MSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
7:6	2h RW	**odftpisodata0_1_0:** 2 LSB of alternative data input to PISO Load of this data is enabled when bypdftmode=DFTPISOLOAD
5:3	0h RO	**reserved529:** reserved
2:0	0h RO	**reserved528:** reserved

18.14.10 TX_DWORD9 (tx_dword9)—Offset 24h

Access Method

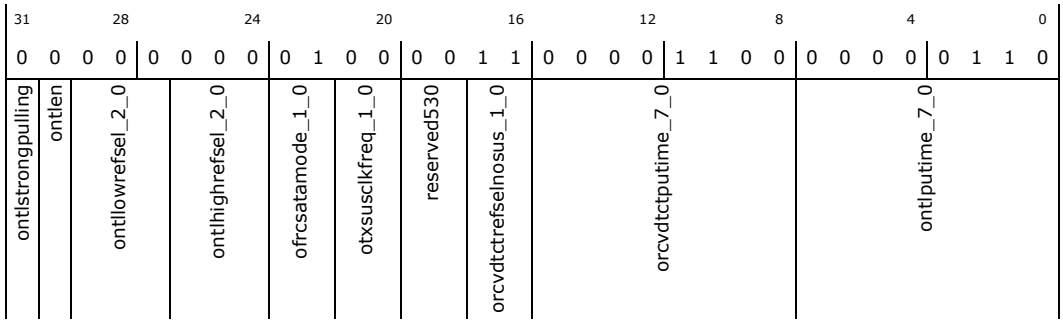
Type: Message Bus Register (Size: 32 bits)

tx_dword9: [Port: 0xA6] + (880h + 24h)

Op Codes:

0h - Read, 1h - Write

Default: 00430C06h



Bit Range	Default & Access	Description
31	0h RW	**ontlstrongpulling:** Make the NTL pulling resistors with stronger pulling. It will be required if leakage will be higher than expected
30	0h RW	**ontlen:** No-touch-leakage test enable
29:27	0h RW	**ontllowrefsel_2_0:** Selects reference voltage for use when pads where pulled-down and were left to leak upwards
26:24	0h RW	**ontlhighrefsel_2_0:** Selects reference voltage for use when pads where pulled-up and were left to leak downwards
23:22	1h RW	**ofrcsatamode_1_0:** 00
21:20	0h RW	**otxsusclkfreq_1_0:** Determines the clock frequency expected on ick_susslow clock pin. 00: in the range of 25MHz to 27MHz (default) 01: in the range of 25MHz - 62.5MHz 10: in the range of 37.5MHz - 100MHz 11: in the range of 62.5MHz - 125MHz
19:18	0h RO	**reserved530:** reserved
17:16	3h RW	**orcvdtctrefselnosus_1_0:** 2-LSBs of reference level for receive detect comparator to be used when core supply is active

Bit Range	Default & Access	Description
15:8	Ch RW	**orcvdtctputime_7_0:** Time (ick_susslow cycles) to wait (a.k.a. step 2) before comparing pads to Vref to detemine if there is a receiver on the far end. Value should be by the following Table: Sus-clock rate P1269.8 P1271.x 25MHz - 27MHz 9 12 25MHz - 62.5MHz 35 43 37.5MHz - 100MHz 64 76 62.5MHz - 125MHz 83 98
7:0	6h RW	**ontlputime_7_0:** [after step 1 of pulldown] time (ick_susslow cycles) to wait (step 2) and let the pads leak upwards before comparing pads to Vref to detemine if the pad exceeded Vref as a result of leakage.

18.14.11 TX_DWORD10 (tx_dword10)—Offset 28h

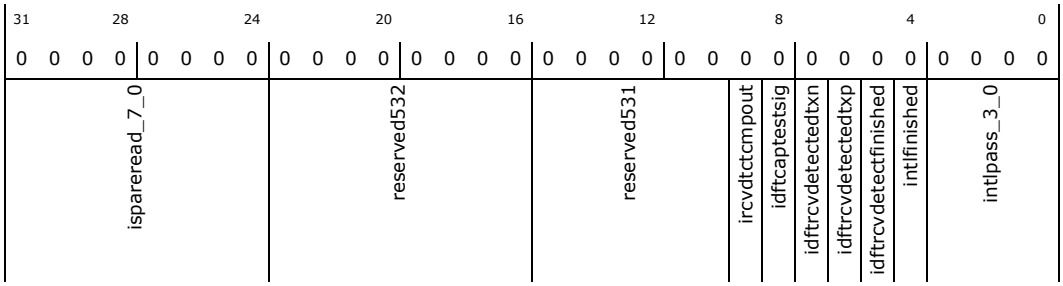
Access Method

Type: Message Bus Register (Size: 32 bits)

tx_dword10: [Port: 0xA6] + (880h + 28h)

Op Codes:
0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:24	X RO	**ispareread_7_0:** spare reg read
23:16	0h RO	**reserved532:** reserved
15:10	0h RO	**reserved531:** reserved
9	0h RO	**ircvdtctcmpout:** Flash Comparator Output Value
8	X RO	**idftcaptestsig:** reserved
7	0h RO	**idftrcvdetectedtxn:** Receive Detect Result for Txn
6	0h RO	**idftrcvdetectedtxp:** Receive Detect Result for Txp
5	0h RO	**idftrcvdetectfinished:** Receive Detect Process status
4	X RO	**intlfinished:** indication of NTL finished
3:0	X RO	**intlpass_3_0:** the four outputs of NTL test

18.14.12 TX_DWORD11 (tx_dword11)—Offset 2Ch

Access Method

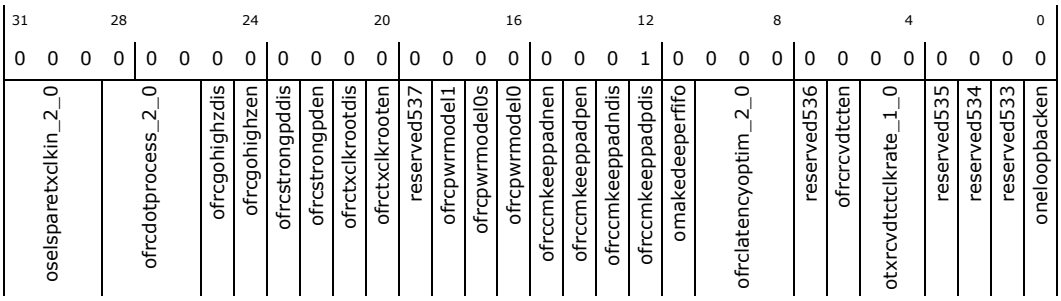
Type: Message Bus Register (Size: 32 bits)

tx_dword11: [Port: 0xA6] + (880h + 2Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00001000h



Bit Range	Default & Access	Description
31:29	0h RW	**oselsparetxclkin_2_0:** Selects data to be used as alternative to fast clock. 000: DAC clock if in DAC mode - Default. 001: cri100m clock 010: i_obsontx_psg 011: i_obsontx_nsg 100: ick_txsymbclk 101: icksusslow 110: ick_dac 111: spare
28:26	0h RW	**ofrcdotprocess_2_0:** forces the dotprocess information 0XX - information of dot process comes from i_dotprocess[1:0] input bus. 100: p1271 dot1 101: p1271 dot4 110: p1271 dot8 111: NA
25	0h RW	**ofrcgohighzdis:** forces disabling of high-z output
24	0h RW	**ofrcgohighzen:** forces enabing of high-z output
23	0h RW	**ofrcstrongpddis:** forces disabling of strong pull-down
22	0h RW	**ofrcstrongpden:** forces enabing of strong pull-down
21	0h RW	**ofrctxclkrootdis:** forces disable of tx-clock output.
20	0h RW	**ofrctxclkrooten:** forces tx-clock to operate and drive clock out.
19	0h RO	**reserved537:** reserved
18	0h RW	**ofrcpwrmodel1:** when aserted. Forces L1 state
17	0h RW	**ofrcpwrmodel0s:** when aserted. Forces L0s state
16	0h RW	**ofrcpwrmodel0:** when aserted. Forces L0 state
15	0h RW	**ofrccmkeeppadnen:** Forces enabling of common-mode keeping of PadN

Bit Range	Default & Access	Description
14	0h RW	**ofrccmkeeppadpen:** Forces enabling of common-mode keeping of PadP
13	0h RW	**ofrccmkeeppadndis:** Forces disabling of common-mode keeping of PadN
12	1h RW	**ofrccmkeeppadpdis:** Forces disabling of common-mode keeping of PadP
11	0h RW	**omakedeeperfifo:** Make FIFO deeper by 1 symbol clock cycle. Still not implemented. Implementation costs 10 flops in symb clock domain. Implementation is required for 8bits PISO only which is in next phase of products.
10:8	0h RW	**ofrclatencyoptim_2_0:** Changes the latency from loadgenen assertion to the sampling of 10bits data into fast-clock domain. The latency is determined by Fuses (through i_latencyoptim[1:0]) + ... 0XX =) + 0 (Not changing the latency.) 100 =) - 4UI 101 =) - 2UI 110 =) + 2UI 111 =) + 4UI Important Note: When changing the latency too high or too low is will wrap-around what might cause data loss on beginning or end of transmitting. If you decide to plan with the latency consider changing 'omakedeeperfifo' too
7	0h RO	**reserved536:** reserved
6	0h RW	**ofrcrcvdtcten:** force initiation of Tx-detect-Rx procedure
5:4	0h RW	**otxrcvdtctclkrate_1_0:** determines the clock rate in the flash comparator. 00 - use sus-clock as is (25MHz in phase2) default 01 - use sus-clock by 4 10 - use sus-clock by 2 11 - reserved In phase1 the rate was 2'b10 susfreq125MHz
3	0h RO	**reserved535:** reserved
2	0h RO	**reserved534:** reserved
1	0h RO	**reserved533:** reserved
0	0h RW	**oneloopbacken:** Near-End LoopBack enable

18.14.13 TX_DWORD12 (tx_dword12)—Offset 30h

Access Method

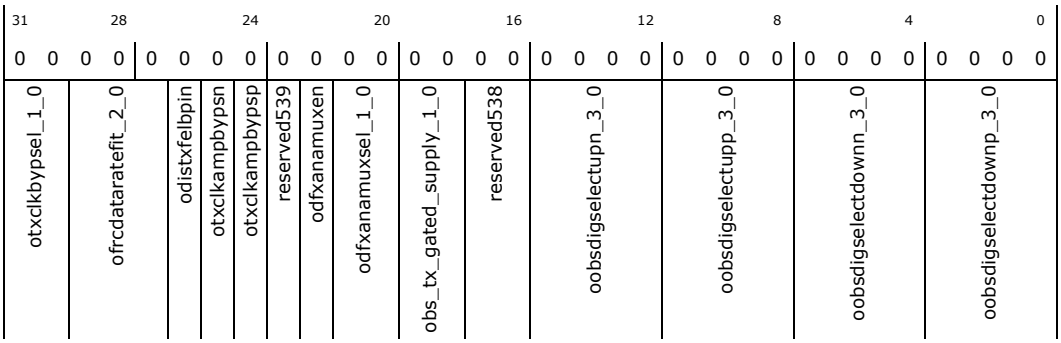
Type: Message Bus Register (Size: 32 bits)

tx_dword12: [Port: 0xA6] + (880h + 30h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RW	**otxclkbypsel_1_0:** Select if to bypass the divided normal clock with some other clock. 2'b00: Don't bypass. Regular clock. 2'b01: bypass the RX clock - dataratefit must be '11' 2'b10: Reserved 2'b11: bypass the sparetxclk clock - dataratefit must be '11'
29:27	0h RW	**ofrcdataratefit_2_0:** Forces TX data rate 3'b0XX - don't force a velue. get it from the I/F pin 3'b100 - no divide (2UIs per clock cyc) 3'b101 - divide by 2 3'b110 - divide by 4 3'b111 - divide by 8 - used also for bypassing with other clocks
26	0h RW	**odistxfelbpin:** when asserted - disables the i_txfelben pin at the interface and force it 0. (needed in case the pin is asserted in KX or sata1 mode)
25	0h RW	**otxclkampbypsn:** 0': Normal operation '1': Enable of the passgate connected from the analog clock N to the control of the DC correction cell. The feedback OTA is disabled.
24	0h RW	**otxclkampbypsp:** 0': Normal operation '1': Enable of the passgate connected from the analog clock P to the control of the DC correction cell. The feedback OTA is disabled.
23	0h RO	**reserved539:** reserved
22	0h RW	**odfxanamuxen:** Enables analog signals probing mux out. When enabled the Vref of Tx-detect-Rx circuit is observed. Note that only one lane is allowed to have a the analog mux enabled to avoid collisions.
21:20	0h RW	**odfxanamuxsel_1_0:** selects analog signal to be sent to analog port in common lane. This bus has no affect at all currently because there is only one analog signal for observation which is observed by odfxanamuxen
19:18	0h RW	**obs_tx_gated_supply_1_0:** Monitor gated vcc supply to Tx upar
17:16	0h RO	**reserved538:** reserved
15:12	0h RW	**oobsdigselectupn_3_0:** selects data to be sent to observability port output 'o_obsup_nsg'. Same mapping as oobsdigselectdownn[3:0]
11:8	0h RW	**oobsdigselectupp_3_0:** selects data to be sent to observability port output 'o_obsup_psg'. Same mapping as oobsdigselectdownp[3:0]

Bit Range	Default & Access	Description
7:4	0h RW	**oobsdigselectdownn_3_0:** Reserved.
3:0	0h RW	**oobsdigselectdownp_3_0:** Reserved.

18.14.14 TX_DWORD13 (tx_dword13)—Offset 34h

Access Method

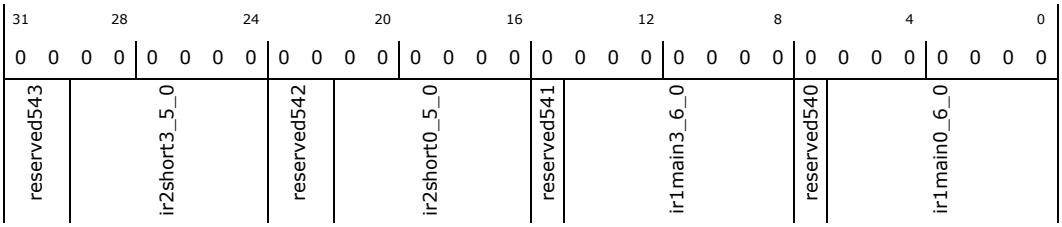
Type: Message Bus Register (Size: 32 bits)

tx_dword13: [Port: 0xA6] + (880h + 34h)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved543:** reserved
29:24	X RO	**ir2short3_5_0:** The slices used in R2 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
23:22	0h RO	**reserved542:** reserved
21:16	X RO	**ir2short0_5_0:** The slices used in R2 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)
15	0h RO	**reserved541:** reserved
14:8	X RO	**ir1main3_6_0:** The slices used in R1 for DE (sub-DE in 3tap FIR) (PstC=Y,C=Y,PreC=Y)
7	0h RO	**reserved540:** reserved
6:0	X RO	**ir1main0_6_0:** The slices used in R1 for FS (sub-FS in 3tap FIR) (PstC=Y,C=Y,PreC=X)

18.14.15 TX_DWORD14 (tx_dword14)—Offset 38h

Access Method

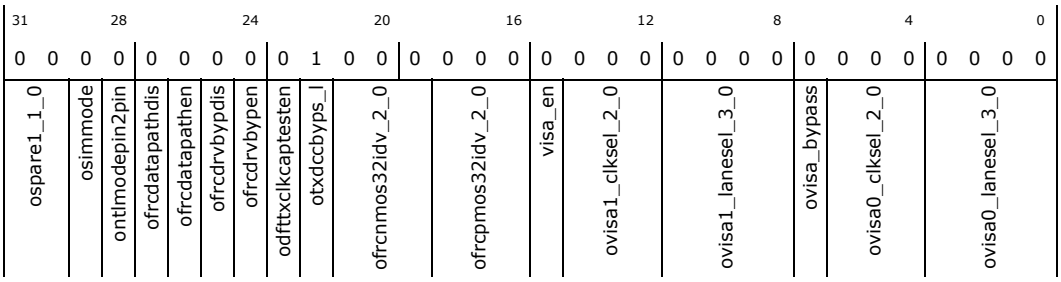
Type: Message Bus Register (Size: 32 bits)

tx_dword14: [Port: 0xA6] + (880h + 38h)

Op Codes:

0h - Read, 1h - Write

Default: 00400000h



Bit Range	Default & Access	Description
31:30	0h RW	**ospare1_1_0:** reserved
29	0h RW	**osimmode:** Counter threshold of receive-detect, NTL, strong-common-mode is shortened dramatically for fast simulation porpuses. (does not impose risk to circuitly but electrical spec will not met)
28	0h RW	**ontlmodepin2pin:** 0 - NTL procedure will be done per pad while both pads are pulled to the same rail. 1 - NTL procedure will be done per pad while the pads are pulled to opposite rails.
27	0h RW	**ofrcdatapathdis:** DFT feature to optionaly be used with other registers
26	0h RW	**ofrcdatapathen:** DFT feature to optionaly be used with other registers
25	0h RW	**ofrcdrvbypdis:** DFT feature to optionaly be used with other registers
24	0h RW	**ofrcdrvbypen:** DFT feature to optionaly be used with other registers
23	0h RW	**odfttxclkcaptesten:** Enables the finger capacitor quality check in the DCC block in Tx-clock block. The test is for shorts between the capacitor terminals.
22	1h RW	**otxdccbyps_l:** Tx DCC Bypass Override Puts DCC (duty cycle correction) circuit in bypass mode 0 - clock's duty cycle is not fixed
21:19	0h RW	**ofrcnmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
18:16	0h RW	**ofrcpmos32idv_2_0:** change the value iabut_idvpmos32_h[1:0] pushes to txclk 3'b0?? - don't affect the idv comp 3'b100 - pull the idv information to be always at slow 3'b101 - pull the idv information a bit slower. 3'b110 - pull the idv information a bit faster. 3'b111 - pull the idv information to be always at fast
15	0h RW	**visa_en:** VISA Enable for the Tx VISA logic
14:12	0h RW	**ovisa1_clksel_2_0:** VISA Clock Select for Lane1. Selects the source synchronous clock to be used for data being sent on lane1.

Bit Range	Default & Access	Description
11:8	0h RW	**ovisa1_lanesel_3_0:** VISA Lane Select for Lane1. Selects the byte of data to be sent out on lane1.
7	0h RW	**ovisa_bypass:** VISA Bypass. Allows for signals to be passed asynchronously through VISA block. Applies to both lane0 and lane1. 0 : Flop signals in local VISA block (default) 1 : Bypass flops in local VISA block
6:4	0h RW	**ovisa0_clksel_2_0:** VISA Clock Select for Lane0. Selects the source synchronous clock to be used for data being sent on lane0.
3:0	0h RW	**ovisa0_lanesel_3_0:** VISA Lane Select for Lane0. Selects data byte to be driven out of VISA-0 byte. Can be either clocked or unclocked data

18.14.16 TX_DWORD15 (tx_dword15)—Offset 3Ch

Access Method

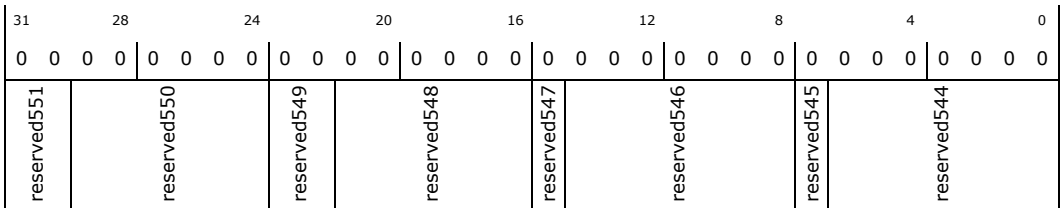
Type: Message Bus Register (Size: 32 bits)

tx_dword15: [Port: 0xA6] + (880h + 3Ch)

Op Codes:

0h - Read, 1h - Write

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0h RO	**reserved551:** reserved
29:24	0h RO	**reserved550:** The slices used in R2 for DE (PstC=X,C=Y,PreC=Y)
23:22	0h RO	**reserved549:** reserved
21:16	0h RO	**reserved548:** The slices used in R2 for FS (PstC=X,C=Y,PreC=X)
15	0h RO	**reserved547:** reserved
14:8	0h RO	**reserved546:** The slices used in R1 for DE (PstC=X,C=Y,PreC=Y)
7	0h RO	**reserved545:** reserved
6:0	0h RO	**reserved544:** The slices used in R1 for FS (PstC=X,C=Y,PreC=X)

18.14.17 TX_DWORD16 (tx_dword16)—Offset 40h

Access Method

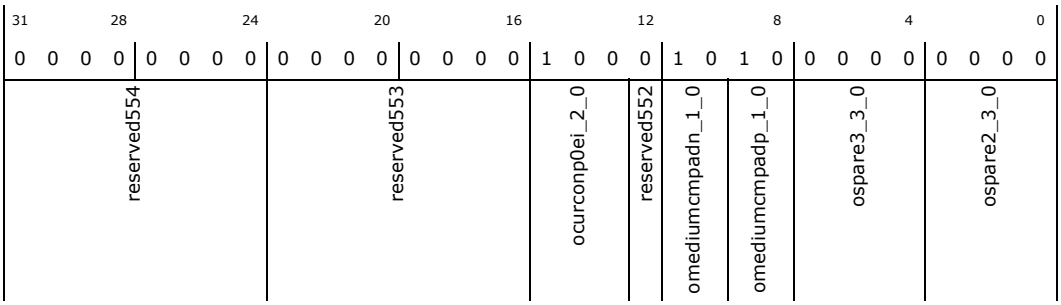
Type: Message Bus Register (Size: 32 bits)

tx_dword16: [Port: 0xA6] + (880h + 40h)

Op Codes:

0h - Read, 1h - Write

Default: 00008A00h



Bit Range	Default & Access	Description
31:24	0h RO	**reserved554:** reserved
23:16	0h RO	**reserved553:** reserved
15:13	4h RW	**ocurconp0ei_2_0:** current consumed (typically) 00X - 0.0mA - not active 01X - 0.9mA 10X - 1.8mA 11X - 2.7mA
12	0h RO	**reserved552:** reserved
11:10	2h RW	**omediumcmpadn_1_0:** During P0-EI pad-N will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 -9.73mA
9:8	2h RW	**omediumcmpadp_1_0:** During P0-EI pad-P will be on medium strength CM and will cause the following current consumption: 00 - 0.00mA (disable) 01 - 2.45mA 10 - 4.87mA 11 - 9.73mA
7:4	0h RW	**ospare3_3_0:** 4 spare CRI register bits
3:0	0h RW	**ospare2_3_0:** 4 spare CRI register bits

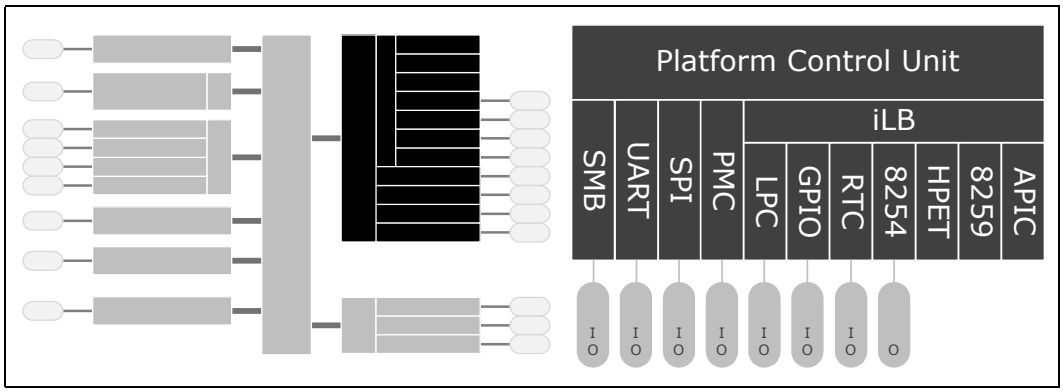
§ §

19 Platform Controller Unit (PCU) Overview

The Platform Controller Unit (PCU) is a collection of hardware blocks that are critical for implementing a Windows* compatible platform. These hardware blocks include:

- PCU – Power Management Controller (PMC)
- PCU – Serial Peripheral Interface (SPI)
  - For boot FW and system configuration data Flash storage
- PCU – Universal Asynchronous Receiver/Transmitter (UART)
- PCU – Intel® Legacy Block (iLB) Overview

The PCU also implements some high level configuration features for BIOS/EFI boot.

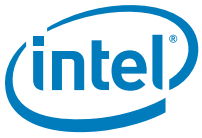


19.1 Features

- The key features of the individual blocks are as follows: SMBus Host Controller
  - Supports System Management Bus (SMBus) 2.0 Specification
  - No support for SMBus Slave functionality aside from the Host Notify Command

No TCO (Total Cost of Ownership) feature support

- Universal Asynchronous Receiver/Transmitter (UART)
  - 16550 controller compliant
  - Reduced Signal Count: TX and RX only
  - COM1 interface
- Serial Peripheral Interface (SPI)
  - For one or two SPI Flash, of up to 16MB size each, only. No other SPI peripherals are supported.
  - Stores boot FW and system configuration data
  - Supports frequencies of 20 MHz, 33MHz and 50MHz.



- Power Management Controller (PMC)
  — Controls many of the power management features present in the processor.
- Intel Legacy Block (iLB)
  — Supports legacy PC platform features
  — Sub-blocks include LPC, GPIO, 8259 PIC, IO-APIC, 8254 timers, HPET timers and the RTC.

19.1.1 BIOS/EFI Top Swap

While updating the BIOS/EFI boot sector in flash, unexpected system power loss can cause an incomplete write resulting in a corrupt boot sector. For this reason, two boot sectors are stored in the flash.

The location of the secondary boot sector is defined by inverting one of the bits of the address (A16, A17 or A18) that the CPU core will attempt to fetch code from. This address bit will vary depending on the size of the boot block. Refer to the GCS.BBSize register bit definition for further details.

Prior to starting writes to the primary BIOS/EFI boot sector, the Top-Swap indicator is set. From this point onwards, the secondary boot sector will be used. Only after successful completion of the primary boot sector write should the Top-Swap indicator be cleared and the primary boot sector be used again.

There are two methods that can be used to implement the Top-Swap indicator.

19.1.1.1 BIOS/EFI Controlled

BIOS/EFI can use the GCS.TS register bit to set the Top-Swap indicator. The GCS.TS bit is stored in the RTC well and, therefore, keeps its value even when the system is powered down.

Note: Writes to GCS.TS will be unsuccessful if the GCS.BILD bit has been set.

19.1.1.2 Hardware Controlled

System hardware, external to the processor, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

Note: The Top-Swap strap, when asserted at power-up, forces Top-Swap to be active even if GCS.TS bit is cleared but doesn't change the GCS.TS bit itself. The GCS.TS bit can not be changed if Top-Swap pin strap was sampled as being asserted until the next power-up when Top-Swap is sampled as being de-asserted.

19.1.2 BIOS/EFI Boot Strap

BIOS/EFI may be booted from the PCU SPI interface or the iLB's LPC interface. The choice of SPI or LPC is configured by the BIOS/EFI Boot Strap (BBS). The possible configurations of the BBS are indicated in Table 142.

Note: The BBS is multiplexed with the GPIO_S0_SC[63] signal.

Note: BIOS/EFI boot from the LPC interface is not available when Secure Boot is enabled.

Table 142. BBS Configurations

BBS Level	Description
Low (0b)	Boot from LPC
High (1b)	Boot from SPI

19.2 PCU iLB LPC Port 80h I/O Registers

Table 143. Summary of PCU iLB LPC Port 80h I/O Registers—

Offset	Size	Register ID—Description	Default Value
80h	1	"PC80—Offset 80h" on page 969	00h
81h	1	"PC81—Offset 81h" on page 970	00h
82h	1	"PC82—Offset 82h" on page 970	00h
83h	1	"PC83—Offset 83h" on page 971	00h
84h	1	"PC84—Offset 84h" on page 971	00h
85h	1	"PC85—Offset 85h" on page 972	00h
86h	1	"PC86—Offset 86h" on page 972	00h
87h	1	"PC87—Offset 87h" on page 973	00h
88h	1	"PC88—Offset 88h" on page 973	00h
89h	1	"PC89—Offset 89h" on page 974	00h
8Ah	1	"PC8A—Offset 8Ah" on page 974	00h
8Bh	1	"PC8B—Offset 8Bh" on page 975	00h
8Ch	1	"PC8C—Offset 8Ch" on page 975	00h
8Dh	1	"PC8D—Offset 8Dh" on page 976	00h
8Eh	1	"PC8E—Offset 8Eh" on page 976	00h
8Fh	1	"PC8F—Offset 8Fh" on page 977	00h

19.2.1 PC80—Offset 80h

Post Code 80 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC80: 80h

Default: 00h

Bit Range	Default & Access	Description
7:0	0h RW	**PC80REG:** Post Code 80 register

19.2.2 PC81—Offset 81h

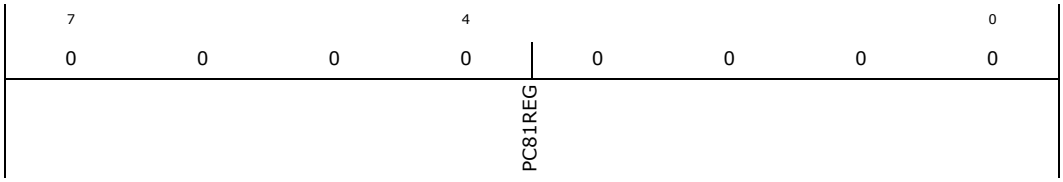
Post Code 81 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC81: 81h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC81REG:** Post Code 81 register

19.2.3 PC82—Offset 82h

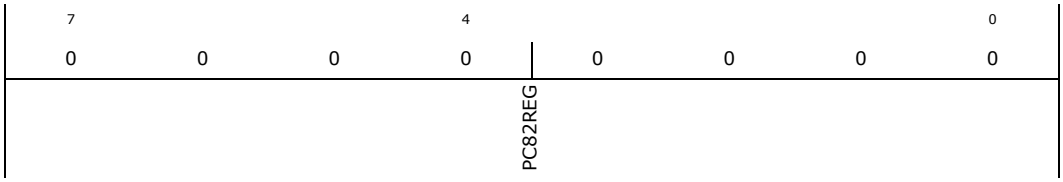
Post Code 82 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC82: 82h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC82REG:** Post Code 82 register

19.2.4 PC83—Offset 83h

Post Code 83 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC83: 83h

Default: 00h

Bit Range	Default & Access	Description
7:0	X RW	**PC83REG:** Post Code 83 register

19.2.5 PC84—Offset 84h

Post Code 84 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC84: 84h

Default: 00h

Bit Range	Default & Access	Description
7:0	X RW	**PC80REG (PC84REG):** Post Code 84 register

19.2.6 PC85—Offset 85h

Post Code 85 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC85: 85h

Default: 00h

Bit Range	Default & Access	Description
7:0	X RW	**PC85REG:** Post Code 85 register

19.2.7 PC86—Offset 86h

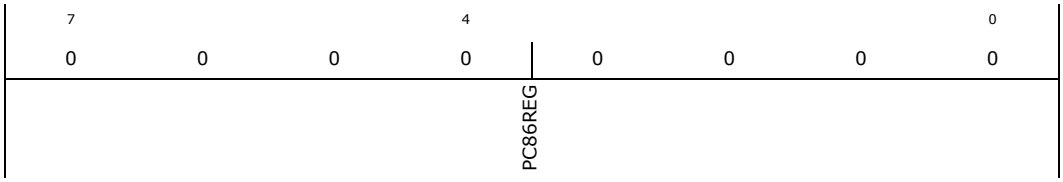
Post Code 86 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC86: 86h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**PC86REG:** Post Code 86 register

19.2.8 PC87—Offset 87h

Post Code 87 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC87: 87h

Default: 00h

Bit Range	Default & Access	Description
7:0	X RW	**PC87REG:** Post Code 87 register

19.2.9 PC88—Offset 88h

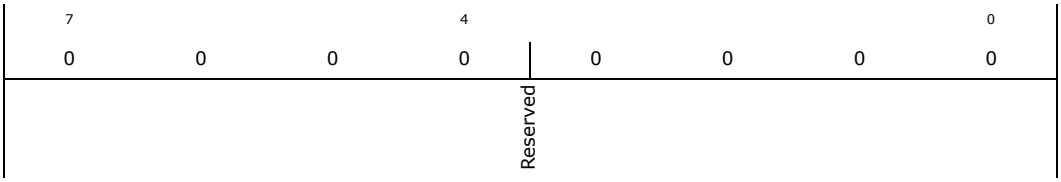
Post Code 88 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC88: 88h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

19.2.10 PC89—Offset 89h

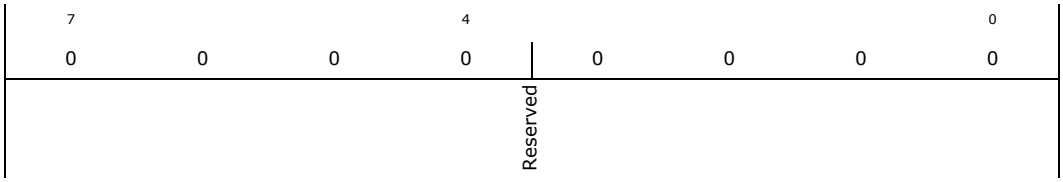
Post Code 89 register

Access Method

Type: I/O Register
(Size: 8 bits)

PC89: 89h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

19.2.11 PC8A—Offset 8Ah

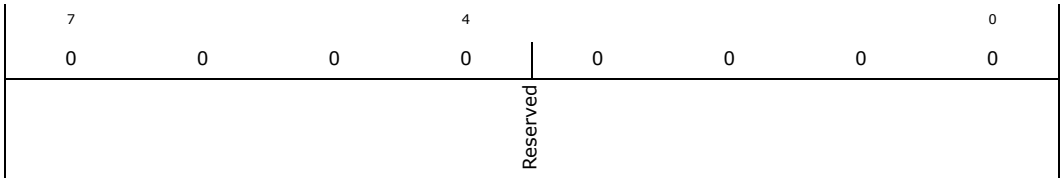
Post Code 8A register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8A: 8Ah

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

19.2.12 PC8B—Offset 8Bh

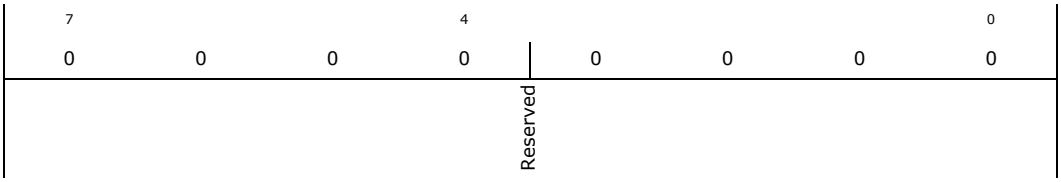
Post Code 8B register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8B: 8Bh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

19.2.13 PC8C—Offset 8Ch

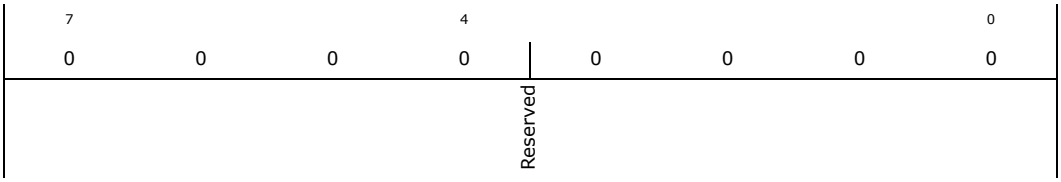
Post Code 8C register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8C: 8Ch

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

19.2.14 PC8D—Offset 8Dh

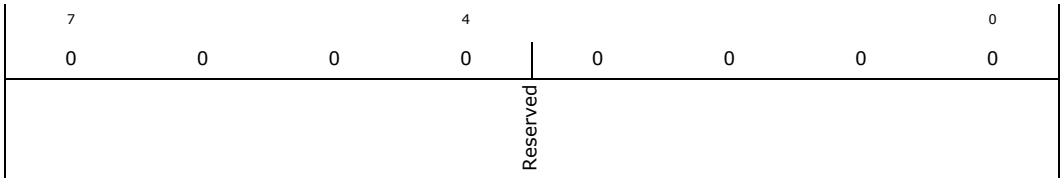
Post Code 8D register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8D: 8Dh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

19.2.15 PC8E—Offset 8Eh

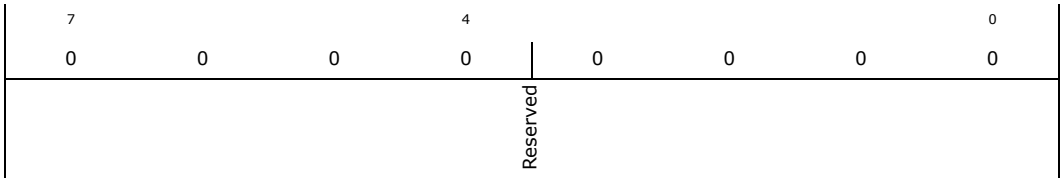
Post Code 8E register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8E: 8Eh

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

19.2.16 PC8F—Offset 8Fh

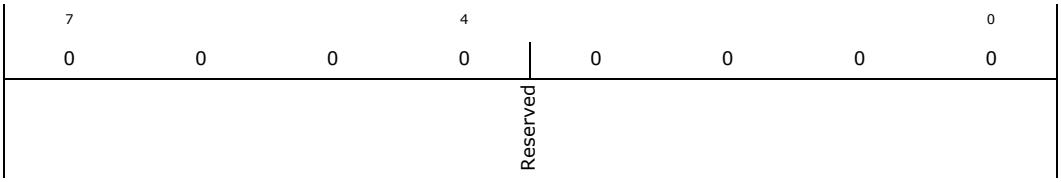
Post Code 8F register

Access Method

Type: I/O Register
(Size: 8 bits)

PC8F: 8Fh

Default: 00h

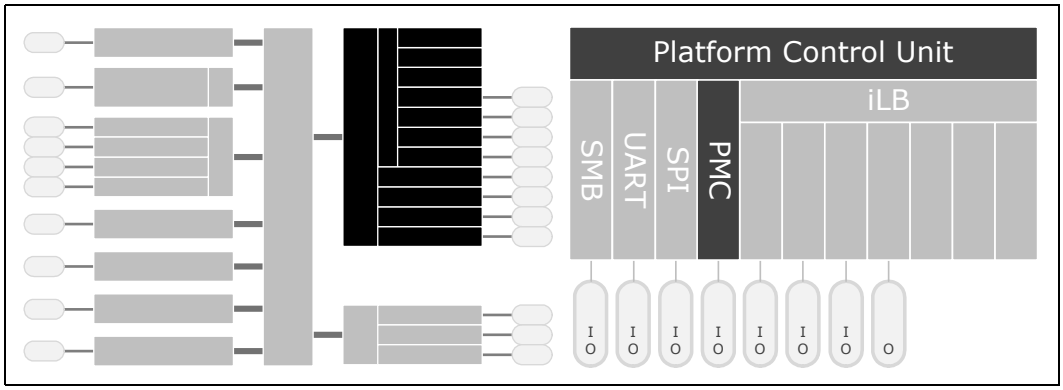


Bit Range	Default & Access	Description
7:0	0h RO	**Reserved:** Reserved.

§ §

20 PCU – Power Management Controller (PMC)

The Power Management Controller (PMC) controls many of the power management features present in the processor.



20.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 144. PMC Signals (Sheet 1 of 3)

Signal Name	Direction/ Type	Description
PMC_ACPRESENT	I CMOS	**AC Present:** This input pin indicates when the platform is plugged into AC power.
PMC_BATLOW#	I CMOS	**Battery Low:** An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from the S3–S5 state. This signal can also be enabled to cause an SMI# when asserted. In desktop configurations without a battery, this signal should be tied high to V1P8_S5.

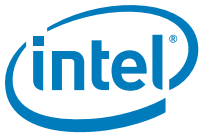


Table 144. PMC Signals (Sheet 2 of 3)

Signal Name	Direction/ Type	Description
PMC_CORE_PWROK	I CMOS	**Core Power OK:** When asserted, this signal is an indication to the processor that all of its core power rails have been stable for 10 ms. It can be driven asynchronously. When it is negated, the processor asserts PMC_PLTRST#. **NOTE:** It is required that the power rails associated with PCI Express (typically the 3.3V, 5V, and 12V core well rails) have been valid for 99 ms prior to PMC_CORE_PWROK assertion in order to comply with the 100 ms T_{PVPERL} PCI Express 2.0 specification on PMC_PLTRST# deassertion. **NOTE:** PMC_CORE_PWROK must not glitch, even if PMC_RSMRST# is low.
PMC_PLTRST#	O CMOS	**Platform Reset:** The processor asserts this signal to reset devices on the platform. The processor asserts the signal during power-up and when software initiates a hard reset sequence through the Reset Control (RST_CNT) register.
PMC_PWRBTN#	I CMOS	**Power Button:** The signal will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If the signal is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S3 & S4 states. This signal has an internal pull-up resistor and has an internal ~16 ms de-bounce on the input.
PMC_RSMRST#	I CMOS	**Resume Well Reset:** Used for resetting the resume well. An external RC circuit is required to guarantee that the resume well power is valid prior to this signal going high.
PMC_RSTBTN#	I CMOS	**System Reset:** This signal forces an internal reset after being debounced (~16 ms). *This signal is multiplexed and may be used by other functions.*
PMC_SLP_S3#	O CMOS	**S3 Sleep Control:** This signal is for power plane control. It can be used to control system power when it is in a S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
PMC_SLP_S4#	O CMOS	**S4 Sleep Control:** This signal is for power plane control. It can be used to control system power when it is in a S4 (Suspend to Disk) or S5 (Soft Off) state.
PMC_SUS_STAT#	O CMOS	**Suspend Status:** This signal is asserted by the processor to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. *This signal is multiplexed and may be used by other functions.*
PMC_SUSCLK	O CMOS	**Suspend Clock:** This 32 kHz clock is an output of the RTC generator circuit for use by other chips for refresh clock. *This signal is multiplexed and may be used by other functions.*
PMC_SUSPWRDNACK	O CMOS	**Suspend Power Down Acknowledge:** Asserted by the processor when it does not require its Suspend well to be powered. This pin requires a pull-up to UNCORE_V1P8_G3. *This signal is multiplexed and may be used by other functions.*
PMC_WAKE_PCIE[0]#	I CMOS	**PCI Express* Port 0 Wake Event:** Sideband wake signal on PCI Express asserted by a component requesting wake up. *This signal is multiplexed and may be used by other functions.*
PMC_WAKE_PCIE[1]#	I CMOS	**PCI Express* Port 1 Wake Event:** Sideband wake signal on PCI Express asserted by a component requesting wake up. *This signal is multiplexed and may be used by other functions.*

Table 144. PMC Signals (Sheet 3 of 3)

Signal Name	Direction/ Type	Description
PMC_WAKE_PCIE[2]#	I CMOS	**PCI Express* Port 2 Wake Event:** Sideband wake signal on PCI Express asserted by a component requesting wake up. *This signal is multiplexed and may be used by other functions.*
PMC_WAKE_PCIE[3]#	I CMOS	**PCI Express* Port 3 Wake Event:** Sideband wake signal on PCI Express asserted by a component requesting wake up. *This signal is multiplexed and may be used by other functions.*
PMC_PLT_CLK[5:0]	O CMOS	**Platform Clocks:** Configurable single ended clocks, configurable to 19.2 MHz or 25 MHz. *This signal is multiplexed and may be used by other functions.*

20.2 Features

20.2.1 Sx-G3-Sx, Handling Power Failures

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

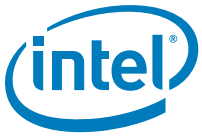
The GEN_PMCON1.AG3E bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). There are only two possible events that will wake the system after a power failure.

- **PMC_PWRBTN#:** PMC_PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PM1_STS_EN.PWRBTN_STS bit is reset. When the processor exits G3 after power returns (PMC_RSMRST# goes high), the PMC_PWRBTN# signal is already high (because the suspend plane goes high before PMC_RSMRST# goes high) and the PM1_STS_EN.PWRBTN_STS bit is 0b.
- **RTC Alarm:** The PM1_STS_EN.RTC_EN bit is in the RTC well and is preserved after a power loss. Like PM1_STS_EN.PWRBTN_STS the PM1_STS_EN.RTC_STS bit is cleared when PMC_RSMRST# goes low.

The processor monitors both PMC_CORE_PWROK and PMC_RSMRST# to detect for power failures. If PMC_CORE_PWROK goes low, the GEN_PMCON1.PWR_FLR bit is set. If PMC_RSMRST# goes low, GEN_PMCON1.SUS_PWR_FLR is set.

Table 145. Transitions Due to Power Failure

State at Power Failure	GEN_PMCON1.AG3E bit	Transition When Power Returns
S0, S3	1 0	S5 S0
S4	1 0	S4 S0
S5	1 0	S5 S0



20.2.2 Event Input Signals and Their Usage

The processor has various input signals that trigger specific events. This section describes those signals and how they should be used.

20.2.3 PCI Express* WAKE# Signal and PME Event Message

PCI Express ports can wake the platform from any sleep state (S3, S4, or S5) using the PMC_WAKE_PCIE[3:0]# pins. PMC_WAKE_PCIE[3:0]# is treated as a wake event, but does not cause any bits to go active in the GPE0a_STS register.

Note: PMC_WAKE_PCIE[3:0]# functionality is disabled by setting PM1_STS_EN.PCIEXP_WAKE_DIS[3:0] respectively to 1b.

PCI Express ports have the ability to cause PME using messages. When a PME message is received, the processor will set the GPE0a_STS.PCI_EXP_STS bit.

20.2.3.1 PMC_PWRBTN# (Power Button)

The PMC_PWRBTN# signal operates as a "Fixed Power Button" as described in the Advanced Configuration and Power Interface specification. The signal has a 16 ms debounce on the input. The state transition descriptions are included in Table 146. Note that the transitions start as soon as the PMC_PWRBTN# is pressed (but after the debounce logic), and does not depend on when the power button is released.

Note: During the time that the PMC_SLP_S4# signal is stretched for the minimum assertion width (if enabled), the power button is not a wake event. Refer to note below for more details.

Table 146. Transitions Due to Power Button

Present State	Event	Transition/Action	Comment
S0/Cx	PMC_PWRBTN# goes low	SMI# or SCI generated (depending on PM1_CNT.SCI_EN, PM1_STS_EN.PWRBTN_EN and SMI_EN.GBL_SMI_EN)	Software typically initiates a Sleep state
S3–S5	PMC_PWRBTN# goes low	Wake Event. Transitions to S0 state	Standard wakeup
G3	PMC_PWRBTN# pressed	None	No effect since no power Not latched nor detected
S0, S3–S4	PMC_PWRBTN# held low for at least 4 consecutive seconds	Unconditional transition to S5 state	No dependence on processor or any other subsystem

Power Button Override Function

If PMC_PWRBTN# is observed active for at least four consecutive seconds, the state machine should unconditionally transition to the S5 state, regardless of present state (S0–S4), even if the PMC_CORE_PWROK is not active. In this case, the transition to the G2/S5 state should not depend on any particular response from the processor nor any similar dependency from any other subsystem.

The PMC_ PWRBTN# status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable using the GEN_PMCON2.PWRBTN_LVL bit.

Note: The 4-second PMC_PWRBTN# assertion should only be used if a system lock-up has occurred. The 4-second timer starts counting when the processor is in a S0 state. If the PMC_PWRBTN# signal is asserted and held active when the system is in a suspend state (S3–S4), the assertion causes a wake event. Once the system has resumed to the S0 state, the 4-second timer starts.

Note: During the time that the SLP_S4# signal is stretched for the minimum assertion width (if enabled by GEN_PMCON1.S4ASE), the power button is not a wake event. As a result, it is conceivable that the user will press and continue to hold the power button waiting for the system to awake. Since a 4-second press of the power button is already defined as an unconditional power down, the power button timer will be forced to inactive while the power-cycle timer is in progress. Once the power-cycle timer has expired, the power button awakes the system. Once the minimum PMC_SLP_S4# power cycle expires, the power button must be pressed for another 4 to 5 seconds to create the override condition to S5.

20.2.3.2 Sleep Button

The Advanced Configuration and Power Interface specification defines an optional sleep button. It differs from the power button in that it only is a request to go from S0 to S3–S4 (not S5). Also, in an S5 state, the power button can wake the system, but the sleep button cannot.

Although the processor does not include a specific signal designated as a sleep button, one of the GPIO signals can be used to create a “Control Method” sleep button. See the Advanced Configuration and Power Interface specification for implementation details.

20.2.3.3 PME_B0 (PCI Power Management Event Bus 0)

The GPE0a_STS.PME_B0_STS bit exists to implement PME#-like functionality for any internal device on Bus 0 with PCI power management capabilities.

20.2.3.4 PMC_RSTBTN# Signal

When the PMC_RSTBTN# pin is detected as active after the 16 ms debounce logic, the processor attempts to perform a “graceful” reset, by waiting for the relevant internal devices to signal their idleness. If all devices are idle when the pin is detected active, the reset occurs immediately; otherwise, a counter starts. If at any point during the count all devices go idle the reset occurs. If the counter expires and any device is still active, a reset is forced upon the system even though activity is still occurring.

Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the PMC_RSTBTN# input remains asserted or not. It cannot occur again until PMC_RSTBTN# has been detected inactive after the debounce logic, and the system is back to a full S0 state with PMC_PLTRST# inactive. Note that if RST_CNT.FULL_RST is set then PMC_RSTBTN# will result in a full power cycle reset.

20.2.4 System Power Planes

The system has several independent power planes, as described in Table 147. Note that when a particular power plane is shut off, it should go to a 0 V level.

Table 147. System Power Planes

Plane	Controlled By	Description
CPU	PMC_SLP_S3#	The SLP_S3# signal can be used to cut the CORE_VCC_S0 rail completely.
Main	PMC_SLP_S3#	When SLP_S3# goes active, power can be shut off to any circuit not required to wake the system from the S3 state. Since the S3 state requires that the memory context be preserved, power must be retained to the main memory. Devices on LPC bus, PCI-Express, and SATA will typically be shut when the Main power plane is shut, although they may have small subsections powered.
Devices and Memory	PMC_SLP_S4#	When PMC_SLP_S4# goes active, power can be shut off to any circuit not required to wake the system from the S4/S5. Since the memory context does not need to be preserved in the S4/S5 state, the power to the memory can also be shut down. S4 and S5 requests are treated the same so no PMC_SLP_S5# signal is implemented.
Devices	Implementation Specific	Individual subsystems may have their own power plane. For example, GPIO signals may be used to control the power to disk drives, audio amplifiers, or the display screen.
Suspend	PMC_SUSPWRDNACK	The suspend power planes are generally left on whenever the system has a charged main battery or is plugged in to AC power. In some cases, it may be preferable to disable the suspend power planes in S4/S5 states to save additional power. This requires some external logic (such as an embedded controller) to ensure that a wake event is still possible (such as the power button). When the SeC is enabled it is advised that the suspend power planes not be removed. Doing so may result in extremely long Sx exit times since the SeC if forced to consider it a cold boot which may, in turn, cause exit latency violations for software using the TXE.

20.2.4.1 Power Plane Control with PMC_SLP_S3#, PMC_SLP_S4#

The PMC_SLP_S3# output signal can be used to cut power to the system core supply, since it only goes active for the Suspend-to-RAM state (typically mapped to ACPI S3). Power must be maintained to the processor suspend well, and to any other circuits that need to generate wake signals from the Suspend-to-RAM state. During S3 (Suspend-to-RAM) all signals attached to powered down plans will be tri-stated or driven low, unless they are pulled using a pull-up resistor.Cutting power to the core may be done using the power supply, or by external FETs on the motherboard.

The PMC_SLP_S4# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done using the power supply, or by external FETs on the motherboard.

20.2.4.2 PMC_SLP_S4# and Suspend-To-RAM Sequencing

The system memory suspend voltage regulator is controlled by the Glue logic. The PMC_SLP_S4# signal should be used to remove power to system memory. The PMC_SLP_S4# logic in the processor provides a mechanism to fully cycle the power to the DRAM and/or detect if the power is not cycled for a minimum time.

Note: To use the minimum DRAM power-down feature that is enabled by the GEN_PMCON1.S4ASE bit, the DRAM power must be controlled by the PMC_SLP_S4# signal.

20.2.4.3 PMC_CORE_PWROK Signal

When asserted, PMC_CORE_PWROK is an indication to the processor that its core well power rails are powered and stable. PMC_CORE_PWROK can be driven asynchronously. When PMC_CORE_PWROK is low, the processor asynchronously asserts PMC_PLTRST#. PMC_CORE_PWROK must not glitch, even if PMC_RSMRST# is low.

It is required that the power rails associated with PCI Express have been valid for 99 ms prior to PWROK assertion in order to comply with the 100 ms T_{PVPERL} PCI Express 2.0 specification on PMC_PLTRST# deassertion.

Note: PMC_RSTBTN# is recommended for implementing the system reset button. This saves external logic that is needed if the PMC_CORE_PWROK input is used. Additionally, it allows for better handling of the SMBus and processor resets and avoids improperly reporting power failures.

20.2.4.4 PMC_BATLOW# (Battery Low)

The PMC_BATLOW# input can inhibit waking from S3, S4, and S5 states if there is not sufficient power. It also causes an SMI if the system is already in an S0 state.

20.2.5 SMI#/SCI Generation

Upon any enabled SMI event taking place while the SMI_EN.EOS bit is set, the processor will clear the EOS bit and assert SMI to the CPU core, which will cause it to enter SMM space. SMI assertion is performed using a Virtual Legacy Wire (VLW) message. Prior system generations (those based upon legacy processors) used an actual SMI# pin.

Once the SMI message has been delivered, the processor takes no action on behalf of active SMI events until Host software sets the End of SMI (EOS) bit. At that point, if any SMI events are still active, the processor will send another SMI message.

The SCI is a level-mode interrupt that is typically handled by an ACPI-aware operating system. In non-APIC systems (which is the default), the SCI IRQ is routed to one of the 8259 interrupts (IRQ 9, 10, or 11). The 8259 interrupt controller must be programmed to level mode for that interrupt.

In systems using the APIC, the SCI can be routed to interrupts IRQs[11:9] or IRQs[23:20]. The interrupt polarity changes depending on whether it is on an interrupt shareable with a PIRQ or not. The interrupt remains asserted until all SCI sources are removed.

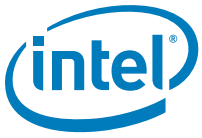
Table 148 shows which events can cause an SMI and SCI. Note that some events can be programmed to cause either an SMI or SCI. The usage of the event for SCI (instead of SMI) is typically associated with an ACPI-based system. Each SMI or SCI source has a corresponding enable and status bit.

Table 148. Causes of SMI and SCI (Sheet 1 of 2)

Event	Status Indication[1]	Enable Condition	Interrupt Result			
			SMI_EN. GBL_SMI_EN=1b		SMI_EN. GBL_SMI_EN=0b	
			PM1_CNT.SCI_EN=1b	PM1_CNT.SCI_EN=0b	PM1_CNT.SCI_EN=1b	PM1_CNT.SCI_EN=0b
Power Button Override[3]	PM1_STS_EN. PWRBTNOR_STS	None	SCI	None	SCI	None
RTC Alarm	PM1_STS_EN. RTC_STS	PM1_STS_EN_EN. RTC_EN=1b	SCI	SMI	SCI	None
Power Button Press	PM1_STS_EN. PWRBTN_STS	PM1_STS_EN_EN. PWRBTN_EN=1b	SCI	SMI	SCI	None
SMI_EN.BIOS_RLS bit written to 1b[4]	PM1_STS_EN. GBL_STS	PM1_STS_EN_EN. GBL_EN=1b	SCI			
ACPI Timer overflow (2.34 seconds)	PM1_STS_EN. TMROF_STS	PM1_STS_EN_EN. TMROF_EN =1b	SCI	SMI	SCI	None
GPI[n][9]	GPE0a_STS. CORE_GPIO_STS[n][2] or GPE0a_STS. SUS_GPIO_STS[n][2]	GPIO_ROUT[n] = 10b & GPE0a_EN. CORE_GPIO_EN[n][2] =1b or GPE0a_EN. SUS_GPIO_EN[n][2]= 1b	SCI	None	SCI	None
Internal, Bus 0, PME-Capable Agents (PME_B0)	GPE0a_STS. PME_B0_STS	GPE0_EN. PME_B0_EN=1b	SCI	SMI	SCI	None
BATLOW# pin goes low	GPE0a_STS. BATLOW_STS#	GPE0_EN. BATLOW_EN=1b	SCI	SMI	SCI	None
PCI Express GPE messages	GPE0a_STS. HOT_PLUG_STS	GPE0_EN. HOT_PLUG_EN=1b	SCI	None	SCI	None
Software Generated GPE	GPE0a_STS. SWGPE_STS	GPE0_EN. SWGPE_EN=1b	SCI	SMI	SCI	None
PCI Express Hot Plug SCI Message	GPE0a_STS. HOT_PLUG_STS	GPE0_EN. HOT_PLUG_EN=1b	SCI	None	SCI	None

Table 148. Causes of SMI and SCI (Sheet 2 of 2)

Event	Status Indication[1]	Enable Condition	Interrupt Result			
			SMI_EN. GBL_SMI_EN=1b		SMI_EN. GBL_SMI_EN=0b	
			PM1_CNT.SCI_EN=1b	PM1_CNT.SCI_EN=0b	PM1_CNT.SCI_EN=1b	PM1_CNT.SCI_EN=0b
ASSERT_SCI message from PCIe	GPE0a_STS. PCI_EXP_STS	None (enabled by PCIe controller)	SCI	None	SCI	None
DOSCI message from GUNIT[5]	GPE0a_STS. GUNIT_STS	None (enabled by G-Unit[8])	SCI	None	SCI	None
ASSERT_SMI message from SPI[5]	SMI_STS. SPI_SMI_STS	None (enabled by SPI controller)	SMI		None	
ASSERT_SMI message from PCIe[5]	SMI_STS. PCI_EXP_SMI_STS	None (enabled by PCIe controller)	SMI		None	
ASSERT_IS_SMI message from USB	SMI_STS. USB_IS_STS	SMI_EN. USB_IS_SMI_EN=1b	SMI		None	
ASSERT_SMI message from USB	SMI_STS.USB_STS	SMI_EN. USB_SMI_EN=1b	SMI		None	
ASSERT_SMI message from SMBus[5]	SMI_STS. SMBUS_SMI_STS	None (enabled by SMBus controller)	SMI		None	
ASSERT_SMI message from iLB[5]	SMI_STS. ILB_SMI_STS	None (enabled by iLB)	SMI		None	
Periodic timer expires	SMI_STS. PERIODIC_STS	SMI_EN. PERIODIC_EN=1b	SMI		None	
WDT first expiration	SMI_STS.TCO_STS	SMI_EN.TCO_EN=1b	SMI		None	
64 ms timer expires	SMI_STS. SWSMI_TMR_STS	SMI_EN. SWSMI_TMR_EN=1b	SMI		None	
PM1_CNT.SLP_EN bit written to 1b	SMI_STS. SMI_ON_SLP_EN_STS	SMI_EN. SMI_ON_SLP_EN =1b	Sync SMI[6]		None	
PM1_CNT.GBL_RLS written to 1b	SMI_STS.BIOS_STS	SMI_EN. BIOS_EN=1b	Sync SMI[6]		None	
DOSMI message from GUNIT[5]	SMI_STS. GUNIT_SMI_STS	None (enabled by G-Unit[8])	SMI		None	
ASSERT_IS_SMI message from iLB[5]	SMI_STS. ILB_SMI_STS	None (enabled by iLB)	Sync SMI[7]		None	
ASSERT_IS_SMI message from PCIe[5]	SMI_STS. PCI_EXP_SMI_STS	None (enabled by PCIe controller)	SMI		None	
GPI[n][10]	ALT_GPIO_SMI. CORE_GPIO_SMI_STS[n][2] or ALT_GPIO_SMI. SUS_GPIO_SMI_STS[n][2]	GPIO_ROUT[n]=01b & ALT_GPIO_SMI. CORE_GPIO_SMI_EN[n][2]=1b or ALT_GPIO_SMI. SUS_GPIO_SMI_EN[n][2]=1b	SMI		None	
USB Per-Port Registers Write Enable bit is changed from 0b to 1b	UPRWC.WE_STS & SMI_STS. USB_IS_STS	UPRWC. WE_SMI_E=1b & SMI_EN. USB_IS_SMI_EN=1b	Sync SMI[6]		None	



NOTES:
1. Most of the status bits (except otherwise is noted) are set according to event occurrence regardless to the enable bit.
2. GPIO status bits are set only if enable criteria is true. GPIO_ROUT[n]=10b & GPE0a_EN.x_GPIO_EN[n] for GPE0a_STS.x_GPIO_STS[n] (SCI). GPIO_ROUT[n]=01b & ALT_GPIO_SMI. x_GPIO_SMI_EN[n]=1b for ALT_GPIO_SMI.x_GPIO_SMI_STS[n] (SMI).
3. When power button override occurs, the system will transition immediately to S5. The SCI will only occur after the next wake to S0 if the residual status bit (PM1_STS_EN.PWRBTNOR_STS) is not cleared prior to setting PM1_CNT.SCI_EN.
4. PM1_STS_EN.GBL_STS being set will cause an SCI, even if the PM1_CNT.SCI_EN bit is not set. Software must take great care not to set the SMI_ENBIOS_RLS bit (which causes PM1_STS_EN.GBL_STS to be set) if the SCI handler is not in place.
5. No enable bits for these SCI/SMI messages in the PMC. Enable capability should be implemented in the source unit.
6. Sync SMI has the same message opcode toward T-Unit. Special treatment regarding this Sync SMI is holding completion to host till SYNC_SMI_ACK message is received from T-Unit.
7. Sync SMI has the same message opcode toward T-Unit. Special treatment regarding this Sync SMI is holding the SSMI_ACK message to iLB till SYNC_SMI_ACK message is received from T-Unit.
8. The G-Unit is an internal functional sub-block which forms part of the graphics functional block.
9. The GPE0a_STS.CORE_GPIO_STS[31:24] & GPE0a_EN.CORE_GPIO_EN[31:24] register bits correspond to GPIO_S0_SC[7:0]. GPE0a_STS.SUS_GPIO_STS[23:16] & GPE0a_EN.SUS_GPIO_EN[23:16] correspond to GPIO_S5[7:0].
10. The ALT_GPIO_SMI.CORE_GPIO_SMI_STS[31:24] & ALT_GPIO_SMI.CORE_GPIO_SMI_EN[15:8] register bits correspond to GPIO_S0_SC[7:0]. ALT_GPIO_SMI.SUS_GPIO_SMI_STS[23:16] & ALT_GPIO_SMI.SUS_GPIO_SMI_EN[7:0] correspond to GPIO_S5[7:0].

20.2.6 Platform Clock Support

The processor supports up to 6 clocks (PMC_PLT_CLK[5:0]) with a frequency of either 19.2 MHz or 25 MHz. These clocks are available for general system use, where appropriate and each have Control & Frequency register fields associated with them.

Note: Intel recommends 25 MHz. 19.2 MHz is not validated.

20.2.7 INIT# (Initialization) Generation

The INIT# functionality is implemented as a 'virtual wire' internal to the processor rather than a discrete signal. This virtual wire is asserted based on any one of the events described in below table. When any of these events occur, INIT# is asserted for 16 PCI clocks and then driven high.

INIT#, when asserted, resets integer registers inside the CPU cores without affecting its internal caches or floating-point registers. The cores then begin execution at the power on Reset vector configured during power on configuration.

Table 149. INIT# Assertion Causes

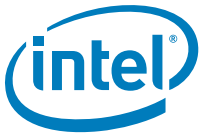
Cause	Comment
PORT92.INIT_NOW transitions from 0b to1b.	
RST_CNT.SYS_RST = 0b and RST_CNT.RST_CPU transitions from 0b to 1b	

20.3 USB Per-Port Register Write Control

The PMC contains the UPRWC.USB_PER_PORT_WE (USB Per-Port Registers Write Enable) bit. When this bit is written from 0b to 1b, the UPRWC.WE_STS (Write Enable Status) bit is asserted. This transaction initiates sync-SMI if the UPRWC.WE_SMIEN (Write Enable SMI Enable) bit and the SMI_EN.USB_IS_SMI_EN (USB Intel Specific SMI Enable) bit are set to 1b.

20.4 References

Advanced Configuration and Power Interface Specification, Revision 3.0: http://www.acpi.info/



20.5 PCU PMC Memory Mapped I/O Registers

Table 150. Summary of PCU iLB PMC Memory Mapped I/O Registers—PMC_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"PRSTS - Power and Reset Status (PRSTS)—Offset 0h" on page 990	00000000h
8h	4	"PM_CFG - Power Management Configuration (PMC_CFG)—Offset 8h" on page 992	00000000h
Ch	4	"VLV_PM_STS - VLV Power Management Status (VLV_PM_STS)—Offset Ch" on page 993	00000000h
10h	4	"MTPMC - Message to PMC (MTPMC)—Offset 10h" on page 994	00000000h
20h	4	"General PM Configuration 1 (GEN_PMCON1)—Offset 20h" on page 995	00004004h
24h	4	"General PM Configuration 2 (GEN_PMCON2)—Offset 24h" on page 997	00000000h
28h	4	"MFPMC - Message from PMC (MFPMC)—Offset 28h" on page 999	00000000h
2Ch	4	"SEC_STS - SEC Status (SEC_STS)—Offset 2Ch" on page 999	00000000h
30h	4	"Configured Revision ID (CRID)—Offset 30h" on page 1000	00000000h
34h	4	"Function Disable (FUNC_DIS)—Offset 34h" on page 1001	00000000h
38h	4	"Function Disable 2 (FUNC_DIS_2)—Offset 38h" on page 1002	00000000h
3Ch	4	"ETR - Extended Test Mode Register (ETR)—Offset 48h" on page 1003	00FFFFFFh
40h	4	"ETR - Extended Test Mode Register (ETR)—Offset 48h" on page 1003	00000000h
48h	4	"ETR - Extended Test Mode Register (ETR)—Offset 48h" on page 1003	00230000h
50h	4	"VLT - Voltage Detect Register (VLT)—Offset 50h" on page 1004	00000000h
58h	4	"GPIO_ROUT - GPIO_ROUT register (GPIO_ROUT)—Offset 58h" on page 1004	00000000h
60h	4	"PLT_CLK_CTL_0 - Platform Clock Control 0 (PLT_CLK_CTL_0)—Offset 60h" on page 1005	00000003h
64h	4	"PLT_CLK_CTL_1 - Platform Clock Control 1 (PLT_CLK_CTL_1)—Offset 64h" on page 1005	00000003h
68h	4	"PLT_CLK_CTL_2 - Platform Clock Control 2 (PLT_CLK_CTL_2)—Offset 68h" on page 1006	00000003h
6Ch	4	"PLT_CLK_CTL_3 - Platform Clock Control 3 (PLT_CLK_CTL_3)—Offset 6Ch" on page 1006	00000003h
70h	4	"PLT_CLK_CTL_4 - Platform Clock Control 4 (PLT_CLK_CTL_4)—Offset 70h" on page 1007	00000003h
74h	4	"PLT_CLK_CTL_5 - Platform Clock Control 5 (PLT_CLK_CTL_5)—Offset 74h" on page 1008	00000003h
80h	4	"S0IR_TMR - S0I Ready Residency Timer (S0IR_TMR)—Offset 80h" on page 1008	00000000h
84h	4	"S3_TMR - S3 Residency Timer (S3_TMR)—Offset 84h" on page 1009	00000000h
88h	4	"S3_TMR - S3 Residency Timer (S3_TMR)—Offset 88h" on page 1009	00000000h
8Ch	4	"S3_TMR - S3Residency Timer (S3_TMR)—Offset 8Ch" on page 1010	00000000h
90h	4	"S0_TMR - S0 Residency Timer (S0_TMR)—Offset 90h" on page 1010	00000000h
98h	4	"PSS - Power island Power Status (PSS)—Offset 98h" on page 1011	00000000h
A0h	4	"D3_STS_0 - D3 Status register 0 (D3_STS_0)—Offset A0h" on page 1012	00000000h
A4h	4	"D3_STS_1 - D3 Status register 1 (D3_STS_1)—Offset A4h" on page 1012	00000000h
A8h	4	"D3_STDBY_STS_0 - D3 Standby Status register 0 (D3_STDBY_STS_0)—Offset A8h" on page 1013	00000000h

Table 150. Summary of PCU iLB PMC Memory Mapped I/O Registers—PMC_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
ACh	4	"D3_STDBY_STS_1 - D3 Standby Status register 1 (D3_STDBY_STS_1)—Offset ACh" on page 1014	00000000h
B0h	4	"MTPMC_1 - Message to PMC 1 (MTPMC_1)—Offset B0h" on page 1015	00000000h
B4h	4	"MTPMC_2 - Message to PMC 2 (MTPMC_2)—Offset B4h" on page 1016	00000000h
B8h	4	"MTPMC_3 - Message to PMC 3 (MTPMC_3)—Offset B8h" on page 1016	00000000h
BCh	4	"MTPMC_4 - Message to PMC 4 (MTPMC_4)—Offset BCh" on page 1017	00000000h
C0h	4	"PME Status 0 – Status bit for PME messages (PME_STS)—Offset C0h" on page 1017	00000000h
C4h	4	"GPE Level Edge mode (GPE_LEVEL_EDGE)—Offset C4h" on page 1018	00000000h
C8h	4	"GPE polarity mode (GPE_POLARITY)—Offset C8h" on page 1019	00000000h
CCh	4	"Lock Register (LOCK)—Offset CCh" on page 1019	00000000h
D0h	4	"Virtual UART register (VUART1)—Offset D0h" on page 1020	00000000h
D4h	4	"Virtual UART register (VUART2)—Offset D4h" on page 1021	00000000h
D8h	4	"Virtual UART register (VUART3)—Offset D8h" on page 1021	00000000h
DCh	4	"Virtual UART register (VUART4)—Offset DCh" on page 1022	00000000h

20.5.1 PRSTS - Power and Reset Status (PRSTS)—Offset 0h

Bits in this register only need to be valid for reading when the Main power well is up. However, since some of the events may initially be detected while the Main power well is down, they are marked as suspend well bits. All suspend well bits in this register are reset by global reset#.

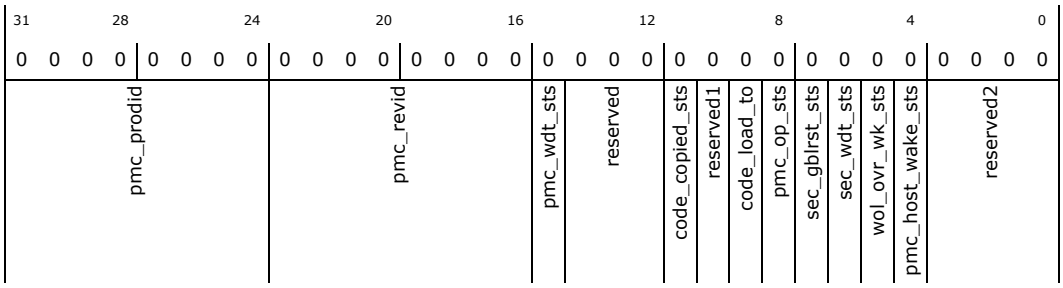
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

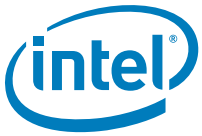
PRSTS: [PMC_BASE_ADDRESS] + 0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**Power Management Controller Product ID (PMC_PRODID) (pmc_prodid):** This field communicates the Product Family of the power management functionality



Bit Range	Default & Access	Description
23:16	0b RO	**Power Management Controller Revision ID (PMC_REVID) (pmc_revid):** This field communicates the implementation revision of the power management functionality.
15	0b RW	**PMC Watchdog Timer Status (PMC_WDT_STS) (pmc_wdt_sts):** This bit will be set to '1' when the PMC Watch Dog Timer triggers a reset. It will be cleared by a write of '1' by software.
14:12	0b RO	**reserved:** Reserved.
11	0b RO	**Code Copied Over Status (CODE_COPIED_STS) (code_copied_sts):** The processor sets this bit when PMC code is successfully authenticated and loaded from the flash
10	0b RO	**reserved (reserved1):** Reserved.
9	0b RO	**Code Load Timeout Status (CODE_LOAD_TO) (code_load_to):** The processor sets this bit if the loading function fails to complete within a reasonable time limit. This bit remains valid after a PMC Code load is attempted until the next global reset
8	0b RO	**PMC Operational Status (PMC_OP_STS) (pmc_op_sts):** The processor sets this bit when the PMC becomes operational after completing the Code Load. BIOS must wait for this bit to be set before performing resets or sleep events. This bit remains valid after a PMC Code load until the next global reset
7	0b RW	**SEC Watch Dog Timer Status (SEC_GBLRST_STS) (sec_gblrst_sts):** This bit will be set to '1' when the SEC FW triggers a reset. It will be cleared by a write of '1' by software.
6	0b RW	**SEC Watch Dog Timer Status (SEC_WDT_STS) (sec_wdt_sts):** This bit will be set to '1' when the SEC Watch Dog Timer triggers a reset. It will be cleared by a write of '1' by software.
5	0b RW	**Wake On LAN Override Wake Status (WOL_OVR_WK_STS) (wol_ovr_wk_sts):** This bit gets set when integrated LAN Signals a Power Management Event AND the system is in S5. BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4	0b RW	**PMC_HOST_WAKE_STS (PMC_HOST_WAKE_STS) (pmc_host_wake_sts):** The processor Power Management Controller sets this bit if it wakes the host for reasons other than typical host-visible wake events. This status bit provides information to BIOS that the PMC caused the wake.
3:0	0b RO	**reserved2:** Reserved.

20.5.2 PM_CFG - Power Management Configuration (PMC_CFG)—Offset 8h

This register contains misc. fields used to configure the processor's power management behavior.

Access Method

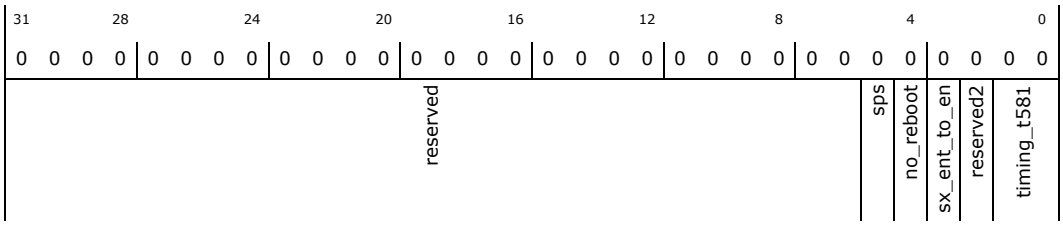
Type: Memory Mapped I/O Register (Size: 32 bits)

PMC_CFG: [PMC_BASE_ADDRESS] + 8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:6	0b RO	**reserved:** Reserved.
5	0b RW	**Shutdown Policy Select (SPS) (sps):** When cleared (default) the processor will drive INIT# in response to the shutdown Message. When set to 1, processor will treat the shutdown message similar to receiving a CF9h I/O write, and will drive PMU_PLTRST active. . BIOS guide note: This register is reset any time PMU_PLTRST asserts.
4	0b RW	**No Reboot (NO_REBOOT) (no_reboot):** This bit is set when the No Reboot strap is sampled high on COREPWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates No Reboot. When set, the TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.
3	0b RW	**S1/3/4/5 Entry Timeout Enable (SX_ENT_TO_EN) (sx_ent_to_en):** This policy bit determines whether the processor will apply a timeout to the S1/S3/S4/S5 entry flow. If this timeout is enabled and the entry flow appears to be hung, the processor will trigger a straight-to-S5 global reset. Encodings: 0: Timeout disabled (default) 1: Timeout enabled reset_type=RSMRST_B
2	0b RO	**reserved (reserved2):** Reserved.
1:0	0b RW	**Timing t581 (TIMING_T581) (timing_t581):** This field configures the t581 timing involved in the power down flow (CPU Power Good indication inactive to PLL Enable inactive). Encodings (all min timings): 00: 10 us (default) 01: 100 us 10: 1 ms 11: 10 ms reset_type=Resume Well Reset#

20.5.3 VLV_PM_STS - VLV Power Management Status (VLV_PM_STS)—Offset Ch

This register contains misc. fields used to record events pertaining to processor power management. Unless otherwise indicated, all RWC bits are cleared with a write of 1 by software.

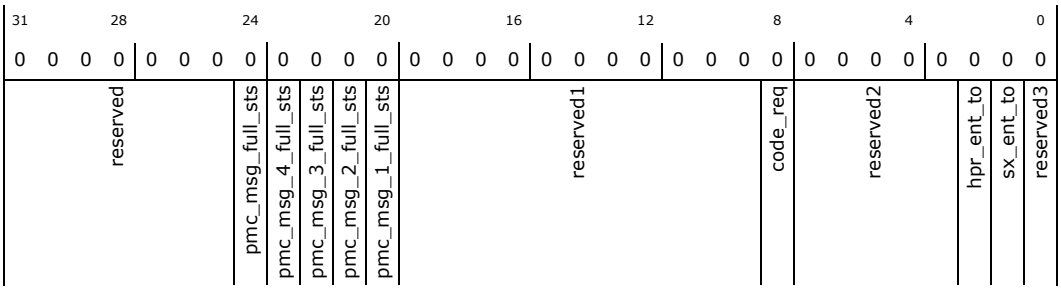
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VLV_PM_STS: [PMC_BASE_ADDRESS] + Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RO	**reserved:** Reserved.
24	0b RO	**PMC Message Full Status (PMC_MSG_FULL_STS) (pmc_msg_full_sts):** 'This bit gets set to 1b automatically when the MTPMC register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
23	0b RO	**PMC Message 4 Full Status (PMC_MSG_4_FULL_STS) (pmc_msg_4_full_sts):** This bit gets set to 1b automatically when the Message to PMC 4 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
22	0b RO	**PMC Message 3 Full Status (PMC_MSG_3_FULL_STS) (pmc_msg_3_full_sts):** This bit gets set to 1b automatically when the Message to PMC 3 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
21	0b RO	**PMC Message 2 Full Status (PMC_MSG_2_FULL_STS) (pmc_msg_2_full_sts):** This bit gets set to 1b automatically when the Message to PMC 2 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
20	0b RO	**PMC Message 1 Full Status (PMC_MSG_1_FULL_STS) (pmc_msg_1_full_sts):** This bit gets set to 1b automatically when the Message to PMC 1 register is written. The PMC clears this bit when it has serviced the message. Host software should poll this bit until it returns a 0b to avoid overwriting the previous message data before the PMC could service it.
19:9	0b RO	**reserved1:** Reserved.

Bit Range	Default & Access	Description
8	0b RO	**Code Requested (CODE_REQ) (code_req):** PMC will set this bit when SEC unit requests exclusion from power flows
7:3	0b RO	**reserved2:** Reserved.
2	0b RW	**Host Partition Reset Entry Timeout (HPR_ENT_TO) (hpr_ent_to):** This bit is set to '1' to record that a global reset was triggered by a timeout during Host partition reset entry sequence.
1	0b RW	**S3/4/5 Entry Timeout (SX_ENT_TO) (sx_ent_to):** This bit is set to '1' to record that a global reset was triggered by a timeout during an S3, S4, or S5 entry sequence.
0	0b RO	**reserved3:** Reserved.

20.5.4 MTPMC - Message to PMC (MTPMC)—Offset 10h

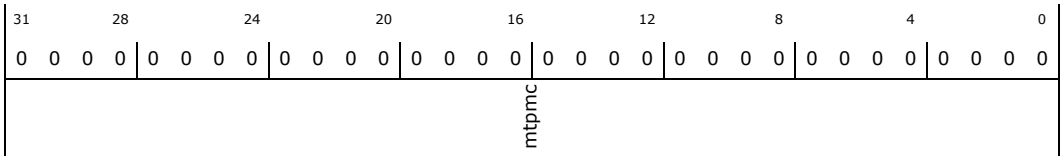
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC: [PMC_BASE_ADDRESS] + 10h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to any of the bytes in this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. In the case of a message that involves a response from the PMC (such as a PMC XRAM read), the host must also consume any data returned by the PMC in the Message from PMC register (MFPMC) before initiating another message

20.5.5 General PM Configuration 1 (GEN_PMCON1)—Offset 20h

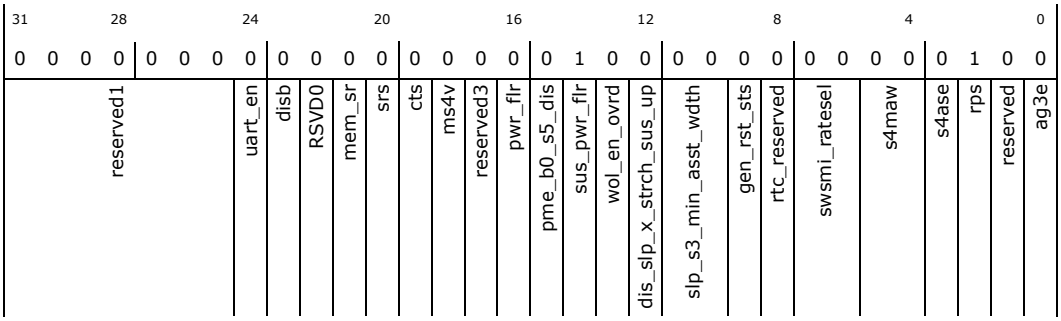
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GEN_PMCON1: [PMC_BASE_ADDRESS] + 20h

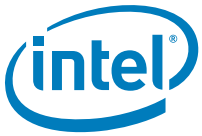
PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00004004h



Bit Range	Default & Access	Description
31:25	0b RO	**reserved1:** Reserved.
24	0b RW	**UART Enable (UART_EN) (uart_en):** When set, PMC enables UART debug port
23	0b RW	**DRAM Initialization Scratchpad Bit (DISB) (disb):** This bit does not effect hardware functionality in any way. It is provided as a scratchpad bit that is maintained through main power well resets and CF9h-initiated resets. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. If the bit is 1, then the DRAM initialization was interrupted. This bit is reset by the assertion of the RSMRST_B pin.
22	0b RO	**RSVD0:** Reserved
21	0b RO	**Memory Placed in Self-Refresh (MEM_SR) (mem_sr):** This bit will be set to 1 if DRAM should have remained powered and held in Self-Refresh through the last power state transition (i.e. the last time the system left S0). The scenarios where this should be the case are: - successful S3 entry and exit - successful Host partition reset without power cycle This bit will be cleared whenever the processor begins a transition out of S0. Note: This bit should not be consulted upon wake from S1, as that state does not involve the same type of handshake or placing memory into Self-Refresh. It is assumed that software is already aware that memory context is not impacted by S1 and therefore does not need to check this bit. reset_type=global reset
20	0b RW	**System Reset Status (SRS) (srs):** Processor sets this bit when the PMU_RESETBUTTON_B# button is pressed. BIOS is expected to read this bit and clear it if it is set. This bit is also reset by RSMRST_B and CF9h resets. reset_type=Resume Well Reset#
19	0b RW	**CPU Thermal Trip Status (CTS) (cts):** This bit is set when the processor thermal trip active while the system is in a valid state to honor the pin. This bit is also reset by RSMRST_B and CF9h resets. It is not reset by the shutdown and reboot associated with the thermal trip event. reset_type=Resume Well Reset#

Bit Range	Default & Access	Description
18	0b RW	**Minimum PMU_SLP_S4_B Assertion Width Violation Status (MS4V) (ms4v):** Hardware sets this bit when the PMU_SLP_S4_B assertion width is less than the time programmed in the PMU_SLP_S4_B Minimum Assertion Width field. The processor begins the timer when PMU_SLP_S4_B pin is asserted during S4/S5 entry, or when the RSMRST_B input is deasserted during SUS well power-up. The status bit is cleared by software writing a 1 to the bit. Note that this bit is functional regardless of the value in the PMU_SLP_S4_B Assertion Stretch Enable and the Disable-SLP_X-Stretching-After-SUS-Power-Failure bits. This bit is reset by the assertion of the RSMRST_B pin, but can be set in some cases before the default value is readable. reset_type=RSMRST_B
17	0b RO	**reserved3:** Reserved.
16	0b RW	**COREPWROK Failure (PWR_FLR) (pwr_flr):** Intel processor sets this bit any time COREPWROK goes low if the system was in an S0 or S1 state. The bit will be cleared only by software writing a 1 back to the bit or by SUS well power loss. reset_type=global reset
15	0b RW	**PME B0 S5 Disable (PME_B0_S5_DIS) (pme_b0_s5_dis):** When set to '1', this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = '1'. Wakes from power states other than S5 are not affected by this policy bit. The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below: Y = Wake N = Don't wake B0 = PME_B0_EN OV = WOL Enable Override B0/OV | S1/S3/S4 | S5 00 | N | N 01 | N | Y (LAN only) 11 | Y (all PME B0 sources) | Y (LAN only) 10 | Y (all PME B0 sources) | N This bit is cleared by the SRTCRST_B pin. reset_type=SRTCRST_B
14	1b RW	**SUS Well Power Failure (SUS_PWR_FLR) (sus_pwr_flr):** This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST_B assertion. Software writes a 1 to this bit to clear it. This bit is in the SUS well, and defaults to '1' based on RSMRST_B assertion (not cleared by any type of reset). Implementation Note: RSMRST_B is an asynchronous set term to this bit. reset_type=RSMRST_B
13	0b RW	**WOL Enable Override (WOL_EN_OVRD) (wol_en_ovrd):** When this bit is set to 1, the integrated LAN is enabled to wake the system from S5 regardless of the value in the PME_B0_EN bit in the GPE0a_EN register. This allows the system BIOS to enable Wake-On-LAN regardless of the policies selected through the operating system. This bit is maintained in the RTC power well, therefore permitting WOL following a surprise power failure even in cases in which the system may have been running in S0 without the PME Enables set. (Note that the LAN NVRAM configuration must support WOL after SUS power loss.) When this bit is cleared to 0, the wake-on-LAN policies are determined by OS-visible bits. This bit has no effect on wakes from S1, S3, or S4. This bit is cleared by the SRTCRST_B pin reset_type=SRTCRST_B
12	0b RW	**Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP) (dis_slp_x_strch_sus_up):** When this bit is set to 1, all SLP_* pin stretching is disabled when powering up after a SUS well power loss. When this bit is left at 0, SLP_* stretching will be performed after SUS power failure as enabled in various other fields. Note that if this bit is a 0, SLP_* stretch timers start on SUS well power up (the processor has no ability to count stretch time while the SUS well is powered down). Setting this bit can therefore prevent long delays after SUS power loss which may be common in mobile platforms and in manufacturing flow testing, while still allowing for the full power cycling during S3, S4 and S5 states. If the platform guarantees minimum SUS power down residence in other ways, an additional processor-induced delay is not needed or wanted. This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by the SRTCRST_B pin.
11:10	0b RW	**PMU_SLP_S3_B Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH) (slp_s3_min_asst_wdth):** This 2-bit value indicates the minimum assertion width of the PMU_SLP_S3_B signal to guarantee that the Main power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power failure detection circuits, etc. Settings are: 00: 60 usec 01: 1 ms 10: 50 ms 11: 2 sec This field is not writable when the SLP_Sx# Stretching Policy Lock- Down bit is set. This bit is cleared by the RSMRST_B pin. reset_type=RSMRST_B



Bit Range	Default & Access	Description
9	0b RW	**General Reset Status (GEN_RST_STS) (gen_rst_sts):** This bit is set by hardware whenever PMU_PLTRST asserts for any reason other than going into a software-entered sleep state (via PM1_CNT.SLP_EN write). This bit is an optional tool to help BIOS determine when a reset might have collided with a wake from a valid sleep state. A possible usage model would be to consult and then write a '1' to clear this bit during the boot flow before determing what action to take based on reading PM1_STS.WAK_STS = '1'. If GEN_RST_STS = '1', the cold reset boot path could be followed rather than the resume path, regardless of the setting of WAK_STS. This bit does not affect processor operation in any way, and can therefore be left set if BIOS chooses not to use it. This bit is set by global reset. reset_type=global reset
8	0b RW	**RTC_reserved (rtc_reserved):** reset_type=SRTCRST_B
7:6	0b RW	**SWSMI Rate Select (SWSMI_RATESEL) (swsmi_ratesel):** This 2-bit value indicates when the SWSMI timer will time out. Valid values are: 00 1.5ms +/- 0.6ms 01 16ms +/- 4ms 10 32ms +/- 4ms 11 64ms +/- 4ms These bits are not cleared by any type of reset except SRTCRST_B.
5:4	0b RW	**PMU_SLP_S4_B Minimum Assertion Width (S4MAW) (s4maw):** This 2-bit value indicates the minimum assertion width of the PMU_SLP_S4_B signal to guarantee that the DRAMs have been safely power-cycled. This value may be modified per platform depending on DRAM types, power supply capacitance, etc. Valid values are: - 11: 1 second - 10: 2 seconds - 01: 3 seconds - 00: 4 seconds This value is used in two ways: 1. If the PMU_SLP_S4_B assertion width is ever shorter than this time, a status bit is set for BIOS to read when S0 is entered 2. If enabled by bit 3 in this register, the hardware will prevent the PMU_SLP_S4_B signal from deasserting within this minimum time period after asserting. Note that the logic that measures this time is in the suspend power well. Therefore, when leaving a G3 state, the minimum time is measured from the deassertion of the internal suspend well reset (unless the Disable SLP_X Stretching After SUS Power Failure bit is set). This field is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. SRTCRST_B forces this field to the conservative default state (00b). reset_type=SRTCRST_B
3	0b RW	**PMU_SLP_S4_B Assertion Stretch Enable (S4ASE) (s4ase):** When set to 1, the PMU_SLP_S4_B pin will minimally assert for the time specified in bits 5:4 of this register. This bit is provided so that all DIMMs in the system can deterministically detect a power-cycle event for proper initialization. Note that there are behavioral changes that may be noticeable to the end-user when this bit is set. Resume times from S4 and S5 and power-up times from G3 may be delayed by several seconds. Cases in which this feature may not be desirable and therefore keeping the bit cleared are: - A customer decides the user confusion due to the hardware delay is a bigger issue than the potential DRAM issue - A customer decides the software status bit solution is adequate - A different DRAM type is used or the platform provides an external solution to solve the power-cycling issue - Validation regressions are impacted by the delay (especially after RSMRST_B deassertion) - Avoid potential resume time WHQL violations This bit is not writable when the SLP_Sx# Stretching Policy Lock-Down bit is set. This bit is cleared by SRTCRST_B. reset_type=SRTCRST_B
2	1b RW	**RTC_PWR_STS (RPS) (rps):** Intel processor will set this bit to 1 when RTEST_B indicates a weak or missing battery. The bit will remain set until the software clears it by writing a 0 back to this bit position. This bit is not cleared by any type of reset. reset_type=RTEST_B
1	0b RO	**reserved:** Reserved.
0	0b RW	**AFTERG3_EN (AG3E) (ag3e):** Determines what state to go to when power is reapplied after a power failure (G3 state). 0 = System will return to an S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4-like state). In the S5 state, the only enabled wake-up event is the Power Button or any enabled wake event that was preserved through the power failure. This bit is in the RTC well and is only cleared by SRTCRST_B assertion. reset_type=SRTCRST_B

20.5.6 General PM Configuration 2 (GEN_PMCON2)—Offset 24h

Access Method

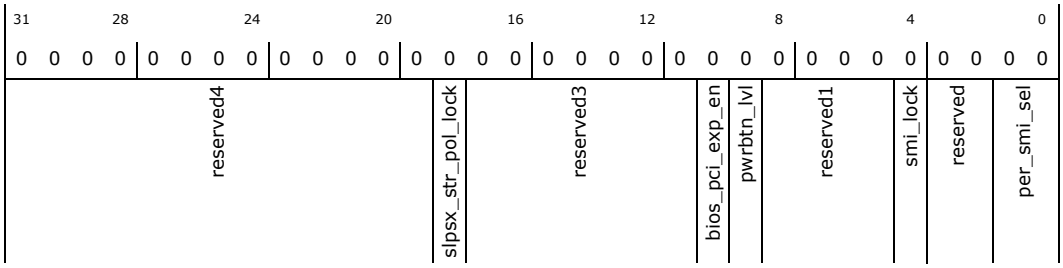
Type: Memory Mapped I/O Register (Size: 32 bits)

GEN_PMCON2: [PMC_BASE_ADDRESS] + 24h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:19	0b RO	**reserved (reserved4):** Reserved.
18	0b RW	**SLP_Sx# Stretching Policy Lock-Down (SLPSX_STR_POL_LOCK) (slpsx_str_pol_lock):** When set to 1, this bit locks down the following fields: - GEN_PMCON_1.DIS_SLP_X_STRCH_SUSPF - GEN_PMCON_1.SLP_S3_MIN_ASST_WDTH - GEN_PMCON_1.S4MAW - GEN_PMCON_1.S4ASE Those bits become read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.
17:11	0b RO	**reserved (reserved3):** Reserved.
10	0b RW	**BIOS PCI Express Enable (BIOS_PCI_EXP_EN) (bios_pci_exp_en):** This bit acts as a global enable for the SCI associated with the PCI express ports. If this bit is not set, then the various PCI Express ports cannot cause the PCI_EXP_STS bit to go active.
9	0b RO	**Power Button Level (PWRBTN_LVL) (pwrbtn_lvl):** This read-only bit indicates the current state of the PMU_PWRBTN_B signal. 1= High, 0 = Low. The value reflected in this bit is the debounced PMU_PWRBTN_B pin value that is seen at the output of a 16ms debouncer.
8:5	0b RO	**reserved (reserved1):** Reserved.
4	0b RW	**SMI Lock (SMI_LOCK) (smi_lock):** When this bit is set, writes to the GBL_SMI_EN bit will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (i.e. once set, this bit can only be cleared by PMU_PLTRST).
3:2	0b RO	**reserved:** Reserved.
1:0	0b RW	**Period SMI Select (PER_SMI_SEL) (per_smi_sel):** Software sets these bits to control the rate at which the periodic SMI# is generated: 00 = 64 seconds (default), 01 = 32 seconds, 10 = 16 seconds, 11 = 8 seconds Tolerance for the timer is +/- 1 second.

20.5.7 MFPMC - Message from PMC (MFPMC)—Offset 28h

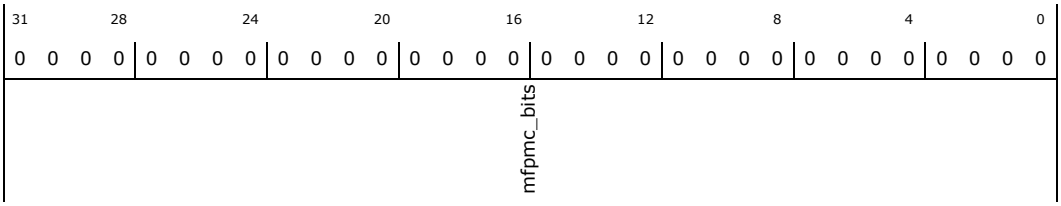
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MFPMC: [PMC_BASE_ADDRESS] + 28h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Message from PMC (MFPMC) (mfpmc_bits):** The data in this register is typically updated in response to a host write to the MTPMC register.

20.5.8 SEC_STS - SEC Status (SEC_STS)—Offset 2Ch

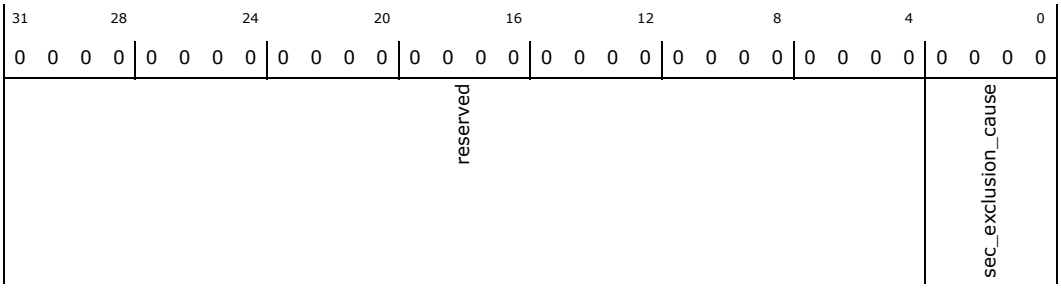
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

SEC_STS: [PMC_BASE_ADDRESS] + 2Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0b RO	**reserved:** Reserved.
3:0	0b RW	**SEC_EXCLUSION_CAUSE (sec_exclusion_cause):** The cause associated with SeC setting requesting exclusion from power flows in SEC_EXCLUSION_REQ field. 0000b: SeC FW Fault Tolerant Initialization failed. 0001b: SeC FLASH Descriptor Override invoked. 0010b: SeC disabled using SW means (such as OEM setting). 0011b: Post-boot SeC applications not supported. 0100b: ROM BIST failure. 0101b: Fuse unit completed with unsupported request for group 1. 0110b: Invalid fuses bit at line 3 of group 1 fuses wasn't written with value 0. 0111b: DRAM Initializaiton by BIOS failed. Other values reserved.

20.5.9 Configured Revision ID (CRID)—Offset 30h

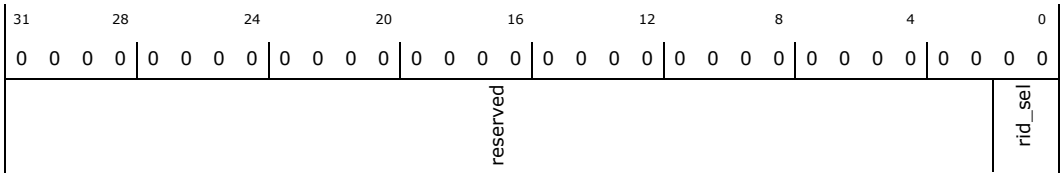
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

CRID: [PMC_BASE_ADDRESS] + 30h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**reserved:** Reserved.
1:0	0b RW	**RID Select(RID_SEL) (rid_sel):** Software writes this field to select the Revision ID reflected in PCI config space. The decoding is: 00 - Revision ID 01 - CRID 0 10 - CRID 1 11 - CRID 2 Once written, this field can only be cleared by a platform reset. reset_type=PMU_PLTRST

20.5.10 Function Disable (FUNC_DIS)—Offset 34h

BIOS uses this register to disable specific function. Upon writing this register PMC will set the corresponding Function Disable bit in the PSF

Access Method

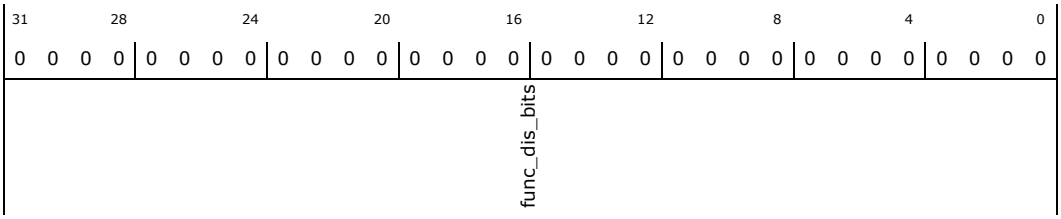
Type: Memory Mapped I/O Register (Size: 32 bits)

FUNC_DIS: [PMC_BASE_ADDRESS] + 34h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**FUNC_DIS_BITS (func_dis_bits):** When a bit is set, the corresponding function should be disabled. : Disable 1'b0: Enable 24 LPSS2_F0_Disable LPSS2 Function0 (DMA) Disable. 1'b1: Disable 1'b0: Enable 23 PCIe_P3_Disable PCIe Port3 Disable. 1'b1: Disable 1'b0: Enable 22 PCIe_P2_Disable PCIe Port2 Disable. 1'b1: Disable 1'b0: Enable 21 PCIe_P1_Disable PCIe Port1 Disable. 1'b1: Disable 1'b0: Enable 20 PCIe_P0_Disable PCIe Port0 Disable. 1'b1: Disable 1'b0: Enable 19 Reserved2 reserved 18 USB_Disable USB2 (EHCI) Disable. 1'b1: Disable 1'b0: Enable 17 SATA_Disable SATA Disable. 1'b1: Disable 1'b0: Enable 16 LAN_Disable LAN Disable. 1'b1: Disable 1'b0: Enable 15 USH_Disable USH Disable. 1'b1: Disable 1'b0: Enable 14 OTG_Disable OTG Disable. 1'b1: Disable 1'b0: Enable 13 HDA_Disable HDA Disable. 1'b1: Disable 1'b0: Enable 11 RESERVED SCC_SDCARD_Disable SDCARD Disable. 1'b1: Disable 1'b0: 1'b1: Disable 1'b0: Enable 7 LPSS1_F7_Disable Reserved for LPSS1 function 7 6 LPSS1_F6_Disable Reserved for LPSS1 function 6 5 LPSS1_F5_Disable PSS1 Function5 (SPI) Disable. 1'b1: Disable 1'b0: Enable 4 LPSS1_F4_Disable LPSS1 Function4 (HSUART#2) Disable. 1'b1: Disable 1'b0: Enable 3 LPSS1_F3_Disable LPSS1 Function3 (HSUART#1) Disable. 1'b1: Disable 1'b0: Enable 2 LPSS1_F2_Disable LPSS1 Function2 (PWM#2) Disable. 1'b1: Disable 1'b0: Enable 1 LPSS1_F1_Disable LPSS1 Function1 (PWM#1) Disable. 1'b1: Disable 1'b0: Enable 0 LPSS1_F0_Disable LPSS1 Function0 (DMA) Disable. 1'b1: Disable 1'b0: Enable

20.5.11 Function Disable 2 (FUNC_DIS_2)—Offset 38h

BIOS uses this register to disable specific function. Upon writing this register PMC will set the corresponding Function Disable bit in the PSF

Access Method

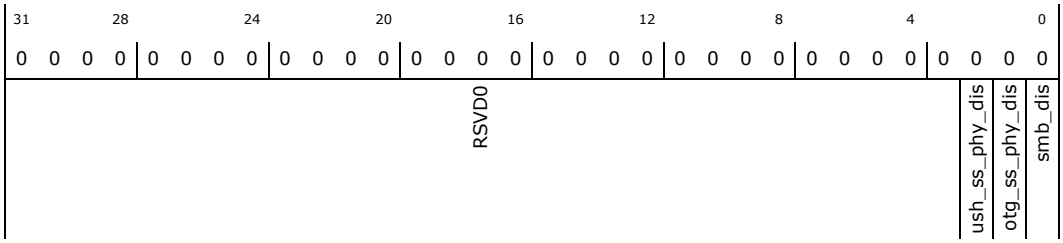
Type: Memory Mapped I/O Register (Size: 32 bits)

FUNC_DIS_2: [PMC_BASE_ADDRESS] + 38h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RO	**RSVD0:** Reserved
2	0b RW	**USH_SS_PHY_DIS (ush_ss_phy_dis):** When this bit is set, USH Super Speed PHY should be disabled.
1	0b RW	**OTG_SS_PHY_DIS (otg_ss_phy_dis):** When this bit is set, OTG Super Speed PHY should be disabled.
0	0b RW	**SMB_DIS (smb_dis):** When this bit is set, SMB function should be disabled.

20.5.12 ETR - Extended Test Mode Register (ETR)—Offset 48h

This register resides in the resume well. All bits except bit[23:16] are reset by internal Resume Well Reset. Bit[23:16] are reset by RSMRST_B only.

Access Method

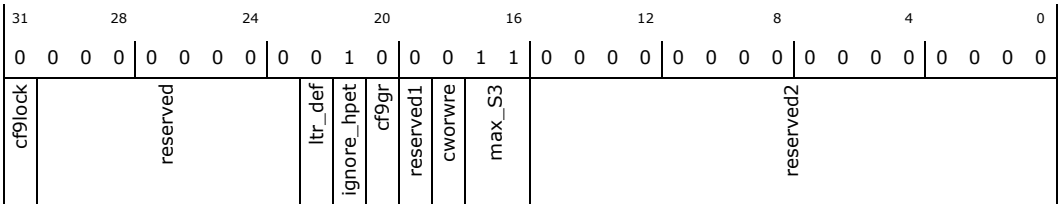
Type: Memory Mapped I/O Register (Size: 32 bits)

ETR: [PMC_BASE_ADDRESS] + 48h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00230000h



Bit Range	Default & Access	Description
31	0b RW	**CF9h Lockdown (CF9LOCK) (cf9lock):** When set, this will lock the CF9h-Global-Reset bit. When set, this register locks itself. This register is reset by a CF9h reset.
30:23	0b RO	**reserved:** Reserved.
22	0b RW	**LTR default (LTR_DEF) (ltr_def):** When this bit is cleared, PMC will assume low LTR by default. When set, PMC will assume high LTR by default
21	1b RW	**Ignore HPET When going to S3 (IGNORE_HPET) (ignore_hpet):** When this bit is set, PMC will not check for HPET disabled before going to S3
20	0b RW	**CF9h Global Reset (CF9GR) (cf9gr):** When this bit is set, a CF9h write of 6h or Eh will cause a Global Reset of the Host partition. If this bit is cleared, a CF9h write of 6h or Eh will only reset the Host partition. It is recommended that BIOS should set this bit early on in the boot sequence, and then clear it and set the CF9LOCK bit prior to loading the OS. When this bit is set, the hardware assumes that bit 18 (CF9h Without Resume Well Reset Enable) is cleared. This register is locked by the CF9 Lockdown (CF9LOCK) bit. This register is not reset by a CF9h reset. reset_type=RSMRST_B
19	0b RO	**reserved (reserved1):** Reserved.
18	0b RW	**CF9h Without Resume Well Reset Enable (CWORWRE) (cworwre):** When this bit is set, a CF9h write of 6h or Eh will not cause internal Resume Well Reset (WrsmrstB) to be asserted and thus resume well logic will maintain its state. When this bit is cleared, CF9h write of 6h or Eh will also reset resume well logic. This bit is to be used when a second reset through CF9 write is desired upon power up or after resume from low power states. This bit has to be set prior to the write to CF9 register and has to be cleared upon completing the reset. Failing to do so prevents resume well registers from being reset in the future CF9 writes. reset_type=RSMRST_B
17:16	11b RW	**MAX_S3 (MAX_S3 (max_S3):** Indicated the maximum S3 state processor can go
15:0	0b RO	**reserved (reserved2):** Reserved.

20.5.13 VLT - Voltage Detect Register (VLT)—Offset 50h

This register reflects the Voltage detect fuses.

Access Method

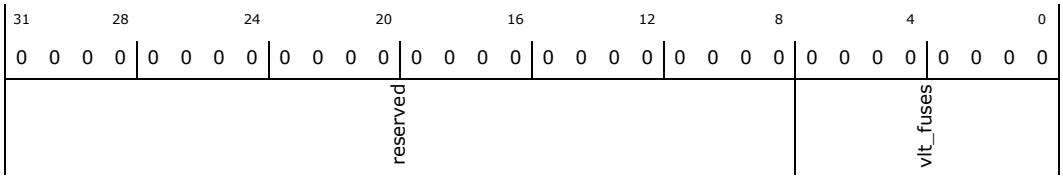
Type: Memory Mapped I/O Register (Size: 32 bits)

VLT: [PMC_BASE_ADDRESS] + 50h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RO	**VLT Fuses (VLT_FUSES) (vlt_fuses):** These bits reflects the Voltage detect fuses

20.5.14 GPIO_ROUT - GPIO_ROUT register (GPIO_ROUT)—Offset 58h

Access Method

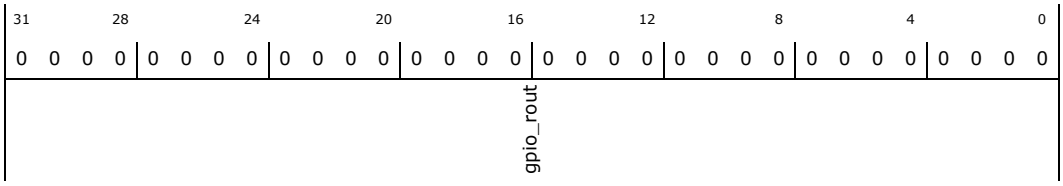
Type: Memory Mapped I/O Register (Size: 32 bits)

GPIO_ROUT: [PMC_BASE_ADDRESS] + 58h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**GPIO Rout (GPIO_ROUT) (gpio_rout):** Bits [15:0] determines GPIO SUS events rout. Bits [31:16] determines GPIO CORE events rout. Bits [1:0] determines GPIO SUS event 0. Bits [3:2] determines GPIO SUS event 1 and so on. Bits [17:16] determines GPIO CORE event 0. Bits [19:18] determines GPIO CORE event 1 and so on. If the corresponding GPIO is implemented and is set to an input, a '1' in the GP_LVL bit can be routed to cause an interrupt. If the GPIO is not set to an input, this field has no effect. * 00 No effect (or GPIO unimplemented), * 01 SMI# (if corresponding ALT_GPIO_SMI bit also set), * 10 SCI (if corresponding GPE0a_EN bit also set), * 11 Reserved If the system is in an S0-S5 state and if the GPE0a_EN bit is also set, then the GPIO can cause a Wake event, even if the GPIO is NOT routed to cause an interrupt. Exception: If the system is in S5 state due to a powerbutton override, then the GPIO's will not cause wake events. Note: Core well GPIO's are not capable of waking the system from sleep states where the core well is not powered.

20.5.15 PLT_CLK_CTL_0 - Platform Clock Control 0 (PLT_CLK_CTL_0)—Offset 60h

This register controls Platform clocks.

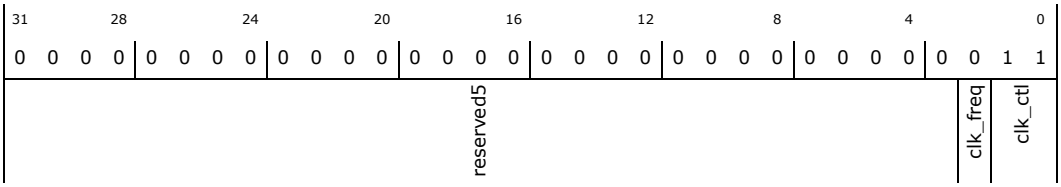
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_0: [PMC_BASE_ADDRESS] + 60h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

20.5.16 PLT_CLK_CTL_1 - Platform Clock Control 1 (PLT_CLK_CTL_1)—Offset 64h

This register controls Platform clocks.

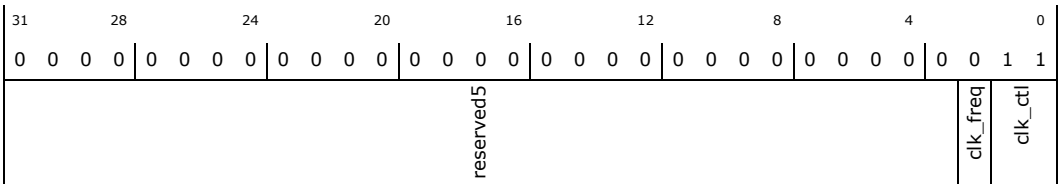
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_1: [PMC_BASE_ADDRESS] + 64h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.

Bit Range	Default & Access	Description
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

20.5.17 PLT_CLK_CTL_2 - Platform Clock Control 2 (PLT_CLK_CTL_2)—Offset 68h

This register controls Platform clocks.

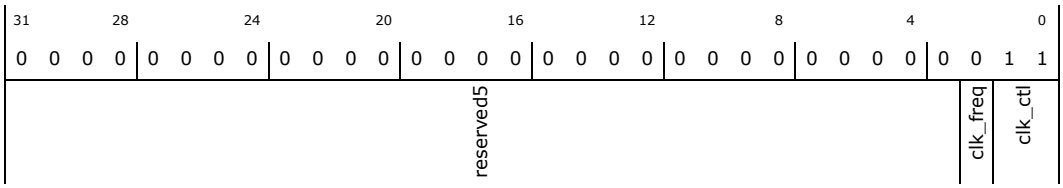
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_2: [PMC_BASE_ADDRESS] + 68h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

20.5.18 PLT_CLK_CTL_3 - Platform Clock Control 3 (PLT_CLK_CTL_3)—Offset 6Ch

This register controls Platform clocks.

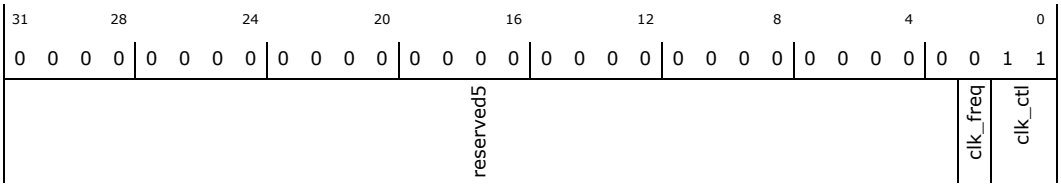
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_3: [PMC_BASE_ADDRESS] + 6Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

20.5.19 PLT_CLK_CTL_4 - Platform Clock Control 4 (PLT_CLK_CTL_4)—Offset 70h

This register controls Platform clocks.

Access Method

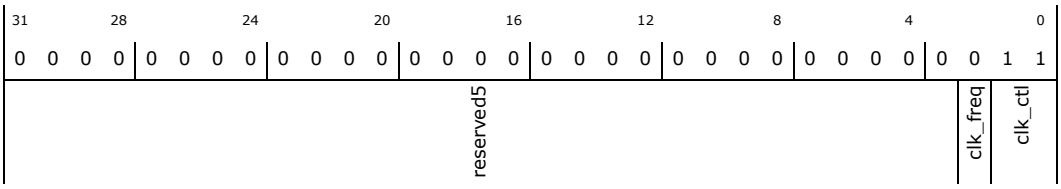
Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_4: [PMC_BASE_ADDRESS] + 70h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

20.5.20 PLT_CLK_CTL_5 - Platform Clock Control 5 (PLT_CLK_CTL_5)—Offset 74h

This register controls Platform clocks.

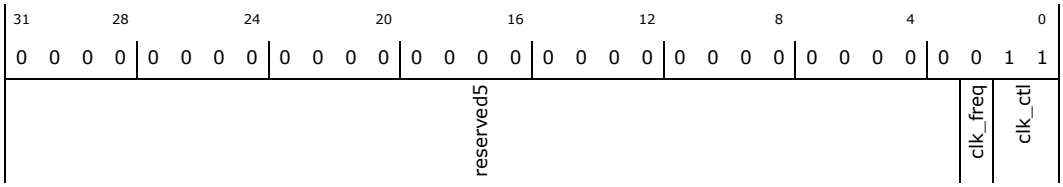
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PLT_CLK_CTL_5: [PMC_BASE_ADDRESS] + 74h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved (reserved5):** Reserved.
2	0b RW	**CLK_FREQ (Clock frequency) (clk_freq):** This field controls clock frequency: 0 - 25 MHz (XTAL), 1: 19.2 (PLL)
1:0	11b RW	**CLK_CTL (Clock control) (clk_ctl):** This field controls clock gating: 00 - gated on D3, 01 - force on, 1* - force off

20.5.21 S0IR_TMR - S0I Ready Residency Timer (S0IR_TMR)—Offset 80h

This timer acumulates time spent in S0I Ready state

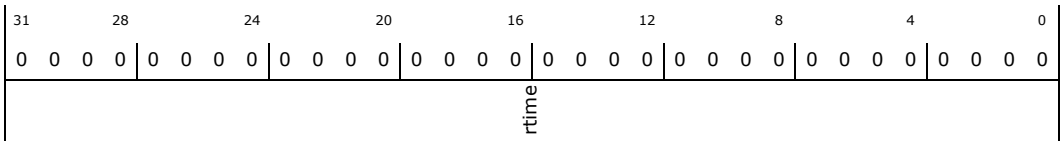
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

S0IR_TMR: [PMC_BASE_ADDRESS] + 80h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0I Ready state, in units of 32 uS

20.5.22 S3_TMR - S3 Residency Timer (S3_TMR)—Offset 84h

This timer acumulates time spent in S3 state

Access Method

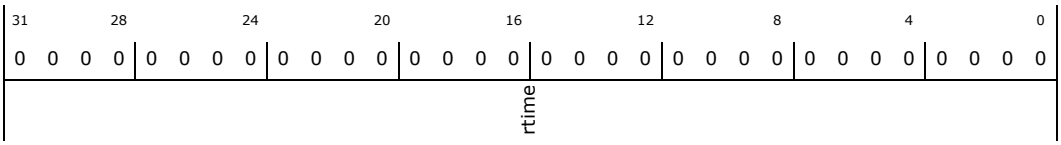
Type: Memory Mapped I/O Register (Size: 32 bits)

S3_TMR: [PMC_BASE_ADDRESS] + 84h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S3 state, in units of 32 uS

20.5.23 S3_TMR - S3 Residency Timer (S3_TMR)—Offset 88h

This timer acumulates time spent in S3 state

Access Method

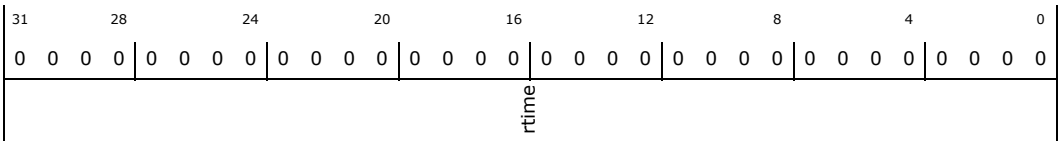
Type: Memory Mapped I/O Register (Size: 32 bits)

S3_TMR: [PMC_BASE_ADDRESS] + 88h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S3 state, in units of 32 uS

20.5.24 S3_TMR - S3Residency Timer (S3_TMR)—Offset 8Ch

This timer acumulates time spent in S3state

Access Method

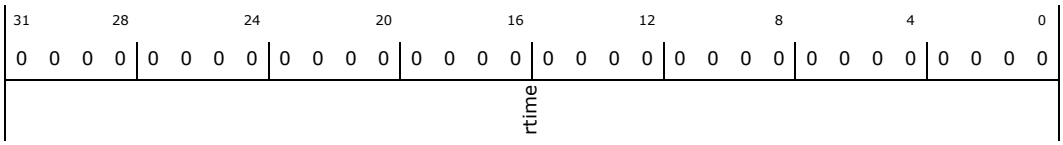
Type: Memory Mapped I/O Register (Size: 32 bits)

S3_TMR: [PMC_BASE_ADDRESS] + 8Ch

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S3state, in units of 32 uS

20.5.25 S0_TMR - S0 Residency Timer (S0_TMR)—Offset 90h

This timer acumulates time spent in S0 state

Access Method

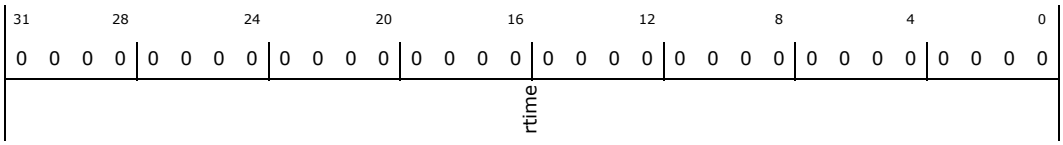
Type: Memory Mapped I/O Register (Size: 32 bits)

S0_TMR: [PMC_BASE_ADDRESS] + 90h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**RTIME (Residency Time) (rtime):** time spent in S0 state, in units of 32 uS

20.5.26 PSS - Power island Power Status (PSS)—Offset 98h

This register reflects the power status for each physical power island controlled by PMC. note it doesnt reflect the tap override values

Access Method

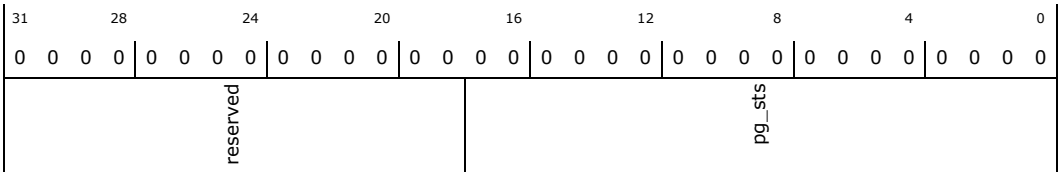
Type: Memory Mapped I/O Register (Size: 32 bits)

PSS: [PMC_BASE_ADDRESS] + 98h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:18	0b RO	**reserved:** Reserved.
17:0	0b RO	**PG_STS (POWER GATE status) (pg_sts):** reflects the power gate status of all power islands 0 - power island is powered on. 1 - power island is powered off bits mapping: 0 - GBE 1 - SATA 2 - HDA 3 - SEC 4 - PCIE 5 - LPSS 6 - DFX 8 - USH control 9 - USH SUS 10 - USH VCCS 11 - USH VCCA 12 - OTG control 13 - OTG VCCS 14 - OTG VCCACLK 15 - OTG VCCA 16 - USB 17 - USB SUS

20.5.27 D3_STS_0 - D3 Status register 0 (D3_STS_0)—Offset A0h

This register reflects D3 status of functions

Access Method

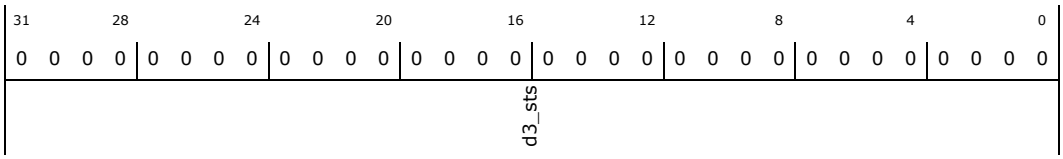
Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STS_0: [PMC_BASE_ADDRESS] + A0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - LPSS 0 function 0 1 - LPSS 0 function 1 2 - LPSS 0 function 2 3 - LPSS 0 function 3 4 - LPSS 0 function 4 5 - LPSS 0 function 5 6 - LPSS 0 function 6 7 - LPSS 0 function 7 8 - SCC function 0 9 - SCC function 1 10 - SCC function 2 11 - RESERVED - HDA 13 - OTG 15 - USH 16 - GBE 17 - SATA 18 - USB 19 - SEC 20 - PCIE function 0 21 - PCIE function 1 22 - PCIE function 2 23 - PCIE function 3 24 - LPSS 1 function 0 25 - LPSS 1 function 1 26 - LPSS 1 function 2 27 - LPSS 1 function 3 28 - LPSS 1 function 4 29 - LPSS 1 function 5 30 - LPSS 1 function 6 31 - LPSS 1 function 7

20.5.28 D3_STS_1 - D3 Status register 1 (D3_STS_1)—Offset A4h

This register reflects D3 status of functions

Access Method

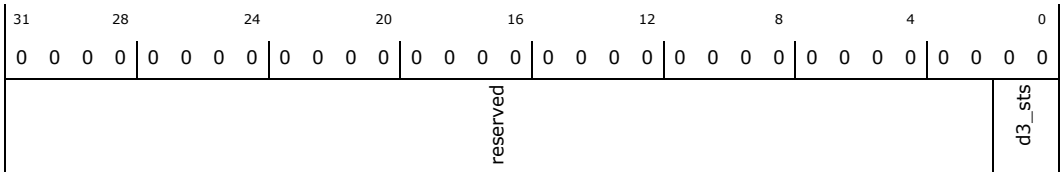
Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STS_1: [PMC_BASE_ADDRESS] + A4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**reserved:** Reserved.
1:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - SMB 1 - USH Super speed PHY 2 - OTG Super speed PHY 3 - DFX

20.5.29 D3_STDBY_STS_0 - D3 Standby Status register 0 (D3_STDBY_STS_0)—Offset A8h

This register reflects D3 status of functions at the moment standby ready message received

Access Method

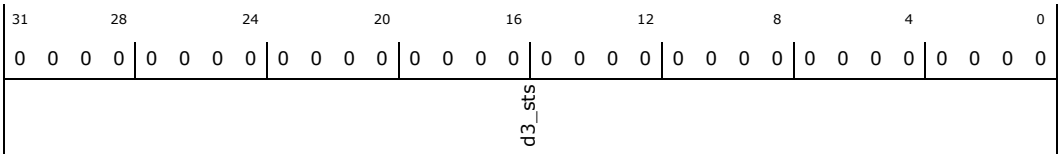
Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STDBY_STS_0: [PMC_BASE_ADDRESS] + A8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - LPSS 0 function 0 1 - LPSS 0 function 1 2 - LPSS 0 function 2 3 - LPSS 0 function 3 4 - LPSS 0 function 4 5 - LPSS 0 function 5 6 - LPSS 0 function 6 7 - LPSS 0 function 7 8 - SCC function 0 9 - SCC function 1 10 - SCC function 2 11 - RESERVED - HDA 13 - OTG 15 - USH 16 - GBE 17 - SATA 18 - HDA 19 - SEC 20 - PCIE function 0 21 - PCIE function 1 22 - PCIE function 2 23 - PCIE function 3 24 - LPSS 1 function 0 25 - LPSS 1 function 1 26 - LPSS 1 function 2 27 - LPSS 1 function 3 28 - LPSS 1 function 4 29 - LPSS 1 function 5 30 - LPSS 1 function 6 31 - LPSS 1 function 7

20.5.30 D3_STDBY_STS_1 - D3 Standby Status register 1 (D3_STDBY_STS_1)—Offset ACh

This register reflects D3 status of functions at the moment Standby Ready Message was received

Access Method

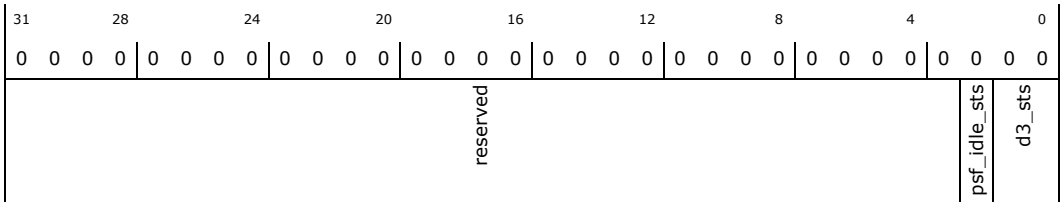
Type: Memory Mapped I/O Register (Size: 32 bits)

D3_STDBY_STS_1: [PMC_BASE_ADDRESS] + ACh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:3	0b RO	**reserved:** Reserved.
1:0	0b RO	**D3_STS (D3 status) (d3_sts):** reflects D3 status of the following functions. 0 - Function is in D0. 1 - Function is in D3 bits mapping: 0 - SMB 1 - USH Super speed PHY 2 - OTG Super speed PHY 3 - DFX

20.5.31 MTPMC_1 - Message to PMC 1 (MTPMC_1)—Offset B0h

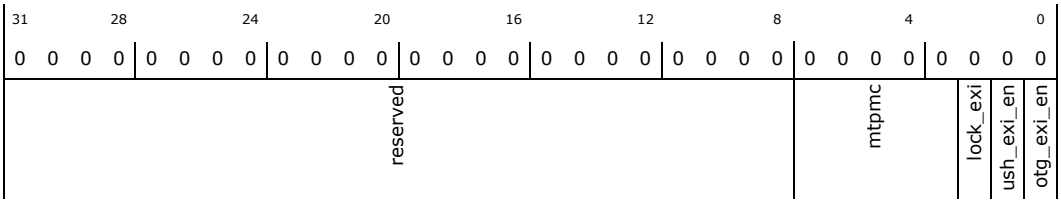
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC_1: [PMC_BASE_ADDRESS] + B0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:3	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS
2	0b RW	**LOCK EXI (lock_exi):** This field locks the ush_exi_en and otg_exi_en fields. The lock is soft lock, meaning register value will be changed but FW will keep the value on inturnal register GP1[2] until warm reset
1	0b RW	**USH_EXI_Enable (ush_exi_en):** A write to this field causes an interrupt to the PMC. The PMC FW will read the contents of this register and will set pcu_ush_exi_enable_xttnfwh signal. The host must wait until the PMC has taken action, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS. This field will be copied to FW internal register and it will hold the value until global reset.
0	0b RW	**OTG_EXI_Enable (otg_exi_en):** A write to this field causes an interrupt to the PMC. The PMC FW will read the contents of this register and will set pcu_otg_exi_enable_xttnfwh signal. The host must wait until the PMC has taken action, as indicated by the PMC Message Full Status (PMC_MSG_1_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS. This field will be copied to FW internal register and it will hold the value until global reset

20.5.32 MTPMC_2 - Message to PMC 2 (MTPMC_2)—Offset B4h

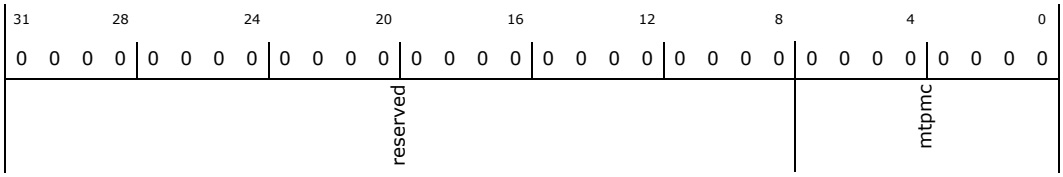
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC_2: [PMC_BASE_ADDRESS] + B4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_2_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

20.5.33 MTPMC_3 - Message to PMC 3 (MTPMC_3)—Offset B8h

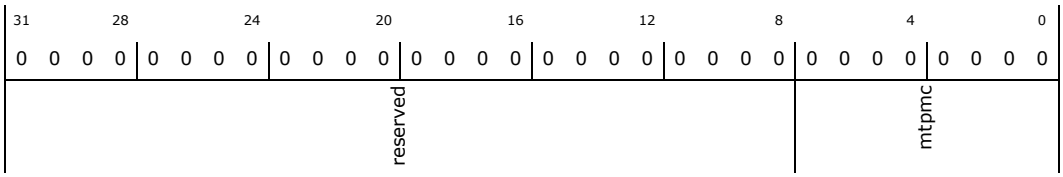
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC_3: [PMC_BASE_ADDRESS] + B8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_3_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

20.5.34 MTPMC_4 - Message to PMC 4 (MTPMC_4)—Offset BCh

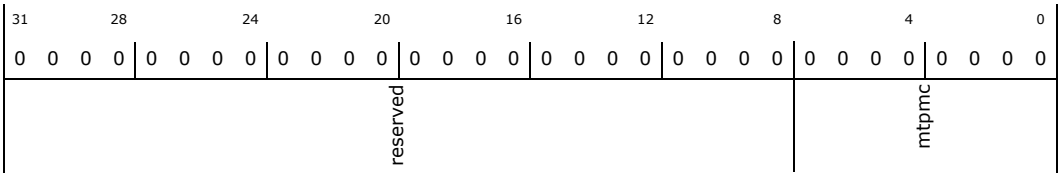
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

MTPMC_4: [PMC_BASE_ADDRESS] + BCh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**reserved:** Reserved.
7:0	0b RW	**Message to PMC (MTPMC) (mtpmc):** A write to this field causes an interrupt to the PMC. The PMC can read the contents of this register. The host must wait until the PMC has taken action on the previous write to MTPMC, as indicated by the PMC Message Full Status (PMC_MSG_4_FULL_STS) bit being cleared, before initiating another write to the MTPMC register. time spent in S0 state, in units of 32 uS

20.5.35 PME Status 0 – Status bit for PME messages (PME_STS)—Offset C0h

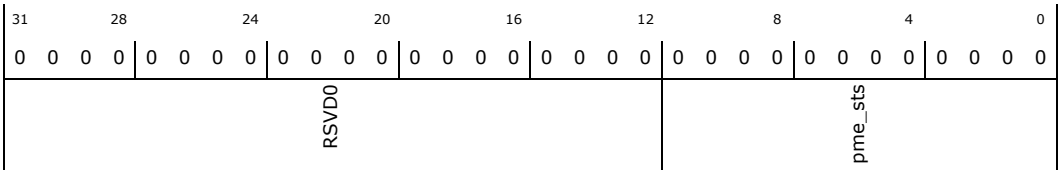
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

PME_STS: [PMC_BASE_ADDRESS] + C0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11:0	0b RO	**PME Status (pme_sts):** when set PME was recived from the following agents 0 = GBE 1 = HDA 2 = SATA 3 = SCCSDIO 4 = SCCSDCARD 5 = LPSDIO1; 6 = SECEP 7 = LPSDIO2 9 = OTG 10 = SCCEMMC 11 = RESERVED

20.5.36 GPE Level Edge mode (GPE_LEVEL_EDGE)—Offset C4h

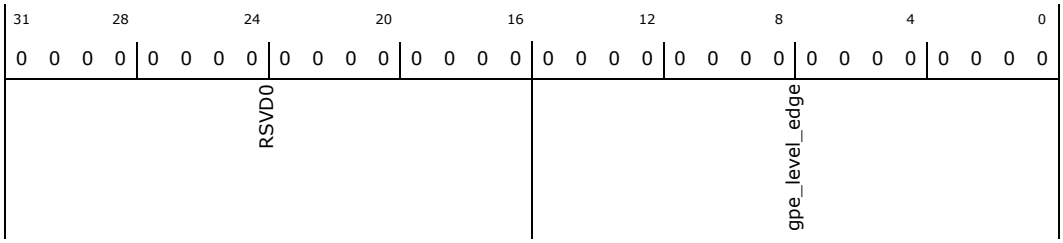
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPE_LEVEL_EDGE: [PMC_BASE_ADDRESS] + C4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0b RW	**Edge Level mode (gpe_level_edge):** When set GPE is in level mode when clear GPE is in edge mode gpe_level_edge[15:8] used for GPIO Core gpe_level_edge[7:0] used for GPIO SUS

20.5.37 GPE polarity mode (GPE_POLARITY)—Offset C8h

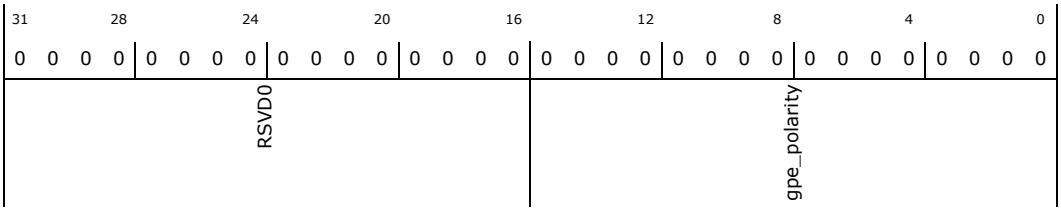
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

GPE_POLARITY: [PMC_BASE_ADDRESS] + C8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:0	0b RW	**Polarity (gpe_polarity):** When set GPE is active high when clear GPE is active low gpe_polarity[15:8] used for GPIO Core gpe_polarity[7:0] used for GPIO SUS

20.5.38 Lock Register (LOCK)—Offset CCh

Register Field Lock bit ---------- GEN_PMCON1 PME_B0_S5_DIS LOCK.Sx_WAKE GEN_PMCON1 WOL_EN_OVRD LOCK.Sx_WAKE GEN_PMCON1 AG3E LOCK.Sx_WAKE GEN_PMCON2 BIOS_PCI_EXP_EN LOCK.PCIE GEN_PMCON2 PER_SMI_SEL LOCK.PER_SMI FUNC_DIS all LOCK.FUNC_DIS FUNC_DIS_2 all ETR MAX_S3 LOCK.SOIX GPIO_ROUT all LOCK.GPIO_ROUT PLT_CLK_CTL_0 all LOCK.PLT_CLK PLT_CLK_CTL_1 all LOCK.PLT_CLK PLT_CLK_CTL_2 all LOCK.PLT_CLK PLT_CLK_CTL_3 all LOCK.PLT_CLK PLT_CLK_CTL_4 all LOCK.PLT_CLK PLT_CLK_CTL_5 all LOCK.PLT_CLK

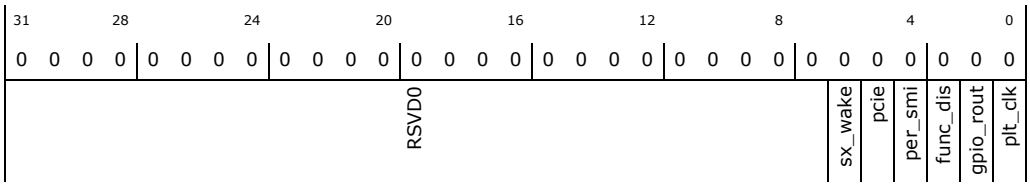
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

LOCK: [PMC_BASE_ADDRESS] + CCh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:7	0b RO	**RSVD0:** Reserved
6	0b RW	**SX_WAKE lock (sx_wake):** Reserved.
5	0b RW	**PCIE lock (pcie):** Reserved.
4	0b RW	**PER_SMI lock (per_smi):** Reserved.
3	0b RW	**FUNC_DIS (func_dis):** Reserved.
1	0b RW	**GPIO_ROUT lock (gpio_rout):** Reserved.
0	0b RW	**PLT_CLK lock (plt_clk):** Reserved.

20.5.39 Virtual UART register (VUART1)—Offset D0h

Access Method

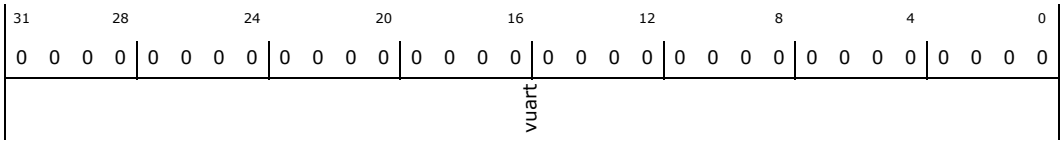
Type: Memory Mapped I/O Register (Size: 32 bits)

VUART1: [PMC_BASE_ADDRESS] + D0h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

20.5.40 Virtual UART register (VUART2)—Offset D4h

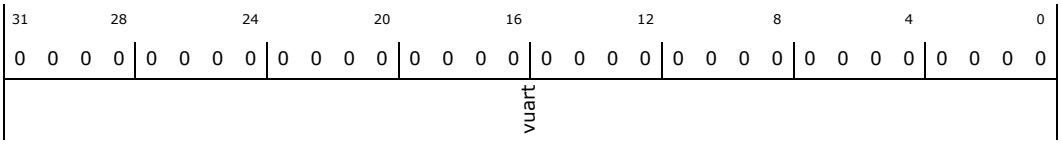
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VUART2: [PMC_BASE_ADDRESS] + D4h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

20.5.41 Virtual UART register (VUART3)—Offset D8h

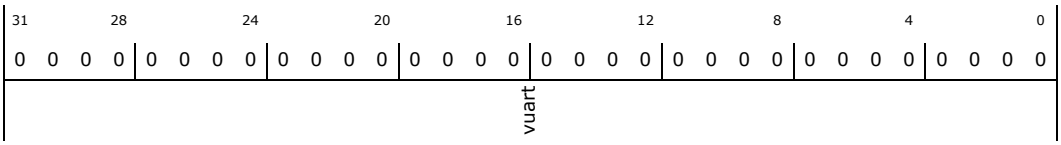
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VUART3: [PMC_BASE_ADDRESS] + D8h

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

20.5.42 Virtual UART register (VUART4)—Offset DCh

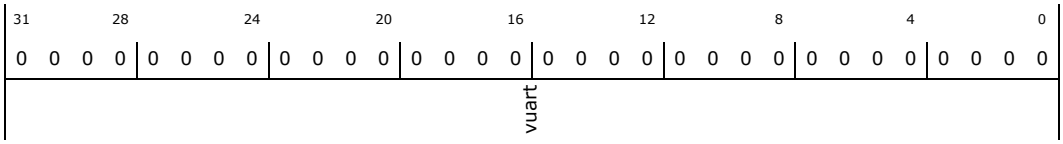
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

VUART4: [PMC_BASE_ADDRESS] + DCh

PMC_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
PMC_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0b RW	**Virtual UART register (vuart):** Reserved.

20.6 PCU PMC IO Registers

Table 151. Summary of PCI iLB PMC I/O Registers

Offset	Size	Register ID—Description	Default Value
92h	1	"PORT92: Init Register (PORT92)—Offset 92h" on page 1023	00h
B2h	1	"APM Register (APM)—Offset B2h" on page 1024	00h
B3h	1	"APM_STS Register (APM_STS)—Offset B3h" on page 1024	00h
CF9h	1	"RST_CNT: Reset Control Register (RST_CNT)—Offset CF9h" on page 1025	00h

20.6.1 PORT92: Init Register (PORT92)—Offset 92h

Access Method

Type: I/O Register
(Size: 8 bits)

PORT92: 92h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
reserved						alt_a20_gate	init_now

Bit Range	Default & Access	Description
7:2	0b RO	**reserved:** Reserved.
1	0b RW	**ALT_A20_GATE - Alternate A20 Gate (alt_a20_gate):** Legacy bit - kept just in case DOS expects it to be read/write
0	0b RW	**INIT_NOW (init_now):** When this bit transitions from a 0 to a 1, PMC will sent an INIT# VLW to T-Unit

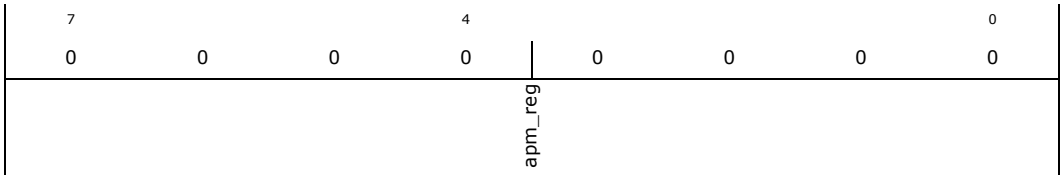
20.6.2 APM Register (APM)—Offset B2h

Access Method

Type: I/O Register
(Size: 8 bits)

APM: B2h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**APM_Register (apm_reg):** TBD

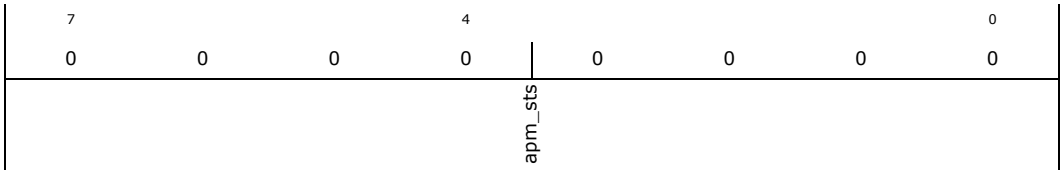
20.6.3 APM_STS Register (APM_STS)—Offset B3h

Access Method

Type: I/O Register
(Size: 8 bits)

APM_STS: B3h

Default: 00h



Bit Range	Default & Access	Description
7:0	0b RW	**APM_STS (apm_sts):** Advanced Power Managment Status Port. used to pass data between the OS and the SMI handler. Basically, this is scratchpad register and is not effected by any other register or function (other than a PCI reset)

20.6.4 RST_CNT: Reset Control Register (RST_CNT)—Offset CF9h

Access Method

Type: I/O Register
(Size: 8 bits)

RST_CNT: CF9h

Default: 00h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
reserved				full_rst	rst_cpu	sys_rst	reserved1

Bit Range	Default & Access	Description
7:4	0b RO	**reserved:** Reserved.
3	0b RW	**Full Reset (FULL_RST) (full_rst):** When this bit is set to 1 and bit 1 is set to 1 (indicating Hard Reset, not Soft Reset), and the RST_CPU bit (bit 2) is written from 0 to 1, the PMC will do a full reset, including driving PMU_SLP_S3_B and PMU_SLP_S4_B active (low) for at least 3 (and no more than 5) seconds. When this bit is set, it also causes the full power cycle (PMU_SLP_S3/4_B assertion) in response to PMU_RESETBUTTON_B, COREPWROK, and Watchdog timer reset sources.
2	0b RW	**Reset CPU (RST_CPU) (rst_cpu):** This bit will cause either a hard or soft reset to the CPU depending on the state of the SYS_RST bit (bit 1 in this same register). The software will cause the reset by setting bit 2 from a 0 to a 1.
1	0b RW	**System Reset (SYS_RST) (sys_rst):** Ths bit determines the type of reset caused via RST_CPU (bit 2 of this register). If SYS_RST is 0 when RST_CPU goes from 0 to 1, then the PMC will force INIT# active for 16 PCI clocks. If SYS_RST is 1 when RST_CPU goes from 0 to 1, then the PMC will force PCI reset active for about 1 ms, however the PMU_SLP_S3_B and PMU_SLP_S4_B signals assertion is dependent on the value of the FULL_RST (bit3 of this register).
0	0b RO	**reserved1:** Reserved.

20.7 PCU iLB PMC I/O Registers

Table 152. Summary of PCU iLB PMC I/O Registers—ACPI_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"PM1_STS_EN - Power Management 1 Status and enable (PM1_STS_EN)—Offset 0h" on page 1027	00000000h
4h	4	"PM1_CNT - Power Management 1 Control (PM1_CNT)—Offset 4h" on page 1029	00000000h
8h	4	"PM1_TMR - Power Management 1 Timer (PM1_TMR)—Offset 8h" on page 1030	00000000h
20h	4	"GPE0a_STS - General Purpose Event 0 Status (GPE0a_STS)—Offset 20h" on page 1031	00000000h
28h	4	"GPE0a_EN - General Purpose Event 0 Enables (GPE0a_EN)—Offset 28h" on page 1033	00000000h
30h	4	"SMI_EN - SMI Control and Enable (SMI_EN)—Offset 30h" on page 1035	00000002h
34h	4	"SMI_STS - SMI Status Register (SMI_STS)—Offset 34h" on page 1036	00000000h
38h	4	"ALT_GPIO_SMI - Alternate GPIO SMI Status and Enable Register. (ALT_GPIO_SMI)—Offset 38h" on page 1038	00000000h
3Ch	4	"UPRWC - USB Per-Port Registers Write Control (UPRWC)—Offset 3Ch" on page 1039	00000000h
40h	4	"GPE_CTRL - General Purpose Event Control (GPE_CTRL)—Offset 40h" on page 1040	00000000h
50h	4	"PM2A_CNT_BLK - PM2a Control Block (PM2A_CNT_BLK)—Offset 50h" on page 1041	00000000h
60h	4	"TCO_RLD: TCO Reload Register (TCO_RLD)—Offset 60h" on page 1041	00000000h
64h	4	"TCO_STS: TCO Timer Status (TCO_STS)—Offset 64h" on page 1042	00000000h
68h	4	"TCO1_CNT: TCO Timer Control (TCO1_CNT)—Offset 68h" on page 1042	00000000h
70h	4	"TCO_TMR: TCO Timer Register (TCO_TMR)—Offset 70h" on page 1043	00040000h

20.7.1 PM1_STS_EN - Power Management 1 Status and enable (PM1_STS_EN)—Offset 0h

Access Method

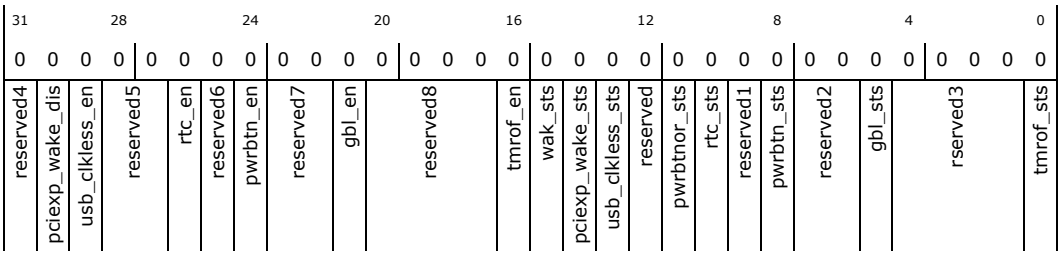
Type: I/O Register (Size: 32 bits)

PM1_STS_EN: [ACPI_BASE_ADDRESS] + 0h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RO	**reserved4:** Reserved.
30	0b RW	**PCI Express Wake Disable (PCIEXP_WAKE_DIS) (pciexp_wake_dis):** This bit disables the inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register from waking the system. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit. reset_type=Resume Well Reset#
29	0b RW	**USB clockless Wake Enable (USB_CLKLESS_EN) (usb_clkless_en):** This bit enables the inputs to the USB_CLKLESS_STS bit in the PM1 Status register to wake the system. Modification of this bit has no impact on the value of the USB_CLKLESS_STS bit. reset_type=Resume Well Reset#
28:27	0b RO	**reserved5:** Reserved.
26	0b RW	**RTC Alarm Enable (RTC_EN) (rtc_en):** This is the RTC alarm enable bit. It works in conjunction with the SCI_EN bit: RTC_EN SCI_EN Effect when RTC_STS is set 0 x No SMI# or SCI. If system was in S1-S5, no wake even occurs. 1 0 SMI#. If system was in S1-S5, then a wake event occurs before the SMI#. 1 1 SCI. If system was in S1-S5, then a wake event occurs before the SCI. Note: This bit needs to be backed by the RTC well to allow an RTC event to wake after a power failure. In addition to being reset by SRTCRST_B assertion, PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
25	0b RO	**reserved6:** Reserved.
24	0b RW	**Power Button Enable (PWRBTN_EN) (pwrbtn_en):** This bit is the power button enable. It works in conjunction with the SCI_EN bit: PWRBTN_EN SCI_EN Effect when PWRBTN_STS is set 0 x No SMI# or SCI. 1 0 SMI#. 1 1 SCI. NOTE: PWRBTN_EN has no effect on the PWRBTN_STS bit being set by the assertion of the power button. The Power Button is always enabled as a Wake event. reset_type=Resume Well Reset#
23:22	0b RO	**reserved7:** Reserved.
21	0b RW	**Global Enable (GBL_EN) (gbl_en):** The global enable bit. When both the GBL_EN and the GBL_STS are set, PMC generates an SCI. reset_type=PMU_PLTRST_B
20:17	0b RO	**reserved8:** Reserved.

Bit Range	Default & Access	Description
16	0b RW	**Timer Overflow Interrupt Enable (TMROF_EN) (tmrof_en):** This is the timer overflow interrupt enable bit. It works in conjunction with the SCI_EN bit: TMROF_EN SCI_EN Effect when TMROF_STS is set 0 x No SMI# or SCI. . 1 0 SMI#. 1 1 SCI. reset_type=PMU_PLTRST_B
15	0b RW	**Wake Status (WAK_STS) (wak_sts):** This bit is set when the system is in one of the Sleep states (via the SLP_EN bit) and an enabled Wake event occurs. Upon setting this bit, the PMC will transition the system to the ON state. This bit can only be set by hardware and can only be cleared by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If a power failure occurs (such as removed batteries) without the SLP_EN bit set, the WAK_STS bit will not be set when the power returns if the AFTER_G3 bit is 0. If the AFTER_G3 bit is 1, then the WAK_STS bit will be set after waking from a power failure. If necessary, the BIOS can clear the WAK_STS bit in this case This is based on discussions with Microsoft. That behavior is not in the ACPI spec. reset_type=RSMRST_B
14	0b RW	**PCI Express Wake Status (PCIEXP_WAKE_STS) (pciexp_wake_sts):** This bit is set by hardware to indicate that the system woke due to a PCI Express wakeup event. This event can be caused by the PCI Express WAKE# pins (PMU_WAKE_B, PCI_WAKE1_B, PCI_WAKE2_B, PCI_WAKE3_B) being active, or one or more of the PCI Express ports being in beacon state, or recept of a PCI Express PME message at root port. This bit should only be set when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independant of the PCIEXP_WAKE_DIS bit. Software writes a 1 to clear this bit. If one of the WAKE# pins is still active during the write or one or more PCI Express ports is in the beacon state or PME message received indication is not cleared in the root port, then the bit will remain Power Management active (i.e. all inputs to this bit are level sensitive) Note: This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus if the bit is 1 and the system is put into a sleeping state, the system will not auatomatically wake. reset_type=pmc_global_rst_b
13	0b RW	**USB clockless Wake Status (USB_CLKLESS_STS) (usb_clkless_sts):** This bit is set by hardware to indicate that the system woke due to change in USB serial lines. This bit is set independant of the USB_CLKLESS_EN bit. Software writes a 1 to clear this bit. reset_type=pmc_global_rst_b
12	0b RO	**reserved:** Reserved.
11	0b RW	**Power Button Override (PWRBTNOR_STS) (pwrbtnor_sts):** This bit is set any time a Power Button Override Event occurs (i.e. the power button is pressed for at least 4 consecutive seconds), or due to an internal thermal sensor catastrophic condition. These events cause an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets via CF9h writes, and is not reset by RSMRST_B. Thus, this bit is preserved through power failures. Note that this bit is still asserted when the global SCI_EN is set to '1' then an SCI will be generated. reset_type=SRTCRST_B
10	0b RW	**RTC Status (RTC_STS) (rtc_sts):** This bit is set when the RTC generates an alarm (assertion of the IRQ8# signal), and is not affected by any other enable bit. See RTC_EN for the effect when RTC_STS goes active. This bit is only set by hardware and can only be reset by writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. reset_type=RSMRST_B
9	0b RO	**reserved1:** Reserved.
8	0b RW	**Power Button Status (PWRBTN_STS) (pwrbtn_sts):** This bit is set when the PMU_PWRBTN_B signal is asserted (low), independent of any other enable bit. See PWRBTN_EN for the effect when PWRBTN_STS goes active. PWRBTN_STS is always a wake event. This bit is only set by hardware and can be cleared by software writing a one to this bit position. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST_B. If the PMU_PWRBTN_B signal is held low for more than 4 seconds, the PMC clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, the system transitions to the S5 state, and only PMU_PWRBTN_B is enabled as a wake event. If PWRBTN_STS bit is cleared by software while the PMU_PWRBTN_B pin is still held low, this will not cause the PWRBTN_STS bit to be set. The PMU_PWRBTN_B signal must go inactive and active again to set the PWRBTN_STS bit. Note that the CPU Thermal Trip and the Internal Thermal Sensors' Catastrophic Condition result in behavior matching the Powerbutton Override, which includes clearing this bit. reset_type=RSMRST_B

Bit Range	Default & Access	Description
7:6	0b RO	**reserved2:** Reserved.
5	0b RW	**GBL Status (GBL_STS) (gbl_sts):** This bit is set when an SCI is generated due to the BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit. The SCI handler should then clear this bit by writing a 1 to it. This bit will not cause wake events or SMI#. This bit is not effected by SCI_EN. Note: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place. reset_type=PMU_PLTRST_B
4:1	0b RO	**reserved3 (rserved3):** reserved
0	0b RW	**Timer Overflow Status (TMROF_STS) (tmrof_sts):** This is the timer overflow status bit. This bit gets set anytime bit 22 of the 24 bit timer goes low (bits are counted from 0 to 23). This will occur every 2.3435 seconds. See TMROF_EN for the effect when TMROF_STS goes active. Software clears this bit by writing a 1 to it. reset_type=PMU_PLTRST_B

20.7.2 PM1_CNT - Power Management 1 Control (PM1_CNT)—Offset 4h

Access Method

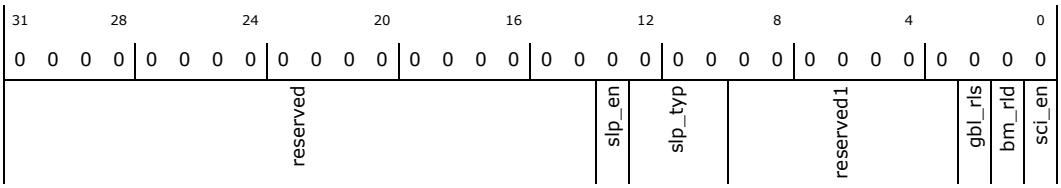
Type: I/O Register (Size: 32 bits)

PM1_CNT: [ACPI_BASE_ADDRESS] + 4h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:14	0b RO	**reserved:** Reserved.
13	0b WO	**Sleep Enable (SLP_EN) (slp_en):** This is a write-only bit and reads to it always return a zero. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.
12:10	0b RW	**Sleep Type (SLP_TYP) (slp_typ):** This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. These bits are reset by SRTCRST_B only. Bits Mode Typical Mapping 000 ON S0 001 Puts CPU in S1 state. S1 010 Reserved 011 Reserved 100 Reserved 101 Suspend-To-RAM S3 110 Suspend-To-Disk S4 111 Soft Off S5
9:3	0b RO	**reserved1:** Reserved.
2	0b RW	**GBL_RLS (GBL_RLS) (gbl_rls):** This bit is used by the ACPI software to raise an event to the BIOS software. BIOS software has a corresponding enable and status bits to control its ability to receive ACPI events. This bit always reads as 0.
1	0b RW	**BM_RLD (BM_RLD) (bm_rld):** This bit is treated as a scratchpad bit

Bit Range	Default & Access	Description
0	0b RW	**SCI Enable (SCI_EN) (sci_en):** SCI Enable (SCI_EN): Selects the SCI interrupt or the SMI# for various events. When this bit is 1, then the events will generate an SCI interrupt. When this bit is 0, these events will generate an SMI#.

20.7.3 PM1_TMR - Power Management 1 Timer (PM1_TMR)—Offset 8h

Access Method

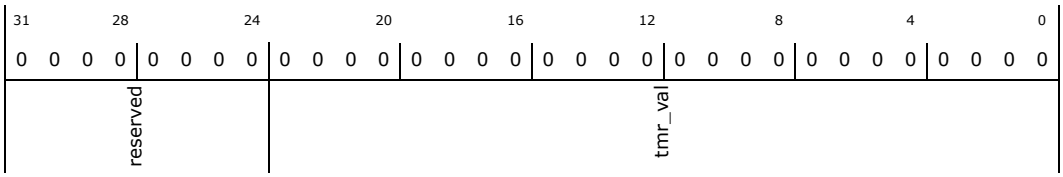
Type: I/O Register (Size: 32 bits)

PM1_TMR: [ACPI_BASE_ADDRESS] + 8h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**reserved:** Reserved.
23:0	0b RO	**Timer Value (TMR_VAL) (tmr_val):** This read-only field returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset (to 0) during a Platform reset, and then continues counting as long as the system is in the S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit is set. The High-to-Low transition will occur every 2.3435 seconds. Writes to this register have no effect.

20.7.4 GPE0a_STS - General Purpose Event 0 Status (GPE0a_STS)—Offset 20h

Note: This register is symmetrical to the General Purpose Event 0a Enable Register. Unless indicated otherwise below, if the corresponding _EN bit is set, then when the STS bit get set, the PMC will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the PMC will also generate an SCI if the SCI_EN bit is set, or an SMI# if the SCI_EN bit is not set. CLARIFICATION: Bits 15:0 should not be reset by CF9 write. Bits 31:16 are reset by CF9h full resets. reset_type=RSMRST_B

Access Method

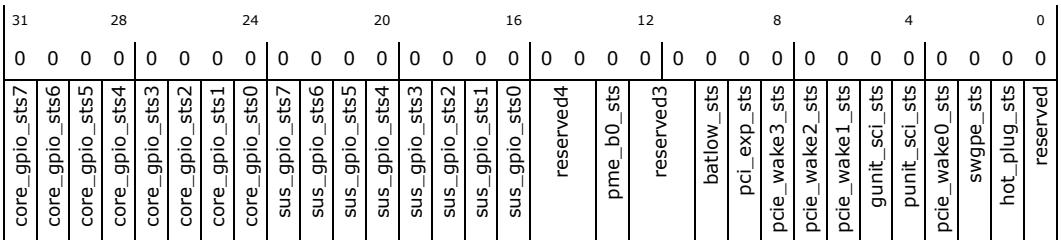
Type: I/O Register (Size: 32 bits)

GPE0a_STS: [ACPI_BASE_ADDRESS] + 20h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts7):** These bits are set any time the corresponding Core GPIO is set up as an input and the corresponding GPIO signal is asserted. Core GPIO pins are: SATA_GP0 (GPIO core 0) SATA_GP1 (GPIO core 1) SATA_LEDN (GPIO core 2) PCIE_CLKREQ0B (GPIO core 3) PCIE_CLKREQ1B (GPIO core 4) PCIE_CLKREQ2B (GPIO core 5) PCIE_CLKREQ3B (GPIO core 6) PCIE_CLKREQ4B (GPIO core 7) If the corresponding enable bit is set in the GPE0a_EN register, then when the CORE_GPIO_STS[n] bit is set, an SCI will be caused, depending on the GPIO_ROUT bits for the corresponding GPIO. These bits are sticky bits and are cleared by writing a 1 back to this bit position. reset_type=Resume Well Reset#
30	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts6):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
29	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts5):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
28	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts4):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
27	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts3):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
26	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts2):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
25	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts1):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)
24	0b RW	**CORE GPIO Status (CORE_GPIO_STS) (core_gpio_sts0):** These bit is part of CORE GPIO Status (CORE_GPIO_STS)

Bit Range	Default & Access	Description
23	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts7):** These bits are set any time the corresponding Sus GPIO is set up as an input and the corresponding GPIO signal is asserted. Sus GPIO pins are GPIO_SUS0-7. If the corresponding enable bit is set in the GPE0a_EN register, then when the SUS_GPIO_STS[n] bit is set: * If the system is in an S3-S5 state, the event will also wake the system. * If the system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIO_ROUT bits for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position. reset_type=Resume Well Reset#
22	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts6):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
21	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts5):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
20	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts4):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
19	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts3):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
18	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts2):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
17	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts1):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
16	0b RW	**SUS GPIO Status (SUS_GPIO_STS) (sus_gpio_sts0):** These bits are part of SUS GPIO Status (SUS_GPIO_STS)
15:14	0b RO	**reserved (reserved4):** Reserved.
13	0b RW	**Power Management Event Bus 0 Status (PME_B0_STS) (pme_b0_sts):** This bit will be set to 1 by the PMC when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). This bit is cleared by a software write of '1'. Internal devices which can set this bit: - Integrated LAN - HD Audio - SATA - USB
12:11	0b RO	**reserved (reserved3):** Reserved.
10	0b RW	**Battery Low Status (BATLOW_STS) (batlow_sts):** This bit will be set to 1 by hardware when the PMU_BATLOW_B signal goes low. Software clears the bit by writing a 1 to the bit position. In Desktop Mode, this bit will be treated as Reserved.
9	0b RW	**PCI Express Status (PCI_EXP_STS) (pci_exp_sts):** This bit will be set to 1 by hardware to indicate that: - The PME event message was received on one or more of the PCI-Express Ports Note: The PCI PMU_WAKE_B pin and the PCI-Express Beacons have no impact on this bit. Software attempts to clear this bit by writing a 1 to this bit position. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the leveltriggered SCI will remain active. Note that a race condition exists where the PCI Express device sends another PME message because the PCI Express device was not serviced within the time when it must resend the message. This may result in a spurious interrupt, and this is comprehended and approved by the PCI Express specification. The window for this race condition is approximately 95-105 milliseconds.
8	0b RW	**PCI Express Wake3 Status (PCIE_WAKE3_STS) (pcie_wake3_sts):** This bit is set by hardware to indicate that the PCI_WAKE3_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE3_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
7	0b RW	**PCI Express Wake2 Status (PCIE_WAKE2_STS) (pcie_wake2_sts):** This bit is set by hardware to indicate that the PCI_WAKE2_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE2_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b

Bit Range	Default & Access	Description
6	0b RW	**PCI Express Wake1 Status (PCIE_WAKE1_STS) (pcie_wake1_sts):** This bit is set by hardware to indicate that the PCI_WAKE1_B pin was asserted. Software writes a 1 to clear this bit. If PCI_WAKE1_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
5	0b RW	**GUNIT SCI status (GUNIT_SCI_STS) (gunit_sci_sts):** This bit will be set if the Graphics Unit requests SCI
4	0b RW	**PUNIT SCI status (PUNIT_SCI_STS) (punit_sci_sts):** This bit will be set if the Power Management Unit requests SCI
3	0b RW	**PCI Express Wake0 Status (PCIE_WAKE0_STS) (pcie_wake0_sts):** This bit is set by hardware to indicate that the PMU_WAKE_B pin was asserted. Software writes a 1 to clear this bit. If PMU_WAKE_B pin is still active during the write, then the bit will remain active (i.e. input to this bit is level sensitive). reset_type=pmc_global_rst_b
2	0b RW	**Software GPE Status (SWGPE_STS) (swgpe_sts):** The SWGPE_CTRL bit (bit 1 of GPE_CTRL reg) acts as a level input to this bit.
1	0b RO	**Hot Plug Status (HOT_PLUG_STS) (hot_plug_sts):** This bit is set to 1 by hardware when a PCI-Express hotplug event occurs. This will cause an SCI if the HOT_PLUG_EN and SCI_EN bits are set. This bit is cleared by writing a 1 to this bit position. The following events cause this bit to set - Assert_GPE message received from any of the PCI_E ports in the processor - Assert_HPGPE message received from any of the PCI_E ports in the processor
0	0b RO	**reserved:** Reserved.

20.7.5 GPE0a_EN - General Purpose Event 0 Enables (GPE0a_EN)—Offset 28h

Note: This register is symmetrical to the General Purpose Event 0a Status Register. reset_type=Resume Well Reset#

Access Method

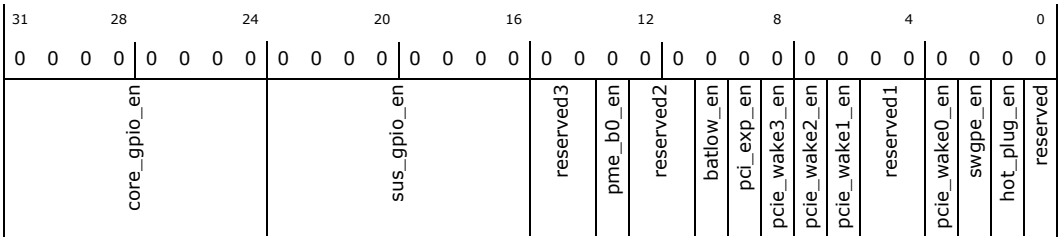
Type: I/O Register (Size: 32 bits)

GPE0a_EN: [ACPI_BASE_ADDRESS] + 28h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**CORE GPIO Enable (CORE_GPIO_EN) (core_gpio_en):** These bits enable the corresponding CORE_GPIO_STS[n] bits being set to cause an SCI and/or wake event.
23:16	0b RW	**SUS GPIO Enable (SUS_GPIO_EN) (sus_gpio_en):** These bits enable the corresponding SUS_GPIO_STS[n] bits being set to cause an SCI and/or wake event.

Bit Range	Default & Access	Description
15:14	0b RO	**reserved (reserved3):** Reserved.
13	0b RW	**PME_B0 Enable (PME_B0_EN) (pme_b0_en):** Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#. In addition to being reset by SRTCRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
12:11	0b RO	**reserved (reserved2):** Reserved.
10	0b RW	**Low Battery Enable (BATLOW_EN) (batlow_en):** This bit enables the PMU_BATLOW_B signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low.This bit does not prevent the PMU_BATLOW_B signal from inhibiting the wake event. In Desktop Mode this bit will be treated as Reserved. In addition to being reset by SRTCRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip reset_type=SRTCRST_B
9	0b RW	**PCI Express Enable (PCI_EXP_EN) (pci_exp_en):** Enables the PMC to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express ports, to cause an SCI due to wake/PME events
8	0b RW	**PCI Express Wake3 Enable (PCIE_WAKE3_EN) (pcie_wake3_en):** This bit, when set to 1, enables the PCIE_WAKE3_STS to to cause an SCI
7	0b RW	**PCI Express Wake2 Enable (PCIE_WAKE2_EN) (pcie_wake2_en):** This bit, when set to 1, enables the PCIE_WAKE2_STS to to cause an SCI
6	0b RW	**PCI Express Wake1 Enable (PCIE_WAKE1_EN) (pcie_wake1_en):** This bit, when set to 1, enables the PCIE_WAKE1_STS to to cause an SCI
5:4	0b RO	**reserved (reserved1):** Reserved.
3	0b RW	**PCI Express Wake0 Enable (PCIE_WAKE0_EN) (pcie_wake0_en):** This bit, when set to 1, enables the PCIE_WAKE0_STS to to cause an SCI
2	0b RW	**Software GPE Enable (SWGPE_EN) (swgpe_en):** This bit, when set to 1, enables the SW GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input) If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1's, an SCI will be generated If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1 then an SMI# will be generated
1	0b RW	**Hot Plug Enable (HOT_PLUG_EN) (hot_plug_en):** Enables the PMC to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express ports to cause an SCI due to hot-plug events.
0	0b RO	**reserved:** Reserved.

20.7.6 SMI_EN - SMI Control and Enable (SMI_EN)—Offset 30h

Access Method

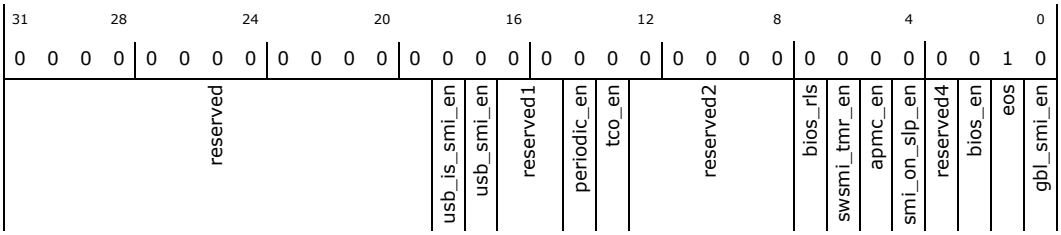
Type: I/O Register (Size: 32 bits)

SMI_EN: [ACPI_BASE_ADDRESS] + 30h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000002h



Bit Range	Default & Access	Description
31:19	0b RO	**reserved:** Reserved.
18	0b RW	**Intel USB 2 Enable (USB_IS_SMI_EN): (usb_is_smi_en):** Enables Intel-Specific USB2 SMI logic to cause SMI#.
17	0b RW	**USB SMI Enable (USB_SMI_EN): (usb_smi_en):** Enables SMI from USB
16:15	0b RO	**reserved1:** Reserved.
14	0b RW	**Periodic Enable (PERIODIC_EN) (periodic_en):** Setting this bit will cause the PMC to generate an SMI# when the PERIODIC_STS bit is set in the SMI_STS register.
13	0b RW	**TCO Enable (TCO_EN): (tco_en):** when set Enables the TCO logic to generate SMI#. when cleared disables TCO logic generating an SMI#. NOTE: This bit can not be written once the TCO_LOCK bit is set. This prevents unauthorized software from disabling the generation of TCO-based SMI's
12:8	0b RO	**reserved2:** Reserved.
7	0b RW	**BIOS_RLS (BIOS_RLS): (bios_rls):** Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software. This bit always reads a zero. NOTE: GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (which causes GBL_STS to be set) if the SCI handler is not in place.
6	0b RW	**Software SMI Timer Enable (SWSMI_TMR_EN): (swsmi_tmr_en):** Software sets this bit to a 1 to start the Software SMI# Timer. When the timer expires (depending on the SWSMI_RATE_SEL bits), it will generate an SMI# and set the SWSMI_TMR_STS bit. The SWSMI_TMR_EN bit will remain at 1 until software sets it back to 0. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. The default for this bit is 0.
5	0b RW	**APMC_EN (apmc_en):** APMC Enable - If set, this enables writes to the APM register to cause an SMI#
4	0b RW	**SMI On Sleep Enable (SMI_ON_SLP_EN): (smi_on_slp_en):** If this bit is set, the PMC will generate an SMI# when a write access attempts to set the SLP_EN bit (in the PM1_CNT register). Furthermore, the PMC will not put the system to a sleep state. This allows the SMI# handler work around chip-level bugs. It is expected that the SMI# handler will turn off the SMI_ON_SLP_EN bit before actually setting the SLP_EN bit.

Bit Range	Default & Access	Description
3	0b RO	**reserved4:** Reserved.
2	0b RW	**BIOS Enable (BIOS_EN): (bios_en):** Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit. Note that if the BIOS_STS bit, which gets set when software writes a 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set.
1	1b RW	**End of SMI (EOS): (eos):** SMI handler sets this bit when it finishes handling the SMI. Setting this bit will force the PMC internal SMI request to zero for 1 clock.Thus if the internal SMI request is still asserted due to new SMI trigger a new rising edge will happen, setting the interrupt to the PMC controller.
0	0b RW	**Global SMI Enable (GBL_SMI_EN): (gbl_smi_en):** When set, this bit enables the generation of SMIs in the system upon any enabled SMI event. This bit is reset by a PMU_PLTRST_B reset event. If this bit is not set, no SMI# will be generated. NOTE: When the SMI_LOCK bit is set, this bit cannot be changed.

20.7.7 SMI_STS - SMI Status Register (SMI_STS)—Offset 34h

Access Method

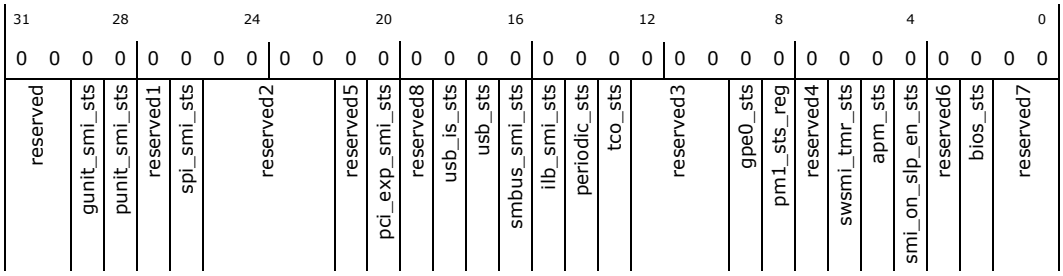
Type: I/O Register (Size: 32 bits)

SMI_STS: [ACPI_BASE_ADDRESS] + 34h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:30	0b RO	**reserved:** Reserved.
29	0b RW	**GUNIT SMI Status (GUNIT_SMI_STS): (gunit_smi_sts):** This bit will be set if Graphics unit is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'
28	0b RW	**PUNIT SMI Status (PUNIT_SMI_STS): (punit_smi_sts):** This bit will be set if Power Management is requesting an SMI#. Writing a '1' to this bit position clears this bit to '0'
27	0b RO	**reserved (reserved1):** Reserved.
26	0b RO	**SPI_SMI Status (SPI_SMI_STS): (spi_smi_sts):** This bit will be set when the SPI logic is requesting an SMI#
25:22	0b RO	**reserved (reserved2):** Reserved.

Bit Range	Default & Access	Description
21	0b RW	**reserved (reserved5):** This bit is reserved for future use
20	0b RO	**PCI_EXP_SMI Status (PCI_EXP_SMI_STS): (pci_exp_smi_sts):** 1- PCI Express SMI event occurred. This could be due to a PCI Express PME event.
19	0b RO	**reserved (reserved8):** Reserved.
18	0b RO	**Intel USB2 Status (USB_IS_STS): (usb_is_sts):** This non-sticky read-only bit is a logical OR of each of the SMI status bits in the Intel-Specific USB2 SMI Status Register ANDed with the corresponding enable bits. Additionally, the Port Disable Write Enable SMI is reported in this bit; the specific status bit for this event is contained in the USB Per-Port Registers Write Control Register in this I/O space. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated USB2 Host Controllers are represented with this bit.
17	0b RO	**USB Status (USB_STS): (usb_sts):** This bit will be set when the USB logic is requesting an SMI#
16	0b RO	**SMBUS_SMI Status (SMBUS_SMI_STS): (smbus_smi_sts):** This bit will be set when the SMBus logic is requesting an SMI#
15	0b RO	**ILB_SMI Status (ILB_SMI_STS): (ilb_smi_sts):** This bit will be set when the ILB logic is requesting an SMI#
14	0b RW	**Periodic Status (PERIODIC_STS): (periodic_sts):** This bit will be set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit is also set, the PMC will generate an SMI#. This bit is cleared by writing a 1 to this bit position.
13	0b RW	**TCO Status (TCO_STS): (tco_sts):** Indicates SMI was caused by the TCO logic. This bit is cleared by writing a 1 to this bit position.
12:10	0b RO	**reserved (reserved3):** Reserved.
9	0b RO	**GPE0a Status (GPE0a_STS): (gpe0_sts):** There are several status/enable bit pairs in GPE0a_STS/EN that are capable of triggering SMI. This bit is a logical OR of all of those pairs (i.e. this bit is asserted whenever at least one of those pairs has both the status and enable bit asserted). This bit is NOT sticky. Writes to this bit will have no effect. Note: The setting of this bit does not cause the SMI#.
8	0b RO	**PM1 Status Register (PM1_STS_REG): (pm1_sts_reg):** This is an OR of the bits (except for bits 5 and 4) in the ACPI PM1_STS_EN Status Reg. Not sticky. Writes to this bit have no effect. Note: The setting of this bit does not cause the SMI#.
7	0b RO	**reserved (reserved4):** Reserved.
6	0b RW	**Software SMI Timer Status (SWSMI_TMR_STS): (swsmi_tmr_sts):** This bit will be set to 1 by the hardware when the Software SMI# Timer expires. This bit will remain 1 until the software writes a 1 to this bit.
5	0b RW	**APM_STS (apm_sts):** APM Status - SMI# was generated by a write access to the APM control register and if the APMC_EN bit is set. This bit is cleared by writing a one to its bit position.
4	0b RW	**SMI_ON_SLP_EN Status (SMI_ON_SLP_EN_STS): (smi_on_slp_en_sts):** This bit will be set by the PMC when a write access attempts to set the SLP_EN bit. This bit is cleared by writing a 1 to this bit position
3	0b RO	**reserved (reserved6):** Reserved.
2	0b RW	**BIOS Status (BIOS_STS): (bios_sts):** This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit. When both BIOS_EN and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to this bit position.
1:0	0b RO	**reserved (reserved7):** Reserved.

20.7.8 ALT_GPIO_SMI - Alternate GPIO SMI Status and Enable Register. (ALT_GPIO_SMI)—Offset 38h

reset_type=Resume Well Reset#

Access Method

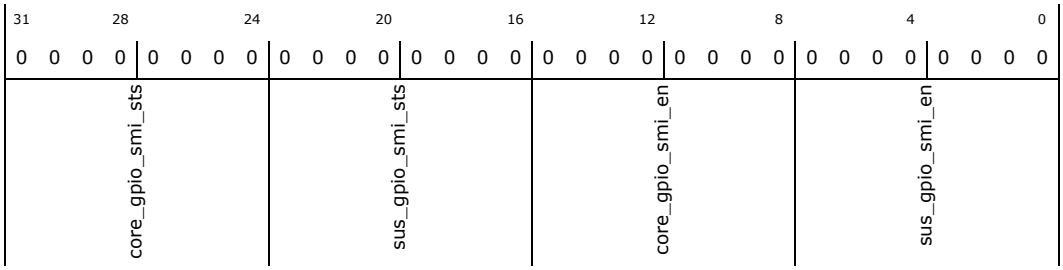
Type: I/O Register (Size: 32 bits)

ALT_GPIO_SMI: [ACPI_BASE_ADDRESS] + 38h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RW	**CORE GPIO SMI Status Setting (CORE_GPIO_SMI_STS): (core_gpio_smi_sts):** These bits report the status of the corresponding GPIO's. 1 = active, -0 = inactive. These bits are sticky. If the following conditions are true, then an SMI# will be generated: 1. The corresponding enable bit in this register is set 2. The corresponding GPIO must be routed in the GPIO_ROUT register to cause an SMI. 3. The corresponding GPIO must be implemented. Core GPIO pins are: SATA_GP0 (GPIO core 0) SATA_GP1 (GPIO core 1) SATA_LEDN (GPIO core 2) PCIE_CLKREQ0B (GPIO core 3) PCIE_CLKREQ1B (GPIO core 4) PCIE_CLKREQ2B (GPIO core 5) PCIE_CLKREQ3B (GPIO core 6) PCIE_CLKREQ4B (GPIO core 7) All bits are in the resume well. Default for these bits are dependent on the state of the GPIO pins.
23:16	0b RW	**SUS GPIO SMI Status Setting (SUS_GPIO_SMI_STS): (sus_gpio_smi_sts):** These bits report the status of the corresponding GPIO's. 1 = active, -0 = inactive. These bits are sticky. If the following conditions are true, then an SMI# will be generated: 1. The corresponding enable bit in this register is set 2. The corresponding GPIO must be routed in the GPIO_ROUT register to cause an SMI. 3. The corresponding GPIO must be implemented. Sus GPIO pins are GPIO_SUS0-7. All bits are in the resume well. Default for these bits are dependent on the state of the GPIO pins.
15:8	0b RW	**CORE GPIO SMI Enable Setting (CORE_GPIO_SMI_EN): (core_gpio_smi_en):** These bits are used to enable the corresponding GPIO to cause an SMI#.
7:0	0b RW	**SUS GPIO SMI Enable Setting (SUS_GPIO_SMI_EN): (sus_gpio_smi_en):** These bits are used to enable the corresponding GPIO to cause an SMI#.

20.7.9 UPRWC - USB Per-Port Registers Write Control (UPRWC)—Offset 3Ch

Access Method

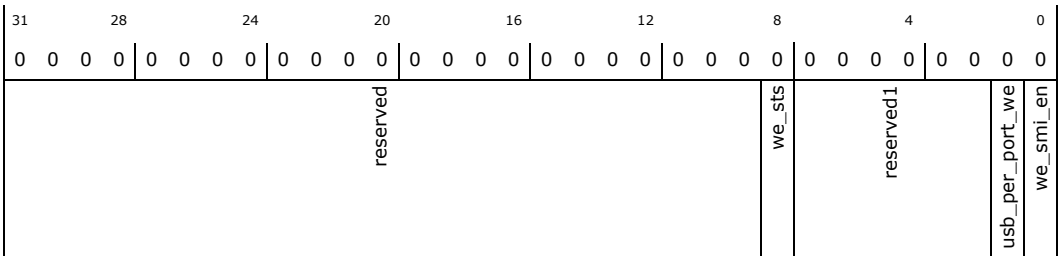
Type: I/O Register (Size: 32 bits)

UPRWC: [ACPI_BASE_ADDRESS] + 3Ch

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	0b RO	**reserved:** Reserved.
8	0b RW	**Write Enable Status (WE_STS) (we_sts):** This bit gets set by hardware when the Per-Port Registers Write Enable bit is written from 0 to 1. This bit is cleared by software writing a 1b to this bit location. The setting condition takes precedence over the clearing condition in the event that both occur at once. When this bit is 1b and bit 0 is 1b, the INTEL_USB2_STS bit is set in the SMI_STS register.
7:2	0b RO	**reserved (reserved1):** Reserved.
1	0b RW	**USB Per-Port Registers Write Enable (USB_PER_PORT_WE) (usb_per_port_we):** This bit controls whether writes are enabled to the USB Port Power Off and Port Disable Override registers
0	0b RW	**Write Enable SMI Enable (WE_SMI_EN) (we_smi_en):** This bit enables the generation of SMI when the Per-Port Registers Write Enable (bit 1) is written from 0 to 1. Once written to 1b, this bit can not be cleared by software.

20.7.10 GPE_CTRL - General Purpose Event Control (GPE_CTRL)—Offset 40h

Access Method

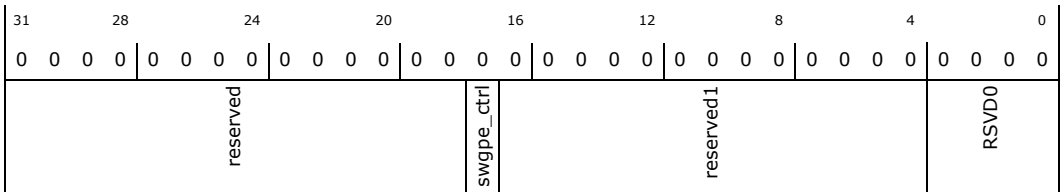
Type: I/O Register (Size: 32 bits)

GPE_CTRL: [ACPI_BASE_ADDRESS] + 40h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:18	0b RO	**reserved:** Reserved.
17	0b RW	**Software GPE Control (SWGPE_CTRL) (swgpe_ctrl):** This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0a_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. In addition to being reset by RSMRST_B assertion, the PMC also clears this bit due to certain events: - Power button override - CPU thermal trip
16:4	0b RO	**reserved1:** Reserved.
3:0	0b RO	**RSVD0:** Reserved

20.7.11 PM2A_CNT_BLK - PM2a Control Block (PM2A_CNT_BLK)—Offset 50h

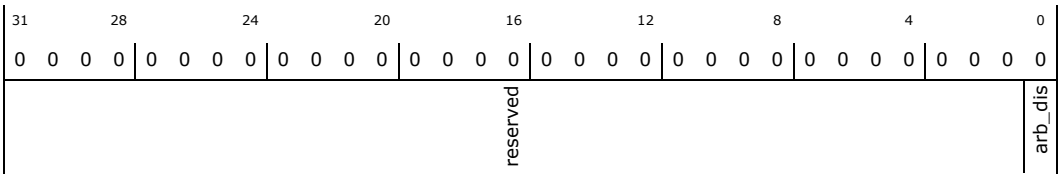
Access Method

Type: I/O Register (Size: 32 bits)

PM2A_CNT_BLK: [ACPI_BASE_ADDRESS] + 50h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**reserved:** Reserved.
0	0b RW	**ARB_DIS (ARB_DIS) (arb_dis):** This bit is essentially just a scratchpad bit for legacy software compatibility.

20.7.12 TCO_RLD: TCO Reload Register (TCO_RLD)—Offset 60h

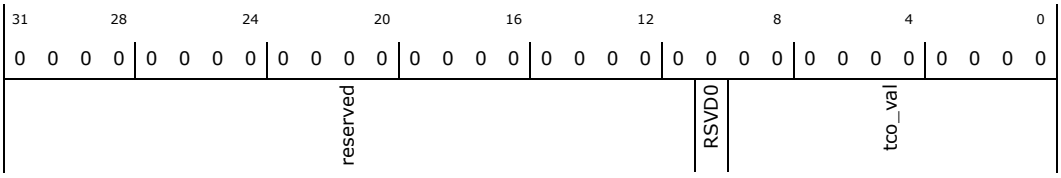
Access Method

Type: I/O Register (Size: 32 bits)

TCO_RLD: [ACPI_BASE_ADDRESS] + 60h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:11	0b RO	**reserved:** Reserved.
10	0b RO	**RSVD0:** Reserved
9:0	0b RO	**TCO Timer Value (TCO_TVAL) (tco_val):** Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

20.7.13 TCO_STS: TCO Timer Status (TCO_STS)—Offset 64h

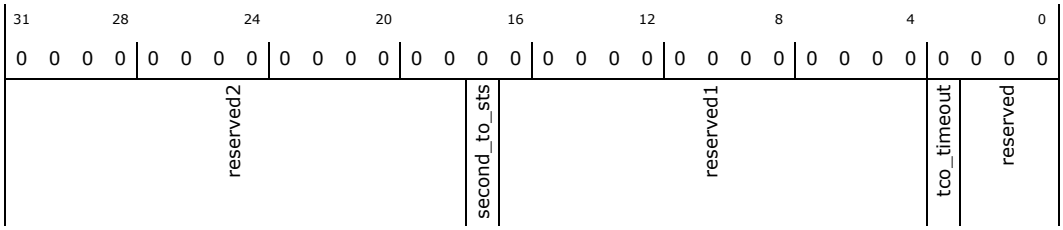
Access Method

Type: I/O Register
(Size: 32 bits)

TCO_STS: [ACPI_BASE_ADDRESS] + 64h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:18	0b RO	**reserved (reserved2):** Reserved.
17	0b RW	**Second Timeout Status(SECOND_TO_STS) (second_to_sts):** PMC sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT config bit is 0, then the PMC will reboot the system after the second timeout. The reboot is done by asserting PMU_PLTRST_B. This bit is only cleared by writing a 1 to this bit or by a RSMRST_B.
16:4	0b RO	**reserved (reserved1):** Reserved.
3	0b RW	**TCO Timeout (TCO_TIMEOUT) (tco_timeout):** Bit set to 1 by PMC to indicate that the SMI was caused by TCO timer reaching 0.
2:0	0b RO	**reserved:** Reserved.

20.7.14 TCO1_CNT: TCO Timer Control (TCO1_CNT)—Offset 68h

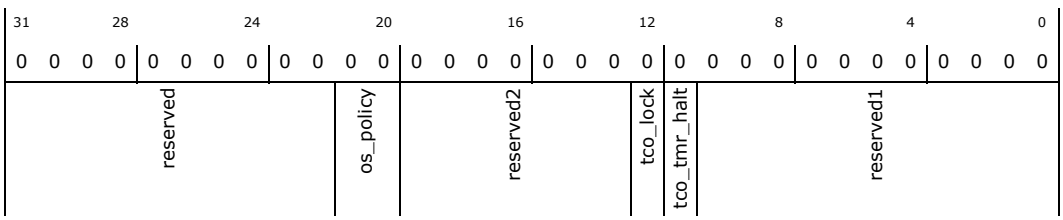
Access Method

Type: I/O Register
(Size: 32 bits)

TCO1_CNT: [ACPI_BASE_ADDRESS] + 68h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00000000h



Bit Range	Default & Access	Description
31:22	0b RO	**reserved:** Reserved.
21:20	0b RW	**OS_POLICY (os_policy):** OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due the WDT. The following convention is recommended for the BIOS and OS: 00 Boot normally 01 Shut down 10 Dont load OS. Hold in pre-boot state and use LAN to determine next step 11 Reserved
19:13	0b RO	**reserved (reserved2):** Reserved.
12	0b RW	**TCO Lock (TCO_LOCK) (tco_lock):** When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.
11	0b RW	**TCO Timer Halt (TCO_TMR_HALT) (tco_tmr_halt):** 1 = The TCO timer will halt. It will not count, and thus cannot reach a value that would cause an SMI# or to cause the SECOND_TO_STS bit to be set. This will also prevent rebooting. 0 = The TCO timer is enabled to count. This is the default.
10:0	0b RO	**reserved1:** Reserved.

20.7.15 TCO_TMR: TCO Timer Register (TCO_TMR)—Offset 70h

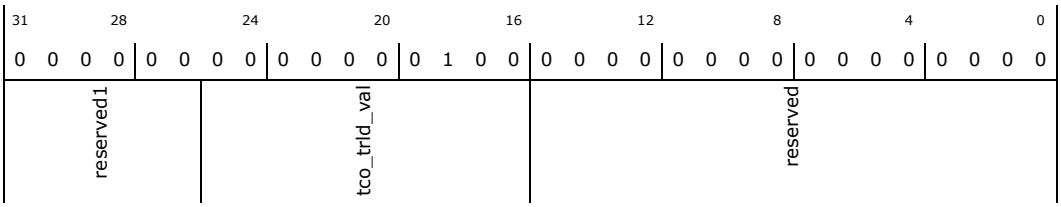
Access Method

Type: I/O Register (Size: 32 bits)

TCO_TMR: [ACPI_BASE_ADDRESS] + 70h

ACPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ACPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 40h

Default: 00040000h



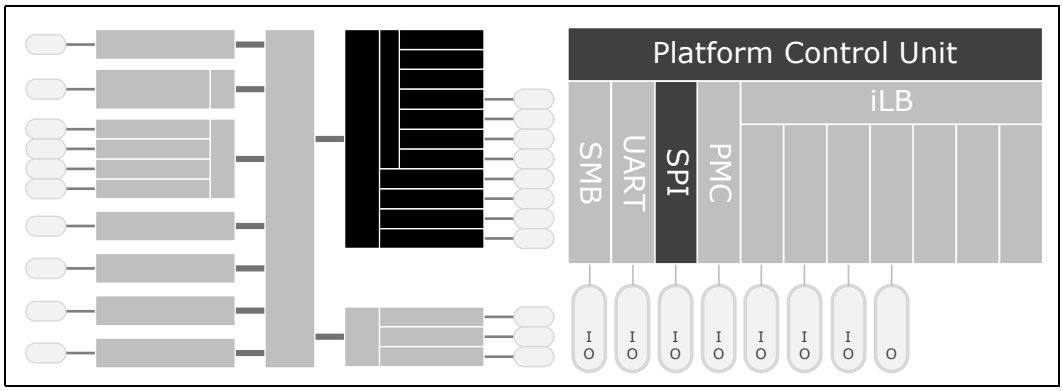
Bit Range	Default & Access	Description
31:26	0b RO	**reserved (reserved1):** Reserved.
25:16	004h RW	**TCO Timer reload value (TCO_TRLD_VAL) (tco_trld_val):** Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. Note: The timer has an error of +/- 1 tick (0.6s). The TCO Timer will only count down in the S0 state.
15:0	0b RO	**reserved:** Reserved.

§ §

21 PCU – Serial Peripheral Interface (SPI)

The processor implements a SPI controller as the interface for BIOS Flash storage. This SPI Flash device is also required to support firmware for the Trusted Execution Engine (required). The controller supports a maximum of two SPI Flash devices, using two chip select signals, with speeds of 20 MHz, 33 MHz or 50 MHz.

Note: The default interface speed is 20 MHz.



21.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

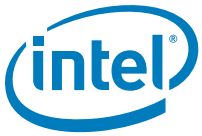


Table 153. SPI Signals

Signal Name	Direction/ Type	Description
PCU_SPI_CLK	O CMOS1.8	**SPI Clock:** When the bus is idle, the owner will drive the clock signal low.
PCU_SPI_CS[0]#	O CMOS1.8	**SPI Chip Select 0:** Used as the SPI bus request signal for the first SPI Flash device.
PCU_SPI_CS[1]#	O CMOS1.8	**SPI Chip Select 1:** Used as the SPI bus request signal for the second SPI Flash devices. *This signal is multiplexed and may be used by other functions.*
PCU_SPI_MISO	I CMOS1.8	**SPI Master IN Slave OUT:** Data input pin for the processor.
PCU_SPI_MOSI	I/O CMOS1.8	**SPI Master OUT Slave IN:** Data output pin for the processor. Operates as a second data input pin for the processor when in Single Input, Dual Output Fast Read mode.

Note: All SPI signals are tri-stated with 20k ohm internal weak pull-up until PMC_CORE_PWROK is asserted.

21.2 Features

The SPI controller supports up to two SPI Flash devices using two separate chip select pins. Each SPI Flash device can be up to 16 MB. The processor SPI interface supports 20 MHz, 33 MHz and 50 MHz SPI Flash devices. No other types of SPI devices are supported.

Communication on the SPI bus is done with a Master – Slave protocol. The Slave is connected to the processor and is implemented as a tri-state bus.

Note: When GCS.BBS = 00b, LPC is selected as the location for BIOS. The SPI Flash may still contain data and firmware for other processor functionality.

Note: When GCS.BBS =11b and a SPI device is detected by the processor, LPC based BIOS Flash is disabled.

21.2.1 Operation Mode Feature Overview

The SPI controller has two operational modes, Non-Descriptor and Descriptor.

21.2.1.1 Non-Descriptor Mode

If no valid signature is read (either because there is no SPI Flash, or there is an SPI Flash with no valid descriptor), the Flash Controller will operate in a Non-Descriptor mode.

The following features are not supported in Non-Descriptor mode:

- Trusted Execution Engine
- Secure Boot
- Soft Straps
- Two SPI Flash device support
- Hardware sequencing access
- Descriptor-based security access restrictions

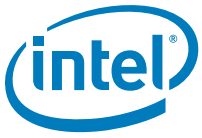
Note: When operating in Non-Descriptor mode, software sequencing must be used to access the Flash.

Note: When operating in Non-Descriptor Mode, and a SPI Flash is attached to the processor, it is required that the Flash Valid Signature, at offset 10h of the Flash Descriptor, does not equal the expected valid value (0FF0A55Ah) or the SPI Controller will wrongly interpret that it has a valid signature and that a Flash Descriptor has been implemented.

21.2.2 Descriptor Mode

Descriptor Mode is required to enable many features of the processor:

- Trusted Execution Engine
- Secure Boot
- PCI Express* root port configuration
- Supports for two SPI components using two separate chip select pins
- Hardware enforced security restricting master accesses to different regions
- Soft Strap region providing the ability to use Flash NVM to remove the need for pull-up/pull-down resistors for strapping processor features
- Support for the SPI Fast Read instruction and frequencies greater than 20 MHz
- Support for Single Input, Dual Output Fast reads
- Use of standardized Flash instruction set



SPI Flash Regions

In Descriptor Mode the Flash is divided into five separate regions as shown in the following table.

Table 154. SPI Flash Regions

Region	Content
0	Flash Descriptor
1	BIOS
2	Trusted Execution Engine
3	
4	Platform Data

Only masters can access the four regions: The processor core running BIOS code and the Trusted Execution Engine. The only required region is Region 0, the Flash Descriptor. Region 0 must be located in the first sector of Device 0.

Flash Regions Sizes

SPI Flash space requirements differ by platform and configuration. Table 155 indicates the space needed in the Flash for each region.

Table 155. Region Size Versus Erase Granularity of Flash Components

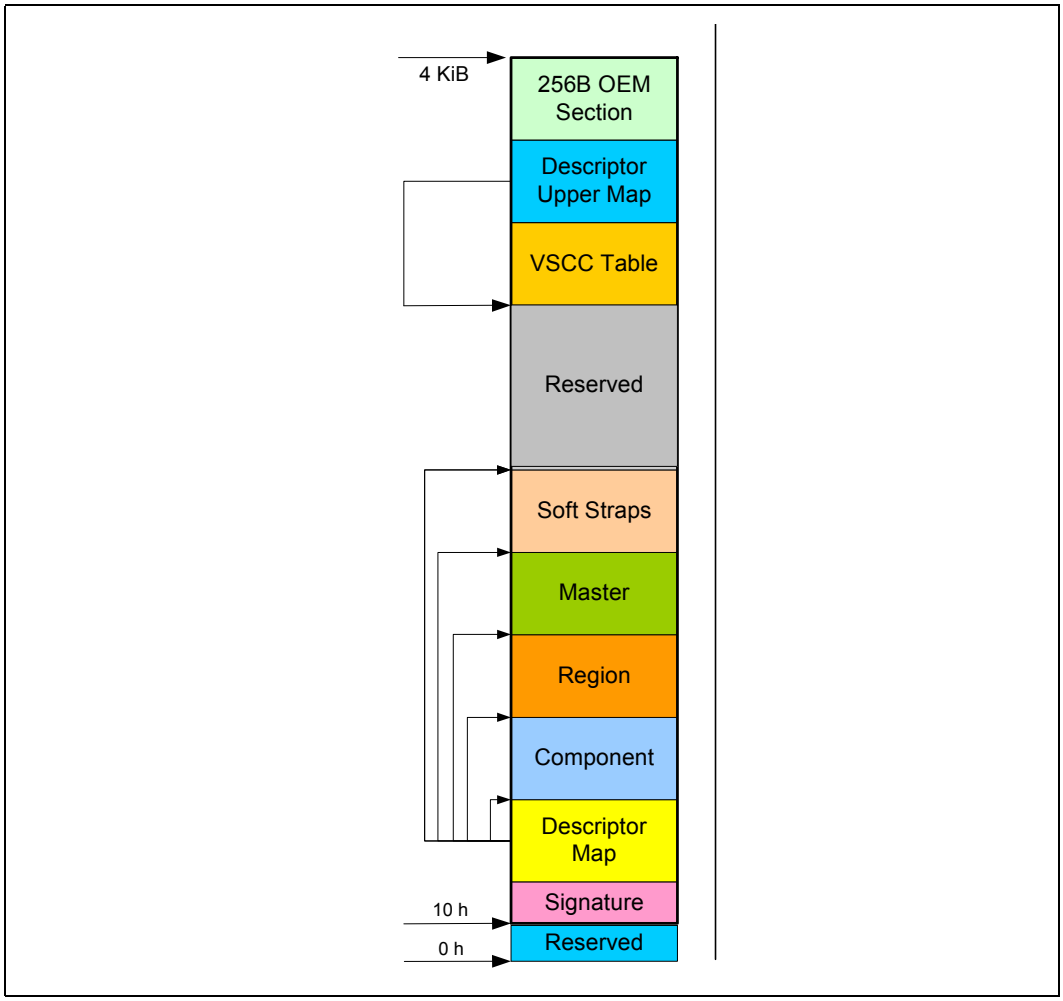
Region	Size with 4 KB Blocks	Size with 8 KB Blocks	Size with 64 KB Blocks
Descriptor	4 KB	8 KB	64 KB
BIOS	Varies by Platform	Varies by Platform	Varies by Platform
Trusted Execution Engine	TBD	TBD	TBD

21.2.3 Flash Descriptor

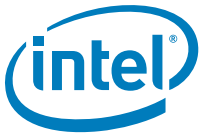
The maximum size of the Flash Descriptor is 4 KB. If the block/sector size of the SPI Flash device is greater than 4 KB, the Flash descriptor will only use the first 4 KB of the first block. The Flash descriptor requires its own block at the bottom of memory (00h). The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read only when the system containing the processor leaves the manufacturing floor.

The Flash Descriptor is made up of eleven sections as indicated in the following figure.

Figure 30. Flash Descriptor Sections



- The **Reserved** section at offset 0h is related to functionality not supported by the processor.
- The **Signature** section selects Descriptor Mode as well as verifies if the Flash is programmed and functioning. The data at the bottom of the Flash (offset 10h) must be 0FF0A55Ah in order to be in Descriptor mode.
- The **Descriptor Map** section defines the logical structure of the Flash in addition to the number of components used.
- The **Component** section has information about the SPI Flash in the system including:
  - — Density of each component
  - — Illegal instructions (such as chip erase)
  - — Frequencies for read, fast read and write/erase instructions.



- The **Region** section points to the four other regions as well as the size of each region.
- The **Master** region contains the security settings for the Flash, granting read/write permissions for each region and identifying each master by a requestor ID.
- The **Soft Straps** section contains parameter bits that can be used to configure processor features and/or behaviors.
- The **Reserved** section between the top of the **Soft Straps** section and the bottom of the **VSCC Table** is reserved for future processor usages.
- The **VSCC Table** section holds the JEDEC ID and the VSCC (Vendor Specific Component Capabilities) information of the entire SPI Flash supported by the NVM image.
- The **Descriptor Upper Map** section determines the length and base address of the **VSCC Table** section.
- The **OEM Section** is 256 Bytes reserved at the top of the Flash Descriptor for use by an OEM.

21.2.3.1 Master Section

The Master section defines read and write access setting for each region of the SPI device, when the SPI controller is running in Descriptor mode. The master region recognizes masters: Processor CPU core running BIOS code and the Trusted Execution Engine.

Note: Each master is only allowed to do direct reads of its primary regions. The Trusted Execution Engine is may also do a direct read of the BIOS region if it has been given read access to that region. See Section 21.2.4.1, "Direct Access" for further details on direct reads.

Table 156. Region Access Control

Master Read/Write Access		
Region	**BIOS**	**Trusted Execution Engine**
Descriptor	N/A	N/A
BIOS	CPU core and BIOS can always read from and write to BIOS Region	Read / Write
Trusted Execution Engine	Read / Write	Trusted Execution can always read from and write to Trusted Execution Engine Region
Platform Data	N/A	N/A

21.2.3.2 Invalid Flash Descriptor Handling

The processor will respond to an invalid Flash Descriptor with the following:

- The SPI controller will operate in Non-Descriptor mode.

- If the BBS strap (see Section 19.1.2 for details) is set to 1, BIOS direct read access will be forwarded to the SPI Controller without any address translation.
- The HSFSTS.FDV register bits remains at 0b.
- All security checks are disabled and the entire Flash is open for reading and writing. No restriction on the 4k crossing.
- Trusted Execution Engine direct read accesses will not be handled, and the SPI controller will return all 1's.

Note: To ensure BIOS boot access even when the Flash Descriptor is invalid the BIOS region can be placed at the top of Flash Component 0. Placing the BIOS region in any other location will necessitate a full reprogramming of the Flash before boot is possible from that Flash.

21.2.3.3 Descriptor Security Override Strap

A strap is implemented on GPIO_S0_SC[065] to allow descriptor security to be overridden when the strap is sampled low.

If the strap is set (0b), it will have the following effect:

- The Master Region Read Access and Master Region Write Access permissions that were loaded from the Flash Descriptor Master Section will be overridden giving every master read and write permissions to the entire Flash component including areas outside the defined regions.
- BIOS Protected Range 4 (PR4), if enabled by soft strap, will be overridden so that all masters are able to write to the PR4. The PR4 base and limit addresses are fetched and received from soft strap.

21.2.4 Flash Access

There are two types of Flash accesses: Direct Access and Program Register Access.

21.2.4.1 Direct Access

- Direct writes are not allowed for any master.
- The processor CPU core is only allowed to do a direct read of the BIOS region
- The Trusted Execution Engine is only allowed to do a direct read of the Trusted Execution Engine region. It may also do a direct read of the BIOS region if it has been given read access to that region.

Note: Trusted Execution Engine region direct reads are not supported when the SPI controller is operating in Non-Descriptor mode. The SPI controller returns all 1s if a direct read is attempted.

21.2.4.2 Security

- Calculated Flash Linear Address (FLA) must fall between primary region base/limit

Note: During non descriptor mode, the Flash Physical Address is used instead. Only the two BIOS ranges at the E0000h and F0000h segments just below 1MB are supported.

- Direct Read Cache contents are reset to 0's on a read from a different master

21.2.4.3 Program Register Access

- Reads, Writes and Erases are all supported.
- Program Register Access may use Hardware or Software Sequencing. See Section 21.3.1, "Hardware vs. Software Sequencing" for further information.
- Program Register Accesses are not allowed to cross a 4 KB boundary and can not issue a command that might extend across two components
- Software programs the FLA corresponding to the region desired
  - — Software must read the devices Primary Region Base/Limit address to create a FLA.

Each master accesses the Flash through a set of memory mapped registers that are dedicated to each device.

There are two separate control and status registers that software can use when using register access to the Flash. The Hardware Sequencing control/status registers rely on hardware to issue appropriate Flash instructions and atomic sequences. The Software Sequencer puts control into the hands of the software for what instructions to issue and when.

The goal is to support all Flash components through hardware sequencing. Software sequencing is intended only for a back-up strategy.

Note: Software sequencing is required when operating in a non-descriptor mode.

21.2.4.4 Security

- Only primary region masters can access the registers
- Masters are only allowed to read or write those regions they have read/write permission
- Using the Flash region access permissions, one master can give another master read/write permissions to their area
- Using the five Protected Range registers, each master can add separate read/write protection above that granted in the Flash Descriptor for their own accesses
  - — Example: BIOS may want to protect different regions of BIOS from being erased
  - — Ranges can extend across region boundaries

21.2.5 Serial Flash Device Compatibility Requirements

A variety of serial Flash devices exist in the market. For a serial Flash device to be compatible with the processor SPI bus, it must meet the minimum requirements detailed in the following sections.

Note: To support a SPI controller clock frequency of 50 MHz, the attached SPI flash device must meet 66 MHz timing requirements.

21.2.5.1 BIOS SPI Flash Requirements

The SPI Flash device must meet the following minimum requirements when used explicitly for system BIOS storage.

- Erase size capability of at least one of the following: 64 Kbytes, 8 Kbytes, 4 Kbytes, or 256 bytes.
- Device must support multiple writes to a page without requiring a preceding erase cycle (Refer to Section 21.2.6.)
- Serial Flash device must ignore the upper address bits such that an address of FFFFFFh aliases to the top of the Flash memory.
- SPI Compatible Mode 0 support (clock phase is 0 and data is latched on the rising edge of the clock).
- If the device receives a command that is not supported or incomplete (less than 8 bits), the device must complete the cycle gracefully without any impact on the Flash content.
- An erase command (page, sector, block, chip, etc.) must set all bits inside the designated area (page, sector, block, chip, etc.) to 1 (Fh).
- Status Register bit 0 must be set to 1 when a write, erase or write to status register is in progress and cleared to 0 when a write or erase is NOT in progress.
- Devices requiring the Write Enable command must automatically clear the Write Enable Latch at the end of Data Program instructions.
- Byte write must be supported. The flexibility to perform a write between 1 byte to 64 bytes is recommended.
- Hardware Sequencing requirements are optional in BIOS only platforms.
- SPI Flash devices that do not meet hardware sequencing command set requirements may work in BIOS only platforms using software sequencing.
- If implementing two SPI flash devices, both devices must have the same erasable block/sector size. Additionally, the first device must be of a binary size.

21.2.5.2 Intel® Trusted Execution Engine Firmware SPI Flash Requirements

Intel Trusted Execution Engine Firmware must meet all the requirements in Section 21.2.5.1 plus:

- Hardware sequencing
- The Flash device must have a uniform 4-KB erasable block throughout the entire device or have 64 KB blocks with the first block (lowest address) divided into 4-KB or 8-KB blocks.
- The write protection scheme must meet SPI Flash unlocking requirements for the Trusted Execution Engine

SPI Flash Unlocking Requirements for the Trusted Execution Engine

Flash devices must be globally unlocked (read, write and erase access on the Trusted Execution Engine region) from power on by writing 00h to the Flash's status register to disable write protection.

If the status register must be unprotected, it must use the enable write status register command 50h or write enable 06h.

Opcode 01h (write to status register) must then be used to write a single byte of 00h into the status register. This must unlock the entire device. If the SPI Flash's status register has non-volatile bits that must be written to, bits [5:2] of the Flash's status register must be all 0h to indicate that the Flash is unlocked.

If bits [5:2] return a non zero values, the Trusted Execution Engine firmware will send a write of 00h to the status register. This must keep the Flash part unlocked.

If there is no need to execute a write enable on the status register, then opcodes 06h and 50h must be ignored.

After global unlock, the BIOS has the ability to lock down small sections of the Flash as long as they do not involve the Trusted Execution Engine.

21.2.5.3 Hardware Sequencing Requirements

Below table contains a list of commands and the associated opcodes that a SPI-based serial Flash device must support in order to be compatible with hardware sequencing.

Table 157. Hardware Sequencing Commands and Opcode Requirements (Sheet 1 of 2)

Commands	Opcode	Notes
Write to Status Register	01h	Writes a byte to SPI Flash's status register. Enable Write to Status Register command must be run prior to this command.
Program Data	02h	Single byte or 64 byte write as determined by Flash part capabilities and software.
Read Data	03h	
Write Disable	04h	

Table 157. Hardware Sequencing Commands and Opcode Requirements (Sheet 2 of 2)

Commands	Opcode	Notes
Read Status	05h	Outputs contents of SPI Flash's status register
Write Enable	06h	
Fast Read	0Bh	
Enable Write to Status Register	50h	Enables a bit in the status register to allow an update to the status register
Erase	Programmable	Uses the value from LVSSC.LEO register or UVSSC.UEO register depending on the FLA and whether it is below or above the FPBA respectively

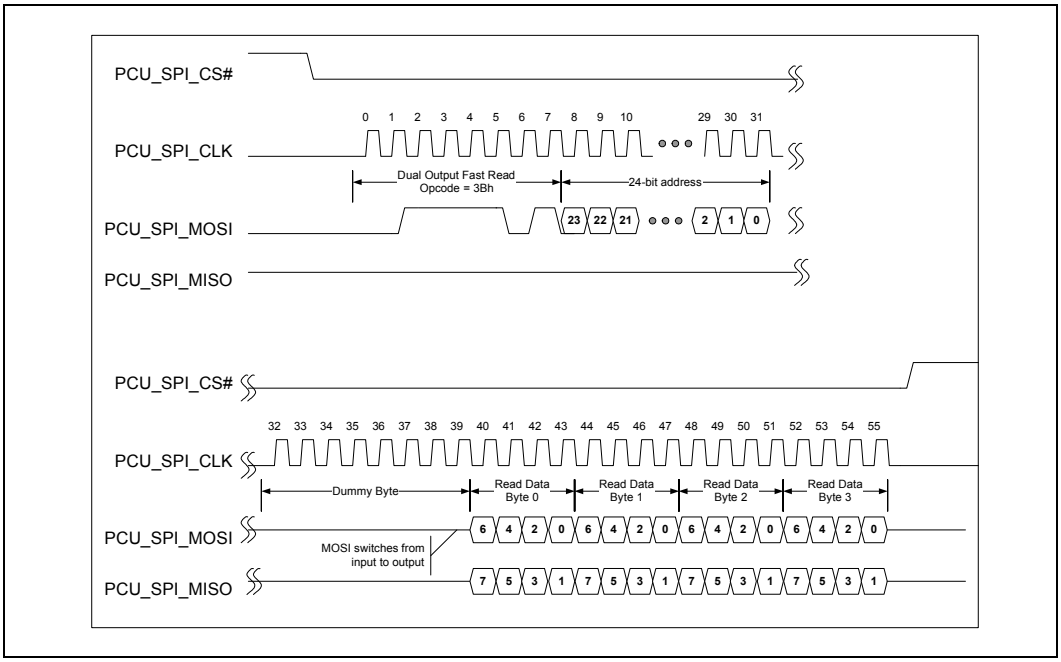
Single Input, Dual Output Fast Read

The SPI controller supports the functionality of a single input, dual output fast read: Opcode 3Bh. This instruction has the same timing (including a dummy byte) and the same frequencies as the Fast Read instruction, with the difference that the read data from the Flash is presented on both the MISO and MOSI pins. During a Dual Read instruction, the odd data bits are on the MISO pin and the even data bits are on the MOSI pin.

Note: When Dual Output Fast Read Support is enabled the Fast Read Support must be enabled as well.

Note: Micronix* SPI Flash uses a different opcode for dual fast read, and requires that during the address phase that the address bits are sent on both MOSI and MISO. The processor does not support this implementation of the protocol.

Figure 31. Dual Output Fast Read Timing



JEDEC ID

Since each serial Flash device may have unique capabilities and commands, the JEDEC ID is the necessary mechanism for identifying the device so the uniqueness of the device can be comprehended by the controller (master). The JEDEC ID uses the opcode 9Fh and a specified implementation and usage model. This JEDEC Standard Manufacturer and Device ID read method is defined in Standard JESD21-C, PRN03-NV.

Error Correction & Detection

If the first 8 bits specify an opcode which is not supported the slave will not respond and wait for the next high to low transition on PCU_SPI_CS[1:0]#. The SPI controller should automatically discard 8 bit words that were not completely received upon de-assertion of the signal.

Any other error correction or detection mechanisms must be implemented in firmware and/or software.

21.2.6 Multiple Page Write Usage Model

The BIOS and Trusted Execution Engine firmware usage models require that the serial Flash device support multiple writes to a page (minimum of 512 writes) without requiring a preceding erase command. The BIOS commonly uses capabilities such as counters that are used for error logging and system boot progress logging. These counters are typically implemented by using byte-writes to 'increment' the bits within a

page that have been designated as the counter. The Trusted Execution Engine firmware usage model requires the capability for multiple data updates within any given page. These data updates occur using byte-writes without executing a preceding erase to the given page. Both the BIOS and Trusted Execution Engine firmware multiple page write usage models apply to sequential and non-sequential data writes.

This usage model requirement is based on any given bit only being written once from a '1' to a '0'without requiring the preceding erase. An erase would be required to change bits back to the 1 state.

21.2.7 Soft Flash Protection

There are two types of Flash protection that are not defined in the Flash descriptor supported by the SPI controller:

1. Flash Range Read and Write Protection
2. Global Write Protection

21.2.7.1 Flash Range Read and Write Protection

The SPI controller provides a method for blocking reads and writes to specific ranges in the Flash when the Protected Ranges are enabled. This is achieved by checking the read or write cycle type and the address of the requested command against the base and limit fields of a Read or Write Protected range. Protected range registers are only applied to Programmed Register accesses and have no effect on Direct Reads.

Note: Once BIOS has locked down the Protected BIOS Range registers, this mechanism remains in place until the next system reset.

21.2.7.2 Global Write Protection

The SPI controller has a Write Protection Disable (BCR.WPD) configuration bit. When BCR.WPD=0b, BIOS is not able to perform any write or erase commands to the Flash. When BCR.WPD=1b, protection against BIOS erase and rewrite is disabled. When the lock enable (BCR.LE) bit is set, the BIOS can disable this protection only during System Management Mode (SMM) execution.

If BCR.LE=1b, the SPI controller confirms that only SMM code succeeds to set BCR.WPD=1b. In addition, if BCS.SMIWPEN=1b, the SPI controller should initiate an SMI when non SMM code tries to set BCR.WPD=1b.

21.2.8 SPI Flash Device Recommended Pinout

This table contains the recommended serial Flash device pin-out for an 8-pin device. Use of the recommended pin-out on an 8-pin device reduces complexities involved with designing the serial Flash device onto a motherboard and allows for support of a common footprint usage model (refer to Section 21.2.9.1).

Table 158. Recommended Pinout for 8-Pin Serial Flash Device

Pin #	Signal
1	Chips Select
2	Data Output
3	Write Protect
4	Ground
5	Data Input
6	Serial Clock
7	Hold / Reset
8	Supply Voltage

Although an 8-pin device is preferred over a 16-pin device due to footprint compatibility, Table 159 contains the recommended serial Flash device pin-out for a 16-pin SOIC.

21.2.9 Serial Flash Device Package

Table 159. Recommended Pinout for 16-Pin Serial Flash Device

Pin #	Signal	Pin #	Signal
1	Hold / Reset	9	Write Protect
2	Supply Voltage	10	Ground
3	No Connect	11	No Connect
4	No Connect	12	No Connect
5	No Connect	13	No Connect
6	No Connect	14	No Connect
7	Chip Select	15	Serial Data In
8	Serial Data Out	16	Serial Clock

21.2.9.1 Common Footprint Usage Model

To minimize platform motherboard redesign and to enable platform Bill of Material (BOM) selectability, many OEMs design their motherboard with a single common footprint. This common footprint allows the population of a soldered down device or a socket that accepts a leadless device. This enables the board manufacturer to support, using selection of the appropriate BOM, either of these solutions on the same system without requiring any board redesign.

The common footprint usage model is desirable during system debug and by Flash content developers since the leadless device can be easily removed and reprogrammed without damage to device leads. When the board and Flash content is mature for high-volume production, both the socketed leadless solution and the soldered down leaded solution are available through BOM selection.

21.2.9.2 Serial Flash Device Package Recommendations

It is highly recommended that the common footprint usage model be supported. An example of how this can be accomplished is as follows:

- The recommended pinout for 8-pin serial Flash devices is used (refer to Table 158).
- The 8-pin device is supported in either an 8-contact VDFPN (6x5 mm MLP) package or an 8-contact WSON (5x6 mm) package. These packages can fit into a socket that is land pattern compatible with the wide body SO8 package.
- The 8-pin device is supported in the SO8 (150 mil) and in the wide-body SO8 (200 mil) packages.
- The 16-pin device is supported in the SO16 (300 mil) package.

21.3 Use

21.3.1 Hardware vs. Software Sequencing

Hardware and Software sequencing are the two methods the processor uses to communicate with the Flash via programming registers for each of the three masters.

21.3.1.1 Hardware Sequencing

Hardware sequencing has a predefined list of opcodes, see Table 157 for more details, with only the erase opcode being programmable. This mode is only available if the descriptor is present and valid. Security Engine firmware must use HW sequencing; thus, BIOS must properly set up the processor to account for this. The Host VSCC registers and VSCC Table have to be correctly configured for BIOS and Security Engine have read/write access to SPI.

21.3.1.2 Software Sequencing

All commands other than the standard (memory) reads must be programmed by the software in the Software Sequencing Control, Flash Address, Flash Data, and Opcode configuration registers. Software must issue either Read ID or Read JEDEC ID, or a combination of the two to determine what Flash component is attached. Based on the Read ID, software can determine the appropriate Opcode instructions sets to set in the program registers and at what SPI frequency to run the command.

Software must program the Flash Linear Address for all commands, even for those commands that do not require address such as the Read ID or Read Status. This is because the SPI controller uses the address to determine which chip select to use.

The opcode type and data byte count fields determine how many clocks to run before deasserting the chip enable. The Flash data is always shifted in for the number of bytes specified and the Flash Data out is always shifted out for the number of data bytes specified. Note that the hardware restricts the burst lengths that are allowed.

A status bit indicates when the cycle has completed on the SPI port allowing the host to know when read results can be checked and/or when to initiate a new command.

The controller also provides the "Atomic Cycle Sequence" for performing erases and writes to the SPI Flash. When this bit is 1 (and the Go bit is written to 1), a sequence of cycles is performed on the SPI interface without allowing other SPI device to arbitrate and interleave cycles to the Flash device. In this case, the specified cycle is preceded by the Prefix Command (8-bit programmable Opcode) and followed by repeated reads to the Status Register (Opcode 05h) until bit 0 indicates the cycle has completed. The hardware does not attempt to check that the programmed cycle is a write or erase.

If a Programmed Access is initiated (Cycle Go written to 1) while the SPI controller is already busy with a Direct Memory Read, then the SPI Host hardware will hold the new Programmed Access pending until the preceding SPI access completes.

Once the SPI controller has committed to running a programmed access, subsequent writes to the programmed cycle registers that occur before it has completed will not modify the original transaction and will result in the assertion of the FCERR bit. Software should never purposely behave in this way and rely on this behavior. However, the FCERR bit provides basic error-reporting in this situation. Writes to the following registers cause the FCERR bit assertion in this situation:

- Software Sequencing Control
- Software Sequencing Address
- SPI Data

With the exception of Illegal Opcodes, the SPI controller does not police which opcodes are valid to be used in SW Sequencing. For example, if SW programs a Dual Output Fast Read opcode, then the Dual Output Fast Read cycle will be issued, independent of whether the Dual Output Fast Read enable bit was set in the component descriptor section.

21.4 PCU SPI for Firmware Memory Mapped I/O Registers

Table 160. Summary of PCU SPI for Firmware Memory Mapped I/O Registers—SPI_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"BFPREG (BIOS_Flash_Primary_Region_bios)—Offset 0h" on page 1061	00001FFFh
4h	2	"HSFSTS (Hardware_Sequencing_Flash_Status_bios)—Offset 4h" on page 1062	0000h
6h	2	"HSFCTL (Hardware_Sequencing_Flash_Control_bios)—Offset 6h" on page 1063	0000h
8h	4	"FADDR (Flash_Address_bios)—Offset 8h" on page 1064	00000000h
10h	4	"FDATA0 (Flash_Data_0_bios)—Offset 10h" on page 1065	00000000h
14h	4	"FDATA1 (Flash_Data_1_bios)—Offset 14h" on page 1065	00000000h
18h	4	"FDATA2 (Flash_Data_2_bios)—Offset 18h" on page 1066	00000000h
1Ch	4	"FDATA3 (Flash_Data_3_bios)—Offset 1Ch" on page 1066	00000000h
20h	4	"FDATA4 (Flash_Data_4_bios)—Offset 20h" on page 1067	00000000h
24h	4	"FDATA5 (Flash_Data_5_bios)—Offset 24h" on page 1067	00000000h
28h	4	"FDATA6 (Flash_Data_6_bios)—Offset 28h" on page 1068	00000000h
2Ch	4	"FDATA7 (Flash_Data_7_bios)—Offset 2Ch" on page 1068	00000000h
30h	4	"FDATA8 (Flash_Data_8_bios)—Offset 30h" on page 1069	00000000h
34h	4	"FDATA9 (Flash_Data_9_bios)—Offset 34h" on page 1069	00000000h
38h	4	"FDATA10 (Flash_Data_10_bios)—Offset 38h" on page 1070	00000000h
3Ch	4	"FDATA11 (Flash_Data_11_bios)—Offset 3Ch" on page 1070	00000000h
40h	4	"FDATA12 (Flash_Data_12_bios)—Offset 40h" on page 1071	00000000h
44h	4	"FDATA13 (Flash_Data_13_bios)—Offset 44h" on page 1071	00000000h
48h	4	"FDATA14 (Flash_Data_14_bios)—Offset 48h" on page 1072	00000000h
4Ch	4	"FDATA15 (Flash_Data_15_bios)—Offset 4Ch" on page 1072	00000000h
50h	4	"FRACC (Flash_Region_Access_Permissions_bios)—Offset 50h" on page 1073	00000202h
54h	4	"FREG0 (Flash_Region_0_bios)—Offset 54h" on page 1074	00001FFFh
58h	4	"FREG1 (Flash_Region_1_bios)—Offset 58h" on page 1074	00001FFFh
5Ch	4	"FREG2 (Flash_Region_2_bios)—Offset 5Ch" on page 1075	00001FFFh
60h	4	"FREG3 (Flash_Region_3_bios)—Offset 60h" on page 1076	00001FFFh
64h	4	"FREG4 (Flash_Region_4_bios)—Offset 64h" on page 1077	00001FFFh
74h	4	"PR0 (Protected_Range_0_bios)—Offset 74h" on page 1077	00000000h
78h	4	"PR1 (Protected_Range_1_bios)—Offset 78h" on page 1078	00000000h
7Ch	4	"PR2 (Protected_Range_2_bios)—Offset 7Ch" on page 1079	00000000h
80h	4	"PR3 (Protected_Range_3_bios)—Offset 80h" on page 1080	00000000h
84h	4	"PR4 (Protected_Range_4_bios)—Offset 84h" on page 1080	00000000h
90h	4	"SSFCTLSTS (Software_Sequencing_Flash_Control_Status_bios)—Offset 90h" on page 1082	F8000000h
94h	2	"PREOP (Prefix_Opcode_Configuration_bios)—Offset 94h" on page 1084	0000h
96h	2	"OPTYPE (Opcode_Type_Configuration_bios)—Offset 96h" on page 1085	0000h
98h	4	"OPMENU0 (Opcode_Menu_Configuration_0_bios)—Offset 98h" on page 1086	00000000h

Table 160. Summary of PCU SPI for Firmware Memory Mapped I/O Registers—SPI_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
9Ch	4	"OPMENU1 (Opcode_Menu_Configuration_1_bios)—Offset 9Ch" on page 1087	00000000h
A4h	4	"LOCK (Individual_Lock_Register)—Offset A4h" on page 1087	00000000h
B0h	4	"FDOC (Flash_Descriptor_Observability_Control_bios)—Offset B0h" on page 1089	00000000h
B4h	4	"FDOD (Flash_Descriptor_Observability_Data_bios)—Offset B4h" on page 1089	00000000h
C0h	4	"AFC (Additional_Flash_Control_bios)—Offset C0h" on page 1090	00000000h
C4h	4	"LVSCC (Lower_Vendor_Specific_Component_Capabilities_bios)—Offset C4h" on page 1091	00000000h
C8h	4	"UVSCC (Upper_Vendor_Specific_Component_Capabilities_bios)—Offset C8h" on page 1092	00000000h
D0h	4	"FPB (Flash_Partition_Boundary_bios)—Offset D0h" on page 1093	00000000h
F8h	4	"SCS (SMI_Control_Status_Register_bios)—Offset F8h" on page 1093	00000080h
FCh	4	"BCR (BIOS_Control_Register_bios)—Offset FCh" on page 1094	00000020h
100h	4	"TCGC (Trunk_Clock_Gating_Control_bios)—Offset 100h" on page 1095	00000510h

21.4.1 BFPREG (BIOS_Flash_Primary_Region_bios)—Offset 0h

BIOS flash primary region addresses

Access Method

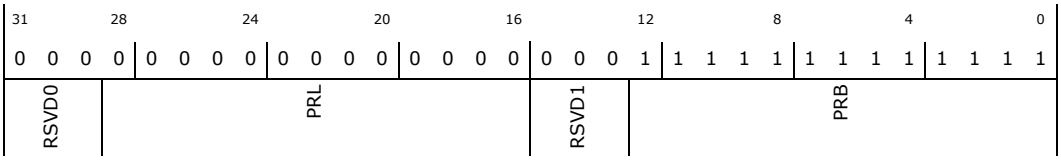
Type: Memory Mapped I/O Register (Size: 32 bits)

BIOS_Flash_Primary_Region_bios: [SPI_BASE_ADDRESS] + 0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**BIOS Flash Primary Region Limit (PRL):** This specifies address bits 24:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG1.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**BIOS Flash Primary Region Base (PRB):** This specifies address bits 24:12 for the Primary Region Base The value in this register iloaded from the contents in the Flash Descriptor.FLREG1.Region Base

21.4.2 HSFSTS (Hardware_Sequencing_Flash_Status_bios)—Offset 4h

Hardware sequencing flash status Note: If operating in Non-Descriptor mode, the Software Sequencing Flash Status register must be used.

Access Method

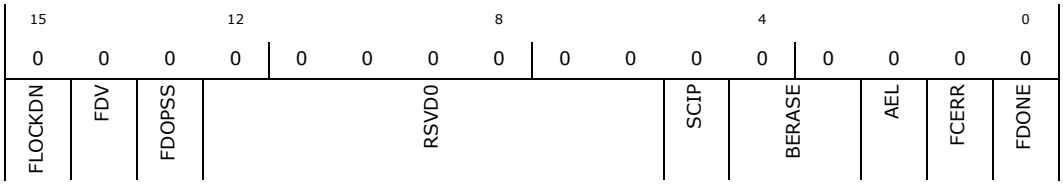
Type: Memory Mapped I/O Register (Size: 16 bits)

Hardware_Sequencing_Flash_Status_bios: [SPI_BASE_ADDRESS] + 4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW/L	**Flash Configuration Lock-Down (FLOCKDN):** When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
14	0b RO	**Flash Descriptor Valid (FDV):** This bit is set to a 1 if the Flash Controller read the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1 , software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	0b RO	**Flash Descriptor Override Pin-Strap Status (FDOPSS):** This register reflects the value the Flash Descriptor Override Pin-Strap. '1': No override '0': The Flash Descriptor Overide strap is set
12:6	0b RO	**RSVD0:** Reserved
5	0b RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4:3	00b RO	**Block/Sector Erase Size (BERASE):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 : 256 Byte 01 : 4K Byte 10 : 8K Byte 11 : 64K Byte If the FLA (FPBA then this field reflects the value in the LVSCC.LBES register. If the FLA)= FPBA then this field reflects the value in the UVSCC.UBES register.
2	0b RW/1C	**Access Error Log (AEL):** Hardware sets this bit to a 1 when a direct read was made by BIOS that violated the security restrictions. Or , when a SB transaction to read/write one of the BIOS registers was accepted with bad SAI - see security table. This bit has no affect on indirect accesses. This bit is cleared by software writing a 1.
1	0b RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1 when an program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occures. Software must clear this bit before setting the FLASH Cycle GO bit in this register.

Bit Range	Default & Access	Description
0	0b RW/1C	**Flash Cycle Done (FDONE):** The SPI controller sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

21.4.3 HSFCTL (Hardware_Sequencing_Flash_Control_bios)—Offset 6h

Hardware sequencing flash control.

Access Method

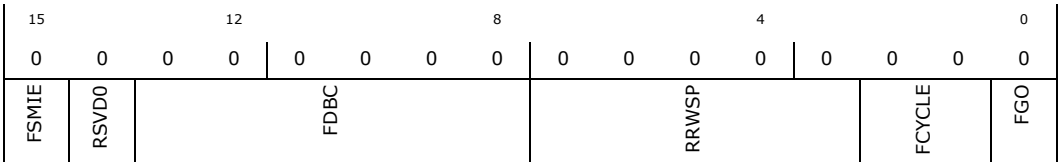
Type: Memory Mapped I/O Register (Size: 16 bits)

Hardware_Sequencing_Flash_Control_bios: [SPI_BASE_ADDRESS] + 6h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 0000h



Bit Range	Default & Access	Description
15	0b RW	**Flash SPI SMI# Enable (FSMIE):** When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
14	0b RO	**RSVD0:** Reserved
13:8	00h RW	**Flash Data Byte Count (FDBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b reprenting 1 byte and 111111b representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
7:3	00h RW	**Reserved RW Scratch Pad (RRWSP):** Reserved: Scratch Pad bits that are R/W to be used during ECO
2:1	00b RW	**FLASH Cycle (FCYCLE):** This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 Read (1 up to 64 bytes by setting FDBC) 01 Reserved 10 Write (1 up to 64 bytes by setting FDBC) 11 Block Erase Implementation Note: if reserved 2'b01 is programmed to this field, flash controller will handle it as if it is 00 (Read)
0	0b RW/SE	**Flash Cycle Go (FGO):** A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.

21.4.4 FADDR (Flash_Address_bios)—Offset 8h

Flash address

Access Method

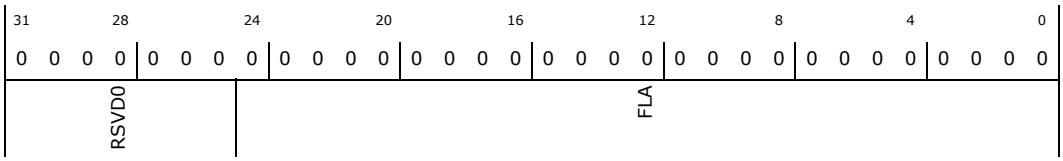
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Address_bios: [SPI_BASE_ADDRESS] + 8h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:25	0b RO	**RSVD0:** Reserved
24:0	00000000h RW	**Flash Linear Address (FLA):** The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus. When operating in Tekoa mode bit 24 is ignored and the FLA[lb]13:0[rb] is the FPA.

21.4.5 FDATA0 (Flash_Data_0_bios)—Offset 10h

Flash data #0

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

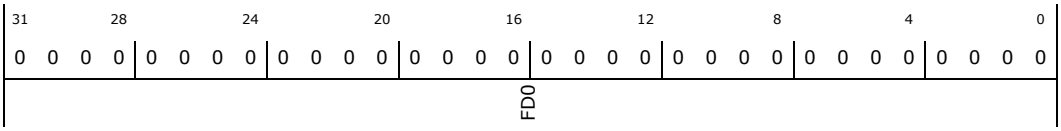
Flash_Data_0_bios: [SPI_BASE_ADDRESS] + 10h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 0 (FD0):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- 8-23-22- 16-31 24 Bit 24 is the last bit shifted out/in. There are no alignment assumptions, byte 0 always represents the value specified by the cycle address. Note that the data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

21.4.6 FDATA1 (Flash_Data_1_bios)—Offset 14h

Flash data #1

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

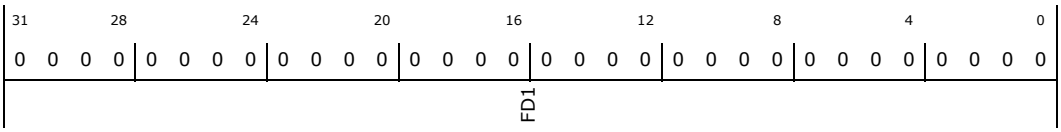
Flash_Data_1_bios: [SPI_BASE_ADDRESS] + 14h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 1 (FD1):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD0 has completely shifted in/out.

21.4.7 FDATA2 (Flash_Data_2_bios)—Offset 18h

Flash data #2

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

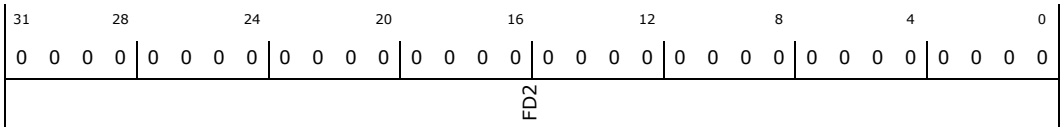
Flash_Data_2_bios: [SPI_BASE_ADDRESS] + 18h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 2 (FD2):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD1 has completely shifted in/out.

21.4.8 FDATA3 (Flash_Data_3_bios)—Offset 1Ch

Flash data #3

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

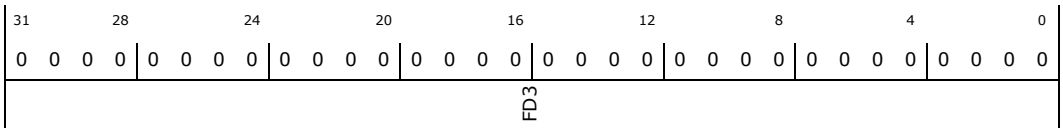
Flash_Data_3_bios: [SPI_BASE_ADDRESS] + 1Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 3 (FD3):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD2 has completely shifted in/out.

21.4.9 FDATA4 (Flash_Data_4_bios)—Offset 20h

Flash data #4

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

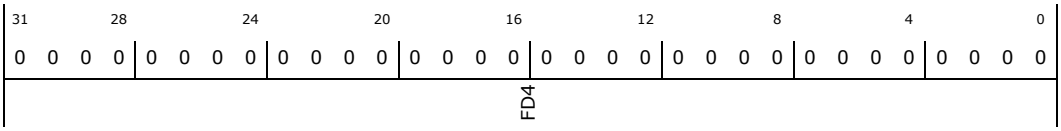
Flash_Data_4_bios: [SPI_BASE_ADDRESS] + 20h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 4 (FD4):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD3 has completely shifted in/out.

21.4.10 FDATA5 (Flash_Data_5_bios)—Offset 24h

Flash data #5

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

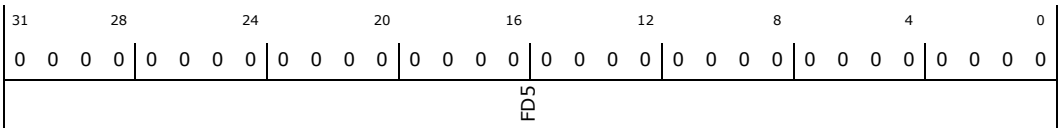
Flash_Data_5_bios: [SPI_BASE_ADDRESS] + 24h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 5 (FD5):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD4 has completely shifted in/out.

21.4.11 FDATA6 (Flash_Data_6_bios)—Offset 28h

Flash data #6

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

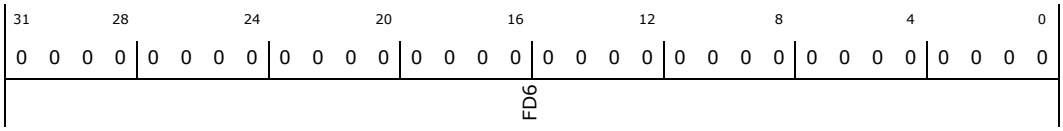
Flash_Data_6_bios: [SPI_BASE_ADDRESS] + 28h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 6 (FD6):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD5 has completely shifted in/out.

21.4.12 FDATA7 (Flash_Data_7_bios)—Offset 2Ch

Flash data #7

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

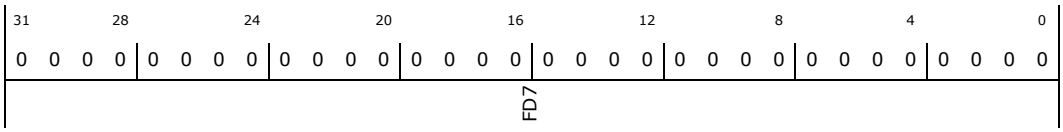
Flash_Data_7_bios: [SPI_BASE_ADDRESS] + 2Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 7 (FD7):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD6 has completely shifted in/out.

21.4.13 FDATA8 (Flash_Data_8_bios)—Offset 30h

Flash data #8

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

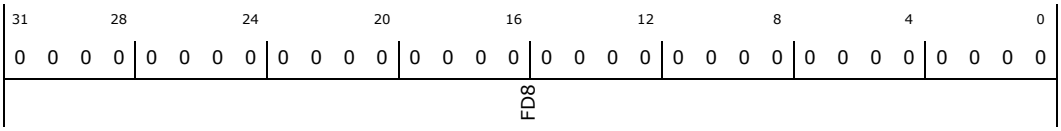
Flash_Data_8_bios: [SPI_BASE_ADDRESS] + 30h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 8 (FD8):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD7 has completely shifted in/out.

21.4.14 FDATA9 (Flash_Data_9_bios)—Offset 34h

Flash data #9

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

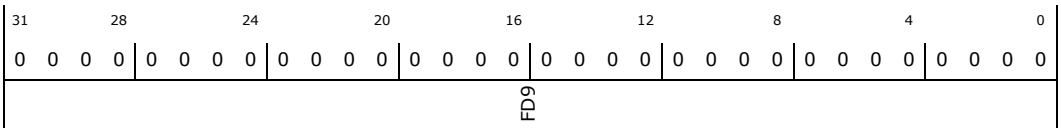
Flash_Data_9_bios: [SPI_BASE_ADDRESS] + 34h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 9 (FD9):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD8 has completely shifted in/out.

21.4.15 FDATA10 (Flash_Data_10_bios)—Offset 38h

Flash data #10

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

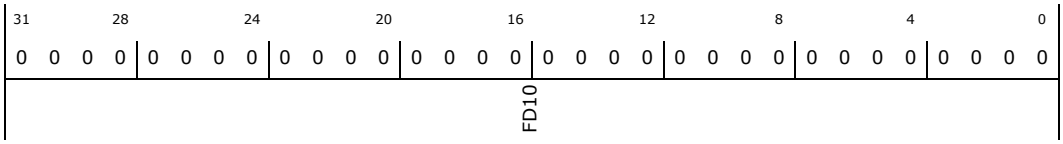
Flash_Data_10_bios: [SPI_BASE_ADDRESS] + 38h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 10 (FD10):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD9 has completely shifted in/out.

21.4.16 FDATA11 (Flash_Data_11_bios)—Offset 3Ch

Flash data #11

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

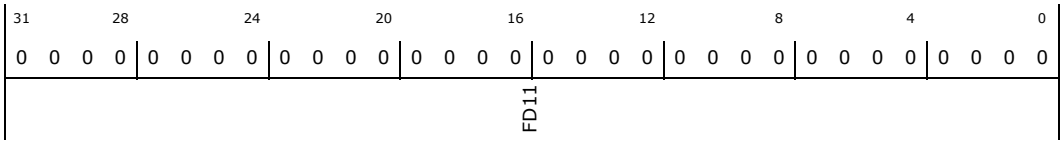
Flash_Data_11_bios: [SPI_BASE_ADDRESS] + 3Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 11 (FD11):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD10 has completely shifted in/out.

21.4.17 FDATA12 (Flash_Data_12_bios)—Offset 40h

Flash data #12

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

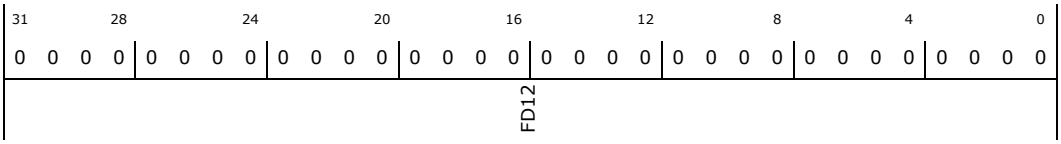
Flash_Data_12_bios: [SPI_BASE_ADDRESS] + 40h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 12 (FD12):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD11 has completely shifted in/out.

21.4.18 FDATA13 (Flash_Data_13_bios)—Offset 44h

Flash data #13

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

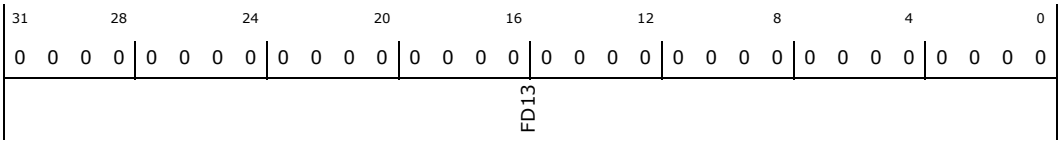
Flash_Data_13_bios: [SPI_BASE_ADDRESS] + 44h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 13 (FD13):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD12 has completely shifted in/out.

21.4.19 FDATA14 (Flash_Data_14_bios)—Offset 48h

Flash data #14

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

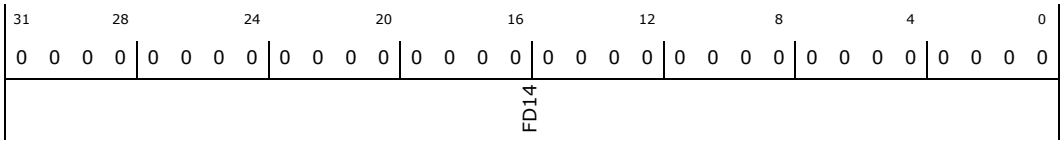
Flash_Data_14_bios: [SPI_BASE_ADDRESS] + 48h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 14 (FD14):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD13 has completely shifted in/out.

21.4.20 FDATA15 (Flash_Data_15_bios)—Offset 4Ch

Flash data #15

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

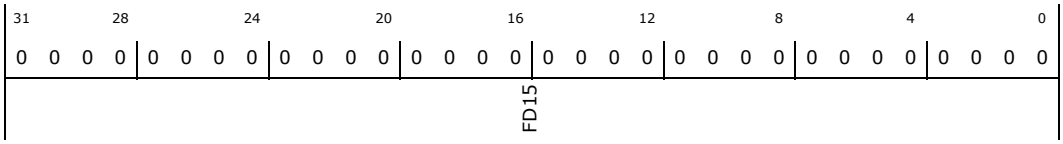
Flash_Data_15_bios: [SPI_BASE_ADDRESS] + 4Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RW	**Flash Data 15 (FD15):** Similar definition as Flash Data 0. However, this register does not begin shifting until FD14 has completely shifted in/out.

21.4.21 FRACC (Flash_Region_Access_Permissions_bios)—Offset 50h

Flash region access permissions

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

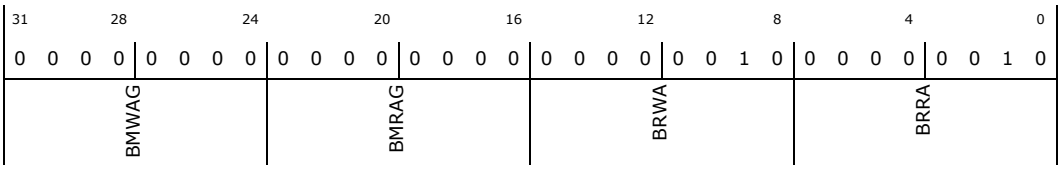
Flash_Region_Access_Permissions_bios: [SPI_BASE_ADDRESS] + 50h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000202h



Bit Range	Default & Access	Description
31:24	00h RW/L	**BIOS Master Write Access Grant (BMWAG):** Each bit [lb]31:24[rb] corresponds to Master[lb]7:0[rb]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/BIOS, Master[lb]2[rb] is SEC, Master[lb]3[rb] is GBE. Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN or BMWAGLOCKDN bits.
23:16	00h RW/L	**BIOS Master Read Access Grant (BMRAG):** Each bit [lb]23:16[rb] corresponds to Master[lb]7:0[rb]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. Master[lb]1[rb] is Host CPU/BIOS, Master[lb]2[rb] is SEC, Master[lb]3[rb] is GBE. Master[lb]0[rb] and Master[lb]7:4[rb] are reserved. The contents of this register are locked by the FLOCKDN or BMRAGLOCKDN bit.
15:8	02h RO	**BIOS Region Write Access (BRWA):** Each bit [lb]15:8[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can erase and write that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS write permissions in their Master Write Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the write access to its own Region 1 by default. Thus, the reset default of this field will be read as 8'h02 regardless of descriptor or non-descriptor mode.
7:0	02h RO	**BIOS Region Read Access (BRRA):** Each bit [lb]7:0[rb] corresponds to Regions [lb]7:0[rb]. If the bit is set, this master can read that particular region through register accesses. The contents of this register are that of the Flash Descriptor.Flash Master 1.Master Region Write Access OR a particular master has granted BIOS read permissions in their Master Read Access Grant register OR the Flash Descriptor Security Override strap is set. BIOS always have the read access to its own Region 1 by default. Thus, the reset default of this field will be read as 8'h02 regardless of descriptor or non-descriptor mode.

21.4.22 FREG0 (Flash_Region_0_bios)—Offset 54h

Flash region 0 (flash descriptor)

Access Method

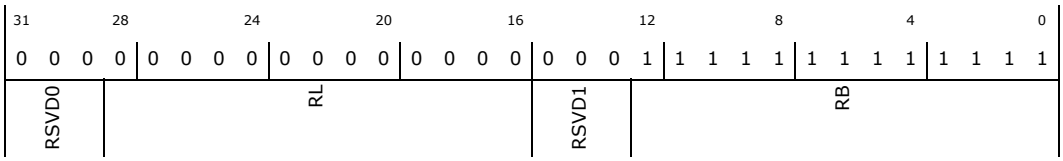
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_0_bios: [SPI_BASE_ADDRESS] + 54h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base

21.4.23 FREG1 (Flash_Region_1_bios)—Offset 58h

Flash region 1 (BIOS)

Access Method

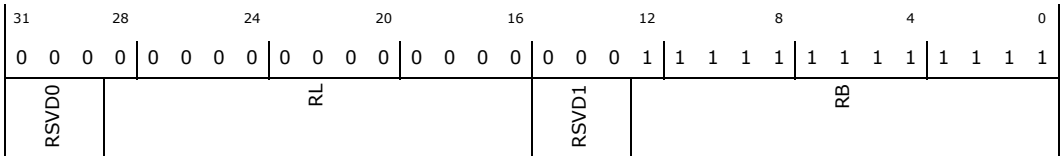
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_1_bios: [SPI_BASE_ADDRESS] + 58h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit

Bit Range	Default & Access	Description
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 1 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base

21.4.24 FREG2 (Flash_Region_2_bios)—Offset 5Ch

Flash region 2 (SEC)

Access Method

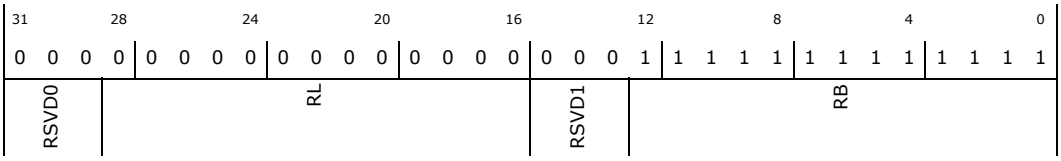
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_2_bios: [SPI_BASE_ADDRESS] + 5Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base

21.4.25 FREG3 (Flash_Region_3_bios)—Offset 60h

Flash region 3 (GBE)

Access Method

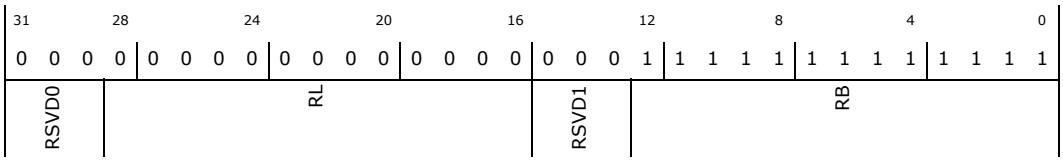
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_3_bios: [SPI_BASE_ADDRESS] + 60h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base

21.4.26 FREG4 (Flash_Region_4_bios)—Offset 64h

Flash region 4 (platform data)

Access Method

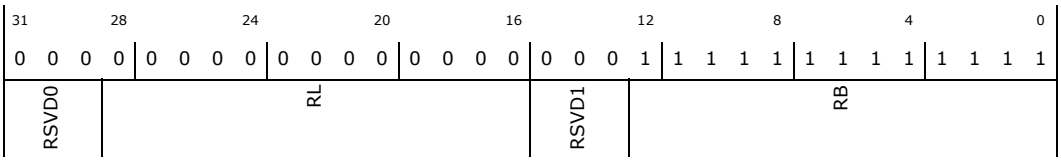
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Region_4_bios: [SPI_BASE_ADDRESS] + 64h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00001FFFh



Bit Range	Default & Access	Description
31:29	0b RO	**RSVD0:** Reserved
28:16	0000h RO	**Region Limit (RL):** This specifies address bits 24:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit
15:13	0b RO	**RSVD1:** Reserved
12:0	1FFFh RO	**Region Base (RB):** This specifies address bits 24:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base

21.4.27 PR0 (Protected_Range_0_bios)—Offset 74h

Protected range #0. This register can not be written when the FLOCKDN or PR0LOCKDN bits are set to 1.

Access Method

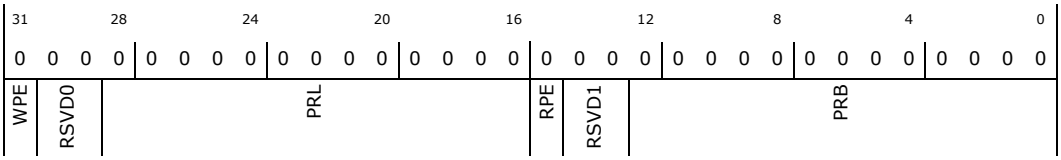
Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_0_bios: [SPI_BASE_ADDRESS] + 74h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.

Bit Range	Default & Access	Description
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.4.28 PR1 (Protected_Range_1_bios)—Offset 78h

Protected range #1. This register can not be written when the FLOCKDN or PR1LOCKDN bits are set to 1.

Access Method

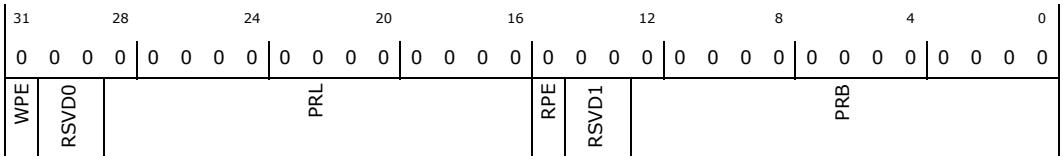
Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_1_bios: [SPI_BASE_ADDRESS] + 78h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.

Bit Range	Default & Access	Description
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.4.29 PR2 (Protected_Range_2_bios)—Offset 7Ch

Protected range #2. This register can not be written when the FLOCKDN or PR2LOCKDN bits are set to 1.

Access Method

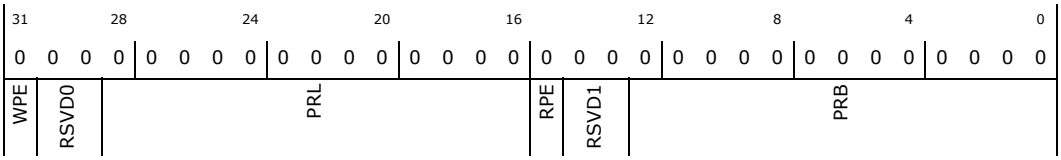
Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_2_bios: [SPI_BASE_ADDRESS] + 7Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.4.30 PR3 (Protected_Range_3_bios)—Offset 80h

Protected range #3. This register can not be written when the FLOCKDN or PR3LOCKDN bits are set to 1.

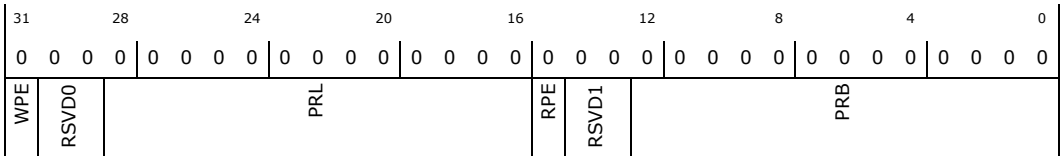
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_3_bios: [SPI_BASE_ADDRESS] + 80h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31	0b RW/L	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	0b RO	**RSVD0:** Reserved
28:16	0000h RW/L	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	0b RW/L	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	0b RO	**RSVD1:** Reserved
12:0	0000h RW/L	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

21.4.31 PR4 (Protected_Range_4_bios)—Offset 84h

Protected range #4. This register use for H/W range protection. All register values are coming from soft-straps, and the Write Protection Enable is controlled also by the Flash Security Override Pin Strap

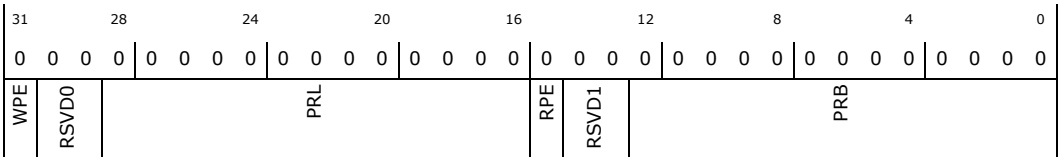
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Protected_Range_4_bios: [SPI_BASE_ADDRESS] + 84h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31	X RO	**Write Protection Enable (WPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. This field value should be an or between soft-strap and the ~Flash Security Override Pin Strap. Such, H/W range protection is active aonly if write protection is enabled by soft-strap and Flash Security Override Pin Strap is deasserted.
30:29	0b RO	**RSVD0:** Reserved
28:16	X RO	**Protected Range Limit (PRL):** This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be 12'hFFF for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range. This field value should be taken from soft-straps.
15	0b RO	**Read Protection Enable (RPE):** When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared. This field should be always 1'b0
14:13	0b RO	**RSVD1:** Reserved
12:0	X RO	**Protected Range Base (PRB):** This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 12'h000 for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range. This field value should be taken from soft-straps.

21.4.32 SSFCTLSTS (Software_Sequencing_Flash_Control_Status_bios)—Offset 90h

The software sequencing flash control and Status register is a combination of two registers the software sequencing flash status register (bits 7:0) and the software sequencing flash control register (bits 31:8). This register is intended to be used only as a back-up mode to the hardware sequencing control and status registers.

Access Method

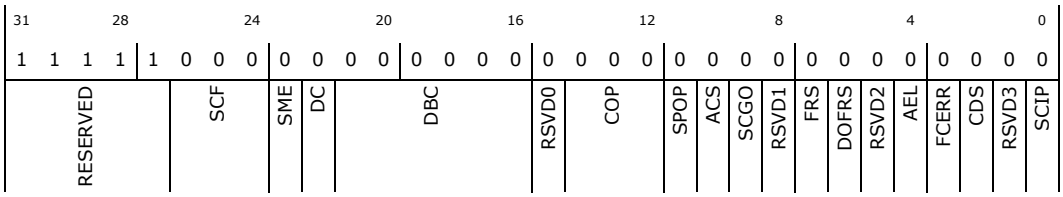
Type: Memory Mapped I/O Register (Size: 32 bits)

Software_Sequencing_Flash_Control_Status_bios: [SPI_BASE_ADDRESS] + 90h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: F8000000h



Bit Range	Default & Access	Description
31:27	11111b RO	**RESERVED:** reserved, should be with default 1
26:24	000b RW/L	**SPI Cycle Frequency (SCF):** 000 : 20MHz 001 : 33MHz 010 : 66MHz (reserved - not supported on VLV) 011 : 25MHz (reserved - not supported on VLV) 100 : 50MHz (reserved - not supported on VLV-DC) All Others: Reserved This register sets frequency to use for all SPI Software Sequencing cycles (write, erase, fast read, read status, .etc) except for the Read cycle which always run at 20MHz. This register is locked when the SPI Configuration Lock-Down bit is set or when FREQLOCKDN bit is set.
23	0b RW	**SPI SMI# Enable (SME):** When set to 1, the SPI asserts an SMI# request whenever the Cycle Done Status bit is 1.
22	0b RW	**Data Cycle (DC):** When set to 1, there is data that corresponds to this transaction. When 0, no data is dleivered for this cycle, and the DBC and data fields themselves are don t cares.
21:16	000000b RW	**Data Byte Count (DBC):** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. Note that when this field is 00_0000b, then there is 1 byte to transfer and that 11_1111b means there are 64 bytes to transfer.
15	0b RO	**RSVD0:** Reserved
14:12	000b RW	**Cycle Opcode Pointer (COP):** This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
11	0b RW	**Sequence Prefix Opcode Pointer (SPOP):** This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the SPI controller supports flash devices that have different opcodes for enabling writes to the data space vs. status register.

Bit Range	Default & Access	Description
10	0b RW	**Atomic Cycle Sequence (ACS):** When set to 1 along with the SCGO assertion, the SPI controller will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of:) Atomic Sequence Prefix Command (8-bit opcode only)) Primary Command specified below by software (can include address and data)) Polling the Flash Status Register (opcode 8'h05) until bit 0 becomes 1'b0. The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.
9	0b RW/SE	**SPI Cycle Go (SCGO):** This bit always returns 1'b0 on reads. However, a write to this register with a 1'b1 in this bit starts the SPI cycle defined by the other bits of this register. The SPI Cycle in Progress (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1'b1. This saves an additional memory write.
8	0b RO	**RSVD1:** Reserved
7	0b RO/U	**Fast Read Supported (FRS):** This bit reflects the value of the Fast Read Support bit in the Flash Descriptor Component Section.
6	0b RO/U	**Dual Output Fast Read Supported (DOFRS):** This bit reflects the value of the Dual Output Fast Read Support bit in the Flash Descriptor Component Section.
5	0b RO	**RSVD2:** Reserved
4	0b RO	**Access Error Log (AEL):** This bit reflects the value of the Hardware Sequencing Status.AEL register.
3	0b RW/1C	**Flash Cycle Error (FCERR):** Hardware sets this bit to 1'b1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset.
2	0b RW/1C	**Cycle Done Status (CDS):** The SPI controller sets this bit to 1'b1 when the SPI Cycle completes (that is, SCIP bit is 1'b0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1'b1 or hardware reset. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	0b RO	**RSVD3:** Reserved
0	0b RO	**SPI Cycle In Progress (SCIP):** Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 1'b0.

21.4.33 PREOP (Prefix_Opcode_Configuration_bios)—Offset 94h

Prefix opcode configuration. This register is not writable when the SPI Configuration Lock-Down bit is set or when the PREOPLOCKDN bit is set.

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

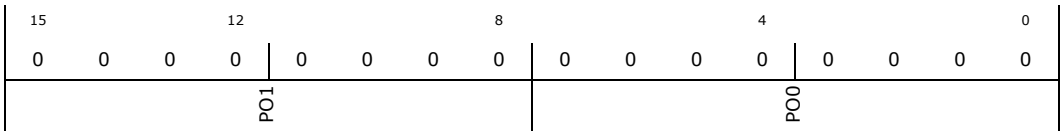
Prefix_Opcode_Configuration_bios: [SPI_BASE_ADDRESS] + 94h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 0000h



Bit Range	Default & Access	Description
15:8	00h RW/L	**Prefix Opcode 1 (PO1):** Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	00h RW/L	**Prefix Opcode 0 (PO0):** Prefix Opcode 0: Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

21.4.34 OPTYPE (Opcode_Type_Configuration_bios)—Offset 96h

Opcode type configuration. This register is not writable when the Flash Configuration Lock-Down bit is set or when the OPTYPELOCKDN bit is set. Entries in this register correspond to the entries in the Opcode Menu Configuration register. Note that the definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, Chip Erase and Auto-Address Increment Byte Program).

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

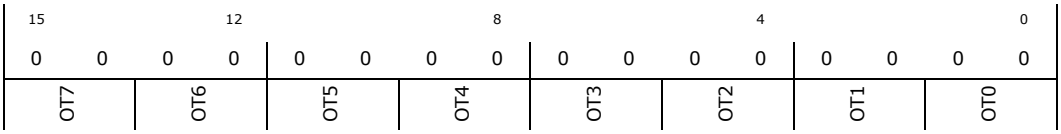
Opcode_Type_Configuration_bios: [SPI_BASE_ADDRESS] + 96h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 0000h



Bit Range	Default & Access	Description
15:14	00b RW/L	**Opcode Type 7 (OT7):** See the description for bits 1:0
13:12	00b RW/L	**Opcode Type 6 (OT6):** See the description for bits 1:0
11:10	00b RW/L	**Opcode Type 5 (OT5):** See the description for bits 1:0
9:8	00b RW/L	**Opcode Type 4 (OT4):** See the description for bits 1:0
7:6	00b RW/L	**Opcode Type 3 (OT3):** See the description for bits 1:0
5:4	00b RW/L	**Opcode Type 2 (OT2):** See the description for bits 1:0
3:2	00b RW/L	**Opcode Type 1 (OT1):** See the description for bits 1:0
1:0	00b RW/L	**Opcode Type 0 (OT0):** This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The hardware implementation also uses the read vs. write information for modifying the behavior of the SPI interface logic. The encoding of the two bits is: 00 = No Address associated with this Opcode and Read Cycle type 01 = No Address associated with this Opcode and Write Cycle type 10 = Address required, Read cycle type 11 = Address required, Write cycle type

21.4.35 OPMENU0 (Opcode_Menu_Configuration_0_bios)—Offset 98h

Opcode (0-3) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set or when OPMENULOCKDN bit is set. Four entries are available in this register and four are available in OPMENU1 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices. It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

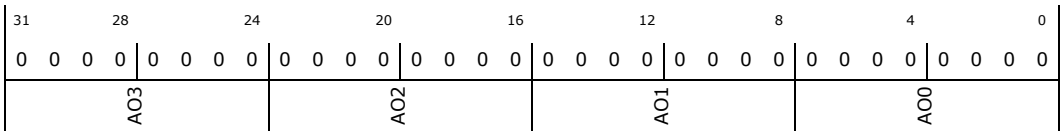
Opcode_Menu_Configuration_0_bios: [SPI_BASE_ADDRESS] + 98h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RW/L	**Allowable Opcode 3 (AO3):** See the description for bits 7:0
23:16	00h RW/L	**Allowable Opcode 2 (AO2):** See the description for bits 7:0
15:8	00h RW/L	**Allowable Opcode 1 (AO1):** See the description for bits 7:0
7:0	00h RW/L	**Allowable Opcode 0 (AO0):** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

21.4.36 OPMENU1 (Opcode_Menu_Configuration_1_bios)—Offset 9Ch

Opcode (7-4) Menu Configuration. This register is not writable when the SPI Configuration Lock-Down bit is set or when OPMENULOCKDN bit is set. Four entries are available in this register and four are available in OPMENU0 register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices. It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

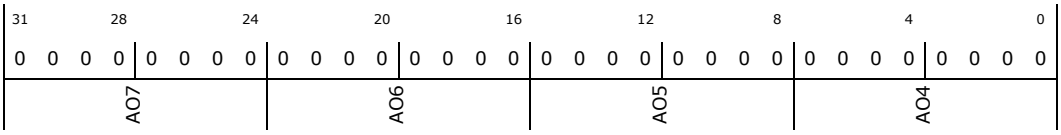
Opcode_Menu_Configuration_1_bios: [SPI_BASE_ADDRESS] + 9Ch

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:24	00h RW/L	**Allowable Opcode 7 (AO7):** See the description for bits 7:0 in OPMENU0
23:16	00h RW/L	**Allowable Opcode 6 (AO6):** See the description for bits 7:0 in OPMENU0
15:8	00h RW/L	**Allowable Opcode 5 (AO5):** See the description for bits 7:0 in OPMENU0
7:0	00h RW/L	**Allowable Opcode 4 (AO4):** See the description for bits 7:0 in OPMENU0

21.4.37 LOCK (Individual_Lock_Register)—Offset A4h

Used to individually lock each one of the registers formaly locked only by FLOCKDN bit. This register doesn't exclude FLOCKDN. It adds an individual option to lock each register in above to FLOCKDN.

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

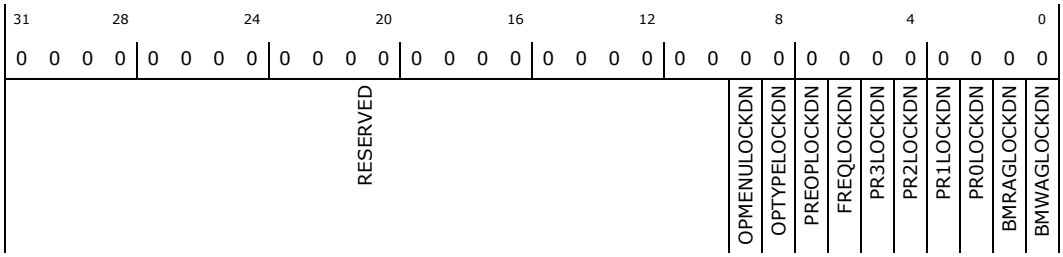
Individual_Lock_Register: [SPI_BASE_ADDRESS] + A4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:10	0000000000000000000000b RO	**RESERVED:** reserved, should be with default 0
9	0b RW/L	**OPMENU Lock-Down (OPMENULOCKDN):** When set to 1, OPMENU0 and OPMENU1 registers cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
8	0b RW/L	**OPTYPE Lock-Down (OPTYPELOCKDN):** When set to 1, OPTYPE register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
7	0b RW/L	**PREOP Lock-Down (PREOPLOCKDN):** When set to 1, PREOP register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
6	0b RW/L	**SCF Lock-Down (FREQLOCKDN):** When set to 1, SCF field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
5	0b RW/L	**PR3 Lock-Down (PR3LOCKDN):** When set to 1, PR3 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
4	0b RW/L	**PR2 Lock-Down (PR2LOCKDN):** When set to 1, PR2 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
3	0b RW/L	**PR1 Lock-Down (PR1LOCKDN):** When set to 1, PR1 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
2	0b RW/L	**PR0 Lock-Down (PR0LOCKDN):** When set to 1, PR0 register cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
1	0b RW/L	**BMRAG Lock-Down (BMRAGLOCKDN):** When set to 1, BMRAG field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.
0	0b RW/L	**BMWAG Lock-Down (BMWAGLOCKDN):** When set to 1, BMWAG field cannot be written. Once set to 1, this bit can only be cleared by a hardware reset.

21.4.38 FDOC (Flash_Descriptor_Observability_Control_bios)—Offset B0h

Flash Descriptor Observability Control. This is a test mode only register that can be used to observe the contents of the Flash Descriptor that is stored internally in the SPI Controller.

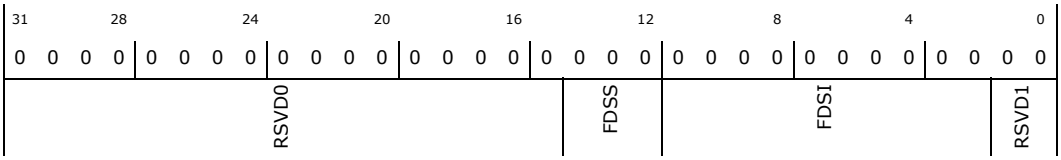
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Descriptor_Observability_Control_bios: [SPI_BASE_ADDRESS] + B0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:15	0b RO	**RSVD0:** Reserved
14:12	000b RW	**Flash Descriptor Section Select (FDSS):** Selects which section within the loaded Flash Descriptor to observe. 000 : Flash Signature and Descriptor Map 001 : Component 010 : Region 011 : Master 100 : Soft Straps 111 : Reserved
11:2	000h RW	**Flash Descriptor Section Index (FDSI):** Selects the DW offset within the Flash Descriptor Section to observe.
1:0	0b RO	**RSVD1:** Reserved

21.4.39 FDOD (Flash_Descriptor_Observability_Data_bios)—Offset B4h

Flash descriptor observability data

Access Method

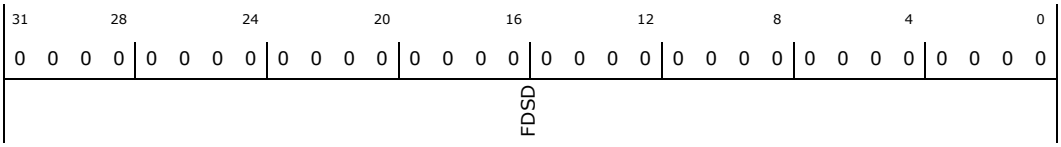
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Descriptor_Observability_Data_bios: [SPI_BASE_ADDRESS] + B4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Power Well: EPW

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Flash Descriptor Section Data (FDSD):** Contains the DW of data to observe as selected in the Flash Descriptor Observability Control. at default the FDSS==3'b000 hence this register contans the data of Flash Signature and Descriptor Map.

21.4.40 AFC (Additional_Flash_Control_bios)—Offset C0h

Additional flash control

Access Method

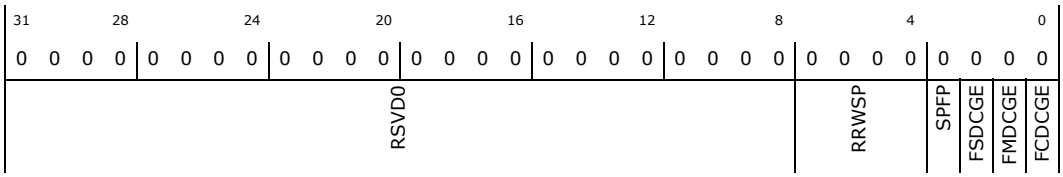
Type: Memory Mapped I/O Register (Size: 32 bits)

Additional_Flash_Control_bios: [SPI_BASE_ADDRESS] + C0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:4	0000b RW	**Reserved RW Scratch Pad (RRWSP):** Scratch Pad bits that are R/W to be used during ECO
3	0b RW	**Stop Prefetch on Flush Pending (SPFP):** When set to 1'b1, the in progress of a prefetch will be ended if subsequence access from the same master is detected to be a cache-miss and read cache will be flushed. When set to 1'b0, the prefetch will be allowed to complete prior to flushing.
2	0b RW	**Flash IOSF PRI Dynamic Clock Gating Enable (FSDCGE):** When set to 1'b1, the SPI controller IOSF-PRI interface logic can be dynamically clock gated. This register is only clear on a reset.
1	0b RW	**Flash IOSF SB Dynamic Clock Gating Enable (FMDCGE):** When set to 1'b1, the SPI controller IOSF-SB interface logic can be dynamically clock gated. This register is only clear on a reset.
0	0b RW	**Flash Core Dynamic Clock Gating Enable (FCDCGE):** When set to 1'b1, the SPI controller core logic can be dynamically clock gated. This register is only clear on a reset.

21.4.41 LVSCC (Lower_Vendor_Specific_Component_Capabilities_bios)—Offset C4h

Lower vendor specific component capabilities

Access Method

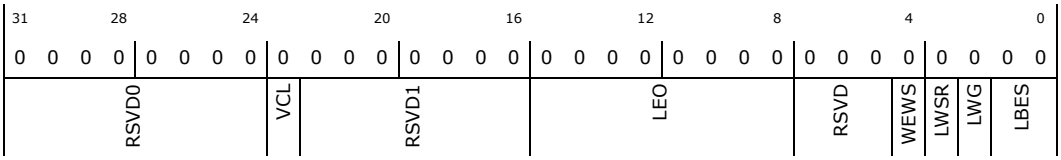
Type: Memory Mapped I/O Register (Size: 32 bits)

Lower_Vendor_Specific_Component_Capabilities_bios: [SPI_BASE_ADDRESS] + C4h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:24	0b RO	**RSVD0:** Reserved
23	0b RW/L	**Vendor Component Lock (VCL):** '0': The lock bit is not set '1': The Vendor Component Lock bit is set. This register locks itself when set. If this register is not set and the Flash is operating in Flash Mode (as opposed to EEPROM mode), then software cannot use hardware sequencing. This requirement is not enforced by hardware, but is a requirement of the the power-on usage model.
22:16	0b RO	**RSVD1:** Reserved
15:8	00h RW/L	**Lower Erase Opcode (LEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address.
7:5	000b RW/L	**Reserved RW/L Scratch Pad (RSVD):** Keep RW/L for future Flash Component Specific capabilities. This register is locked by the Vendor Component Lock (VCL) bit.
4	0b RW/L	**Write Enable on Write Status (WEWS):** '0' : No Write Enable command is required to write to the Write Status register '1' : Write Enable command is required to write to the Write Status register Must be set to 1'b1 for Intel's Blanshard Flash Component and for Atmel
3	0b RW/L	**Lower Write Status Required (LWSR):** '0' : No requirement to to write to the Write Status Register prior to a write '1' : A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address.
2	0b RW/L	**Lower Write Granularity (LWG):** '0' : 1 Byte '1' : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses below the Flash Partition Address.
1:0	00b RW/L	**Lower Block/Sector Erase Size (LBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte This register is locked by the Vendor Component Lock (VCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers. This field is used for cycles targeting addresses below the Flash Partition Address.

21.4.42 UVSCC (Upper_Vendor_Specific_Component_Capabilities_bios)—Offset C8h

Upper vendor specific component capabilities

Access Method

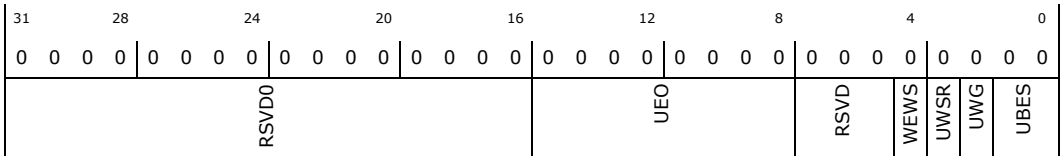
Type: Memory Mapped I/O Register (Size: 32 bits)

Upper_Vendor_Specific_Component_Capabilities_bios: [SPI_BASE_ADDRESS] + C8h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RW/L	**Upper Erase Opcode (UEO):** This register is programed with the Flash erase instruction opcode required by this vendors Flash component. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address.
7:5	0h RW/L	**Reserved RW/L Scratch Pad (RSVD):** Keep RW/L for future Flash Component Specific capabilities. This register is locked by the Vendor Component Lock (VCL) bit.
4	0b RW/L	**Write Enable on Write Status (WEWS):** '0' : No Write Enable command is required to write to the Write Status register '1' : Write Enable command is required to write to the Write Status register Must be set to 1'b1 for Intel's Blanshard Flash Component and for Atmel
3	0b RW/L	**Upper Write Status Required (UWSR):** '0': No requirement to to write to the Write Status Register prior to a write '1': A write is required to the Write Status Register prior to write and erase to remove any protection. This is required for SST components. This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address.
2	0b RW/L	**Upper Write Granularity (UWG):** '0' : 1 Byte '1' : 64 Byte This register is locked by the Vendor Component Lock (VCL) bit. This field is used for cycles targeting addresses above the Flash Partition Address.
1:0	00b RW/L	**Upper Block/Sector Erase Size (UBES):** This field identifies the erasable sector size for all Flash components. Valid Bit Settings: '00' : 256 Byte '01' : 4K Byte '10' : 8K Byte '11' : 64K Byte Note: If supporting more than one Flash component, all flash components must have identical Block/ Sector erase sizes. This register is locked by the Vendor Component Lock (VCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GBE program registers. This field is used for cycles targeting addresses above the Flash Partition Address.

21.4.43 FPB (Flash_Partition_Boundary_bios)—Offset D0h

Flash partition boundary

Access Method

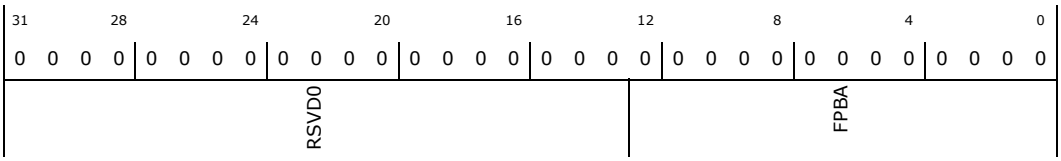
Type: Memory Mapped I/O Register (Size: 32 bits)

Flash_Partition_Boundary_bios: [SPI_BASE_ADDRESS] + D0h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:13	0b RO	**RSVD0:** Reserved
12:0	0000h RO/U	**Flash Partition Boundary Address (FPBA):** This register reflects the value of the Flash Descriptor Component FPBA field

21.4.44 SCS (SMI_Control_Status_Register_bios)—Offset F8h

SMI Control and Status

Access Method

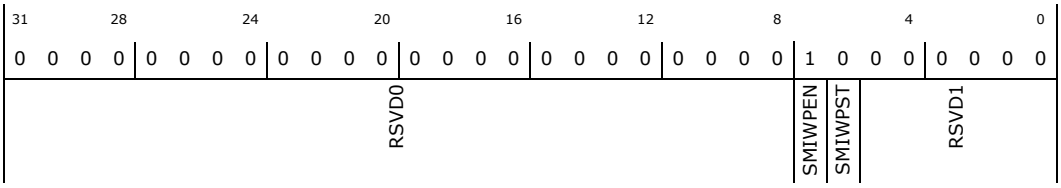
Type: Memory Mapped I/O Register (Size: 32 bits)

SMI_Control_Status_Register_bios: [SPI_BASE_ADDRESS] + F8h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000080h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	1b RW	**SMI WPD Enable (SMIWPEN):** When this bit is set to a 1'b1, it enables the SPI controller to generate SMI upon not SMM code is trying to set WPD from a 1'b0 to a 1'b1 while LE is set.

Bit Range	Default & Access	Description
6	0b RW/1C	**SMI WPD Status (SMIWPST):** Set when SMI is generated upon trying to set WPD from a 1'b0 to a 1'b1 by not SMM code (while LE and SMIWPEN are set). Write a 1'b1 to this bit should clear it and clear the SMI (send DEASSERT_SMI)
5:0	0b RO	**RSVD1:** Reserved

21.4.45 BCR (BIOS_Control_Register_bios)—Offset FCh

BIOS control register. This register formerly was in the 0:31:0 config space

Access Method

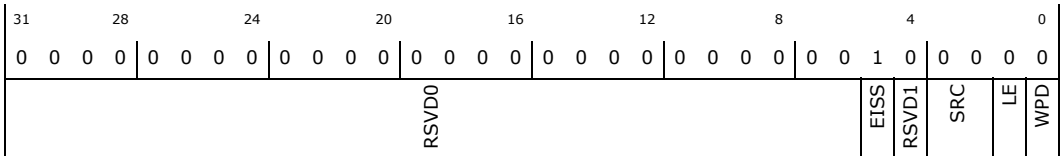
Type: Memory Mapped I/O Register (Size: 32 bits)

BIOS_Control_Register_bios: [SPI_BASE_ADDRESS] + FCh

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000020h



Bit Range	Default & Access	Description
31:6	0b RO	**RSVD0:** Reserved
5	1b RW/L	**Enable InSMM_STS (EISS):** When this bit is set, the BIOS region is writable only to SMM code. Today BIOS Flash is writable if WPD is a '1'. If this bit [lb]5[rb] is set, then WPD must be a 1'b1 and iosfep_xxx_hprot[lb]1[rb] signal be 1'b1 also. If this bit [lb]5[rb] is clear, then BIOS is writable based only on WPD = 1'b1 and the iosfep_xxx_hprot[lb]1[rb] signal is a don't care.
4	0b RO	**RSVD1:** Reserved
3:2	00b RW	**SPI Read Configuration (SRC):** This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3 - Prefetch Enable, Bit 2 - Cache Disable. Settings are summarized below: '00' : No prefetching, but caching enabled. Direct Memory reads load the read buffer cache with 'valid' data, allowing repeated reads to the same range to complete quickly. '01' : No prefetching and no caching. One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache. '10' : Prefetching and Caching enabled. This mode is used for long sequences of short reads to consecutive addresses (i.e. shadowing) '11' : Illegal. Caching must be enabled when Prefetching is enabled. This eliminates the need for a complex prefetch-flushing mechanism. Note that if BIOS direct read caching is disabled while data has already been cached internally, subsequent BIOS direct reads will continue to return data from the cache until the cache is invalidated.
1	0b RW/L	**Lock Enable (LE):** When set, WPD bit could be set from a 1'b0 to a 1'b1 only by SMM code. When cleared, setting the WP bit is allowed in all modes and SMI is not generated. Once set, this bit can only be cleared by a PLTRST#. When this bit is set, EISS - bit [lb]5[rb] of this register is locked down.

Bit Range	Default & Access	Description
0	0b RW	**Write Protect Disable (WPD):** When set, access to the BIOS space is enabled for both read and write cycles. When cleared, only read cycles are permitted to the flash. When LE bit is set this bit could be written from a 1'b0 to a 1'b1 only by SMM code. When not SMM code tries to writes this bit from a 1'b0 to a 1'b1, bit remain in its 1'b0 value. An Async-SMI is generated (Send ASSERT_SMI) if SMIWPEN is set. This ensures that only SMM code can update BIOS.

21.4.46 TCGC (Trunk_Clock_Gating_Control_bios)—Offset 100h

Trunk_Clock_Gating_Control

Access Method

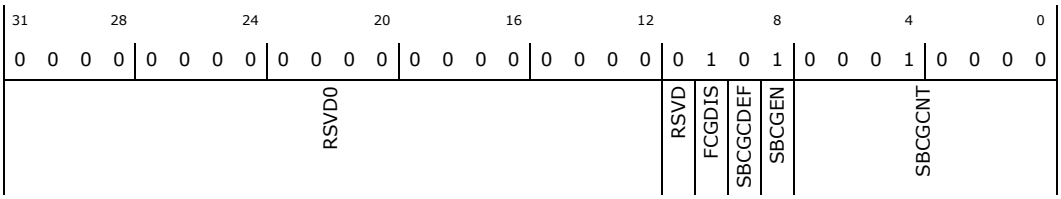
Type: Memory Mapped I/O Register (Size: 32 bits)

Trunk_Clock_Gating_Control_bios: [SPI_BASE_ADDRESS] + 100h

SPI_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 54h

Default: 00000510h



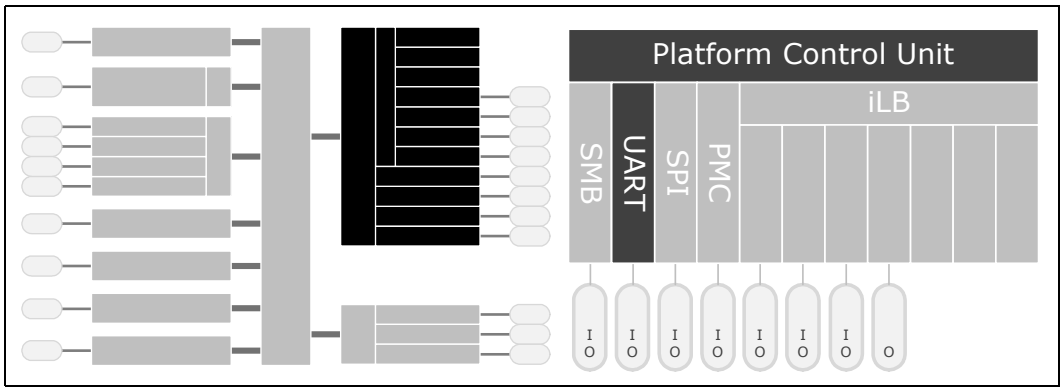
Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RO	**Reserved (RSVD):** Reserved.
10	1b RW	**FCGDIS:** Functional clock gating disable, chicken bit for the func_clk_gating FSM
9	0b RW	**SBCGCDEF:** SideBanb Control Gating Clock Defeature .Clock gate defeature bit which allows the ISM to transition to idle, but prevents the final clock masking from occurring. The value of this bit goes to the 'cgctrl_clkgatedef' port of the SideBand EndPoint
8	1b RW	**SBCGEN:** SideBanb Control Gating Clock Enable. Clock gate enable which prevents ISM from leaving ACTIVE. Also prevents the clocks from being gated. The value of this bit goes to the 'cgctrl_clkgaten' port of the SideBand EndPoint
7:0	10h RW	**SBCGCNT:** SideBanb Control Gating Clock Counter. Idle count limit for ISM which is used to determine the block is idle.Recommended value 8'd16 . The value of those bits goes to the 'cgctrl_idlecnt' ports of the SideBand EndPoint

§ §

22 PCU – Universal Asynchronous Receiver/Transmitter (UART)

This section describes the Universal Asynchronous Receiver/Transmitter (UART) serial port integrated into the PCU. The UART may be controlled through programmed IO.

Note: Only a minimal ball-count, comprising receive & transmit signals, UART port is implemented. Further, a maximum baud rate of only 115,200 bps is supported. For this reason, it is recommended that the UART port be used for debug purposes only.



22.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 161. UART Signals

Signal Name	Direction/ Type	Description
PCU_UART_RXD	I TBD	**COM1 Receive:** Serial data input from device pin to the receive port. *This signal is multiplexed and may be used by other functions.*
PCU_UART_TXD	O TBD	**COM1 Transmit:** Serial data output from transmit port to the device pin. *This signal is multiplexed and may be used by other functions.*

22.2 Features

The serial port consists of a UART which supports a subset of the functions of the 16550 industry standard.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the processor. The processor may read the complete status of the UART at any time during the functional operation. Available status information includes the type and condition of the transfer operations being performed by the UART and any error conditions.

The serial port may operate in either FIFO or non-FIFO mode. In FIFO mode, a 16-byte transmit FIFO holds data from the processor to be transmitted on the serial link and a 16-byte Receive FIFO buffers data from the serial link until read by the processor.

The UART includes a programmable baud rate generator which is capable of generating a baud rate of between 50 bps and 115,200 bps from a fixed baud clock input of 1.8432 MHz. The baud rate is calculated as follows:

Baud Rate Calculation:

$$\text{BaudRate} = \frac{1.8432 \times 10^6}{16 \times \text{Divisor}}$$

The divisor is defined by the Divisor Latch LSB and Divisor Latch MSB registers. Some common values are shown in Table 162.

Table 162. Baud Rate Examples

Desired Baud Rate	Divisor	Divisor Latch LSB Register	Divisor Latch MSB Register
115,200	1	1h	0h
57,600	2	2h	0h
38,400	3	3h	0h
19,200	6	6h	0h
9,600	12	Ch	0h
4,800	24	18h	0h
2,400	48	30h	0h
1,200	96	60h	0h
300	384	80h	1h
50	2,304	0h	9h

The UART has interrupt support and those interrupts may be programmed to the user's requirements, minimizing the computing required to handle the communications link. Each UART may operate in a polled or an interrupt driven environment as configured by software.

22.2.1 FIFO Operation

22.2.1.1 FIFO Interrupt Mode Operation

Receiver Interrupt

When the Receive FIFO and receiver interrupts are enabled (FIFO Control Register, bit 0 = 1b and Interrupt Enable Register (IIR), bit 0 = 1b), receiver interrupts occur as follows:

- The receive data available interrupt is invoked when the FIFO has reached its programmed trigger level. The interrupt is cleared when the FIFO drops below the programmed trigger level.
- The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, the bits are cleared when the FIFO drops below the trigger level.
- The receiver line status interrupt (IIR = C6h), as before, has the highest priority. The receiver data available interrupt (IIR = C4h) is lower. The line status interrupt occurs only when the character at the top of the FIFO has errors.
- The COM1_LSR.DR bit is set to 1b as soon as a character is transferred from the shift register to the Receive FIFO. This bit is reset to 0b when the FIFO is empty.

Character Time Out Interrupt

When the receiver FIFO and receiver time out interrupt are enabled, a character time out interrupt occurs when all of the following conditions exist:

- At least one character is in the FIFO.
- The last received character was longer than four continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
- The most recent processor read of the FIFO was longer than four continuous character times ago.
- The receiver FIFO trigger level is greater than one.

The maximum time between a received character and a timeout interrupt is 160 ms at 300 baud with a 12-bit receive character (that is, 1 start, 8 data, 1 parity, and 2 stop bits).

When a time out interrupt occurs, it is cleared and the timer is reset when the processor reads one character from the receiver FIFO. If a time out interrupt has not occurred, the time out timer is reset after a new character is received or after the processor reads the receiver FIFO.

Transmit Interrupt

When the transmitter FIFO and transmitter interrupt are enabled (FIFO Control Register, bit 0 = 1b and Interrupt Enable Register, bit 0 = 1b), transmit interrupts occur as follows:

The Transmit Data Request interrupt occurs when the transmit FIFO is half empty or more than half empty. The interrupt is cleared as soon as the Transmit Holding Register is written (1 to 16 characters may be written to the transmit FIFO while servicing the interrupt) or the Interrupt Identification Register is read.

22.2.1.2 FIFO Polled Mode Operation

With the FIFOs enabled (FIFO Control register, bit 0 = 1b), setting Interrupt Enable register (IER), bits 3:0 = 000b puts the serial port in the FIFO polled mode of operation. Since the receiver and the transmitter are controlled separately, either one or both may be in the polled mode of operation. In this mode, software checks receiver and transmitter status through the Line Status Register (LSR). As stated in the register description:

- LSR[0] is set as long as there is one byte in the receiver FIFO.
- LSR[1] through LSR[4] specify which error(s) has occurred for the character at the top of the FIFO. Character error status is handled the same way as interrupt mode. The Interrupt Identification Register is not affected since IER[2] = 0b.
- LSR[5] indicates when the transmitter FIFO needs data.
- LSR[6] indicates that both the transmitter FIFO and shift register are empty.
- LSR[7] indicates whether there are any errors in the receiver FIFO.

22.3 Use

22.3.1 Base I/O Address

22.3.1.1 COM1

The base I/O address for the COM1 UART is fixed to 3F8h.

22.3.2 Legacy Interrupt

22.3.2.1 COM1

The legacy interrupt assigned to the COM1 UART is fixed to IRQ3.

22.4 UART Enable/Disable

The COM1 UART may be enabled or disabled using the UART_CONT.COM1EN register bit. By default, the UART is disabled.

Note: It is recommended that the UART be disabled during normal platform operation. An enabled UART can interfere with platform power management.

22.5 Register Map

TBD

22.6 IO Mapped Registers

There are 12 registers associated with the UART. These registers share eight address locations in the IO address space. Table 163 shows the registers and their addresses as offsets of a base address. Note that the state of the COM1_LCR.DLAB register bit, which is the most significant bit (MSB) of the Serial Line Control register, affects the selection of certain of the UART registers. The COM1_LCR.DLAB register bit must be set high by the system software to access the Baud Rate Generator Divisor Latches.

Table 163. Register Access List

Register Address (Offset to Base IO Address)	COM1_LCR.DLAB Value	Register Access Type	Register Accessed
0h	0b	RO	Receiver Buffer[1]
0h	0b	WO	Transmitter Holding[1]
0h	1b	RW	Divisor Latch LSB (Lowest Significant Bit)[1]
1h	0b	RW	Interrupt Enable[2]
1h	1b	RW	Divisor Latch MSB (Most Significant Bit)[2]
2h	xb	RO	Interrupt Identification[3]
2h	xb	WO	FIFO Control[3]
3h	xb	RW	Line Control
4h	xb	RW	Modem Control[4]
5h	xb	RO	Line Status
6h	xb	RO	Modem Status[4]
7h	xb	RW	Scratchpad

Notes:
1. These registers are consolidated in the Receiver Buffer / Transmitter Holding Register (COM1_RX_TX_BUFFER)
2. These registers are consolidated in the Interrupt Enable Register (COM1_IER)
3. These registers are consolidated in the Interrupt Identification / FIFO Control Register (COM1_IIR)
4. These registers are implemented but unused since the UART signals related to modem interaction are not implemented.

PCU - Universal Asynchronous Receiver/Transmitter (UART)

22.7 PCU iLB UART IO Registers

Table 164. Summary of PCU iLB UART I/O Registers

Offset	Size	Register ID—Description	Default Value
3F8h	1	"Receiver Buffer / Transmitter Holding Register (COM1_Rx_Tx_Buffer)—Offset 3F8h" on page 1101	00h
3F9h	1	"Interrupt Enable Register (COM1_IER)—Offset 3F9h" on page 1102	00h
3FAh	1	"Interrupt Identification / FIFO Control Register (COM1_IIR)—Offset 3FAh" on page 1103	01h
3FBh	1	"Line Control Register (COM1_LCR)—Offset 3FBh" on page 1104	00h
3FCh	1	"Modem Control Register (COM1_MCR)—Offset 3FCh" on page 1105	00h
3FDh	1	"Line Status Register (COM1_LSR)—Offset 3FDh" on page 1106	60h
3FEh	1	"Modem Status Register (COM1_MSR)—Offset 3FEh" on page 1108	00h
3FFh	1	"Scratchpad Register (COM1_SCR)—Offset 3FFh" on page 1109	00h

22.7.1 Receiver Buffer / Transmitter Holding Register (COM1_Rx_Tx_Buffer)—Offset 3F8h

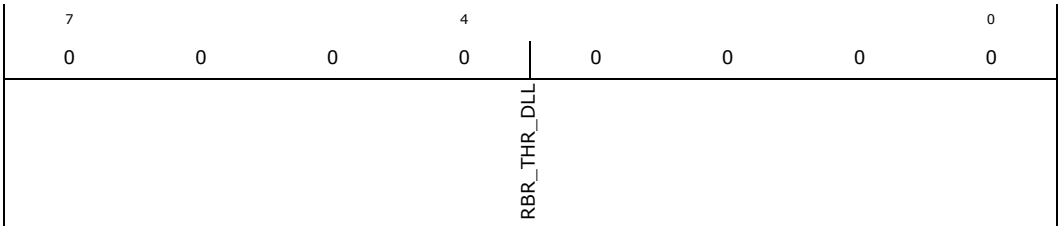
This register is a combination of three registers: the receiver buffer register (RBR) that is a read-only register when DLAB=0, the transmitter holding register (THR) that is a write-only register when DLAB=0 and the divisor latch LSB (DLL) register when DLAB=1.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_Rx_Tx_Buffer: 3F8h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Receiver buffer / transmitter holding (RBR_THR_DLL): When reading from this register and DLAB=1'b0**, it contains the byte received if no FIFO is used, or the oldest unread byte with FIFO's. If FIFO buffering is used, each new read action of the register will return the next byte, until no more bytes are present. Bit 0 in the LSR line status register can be used to check if all received bytes have been read. This bit wil change to zero if no more bytes are present. **When writing to this register and DLAB=1'b0**, it is used to buffer outgoing characters. If no FIFO buffering is used, only one character can be stored. Otherwise the amount of characters depends on the type of UART. Bit 5 in the LSR, line status register can be used to check if new information must be written to this register. The value 1'b1 indicates that the register is empty. If FIFO buffering is used, more than one character can be written to the transmitter holding register when the bit signals an empty state. There is no indication of the amount of bytes currently present in the transmitter FIFO. This register is not used to transfer the data directly. The byte is first transferred to a shift register where the information is broken in single bits which are sent one by one. **If DLAB=1'b1**, this register is used as DLL (Divisor Latch LSB). For generating its timing information, each UART uses an oscillator generating a frequency of about 1.8432 MHz. This frequency is divided by 16 to generate the time base for communucation. Because of this division, the maximum allowed communication speed is 115200 bps. Modern UARTS like the 16550 are capable of handling higher input frequencies up to 24 MHz which makes it possible to communicate with a maximum speed of 1.5 Mbps. On PC's higher frequencies than the 1.8432 MHz are rarely seen because this would be software incompatible with the original XT configuration. This 115200 bps communication speed is not suitable for all applications. To change the communication speed, the frequency can be further decreased by dividing it by a programmable value. For very slow communications, this value can go beyond 255. Therefore, the divisor is stored in two seperate bytes, the divisor latch registers DLL and DLM which contain the least, and most significant byte. For error free communication, it is necessary that both the transmitting and receiving UART use the same time base. Default values have been defined which are commonly used. The table shows the most common values with the appropriate settings of the divisor latch bytes. Note that these values only hold for a PC compatible system where a clock frequency of 1.8432 MHz is used. Speed(bps) Divisor DLL DLM 50 2,304 0x00 0x09 300 384 0x80 0x01 1,200 96 0x60 0x00 2,400 48 0x30 0x00 4,800 24 0x18 0x00 9,600 12 0x0C 0x00 19,200 6 0x06 0x00 38,400 3 0x03 0x00 57,600 2 0x02 0x00 115,200 1 0x01 0x00

22.7.2 Interrupt Enable Register (COM1_IER)—Offset 3F9h

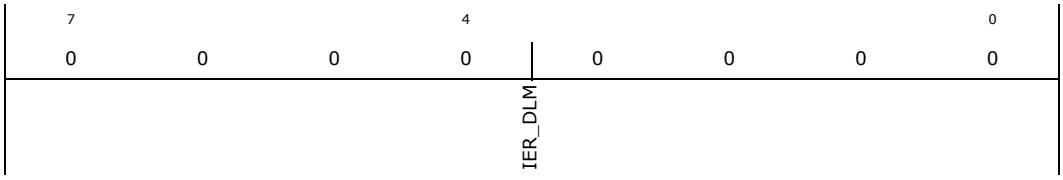
This register is a combination of two registers: the interrupt enable register (IER) when DLAB=0 and the divisor latch MSB (DLM) register when DLAB=1.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_IER: 3F9h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Interrupt Enable (IER_DLM): If DLAB=1'b0**, This field is used as interrupt enable register. The smartest way to perform serial communications on a PC is using interrupt driven routines. In that configuration, it is not necessary to poll the registers of the UART periodically for state changes. The UART will signal each change by generating a processor interrupt. A software routine must be present to handle the interrupt and to check what state change was responsible for it. Interrupts are not generated, unless the UART is told to do so. This is done by setting bits in the IER, interrupt enable register. A bit value 1 indicates, that an interrupt may take place. Bit Description 0 ERBFI - Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1 ETBEI - Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 2 ELSI - Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 3 EDSSI - Enable Modem Status Interrupt. This is used to enable/ disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 4 Reserved and read as zero 5 Reserved and read as zero 6 Reserved and read as zero 7 PTIME - Programmable THRE Interrupt Mode Enable that can be written to only when THRE_MODE_USER == Enabled, always readable. This is used to enable/disable the generation of THRE Interrupt. **If DLAB=1'b1**, this register is used as DLM (Divisor Latch MSB). See DLL field description in the Rx_Tx_Buffer register.

22.7.3 Interrupt Identification / FIFO Control Register (COM1_IIR)—Offset 3FAh

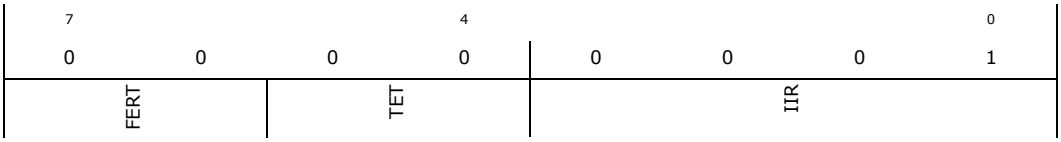
This register is a combination of two registers: the interrupt identification register (IIR) that is a read-only register and the FIFO control register (FCR) that is a write-only register. If FIFOs are not implemented, the FIFO control register does not exist and writing to this register address has no effect.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_IIR: 3FAh

Default: 01h



Bit Range	Default & Access	Description
7:6	00b RO	**FIFOs Enabled / RCVR Trigger (FERT): Read** from this field is used to indicate whether the FIFOs are enabled or disabled. '00' - disabled '11' - enabled **Write** to this field is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. The following trigger levels are supported: '00' - 1 character in the FIFO '01' - FIFO 1/4 full '10' - FIFO 1/2 full '11' - FIFO 2 less than full
5:4	00b RO	**TX Empty Trigger (TET): Read** from this field is reserved and should return zero **Write** to this field is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported: '00' - FIFO empty '01' - 2 characters in the FIFO '10' - FIFO 1/4 full '11' - FIFO 1/2 full

Bit Range	Default & Access	Description
3:0	0001b RO	**Interrupt ID (IIR): Read** from this field indicates the highest priority pending interrupt which can be one of the following types: '0000' - modem status '0001' - no interrupt pending '0010' - THR empty '0100' - received data available '0110' - receiver line status '0111' - busy detect '1100' - character timeout **Write** to this field is split to four bits: Bit Description 3 DMA Mode, determines the DMA signalling mode used: '0'- mode 0, '1' - mode 1 2 XMIT FIFO Reset, resets the control portion of the transmit FIFO and treats the FIFO as empty. 1 RCVR FIFO Reset, resets the control portion of the receive FIFO and treats the FIFO as empty. 0 FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.

22.7.4 Line Control Register (COM1_LCR)—Offset 3FBh

The LCR, line control register is used at initialisation to set the communication parameters. Parity and number of data bits can be changed for example. The register also controls the accessibility of the DLL and DLM registers. These registers are mapped to the same I/O port as the RBR, THR and IER registers. Because they are only accessed at initialisation when no communication occurs this register swapping has no influence on performance.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_LCR: 3FBh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
DLAB	BC	SP	EPS	PEN	STOP	DLS	

Bit Range	Default & Access	Description
7	0b RW	**Divisor Latch Access Bit (DLAB):** This field is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers. '0' - RBR, THR and IER accessible '1' - DLL and DLM accessible See Rx_Tx_Buffer and IER registers description for more details.
6	0b RW	**Break Control (BC):** This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE == Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	0b RO	**Stick Parity (SP):** Reserved and read as zero
4	0b RW	**Even Parity Select (EPS):** This is used to select between even and odd parity, when parity is enabled (PEN set to one). If set to one, an even number of logic 1s is transmitted or checked. If set to zero, an odd number of logic 1s is transmitted or checked.
3	0b RW	**Parity Enable (PEN):** This is used to enable and disable parity generation and detection in transmitted and received serial character respectively. '0' - parity disabled '1' - parity enabled

Bit Range	Default & Access	Description
2	0b RW	**Number ofStop bits (STOP):** This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. '0' - 1 stop bit '1' - 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	00b RW	**Data Length Select (DLS):** This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: '00' - 5 bits '01' - 6 bits '10' - 7 bits '11' - 8 bits

22.7.5 Modem Control Register (COM1_MCR)—Offset 3FCh

The MCR, modem control register is used to perform handshaking actions with the attached device. In the original UART series including the 16550, setting and resetting of the control signals must be done by software. The new 16750 is capable of handling flow control automatically, thereby reducing the load on the processor.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_MCR: 3FCh

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
RSVD0	SIRE	AFCE	LB	OUT2	OUT1	RTS	DTR

Bit Range	Default & Access	Description
7	0b RO	**RSVD0:** Reserved
6	0b RW	**SIR Mode Enable (SIRE):** Writeable only when SIR_MODE == Enabled, always readable. This is used to enable/disable the IrDA SIR Mode features as described in 'IrDA 1.0 SIR Protocol' on Synopsys UART specification. '0' - IrDA SIR Mode disabled '1' - IrDA SIR Mode enabled
5	0b RW	**Auto Flow Control Enable (AFCE):** Writeable only when AFCE_MODE == Enabled, always readable. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled as described in 'Auto Flow Control' on Synopsys UART specification. '0' - Auto Flow Control Mode disabled '1' - Auto Flow Control Mode enabled
4	0b RW	**LoopBack (LB):** This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	0b RW	**Auxiliary output 2 (OUT2):** This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: '0' - out2_n de-asserted (logic 1) '1' - out2_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.

Bit Range	Default & Access	Description
2	0b RW	**Auxiliary output 1 (OUT1):** This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: '0' - out1_n de-asserted (logic 1) '1' - out1_n asserted (logic 0) Note that in Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	0b RW	**Request to Send (RTS):** This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high.In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input. Note that PCU-UART does not implement the Request to Send (rts_n) output.
0	0b RW	**Data Terminal Ready (DTR):** This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: '0' - dtr_n de-asserted (logic 1) '1' - dtr_n asserted (logic 0) The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input. Note that PCU-UART does not implement the Data Terminal Ready (dtr_n) output.

22.7.6 Line Status Register (COM1_LSR)—Offset 3FDh

The LSR, line status register shows the current state of communication. Errors are reflected in this register. The state of the receive and transmit buffers is also available.

Access Method

Type: I/O Register (Size: 8 bits)

COM1_LSR: 3FDh

Default: 60h

7			4				0
0	1	1	0	0	0	0	0
RFE	TEMT	THRE	BI	FE	PE	OE	DR

Bit Range	Default & Access	Description
7	0b RO	**Receiver FIFO Error (RFE):** This bit is only relevant when FIFO_MODE != NONE AND FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. '0' - no error in RX FIFO '1' - error in RX FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.
6	1b RO	**Transmitter Empty (TEMT):** If in FIFO mode (FIFO_MODE != NONE) and FIFOs enabled (FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If in non-FIFO mode or FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.

Bit Range	Default & Access	Description
5	1b RO	**Transmit Holding Register Empty (THRE):** If THRE_MODE_USER == Disabled or THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/ enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If THRE_MODE_USER == Enabled AND FIFO_MODE != NONE and both modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting.
4	0b RO	**Break Interrupt (BI):** This is used to indicate the detection of a break sequence on the serial input data. If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.
3	0b RO	**Framing Error (FE):** This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit; that is, data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). '0' - no framing error '1' - framing error Reading the LSR clears the FE bit.
2	0b RO	**Parity Error (PE):** This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). '0' - no parity error '1' - parity error Reading the LSR clears the PE bit.
1	0b RO	**Overrun Error (OE):** This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. '0' - no overrun error '1' - overrun error Reading the LSR clears the OE bit.
0	0b RO	**Data Ready (DR):** This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO. '0' - no data ready '1' - data ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.

22.7.7 Modem Status Register (COM1_MSR)—Offset 3FEh

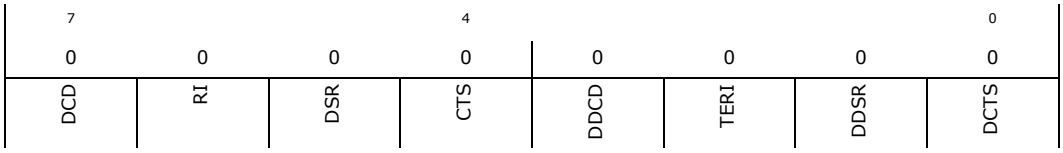
The MSR, modem status register contains information about the four incomming modem control lines on the device. The information is split in two nibbles. The four most siginificant bits contain information about the current state of the inputs where the least significant bits are used to indicate state changes. The four LSB's are reset, each time the register is read. Whenever bits 0, 1, 2 or 3 are set to logic one, to indicate a change on the modem control inputs, a modem status interrupt is generated if enabled through the IER, regardless of when the change occurred. Since the delta bits (bits 0, 1, 3) can get set after a reset if their respective modem signals are active (see individual bits for details), a read of the MSR after reset can be performed to prevent unwanted interrupts.

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_MSR: 3FEh

Default: 00h



Bit Range	Default & Access	Description
7	0b RO	**Data Carrier Detect (DCD):** This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. '0' - dcd_n input is de-asserted (logic 1) '1' - dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2). Note that PCU-UART does not implement the Data Carrier Detect (dcd_n) input.
6	0b RO	**Ring Indicator (RI):** This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. '0' - ri_n input is de-asserted (logic 1) '1' - ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1). Note that PCU-UART does not implement the Ring Indicator (ri_n) input.
5	0b RO	**Data Set Ready (DSR):** This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the DW_apb_uart. '0' - dsr_n input is de-asserted (logic 1) '1' - dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR). Note that PCU-UART does not implement the Data Set Ready (dsr_n) input.
4	0b RO	**Clear to Send (CTS):** This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the DW_apb_uart. '0' - cts_n input is de-asserted (logic 1) '1' - cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS). Note that PCU-UART does not implement the Clear to Send (cts_n) input.
3	0b RO	**Delta Data Carrier Detect (DDCD):** This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. '0' - no change on dcd_n since last read of MSR '1' - change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). Note, if the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted. Note that PCU-UART does not implement the Data Carrier Detect (dcd_n) input.

Bit Range	Default & Access	Description
2	0b RO	**Trailing Edge of Ring Indicator (TERI):** This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. '0' - no change on ri_n since last read of MSR '1' - change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low. Note that PCU-UART does not implement the Ring Indicator (ri_n) input.
1	0b RO	**Delta Data Set Ready (DDSR):** This is used to indicate that the modem control line dsr_n has changed since the last time the MSR was read. '0' - no change on dsr_n since last read of MSR '1' - change on dsr_n since last read of MSR Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR). Note, if the DDSR bit is not set and the dsr_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the dsr_n signal remains asserted. Note that PCU-UART does not implement the Data Set Ready (dsr_n) input.
0	0b RO	**Delta Clear to Send (DCTS):** This is used to indicate that the modem control line cts_n has changed since the last time the MSR was read. '0' - no change on cts_n since last read of MSR '1' - change on cts_n since last read of MSR Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS). Note, if the DCTS bit is not set and the cts_n signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the cts_n signal remains asserted. Note that PCU-UART does not implement the Clear to Send (cts_n) input.

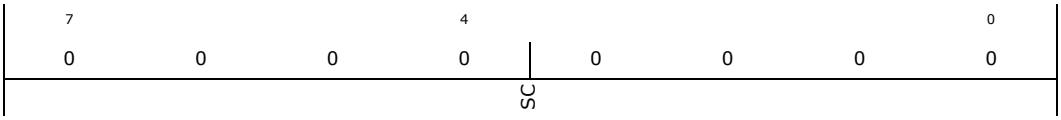
22.7.8 Scratchpad Register (COM1_SCR)—Offset 3FFh

Access Method

Type: I/O Register
(Size: 8 bits)

COM1_SCR: 3FFh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**Scratchpad (SC):** This register is for programmers to use as a temporary storage space.

§ §

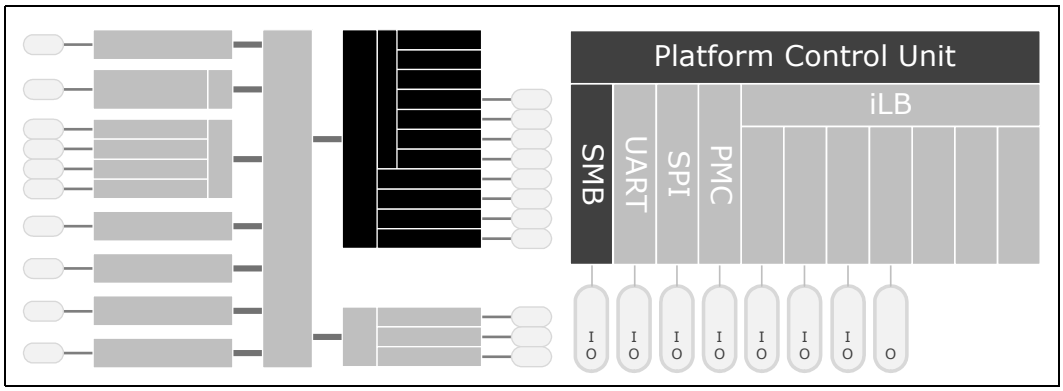
23 PCU – System Management Bus (SMBus)

The processor provides a System Management Bus (SMBus) 2.0 host controller. The host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves).

The processor can perform SMBus messages with packet error checking (PEC) enabled or disabled. The actual PEC calculation and checking can be performed in either hardware or software.

The SMBus Address Resolution Protocol (ARP) is supported by using the existing host controller commands through software, except for the Host Notify command (which is actually a received message).

The programming model of the host controller is combined into two portions: a PCI configuration portion, and a system I/O mapped portion. All static configuration, such as the I/O base address, is done using the PCI configuration space. Real-time programming of the Host interface is done in system I/O space.



23.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

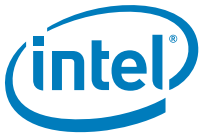


Table 165. SMBus Signal Names

Signal Name	Direction Type	Description
PCU_SMB_ALERT#	I/OD CMOS1.8	**SMBus Alert:** This signal is used to generate internal SMI#. *This signal is multiplexed and may be used by other functions.*
PCU_SMB_CLK	I/OD CMOS1.8	**SMBus Clock:** External pull-up resistor is required. *This signal is multiplexed and may be used by other functions.*
PCU_SMB_DATA	I/OD CMOS1.8	**SMBus Data:** External pull-up resistor is required. *This signal is multiplexed and may be used by other functions.*

23.2 Features

23.2.1 Host Controller

The SMBus host controller is used to send commands to other SMBus slave devices. Software sets up the host controller with an address, command, and, for writes, data and optional PEC; and then tells the controller to start. When the controller has finished transmitting data on writes, or receiving data on reads, it generates an SMI# or interrupt, if enabled.

The host controller supports 8 command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification, Version 2.0*): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write and Block Write–Block Read Process Call.

The SMBus host controller requires that the various data and command fields be setup for the type of command to be sent. When software sets the START bit, the SMBus Host controller performs the requested transaction, and interrupts the processor (or generates an SMI#) when the transaction is completed. Once a START command has been issued, the values of the "active registers" (Host Control (SMB_Mem_HCTL), Host Command (SMB_Mem_HCMD), Transmit Slave Address (SMB_Mem_TSA), Data 0 (SMB_Mem_HD0), Data 1 (SMB_Mem_HD1)) should not be changed or read until the interrupt status message (SMB_Mem_HSTS.INTR) has been set (indicating the completion of the command). Any register values needed for computation purposes should be saved prior to issuing of a new command, as the SMBus host controller updates all registers while completing the new command.

23.2.1.1 Command Protocols

In all of the following commands, the Host Status (SMB_Mem_HSTS) register is used to determine the progress of the command. While the command is in operation, the SMB_Mem_HSTS.HBSY bit is set. If the command completes successfully, the SMB_Mem_HSTS.INTR bit will be set. If the device does not respond with an acknowledge, and the transaction times out, the SMB_Mem_HSTS.DEVERR bit is set. If software sets the SMB_Mem_HCTL.KILL bit while the command is running, the transaction will stop and the SMB_Mem_HSTS.FAILED bit will be set.

Quick Command

When programmed for a Quick Command, the Transmit Slave Address (SMB_Mem_TSA) register is sent. The PEC byte is never appended to the Quick Protocol. Software should force the SMB_Config_HCTL.PECEN bit to 0b when performing the Quick Command. See section 5.5.1 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Send Byte / Receive Byte

For the Send Byte command, the Transmit Slave Address (SMB_Mem_TSA) and Host Command (SMB_Mem_HCMD) registers are sent. For the Receive Byte command, the Transmit Slave Address (SMB_Mem_TSA) register is sent. The data received is stored in the Data 0 (SMB_Mem_HD0) register.

The Receive Byte is similar to a Send Byte, the only difference is the direction of data transfer. See sections 5.5.2 and 5.5.3 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

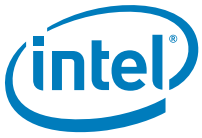
Write Byte/Word

The first byte of a Write Byte/Word access is the command code. The next 1 or 2 bytes are the data to be written. When programmed for a Write Byte/Word command, the Transmit Slave Address (SMB_Mem_TSA), Host Command (SMB_Mem_HCMD), and Data 0 (SMB_Mem_HD0) registers are sent. In addition, the Data 1 (SMB_Mem_HD1) register is sent on a Write Word command. See section 5.5.4 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Read Byte/Word

Reading data is slightly more complicated than writing data. First the processor must write a command to the slave device. Then it must follow that command with a repeated start condition to denote a read from that device's address. The slave then returns 1 or 2 bytes of data.

When programmed for the read byte/word command, the Transmit Slave Address (SMB_Mem_TSA) and Host Command (SMB_Mem_HCMD) registers are sent. Data is received into the Data 0 (SMB_Mem_HD0) on the read byte, and the Data 0 (SMB_Mem_HD0) and Data 1 (SMB_Mem_HD1) registers on the read word. See section 5.5.5 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.



Process Call

The process call is so named because a command sends data and waits for the slave to return a value dependent on that data. The protocol is simply a Write Word followed by a Read Word, but without a second command or stop condition.

When programmed for the Process Call command, the processor transmits the Transmit Slave Address (SMB_Mem_TSA), Host Command (SMB_Mem_HCMD), Data 0 (SMB_Mem_HD0) and Data 1 (SMB_Mem_HD1) registers. Data received from the device is stored in the Data 0 (SMB_Mem_HD0) and Data 1 (SMB_Mem_HD1) registers. The Process Call command with SMB_Config_HCFG.I2C_EN set and the SMB_Config_HCTL.PECEN bit set produces undefined results. Software must force SMB_Config_HCTL.PECEN & SMB_Mem_AUXC.AAC to 0b when running this command. See section 5.5.6 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Note: For process call command, the value written into SMB_Mem_TSA.RW needs to be 0b.

Block Read/Write

The processor contains a 32-byte buffer for read and write data which can be enabled by setting SMB_Mem_AUXC.E32B, as opposed to a single byte of buffering. This 32-byte buffer is filled with write data before transmission, and filled with read data on reception. In the processor, the interrupt is generated only after a transmission or reception of 32 bytes, or when the entire byte count has been transmitted/received.

The byte count field is transmitted but ignored by the processor as software will end the transfer after all bytes it cares about have been sent or received.

For a Block Write, software must either force both the SMB_Config_HCTL.PECEN and SMB_Mem_AUXC.AAC bits to 0b when running this command.

The block write begins with a slave address and a write condition. After the command code the processor issues a byte count describing how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by 20 bytes of data. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

When programmed for a block write command, the Transmit Slave Address (SMB_Mem_TSA), Host Command (SMB_Mem_HCMD) and Data 0 (SMB_Mem_HD0) registers are sent. Data is then sent from the Host Block Data (SMB_Mem_HBD) register; the total data sent being the value stored in the Data 0 (SMB_Mem_HD0) register. On block read commands, the first byte received is stored in the Data 0 (SMB_Mem_HD0) register, and the remaining bytes are stored in the Host Block Data (SMB_Mem_HBD) register. See section 5.5.7 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

Note: The processor will still send the number of bytes (on writes) or receive the number of bytes (on reads) indicated in the Data 0 (SMB_Mem_HD0) register. However, it will not send the contents of the Data 0 (SMB_Mem_HD0) register as part of the message.

Also, the Block Write protocol sequence changes slightly: the Byte Count (bits 27:20 in the bit sequence) are not sent - as a result, the slave will not acknowledge (bit 28 in the sequence).

Block Write–Block Read Process Call

The block write-block read process call is a two-part message. The call begins with a slave address and a write condition. After the command code the host issues a write byte count (M) that describes how many more bytes will be written in the first part of the message. If a master has 6 bytes to send, the byte count field will have the value 6 (0000 0110b), followed by the 6 bytes of data. The write byte count (M) cannot be 0.

The second part of the message is a block of read data beginning with a repeated start condition followed by the slave address and a Read bit. The next byte is the read byte count (N), which may differ from the write byte count (M). The read byte count (N) cannot be 0.

The combined data payload must not exceed 32 bytes. The byte length restrictions of this process call are summarized as follows:

- M ≥ 1 byte
- N ≥ 1 byte
- M + N ≤ 32 bytes

The read byte count does not include the PEC byte. The PEC is computed on the total message beginning with the first slave address and using the normal PEC computational rules. It is highly recommended that a PEC byte be used with the Block Write-Block Read Process Call. Software must do a read to the Host Command (SMB_Mem_HCMD) register to reset the 32 byte buffer pointer prior to reading the Host Block Data (SMB_Mem_HBD) register.

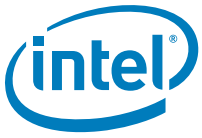
Note that there is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer.

Note: The SMB_Mem_AUXC.E32B bit in the Auxiliary Control register must be set when using this protocol.

See section 5.5.8 of the *System Management Bus (SMBus) Specification,* Version 2.0 for the format of the protocol.

23.2.2 Bus Arbitration

Several masters may attempt to get on the bus at the same time by driving the PCU_SMB_DATA line low to signal a start condition. The processor continuously monitors the PCU_SMB_DATA line. When the processor is attempting to drive the bus to a 1 by letting go of the PCU_SMB_DATA line, and it samples PCU_SMB_DATA low, then some other master is driving the bus and the processor will stop transferring data.



If the processor sees that it has lost arbitration, the condition is called a collision. The processor will set SMB_Mem_HSTS.BERR, and if enabled, generate an interrupt or SMI#. The processor is responsible for restarting the transaction.

The processor, as a SMBus master, drives the clock. When the processor is sending address or command or data bytes on writes, it drives data relative to the clock it is also driving. It will not start toggling the clock until the start or stop condition meets proper setup and hold time. The processor will also ensure minimum time between SMBus transactions as a master.

23.2.3 Bus Timing

23.2.3.1 Clock Stretching

Some devices may not be able to handle their clock toggling at the rate that the processor as an SMBus master would like. They have the capability of stretching the low time of the clock. When the processor attempts to release the clock (allowing the clock to go high), the clock will remain low for an extended period of time.

The processor monitors the SMBus clock line after it releases the bus to determine whether to enable the counter for the high time of the clock. While the bus is still low, the high time counter must not be enabled. Similarly, the low period of the clock can be stretched by an SMBus master if it is not ready to send or receive data.

23.2.3.2 Bus Time Out (Processor as SMBus Master)

If there is an error in the transaction, such that an SMBus device does not signal an acknowledge, or holds the clock lower than the allowed time-out time, the transaction will time out. The processor will discard the cycle and set the SMB_Mem_HSTS.DEVERR bit. The time-out minimum is 25 ms (800 RTC clocks). The time-out counter inside the processor will start after the last bit of data is transferred by the processor and it is waiting for a response.

The 25-ms time-out counter will not count under the following conditions:

1. The SMB_Mem_HSTS.BYTE_DONE_STS bit is set
2. The TCO_STS.SECOND_TO_STS bit is not set (this indicates that the system has not locked up).

23.2.4 Interrupts / SMI#

The processor SMBus controller uses INTB as its virtual interrupt wire. However, the system can alternatively be set up to generate SMI# instead of an interrupt, by setting the SMB_Config_HCFG.SMI_EN bit.

The following tables specify how the various enable bits in the SMBus function control the generation of the interrupt and Host SMI internal signals. The rows in the tables are additive, which means that if more than one row is true for a particular scenario then the results for all of the activated rows will occur.

Table 166. Enable for PCU_SMB_ALERT#

Event	SMB_Mem_ HCTL.INTREN	SMB_Config_ HCFG.SMI_EN	SMB_Mem_ SCMD.SMBALTDIS	Result
PCU_SMB_ALERT# asserted low (always reported in SMB_Mem_ HSTS.SMBALERT)	X	1	0	Slave SMI# generated (SMBUS_SMI_STS)
	1	0	0	Interrupt generated

Table 167. Enables for SMBus Host Events

Event	SMB_Mem_ HCTL.INTREN	SMB_Config_ HCFG.SMI_EN	Event
Any combination of SMB_Mem_HSTS. FAILED, SMB_Mem_HSTS. BERR, SMB_Mem_HSTS. DEVERR, SMB_Mem_HSTS. INTR asserted	0	X	None
	1	0	Interrupt generated
	1	1	Host SMI# generated

Table 168. Enables for the Host Notify Command

SMB_Mem_ SCMD.HNINTREN	SMB_Config_ HCFG.SMI_EN	SMB_Mem_ SCMD.HNWAKEEN	Result
0	X	0	None
1	0	X	Interrupt generated
1	1	X	Slave SMI# generated (SMBUS_SMI_STS)

23.2.5 PCU_SMB_ALERT#

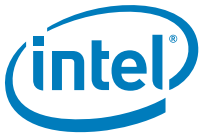
PCU_SMB_ALERT# is multiplexed with GPIO_S0_SC[53]. When enabled and the signal is asserted, the processor can generate an interrupt or an SMI#.

Note: Using this signal as a wake event from S3–S5 is not supported.

23.2.6 SMBus CRC Generation and Checking

If the SMB_Mem_AUXC.AAC is set, the processor automatically calculates and drives CRC at the end of the transmitted packet for write cycles, and will check the CRC for read cycles. It will not transmit the contents of the Packet Error Check Data Register (SMB_Mem_PEC) PEC register for CRC. The SMB_Mem_HCTL.PECEN bit must not be set if this bit is set, or unspecified behavior will result.

If the read cycle results in a CRC error, the SMB_Mem_HSTS.DEVERR bit and the SMB_Mem_AUXS.CRCE bit will be set.



23.2.7 SMBus Slave Interface

The processor does not implement a complete SMBus slave interface. Only the Host Notify Command is implemented to maintain specification compatibility.

23.2.7.1 Format of Host Notify Command

The processor tracks and responds to the standard Host Notify command as specified in the System Management Bus (SMBus) Specification, Version 2.0. The host address for this command is fixed to 0001000b. If the processor already has data for a previously-received host notify command which has not been serviced yet by the host software (as indicated by the SMB_Mem_SSTS.HNST bit), then it will NACK following the host address byte of the protocol. This allows the host to communicate non-acceptance to the master and retain the host notify address and data values for the previous cycle until host software completely services the interrupt.

Note: Host software must always clear the SMB_Mem_SSTS.HNST bit after completing any necessary reads of the address and data registers.

The following table shows the Host Notify format.

Table 169. Host Notify Format

Bit	Description	Driven By	Comment
1	Start	External Master	
8:2	SMB Host Address – 7 bits	External Master	Always 0001_000
9	Write	External Master	Always 0
10	ACK (or NACK)	Processor	Processor NACKs if SMB_Mem_SSTS.HNST is 1
17:11	Device Address – 7 bits	External Master	Indicates the address of the master; loaded into the Notify Device Address Register (SMB_Mem_NDA)
18	Unused – Always 0	External Master	7-bit-only address; this bit is inserted to complete the byte
19	ACK	Processor	
27:20	Data Byte Low – 8 bits	External Master	Loaded into the Notify Data Low Byte Register (SMB_Mem_NDLB)
28	ACK	Processor	
36:29	Data Byte High – 8 bits	External Master	Loaded into the Notify Data High Byte Register (SMB_Mem_NDHB)
37	ACK	Processor	
38	Stop	External Master	

23.3 Use

23.3.1 Function Disable

The SMBus interface may be disable by setting FUNC_DIS_2.SMB_DIS to 1b.

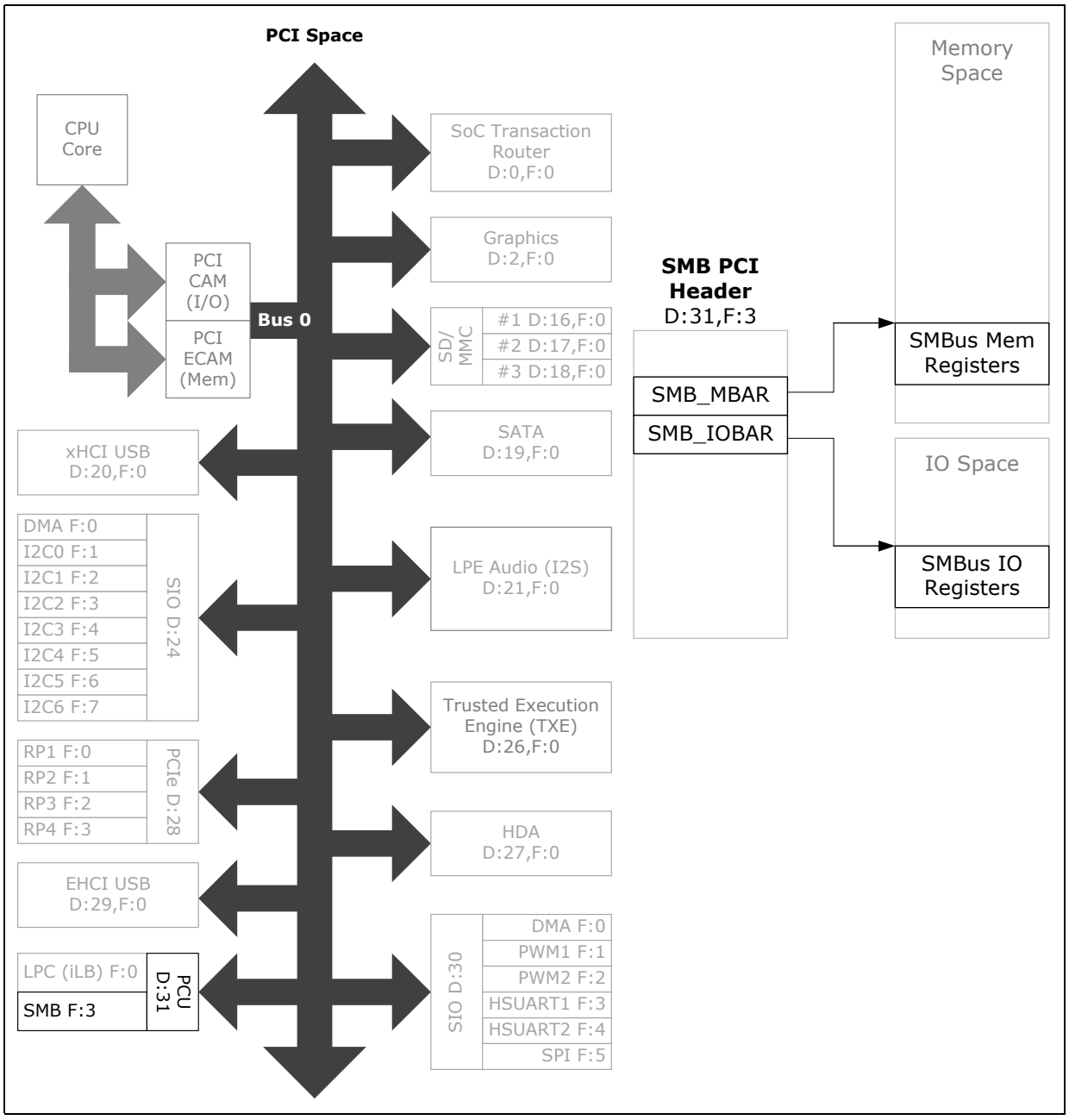
23.4 References

- System Management Bus (SMBus) Specification Version 2.0: http://www.smbus.org/specs/

23.5 Register Map

Refer to Chapter 3, "Register Access Methods" and Chapter 4, "Mapping Address Spaces" for additional information.

Figure 32. PCU – SMBus Register Map



23.6 PCU SMBus PCI Configuration Registers

Table 170. Summary of PCU SMBus PCI Configuration Registers—0/31/3

Offset	Size	Register ID—Description	Default Value
0h	2	"D31_F3_Vendor ID (SMB_Config_VID)—Offset 0h" on page 1121	8086h
2h	2	"D31_F3_Device ID (SMB_Config_DID)—Offset 2h" on page 1121	0F12h
4h	2	"D31_F3_Command (SMB_Config_CMD)—Offset 4h" on page 1122	0000h
6h	2	"D31_F3_Device_Status (SMB_Config_STAT)—Offset 6h" on page 1123	0290h
8h	1	"D31_F3_Revision ID (SMB_Config_REV)—Offset 8h" on page 1124	00h
9h	1	"D31_F3_Programming Interface (SMB_Config_PRGIF)—Offset 9h" on page 1124	00h
Ah	1	"D31_F3_Sub Class Code (SMB_config_SCC)—Offset Ah" on page 1125	05h
Bh	1	"D31_F3_Base Class Code (SMB_Config_BCC)—Offset Bh" on page 1125	0Ch
10h	4	"D31_F3_SMBus Memory Base Address (SMB_Config_MBARL)—Offset 10h" on page 1126	00000000h
14h	4	"D31_F3_SMBus Memory Base Address (SMB_Config_MBARH)—Offset 14h" on page 1126	00000000h
20h	4	"D31_F3_SMB Base Addr (SMB_Config_IOBAR)—Offset 20h" on page 1127	00000001h
2Ch	2	"D31_F3_SVID (SMB_Config_SVID)—Offset 2Ch" on page 1127	0000h
2Eh	2	"D31_F3_SID (SMB_Config_SID)—Offset 2Eh" on page 1128	0000h
34h	1	"D31_F3_CAP_POINTER (SMB_Config_CAP_POINTER)—Offset 34h" on page 1128	50h
3Ch	1	"D31_F3_Interrupt Line (SMB_Config_INTLN)—Offset 3Ch" on page 1129	00h
3Dh	1	"D31_F3_Interrupt Pin (SMB_Config_INTPN)—Offset 3Dh" on page 1129	02h
40h	1	"D31_F3_Host Configuration (SMB_Config_HCFG)—Offset 40h" on page 1130	00h
50h	2	"D31_F3_PID (SMB_Config_CAP_ID)—Offset 50h" on page 1131	0001h
52h	2	"D31_F3_PC (SMB_Config_PMC)—Offset 52h" on page 1131	0003h
54h	2	"D31_F3_PMCSR (SMB_Config_PMCSR)—Offset 54h" on page 1132	0008h
56h	1	"D31_F3_PMCSR_BSE (SMB_Config_PMCSR_BSE)—Offset 56h" on page 1133	00h
57h	1	"D31_F3_DATA (SMB_Config_DATA)—Offset 57h" on page 1133	00h
F0h	4	"IOSF Error Control (SMB_Config_ERR)—Offset F0h" on page 1134	00000000h
F8h	4	"D31_F3_Manufacturer's ID (SMB_Config_MANID)—Offset F8h" on page 1134	00000000h

23.6.1 D31_F3_Vendor ID (SMB_Config_VID)—Offset 0h

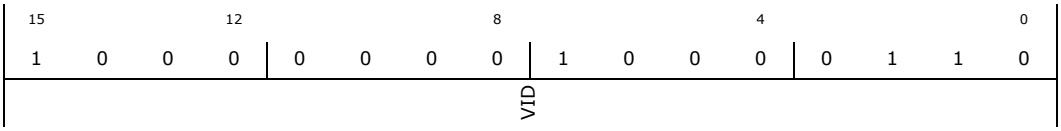
Vendor ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_VID: [B:0, D:31, F:3] + 0h

Default: 8086h



Bit Range	Default & Access	Description
15:0	8086h RO	**VID:** Vendor ID

23.6.2 D31_F3_Device ID (SMB_Config_DID)—Offset 2h

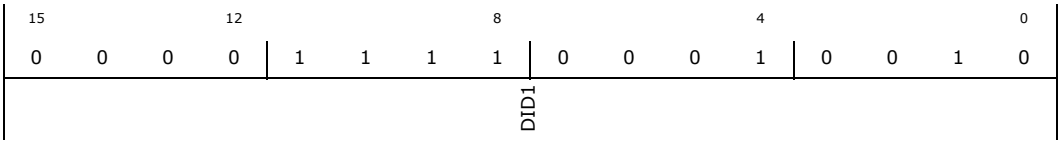
Indicates the SMBus controller device number. The upper 9-bits of this register are coming from centralize DevID unit indicating this processor. The lower 7 bits are indicating SMBus controller while the 2 most lower bits are controlled by the SMBus DID fuses.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_DID: [B:0, D:31, F:3] + 2h

Default: 0F12h



Bit Range	Default & Access	Description
15:0	0000111100010010b RO	**DID (DID1):** Device ID-Processor, value from the SETIDVALUE message

23.6.3 D31_F3_Command (SMB_Config_CMD)—Offset 4h

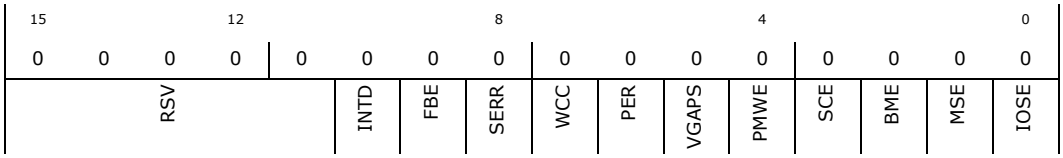
CMD register enables/disables memory/io space access and interrupt

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_CMD: [B:0, D:31, F:3] + 4h

Default: 0000h



Bit Range	Default & Access	Description
15:11	00000b RO	**Reserved (RSV):** Reserved
10	0b RW	**INTD:** Interrupt disable - 1 Disable SMBus to assert its interrupt
9	0b RO	**FBE:** FBE - reserved as '0'
8	0b RO	**SERR:** SERR enable - reserved as '0'
7	0b RO	**Wait Cycle Ctrl (WCC):** Wait cycle control - reserved as '0'
6	0b RO	**Parity error response (PER):** Parity error - reserved as '0'
5	0b RO	**VGA palette snnop (VGAPS):** VGA palette snoop - reserved as '0'
4	0b RO	**PMWE:** Postable Memory Write Enable - reserved as '0'
3	0b RO	**SCE:** Special Cycle Enable - reserved as '0'
2	0b RO	**BME:** Bus Master Enable - reserved as '0'
1	0b RW	**MSE:** Memory space enable - 1 enables access to the SM Bus memory space registers as defined by the Base Address Registes
0	0b RW	**IOSE:** I/O space enable - 1 enables access to the SM Bus I/O space registers as defined by the Base Address Register

23.6.4 D31_F3_Device_Status (SMB_Config_STAT)—Offset 6h

Configuration status register

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_STAT: [B:0, D:31, F:3] + 6h

Default: 0290h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DEVT		DPED	FB2B	UDF	FREQ66	CLI	INTS	RSV		

Bit Range	Default & Access	Description
15	0b RO	**DPE:** Detect Parity Error - reserved as '0'
14	0b RO	**SSE:** Signaled System Error - reserved as '0'
13	0b RO	**RMA:** Received Master Abort - reserved as '0'
12	0b RO	**RTA:** Received Target Abort - reserved as '0'
11	0b RO	**STA:** Signaled Target Abort - reserved as '0'
10:9	01b RO	**DEVT:** Devsel Timing Status reserved as 2'b01
8	0b RO	**DPED:** Data Parity Error Detected - reserved as '0'
7	1b RO	**Fast Back To Back (FB2B):** Fast Back To Back Capable - reserved as '1'
6	0b RO	**UDF:** User Defined Features - reserved as '0'
5	0b RO	**66 MHz Capable (FREQ66):** 66 MHz Capable - reserved as '0'
4	1b RO	**Capabilities List Indicator (CLI):** Capabilities List Indicator - set to '1'
3	0b RO	**INTS:** This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the command register
2:0	000b RO	**Reserved (RSV):** Reserved

23.6.5 D31_F3_Revision ID (SMB_Config_REV)—Offset 8h

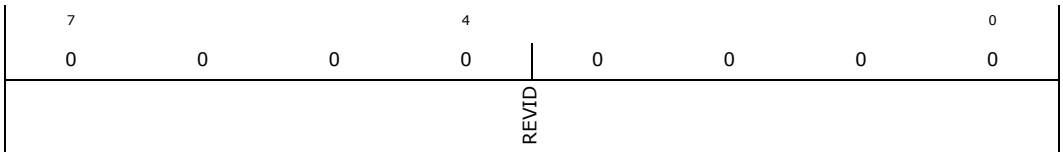
The value reported in this register is coming from centralize unit by the SETIDVALUE message

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_REV: [B:0, D:31, F:3] + 8h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**Revision ID (REVID):** Revision ID

23.6.6 D31_F3_Programming Interface (SMB_Config_PRGIF)—Offset 9h

The value reported in this register is coming from centralize unit by the SETIDVALUE message

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_PRGIF: [B:0, D:31, F:3] + 9h

Default: 00h

Bit Range	Default & Access	Description
7:0	00h RO	**Programming Interface (PRGIF):** Programming Interface

23.6.7 D31_F3_Sub Class Code (SMB_config_SCC)—Offset Ah

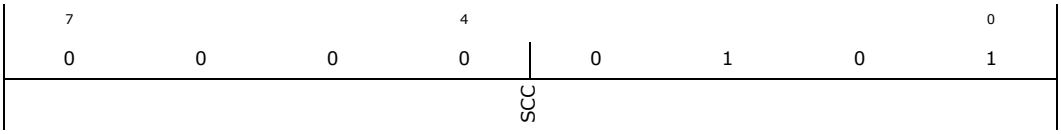
A value of 05h indicates that this device is a SM Bus serial controller

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_config_SCC: [B:0, D:31, F:3] + Ah

Default: 05h



Bit Range	Default & Access	Description
7:0	05h RO	**SCC:** Sub Class Code

23.6.8 D31_F3_Base Class Code (SMB_Config_BCC)—Offset Bh

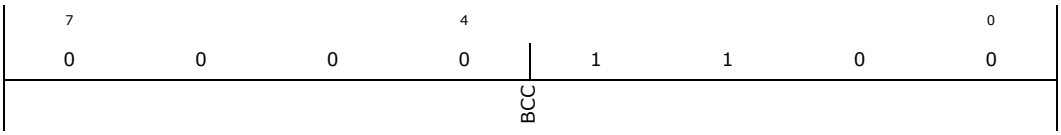
A value of 0Ch indicates that this device is a serial controller

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_BCC: [B:0, D:31, F:3] + Bh

Default: 0Ch



Bit Range	Default & Access	Description
7:0	0Ch RO	**BCC:** Base Class Code

23.6.9 D31_F3_SMBus Memory Base Address (SMB_Config_MBARL)—Offset 10h

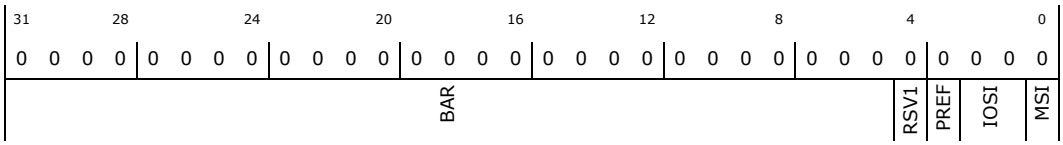
The memory bar

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SMB_Config_MBARL: [B:0, D:31, F:3] + 10h

Default: 00000000h



Bit Range	Default & Access	Description
31:5	000000h RW	**BAR:** Base Address - Provides the 32 byte system memory base address
4	0b RO	**Reserved (RSV1):** Reserved
3	0b RO	**PREF:** Hardwired to 0. Indicated that SMBMBAR is not prefetchable
2:1	00b RO	**Type (IOSI):** This field is hardwired to 2'b00 indicating that this range can be mapped anywhere within 32-bit address space.
0	0b RO	**MSI:** Memory Space Indicator - This read-only bit always is 0, indicating that the SMB logic is Memory mapped

23.6.10 D31_F3_SMBus Memory Base Address (SMB_Config_MBARH)—Offset 14h

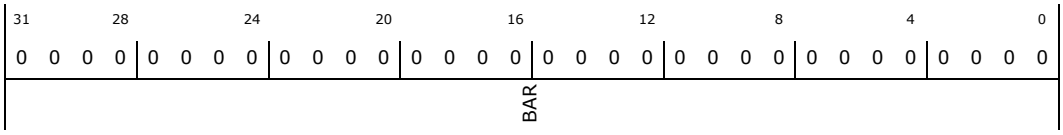
RESERVED

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SMB_Config_MBARH: [B:0, D:31, F:3] + 14h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**BAR:** RESERVED

23.6.11 D31_F3_SMB Base Addr (SMB_Config_IOBAR)—Offset 20h

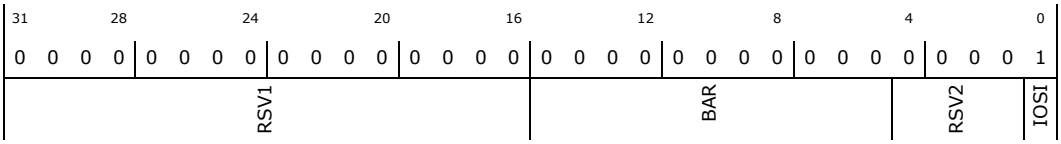
The I/O memory bar

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SMB_Config_IOBAR: [B:0, D:31, F:3] + 20h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0000h RO	**Reserved (RSV1):** Reserved
15:5	00000000000b RW	**BAR:** Base Address - Provides the 32 byte system I/O base address
4:1	0000b RO	**Reserved (RSV2):** Reserved
0	1b RO	**I/O Space Indicator (IOSI):** IO Space Indicator - This read-only bit always is 1, indicating that the SMB logic is I/O mapped

23.6.12 D31_F3_SVID (SMB_Config_SVID)—Offset 2Ch

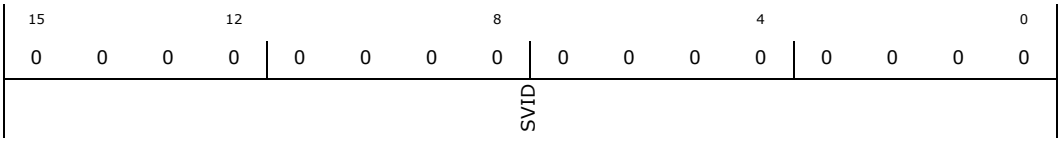
BIOS sets the value in this register to identify the Subsystem Vendor ID. The SMBus SVID register, in combination with the SMBus Subsystem ID register, enables the operating system to distinguish each subsystem from the others. **Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.**

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_SVID: [B:0, D:31, F:3] + 2Ch

Default: 0000h



Bit Range	Default & Access	Description
15:0	0000h RW/O	**SVID:** Subsystem Vendor ID

23.6.13 D31_F3_SID (SMB_Config_SID)—Offset 2Eh

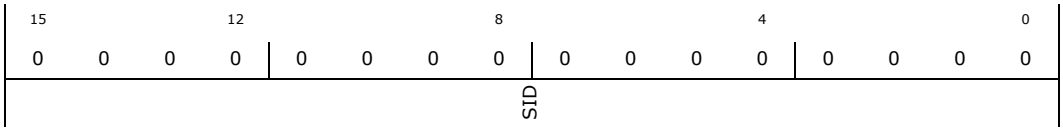
BIOS can write to this register to identify the Subsystem ID. The SID register, in combination with the SVID, enable the operating system to distinguish each subsystem from other(s). **Note: The software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.**

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_SID: [B:0, D:31, F:3] + 2Eh

Default: 0000h



Bit Range	Default & Access	Description
15:0	0000h RW/O	**SID:** Subsystem ID

23.6.14 D31_F3_CAP_POINTER (SMB_Config_CAP_POINTER)—Offset 34h

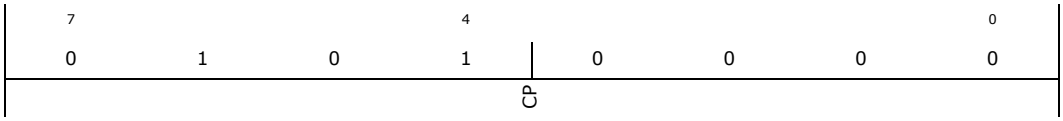
This optional register is used to point to a linked list of new capabilities implemented by this device. This register is only valid if the Capabilities List bit in the Status Register is set. If implemented, the bottom two bits are reserved and should be set to 00b. Software should mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_CAP_POINTER: [B:0, D:31, F:3] + 34h

Default: 50h



Bit Range	Default & Access	Description
7:0	50h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

23.6.15 D31_F3_Interrupt Line (SMB_Config_INTLN)—Offset 3Ch

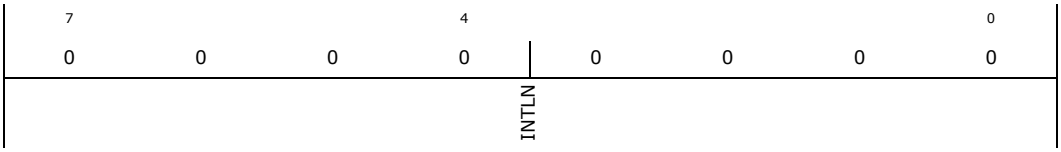
This data is not used

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_INTLN: [B:0, D:31, F:3] + 3Ch

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**INTLN:** Intrerrupt Line

23.6.16 D31_F3_Interrupt Pin (SMB_Config_INTPN)—Offset 3Dh

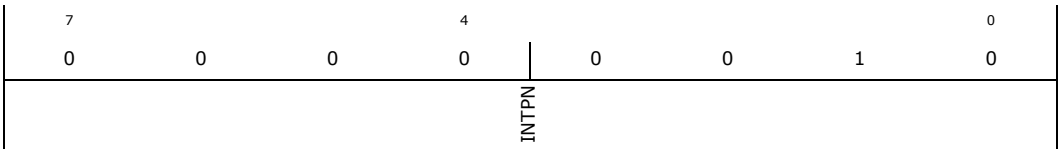
This register reflects the D31IP.SMIP in chipset configuration space

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_INTPN: [B:0, D:31, F:3] + 3Dh

Default: 02h



Bit Range	Default & Access	Description
7:0	02h RO	**INTPN:** The 4 msb bits are hardwired to 0, and the 4 lsb bitsare hardwired to 4'h2 indicates the INTB is used by the SMBus controller

23.6.17 D31_F3_Host Configuration (SMB_Config_HCFG)—Offset 40h

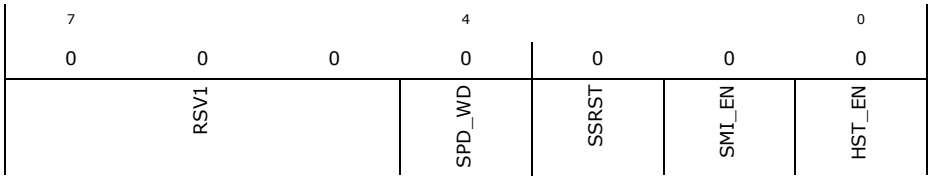
Host Configuration Register

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_HCFG: [B:0, D:31, F:3] + 40h

Default: 00h



Bit Range	Default & Access	Description
7:5	000b RO	**Reserved (RSV1):** Reserved
4	0b RW/O	**SPD write disable (SPD_WD):** This bit is must be set to 1b1 to disable writes to SPD which are on Host SMB address ranges 0xA0 0xAE. The SMBus range is unwriteable until next platform reset HW Default is 1b0. Note: This bit is locked on 1b1 and will be reset on PLTRST# reset. This should be set by BIOS memory reference code to 1b1. SW can only program this bit when both HCTL[6] = 1b0 (START) and HSTS[0] = 1b0 (HBSY), else it may result in an undefined behavior.
3	0b RW	**SSRST:** Soft SMBus Reset - When this bit is 1, the SMbus state machine and logic is reset. The HW will reset this bit to 0 when reset operation is completed
1	0b RW	**SMI_EN:** When this bit is set, any source of an SMB interrupt will instead be routed to generate an SMI
0	0b RW	**HST_EN:** When set, the SMB Host Controller interface is enabled to execute commands. The SMB_Mem_HCTL.INTREN bit needs to be enabled in order for the SMB Host Controller to interrupt or SMI#. Additionally, the SMB Host Controller will not respond to any new requests until all interrupt requests have been cleared

23.6.18 D31_F3_PID (SMB_Config_CAP_ID)—Offset 50h

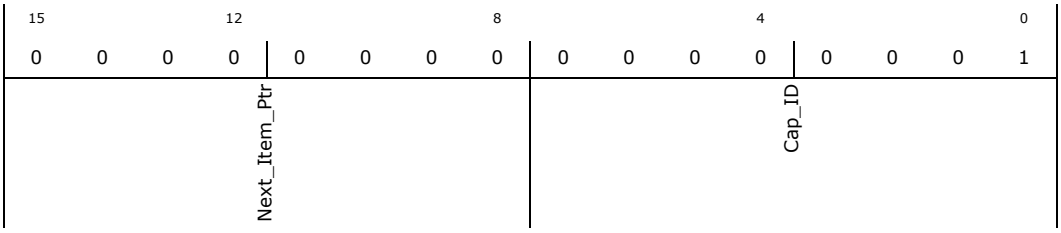
Power Management Capability ID

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_CAP_ID: [B:0, D:31, F:3] + 50h

Default: 0001h



Bit Range	Default & Access	Description
15:8	00h RO	**Next Item Pointer (Next_Item_Ptr):** This field provides an offset into the functions PCI Configuration Space pointing to the location of next item in the functions capability list. If there are no additional items in the Capabilities List, this register is set to 00h.
7:0	01h RO	**Capability Identifier (Cap_ID):** This field, when 01h identifies the linked list item as being the PCI Power Management registers.

23.6.19 D31_F3_PC (SMB_Config_PMC)—Offset 52h

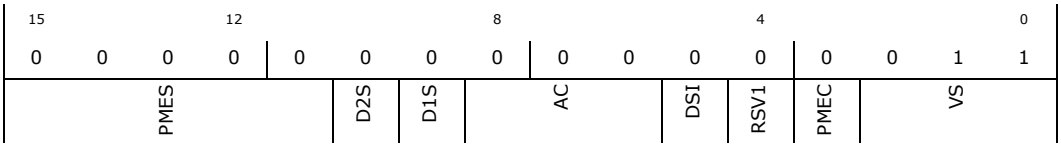
Power Management Capabilities

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_PMC: [B:0, D:31, F:3] + 52h

Default: 0003h



Bit Range	Default & Access	Description
15:11	00000b RO	**PME_Support (PMES):** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. bit(11) X XXX1b - PME# can be asserted from D0 bit(12) X XX1Xb - PME# can be asserted from D1 bit(13) X X1XXb - PME# can be asserted from D2 bit(14) X 1XXXb - PME# can be asserted from D3hot bit(15) 1 XXXXb - PME# can be asserted from D3cold
10	0b RO	**D2_Support (D2S):** If this bit is a '1', this function supports the D2 Power Management State. Functions that do not support D2 must always return a value of '0' for this bit.
9	0b RO	**D1_Support (D1S):** If this bit is a '1', this function supports the D1 Power Management State. Functions that do not support D2 must always return a value of '0' for this bit.

Bit Range	Default & Access	Description
8:6	000b RO	**Aux_Current (AC):** Auxiliary current - should be 3'b000
5	0b RO	**DSI:** Device specific initialization
4	0b RO	**Reserved (RSV1):** Reserved
3	0b RO	**PME Clock (PMEC):** PME Clock. Does not apply.
2:0	011b RO	**Version (VS):** A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.

23.6.20 D31_F3_PMCSR (SMB_Config_PMCSR)—Offset 54h

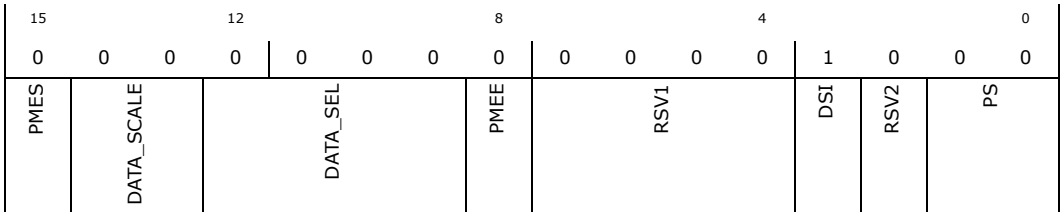
Power Management Control/Status Register

Access Method

Type: PCI Configuration Register (Size: 16 bits)

SMB_Config_PMCSR: [B:0, D:31, F:3] + 54h

Default: 0008h



Bit Range	Default & Access	Description
15	0b RO	**PME_Status (PMES):** SMBus does not initiate PME#. Hence this bit should be always '0'
14:13	00b RO	**Data_Scale (DATA_SCALE):** If the Data register has not been implemented, this field must return '00b' when the PMCSR is read.
12:9	0000b RO	**Data_Select (DATA_SEL):** If the Data register is not implemented, this field should be read only and return '0000b' when the PMCSR is read.
8	0b RO	**PME_En (PMEE):** Should be '0' since SMBus does not initiate PME#
7:4	0000b RO	**Reserved (RSV1):** Reserved
3	1b RO	**No_Soft_Reset (DSI):** When set (1), this bit indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	0b RO	**Reserved (RSV2):** Reserved

Bit Range	Default & Access	Description
1:0	00b RW	**PowerState (PS):** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.

23.6.21 D31_F3_PMCSR_BSE (SMB_Config_PMCSR_BSE)—Offset 56h

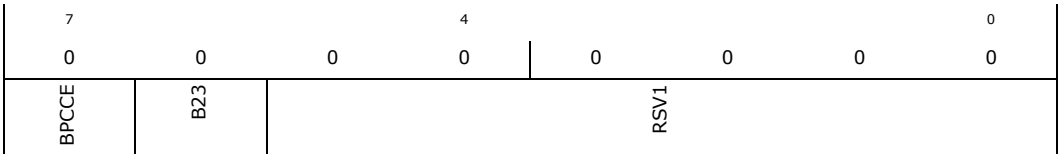
PMCSR_BSE supports PCI bridge specific functionality and is required for all PCI-to-PCI bridges.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_PMCSR_BSE: [B:0, D:31, F:3] + 56h

Default: 00h



Bit Range	Default & Access	Description
7	0b RO	**BPCC_En (BPCCE):** Bus Power/Clock Control Enable - Does not apply
6	0b RO	**B2_B3 (B23):** B2/B3 support for D3hot - Does not apply
5:0	00h RO	**Reserved (RSV1):** Reserved

23.6.22 D31_F3_DATA (SMB_Config_DATA)—Offset 57h

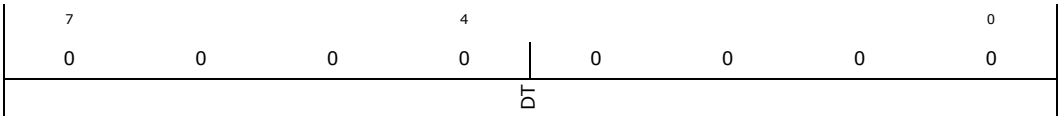
PMCSR_BSE supports PCI bridge specific functionality and is required for all PCI-to-PCI bridges.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

SMB_Config_DATA: [B:0, D:31, F:3] + 57h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**Data (DT):** Data - Does not apply

23.6.23 IOSF Error Control (SMB_Config_ERR)—Offset F0h

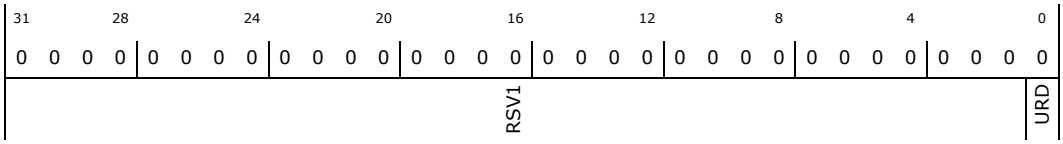
IOSF Error Control- is set when an Unsupported Request Detected

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SMB_Config_ERR: [B:0, D:31, F:3] + F0h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0000h RO	**Reserved (RSV1):** Reserved
0	0b RW	**URD:** Unsupported Request Detected, SMBus could not receive unsupported request hence this bit is tied to 1b0

23.6.24 D31_F3_Manufacturer's ID (SMB_Config_MANID)—Offset F8h

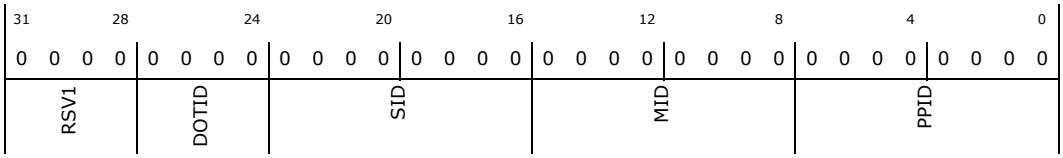
Manufacturer's ID Register,The value reported in this register is coming from centralize unit by the SETIDVALUE message

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SMB_Config_MANID: [B:0, D:31, F:3] + F8h

Default: 00000000h



Bit Range	Default & Access	Description
31:28	00h RO	**Reserved (RSV1):** Reserved
27:24	0000b RO	**DOTID:** The value reported in this field is coming from centralize unit by the SETIDVALUE message
23:16	00h RO	**SID:** The value reported in this field is coming from centralize unit by the SETIDVALUE message
15:8	00h RO	**MID:** The value reported in this field is coming from centralize unit by the SETIDVALUE message
7:0	00h RO	**PPID:** The value reported in this field is coming from centralize unit by the SETIDVALUE message

23.7 PCU SMBus Memory Mapped I/O Registers

Table 171. Summary of PCU SMBus Memory Mapped I/O Registers—SMB_Config_MBARL

Offset	Size	Register ID—Description	Default Value
0h	1	"Host Status Register (SMB_Mem_HSTS)—Offset 0h" on page 1135	00h
2h	1	"Host Control Register (SMB_Mem_HCTL)—Offset 2h" on page 1136	00h
3h	1	"Host Command Register (SMB_Mem_HCMD)—Offset 3h" on page 1138	00h
4h	1	"Transmit Slave Address Register (SMB_Mem_TSA)—Offset 4h" on page 1138	00h
5h	1	"Data 0 Register (SMB_Mem_HD0)—Offset 5h" on page 1139	00h
6h	1	"Data 1 Register (SMB_Mem_HD1)—Offset 6h" on page 1139	00h
7h	1	"Host Block Data (SMB_Mem_HBD)—Offset 7h" on page 1140	00h
8h	1	"Packet Error Check Data Register (SMB_Mem_PEC)—Offset 8h" on page 1141	00h
Ch	1	"Auxiliary Status (SMB_Mem_AUXS)—Offset Ch" on page 1141	00h
Dh	1	"Auxiliary Control (SMB_Mem_AUXC)—Offset Dh" on page 1142	00h
Fh	1	"SMBUS_PIN_CTL Register (SMB_Mem_SMBC)—Offset Fh" on page 1142	07h
10h	1	"Slave Status Register (SMB_Mem_SSTS)—Offset 10h" on page 1143	00h
11h	1	"Slave Command Register (SMB_Mem_SCMD)—Offset 11h" on page 1143	00h
14h	1	"Notify Device Address Register (SMB_Mem_NDA)—Offset 14h" on page 1144	00h
16h	1	"Notify Data Low Byte Register (SMB_Mem_NDLB)—Offset 16h" on page 1145	00h
17h	1	"Notify Data High Byte Register (SMB_Mem_NDHB)—Offset 17h" on page 1145	00h

23.7.1 Host Status Register (SMB_Mem_HSTS)—Offset 0h

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no affect

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_HSTS: [MBARL] + 0h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
BDS	IUS	SMB_ALERTB	FAILED	BERR	DEVERR	INTR	HBSY

Bit Range	Default & Access	Description
7	0b RW	**BDS:** BYTE_DONE_STS (BDS) - This bit will be set to 1 when the host controller has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. Software clears the bit by writing a 1 to the bit position. This bit has no meaning for block transfers when the 32-byte buffer is enabled.**Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the SMBus host will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.**
6	0b RW	**IUS:** In Use Status (IUS) - After a full PCI reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller. This bit has no other effect on the hardware, and is only used as semaphore among various independent software threads that may need to use the SMBus host
5	0b RW	**SMB_ALERTB:** the processor sets this bit to a '1' to indicates source of the interrupt or SMI# was the SMB_ALERTB signal. Software resets this bit by writing a 1 to this location.
4	0b RW	**FAILED:** Failed (FAIL) - When set, this indicates that the source of the interrupt or SMI was a failed bus transaction. This is set in response to the KILL bit being set to terminate the host transaction.
3	0b RW	**BERR:** Bus Error (BERR) - When set, this indicates the source of the interrupt or SMI was a transaction collision.
2	0b RW	**DEVERR:** Device Error (DERR) - When set, this indicates that the source of the interrupt or SMI was due one of the following: Illegal Command Field Unclaimed Cycle (host initiated) Host Device Time-out Error. CRC Error Write Protection Access Error (START bit will be cleared, Device Error will be set and Host Busy is never set because SMB Transaction never took place).
1	0b RW	**INTR:** Interrupt (INTR) - When set, this indicates that the source of the interrupt or SMI was the successful completion of its last command.
0	0b RW	**HBSY:** Host Busy (HBSY) - A '1' indicates that the SMBus host is running a command from the host interface. No SMB registers should be accessed while this bit is set.

23.7.2 Host Control Register (SMB_Mem_HCTL)—Offset 2h

Host Control Register

Note: A read to this register will clear the pointer in the 32-byte buffer.

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_HCTL: [MBARL] + 2h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
PECEN	SATRT	LBYTE	SMBCMD			KILL	INTREN

Bit Range	Default & Access	Description
7	0b RW	**PECEN:** PEC_EN: When set to '1', this bit causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. When this bit is cleared to '0', the SMBus host controller does not perform the transaction with the PEC phase appended. This bit must be written prior to the write in which the START bit is set.
6	0b WO	**START (SATRT):** START: This write-only bit is used to initiate the command described in the SMB_CMD field. All registers should be setup prior to writing a '1' to this bit position. This bit always reads zero. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the SMBus controller has finished the command.
4:2	000b RW	**SMBCMD:** SMB_CMD - As shown by the bit encoding below, indicates which command the SMBus host is to perform. If enabled, the SMBus host will generate an interrupt or SMI when the command has completed If the value is for a non-supported or reserved command, the SMBus host will set the device error (DEV_ERR) status bit and generate an interrupt when the START bit is set. The SMBus controller will perform no command, and will not operate until DEV_ERR is cleared.***3'b000 - Quick*** The slave address and read/write value (bit 0) are stored in the tx slave address register ***3'b001 - Byte*** This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 register will contain the read data. ***3'b010 - Byte Data*** This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data ***3'b011 - Word Data*** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 and DATA1 registers will contain the read data. ***3'b100 - Process Call*** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. ***3'b101 - Block*** This command uses the transmit slave address, command, and DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. ***3'b111 - Block Process*** This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. **Note: E32B bit in the Auxiliary Control Register must be set for this command to work.**
1	0b RW	**KILL:** KILL - When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI) selected by the SMB_Cfg_HCFG.SMI_EN field. This bit, once set, must be cleared to allow the SMB Host Controller to function normally
0	0b RW	**INTREN:** Enable the generation of an interrupt or SMI upon the completion of the command. Enables also other interrupt sendings , like ALERT and HOST_NOTIFY

23.7.3 Host Command Register (SMB_Mem_HCMD)—Offset 3h

This eight bit field is transmitted by the host controller in the command field of the SMB protocol during the execution of any command.

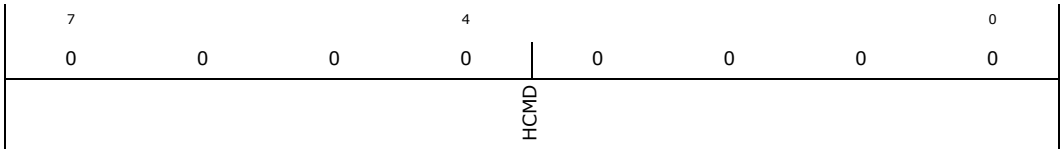
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_HCMD: [MBARL] + 3h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**HCMD:** Command to be transmitted

23.7.4 Transmit Slave Address Register (SMB_Mem_TSA)—Offset 4h

This register is transmitted by the host controller in the slave address field of the SMB protocol. This is the address of the target

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_TSA: [MBARL] + 4h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h

Bit Range	Default & Access	Description
7:1	0000000b RW	**ADDR:** 7-bit address of the targeted slave
0	0b RW	**RW:** Direction of the host transfer. 1 = read, 0 = write Note: Writes to TSA values of 0xA0 0xAE are blocked depending on the setting of the SPD write disable bit in HCFG D31_F3_HostConfiguration.

23.7.5 Data 0 Register (SMB_Mem_HD0)—Offset 5h

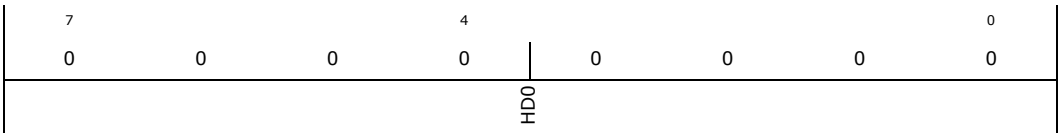
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_HD0: [MBARL] + 5h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**HD0:** DATA0/COUNT - This field contains the eight bit data sent in the DATA0 field of the SMB protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log illegal block counts.

23.7.6 Data 1 Register (SMB_Mem_HD1)—Offset 6h

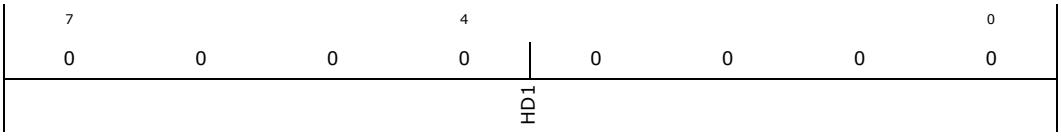
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_HD1: [MBARL] + 6h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**HD1:** DATA1 - This eight bit register is transmitted in the DATA1 field of the SMB protocol during the execution of any command.

23.7.7 Host Block Data (SMB_Mem_HBD)—Offset 7h

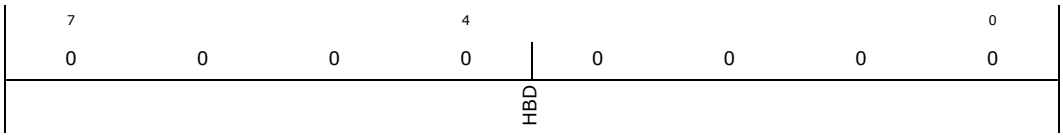
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_HBD: [MBARL] + 7h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**HBD:** Block Data (BDTA) - This is either a register, or a pointer into a 32-byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the INTEL Processor. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E32B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host Controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E32B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the FIFO pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E32B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the FIFO pointed to by this register. If the byte count has been exhausted or the 32-byte FIFO has been filled, the controller will generate an SMI or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the FIFO to when the DONE_STS bit is cleared, the controller will insert wait-states on the interface.

23.7.8 Packet Error Check Data Register (SMB_Mem_PEC)—Offset 8h

This register contains the 8-bit CRC value that is used as the Packet Error Check on SMBus. For writes, this register is written by software prior to running the command. For reads, this register is read by software after the read command is completed on SMBus.

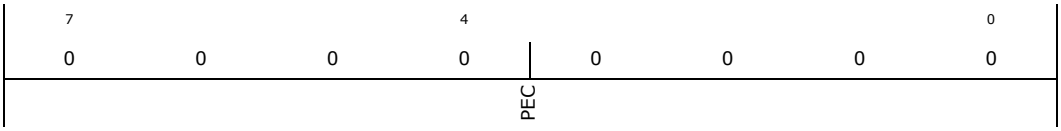
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_PEC: [MBARL] + 8h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**PEC:** This 8-bit register is written with the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the IUS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

23.7.9 Auxiliary Status (SMB_Mem_AUXS)—Offset Ch

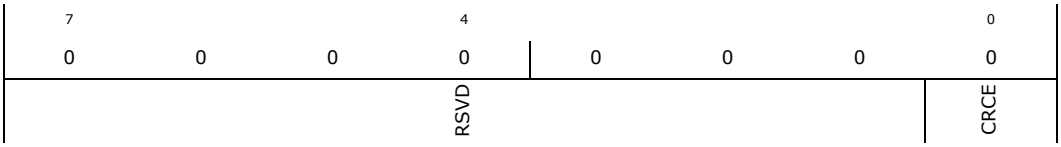
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_AUXS: [MBARL] + Ch

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:1	0000000b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**CRCE:** CRC Error (CRCE) - This bit is set if a received message contained a CRC error. When this bit is set, the DEVERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after SMBus controller has received the final data bit transmitted by external slave.

23.7.10 Auxiliary Control (SMB_Mem_AUXC)—Offset Dh

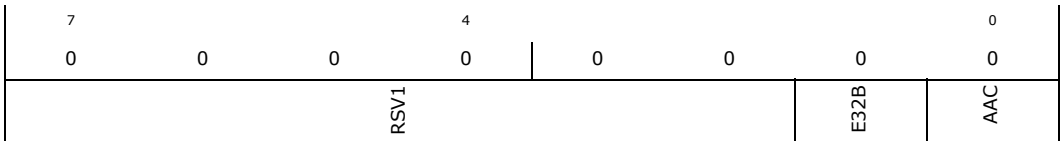
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_AUXC: [MBARL] + Dh

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:2	000000b RO	**Reserved (RSV1):** Reserved
1	0b RW	**E32B:** Enable 32-byte Buffer (E32B) - When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the controller generates an interrupt
0	0b RW/O	**AAC:** Automatically Append CRC (AAC) - When set, the SMBus controller will automatically append the CRC. This bit must not be changed during SM Bus transactions, or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

23.7.11 SMBUS_PIN_CTL Register (SMB_Mem_SMBC)—Offset Fh

Software bus accesses register

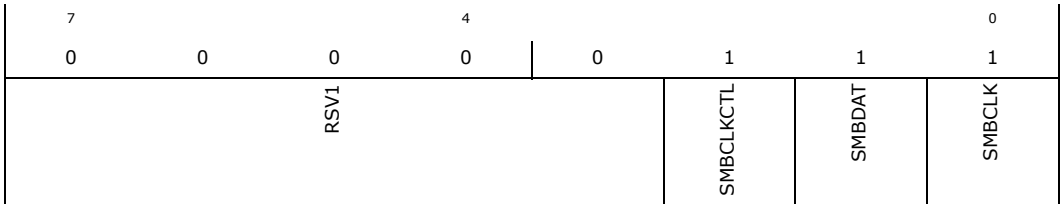
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_SMBC: [MBARL] + Fh

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 07h



Bit Range	Default & Access	Description
7:3	00000b RO	**Reserved (RSV1):** Reserved

Bit Range	Default & Access	Description
2	1b RW	**SMBCLKCTL:** This Read/Write bit has a default of 1. 0 = SMBus controller will drive the SMB_CLK pin low, independent of what the other SMB logic would otherwise indicate for the SMB_CLK pin. 1 = The SMB_CLK pin is Not overdriven low. The other SMBus logic controls the state of the pin.
1	1b RO	**SMBDAT:** This pin returns the value on the SMB_DATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	1b RO	**SMBCLK:** This pin returns the value on the SMB_CLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

23.7.12 Slave Status Register (SMB_Mem_SSTS)—Offset 10h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally

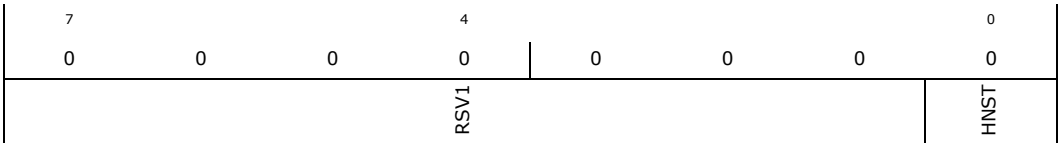
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_SSTS: [MBARL] + 10h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:1	0000000b RO	**Reserved (RSV1):** Reserved
0	0b RW	**HNST:** HOST_NOTIFY_STS: The SMBus controller sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the SMBus controller will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the SMBus controller will NACK the first byte (host address) of any new 'Host Notify' commands on the SMBus. Writing a 0 to this bit has no effect.

23.7.13 Slave Command Register (SMB_Mem_SCMD)—Offset 11h

All bits in this register are implemented in a slow (64khz) clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally. Also, software must confirm the prior written value before writing to the register again.

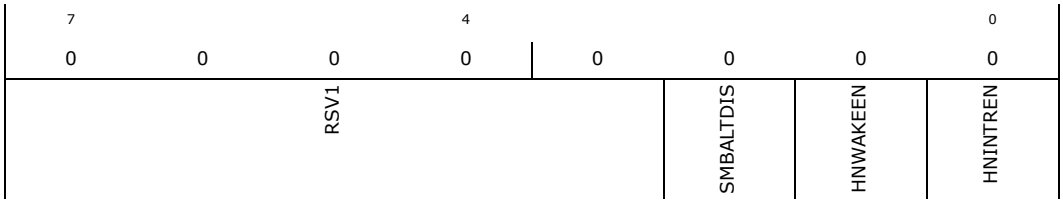
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_SCMD: [MBARL] + 11h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:3	00000b RO	**Reserved (RSV1):** Reserved
2	0b RW	**SMBALTDIS:** Software sets this bit to 1 to block the generation of the interrupt or SMI# due to the SMB_ALERTB source. This bit is logically inverted and 'AND'ed with the SMB_ALERTB bit of HSTS register. The resulting signal is distributed to the SMI# and/or interrupt generation logic.
1	0b RW	**HNWAKEEN:** Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event.
0	0b RW	**HNINTREN:** Software sets this bit to 1 to enable the generation of interrupt or SMI when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either INTRB or SMI is generated, depending on the value of the SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI) will be generated. The interrupt (or SMI) is logically generated by AND'ing the STS and INTREN bits.

23.7.14 Notify Device Address Register (SMB_Mem_NDA)—Offset 14h

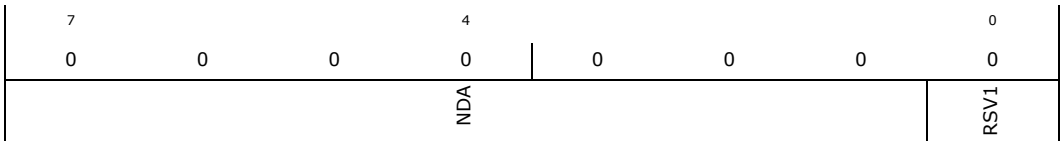
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_NDA: [MBARL] + 14h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:1	0000000b RO	**NDA:** DEVICE_ADDRESS - This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	0b RO	**Reserved (RSV1):** Reserved

23.7.15 Notify Data Low Byte Register (SMB_Mem_NDLB)—Offset 16h

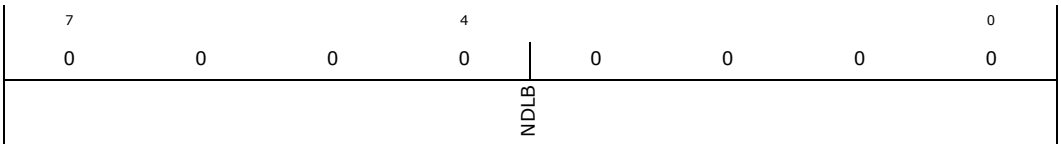
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_NDLB: [MBARL] + 16h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**NDLB:** DATA_LOW_BYTE - This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

23.7.16 Notify Data High Byte Register (SMB_Mem_NDHB)—Offset 17h

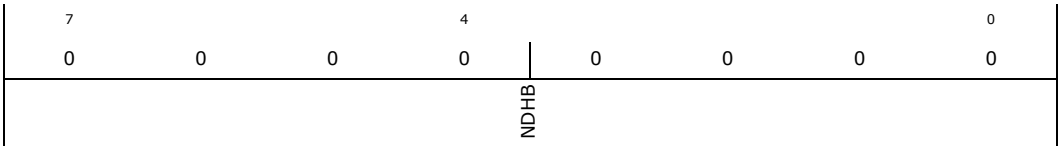
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

SMB_Mem_NDHB: [MBARL] + 17h

MBARL Type: PCI Configuration Register (Size: 32 bits)
MBARL Reference: [B:0, D:31, F:3] + 10h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**NDHB:** DATA_HIGH_BYTE - This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

23.8 PCU SMBus I/O Registers

Table 172. Summary of PCU SMBus I/O Registers—SMB_Config_IOBAR

Offset	Size	Register ID—Description	Default Value
0h	1	"Host Status Register (SMB_Mem_HSTS_io)—Offset 0h" on page 1147	00h
2h	1	"Host Control Register (SMB_Mem_HCTL_io)—Offset 2h" on page 1148	00h
3h	1	"Host Command Register (SMB_Mem_HCMD_io)—Offset 3h" on page 1150	00h
4h	1	"Transmit Slave Address Register (SMB_Mem_TSA_io)—Offset 4h" on page 1150	00h
5h	1	"Data 0 Register (SMB_Mem_HD0_io)—Offset 5h" on page 1151	00h
6h	1	"Data 1 Register (SMB_Mem_HD1_io)—Offset 6h" on page 1151	00h
7h	1	"Host Block Data (SMB_Mem_HBD_io)—Offset 7h" on page 1152	00h
8h	1	"Packet Error Check Data Register (SMB_Mem_PEC_io)—Offset 8h" on page 1153	00h
Ch	1	"Auxiliary Status (SMB_Mem_AUXS_io)—Offset Ch" on page 1153	00h
Dh	1	"Auxiliary Control (SMB_Mem_AUXC_io)—Offset Dh" on page 1154	00h
Fh	1	"SMBUS_PIN_CTL Register (SMB_Mem_SMBC_io)—Offset Fh" on page 1154	07h
10h	1	"Slave Status Register (SMB_Mem_SSTS_io)—Offset 10h" on page 1155	00h
11h	1	"Slave Command Register (SMB_Mem_SCMD_io)—Offset 11h" on page 1156	00h
14h	1	"Notify Device Address Register (SMB_Mem_NDA_io)—Offset 14h" on page 1157	00h
16h	1	"Notify Data Low Byte Register (SMB_Mem_NDLB_io)—Offset 16h" on page 1157	00h
17h	1	"Notify Data High Byte Register (SMB_Mem_NDHB_io)—Offset 17h" on page 1158	00h

23.8.1 Host Status Register (SMB_Mem_HSTS_io)—Offset 0h

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a zero to any bit position has no affect

Access Method

Type: I/O Register (Size: 8 bits)

SMB_Mem_HSTS_io: [IOBAR] + 0h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
BDS	IUS	SMB_ALERTB	FAILED	BERR	DEVERR	INTR	HBSY

Bit Range	Default & Access	Description
7	0b RW	**BDS:** BYTE_DONE_STS (BDS) - This bit will be set to 1 when the host controller has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. Note that this bit will be set, even on the last byte of the transfer. Software clears the bit by writing a 1 to the bit position. This bit has no meaning for block transfers when the 32-byte buffer is enabled.**Note: When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit (bit 1 in this register). When the interrupt handler clears the BYTE_DONE_STS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the SMBus host will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases.**
6	0b RW	**IUS:** In Use Status (IUS) - After a full PCI reset, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller. This bit has no other effect on the hardware, and is only used as semaphore among various independent software threads that may need to use the SMBus host
5	0b RW	**SMB_ALERTB:** the processor sets this bit to a '1' to indicates source of the interrupt or SMI# was the SMB_ALERTB signal. Software resets this bit by writing a 1 to this location.
4	0b RW	**FAILED:** Failed (FAIL) - When set, this indicates that the source of the interrupt or SMI was a failed bus transaction. This is set in response to the KILL bit being set to terminate the host transaction.
3	0b RW	**BERR:** Bus Error (BERR) - When set, this indicates the source of the interrupt or SMI was a transaction collision.
2	0b RW	**DEVERR:** Device Error (DERR) - When set, this indicates that the source of the interrupt or SMI was due one of the following: Illegal Command Field Unclaimed Cycle (host initiated) Host Device Time-out Error. CRC Error Write Protection Access Error (START bit will be cleared, Device Error will be set and Host Busy is never set because SMB Transaction never took place).
1	0b RW	**INTR:** Interrupt (INTR) - When set, this indicates that the source of the interrupt or SMI was the successful completion of its last command.
0	0b RW	**HBSY:** Host Busy (HBSY) - A '1' indicates that the SMBus host is running a command from the host interface. No SMB registers should be accessed while this bit is set. Exception: The BLOCK DATA REGISTER can be accessed when this bit is set ONLY when the SMB_CMD bits (in Host control register) are programmed for Block command or I2C Read command. This is necessary in order to check the DONE_STS bit.

23.8.2 Host Control Register (SMB_Mem_HCTL_io)—Offset 2h

Host Control Register

Note: A read to this register will clear the pointer in the 32-byte buffer.

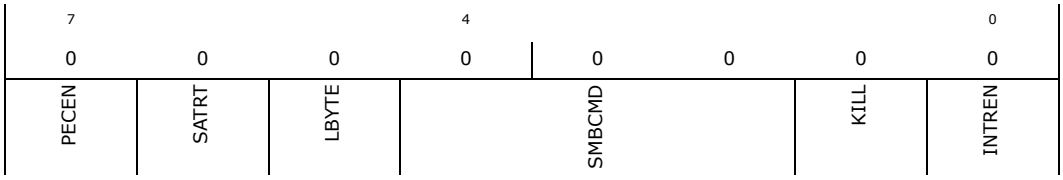
Access Method

Type: I/O Register (Size: 8 bits)

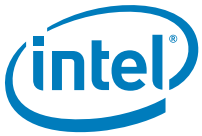
SMB_Mem_HCTL_io: [IOBAR] + 2h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7	0b RW	**PECEN:** PEC_EN: When set to '1', this bit causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC Register. For reads, the PEC byte is loaded in to the PEC Register. When this bit is cleared to '0', the SMBus host controller does not perform the transaction with the PEC phase appended. This bit must be written prior to the write in which the START bit is set.
6	0b WO	**START (SATRT):** START: This write-only bit is used to initiate the command described in the SMB_CMD field. All registers should be setup prior to writing a '1' to this bit position. This bit always reads zero. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the SMBus controller has finished the command.
5	0b RW	**LBYTE:** LAST_BYTE: Used for I2C Read commands as an indication that the next byte will be the last one to be received for that block. The algorithm and usage model for this bit will be as follows (assume a message of n bytes): A. When the software sees the BYTE_DONE_STS bit set (bit 7 in the SMBus Host Status Register) for each of bytes 1 through n-2 of the message, the software should then read the Block Data Byte Register to get the byte that was just received. B. After reading each of bytes 1 to n-2 of the message, the software will then clear the BYTE_DONE_STS bit. C. After receiving byte n-1 of the message, the software will then set the 'LAST BYTE' bit. The software will then clear the BYTE_DONE_STS bit. D. The Intel PCH will then receive the last byte of the message (byte n). However, the Intel PCH state machine will see the LAST BYTE bit set, and instead of sending an ACK after receiving the last byte, it will instead send a NAK. E. After receiving the last byte (byte n), the software will still clear the BYTE_DONE_STS bit. However, the LAST_BYTE bit will be irrelevant at that point. Note: This bit may be set when the TCO timer causes the SECOND_TO_STS bit to be set. See the TCO2_STS Register in Volume 1, bit 1 for more details on that bit. The SMBus device driver should clear the LAST_BYTE bit (if it is set) before starting any new command. Note: In addition to I2C Read Commands, the LAST_BYTE bit will also cause Block Read/Write cycles to stop prematurely (at the end of the next byte).



Bit Range	Default & Access	Description
4:2	000b RW	**SMBCMD:** SMB_CMD - As shown by the bit encoding below, indicates which command the SMBus host is to perform. If enabled, the SMBus host will generate an interrupt or SMI when the command has completed If the value is for a non-supported or reserved command, the SMBus host will set the device error (DEV_ERR) status bit and generate an interrupt when the START bit is set. The SMBus controller will perform no command, and will not operate until DEV_ERR is cleared.***3'b000 - Quick*** The slave address and read/write value (bit 0) are stored in the tx slave address register ***3'b001 - Byte*** This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 register will contain the read data. ***3'b010 - Byte Data*** This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data ***3'b011 - Word Data*** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes the DATA0 and DATA1 registers will contain the read data. ***3'b100 - Process Call*** This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. ***3'b101 - Block*** This command uses the transmit slave address, command, and DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. ***3'b110 - I2C Read*** This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The Intel PCH will continue reading data until the NAK is received. ***3'b111 - Block Process*** This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. **Note: E32B bit in the Auxiliary Control Register must be set for this command to work.**
1	0b RW	**KILL:** KILL - When set, kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI) selected by the SMB_INTRSEL field. This bit, once set, must be cleared to allow the SMB Host Controller to function normally
0	0b RW	**INTREN:** Enable the generation of an interrupt or SMI upon the completion of the command. Enables also other interrupt sendings , like ALERT and HOST_NOTIFY

23.8.3 Host Command Register (SMB_Mem_HCMD_io)—Offset 3h

This eight bit field is transmitted by the host controller in the command field of the SMB protocol during the execution of any command.

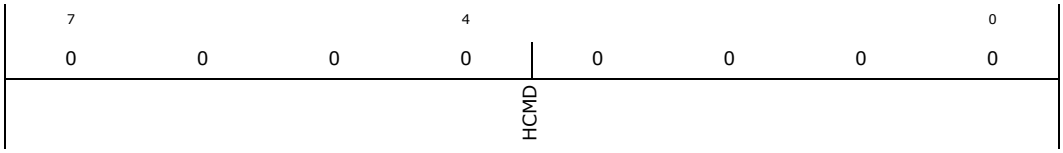
Access Method

Type: I/O Register (Size: 8 bits)

SMB_Mem_HCMD_io: [IOBAR] + 3h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**HCMD:** Command to be transmitted

23.8.4 Transmit Slave Address Register (SMB_Mem_TSA_io)—Offset 4h

This register is transmitted by the host controller in the slave address field of the SMB protocol. This is the address of the target

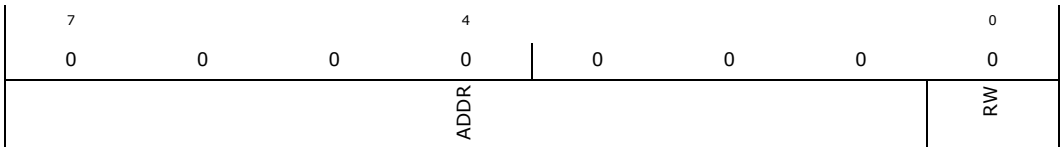
Access Method

Type: I/O Register (Size: 8 bits)

SMB_Mem_TSA_io: [IOBAR] + 4h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:1	0000000b RW	**ADDR:** 7-bit address of the targeted slave
0	0b RW	**RW:** Direction of the host transfer. 1 = read, 0 = write Note: Writes to TSA values of 0xA0 0xAE are blocked depending on the setting of the SPD write disable bit in HCFG D31_F3_HostConfiguration.

23.8.5 Data 0 Register (SMB_Mem_HD0_io)—Offset 5h

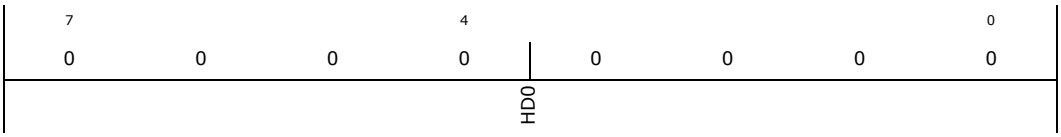
Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_HD0_io: [IOBAR] + 5h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**HD0:** DATA0/COUNT - This field contains the eight bit data sent in the DATA0 field of the SMB protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log illegal block counts.

23.8.6 Data 1 Register (SMB_Mem_HD1_io)—Offset 6h

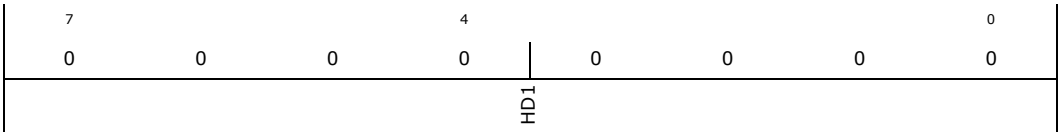
Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_HD1_io: [IOBAR] + 6h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**HD1:** DATA1 - This eight bit register is transmitted in the DATA1 field of the SMB protocol during the execution of any command.

23.8.7 Host Block Data (SMB_Mem_HBD_io)—Offset 7h

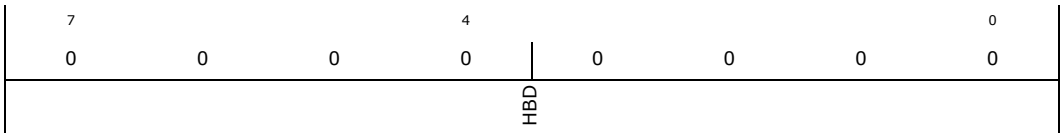
Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_HBD_io: [IOBAR] + 7h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**HBD:** Block Data (BDTA) - This is either a register, or a pointer into a 32-byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read, just as it behaved on the INTEL Processor. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E32B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host Controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E32B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the FIFO pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E32B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the FIFO pointed to by this register. If the byte count has been exhausted or the 32-byte FIFO has been filled, the controller will generate an SMI or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the FIFO to when the DONE_STS bit is cleared, the controller will insert wait-states on the interface.

23.8.8 Packet Error Check Data Register (SMB_Mem_PEC_io)—Offset 8h

This register contains the 8-bit CRC value that is used as the Packet Error Check on SMBus. For writes, this register is written by software prior to running the command. For reads, this register is read by software after the read command is completed on SMBus.

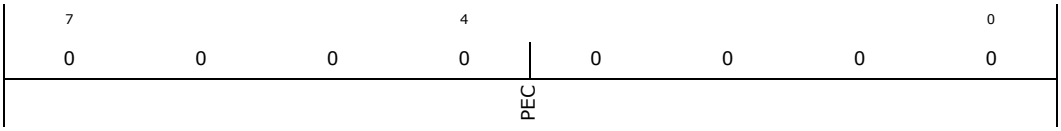
Access Method

Type: I/O Register (Size: 8 bits)

SMB_Mem_PEC_io: [IOBAR] + 8h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**PEC:** This 8-bit register is written with the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the IUS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.

23.8.9 Auxiliary Status (SMB_Mem_AUXS_io)—Offset Ch

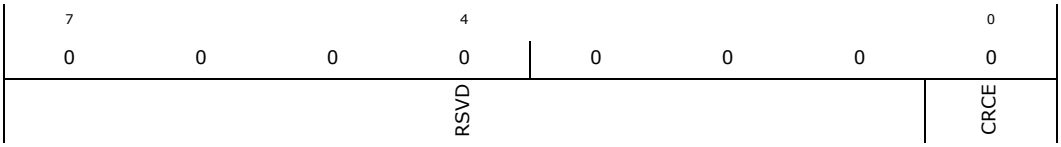
Access Method

Type: I/O Register (Size: 8 bits)

SMB_Mem_AUXS_io: [IOBAR] + Ch

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:1	0000000b RO	**Reserved (RSVD):** Reserved.
0	0b RW	**CRCE:** CRC Error (CRCE) - This bit is set if a received message contained a CRC error. When this bit is set, the DEVERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after SMBus controller has received the final data bit transmitted by external slave.

23.8.10 Auxiliary Control (SMB_Mem_AUXC_io)—Offset Dh

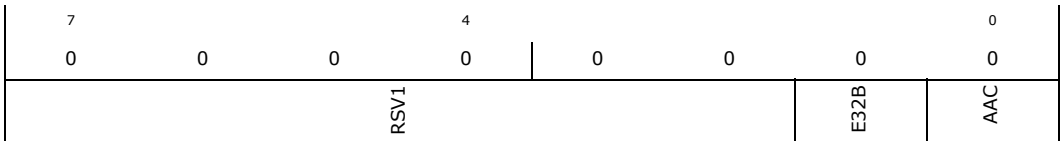
Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_AUXC_io: [IOBAR] + Dh

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:2	000000b RO	**Reserved (RSV1):** Reserved
1	0b RW	**E32B:** Enable 32-byte Buffer (E32B) - When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the controller generates an interrupt
0	0b RW/O	**AAC:** Automatically Append CRC (AAC) - When set, the SMBus controller will automatically append the CRC. This bit must not be changed during SM Bus transactions, or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

23.8.11 SMBUS_PIN_CTL Register (SMB_Mem_SMBC_io)—Offset Fh

Software bus accesses register

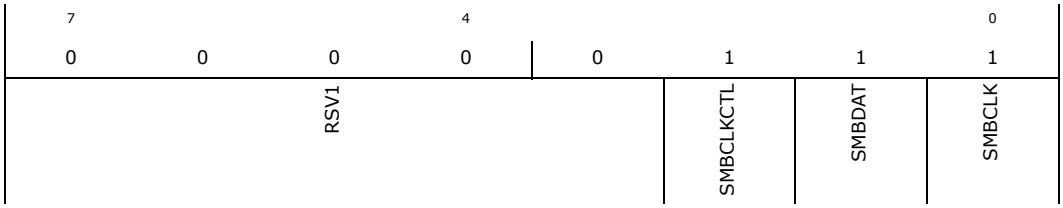
Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_SMBC_io: [IOBAR] + Fh

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 07h



Bit Range	Default & Access	Description
7:3	00000b RO	**Reserved (RSV1):** Reserved

Bit Range	Default & Access	Description
2	1b RW	**SMBCLKCTL:** This Read/Write bit has a default of 1. 0 = SMBus controller will drive the SMB_CLK pin low, independent of what the other SMB logic would otherwise indicate for the SMB_CLK pin. 1 = The SMB_CLK pin is Not overdriven low. The other SMBus logic controls the state of the pin.
1	1b RO	**SMBDAT:** This pin returns the value on the SMB_DATA pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.
0	1b RO	**SMBCLK:** This pin returns the value on the SMB_CLK pin. It will be 1 to indicate high, 0 to indicate low. This allows software to read the current state of the pin.

23.8.12 Slave Status Register (SMB_Mem_SSTS_io)—Offset 10h

All bits in this register are implemented in the 64 kHz clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally

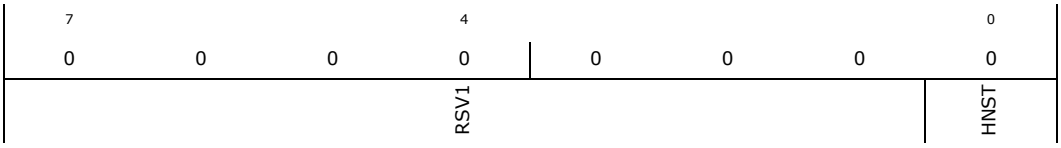
Access Method

Type: I/O Register (Size: 8 bits)

SMB_Mem_SSTS_io: [IOBAR] + 10h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:1	0000000b RO	**Reserved (RSV1):** Reserved
0	0b RW	**HNST:** HOST_NOTIFY_STS: The SMBus controller sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. Note that the SMBus controller will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the SMBus controller will NACK the first byte (host address) of any new 'Host Notify' commands on the SMBus. Writing a 0 to this bit has no effect.

23.8.13 Slave Command Register (SMB_Mem_SCMD_io)—Offset 11h

All bits in this register are implemented in a slow (64khz) clock domain. Therefore, software must poll the register until a write takes effect before assuming that a write has completed internally. Also, software must confirm the prior written value before writing to the register again.

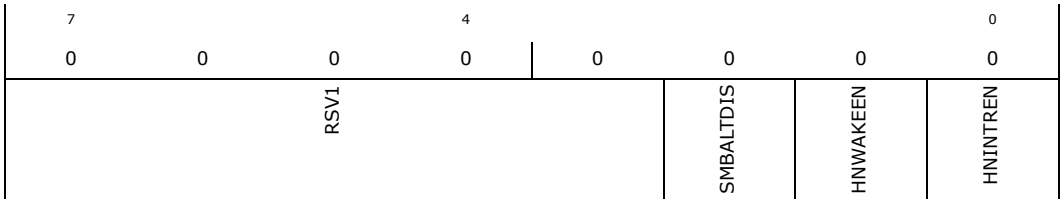
Access Method

Type: I/O Register (Size: 8 bits)

SMB_Mem_SCMD_io: [IOBAR] + 11h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:3	00000b RO	**Reserved (RSV1):** Reserved
2	0b RW	**SMBALTDIS:** Software sets this bit to 1 to block the generation of the interrupt or SMI# due to the SMB_ALERTB source. This bit is logically inverted and 'AND'ed with the SMB_ALERTB bit of HSTS register. The resulting signal is distributed to the SMI# and/or interrupt generation logic.
1	0b RW	**HNWAKEEN:** Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event.
0	0b RW	**HNINTREN:** Software sets this bit to 1 to enable the generation of interrupt or SMI when HOST_NOTIFY_STS is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either INTRB or SMI is generated, depending on the value of the SMI_EN bit (D31, F3, Off40h, B1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI) will be generated. The interrupt (or SMI) is logically generated by AND'ing the STS and INTREN bits.

23.8.14 Notify Device Address Register (SMB_Mem_NDA_io)—Offset 14h

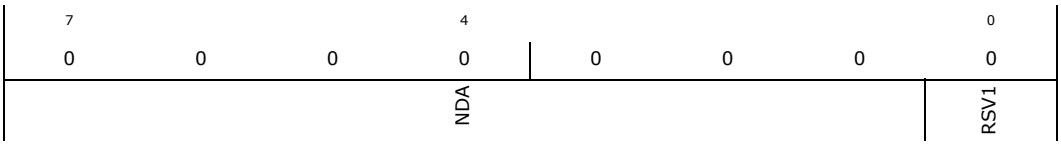
Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_NDA_io: [IOBAR] + 14h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:1	0000000b RO	**NDA:** DEVICE_ADDRESS - This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.
0	0b RO	**Reserved (RSV1):** Reserved

23.8.15 Notify Data Low Byte Register (SMB_Mem_NDLB_io)—Offset 16h

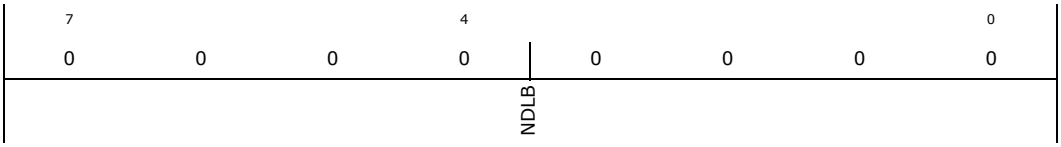
Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_NDLB_io: [IOBAR] + 16h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RO	**NDLB:** DATA_LOW_BYTE - This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

23.8.16 Notify Data High Byte Register (SMB_Mem_NDHB_io)—Offset 17h

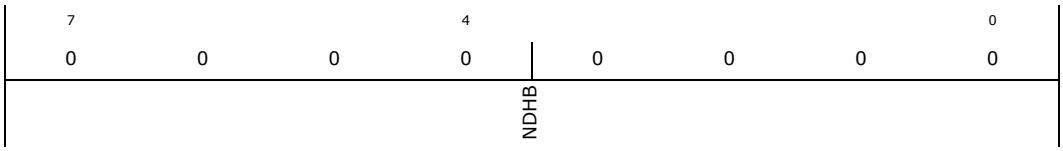
Access Method

Type: I/O Register
(Size: 8 bits)

SMB_Mem_NDHB_io: [IOBAR] + 17h

IOBAR Type: PCI Configuration Register (Size: 32 bits)
IOBAR Reference: [B:0, D:31, F:3] + 20h

Default: 00h



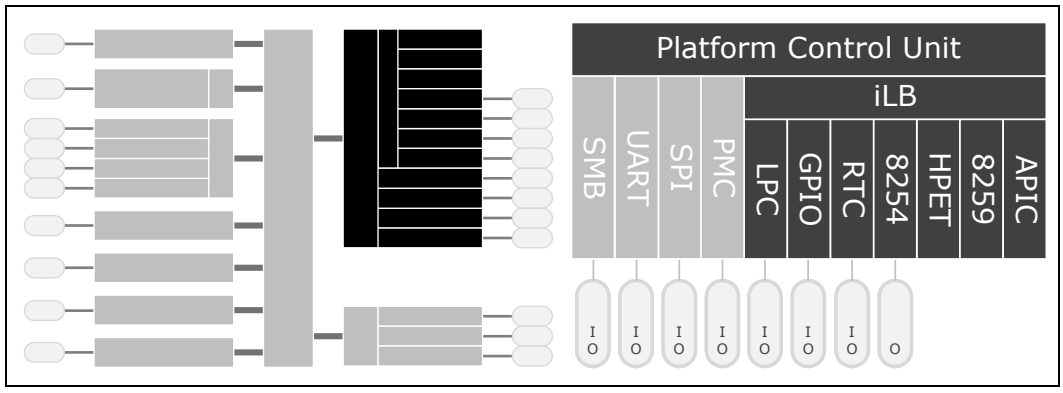
Bit Range	Default & Access	Description
7:0	00h RO	**NDHB:** DATA_HIGH_BYTE - This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit is set to 1.

24 PCU – Intel® Legacy Block (iLB) Overview

The Intel Legacy Block (iLB) is a collection of disparate functional blocks that are critical for implementing the legacy PC platform features. These blocks include:

- PCU – iLB – Low Pin Count (LPC) Bridge
- PCU – iLB – Real Time Clock (RTC)
- PCU – iLB – 8254 Timers
- PCU – iLB – High Precision Event Timer (HPET)
- PCU – iLB – GPIO
- PCU – iLB – IO APIC
- PCU – iLB – 8259 Programmable Interrupt Controllers (PIC)

The iLB also implements a register range for configuration of some of those blocks along with support for Non-Maskable Interrupts (NMI).



24.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details as well as the subsequent sections.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 173. iLB Signals

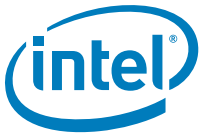
Signal Name	Direction/ Type	Description
ILB_NMI	I TBD	Non-Maskable Interrupt: This is an NMI event indication into the processor. *This signal is multiplexed and may be used by other functions.*

24.2 Features

24.2.1 Key Features

The key features of various blocks are as follows:

- LPC Interface
  - Supports Low Pin Count (LPC) 1.1 Specification
  - No support for DMA or bus mastering
  - Supports Trusted Platform Module (TPM) 1.2
- General Purpose Input Output
  - Legacy control interface for processor GPIOs
  - I/O mapped registers
- 8259 Programmable Interrupt Controller
  - Legacy interrupt support
  - 15 total interrupts through two cascaded controllers
  - I/O mapped registers
- I/O Advanced Programmable Interrupt Controller
  - Legacy-free interrupt support
  - 87 total interrupts
  - Memory mapped registers
- 8254
  - Legacy timer support
  - Three timers with fixed uses: System Timer, Refresh Request Signal and Speaker Tone
  - I/O mapped registers
- HPET - High Performance Event Timers
  - Legacy-free timer support
  - Three timers and one counter
  - Memory mapped registers
- Real-Time Clock (RTC)
  - 242 byte RAM backed by battery (also known as CMOS RAM)
  - Can generate wake/interrupt when time matches programmed value
  - I/O and indexed registers



24.2.2 Non-Maskable Interrupt

NMI support is enabled by setting the NMI Enable (NMI_EN) bit, at IO Port 70h, Bit 7, to 1b.

Non-Maskable Interrupts (NMIs) can be generated by several sources, as described in Table 174.

Table 174. NMI Sources

NMI Source	NMI Source Enabler/ Disabler	NMI Source Status	Alternate Configuration
SERR# goes active **NOTE:** A SERR# is only generated internally in the processor)	NSC.SNE	NSC.SNS	All NMI sources may, alternatively, generate a SMI by setting GNMI.NMI2SMIEN=1b The processor uses GNMI.NMI2SMIST for observing SMI status
IOCHK# goes active **NOTE:** A IOCHK# is only generated as a SERIRQ# frame	NSC.INE	NSC.INS	
ILB_NMI goes active **NOTE:** Active can be defined as being on the positive or negative edge of the signal using the GNMI.GNMIED register bit.	GNMI.GNMIED	GNMI.GNMIS	
Software sets the GNMI.NMIN register bit	GNMI.NMIN	GNMI.NMINS	

24.3 PCU iLB Interrupt Decode and Route

Table 175. Summary of PCU iLB Interrupt Decode and Route Memory Mapped I/O Registers—ILB_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"ACTL—Offset 0h" on page 1163	00000003h
4h	4	"MC—Offset 4h" on page 1164	00000000h
8h	1	"PIRQA—Offset 8h" on page 1165	80h
9h	1	"PIRQB—Offset 9h" on page 1165	80h
Ah	1	"PIRQC—Offset Ah" on page 1166	80h
Bh	1	"PIRQD—Offset Bh" on page 1167	80h
Ch	1	"PIRQE—Offset Ch" on page 1167	80h
Dh	1	"PIRQF—Offset Dh" on page 1168	80h
Eh	1	"PIRQG—Offset Eh" on page 1169	80h
Fh	1	"PIRQH—Offset Fh" on page 1169	80h
10h	4	"SCNT—Offset 10h" on page 1170	00000000h
14h	4	"KMC—Offset 14h" on page 1171	00000000h
18h	4	"FS—Offset 18h" on page 1172	00112233h
1Ch	4	"BC—Offset 1Ch" on page 1173	00000100h
20h	2	"IR0—Offset 20h" on page 1174	0000h
22h	2	"IR1—Offset 22h" on page 1174	0000h
24h	2	"IR2—Offset 24h" on page 1175	0000h
26h	2	"IR3—Offset 26h" on page 1176	0000h
28h	2	"IR4—Offset 28h" on page 1176	0000h
2Ah	2	"IR5—Offset 2Ah" on page 1177	0000h
2Ch	2	"IR6—Offset 2Ch" on page 1178	0000h
2Eh	2	"IR7—Offset 2Eh" on page 1178	0000h
30h	2	"IR8—Offset 30h" on page 1179	0000h
32h	2	"IR9—Offset 32h" on page 1180	0000h
34h	2	"IR10—Offset 34h" on page 1180	0000h
36h	2	"IR11—Offset 36h" on page 1181	0000h
38h	2	"IR12—Offset 38h" on page 1182	0000h
3Ah	2	"IR13—Offset 3Ah" on page 1182	0000h
3Ch	2	"IR14—Offset 3Ch" on page 1183	0000h
3Eh	2	"IR15—Offset 3Eh" on page 1184	0000h
40h	2	"IR16—Offset 40h" on page 1184	0000h
42h	2	"IR17—Offset 42h" on page 1185	0000h
44h	2	"IR18—Offset 44h" on page 1186	0000h
46h	2	"IR19—Offset 46h" on page 1186	0000h
48h	2	"IR20—Offset 48h" on page 1187	0000h

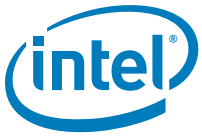


Table 175. Summary of PCU iLB Interrupt Decode and Route Memory Mapped I/O Registers—ILB_BASE_ADDRESS (Continued)

Offset	Size	Register ID—Description	Default Value
4Ah	2	"IR21—Offset 4Ah" on page 1188	0000h
4Ch	2	"IR22—Offset 4Ch" on page 1188	0000h
4Eh	2	"IR23—Offset 4Eh" on page 1189	0000h
50h	2	"IR24—Offset 50h" on page 1190	0000h
52h	2	"IR25—Offset 52h" on page 1190	0000h
54h	2	"IR26—Offset 54h" on page 1191	0000h
56h	2	"IR27—Offset 56h" on page 1192	0000h
58h	2	"IR28—Offset 58h" on page 1192	0000h
5Ah	2	"IR29—Offset 5Ah" on page 1193	0000h
5Ch	2	"IR30—Offset 5Ch" on page 1194	0000h
5Eh	2	"IR31—Offset 5Eh" on page 1194	0000h
60h	4	"OIC—Offset 60h" on page 1195	00001100h
64h	4	"RC—Offset 64h" on page 1196	00000000h
6Ch	4	"BCS - BIOS Control Status (BCS)—Offset 6Ch" on page 1196	00000002h
70h	4	"LE—Offset 70h" on page 1197	00000003h
80h	4	"NMI (GNMI)—Offset 80h" on page 1198	00000004h
84h	4	"LPCC—Offset 84h" on page 1199	00000001h
88h	4	"IRQEN (IRQE)—Offset 88h" on page 1200	00000000h

24.3.1 ACTL—Offset 0h

ACPI Control

Access Method

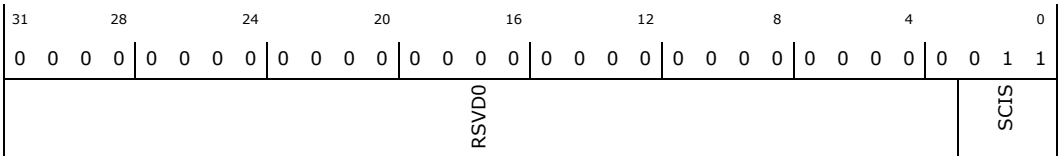
Type: Memory Mapped I/O Register (Size: 32 bits)

ACTL: [ILB_BASE_ADDRESS] + 0h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000003h



Bit Range	Default & Access	Description
31:3	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
2:0	011b RW	**SCIS:** SCI IRQ Select (SCIS): Specifies on which IRQ SCI will rout to. If not using APIC, SCI must be routed to IRQ9-11 , and that interrupt is not sharable with SERIRQ, but is shareable with other interrupts. If using APIC, SCI can be mapped to IRQ20-23, and can be shared with other interrupts. When the interrupt is mapped to APIC interrupts 9, 10 or 11, APIC must be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, APIC must be programmed for active-low reception.

24.3.2 MC—Offset 4h

Miscellaneous Control

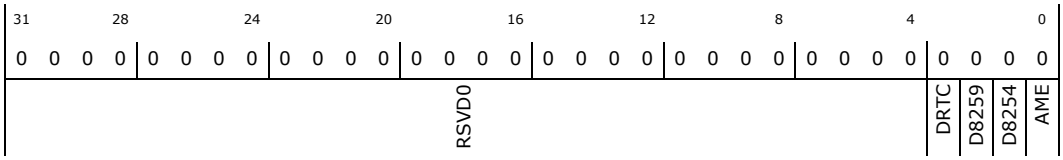
Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

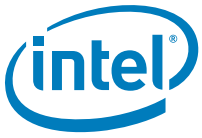
MC: [ILB_BASE_ADDRESS] + 4h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:4	0b RO	**RSVD0:** Reserved
3	0b RW	**DRTC:** Disable RTC (DRTC): When set, decodes to the RTC will be disabled, and the accesses instead will be sent to LPC. This allows testing to determine whether these functions are needed for XP and Vista 'EDS Note: Do not include this field in the EDS.
2	0b RW	**D8259:** Disable 8259 (D8259): When set, decodes to the 8259 will be disabled, and the accesses instead will be sent to LPC. This allows testing to determine whether these functions are needed for XP and Vista 'EDS Note: Do not include this field in the EDS.
1	0b RW	**D8254:** Disable 8254 (D8254): When set, decodes to the 8254 will be disabled, and the accesses instead will be sent to LPC. This allows testing to determine whether these functions are needed for XP and Vista 'EDS Note: Do not include this field in the EDS.
0	0b RW	**AME:** Alt Access Mode is a mode that enables host reading some WO registers . 1. Read 8254 (legacy timers) indirect WO registers 2. Read 8259 (legacy interrupt controller) indirect WO registers 3. Read port 0x70 - port 0x70 includes the RTC memory address [6:0] and the NMI enable bit [7]



24.3.3 PIRQA—Offset 8h

PIRQA Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQA: [ILB_BASE_ADDRESS] + 8h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

24.3.4 PIRQB—Offset 9h

PIRQB Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQB: [ILB_BASE_ADDRESS] + 9h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

24.3.5 PIRQC—Offset Ah

PIRQC Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQC: [ILB_BASE_ADDRESS] + Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

24.3.6 PIRQD—Offset Bh

PIRQD Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQD: [ILB_BASE_ADDRESS] + Bh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

24.3.7 PIRQE—Offset Ch

PIRQE Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQE: [ILB_BASE_ADDRESS] + Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

24.3.8 PIRQF—Offset Dh

PIRQF Routing Control

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQF: [ILB_BASE_ADDRESS] + Dh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h

7			4				0
1	0	0	0	0	0	0	0
REN	RSVD0			IR			

Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

24.3.9 PIRQG—Offset Eh

PIRQG Routing Control

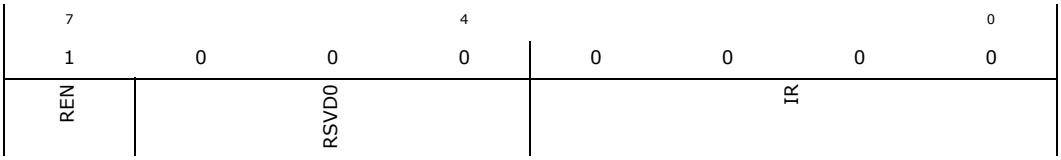
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQG: [ILB_BASE_ADDRESS] + Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h



Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

24.3.10 PIRQH—Offset Fh

PIRQH Routing Control

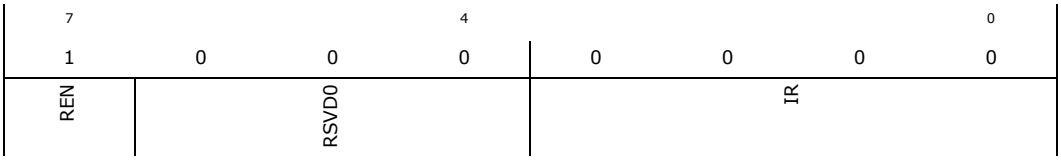
Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

PIRQH: [ILB_BASE_ADDRESS] + Fh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 80h



Bit Range	Default & Access	Description
7	1b RW	**REN:** Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.
6:4	0b RO	**RSVD0:** Reserved

Bit Range	Default & Access	Description
3:0	0b RW	**IR:** IRQ Routing (IR): Indicates how to route PIRQx Bits Mapping Bits Mapping 0h Reserved 8h Reserved 1h Reserved 9h IRQ9 2h Reserved Ah IRQ10 3h IRQ3 Bh IRQ11 4h IRQ4 Ch IRQ12 5h IRQ5 Dh Reserved 6h IRQ6 Eh IRQ14 7h IRQ7 Fh IRQ15

24.3.11 SCNT—Offset 10h

SCNT - Serial IRQ Control

Access Method

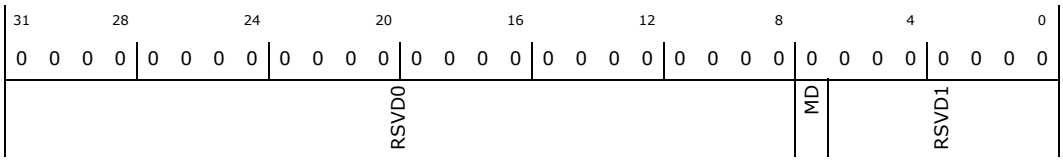
Type: Memory Mapped I/O Register (Size: 32 bits)

SCNT: [ILB_BASE_ADDRESS] + 10h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7	0b RW	**MD:** Mode (MD): When set, the SERIRQ is in continuous mode. When cleared, SERIRQ is in quiet mode. This bit must be set to guarantee that the first action of SERIRQ is a start frame.
6:0	0b RO	**RSVD1:** Reserved

24.3.12 KMC—Offset 14h

USB Legacy Keyboard/Mouse Control

Access Method

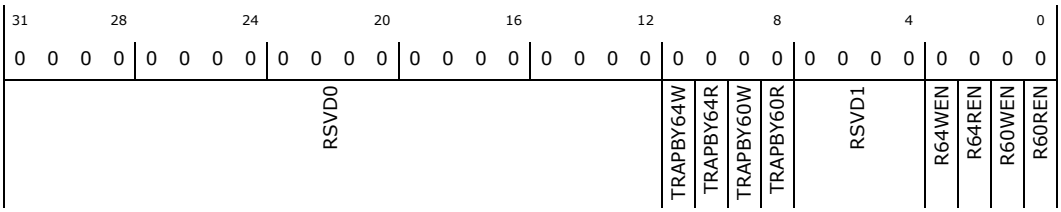
Type: Memory Mapped I/O Register (Size: 32 bits)

KMC: [ILB_BASE_ADDRESS] + 14h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:12	0b RO	**RSVD0:** Reserved
11	0b RW/1C	**TRAPBY64W:** TRAPBY64W - SMI Caused by Port 64 Write: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 3, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
10	0b RW/1C	**TRAPBY64R:** TRAPBY64R - SMI Caused by Port 64 Read: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 2, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
9	0b RW/1C	**TRAPBY60W:** TRAPBY60W - SMI Caused by Port 60 Write: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 1, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
8	0b RW/1C	**TRAPBY60R:** TRAPBY60R - SMI Caused by Port 60 Read: Indicates if the event occurred. Note that even if the corresponding enable bit is not set in the Bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. Writing a 1 to this bit will clear the latch.
7:4	0b RO	**RSVD1:** Reserved
3	0b RW	**R64WEN:** R64WEN - SMI on Port 64 Writes Enable: When set, a 1 in bit 11 will cause an SMI event.
2	0b RW	**R64REN:** R64REN - SMI on Port 64 Reads Enable: When set, a 1 in bit 10 will cause an SMI event.
1	0b RW	**R60WEN:** R60WEN - SMI on Port 60 Writes Enable: When set, a 1 in bit 9 will cause an SMI event.
0	0b RW	**R60REN:** R60REN - SMI on Port 60 Reads Enable: When set, a 1 in bit 8 will cause an SMI event.

24.3.13 FS—Offset 18h

FS - FWH ID Select

Access Method

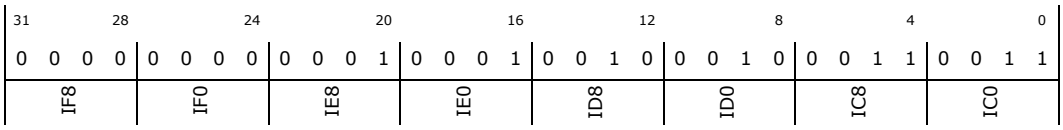
Type: Memory Mapped I/O Register (Size: 32 bits)

FS: [ILB_BASE_ADDRESS] + 18h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00112233h



Bit Range	Default & Access	Description
31:28	0h RO	**IF8:** F8-FF IDSEL (IF8): IDSEL to use in FWH cycle for range enabled by BDE.EF8. The Address ranges are: FFF80000h - FFFFFFFFh, FFB80000h - FFBFFFFFh and 000E0000h - 000FFFFFh
27:24	0h RW	**IF0:** F0-F7 IDSEL (IF0): IDSEL to use in FWH cycle for range enabled by BDE.EF0. The Address ranges are: FFF00000h - FFF7FFFFh, FFB00000h - FFB7FFFFh
23:20	1h RW	**IE8:** E8-EF IDSEL (IE8): IDSEL to use in FWH cycle for range enabled by BDE.EE8. The Address ranges are: FFE80000h - FFEFFFFFh, FFA80000h - FFAFFFFFh
19:16	1h RW	**IE0:** E0-E7 IDSEL (IE0): IDSEL to use in FWH cycle for range enabled by BDE.EE0. The Address ranges are: FFE00000h - FFE7FFFFh, FFA00000h - FFA7FFFFh
15:12	2h RW	**ID8:** D8-DF IDSEL (ID8): IDSEL to use in FWH cycle for range enabled by BDE.ED8. The Address ranges are: FFD80000h - FFDFFFFFh, FF980000h - FF9FFFFFh
11:8	2h RW	**ID0:** D0-D7 IDSEL (ID0): IDSEL to use in FWH cycle for range enabled by BDE.ED0. The Address ranges are: FFD00000h - FFD7FFFFh, FF900000h - FF97FFFFh
7:4	3h RW	**IC8:** C8-CF IDSEL (IC8): IDSEL to use in FWH cycle for range enabled by BDE.EC8. The Address ranges are: FFC80000h - FFCFFFFFh, FF880000h - FF8FFFFFh
3:0	3h RW	**IC0:** C0-C7 IDSEL (IC0): IDSEL to use in FWH cycle for range enabled by BDE.EC0. The Address ranges are: FFC00000h - FFC7FFFFh, FF800000h - FF87FFFFh

24.3.14 BC—Offset 1Ch

BC - BIOS Control

Access Method

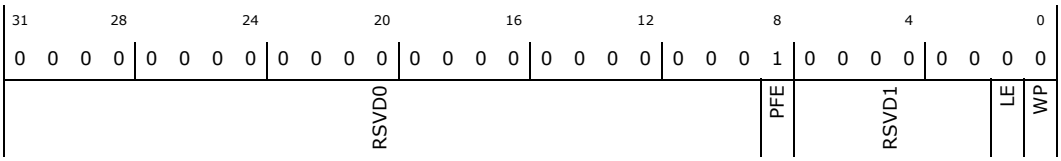
Type: Memory Mapped I/O Register (Size: 32 bits)

BC: [ILB_BASE_ADDRESS] + 1Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000100h



Bit Range	Default & Access	Description
31:9	0b RO	**RSVD0:** Reserved
8	1b RW	**PFE:** Prefetch Enable (PFE): When set, BIOS prefetching is enabled. An access to BIOS causes a 64-byte fetch of the line starting at that region. Subsequent accesses within that region result in data being returned from the prefetch buffer. The prefetch buffer is invalidated when this bit is cleared, or a BIOS access occurs to a different line than what is currently in the buffer.
7:2	0b RO	**RSVD1:** Reserved
1	0b RW	**LE:** Lock Enable (LE): When set, setting the WP bit will cause SMIs. When cleared, setting the WP bit will not cause SMIs. Once set, this bit can only be cleared by a PMU_PLTRST_B#.
0	0b RW	**WP:** Write Protect (WP): When set, access to BIOS is enabled for both read and write cycles. When cleared, only read cycles are permitted to BIOS. When written from a 0 to a 1 and LE is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

24.3.15 IR0—Offset 20h

IR0 - Interrupt Routing Device 0

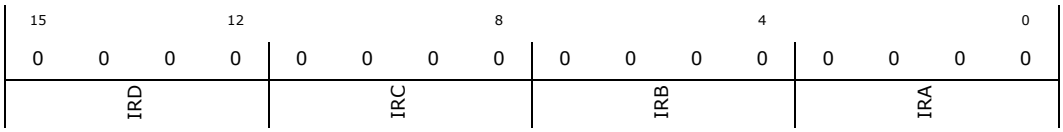
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR0: [ILB_BASE_ADDRESS] + 20h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.16 IR1—Offset 22h

IR1 - Interrupt Routing Device 1

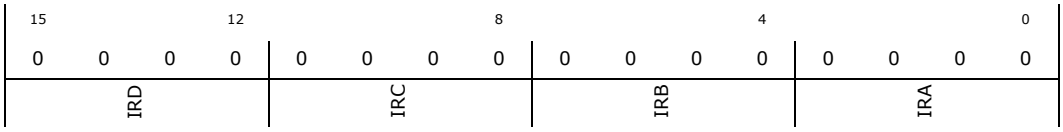
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR1: [ILB_BASE_ADDRESS] + 22h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.17 IR2—Offset 24h

IR2 - Interrupt Routing Device 2

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR2: [ILB_BASE_ADDRESS] + 24h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.18 IR3—Offset 26h

IR3 - Interrupt Routing Device 3

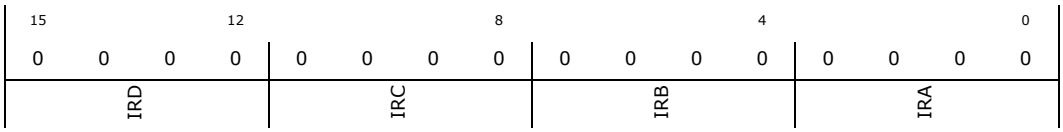
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR3: [ILB_BASE_ADDRESS] + 26h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.19 IR4—Offset 28h

IR4 - Interrupt Routing Device 4

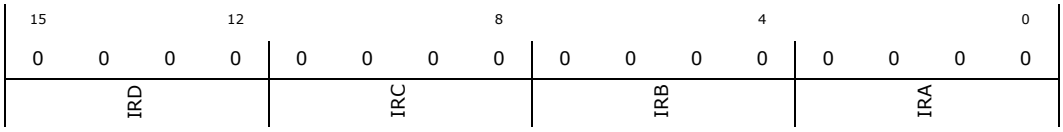
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR4: [ILB_BASE_ADDRESS] + 28h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.20 IR5—Offset 2Ah

IR5 - Interrupt Routing Device 5

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR5: [ILB_BASE_ADDRESS] + 2Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.21 IR6—Offset 2Ch

IR6 - Interrupt Routing Device 6

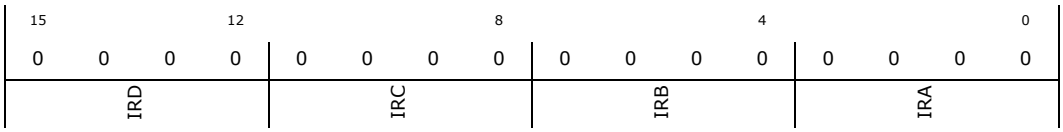
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR6: [ILB_BASE_ADDRESS] + 2Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.22 IR7—Offset 2Eh

IR7 - Interrupt Routing Device 7

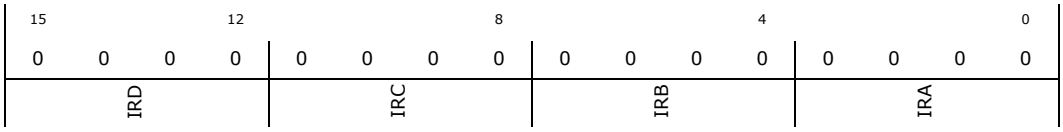
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR7: [ILB_BASE_ADDRESS] + 2Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.23 IR8—Offset 30h

IR8 - Interrupt Routing Device 8

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR8: [ILB_BASE_ADDRESS] + 30h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.24 IR9—Offset 32h

IR9 - Interrupt Routing Device 9

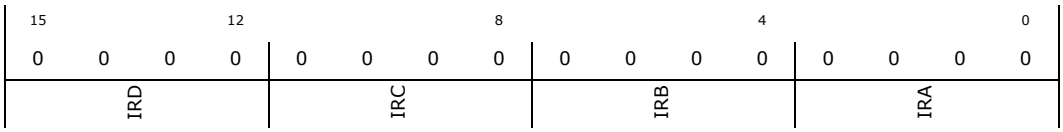
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR9: [ILB_BASE_ADDRESS] + 32h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.25 IR10—Offset 34h

IR10 - Interrupt Routing Device 10

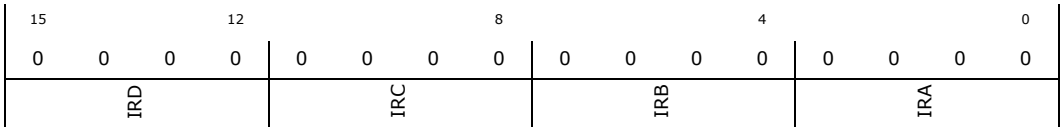
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR10: [ILB_BASE_ADDRESS] + 34h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.26 IR11—Offset 36h

IR11 - Interrupt Routing Device 11

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR11: [ILB_BASE_ADDRESS] + 36h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.27 IR12—Offset 38h

IR12 - Interrupt Routing Device 12

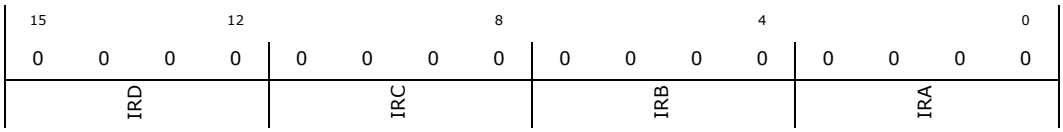
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR12: [ILB_BASE_ADDRESS] + 38h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.28 IR13—Offset 3Ah

IR13 - Interrupt Routing Device 13

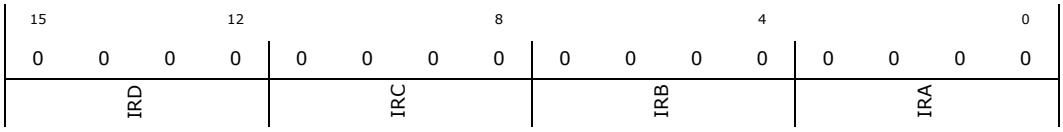
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR13: [ILB_BASE_ADDRESS] + 3Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.29 IR14—Offset 3Ch

IR14 - Interrupt Routing Device 14

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR14: [ILB_BASE_ADDRESS] + 3Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.30 IR15—Offset 3Eh

IR15 - Interrupt Routing Device 15

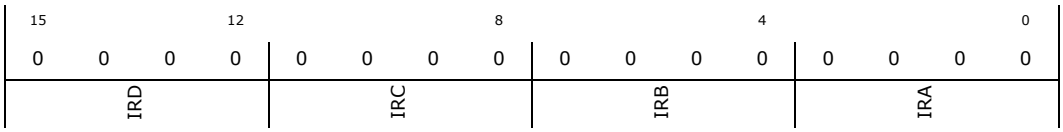
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR15: [ILB_BASE_ADDRESS] + 3Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.31 IR16—Offset 40h

IR16 - Interrupt Routing Device 16

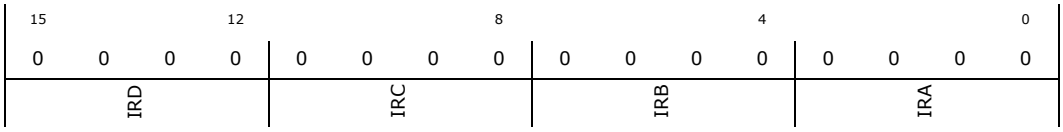
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR16: [ILB_BASE_ADDRESS] + 40h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.32 IR17—Offset 42h

IR17 - Interrupt Routing Device 17

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR17: [ILB_BASE_ADDRESS] + 42h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.33 IR18—Offset 44h

IR18 - Interrupt Routing Device 18

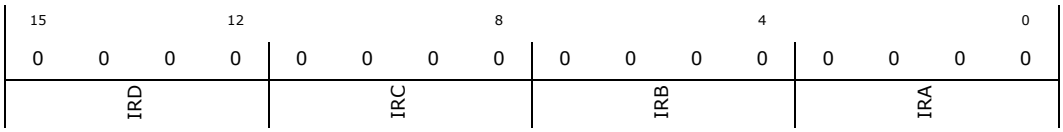
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR18: [ILB_BASE_ADDRESS] + 44h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.34 IR19—Offset 46h

IR19 - Interrupt Routing Device 19

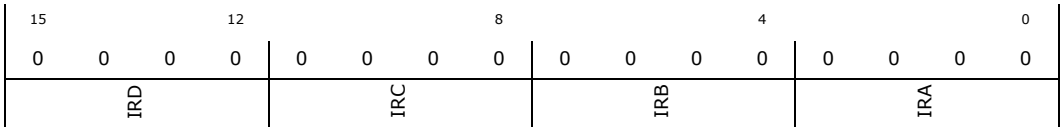
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR19: [ILB_BASE_ADDRESS] + 46h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.35 IR20—Offset 48h

IR20 - Interrupt Routing Device 20

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR20: [ILB_BASE_ADDRESS] + 48h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15			12				8				4				0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.36 IR21—Offset 4Ah

IR21 - Interrupt Routing Device 21

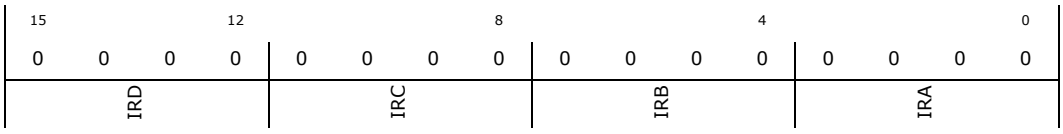
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR21: [ILB_BASE_ADDRESS] + 4Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.37 IR22—Offset 4Ch

IR22 - Interrupt Routing Device 22

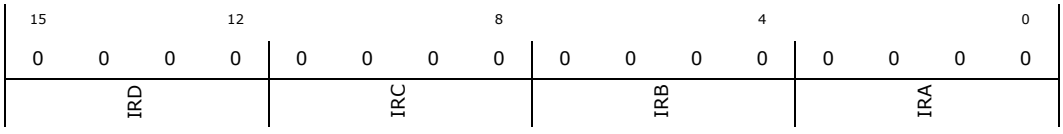
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR22: [ILB_BASE_ADDRESS] + 4Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.38 IR23—Offset 4Eh

IR23 - Interrupt Routing Device 23

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR23: [ILB_BASE_ADDRESS] + 4Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.39 IR24—Offset 50h

IR24 - Interrupt Routing Device 24

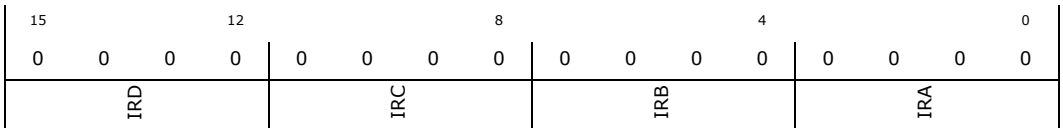
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR24: [ILB_BASE_ADDRESS] + 50h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.40 IR25—Offset 52h

IR25 - Interrupt Routing Device 25

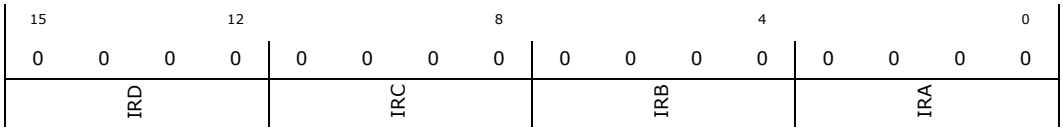
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR25: [ILB_BASE_ADDRESS] + 52h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.41 IR26—Offset 54h

IR26 - Interrupt Routing Device 26

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR26: [ILB_BASE_ADDRESS] + 54h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.42 IR27—Offset 56h

IR27 - Interrupt Routing Device 27

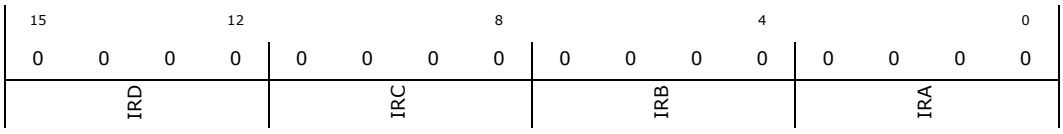
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR27: [ILB_BASE_ADDRESS] + 56h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.43 IR28—Offset 58h

IR28 - Interrupt Routing Device 28

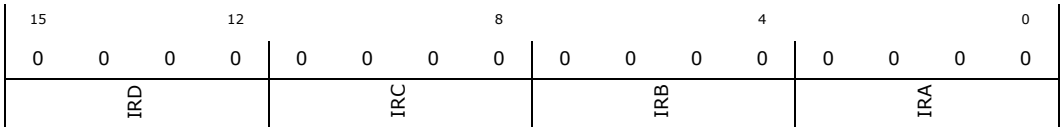
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR28: [ILB_BASE_ADDRESS] + 58h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.44 IR29—Offset 5Ah

IR29 - Interrupt Routing Device 29

Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR29: [ILB_BASE_ADDRESS] + 5Ah

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IRD				IRC				IRB				IRA			

Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.45 IR30—Offset 5Ch

IR30 - Interrupt Routing Device 30

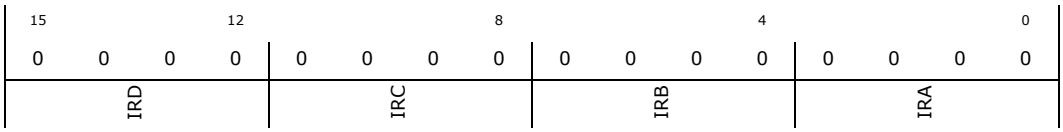
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR30: [ILB_BASE_ADDRESS] + 5Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.46 IR31—Offset 5Eh

IR31 - Interrupt Routing Device 31

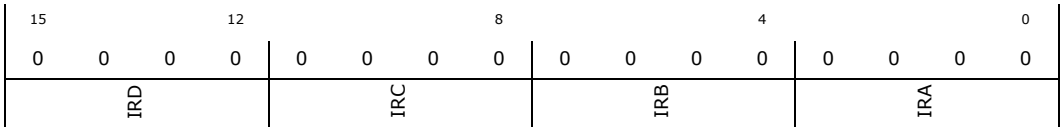
Access Method

Type: Memory Mapped I/O Register (Size: 16 bits)

IR31: [ILB_BASE_ADDRESS] + 5Eh

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)
ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 0000h



Bit Range	Default & Access	Description
15:12	4'd3 RW	**IRD:** INTD mapping to IRQ A-H
11:8	4'd2 RW	**IRC:** INTC mapping to IRQ A-H

Bit Range	Default & Access	Description
7:4	4'd1 RW	**IRB:** INTB mapping to IRQ A-H
3:0	4'd0 RW	**IRA:** INTA mapping to IRQ A-H

24.3.47 OIC—Offset 60h

Other Interrupt Control

Access Method

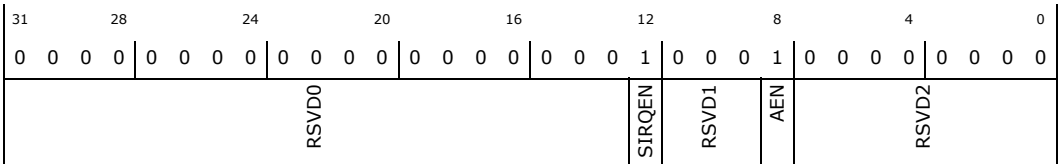
Type: Memory Mapped I/O Register (Size: 32 bits)

OIC: [ILB_BASE_ADDRESS] + 60h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00001100h



Bit Range	Default & Access	Description
31:13	0b RO	**RSVD0:** Reserved
12	1b RW	**SIRQEN:** When set, enables the internal SIRQ . when cleared the internal sIRQ is disabled
11:9	0b RO	**RSVD1:** Reserved
8	1b RW	**AEN:** When set, enables the internal IOAPIC and its address decode, when cleared the internal IOxAPIC is disabled. software should read this register after modifying the APIC enable prior to acces to IOxAPIC addresss range.
7:0	0b RO	**RSVD2:** Reserved

24.3.48 RC—Offset 64h

RC - RTC Configuration

Access Method

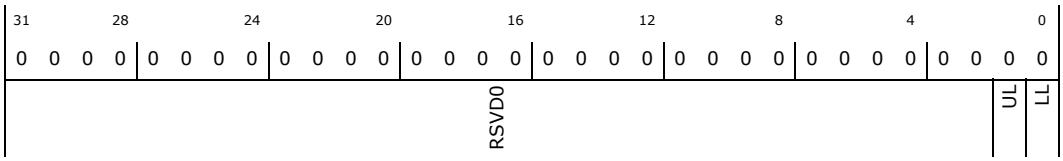
Type: Memory Mapped I/O Register (Size: 32 bits)

RC: [ILB_BASE_ADDRESS] + 64h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	0b RW/L	**UL:** Upper 128 Byte Lock (UL): When set, bytes 38h-3Fh in the upper 128 byte bank of RTC RAM are locked. Writes will be dropped and reads will not return any guaranteed data.
0	0b RW/L	**LL:** Lower 128 Byte Lock (LL): When set, bytes 38h-3Fh in the lower 128 byte bank of RTC RAM are locked. Writes will be dropped and reads will not return any guaranteed data.

24.3.49 BCS - BIOS Control Status (BCS)—Offset 6Ch

Access Method

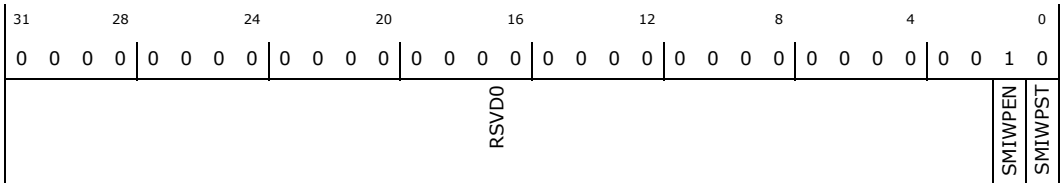
Type: Memory Mapped I/O Register (Size: 32 bits)

BCS: [ILB_BASE_ADDRESS] + 6Ch

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000002h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	1b RW	**SMIWPEN:** SMI WP Enable (SMIWPEN): When this bit is set to a 1, it enables the LPC to generate SMI upon not SMM code is trying to set BC.WP from a 0 to a 1 while BC.LE is set.

Bit Range	Default & Access	Description
0	0b RW/1C	**SMIWPST:** SMI WP Status (SMIWPST): Set when SMI is generated upon trying to set BC.WP from a 0 to a 1 by not SMM code (while BC.LE and SMIWPEN are set). Write a 1 to this bit should clear it and clear the SMI (send DEASSERT_SMI)

24.3.50 LE—Offset 70h

Access Method

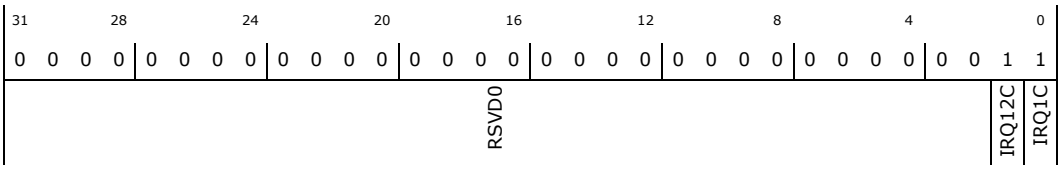
Type: Memory Mapped I/O Register (Size: 32 bits)

LE: [ILB_BASE_ADDRESS] + 70h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000003h



Bit Range	Default & Access	Description
31:2	0b RO	**RSVD0:** Reserved
1	1b RW	**IRQ12_CAUSE (IRQ12C):** When software sets the bit to 1, IRQ12 will be high (asserted), When software set bit to 0,IRQ12 will be low (deasserted). default for this bit is 1
0	1b RW	**IRQ1_CAUSE (IRQ1C):** When software sets the bit to 1, IRQ11 will be high (asserted), When software set bit to 0,IRQ1 will be low (deasserted). default for this bit is 1

24.3.51 NMI (GNMI)—Offset 80h

NMI register

Access Method

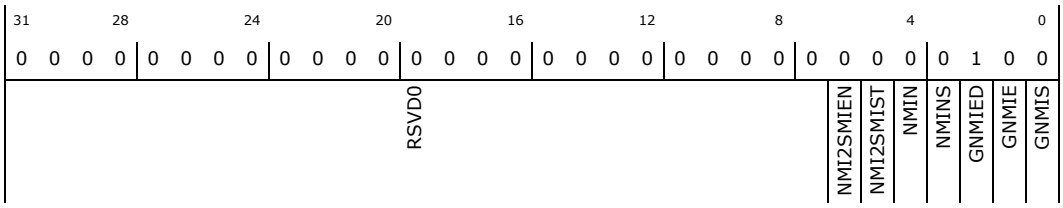
Type: Memory Mapped I/O Register (Size: 32 bits)

GNMI: [ILB_BASE_ADDRESS] + 80h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000004h



Bit Range	Default & Access	Description
31:7	0b RO	**RSVD0:** Reserved
6	0b RW	**NMI2SMIEN:** NMI to SMI Enable (NMI2SMIEN): When set, instead of NMI messgae SMI message will be sent.
5	0b RO	**NMI2SMIST:** NMI to SMI bit Status (NMI2SMIST)
4	0b RW/1C	**NMIN:** NMI NOW (NMIN): When set, NMI messgae will be sent. Writing 1'b1 to NMI_NOW inverts NMI_MOW and NMI_NOW_STS value
3	0b RO	**NMINS:** NMI_NOW_STS is a result of the NMI_NOW configuration bit. Writing 1'b1 to NMI_NOW inverts NMI_NOW_STS value. Resulting that the first time NMI_NOW is written sets the NMI_NOW_STS and initiates NMI. Next writing clears the NMI_NOW_STS and allows initiating NMI by the next writing to NMI_NOW
2	1b RW	**GNMIED:** GPIO NMI Edge Detction (GNMIED): When set, NMI messgae will be sent on NMI GPIO posedge. when cleared the NMI message will be sent on negedge
1	0b RW	**GNMIE:** GPIO NMI Enable (GNMIE): When set, NMI messgae will be sent when NMI GPIO occured. when cleared the message will not be sent
0	0b RW/1C	**GNMS (GNMIS):** GPIO NMI Status (GNMIS), when NMI is recieved from GPIO this bit is set. write '1' to this register to clear the status bit

24.3.52 LPCC—Offset 84h

LPC Control register

Access Method

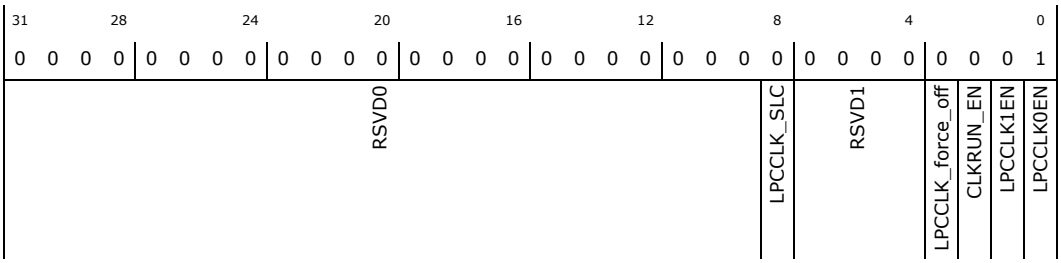
Type: Memory Mapped I/O Register (Size: 32 bits)

LPCC: [ILB_BASE_ADDRESS] + 84h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000001h



Bit Range	Default & Access	Description
31:9	0b RO	**RSVD0:** Reserved
8	0b RO	**LPCCLK_SLC:** iLPCCLK multiplex select (0 - ilpcclk0, 1 ilpcclk1)This bit get value from soft strap.
7:4	0b RO	**RSVD1:** Reserved
3	0b RW	**LPCCLK_force_off:** when asserted,oLPCCLK shut off similarly to CLKRUN protocol while ignoring iCLKRUN (LPC device reactions)
2	0b RW	**CLKRUN_EN:** LPC CLKRUN protocol enable (when not asserted, oLPCCLK toggles)
1	0b RO	**LPCCLK1EN:** Clock 1 Enable (EN): This bit get value from soft strap. When set, LPC clock 1 is enabled. When cleared, it is disabled.
0	1b RO	**LPCCLK0EN:** Clock 0 Enable (EN): When set, LPC clock 0 is enabled. When cleared, it is disabled.

24.3.53 IRQEN (IRQE)—Offset 88h

IRQ Enable Control

Access Method

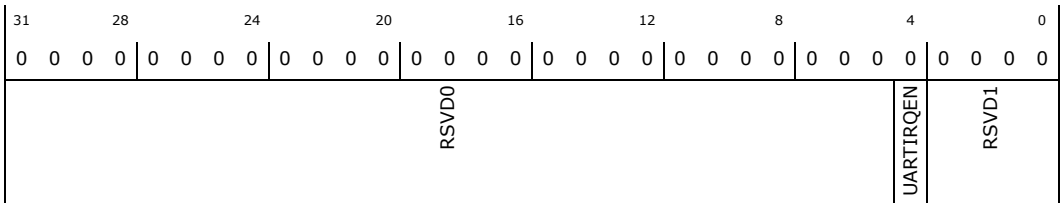
Type: Memory Mapped I/O Register (Size: 32 bits)

IRQE: [ILB_BASE_ADDRESS] + 88h

ILB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + 50h

Default: 00000000h

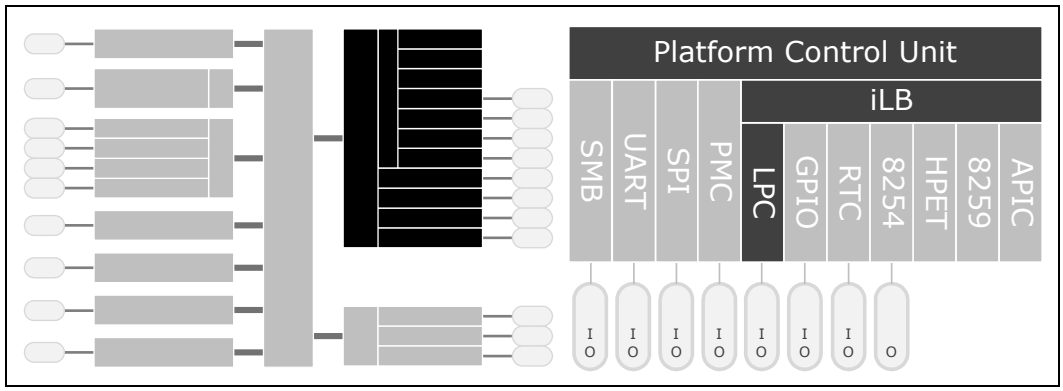


Bit Range	Default & Access	Description
31:5	0b RO	**RSVD0:** Reserved
4	0b RO	**UARTIRQEN:** UART IRQ4 Enable
3:0	0b RO	**RSVD1:** Reserved

25 PCU – iLB – Low Pin Count (LPC) Bridge

The processor implements an LPC Interface as described in the LPC 1.1 Specification. The Low Pin Count (LPC) bridge function of the processor resides in PCI Device 31, Function 0.

Note: In addition to the LPC bridge interface function, D31:F0 contains other functional units including interrupt controllers, timers, power management, system management, GPIO, and RTC.



25.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 176. LPC Signals

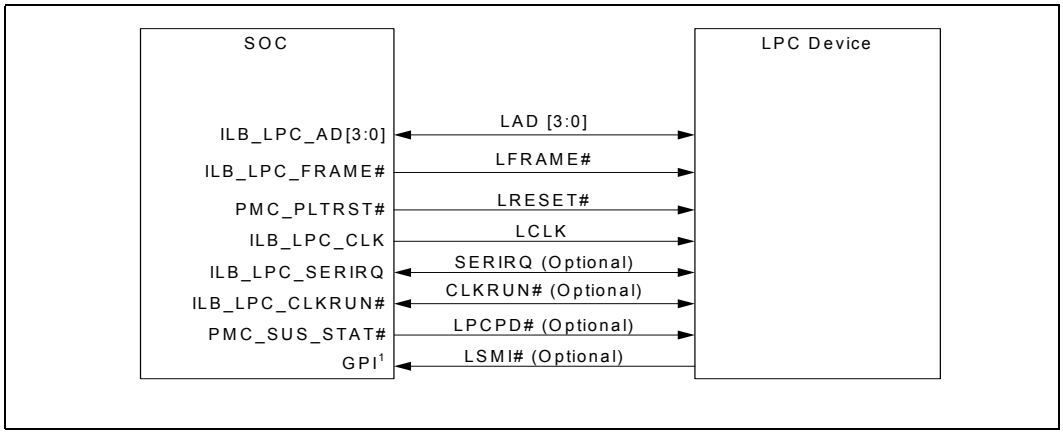
Signal Name	Direction/ Type	Description
ILB_LPC_AD[3:0]	I/O CMOS3.3/1.8	**LPC Multiplexed Command, Address, Data:** Internal pull-ups are provided for these signals. *These signals are multiplexed and may be used by other functions.*
ILB_LPC_CLK[0]	O CMOS3.3/1.8	**LPC Clock [0] Out:** 25 MHz PCI-like clock driven to LPC peripherals. *These signals are multiplexed and may be used by other functions.*
ILB_LPC_CLK[1]	O or I CMOS3.3/1.8	**LPC Clock [1] Out:** 25 MHz PCI-like clock driven to LPC peripherals. Can be configured as an input to compensate for board routing delays through Soft Strap. *These signals are multiplexed and may be used by other functions.*
ILB_LPC_CLKRUN#	I/OD CMOS3.3/1.8	**LPC Clock Run:** Input to determine the status of ILB_LPC_CLK and an open drain output used to request starting or speeding up ILB_LPC_CLK. This is a sustained tri-state signal used by the central resource to request permission to stop or slow ILB_LPC_CLK. The central resource is responsible for maintaining the signal in the asserted state when ILB_LPC_CLK is running and deasserts the signal to request permission to stop or slow ILB_LPC_CLK. An internal pull-up is provided for this signal. *This signal is multiplexed and may be used by other functions.*
ILB_LPC_FRAME#	O CMOS3.3/1.8	**LPC Frame:** This signal indicates the start of an LPC cycle, or an abort. *This signal is multiplexed and may be used by other functions.*
ILB_LPC_SERIRQ	I/O CMOS1.8	**Serial Interrupt Request:** This signal implements the serial interrupt protocol. *This signal is multiplexed and may be used by other functions.*

25.2 Features

The LPC interface to the processor is shown in Figure 33. Note that the processor implements all of the signals that are shown as optional, but peripherals are not required to do so.

Note: The LPC controller does not implement bus mastering cycles or DMA.

Figure 33. LPC Interface Diagram



NOTES:
1. The General Purpose Input (GPI) must use a SMI capable GPIO: GPIO_S0_SC[7:0].

25.2.1 Memory Cycle Notes

For cycles below 16M, the LPC Controller will perform standard LPC memory cycles. For cycles targeting firmware (BIOS/EFI code only), firmware memory cycles are used. Only 8-bit transfers are performed. If a larger transfer appears, the LPC controller will break it into multiple 8-bit transfers until the request is satisfied.

If the cycle is not claimed by any peripheral (and subsequently aborted), the LPC Controller will return a value of all 1s to the CPU.

25.2.2 Trusted Platform Module (TPM) 1.2 Support

The LPC interface supports accessing Trusted Platform Module (TPM) 1.2 devices using the LPC TPM START encoding. Memory addresses within the range FED00000h to FED40FFFh will be accepted by the LPC Bridge and sent on LPC as TPM special cycles. No additional checking of the memory cycle is performed.

Note: This is different to the FED00000h to FED4BFFFh range implemented on some other Intel components since no Intel® Trusted Execution Technology (Intel® TXT) transactions are supported.

25.2.3 FWH Cycle Notes

If the LPC controller receives any SYNC returned from the device other than short (0101), long wait (0110), or ready (0000) when running a FWH cycle, indeterminate results may occur. A FWH device is not allowed to assert an Error SYNC.

BIOS/EFI boot from LPC is not supported when Secure Boot is enabled.

25.2.4 Other Notes

All cycles that are not decoded internally, and are not targeted for LPC (that is, configuration cycles, IO cycles above 64KB, and memory cycles above 16MB) will be sent to LPC with ILB_LPC_FRAME# not asserted.

25.2.5 POST Code Redirection

Writes to addresses 80h – 8Fh in IO register space will also be passed to the LPC bus.

Note: Reads of these addresses do not result in any LPC transactions.

25.2.6 Power Management

25.2.6.1 LPCPD# Protocol

Same timings as for PMC_SUS_STAT#. After driving PMC_SUS_STAT# active, the processor drives ILB_LPC_FRAME# low, and tri-states (or drives low) ILB_LPC_AD[3:0].

Note: The Low Pin Count Interface Specification, Revision 1.1 defines the LPCPD# protocol where there is at least 30 µs from LPCPD# assertion to LRST# assertion. This specification explicitly states that this protocol only applies to entry/exit of low-power states which does not include asynchronous reset events. The processor asserts both PMC_SUS_STAT# (connects to LPCPD#) and ILB_PLTRST# (connects to LRST#) at the same time during a global reset. This is not inconsistent with the LPC LPCPD# protocol.

25.2.6.2 Clock Run (CLKRUN)

When there are no pending LPC cycles, and SERIRQ is in quiet mode, the processor can shut down the LPC clock. The processor indicates that the LPC clock is going to shut down by de-asserting the ILB_LPC_CLKRUN# signal. LPC devices that require the clock to stay running should drive ILB_LPC_CLKRUN# low within 4 clocks of its de-assertion. If no device drives the signal low within 4 clocks, the LPC clock will stop. If a device asserts ILB_LPC_CLKRUN#, the processor will start the LPC clock and assert ILB_LPC_CLKRUN#.

Note: The CLKRUN protocol is disabled by default. See Section 25.3.2.2, "Clock Run Enable" for further details.

25.2.7 Serialized IRQ (SERIRQ)

25.2.7.1 Overview

The interrupt controller supports a serial IRQ scheme. The signal used to transmit this information is shared between the interrupt controller and all peripherals that support serial interrupts. The signal line, ILB_LPC_SERIRQ, is synchronous to LPC clock, and follows the sustained tri-state protocol that is used by LPC signals. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase:** Signal driven low
- **R – Recovery Phase:** Signal driven high
- **T – Turn-around Phase:** Signal released

The interrupt controller supports 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. Serial interrupt information is transferred using three types of frames:

- Start Frame: ILB_LPC_SERIRQ line driven low by the interrupt controller to indicate the start of IRQ transmission
- Data Frames: IRQ information transmitted by peripherals. The interrupt controller supports 21 data frames.
- Stop Frame: ILB_LPC_SERIRQ line driven low by the interrupt controller to indicate end of transmission and next mode of operation.

25.2.7.2 Start Frame

The serial IRQ protocol has two modes of operation which affect the start frame:

- Continuous Mode: The interrupt controller is solely responsible for generating the start frame
- Quiet Mode: Peripheral initiates the start frame, and the interrupt controller completes it.

These modes are entered using the length of the stop frame.

Continuous mode must be entered first, to start the first frame. This start frame width is 8 LPC clocks. This is a polling mode.

In Quiet mode, the ILB_LPC_SERIRQ line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives ILB_LPC_SERIRQ low. The interrupt controller senses the line low and drives it low for the remainder of the Start Frame. Since the first LPC clock of the start frame was driven by the peripheral, the interrupt controller drives ILB_LPC_SERIRQ low for 1 LPC clock less than in continuous mode. This mode of operation allows for lower power operation.

25.2.7.3 Data Frames

Once the Start frame has been initiated, the ILB_LPC_SERIRQ peripherals start counting frames based on the rising edge of ILB_LPC_SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each:

- **Sample Phase:** During this phase, a device drives ILB_LPC_SERIRQ low if its corresponding interrupt signal is low. If its corresponding interrupt is high, then the ILB_LPC_SERIRQ devices tri-state ILB_LPC_SERIRQ. ILB_LPC_SERIRQ remains high due to pull-up resistors.
- **Recovery Phase:** During this phase, a device drives ILB_LPC_SERIRQ high if it was driven low during the Sample Phase. If it was not driven during the sample phase, it remains tri-stated in this phase.
- **Turn-around Phase:** The device tri-states ILB_LPC_SERIRQ.

25.2.7.4 Stop Frame

After the data frames, a Stop Frame will be driven by the interrupt controller. ILB_LPC_SERIRQ will be driven low for two or three LPC clocks. The number of clocks is determined by the SCNT.MD register bit. The number of clocks determines the next mode, as indicated in Table 177.

Table 177. SERIRQ, Stop Frame Width to Operation Mode Mapping

Stop Frame Width	Next Mode
Two LPC clocks	**Quiet Mode:** Any SERIRQ device initiates a Start Frame
Three LPC clocks	**Continuous Mode:** Only the interrupt controller initiates a Start Frame

25.2.7.5 Serial Interrupts Not Supported

There are four interrupts on the serial stream which are not supported by the interrupt controller. These interrupts are:

- IRQ0: Heartbeat interrupt generated off of the internal 8254 counter 0.
- IRQ8: RTC interrupt can only be generated internally.
- IRQ13: This interrupt (floating point error) is not supported.
- IRQ14: Interrupt can only be generated by the SATA controller in Legacy mode.

The interrupt controller will ignore the state of these interrupts in the stream.

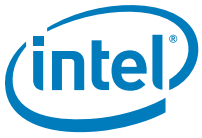
25.2.7.6 Data Frame Format and Issues

The following table shows the format of the data frames. The decoded INT[A:D]# values are ANDed with the corresponding PCI-express input signals (PIRQ[A:D]#). This way, the interrupt can be shared.

The other interrupts decoded via SERIRQ are also ANDed with the corresponding internal interrupts. For example, if IRQ10 is set to be used as the SCI, then it is ANDed with the decoded value for IRQ10 from the SERIRQ stream.

Table 178. SERIRQ Interrupt Mapping

Data Frame #	Interrupt	Clocks Past Start Frame	Comment
1	IRQ0	2	Ignored. Can only be generated via the internal 8524
2	IRQ1	5	Before port 60h latch
3	SMI#	8	Causes SMI# if low. Sets SMI_STS.ILB_SMI_STS register bit.
4	IRQ3	11	
5	IRQ4	14	
6	IRQ5	17	
7	IRQ6	20	
8	IRQ7	23	
9	IRQ8	26	Ignored. IRQ8# can only be generated internally
10	IRQ9	29	
11	IRQ10	32	
12	IRQ11	35	
13	IRQ12	38	Before port 60h latch
14	IRQ13	41	Ignored.
15	IRQ14	44	Ignored
16	IRQ15	47	
17	IOCHCK#	50	Same as ISA IOCHCK# going active.
18	PCI INTA#	53	
19	PCI INTB#	56	
20	PCI INTC#	59	
21	PCI INTD#	62	



25.3 Use

25.3.1 LPC Clock Delay Compensation

In order to meet LPC interface AC timing requirements, a LPC clock loop back is required. The operation of this loop back can be configured in two ways:

1. On the processor: In this configuration, ILB_LPC_CLK[0] is looped back on itself on the processor pad.

   a. Benefit:

   ILB_LPC_CLK[0] and ILB_LPC_CLK[1] are both available for system clocking

   b. Drawback:

   Clock delay compensation is less effective at compensating for mainboard delay

   c. Soft Strap & Register Requirements:

   Soft Strap LPCCLK_SLC = 0b

   Configuration is reflected by register bit LPCC.LPCCLK_SLC=0b

   Soft Strap LPCCLK1_ENB = 0b (ILB_LPC_CLK[1] disabled) or 1b (ILB_LPC_CLK[1] enabled)

2. Configuration is reflected by register bit LPCC.LPCCLK1EN=0b (ILB_LPC_CLK[1] disabled) or 1b (ILB_LPC_CLK[1] enabled)

3. On the main board: In this configuration, ILB_LPC_CLK[0] is looped back to ILB_LPC_CLK[1] on the main board.

   a. Benefit:

   Clock delay compensating in more effective at compensating for main board delay

   b. Drawback:

   Only ILB_LPC_CLK[0] is available for system clocking. ILB_LPC_CLK[1] must be disabled.

   c. Soft Strap & Register Requirements:

   Soft Strap LPCCLK_SLC = 1b

   Configuration is reflected by register bit LPCC.LPCCLK_SLC=1b

   Soft Strap LPCCLK1_ENB = 0b (ILB_LPC_CLK[1] disabled)

   Configuration is reflected by register bit LPCC.LPCCLK1EN=0b

25.3.2 LPC Power Management

25.3.2.1 Clock Enabling

The LPC clocks can be enabled or disabled by setting or clearing, respectively, the LPCC.LPCCLK[1:0]EN bits.

25.3.2.2 Clock Run Enable

The Clock Run protocol is disabled by default and should only be enabled during operating system run-time, once all LPC devices have been initialized. The Clock Run protocol is enabled by setting the LPCC.CLKRUN_EN register bit.

25.3.3 SERIRQ Disable

Serialized IRQ support may be disabled by setting the OIC.SIRQEN bit to 0b.

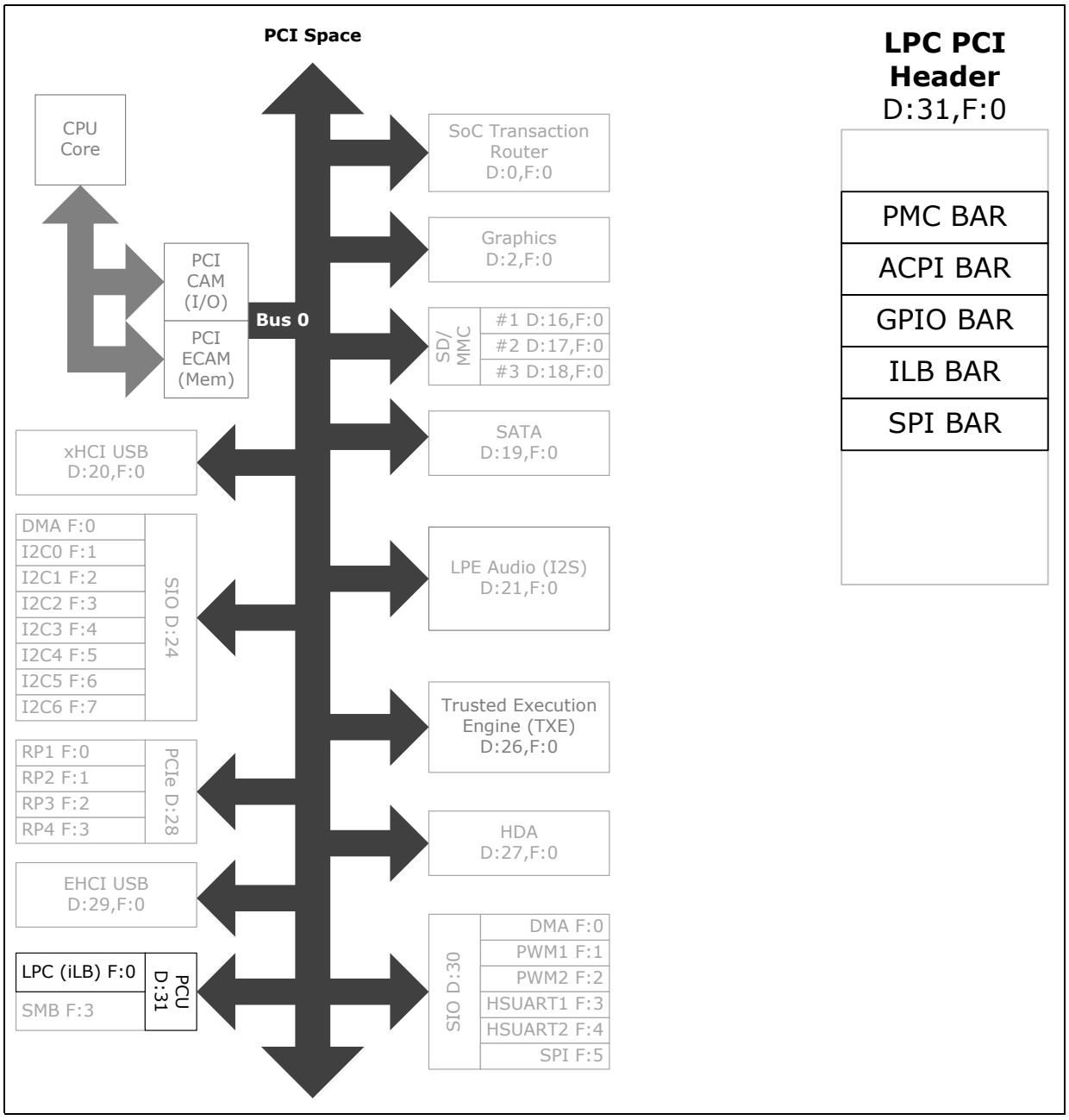
25.4 References

- Low Pin Count Interface Specification, Revision 1.1 (LPC): http://www.intel.com/design/chipsets/industry/lpc.htm
- Serialized IRQ Support for PCI Systems, Revision 6.0: http://www.smsc.com/media/Downloads_Public/papers/serirq60.doc
- Implementing Industry Standard Architecture (ISA) with Intel® Express Chipsets (318244): http://www.intel.com/assets/pdf/whitepaper/318244.pdf

25.5 Register Map

Refer to Chapter 3, "Register Access Methods" and Chapter 4, "Mapping Address Spaces" for additional information.

Figure 34. PCU - iLB - LPC Register Map



25.6 PCU iLB Low Pin Count (LPC) Bridge PCI Configuration Registers

Table 179. Summary of PCU iLB Low Pin Count (LPC) Bridge PCI Configuration Registers—0/31/0

Offset	Size	Register ID—Description	Default Value
0h	4	"Identifiers Register (PCIE_REG_Identifiers)—Offset 0h" on page 1211	00008086h
4h	2	"Command (PCIE_REG_COMMAND)—Offset 4h" on page 1211	0007h
6h	2	"Status (PCIE_REG_STATUS)—Offset 6h" on page 1212	0210h
8h	4	"Revision ID and Class Code (PCIE_REG_REVISION_ID_CLASS_CODE)—Offset 8h" on page 1214	06010000h
Dh	1	"Master Latency Timer (PCIE_REG_MASTER_LAT_TIMER)—Offset Dh" on page 1215	00h
Eh	1	"Header Type (PCIE_REG_HEADER_TYPE)—Offset Eh" on page 1215	80h
2Ch	4	"Subsystem ID and Vendor ID (PCIE_REG_SUBSYS_VENDOR_ID)—Offset 2Ch" on page 1216	00000000h
34h	4	"Capability List Pointer (PCIE_REG_CAP_POINTER)—Offset 34h" on page 1217	000000E0h
40h	4	"ABASE (ACPI_BASE_ADDRESS)—Offset 40h" on page 1217	00000001h
44h	4	"PBASE (PMC_BASE_ADDRESS)—Offset 44h" on page 1218	00000000h
48h	4	"GBASE (GPIO_BASE_ADDRESS)—Offset 48h" on page 1219	00000001h
4Ch	4	"IOBASE (IO_CONTROLLER_BASE_ADDRESS)—Offset 4Ch" on page 1220	00000000h
50h	4	"IBASE (ILB_BASE_ADDRESS)—Offset 50h" on page 1221	00000000h
54h	4	"SBASE (SPI_BASE_ADDRESS)—Offset 54h" on page 1222	00000000h
58h	4	"MPBASE (MPHY_BASE_ADDRESS)—Offset 58h" on page 1223	00000000h
5Ch	4	"PUBASE (PUNIT_BASE_ADDRESS)—Offset 5Ch" on page 1224	00000000h
80h	4	"UART Control (UART_CONT)—Offset 80h" on page 1225	00000000h
D8h	2	"BIOS Decode Enable (PCIE_REG_BIOS_DECODE_EN)—Offset D8h" on page 1225	FFCFh
E0h	2	"FDCAP (Feature_Detection_Capability_ID)—Offset E0h" on page 1226	0009h
E2h	1	"FDLEN (Feature_Detection_Capability_Length)—Offset E2h" on page 1227	0Ch
E3h	1	"FDVER (Feature_Detection_Version_Register)—Offset E3h" on page 1227	10h
E4h	4	"FVECTIDX (Feature_Vector_Index)—Offset E4h" on page 1228	00000000h
E8h	4	"FVECTD (Feature_Vector_Data)—Offset E8h" on page 1228	00000000h
F0h	4	"RCBA (RCRB_BASE_ADDRESS)—Offset F0h" on page 1229	00000000h

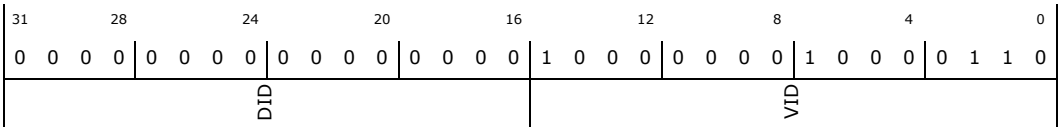
25.6.1 Identifiers Register (PCIE_REG_Identifiers)—Offset 0h

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_Identifiers: [B:0, D:31, F:0] + 0h

Default: 00008086h



Bit Range	Default & Access	Description
31:16	X RO	**Device Identification (DID):** This field identifies the particular device. This identifier is allocated by the vendor. This field is controlled by the LPC DID fuses Bits [31:23] are coming from the SETIDVALUE message Device ID[15:7] bits. Bits [22:21] are set constantly to 2'b00. Bits [20:16] are set constantly by pcu_did fuses.
15:0	8086h RO	**Vendor Identification (VID):** This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. 0 FFFFh is an invalid value for Vendor ID.

25.6.2 Command (PCIE_REG_COMMAND)—Offset 4h

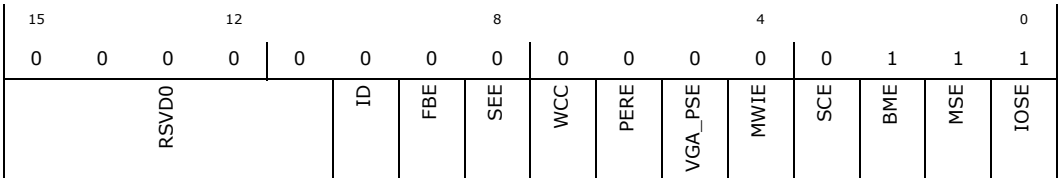
The Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not be implemented depending on a device's functionality

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCIE_REG_COMMAND: [B:0, D:31, F:0] + 4h

Default: 0007h



Bit Range	Default & Access	Description
15:11	0b RO	**RSVD0:** Reserved
10	0b RO	**Interrupt Disable (ID):** This bit disables the device/function from asserting INTx#. A value of 0 enables the assertion of its INTx# signal. A value of 1 disables the assertion of its INTx# signal. The LPC bridge has no interrupts to disable
9	0b RO	**Fast Back to Back Enable (FBE):** This optional read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. A value of 0 means fast back-to-back transactions are only allowed to the same agent
8	0b RW	**SERR# Enable (SEE):** This bit is an enable bit for the SERR# driver. A value of 0 disables the SERR# driver. A value of 1 enables the SERR# driver.

Bit Range	Default & Access	Description
7	0b RO	**Wait Cycle Control (WCC):** Reserved as '0' per PCI-Express spec
6	0b RW	**Parity Error Response Enable (PERE):** This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error status bit (bit 15 in the Status register) when an error is detected, but does not assert PERR# and continues normal operation.
5	0b RO	**VGA Palette Snoop (VGA_PSE):** This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. When this bit is 1, palette snooping is enabled (that is, the device does not respond to palette register writes and snoops the data). When the bit is 0, the device should treat palette write accesses like all other accesses. Reserved as '0' per PCI-Express spec
4	0b RO	**Memory Write and Invalidate Enable (MWIE):** This is an enable bit for using the Memory Write and Invalidate command. When this bit is 1, masters may generate the command. When it is 0, Memory Write must be used instead. Reserved as '0' per PCI-Express spec
3	0b RO	**Special Cycle Enable (SCE):** Controls a device's action on Special Cycle operations. A value of 0 causes the device to ignore all Special Cycle operations. A value of 1 allows the device to monitor Special Cycle operations. Reserved as '0' per PCI-Express spec
2	1b RO	**Bus Master Enable (BME):** Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. Bus master cannot be disabled on LPC
1	1b RO	**Memory Space Enable (MSE):** Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. Memory space cannot be disable on LPC
0	1b RO	**I/O Space Enable (IOSE):** Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. I/O space cannot be disable on LPC

25.6.3 Status (PCIE_REG_STATUS)—Offset 6h

The Status register is used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A one bit is reset (if it is not read-only) whenever the register is written, and the write data in the corresponding bit location is a 1. For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCIE_REG_STATUS: [B:0, D:31, F:0] + 6h

Default: 0210h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
DPE	SSE	RMA	RTA	STA	DTS		DPD	FBC	RSVD0	C66	CLIST	IS	RSVD1		

Bit Range	Default & Access	Description
15	0b RW	**Detected Parity Error (DPE):** This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 in the Command register).

Bit Range	Default & Access	Description
14	0b RW	**Signaled System Error (SSE):** This bit must be set whenever the device asserts SERR#. Set when the LPC bridge signals a system error to the internal SERR# logic.
13	0b RW	**Received Master Abort (RMA):** This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with Master-Abort. All master devices must implement this bit.
12	0b RW	**Received Target Abort: (RTA):** This bit must be set by a master device whenever its transaction is terminated with Target-Abort. All master devices must implement this bit.
11	0b RW	**Signaled Target Abort (STA):** This bit must be set by a target device whenever it terminates a transaction with Target-Abort. Devices that will never signal Target- Abort do not need to implement this bit.
10:9	01b RO	**DEVSEL# Timing Status (DTS):** These bits encode the timing of DEVSEL#. These are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). These bits Indicate medium timing, although this has no meaning on the backbone
8	0b RW	**Data Parity Error Detected (DPD):** This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself (on a read) or observed PERR# asserted (on a write); 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response bit (Command register) is set.
7	0b RO	**Fast Back to Back Capable (FBC):** This optional read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to 1 if the device can accept these transactions and must be set to 0 otherwise. This bit has no meaning on internal backbone.
6	0b RO	**RSVD0:** Reserved
5	0b RO	**66 MHz Capable (C66):** This optional read-only bit indicates whether or not this device is capable of running at 66 MHz. A value of zero indicates 33 MHz. A value of 1 indicates that the device is 66 MHz capable. This bit has no meaning on internal backbone
4	1b RO	**Capabilities List (CLIST):** This optional read-only bit indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. A value of zero indicates that no New Capabilities linked list is available. A value of one indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities. There is a capabilities list in the LPC bridge.
3	0b RO	**Interrupt Status (IS):** This read-only bit reflects the state of the interrupt in the device/function. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. The LPC bridge does not generate interrupts
2:0	0b RO	**RSVD1:** Reserved

25.6.4 Revision ID and Class Code (PCIE_REG_REVISION_ID_CLASS_CODE)—Offset 8h

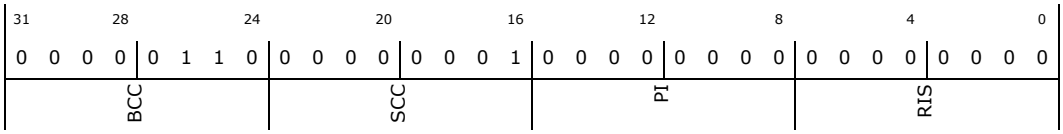
This register is a combination of two registers the Revision ID register and the Class Code register. The revision ID register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. The Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific registerlevel programming interface.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_REVISION_ID_CLASS_CODE: [B:0, D:31, F:0] + 8h

Default: 06010000h



Bit Range	Default & Access	Description
31:24	06h RO	**Base Class Code (BCC):** This field is a base class code which broadly classifies the type of function the device performs. Indicates the device is a bridge device.
23:16	01h RO	**Sub-Class Code (SCC):** This field is a sub-class code which identifies more specifically the function of the device. Indicates the device a PCI to ISA bridge
15:8	00h RO	**Programming Interface (PI):** This field identifies a specific register-level programming interface if any) so that device independent software can interact with the device. The LPC bridge has no programming interface.
7:0	X RO	**Revision ID (RIS):** This register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the Device ID. This field is controlled by the LPC RID fuses. Coming from the SETIDVALUE message Revision ID field

25.6.5 Master Latency Timer (PCIE_REG_MASTER_LAT_TIMER)—Offset Dh

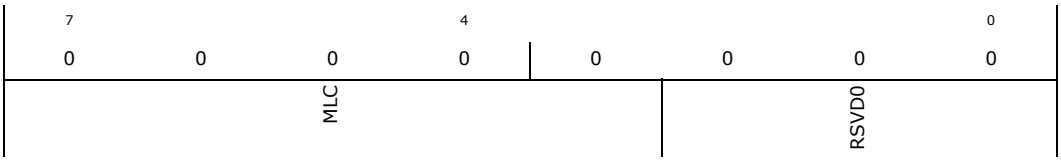
This register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. This register is implemented as read-only, the register must be initialized to 0.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PCIE_REG_MASTER_LAT_TIMER: [B:0, D:31, F:0] + Dh

Default: 00h



Bit Range	Default & Access	Description
7:3	00h RO	**Master Latency Count (MLC):** Reserved per PCIe spec.
2:0	0b RO	**RSVD0:** Reserved

25.6.6 Header Type (PCIE_REG_HEADER_TYPE)—Offset Eh

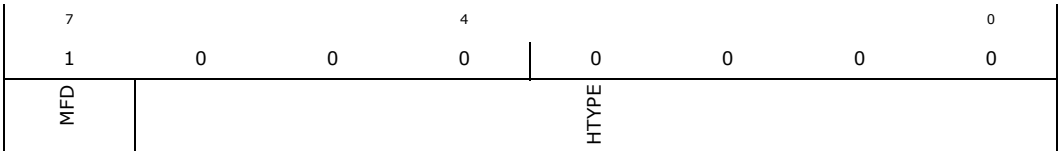
This byte identifies the layout of the second part of the predefined header (beginning at byte 10h in Configuration Space) and also whether or not the device contains multiple functions.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

PCIE_REG_HEADER_TYPE: [B:0, D:31, F:0] + Eh

Default: 80h



Bit Range	Default & Access	Description
7	1b RO	**Multi-function Device (MFD):** This field is used to identify a multi-function device. If the bit is 0, then the device is single function. If the bit is 1, then the device has multiple functions.
6:0	00h RO	**Header Type (HTYPE):** This field identifies the layout of the second part of the predefined header. The encoding 00h specifies the standard layout.

25.6.7 Subsystem ID and Vendor ID (PCIE_REG_SUBSYS_VENDOR_ID)—Offset 2Ch

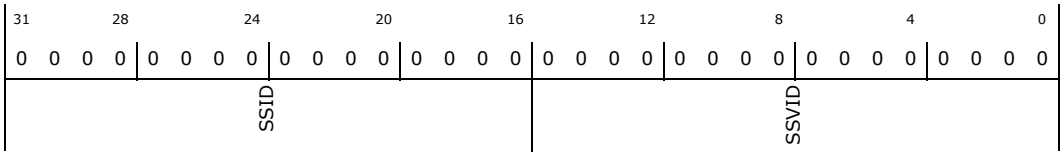
This register is used to uniquely identify the add-in card or subsystem where the PCI device resides. It provides a mechanism for add-in card vendors to distinguish their add- in cards from one another even though the add-in cards may have the same PCI controller on them (and, therefore, the same Vendor ID and Device ID). Implementation of this register is required for all PCI devices except those that have a base class 6 with sub class 0-4 (0, 1, 2, 3, 4), or a base class 8 with sub class 0-3 (0, 1, 2, 3). Subsystem Vendor IDs can be obtained from the PCI SIG and are used to identify the vendor of the add-in card or subsystem. Values for the Subsystem ID are vendor specific. Values in these registers must be loaded and valid prior to the system firmware or any system software accessing the PCI Configuration Space. How these values are loaded is not specified but could be done during the manufacturing process or loaded from external logic (e.g., strapping options, serial ROMs, etc.). These values must not be loaded using expansion ROM software because expansion ROM software is not guaranteed to be run during POST in all systems. Devices are responsible for guaranteeing the data is valid before allowing reads to these registers to complete. This can be done by responding to any accesses with Retry until the data is valid. If a device is designed to be used exclusively on the system board, the system vendor may use system specific software to initialize these registers after each power-on. This register can be written only once after PMU_PLTRST_B de-assertion.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_SUBSYS_VENDOR_ID: [B:0, D:31, F:0] + 2Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:16	0000h RW	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value. This field could be written only once.
15:0	0000h RW	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value. This field could be written only once.

25.6.8 Capability List Pointer (PCIE_REG_CAP_POINTER)—Offset 34h

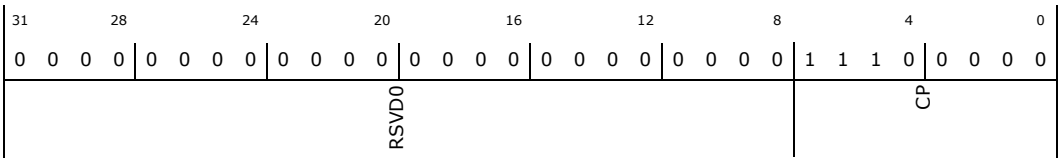
This optional register is used to point to a linked list of new capabilities implemented by this device. This register is only valid if the Capabilities List bit in the Status Register is set. If implemented, the bottom two bits are reserved and should be set to 00b. Software should mask these bits off before using this register as a pointer in Configuration Space to the first entry of a linked list of new capabilities.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PCIE_REG_CAP_POINTER: [B:0, D:31, F:0] + 34h

Default: 000000E0h



Bit Range	Default & Access	Description
31:8	0b RO	**RSVD0:** Reserved
7:0	E0h RO	**Capability Pointer (CP):** Indicates the offset of the first Capability Item.

25.6.9 ABASE (ACPI_BASE_ADDRESS)—Offset 40h

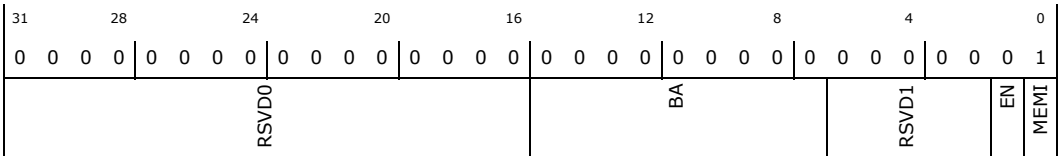
ACPI is mapped into I/O space. It is used by the PMC. Base Address registers that map into I/O Space are always 32 bits wide with bit 0 hardwired to a 1. Bit 1 is used to enable IO range pointed by this base address. Bits 31:16 are reserved and must return 0 on reads and the other bits could be used to map the device into I/O Space.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ACPI_BASE_ADDRESS: [B:0, D:31, F:0] + 40h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:7	000h RW	**Base Address (BA):** Provides the 128 bytes of I/O space for ACPI and TCO logic
6:2	0b RO	**RSVD1:** Reserved

Bit Range	Default & Access	Description
1	0b RW	**Enable (EN):** When set, decode of the IO range pointed to by the ABASE is enabled.
0	1b RO	**Memory Space Indication (MEMI):** This read-only bit always is 1, indicating that this BAR is IO mapped

25.6.10 PBASE (PMC_BASE_ADDRESS)—Offset 44h

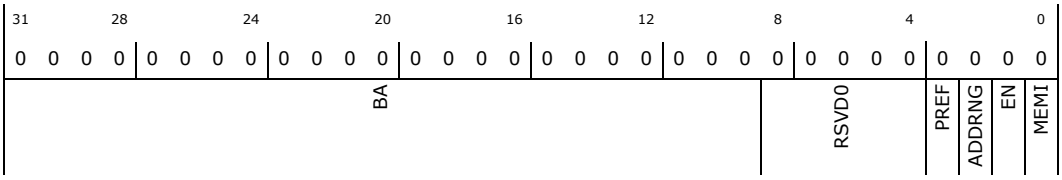
PMC registers are mapped into memory space. It is used by the PMC. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PMC_BASE_ADDRESS: [B:0, D:31, F:0] + 44h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	000000h RW	**Base Address (BA):** Provides 512 byte system memory base address for the PMC logic
8:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the PBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

25.6.11 GBASE (GPIO_BASE_ADDRESS)—Offset 48h

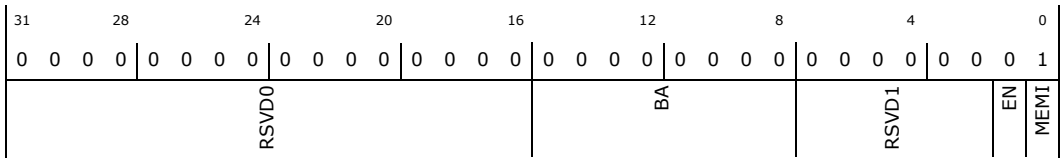
GPIO registers are mapped into I/O space. It is used by the Proxy agent (to IO controllers). Base Address registers that map into I/O Space are always 32 bits wide with bit 0 hardwired to a 1. Bit 1 is used to enable IO range pointed by this base address. Bits 31:16 are reserved and must return 0 on reads and the other bits could be used to map the device into I/O Space.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

GPIO_BASE_ADDRESS: [B:0, D:31, F:0] + 48h

Default: 00000001h



Bit Range	Default & Access	Description
31:16	0b RO	**RSVD0:** Reserved
15:8	00h RW	**Base Address (BA):** Provides the 256 bytes of I/O space for GPIO logic
7:2	0b RO	**RSVD1:** Reserved
1	0b RW	**Enable (EN):** When set, decode of the IO range pointed to by the GBASE is enabled.
0	1b RO	**Memory Space Indication (MEMI):** This read-only bit always is 1, indicating that this BAR is IO mapped

25.6.12 IOBASE (IO_CONTROLLER_BASE_ADDRESS)—Offset 4Ch

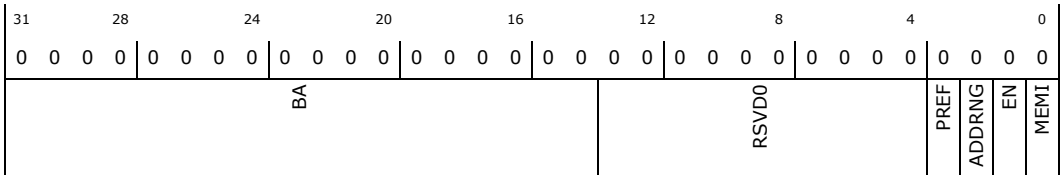
IO Controllers registers are mapped into memory space. It is used by the Proxy agent (to IO controllers). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

IO_CONTROLLER_BASE_ADDRESS: [B:0, D:31, F:0] + 4Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:14	00000h RW	**Base Address (BA):** Provides 8K byte system memory base address for the IO controllers logic
13:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the IOBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

25.6.13 IBASE (ILB_BASE_ADDRESS)—Offset 50h

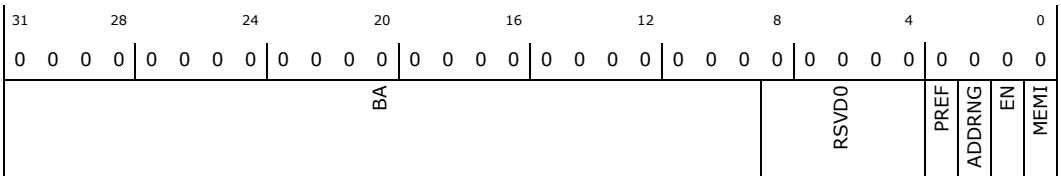
iLB registers are mapped into memory space. It is used by the iLB. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

ILB_BASE_ADDRESS: [B:0, D:31, F:0] + 50h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	000000h RW	**Base Address (BA):** Provides 512 byte system memory base address for the iLB logic
8:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the IBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

25.6.14 SBASE (SPI_BASE_ADDRESS)—Offset 54h

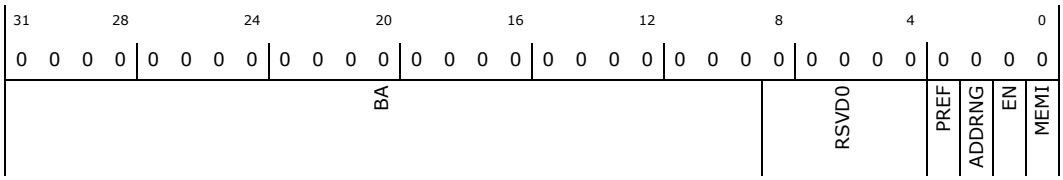
SPI registers are mapped into memory space. It is used by the SPI. Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

SPI_BASE_ADDRESS: [B:0, D:31, F:0] + 54h

Default: 00000000h



Bit Range	Default & Access	Description
31:9	000000h RW	**Base Address (BA):** Provides 512 byte system memory base address for the SPI logic
8:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the SBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

25.6.15 MPBASE (MPHY_BASE_ADDRESS)—Offset 58h

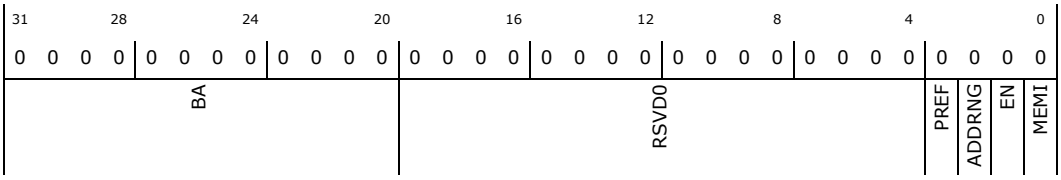
M-phys registers are mapped into memory space. It is used by the Proxy agent (to M-phys). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

MPHY_BASE_ADDRESS: [B:0, D:31, F:0] + 58h

Default: 00000000h



Bit Range	Default & Access	Description
31:20	000h RW	**Base Address (BA):** Provides 1M byte system memory base address for the M phys logic
19:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the MPBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

25.6.16 PUBASE (PUNIT_BASE_ADDRESS)—Offset 5Ch

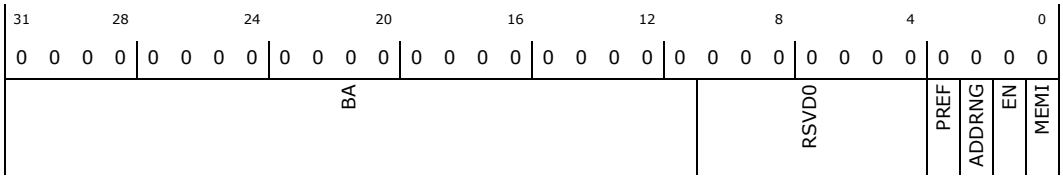
P-Unit registers are mapped into memory space. It is used by the Proxy agent (to P-Unit). Base Address registers that map into Memory Space are always 32 bits wide bit 0 hardwired to a 0. Bit 1 is used to enable memory range pointed by this base address. For Memory Base Address registers, bit 2 indicates if base address could be on 64 bit space or only on 32 bit space. Bit 3 should be set to 1 if the data is prefetchable and reset to 0 otherwise

Access Method

Type: PCI Configuration Register (Size: 32 bits)

PUNIT_BASE_ADDRESS: [B:0, D:31, F:0] + 5Ch

Default: 00000000h



Bit Range	Default & Access	Description
31:11	00000h RW	**Base Address (BA):** Provides 2K byte system memory base address for the P-Unit registers
10:4	0b RO	**RSVD0:** Reserved
3	0b RO	**Prefetchable (PREF):** Hardwired to 0. Indicated that this BAR is not prefetchable. Set to one, only if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range without causing errors.
2	0b RO	**Address Range (ADDRNG):** If set indicates that this BAR can be located in 64 bit address space, if clear indicates that this BAR can be located only in 32 bit address space.
1	0b RW	**Enable (EN):** When set, decode of the memory range pointed to by the PUBASE is enabled.
0	0b RO	**Memory Space Indication (MEMI):** This read-only bit always is 0, indicating that this BAR is memory mapped

25.6.17 UART Control (UART_CONT)—Offset 80h

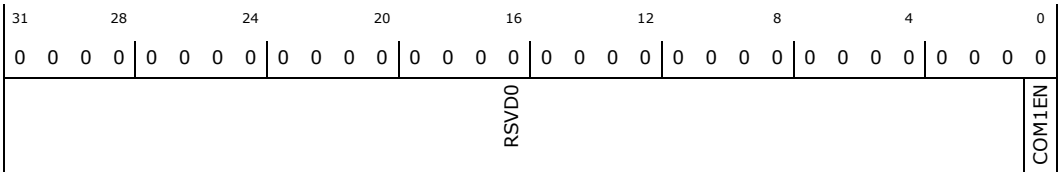
Controls the internal PCU UART ports

Access Method

Type: PCI Configuration Register (Size: 32 bits)

UART_CONT: [B:0, D:31, F:0] + 80h

Default: 00000000h



Bit Range	Default & Access	Description
31:1	0b RO	**RSVD0:** Reserved
0	0b RW	**COM1 Enable (COM1EN):** When set, enables the internal PCU COM1 UART port.

25.6.18 BIOS Decode Enable (PCIE_REG_BIOS_DECODE_EN)—Offset D8h

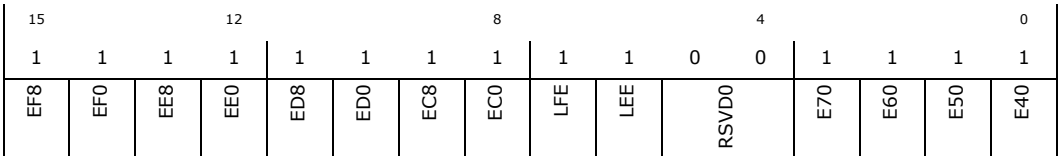
This register enables ranges in the BIOS for decoding purposes. Note that this register affects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. PCU EP simply decodes these ranges as memory accesses when enabled for the SPI/LPC flash interface.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

PCIE_REG_BIOS_DECODE_EN: [B:0, D:31, F:0] + D8h

Default: FFCFh



Bit Range	Default & Access	Description
15	1b RW	**F8-FF Enable (EF8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFF80000 - 0xFFFFFFFF - Feature space: 0xFFB80000 - 0xFFBFFFFF
14	1b RW	**F0-F8 Enable (EF0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFF00000 - 0xFFF7FFFF - Feature space: 0xFFB00000 - 0xFFB7FFFF
13	1b RW	**E8-EF Enable (EE8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFE80000 - 0xFFEFFFFF - Feature space: 0xFFA80000 - 0xFFAFFFFF
12	1b RW	**E0-E8 Enable (EE0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFE00000 - 0xFFE7FFFF - Feature space: 0xFFA00000 - 0xFFA7FFFF

Bit Range	Default & Access	Description
11	1b RW	**D8-DF Enable (ED8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFD80000 - 0xFFDFFFFF - Feature space: 0XFF980000 - 0xFF9FFFFF
10	1b RW	**D0-D8 Enable (ED0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFD00000 - 0xFFD7FFFF - Feature space: 0XFF900000 - 0xFF97FFFF
9	1b RW	**C8-CF Enable (EC8):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFC80000h - 0xFFCFFFFF - Feature space: 0xFF880000h - 0xFF8FFFFF
8	1b RW	**C0-C8 Enable (EC0):** Enables decoding of 512K of the following BIOS range: - Data space: 0xFFC00000 - 0xFFC7FFFF - Feature space: 0xFF800000 - 0xFF87FFFF
7	1b RW	**Legacy F Segment Enable (LFE):** This enables the decoding of the legacy 64KB range at 0xF0000 - 0xFFFFF
6	1b RW	**Legacy E Segment Enable (LEE):** This enables the decoding of the legacy 64KB range at 0xE0000 - 0xEFFFF
5:4	0b RO	**RSVD0:** Reserved
3	1b RW	**70-7F Enable (E70):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF700000 - 0xFF7FFFFF - Feature space: 0xFF300000 - 0xFF3FFFFF
2	1b RW	**60-6F Enable (E60):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF600000 - 0xFF6FFFFF - Feature Space: 0xFF200000 - 0xFF2FFFFF
1	1b RW	**50-5F Enable (E50):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF500000 - 0xFF5FFFFF - Feature space: 0xFF100000 - 0xFF1FFFFF
0	1b RW	**40-4F Enable (E40):** Enables decoding of 1MB of the following BIOS range: - Data space: 0xFF400000 - 0xFF4FFFFF - Feature Space: 0xFF000000 - 0xFF0FFFFF

25.6.19 FDCAP (Feature_Detection_Capability_ID)—Offset E0h

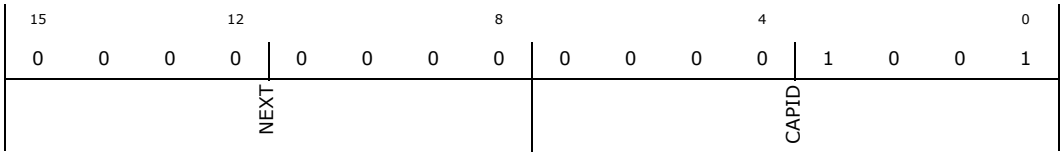
Feature detection capability ID.

Access Method

Type: PCI Configuration Register (Size: 16 bits)

Feature_Detection_Capability_ID: [B:0, D:31, F:0] + E0h

Default: 0009h



Bit Range	Default & Access	Description
15:8	00h RO	**Next Item Pointer (NEXT):** Configuration offset of the next Capability Item. 0x00 indicates the last item in the Capability List.
7:0	09h RO	**Capability ID (CAPID):** Value of 0x09 indicates a Vendor Specific Capability

25.6.20 FDLEN (Feature_Detection_Capability_Length)—Offset E2h

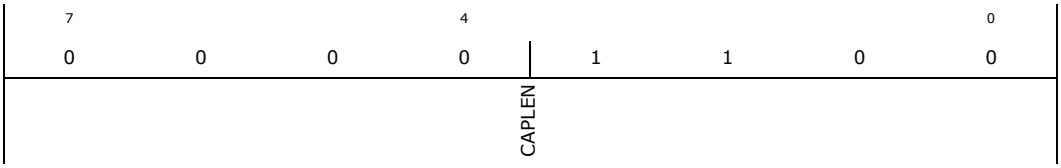
Feature detection capability length.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Feature_Detection_Capability_Length: [B:0, D:31, F:0] + E2h

Default: 0Ch



Bit Range	Default & Access	Description
7:0	0Ch RO	**Capability Length (CAPLEN):** Indicates the length of this Vendor Specific capability, as required by PCI Spec

25.6.21 FDVER (Feature_Detection_Version_Register)—Offset E3h

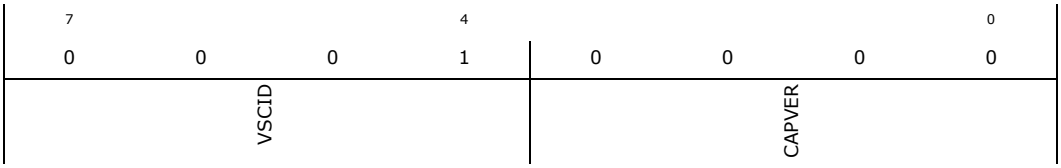
Feature detection version register.

Access Method

Type: PCI Configuration Register (Size: 8 bits)

Feature_Detection_Version_Register: [B:0, D:31, F:0] + E3h

Default: 10h



Bit Range	Default & Access	Description
7:4	1h RO	**Vendor-Specific Capability ID (VSCID):** A value of 0x1 in this 4-bit field identifies this Capability as Feature Detection Type. This field allows software to differentiate the Feature Detection Capability from other Vendor-Specific capabilities.
3:0	0h RO	**Capability Version (CAPVER):** This field indicates the version of the Feature Detection capability

25.6.22 FVECTIDX (Feature_Vector_Index)—Offset E4h

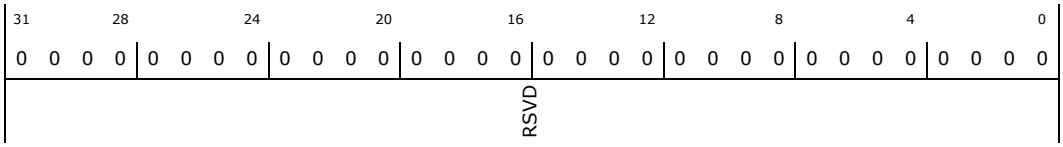
Feature vector index - Reserved

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Feature_Vector_Index: [B:0, D:31, F:0] + E4h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**RSVD:** RSVD

25.6.23 FVECTD (Feature_Vector_Data)—Offset E8h

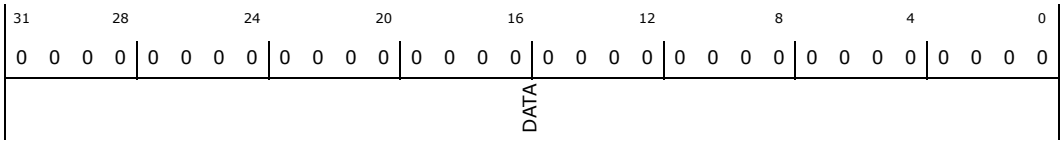
Feature vector data

Access Method

Type: PCI Configuration Register (Size: 32 bits)

Feature_Vector_Data: [B:0, D:31, F:0] + E8h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	00000000h RO	**Data (DATA):** 32-bit data value that is taken from capability feature fuses

25.6.24 RCBA (RCRB_BASE_ADDRESS)—Offset F0h

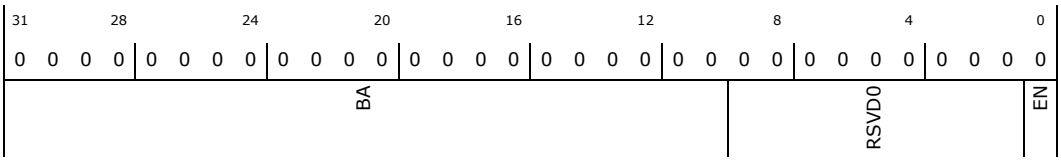
Root Complex registers are mapped into memory space. It is used by the PCU EP and Proxy engine.

Access Method

Type: PCI Configuration Register (Size: 32 bits)

RCRB_BASE_ADDRESS: [B:0, D:31, F:0] + F0h

Default: 00000000h



Bit Range	Default & Access	Description
31:10	000000h RW	**Base Address (BA):** Base Address for the root complex register block decode range. This address is aligned on a 1KB boundary.
9:1	0b RO	**RSVD0:** Reserved
0	0b RW	**Enable (EN):** When set, enables the range specified in BA to be claimed as the RCRB.

25.7 PCU iLB LPC BIOS Control Memory Mapped I/O Registers

Table 180. Summary of PCU iLB LPC BIOS Control Memory Mapped I/O Registers—RCRB_BASE_ADDRESS

Offset	Size	Register ID—Description	Default Value
0h	4	"GCS (RCRB_GENERAL_CONTROL)—Offset 0h" on page 1230	00000000h

25.7.1 GCS (RCRB_GENERAL_CONTROL)—Offset 0h

General Control and Status - contains BIOS configuration and status

Access Method

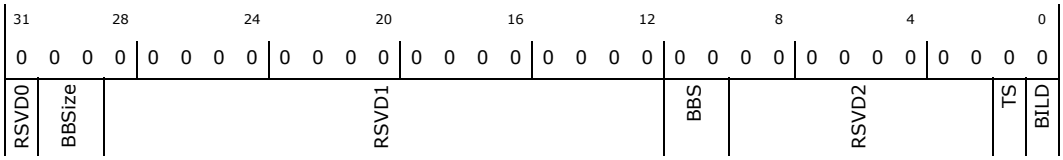
Type: Memory Mapped I/O Register (Size: 32 bits)

RCRB_GENERAL_CONTROL: [RCRB_BASE_ADDRESS] + 0h

RCRB_BASE_ADDRESS Type: PCI Configuration Register (Size: 32 bits)

RCRB_BASE_ADDRESS Reference: [B:0, D:31, F:0] + F0h

Default: 00000000h



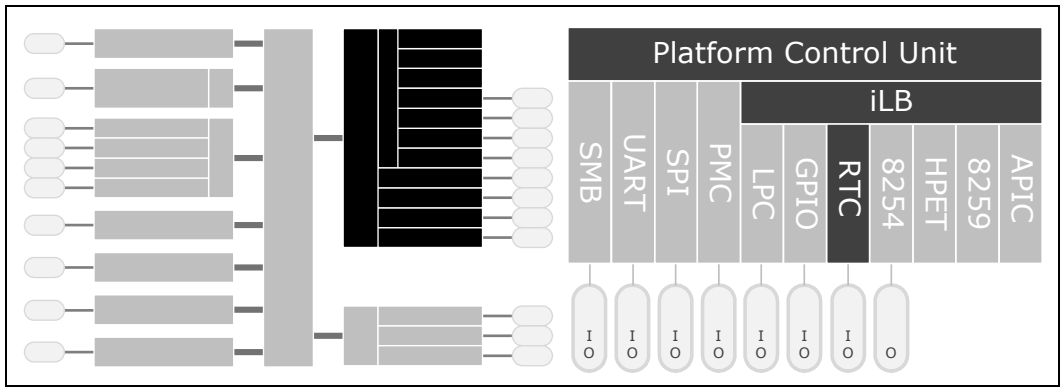
Bit Range	Default & Access	Description
31	0b RO	**RSVD0:** Reserved
30:29	X RO	**Boot Block Size (BBSize):** This field determines the size of the BIOS boot block. Default is controlled by 'Boot Block Size' soft strap. 00 : 64KB (Default) : Invert A16 if Top Swap is enabled 01 : 128KB : Invert A17 if Top Swap is enabled 10 : 256KB : Invert A18 if Top Swap is enabled 11 : Reserved This soft strap only applies when booting from SPI. Boot from LPC (FWH) only supports a 64KB boot block size (Invert A16) and this soft strap value is a don't care.
28:12	0b RO	**RSVD1:** Reserved
11:10	X RW	**Boot BIOS Straps (BBS):** This field determines the destination of accesses to the BIOS memory range. Default is controlled by 'Boot BIOS Straps' pin strap. 00 LPC 01 Reserved 10 Reserved 11 SPI The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) is not set.
9:2	0b RO	**RSVD2:** Reserved
1	X RW	**Top Swap (TS):** When set, PCU EP will invert either A16, A17, or A18 for cycles going to the BIOS space (but not the feature space) in the FWH. When cleared, PCU EP will not invert A16. If booting from LPC (FWH), then the Boot Blook size is 64KB and A16 is inverted if Top Swap is enabled. If booting from SPI, then the BOOT_BLOCK_SIZE soft strap determines if A16, A17, or A18 should be inverted if Top Swap is enabled. If Top-Swap pin-strap is active, then this bit cannot be cleared by software. This bit should be kept in RTC well and should be reset only by SRTCRST_b
0	0h RW	**BIOS Interface Lock-Down (BILD):** When set, prevents GCS.TS and GCS.BBS from being changed. This bit can only be written from 0 to 1 once.

26 PCU – iLB – Real Time Clock (RTC)

The processor contains a Motorola MC146818B-compatible real-time clock with 242 bytes of battery-backed RAM. The real-time clock performs twos key functions—keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 kHz crystal and a 3.3 V battery.

The RTC supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC supports a date alarm that allows for scheduling a wake up event up to 30 days in advance.



26.1 Signal Descriptions

Please see Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 181. RTC Signals (Sheet 1 of 2)

Signal Name	Direction/ Type	Description
ILB_RTC_X1	I Analog	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, the signal can be driven with the desired clock rate.

Table 181. RTC Signals (Sheet 2 of 2)

Signal Name	Direction/ Type	Description
ILB_RTC_X2	I Analog	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, the signal should be left floating.
ILB_RTC_RST#	I Digital	**RTC Reset:** An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. The RC time delay should be in the 10-20 ms range When asserted, this signal resets all register bits in the RTC well except for GEN_PMCON1.RPS. **NOTE:** Unless registers are being cleared (only to be done in the G3 power state), the signal input must always be high when all other RTC power planes are on. **NOTE:** In the case where the RTC battery is dead or missing on the platform, the signal should be deasserted before the PMC_RSMRST# signal is deasserted.
ILB_RTC_TEST#	I Digital	**RTC Battery Test:** An external RC circuit creates a time delay for the signal such that it will go high (de-assert) sometime after the battery voltage is valid. The RC time delay should be in the 10-20 ms range. If the battery is missing/weak, this signal appears low (asserted) at boot just after the suspend power rail (V3P3A) is up since it will not have time to meet Vih when V3P3A is high. The weak/missing battery condition is reported in the GEN_PMCON1.RPS (RTC Power Status) register. When asserted, BIOS may clear the RTC CMOS RAM. **NOTE:** Unless CMOS is being cleared (only to be done in the G3 power state) or the battery is low, the signal input must always be high when all other RTC power planes are on. **NOTE:** This signal may also be used for debug purposes, as part of a XDP port.
ILB_RTC_EXTPAD	I Analog	External capacitor connection

26.2 Features

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 ms to 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block have very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions. A host-initiated write takes precedence over a hardware update in the event of a collision.

26.2.1 Update Cycles

An update cycle occurs once a second, if the B.SET bit is not asserted and the divide chain is properly configured. During this procedure, the stored time and date are incremented, overflow checked, a matching alarm condition is checked, and the time and date are rewritten to the RAM locations. The update cycle starts at least 488 ms

after A.UIP is asserted, and the entire cycle does not take more than 1984 ms to complete. The time and date RAM locations (00h to 09h) are disconnected from the external bus during this time.

26.3 Interrupts

The real-time clock interrupt is internally routed within the processor both to the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the processor, nor is it shared with any other interrupt. IRQ8# from the ILB_LPC_SERIRQ stream is ignored. However, the High Performance Event Timers can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

26.3.1 Lockable RAM Ranges

The RTC battery-backed RAM supports two 8-byte ranges that can be locked: the RC.UL and RC.LL register bits. When the locking bits are set, the corresponding range in the RAM is not readable or writable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the location's actual value (resultant value is undefined).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to re-lock the RAM range.

26.3.2 Clearing Battery-Backed RTC CMOS RAM

Clearing CMOS RAM in an processor-based platform can be done by using a jumper on ILB_RTC_TEST# or a GPI. Implementations should not attempt to clear CMOS by using a jumper to pull RTC_VCC low.

Note: The entire Extended Bank and bytes 0Eh-7Fh of the Standard Bank will be cleared.

26.3.2.1 Using ILB_RTC_TEST# to Clear the RTC CMOS RAM

A jumper on ILB_RTC_TEST# can be used to clear CMOS values. When ILB_RTC_TEST# is low, the GEN_PMCON1.RPS register bit will be set. BIOS can monitor the state of this bit, and manually clear the RTC CMOS array once the system is booted. The normal position will cause ILB_RTC_TEST# to be pulled up through a weak pull-up resistor. This ILB_RTC_TEST# jumper technique allows the jumper to be moved and then replaced—all while the system is powered off. Then, once booted, the GEN_PMCON1.RPS bit can be detected in the set state.

26.3.3 Using a GPI to Clear CMOS

A jumper on a GPI can also be used to clear CMOS values. BIOS should detect the setting of this GPI on system boot-up, and manually clear the CMOS array.

Note: The GPI strap technique to clear CMOS requires multiple steps to implement. The system is booted with the jumper in new position, then powered back down. The jumper is replaced back to the normal position, then the system is rebooted again.

Warning: Do not implement a jumper on RTC_VCC to clear CMOS.

26.3.4 Clearing Battery Backed RTC Registers

Clearing Battery Backed RTC Registers in a processor based platform can be done by using a jumper on ILB_RTC_RST#. Implementations should not attempt to clear the registers by using a jumper to pull RTC_VCC low. A jumper on ILB_RTC_RST# pulled to ground can be used to reset the state of those Battery Backed RTC Register configurations bit that reside in the RTC power well to their default state. Table 182 shows which bits are set to their default state when ILB_RTC_RST# is asserted low.

Table 182. Register Bits Reset by ILB_RTC_RST# Assertion

Register Bit	Bit(s)	Default State
RCRB_GENERAL_CONTROL.TS	1	xb
GEN_PMCON1.PME_B0_S5_DIS	15	0b
GEN_PMCON1.WOL_EN_OVRD	13	0b
GEN_PMCON1.DIS_SLP_X_STRCH_SUS_UP	12	0b
GEN_PMCON1.RTC Reserved	8	0b
GEN_PMCON1.SWSMI_RATESEL	7:6	00b
GEN_PMCON1.S4MAW	5:4	00b
GEN_PMCON1.S4ASE	3	0b
GEN_PMCON1.AG3E	0	0b
PM1_STS_EN.RTC_EN	26	0b
PM1_STS_EN.PWRBTNOR_STS	11	0b
PM1_CNT.SLP_TYP	12:10	0b
GPE0a_EN.PME_B0_EN	13	0b
GPE0a_EN.BATLOW_EN	10	0b

26.4 References

Accessing the Real Time Clock Registers and the NMI Enable Bit: http://download.intel.com/design/intarch/PAPERS/321088.pdf

26.5 Register Map

26.6 IO Mapped Registers

The RTC internal registers and RAM is organized as two banks of 128 bytes each, called the standard and extended banks.

Note: It is not possible to disable the extended bank.

The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A - D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM. All data movement between the host CPU and the RTC is done through registers mapped to the standard I/O space.

Note: Registers reg_RTC_IR_type and reg_RTC_TR_type are used for data movement to and from the standard bank. Registers reg_RTC_RIR_type and reg_RTC_RTR_type are used for data movement to and from the extended bank. All of these registers have alias I/O locations, as indicated in Table 183.

Table 183. I/O Registers Alias Locations

Register	Original I/O Location	Alias I/O Location
reg_RTC_IR_type	70h	74h
reg_RTC_TR_type	71h	75h
reg_RTC_RIR_type	72h	76h
reg_RTC_RTR_type	73h	77h

26.7 Indexed Registers

The RTC contains indexed registers that are accessed via the reg_RTC_IR_type and reg_RTC_TR_type registers.

Table 184. RTC Indexed Registers (Sheet 1 of 2)

Start	End	Name
00h	00h	Seconds
01h	01h	Seconds Alarm
02h	02h	Minutes
03h	03h	Minutes Alarm
04h	04h	Hours
05h	05h	Hours Alarm
06h	06h	Day of Week
07h	07h	Day of Month
08h	08h	Month
09h	09h	Year
0Ah	0Ah	Register A

Table 184. RTC Indexed Registers (Sheet 2 of 2)

Start	End	Name
0Bh	0Bh	Register B
0Ch	0Ch	Register C
0Dh	0Dh	Register D
0Eh	7Fh	114 Bytes of User RAM

26.8 PCU iLB Real Time Clock (RTC) I/O Registers

Table 185. Summary of PCU iLB Real Time Clock (RTC) I/O Registers

Offset	Size	Register ID—Description	Default Value
70h	1	"IR (reg_RTC_IR_type)—Offset 70h" on page 1237	00h
71h	1	"TR (reg_RTC_TR_type)—Offset 71h" on page 1237	00h
72h	1	"RIR (reg_RTC_RIR_type)—Offset 72h" on page 1238	00h
73h	1	"RTR (reg_RTC_RTR_type)—Offset 73h" on page 1238	00h

26.8.1 IR (reg_RTC_IR_type)—Offset 70h

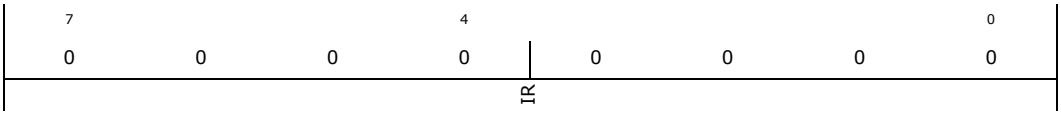
Indexed Registers

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_IR_type: 70h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**IR:** Real-Time Clock (Standard RAM) Index Register Note: Writes to 72h, 74h, and 76h do not affect the NMI enable (bit 7 of 70h)

26.8.2 TR (reg_RTC_TR_type)—Offset 71h

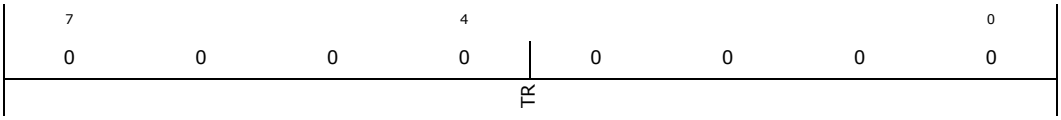
Target Registers

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_TR_type: 71h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**TR:** Real-Time Clock (Standard RAM) Target Register

26.8.3 RIR (reg_RTC_RIR_type)—Offset 72h

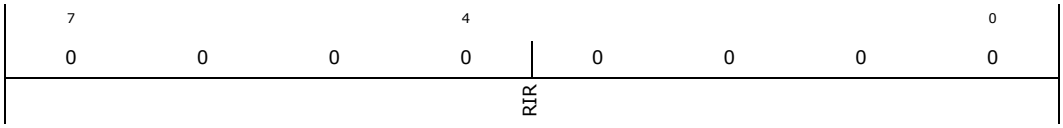
Extended RAM Index Register

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_RIR_type: 72h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**RIR:** Extended RAM Index Register

26.8.4 RTR (reg_RTC_RTR_type)—Offset 73h

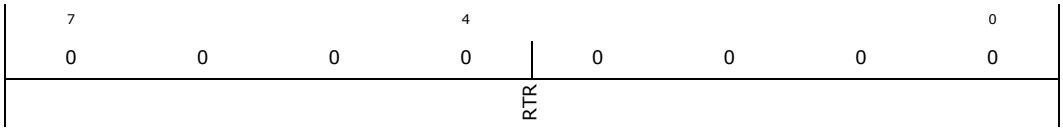
Extended RAM Target Register

Access Method

Type: I/O Register
(Size: 8 bits)

reg_RTC_RTR_type: 73h

Default: 00h

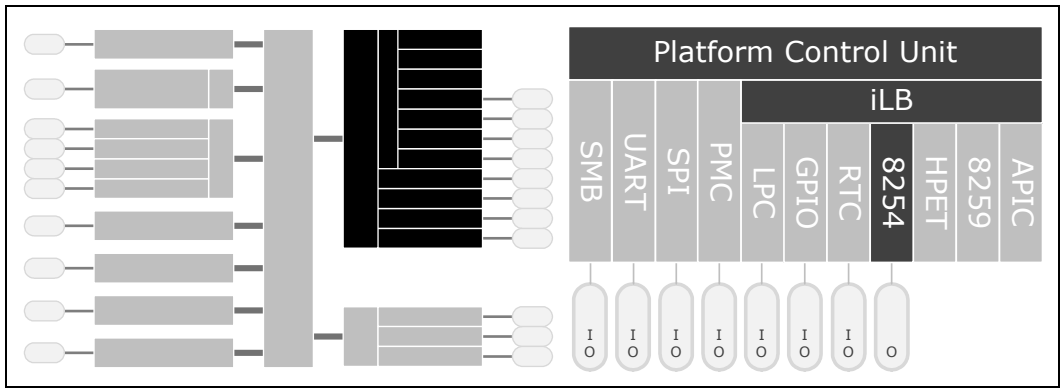


Bit Range	Default & Access	Description
7:0	X RW	**RTR:** Extended RAM Target Register

§ §

27 PCU – iLB – 8254 Timers

The 8254 contains three counters which have fixed uses including system timer and speaker tone. All registers are clocked by a 14.31818 MHz clock.



27.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 186. 8254 Signals

Signal Name	Direction/ Type	Description
ILB_8254_SPKR	O TBD	**Speaker:** The signal drives an external speaker driver device, which in turn drives the system speaker. Upon PMC_PLTRST#, its output state is 0. *This signal is multiplexed and may be used by other functions.*

27.2 Features

27.2.1 Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count

value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

27.2.2 Counter 1, Refresh Request Signal

This counter is programmed for Mode 2 operation and impacts the period of the NSC.RTS register bit. Programming the counter to anything other than Mode 2 results in undefined behavior.

27.2.3 Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to the NSC.SDE register bit.

27.3 Use

27.3.1 Timer Programming

The counter/timers are programmed in the following fashion:

1. Write a control word to select a counter.
2. Write an initial count for that counter.
3. Load the least and/or most significant bytes (as required by Control Word Bits 5, 4) of the 16-bit counter.
4. Repeat with other counters.

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting is affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The Control Word Register at port 43h controls the operation of all three counters. Several commands are available:

- **Control Word Command.** Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- **Counter Latch Command.** Latches the current count so that it can be read by the system. The countdown process continues.
- **Read Back Command.** Reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 187 lists the six operating modes for the interval counters.

Table 187. Counter Operating Modes

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware re-triggerable one-shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.
3	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, etc.
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.

27.3.2 Reading from the Interval Timer

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters: a simple read operation, counter Latch command, and the Read-Back command. Each is explained below.

With the simple read and counter latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

27.3.2.1 Simple Read

The first method is to perform a simple read operation. The counter is selected through Port 40h (Counter 0), 41h (Counter 1), or 42h (Counter 2).

Note: Performing a direct read from the counter does not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of Counter 2, the count can be stopped by writing 0b to the NSC.TC2E register bit.

27.3.2.2 Counter Latch Command

The Counter Latch command, written to Port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a two-byte count. The count value is then read from each counter's Count register as was programmed by the Control register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Counter Latch commands do not affect the programmed mode of the counter in any way.

If a counter is latched and then, some time later, latched again before the count is read, the second Counter Latch command is ignored. The count read is the count at the time the first Counter Latch command was issued.

27.3.2.3 Read Back Command

The Read Back command, written to Port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back commands. If multiple count and/or status Read Back commands are issued to the same counters without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter returns the latched status, regardless of which was latched first. The next one or two reads, depending on whether the counter is programmed for one or two type counts, returns the latched count. Subsequent reads return unlatched count.

27.4 Register Map

27.5 IO Mapped Registers

The IO ports listed in Table 188 have multiple register functions depending on the current programmed state of the 8254. The port numbers referenced in the register descriptions following Table 188 is one possible combination but not the only one.

Table 188. Register Aliases

Port	Alias	Register Name	Default Value	Access
40h	50h	Counter 0 Interval Time Status Byte Format (C0TS)	0xxxxxxxb	RO
		Counter 0 Counter Access Port Register (C0AP)	Undefined	RW
41h	51h	Counter 1 Interval Time Status Byte Format (C1TS)	0xxxxxxxb	RO
		Counter 1 Counter Access Port Register (C1AP)	Undefined	RW
42h	52h	Counter 2 Interval Time Status Byte Format (C2TS)	0xxxxxxxb	RO
		Counter 2 Counter Access Port Register (C2AP)	Undefined	RW
43h	-	Timer Control Word Register (TCW)	Undefined	WO
		Read Back Command (RBC)	xxxxxxx0b	WO
		Counter Latch Command (CLC)	xxxx0000b	WO

27.6 PCU iLB 8254 Timers IO Registers

Table 189. Summary of PCU iLB 8254 Timers I/O Registers

Offset	Size	Register ID—Description	Default Value
40h	1	"C0TS—Offset 40h" on page 1244	00h
41h	1	"C1TS—Offset 41h" on page 1245	00h
42h	1	"C2TS—Offset 42h" on page 1246	00h
43h	1	"TCW—Offset 43h" on page 1247	00h
50h	1	"C0AP—Offset 50h" on page 1247	00h
51h	1	"C1AP—Offset 51h" on page 1248	00h
52h	1	"C2AP—Offset 52h" on page 1248	00h
61h	1	"NSC—Offset 61h" on page 1249	20h

27.6.1 C0TS—Offset 40h

Counter 0 Interval Time Status Byte Format.Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 0, the next read from this register returns the status byte.

Access Method

Type: I/O Register (Size: 8 bits)

C0TS: 40h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
CS	CR	RWS		MD			CT

Bit Range	Default & Access	Description
7	0b RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

27.6.2 C1TS—Offset 41h

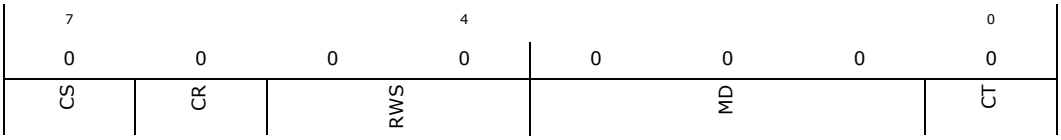
Counter 1 Interval Time Status Byte Format. Counter 1 Interval Time Status Byte Format. Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 1, the next read from this register returns the status byte.

Access Method

Type: I/O Register
(Size: 8 bits)

C1TS: 41h

Default: 00h



Bit Range	Default & Access	Description
7	0b RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

27.6.3 C2TS—Offset 42h

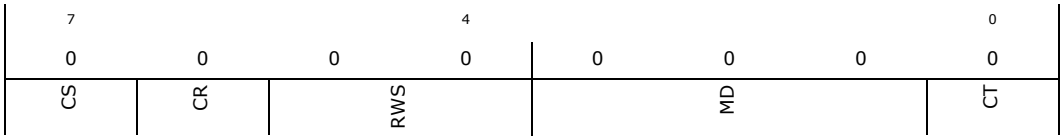
Counter 2 Interval Time Status Byte Format. Counter 2 Interval Time Status Byte Format. Status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for counter 2, the next read from this register returns the status byte.

Access Method

Type: I/O Register (Size: 8 bits)

C2TS: 42h

Default: 00h



Bit Range	Default & Access	Description
7	0b RO	**CS:** Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.
6	X RO	**CR:** Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode.
5:4	X RO	**RWS:** Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X RO	**MD:** Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. Bits Mode Description 000 0 Out signal on end of count (=0) 001 1 Hardware retriggerable one-shot x10 2 Rate generator (divide by n counter) x11 3 Square wave output 100 4 Software triggered strobe 101 5 Hardware triggered strobe
0	X RO	**CT:** Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.

27.6.4 TCW—Offset 43h

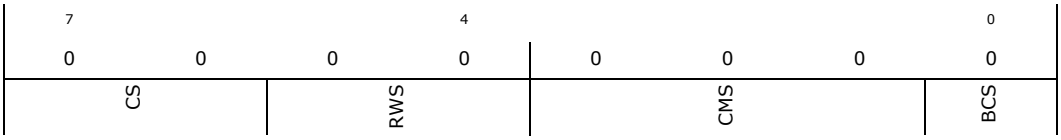
Timer Control Word Register. This register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Access Method

Type: I/O Register
(Size: 8 bits)

TCW: 43h

Default: 00h



Bit Range	Default & Access	Description
7:6	X WO	**CS:** Counter Select (CS): The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select 11 Read Back Command
5:4	X WO	**RWS:** Read/Write Select RWS): The counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2) 00 Counter Latch Command 01 Read/Write Least Significant Byte (LSB) 10 Read/Write Most Significant Byte (MSB) 11 Read/Write LSB then MSB
3:1	X WO	**CMS:** Counter Mode Selection (CMS): Selects one of six modes of operation for the selected counter. 000 = Out signal on end of count (=0) 001 = Hardware retriggerable one-shot x10 = Rate generator (divide by n counter) x11 = Square wave output 100 = Software triggered strobe 101 = Hardware triggered strobe
0	X WO	**BCS:** Binary/BCD Countdown Select (BCS): 0 Binary countdown is used. The largest possible binary count is 216 1 Binary coded decimal (BCD) count is used. The largest possible BCD count is 104

27.6.5 C0AP—Offset 50h

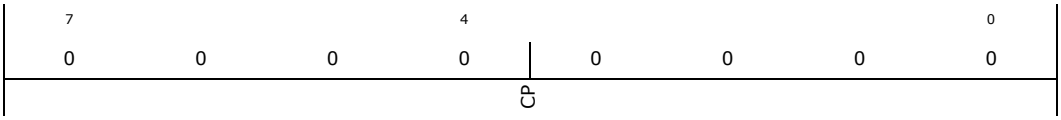
Counter 0 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

C0AP: 50h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

27.6.6 C1AP—Offset 51h

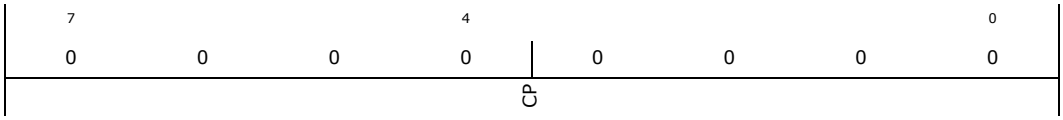
Counter 1 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

C1AP: 51h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

27.6.7 C2AP—Offset 52h

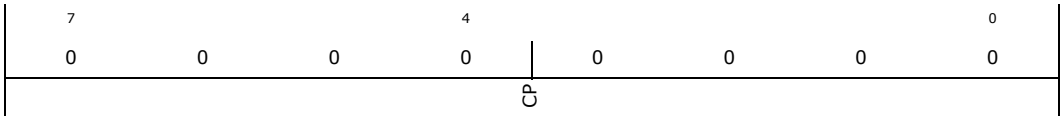
Counter 2 Counter Access Port Register

Access Method

Type: I/O Register
(Size: 8 bits)

C2AP: 52h

Default: 00h



Bit Range	Default & Access	Description
7:0	X RW	**CP:** Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

27.6.8 NSC—Offset 61h

NMI Status and Control

Access Method

Type: I/O Register
(Size: 8 bits)

NSC: 61h

Default: 20h

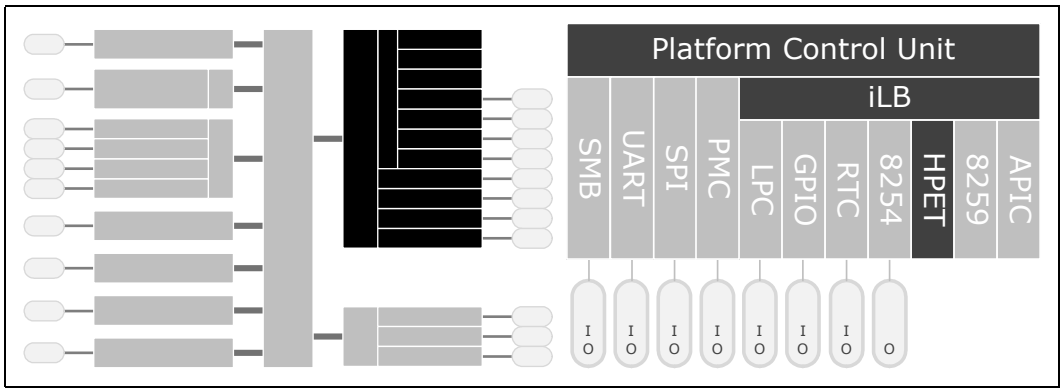
7			4				0
0	0	1	0	0	0	0	0
SNS	INS	T2S	RTS	INE	SNE	SDE	TC2E

Bit Range	Default & Access	Description
7	0b RO	**SNS:** SERR# NMI Status (SNS): Set on errors from a PCIe port or internal functions that generate SERR#. SNE in this register must be cleared in order for this bit to be set. To reset the interrupt, set bit 2 to 1 and then set it to 0.
6	0b RO	**INS:** IOCHK NMI Status (INS): Set when SERIRQ asserts IOCHK# and INE in this register is cleared. To reset the interrupt, set bit 3 to 1 and then set it to 0.
5	1b RO	**RTS (T2S):** Timer Counter 2 Status (T2S): Reflects the current state of the 8254 counter 2 outputs. Counter 2 must be programmed for this bit to have a determinate value.
4	0b RO	**RTS:** Refresh Cycle Toggle Status (RTS): Reflects the current state of 8254 counter 1
3	X RW	**INE:** IOCHK NMI Enable (INE): When set, IOCHK# NMIs are disabled. When cleared, IOCHK# NMIs are enabled.
2	0b RW	**SNE:** SERR# NMI Enable (SNE): When set, SERR# NMIs are disabled. When cleared, SERR# NMIs are enabled.
1	0b RW	**SDE:** Speaker Data Enable (SDE): When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	0b RW	**TC2E:** Timer Counter 2 Enable (TC2E): When cleared, counter 2 counting is disabled. When set, counting is enabled.

§ §

28 PCU – iLB – High Precision Event Timer (HPET)

This function provides a set of timers that to be used by the operating system for timing events. One timer block is implemented, containing one counter and three timers.



28.1 Features

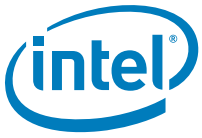
28.1.1 Non-Periodic Mode – All Timers

This mode can be thought of as creating a one-shot. When a timer is set up for non-periodic mode, it generates an interrupt when the value in the main counter matches the value in the timer's comparator register. As timers 1 and 2 are 32-bit, they will generate another interrupt when the main counter wraps.

T0CV cannot be programmed reliably by a single 64-bit write in a 32-bit environment unless only the periodic rate is being changed. If T0CV needs to be re-initialized, the following algorithm is performed:

1. Set T0C.TVS
2. Set T0CV[31:0]
3. Set T0C.TVS
4. Set T0CV[63:32]

Every timer is required to support the non-periodic mode of operation.



28.1.2 Periodic Mode –Timer 0 only

When set up for periodic mode, when the main counter value matches the value in T0CV, an interrupt is generated (if enabled). Hardware then increases T0CV by the last value written to T0CV. During run-time, T0CV can be read to find out when the next periodic interrupt will be generated. Software is expected to remember the last value written to T0CV.

Example: if the value written to T0CV is 00000123h, then

- An interrupt will be generated when the main counter reaches 00000123h.
- T0CV will then be adjusted to 00000246h.
- Another interrupt will be generated when the main counter reaches 00000246h.
- T0CV will then be adjusted to 00000369h.

When the incremented value is greater than the maximum value possible for T0CV, the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h.

If software wants to change the periodic rate, it writes a new value to T0CV. When the timer's comparator matches, the new value is added to derive the next matching point. If software resets the main counter, the value in the comparator's value register must also be reset by setting T0C.TVS. To avoid race conditions, this should be done with the main counter halted. The following usage model is expected:

1. Software clears GCFG.EN to prevent any interrupts.
2. Software clears the main counter by writing a value of 00h to it.
3. Software sets T0C.TVS.
4. Software writes the new value in T0CV.
5. Software sets GCFG.EN to enable interrupts.

28.1.2.1 Interrupts

If each timer has a unique interrupt and the timer has been configured for edge-triggered mode, then there are no specific steps required. If configured to level-triggered mode, then its interrupt must be cleared by software by writing a '1' back to the bit position for the interrupt to be cleared.

Interrupts associated with the various timers have several interrupt mapping options. Software should mask GCFG.LRE when reprogramming HPET interrupt routing to avoid spurious interrupts.

28.1.2.2 Mapping Option #1: Legacy Option (GCFG.LRE set)

This forces the mapping indicated in the following table.

Table 190. 8254 Interrupt Mapping

Timer	8259 Mapping	APIC Mapping	Comment
0	IRQ0	IRQ2	The 8254 timer will not cause any interrupts
1	IRQ8	IRQ8	RTC will not cause any interrupts.
2	T2C.IR	T2C.IRC	

28.1.2.3 Mapping Option #2: Standard Option (GCFG.LRE cleared)

Each timer has its own routing control. The interrupts can be routed to various interrupts in the I/O APIC. T[2:0]C.IRC indicates which interrupts are valid options for routing. If a timer is set for edge-triggered mode, the timers should not be shared with any other interrupts.

28.2 References

IA-PC HPET (High Precision Event Timers) Specification, Revision 1.0a: http://www.intel.com/hardware design/hpetspec_1.pdf

28.3 Register Map

28.4 Memory Mapped Registers

The register space is memory mapped to a 1K block at address FED00000h. All registers are in the core well. Accesses that cross register boundaries result in undefined behavior.

28.5 PCU iLB High Performance Event Timer (HPET) Memory Mapped IO Registers

Table 191. Summary of PCU iLB High Performance Event Timer (HPET) Memory Mapped I/O Registers

Offset	Size	Register ID—Description	Default Value
FED00000h	8	"GCID (HPET_GCID)—Offset FED00000h" on page 1253	0429B17F8086A201h
FED00010h	8	"GCFG (HPET_GCFG)—Offset FED00010h" on page 1254	0000000000000000h
FED00020h	8	"GIS (HPET_GIS)—Offset FED00020h" on page 1255	0000000000000000h
FED000F0h	8	"MCV (HPET_MCV)—Offset FED000F0h" on page 1255	0000000000000000h
FED00100h	8	"T0C (HPET_T0C)—Offset FED00100h" on page 1256	00F0000000000030h
FED00108h	4	"T0CV_L (HPET_T0CV_L)—Offset FED00108h" on page 1257	FFFFFFFFh
FED0010Ch	4	"T0CV_U (HPET_T0CV_U)—Offset FED0010Ch" on page 1257	FFFFFFFFh
FED00120h	8	"T1C (HPET_T1C)—Offset FED00120h" on page 1258	00F0000000000000h
FED00128h	8	"T1CV (HPET_T1CV)—Offset FED00128h" on page 1259	00000000FFFFFFFFh
FED00140h	8	"T2C (HPET_T2C)—Offset FED00140h" on page 1259	00F0080000000000h
FED00148h	8	"T2CV (HPET_T2CV)—Offset FED00148h" on page 1261	00000000FFFFFFFFh

28.5.1 GCID (HPET_GCID)—Offset FED00000h

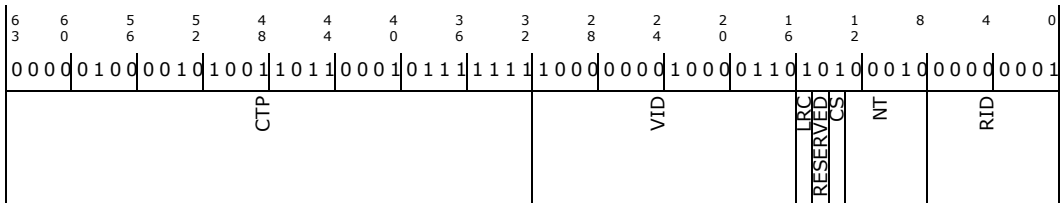
General Capabilities and ID

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_GCID: FED00000h

Default: 0429B17F8086A201h



Bit Range	Default & Access	Description
63:32	0429B17Fh RO	**CTP:** Counter Tick Period (CTP): Indicates a period of 69.841279ns, (14.1318 MHz clock period)
31:16	8086h RO	**VID:** Vendor ID (VID): Value of 8086h indicates Intel.
15	1b RO	**LRC:** Legacy Rout Capable (LRC): Indicates support for Legacy Interrupt Rout.
14	0b RO	**RESERVED:** Reserved.
13	1b RO	**CS:** Counter Size (CS): This bit is set to indicate that the main counter is 64 bits wide.

Bit Range	Default & Access	Description
12:8	02h RO	**NT:** Number of Timers (NT): Indicates that 3 timers are supported.
7:0	01h RO	**RID:** Revision ID (RID): Indicates that revision 1.0 of the specification is implemented.

28.5.2 GCFG (HPET_GCFG)—Offset FED00010h

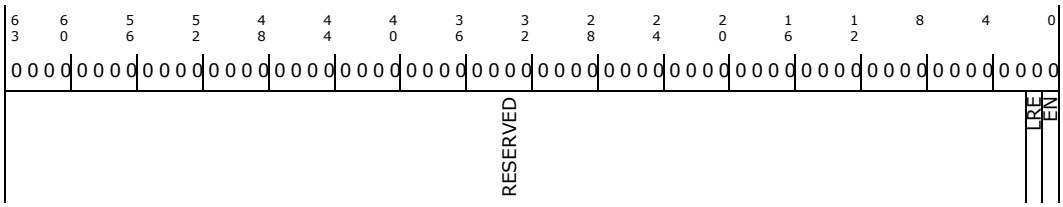
General Configuration

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_GCFG: FED00010h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:2	0b RO	**RESERVED:** Reserved.
1	0b RW	**LRE:** Legacy Rout Enable (LRE): When set, interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in 8259 or IRQ2 in the I/O APIC Timer 1 will be routed to IRQ8 in 8259 and I/O APIC Timer 2 will be routed as per the routing in T2C When set, the T[1:0]C.IR will have no impact for timers 0 and 1.
0	0b RW	**EN:** Overall Enable (EN): When set, the timers can generate interrupts. When cleared, the main counter will halt and no interrupts will be caused by any timer. For level-triggered interrupts, if an interrupt is pending when this bit is cleared, the GIS.Tx will not be cleared.

28.5.3 GIS (HPET_GIS)—Offset FED00020h

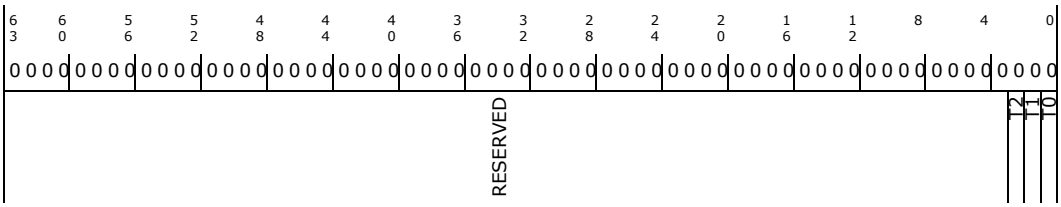
General Interrupt Status

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_GIS: FED00020h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:3	0b RO	**RESERVED:** Reserved.
2	0b RW	**T2:** Timer 2 Status (T2): Same functionality as T0, for timer 2.
1	0b RW	**T1:** Timer 1 Status (T1): Same functionality as T0, for timer 1.
0	0b RW	**T0:** Timer 0 Status (T0): In edge triggered mode, this bit always reads as 0. In level triggered mode, this bit is set when an interrupt is active.

28.5.4 MCV (HPET_MCV)—Offset FED000F0h

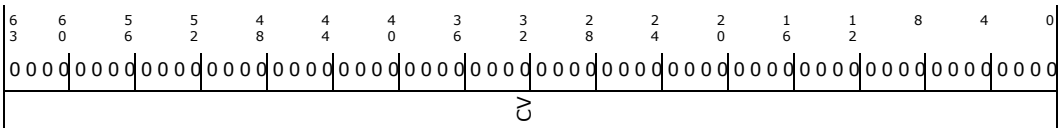
Main Counter Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_MCV: FED000F0h

Default: 0000000000000000h



Bit Range	Default & Access	Description
63:0	0b RW	**CV:** Counter Value (CV): Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

28.5.5 T0C (HPET_T0C)—Offset FED00100h

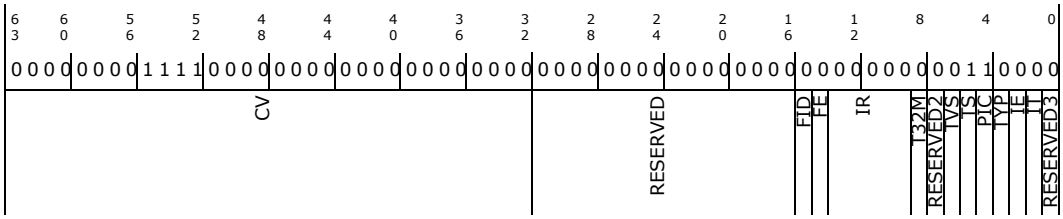
Timer 0 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T0C: FED00100h

Default: 00F0000000000030h



Bit Range	Default & Access	Description
63:32	00f00000h RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0h RO	**RESERVED:** Reserved.
15	0b RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0b RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0b RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this prarticular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0b RW	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0b RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0b RW	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	1b RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	1b RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0b RW	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0b RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0b RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.

Bit Range	Default & Access	Description
0	0b RO	**RESERVED (RESERVED3):** Reserved.

28.5.6 T0CV_L (HPET_T0CV_L)—Offset FED00108h

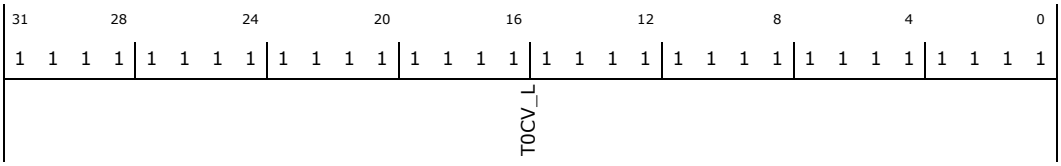
Lower Timer 0 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HPET_T0CV_L: FED00108h

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW	**T0CV_L:** Lower Timer 0 Comperator Value

28.5.7 T0CV_U (HPET_T0CV_U)—Offset FED0010Ch

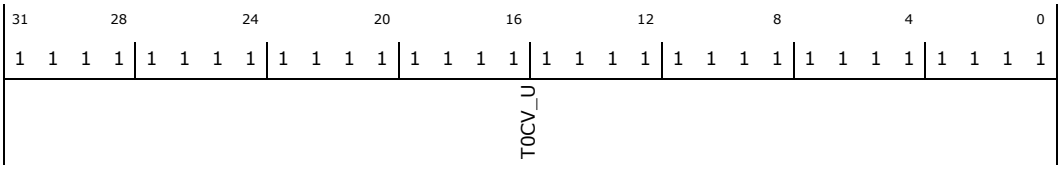
Upper Timer 0 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

HPET_T0CV_U: FED0010Ch

Default: FFFFFFFFh



Bit Range	Default & Access	Description
31:0	FFFFFFFFh RW	**T0CV_U:** Upper Timer 0 Comperator Value

28.5.8 T1C (HPET_T1C)—Offset FED00120h

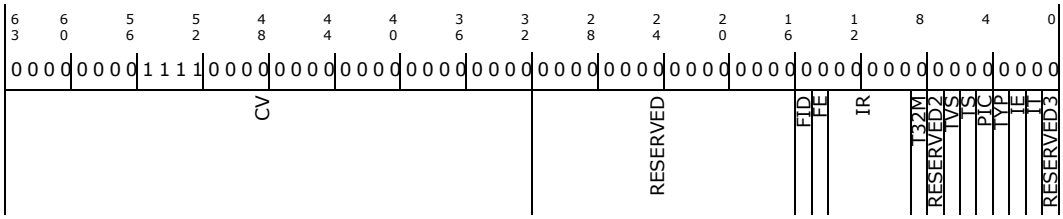
Timer 1 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T1C: FED00120h

Default: 00F0000000000000h



Bit Range	Default & Access	Description
63:32	00f00000h RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0h RO	**RESERVED:** Reserved.
15	0b RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0b RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0b RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this prarticular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0b RO	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0b RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0b RO	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0b RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	0b RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0b RO	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0b RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0b RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.

Bit Range	Default & Access	Description
0	0b RO	**RESERVED (RESERVED3):** Reserved.

28.5.9 T1CV (HPET_T1CV)—Offset FED00128h

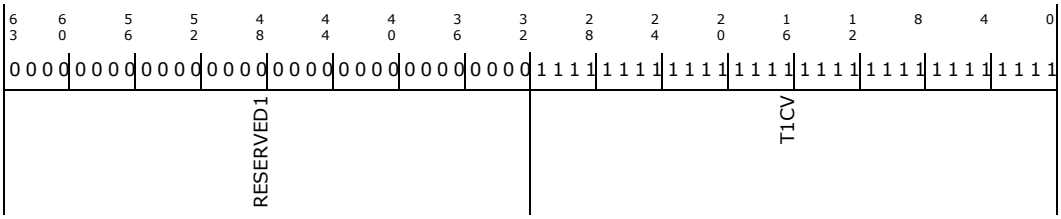
Timer 1 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T1CV: FED00128h

Default: 00000000FFFFFFFFh



Bit Range	Default & Access	Description
63:32	0b RO	**RESERVED (RESERVED1):** Reserved.
31:0	FFFFFFFFh RO	**T1CV:** Timer 1 Comperator Value

28.5.10 T2C (HPET_T2C)—Offset FED00140h

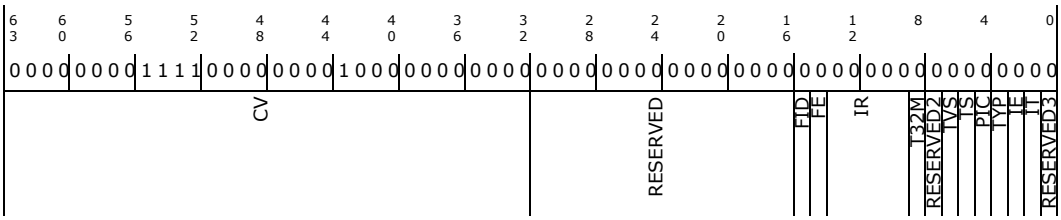
Timer 2 Config and Capabilities

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T2C: FED00140h

Default: 00F0080000000000h



Bit Range	Default & Access	Description
63:32	00f00800h RO	**IRC (CV):** Interrupt Rout Capability (IRC): Indicates I/OxAPIC interrupts the timer can use: Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23 Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	0h RO	**RESERVED:** Reserved.

Bit Range	Default & Access	Description
15	0b RO	**FID:** FSB Interrupt Delivery (FID): Not supported
14	0b RO	**FE:** FSB Enable (FE): Not supported, since FID is not supported.
13:9	0b RW	**IR:** Interrupt Rout (IR): Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this prarticular timer, the value read back will not match what is written. If GCFG.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no effect.
8	0b RO	**T32M:** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
7	0b RO	**RESERVED (RESERVED2):** Timer 32-bit Mode (T32M): When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For timers 1 and 2, this bit is read only '0'.
6	0b RO	**TVS:** Timer Value Set (TVS): This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1 and 2.
5	0b RO	**TS:** Timer Size (TS): 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
4	0b RO	**PIC:** Periodic Interrupt Capable (PIC): When set, hardware supports a periodic mode for this timer's interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
3	0b RO	**TYP:** Timer Type (TYP): If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
2	0b RW	**IE:** Interrupt Enable (IE): When set, enables the timer to cause an interrupt when it times out. When cleared, the timer count and generates status bits, but will not cause an interrupt.
1	0b RW	**IT:** Timer Interrupt Type (IT): When cleared, interrupt is edge triggered. When set, interrupt is level triggered and will be held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
0	0b RO	**RESERVED (RESERVED3):** Reserved.

28.5.11 T2CV (HPET_T2CV)—Offset FED00148h

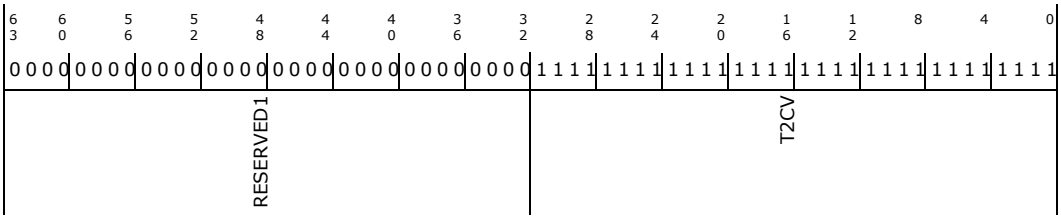
Timer 2 Comperator Value

Access Method

Type: Memory Mapped I/O Register (Size: 64 bits)

HPET_T2CV: FED00148h

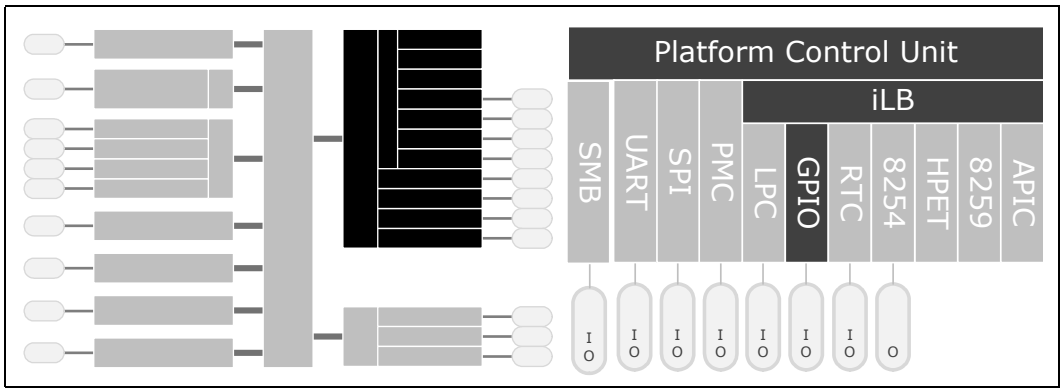
Default: 00000000FFFFFFFFh



Bit Range	Default & Access	Description
63:32	0b RO	**RESERVED (RESERVED1):** Reserved.
31:0	FFFFFFFFh RO	**T2CV:** Timer 2 Comperator Value

29 PCU – iLB – GPIO

There are 102 GPIOs available for use during the S0 ACPI state, and 44 are available for use from S5 to S0 (SUS). Most of these GPIOs can be used as legacy GPIOs through IO registers. This chapter describes their use as legacy GPIOs.



29.1 Signal Descriptions

See Chapter 2, "Physical Interfaces" for additional details.

The signal description table has the following headings:

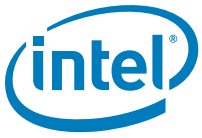
- **Signal Name:** The name of the signal/pin
- **Direction**: The buffer direction can be either input, output, or I/O (bidirectional)
- **Type:** The buffer type found in Chapter 9, "Electrical Specifications"
- **Description**: A brief explanation of the signal's function

Table 192. GPIO Signals

Signal Name	Direction/ Type	Description
GPIO_S0_SC[101:0]	I/O Varies	These GPIO pins are powered and active in S0 only. Many of these are multiplexed with other functions and may have different default pin names.
GPIO_S5[43:0]	I/O Varies	These GPIO pins are powered and active in S5–S0 (SUS). Many of these are multiplexed with other functions and may have different default pin names. Some are used as straps.

29.2 Features

GPIOs can generate general purpose events (GPEs) on rising and/or falling edges.



29.3 Use

Each GPIO has six registers that control how it is used, or report its status:

- Use Select
- I/O Select
- GPIO Level
- Trigger Positive Edge
- Trigger Negative Edge
- Trigger Status

The Use Select register selects a GPIO pin as a GPIO, or leaves it as its programmed function. This register must be set for all other registers to affect the GPIO.

The I/O Select register determines the direction of the GPIO.

The Trigger Positive Edge and Trigger Negative Edge registers enable general purpose events on a rising and falling edge respectively. This only applies to GPIOs set as input.

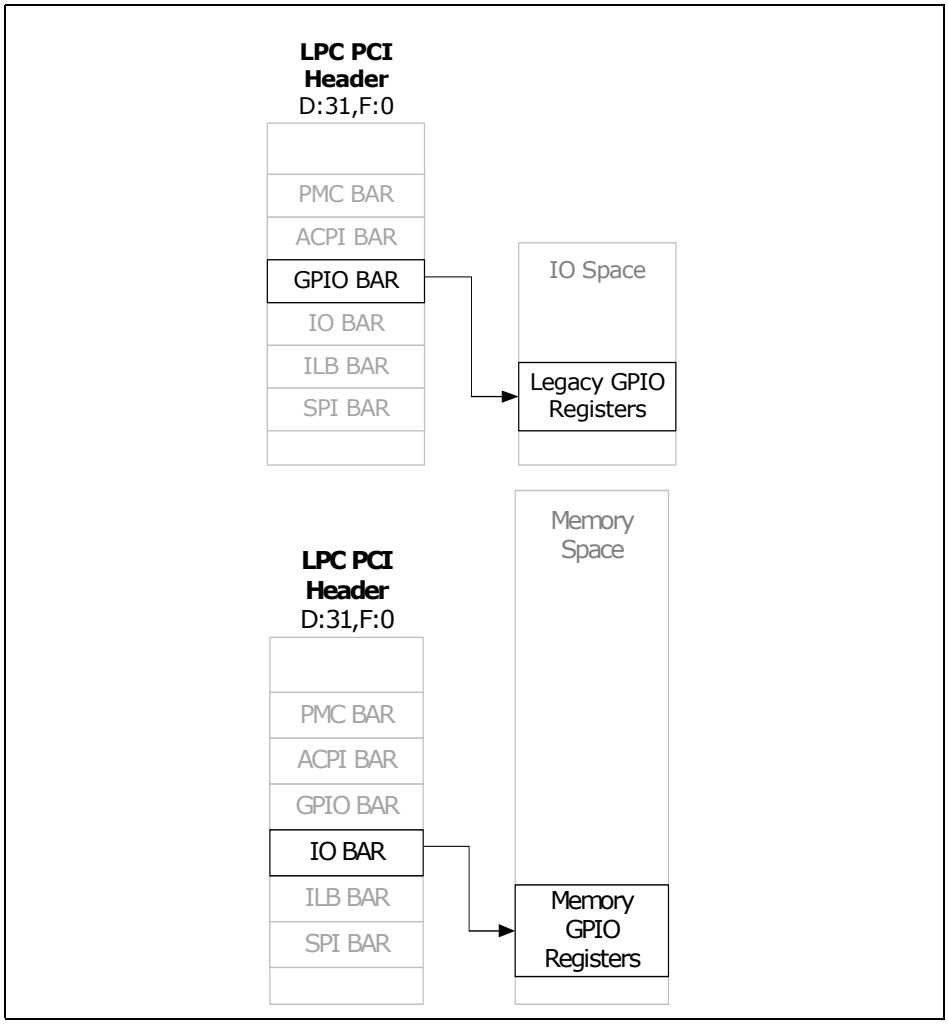
The Trigger Status register is used by software to determine if the GPIO triggered a GPE. This only applies to GPIOs set as input and with one or both of the Trigger modes enabled.

Additionally, there is one additional register for each S5 GPIO:

- Wake Enable

This register allows S5 GPIOs to trigger a wake event based on the Trigger registers' settings.

29.4 Register Map



29.5 GPIO Registers

Registers are broken into two groups: memory mapped and legacy IO registers. Memory mapped registers are used by BIOS and firmware to select the configurable function of the GPIO and setup analog states needed for that function's operation. They are named based on the pin/ball name. Legacy IO registers are the more traditional GPIO control/status type, and are used when the function selected is a traditional GPIO (direction, level, use registers). They are numbered based on the GPIO number.

Each group is further broken down into SCORE (internal partition naming) and SSUS. SCORE are for the GPIOs named GPIO_S0_SC[xxx], while SSUS are for the GPIOs named GPIO_S5[xx].

Note: All GPIO registers must be accessed as double words. Unpredictable results will occur otherwise.

Note: All memory mapped GPIO *_PAD_VAL's must set Ienenb = 0 in order to read the pad_val of the GPIO. This applies to RO GPIOs as well.

Note: vGPIO's are virtual GPIO's for use by software to generate interrupts. They are not tied to physical pins.

Note: When a GPIO is selected via the IO USE_SEL, Memory accesses are denied (pconf0, pconf1 and pad_val).

§

30 PCU – iLB – Interrupt Decoding and Routing

The interrupt decoder is responsible for receiving interrupt messages from other devices in the processor and decoding them for consumption by the interrupt router, the PCU – iLB – 8259 Programmable Interrupt Controllers (PIC) and/or the PCU – iLB – IO APIC.

The interrupt router is responsible for mapping each incoming interrupt to the appropriate PIRQx, for consumption by the PCU – iLB – 8259 Programmable Interrupt Controllers (PIC) and/or PCU – iLB – IO APIC.

30.1 Features

30.1.1 Interrupt Decoder

The interrupt decoder receives interrupt messages from devices in the processor. These interrupts can be split into two primary groups:

- For consumption by the interrupt router
- For consumption by the 8259 PIC

30.1.1.1 For Consumption by the Interrupt Router

When a PCI-mapped device in the processor asserts or de-asserts an INT[A:D] interrupt, an interrupt message is sent to the decoder. This message is decoded to indicate to the interrupt router which specific interrupt is asserted or de-asserted and which device the INT[A:D] interrupt originated from.

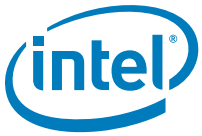
30.1.1.2 For Consumption by the 8259 PIC

When a device in the processor asserts or de-asserts a legacy interrupt (IRQ), an interrupt message is sent to the decoder. This message is decoded to indicate to the 8259 PIC which specific interrupt (IRQ[3, 4, 14 or 15]) was asserted or de-asserted.

30.1.2 Interrupt Router

The interrupt router aggregates the INT[A:D] interrupts for each PCI-mapped device in the processor, received from the interrupt decoder, and the INT[A:D] interrupts direct from the Serialized IRQ controller. It then maps these aggregated interrupts to 8 PCI based interrupts: PIRQ[A:H]. This mapping is configured using the IR[31:0] registers.

PCI based interrupts PIRQ[A:H] are then available for consumption by either the 8259 PICs or the IO-APIC, depending on the configuration of the 8 PIRQx Routing Control Registers: PIRQA, PIQRB, PIRQC, PIRQD, PIRQE, PIRQF, PIRQG, PIRQH.



30.1.2.1 Routing PCI Based Interrupts to 8259 PIC

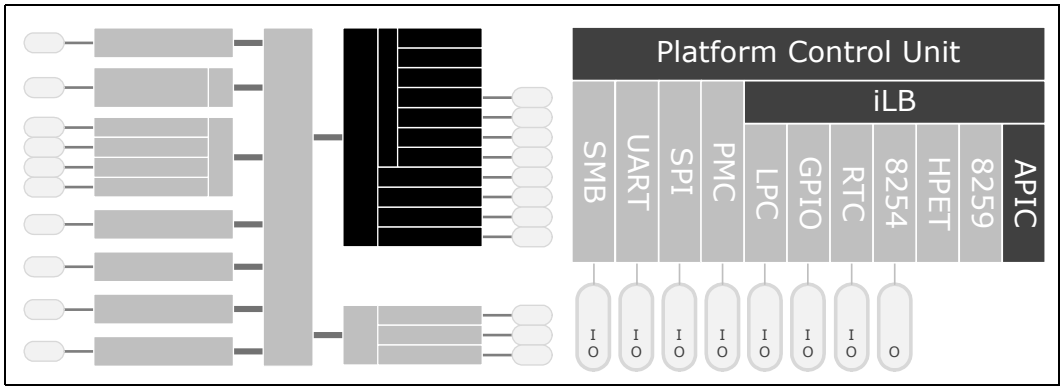
The interrupt router can be programmed to allow PIRQA-PIRQH to be routed internally to the 8259 as ISA compatible interrupts IRQ 3–7, 9–12 & 14–15. The assignment is programmable through the 8 PIRQx Routing Control Registers: PIRQA, PIQRB, PIRQC, PIRQD, PIRQE, PIRQF, PIRQG, PIRQH. One or more PIRQs can be routed to the same IRQ input. If ISA Compatible Interrupts are not required, the Route registers can be programmed to disable steering.

The PIRQx# lines are defined as active low, level sensitive. When a PIRQx# is routed to specified IRQ line, software must change the IRQ's corresponding ELCR bit to level sensitive mode. The processor internally inverts the PIRQx# line to send an active high level to the PIC. When a PCI interrupt is routed onto the PIC, the selected IRQ can no longer be used by an active high device (through SERIRQ). However, active low interrupts can share their interrupt with PCI interrupts.

§

31 PCU – iLB – IO APIC

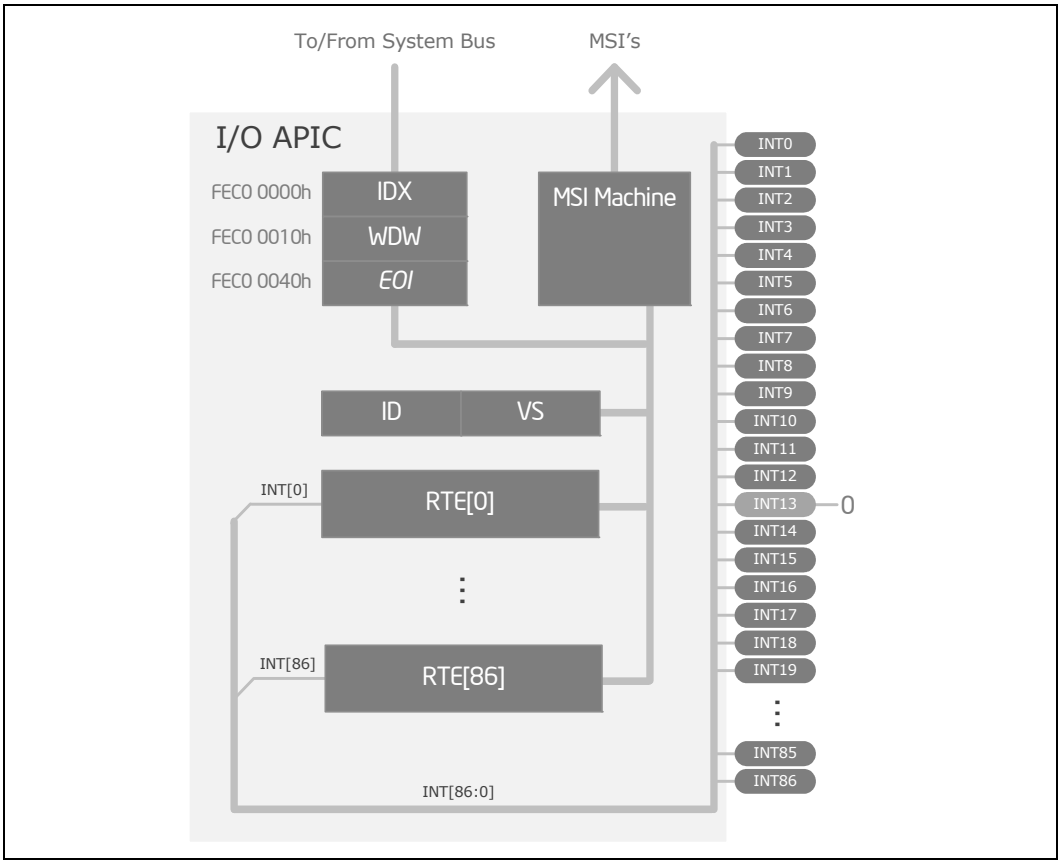
The IO Advanced Programmable Interrupt Controller (APIC) is used to support line interrupts more flexibly than the 8259 PIC. Line interrupts are routed to it from multiple sources, including legacy devices, using the interrupt decoder and serial IRQs, or they are routed to it from the interrupt router in the iLB. These line based interrupts are then used to generate interrupt messages targeting the local APIC in the processor.



31.1 Features

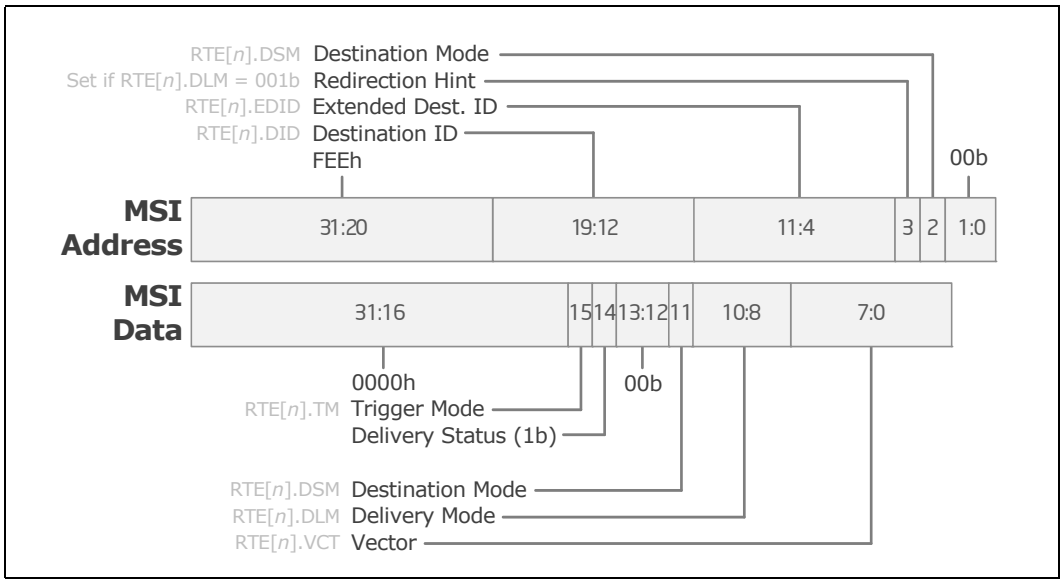
- 87 interrupt lines
  - — IRQ0-86
- Edge or level trigger mode per interrupt
- Active low or high polarity per interrupt
- Works with local APIC in processor via MSIs
- MSIs can target specific processor core
- Established APIC programming model

Figure 35. Detailed Block Diagram



MSIs generated by the I/O APIC are sent as 32-bit memory writes to the Local APIC. The address and data of the write transaction are used as follows.

Figure 36. MSI Address and Data



Destination ID (DID) and Extended Destination ID (EDID) are used to target a specific processor core's local APIC.

31.2 Use

The I/O APIC contains indirectly accessed I/O APIC registers and normal memory mapped registers. There are three memory mapped registers:

- Index Register (IDX)
- Window Register (WDW)
- End Of Interrupt Register (EOI)

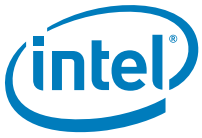
The Index register selects an indirect I/O APIC register (ID/VS/RTE[*n*]) to appear in the Window register.

The Window register is used to read or write the indirect register selected by the Index register.

The EOI register is written to by the Local APIC in the processor. The I/O APIC compares the lower eight bits written to the EOI register to the Vector set for each interrupt (RTE.VCT). All interrupts that match this vector will have their RTE.RIRR register cleared. All other EOI register bits are ignored.

31.3 References

TBD



31.4 Indirect I/O APIC Registers

These registers are selected with the IDX register, and read/written through the WDW register. Accessing these registers must be done as DW requests; otherwise, unspecified behavior will result. Software should not attempt to write to reserved registers. Reserved registers may return non-zero values when read.

Note: There is one pair of redirection (RTE) registers per interrupt line. Each pair forms a 64-bit RTE register.

Note: Specified offsets should be placed in IDX, not added to IDX.

31.5 PCU iLB IO APIC Memory Mapped I/O Registers

Table 193. Summary of PCU iLB I/O APIC Memory Mapped I/O Registers

Offset	Size	Register ID—Description	Default Value
FEC00000h	1	"IDX (IOAPIC_IDX)—Offset FEC00000h" on page 1272	00h
FEC00010h	4	"WDW (IOAPIC_WDW)—Offset FEC00010h" on page 1272	00000000h
FEC00040h	4	"EOI (IOAPIC_EOI)—Offset FEC00040h" on page 1273	00000000h

31.5.1 IDX (IOAPIC_IDX)—Offset FEC00000h

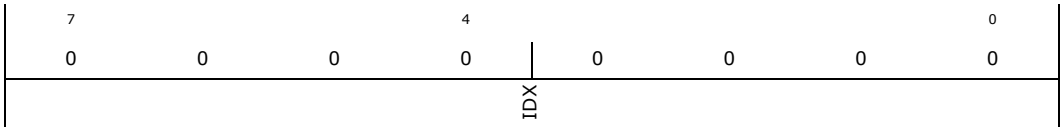
Index Register

Access Method

Type: Memory Mapped I/O Register (Size: 8 bits)

IOAPIC_IDX: FEC00000h

Default: 00h



Bit Range	Default & Access	Description
7:0	0h RW	**IDX:** This 8-bit register selects which indirect register appears in the window register to be manipulated by software. Software will program this register to select the desired APIC internal register.

31.5.2 WDW (IOAPIC_WDW)—Offset FEC00010h

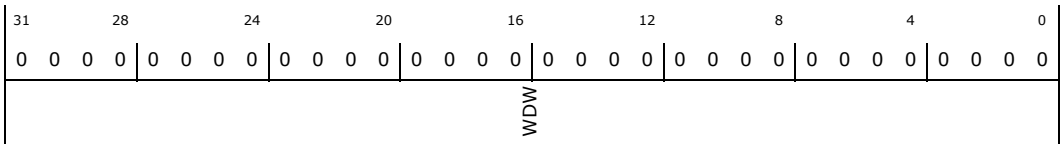
Window Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IOAPIC_WDW: FEC00010h

Default: 00000000h



Bit Range	Default & Access	Description
31:0	0h RW	**WDW:** This 32-bit register specifies the data to be read or written to the register pointed to by the IDX register. This register can be accessed only in DW quantities.

31.5.3 EOI (IOAPIC_EOI)—Offset FEC00040h

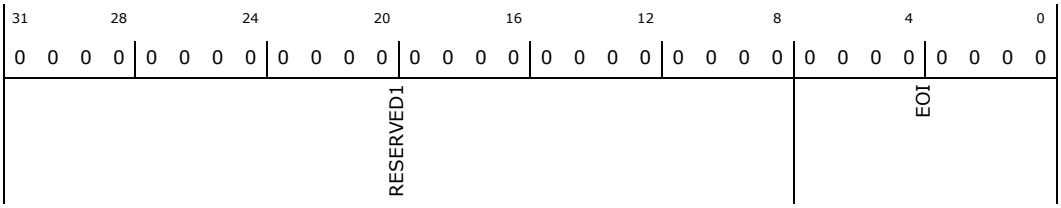
EOI Register

Access Method

Type: Memory Mapped I/O Register (Size: 32 bits)

IOAPIC_EOI: FEC00040h

Default: 00000000h

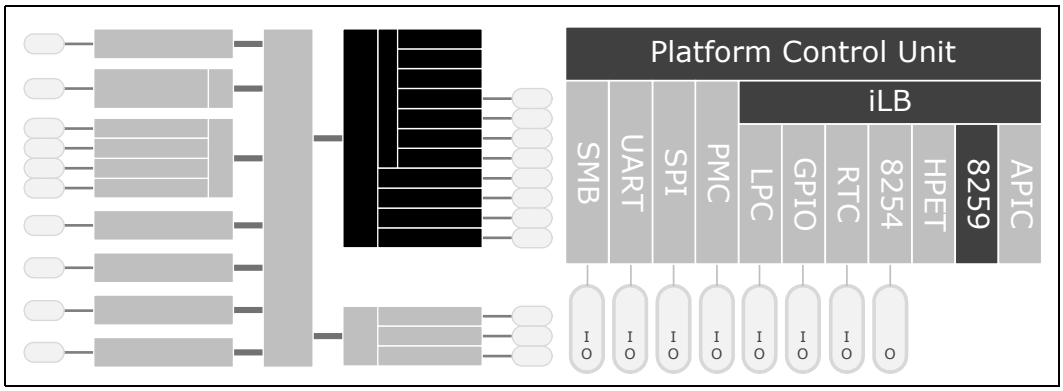


Bit Range	Default & Access	Description
31:8	0b WO	**RESERVED (RESERVED1):** Reserved.
7:0	0h WO	**EOI:** When a write is issued to this register, the IOxAPIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry will be cleared. If multiple entries have the same vector, each of those entries will have RTE.RIRR cleared.

§ §

32 PCU – iLB – 8259 Programmable Interrupt Controllers (PIC)

The processor provides an ISA-compatible programmable interrupt controller (PIC) that incorporates the functionality of two, cascaded 8259 interrupt controllers.



32.1 Features

In addition to providing support for ISA compatible interrupts, this interrupt controller can also support PCI-based interrupts (PIRQs) by mapping the PCI interrupt onto a compatible ISA interrupt line. Each 8259 controller supports eight interrupts, numbered 0–7. Table 194 shows how the controllers are connected.

Note: The processor does not implement any external PIRQ# signals. The PIRQs referred to in this chapter originate from the interrupt routing unit.

Table 194. Interrupt Controller Connections (Sheet 1 of 2)

8259	8259 Input	Connected Pin / Function
Master	0	Internal Timer / Counter 0 output or HPET #0; determined by GCFG.LRE register bit
	1	IRQ1 using SERIRQ, Keyboard Emulation
	2	Slave controller INTR output
	3	IRQ3 via SERIRQ, PIRQx or PCU UART 1
	4	IRQ4 via SERIRQ or PIRQx
	5	IRQ5 via SERIRQ or PIRQx
	6	IRQ6 via SERIRQ or PIRQx
	7	IRQ7 via SERIRQ or PIRQx

Table 194. Interrupt Controller Connections (Sheet 2 of 2)

8259	8259 Input	Connected Pin / Function
Slave	0	Inverted IRQ8# from internal RTC or HPET
	1	IRQ9 via SERIRQ, SCI or PIRQx
	2	IRQ10 via SERIRQ, SCI or PIRQx
	3	IRQ11 via SERIRQ, SCI, HPET or PIRQx
	4	IRQ12 via SERIRQ, PIRQx or mouse emulation
	5	None
	6	PIRQx or IRQ14 from SATA controller
	7	IRQ15 via SERIRQ or PIRQx or IRQ15 from SATA controller

The processor cascades the slave controller onto the master controller through master controller interrupt input 2. This means there are only 15 possible interrupts for the processor PIC.

Interrupts can be programmed individually to be edge or level, except for IRQ0, IRQ2, and IRQ8#.

Note: Active-low interrupt sources (such as a PIRQ#) are inverted inside the processor. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term “high” indicates “active,” which means “low” on an originating PIRQ#.

32.1.1 Interrupt Handling

32.1.1.1 Generating Interrupts

The PIC interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. Table 195 defines the IRR, ISR, and IMR.

Table 195. Interrupt Status Registers

Bit	Description
IRR	**Interrupt Request Register.** This bit is set on a low-to-high transition of the interrupt line in edge mode, and by an active high level in level mode.
ISR	**Interrupt Service Register.** This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.
IMR	**Interrupt Mask Register.** This bit determines whether an interrupt is masked. Masked interrupts will not generate INTR.

32.1.1.2 Acknowledging Interrupts

The processor generates an interrupt acknowledge cycle that is translated into a Interrupt Acknowledge Cycle to the processor. The PIC translates this command into two internal INTA# pulses expected by the 8259 controllers. The PIC uses the first

internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the master or slave sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon the ICW2.IVBA bits, combined with the ICW2.IRL bits representing the interrupt within that controller.

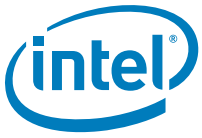
Note: References to ICWx and OCWx registers are relevant to both the master and slave 8259 controllers.

Table 196. Content of Interrupt Vector Byte

Master, Slave Interrupt	Bits [7:3]	Bits [2:0]
IRQ7,15	ICW2.IVBA	111
IRQ6,14		110
IRQ5,13		101
IRQ4,12		100
IRQ3,11		011
IRQ2,10		010
IRQ1,9		001
IRQ0,8		000

32.1.1.3 Hardware/Software Interrupt Sequence

1. One or more of the Interrupt Request lines (IRQ) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
2. The PIC sends INTR active to the processor if an asserted interrupt is not masked.
3. The processor acknowledges the INTR and responds with an interrupt acknowledge cycle.
4. Upon observing the special cycle, the processor converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a slave identification code is broadcast by the master to the slave on a private, internal three bit wide bus. The slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
6. Upon receiving the second internally generated INTA# pulse, the PIC returns the interrupt vector. If no interrupt request is present because the request was too short in duration, the PIC returns vector 7 from the master controller.
7. This completes the interrupt cycle. In AEOI mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.



32.1.2 Initialization Command Words (ICWx)

Before operation can begin, each 8259 must be initialized. In the processor, this is a four-byte sequence. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

The base address for each 8259 initialization command word is a fixed location in the I/O memory space: 20h for the master controller, and A0h for the slave controller.

32.1.2.1 ICW1

A write to the master or slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, the PIC expects three more byte writes to 21h for the master controller, or A1h for the slave controller, to complete the ICW sequence.

A write to ICW1 starts the initialization sequence during which the following automatically occur:

1. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.
2. The Interrupt Mask Register is cleared.
3. IRQ7 input is assigned priority 7.
4. The slave mode address is set to 7.
5. Special mask mode is cleared and Status Read is set to IRR.

32.1.2.2 ICW2

The second write in the sequence (ICW2) is programmed to provide bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

32.1.2.3 ICW3

The third write in the sequence (ICW3) has a different meaning for each controller.

- For the master controller, ICW3 is used to indicate which IRQ input line is used to cascade the slave controller. Within the processor, IRQ2 is used. Therefore, MICW3.CCC is set to a 1, and the other bits are set to 0s.
- For the slave controller, ICW3 is the slave identification code used during an interrupt acknowledge cycle. On interrupt acknowledge cycles, the master controller broadcasts a code to the slave controller if the cascaded interrupt won arbitration on the master controller. The slave controller compares this identification code to the value stored in its ICW3, and if it matches, the slave controller assumes responsibility for broadcasting the interrupt vector.

32.1.2.4 ICW4

The final write in the sequence (ICW4) must be programmed for both controllers. At the very least, ICW4.MM must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

32.1.3 Operation Command Words (OCW)

These command words reprogram the Interrupt controller to operate in various interrupt modes.

- OCW1 masks and unmasks interrupt lines.
- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function.
- OCW3 sets up ISR/IRR reads, enables/disables the special mask mode (SMM), and enables/disables polled interrupt mode.

32.1.4 Modes of Operation

32.1.4.1 Fully Nested Mode

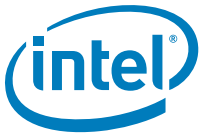
In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the processor issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels generate another interrupt.

Interrupt priorities can be changed in the rotating priority mode.

32.1.4.2 Special Fully-Nested Mode

This mode is used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully-nested mode is programmed to the master controller. This mode is similar to the fully-nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority interrupts within the slave are recognized by the master and initiate interrupts to the processor. In the normal-nested mode, a slave is masked out when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a Non-Specific EOI command to the slave and then reading its ISR. If it is 0, a non-specific EOI can also be sent to the master.



32.1.4.3 Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt has to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2.REOI; the Rotation on Non-Specific EOI Command (OCW2.REOI=101b) and the rotate in automatic EOI mode which is set by (OCW2.REOI=100b).

32.1.4.4 Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 is the highest priority device. The Set Priority Command is issued in OCW2 to accomplish this, where: OCW2.REOI=11xb, and OCW2.ILS is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (OCW2.REOI=111b) and OCW2.ILS=IRQ level to receive bottom priority.

32.1.4.5 Poll Mode

Poll mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command. Poll mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting OCW3.PMC. The PIC treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read contains a 1 in Bit 7 if there is an interrupt, and the binary code of the highest priority level in Bits 2:0.

32.1.4.6 Edge and Level Triggered Mode

In ISA systems this mode is programmed using ICW1.LTIM, which sets level or edge for the entire controller. In the processor, this bit is disabled and a register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/Level control Registers ELCR1 and ELCR2.

If an ELCR bit is 0, an interrupt request will be recognized by a low-to-high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector is returned.

32.1.5 End of Interrupt (EOI) Operations

An EOI can occur in one of two fashions: by a command word write issued to the PIC before returning from a service routine, the EOI command; or automatically when the ICW4.AEOI bit is set to 1.

32.1.5.1 Normal End of Interrupt

In normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non-Specific. When a Non-Specific EOI command is issued, the PIC clears the highest ISR bit of those that are set to 1. Non-Specific EOI is the normal mode of operation of the PIC within the processor, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the PIC is operated in modes that preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI.

An ISR bit that is masked is not cleared by a Non-Specific EOI if the PIC is in the special mask mode. An EOI command must be issued for both the master and slave controller.

32.1.5.2 Automatic End of Interrupt Mode

In this mode, the PIC automatically performs a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single PIC. The AEOI mode can only be used in the master controller and not the slave controller.

Note: Both the master and slave PICs have an AEOI bit: MICW4.AEOI and SICW4.AEOI respectively. Only the MICW4.AEOI bit should be set by software. The SICW4.AEOI bit should not be set by software.

32.1.6 Masking Interrupts

32.1.6.1 Masking on an Individual Interrupt Request

Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the master controller masks all requests for service from the slave controller.

32.1.6.2 Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The special mask mode enables all interrupts not masked by a bit set in the Mask register. Normally, when an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the special mask mode, any interrupts may be selectively enabled by loading the Mask Register with the appropriate pattern.

The special mask mode is set by OCW3.ESMM=1b & OCW3.SMM=1b, and cleared where OCW3.ESMM=1b & OCW3.SMM=0b.

32.2 IO Mapped Registers

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ0 - 7), and at A0h and A1h for the slave controller (IRQ8 - 13). These registers have multiple functions, depending upon the data written to them. Table 197 is a description of the different register possibilities for each address.

Note: The register descriptions after Table 197 represent one register possibility.

Table 197. I/O Registers Alias Locations (Sheet 1 of 2)

Registers	Original I/O Location	Alias I/O Locations
MICW1	20h	24h
MOCW2		28h
MOCW3		2Ch
		30h
		34h
		38h
		3Ch

Table 197. I/O Registers Alias Locations (Sheet 2 of 2)

Registers	Original I/O Location	Alias I/O Locations
MICW2 MICW3 MICW4 MOCW1	21h	25h
		29h
		2Dh
		31h
		35h
		39h
		3Dh
SICW1 SOCW2 SOCW3	A0h	A4h
		A8h
		ACh
		B0h
		B4h
		B8h
		BCh
SICW2 SICW3 SICW4 SOCW1	A1h	A5h
		A9h
		ADh
		B1h
		B5h
		B9h
		BDh
ELCR1	4D0h	N/A
ELCR2	4D1h	N/A

32.3 PCU iLB 8259 Interrupt Controller (PIC) I/O Registers

Table 198. Summary of PCU iLB 8259 Interrupt Controller (PIC) I/O Registers

Offset	Size	Register ID—Description	Default Value
20h	1	"MICW1—Offset 20h" on page 1283	00h
21h	1	"MICW2—Offset 21h" on page 1284	00h
24h	1	"MOCW2—Offset 24h" on page 1285	20h
25h	1	"MICW3—Offset 25h" on page 1285	00h
28h	1	"MOCW3—Offset 28h" on page 1286	22h
29h	1	"MICW4—Offset 29h" on page 1287	01h
2Dh	1	"MOCW1—Offset 2Dh" on page 1287	00h
A0h	1	"SICW1—Offset A0h" on page 1288	00h
A1h	1	"SICW2—Offset A1h" on page 1289	00h
A4h	1	"SOCW2—Offset A4h" on page 1289	20h
A5h	1	"SICW3—Offset A5h" on page 1290	00h
A8h	1	"SOCW3—Offset A8h" on page 1291	22h
A9h	1	"SICW4—Offset A9h" on page 1292	01h
ADh	1	"SOCW1—Offset ADh" on page 1292	00h
4D0h	1	"ELCR1—Offset 4D0h" on page 1293	00h
4D1h	1	"ELCR2—Offset 4D1h" on page 1293	00h

32.3.1 MICW1—Offset 20h

Master Initialization Command Word 1.A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs: * The Interrupt Mask register is cleared. * IRQ7 input is assigned priority 7. * The slave mode address is set to 7. * Special Mask Mode is cleared and Status Read is set to IRR. Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: I/O Register
(Size: 8 bits)

MICW1: 20h

Default: 00h

7			4				0
0	0	0	0	0	0	0	0
MCS85			ICWOCWSEL	LTIM	ADI	SNGL	IC4

Bit Range	Default & Access	Description
7:5	X WO	**MCS85:** These bits are MCS-85 specific, and not needed. Should be programmed to 000

Bit Range	Default & Access	Description
4	X WO	**ICWOCWSEL:** ICW/OCW select: This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	X WO	**LTIM:** Edge/Level Bank Select (LTIM): Disabled. Replaced by ELCR1 and ELCR2.
2	X WO	**ADI:** ADI. Ignored for VLV. Should be programmed to 0.
1	X WO	**SNGL:** Single or Cascade (SNGL): Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	X WO	**IC4:** wICW4 Write Required (IC4): This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

32.3.2 MICW2—Offset 21h

Master ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: I/O Register (Size: 8 bits)

MICW2: 21h

Default: 00h

7				4				0
0	0	0	0	0	0	0	0	
IVBA						IRL		

Bit Range	Default & Access	Description
7:3	X WO	**IVBA:** Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	X WO	**IRL:** Interrupt Request Level: When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

32.3.3 MOCW2—Offset 24h

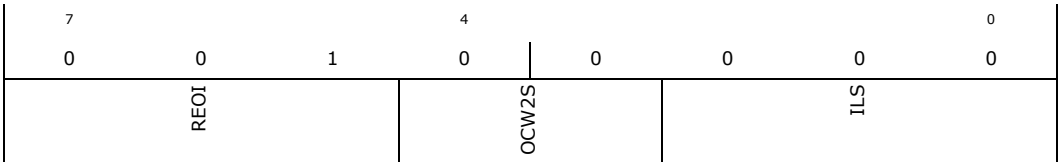
Master Operational Control Word 2 (Interrupt Mask).Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: I/O Register
(Size: 8 bits)

MOCW2: 24h

Default: 20h



Bit Range	Default & Access	Description
7:5	001b WO	**REOI:** Rotate and EOI Codes: R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 - Rotate in Auto EOI Mode (Clear) 001 - Non-specific EOI command 010 - No Operation 011 - *Specific EOI Command 100 - Rotate in Auto EOI Mode (Set) 101 - Rotate on Non-Specific EOI Command 110 - *Set Priority Command 111 - *Rotate on Specific EOI Command *L0 - L2 Are Used
4:3	X WO	**OCW2S:** OCW2 Select: When selecting OCW2, bits 4:3 = 00
2:0	X WO	**ILS:** Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. Bits Interrupt Level Bits Interrupt Level 000 IRQ0/8 100 IRQ4/12 001 IRQ1/9 101 IRQ5/13 010 IRQ2/10 110 IRQ6/14 011 IRQ3/11 111 IRQ7/15

32.3.4 MICW3—Offset 25h

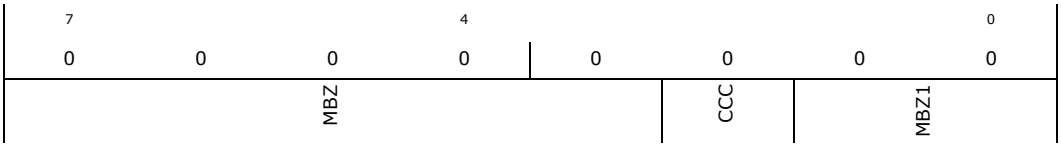
Master Initialization Command Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

MICW3: 25h

Default: 00h



Bit Range	Default & Access	Description
7:3	X WO	**MBZ:** These bits must be programmed to zero.
2	X WO	**CCC:** Cascaded Controller Connection (CCC): This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 15 is cascaded on IRQ2.

Bit Range	Default & Access	Description
1:0	X WO	**MBZ (MBZ1):** These bits must be programmed to zero.

32.3.5 MOCW3—Offset 28h

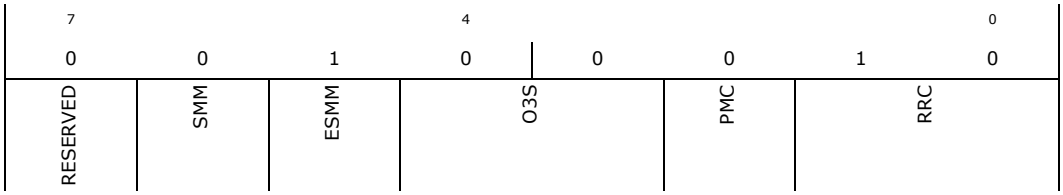
Master Operational Control Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

MOCW3: 28h

Default: 22h



Bit Range	Default & Access	Description
7	0b RO	**RESERVED:** Reserved. Must be 0.
6	0b WO	**SMM:** Special Mask Mode (SMM): If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	1b WO	**ESMM:** Enable Special Mask Mode (ESMM): When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a don't care.
4:3	X WO	**O3S:** OCW3 Select (O3S): When selecting OCW3, bits 4:3 = 01
2	X WO	**PMC:** Poll Mode Command (PMC): When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	10b WO	**RRC:** Register Read Command (RRC): These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be read IRR. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

32.3.6 MICW4—Offset 29h

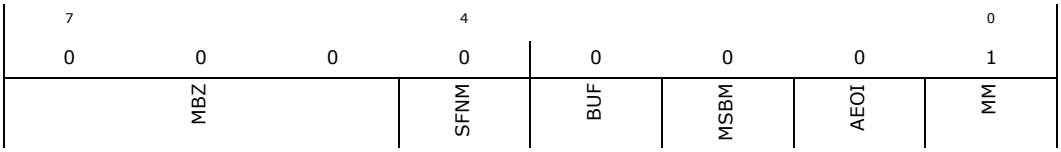
Master Initialization Command Word 4

Access Method

Type: I/O Register
(Size: 8 bits)

MICW4: 29h

Default: 01h



Bit Range	Default & Access	Description
7:5	X WO	**MBZ:** These bits must be programmed to zero.
4	0b WO	**SFNM:** Special Fully Nested Mode (SFNM): Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0b WO	**BUF:** Buffered Mode (BUF): Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0b WO	**MSBM:** Master/Slave in Buffered Mode (MSBM): Not used. Should always be programmed to 0.
1	0b WO	**AEOI:** Automatic End of Interrupt (AEOI): This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	1b WO	**MM:** Microprocessor Mode (MM): This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.

32.3.7 MOCW1—Offset 2Dh

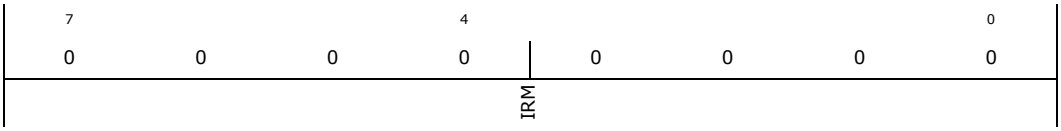
Master Operational Control Word 1 (Interrupt Mask)

Access Method

Type: I/O Register
(Size: 8 bits)

MOCW1: 2Dh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**IRM:** Interrupt Request Mask (IRM): When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

32.3.8 SICW1—Offset A0h

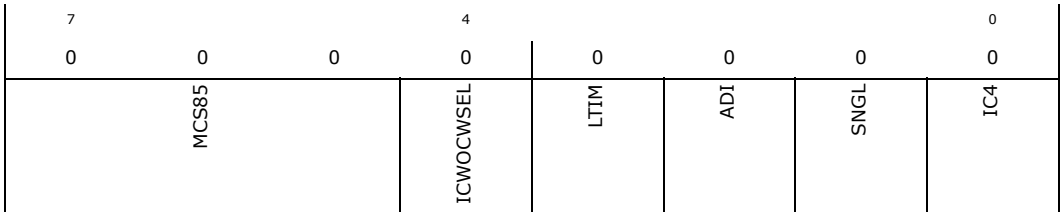
Slave Initialization Command Word 1.A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs: * The Interrupt Mask register is cleared. * IRQ7 input is assigned priority 7. * The slave mode address is set to 7. * Special Mask Mode is cleared and Status Read is set to IRR. Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Access Method

Type: I/O Register
(Size: 8 bits)

SICW1: A0h

Default: 00h



Bit Range	Default & Access	Description
7:5	X WO	**MCS85:** These bits are MCS-85 specific, and not needed. Should be programmed to 000
4	X WO	**ICWOCWSEL:** ICW/OCW select: This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	X WO	**LTIM:** Edge/Level Bank Select (LTIM): Disabled. Replaced by ELCR1 and ELCR2.
2	X WO	**ADI:** ADI. Ignored for VLV. Should be programmed to 0.
1	X WO	**SNGL:** Single or Cascade (SNGL): Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	X WO	**IC4:** wICW4 Write Required (IC4): This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

32.3.9 SICW2—Offset A1h

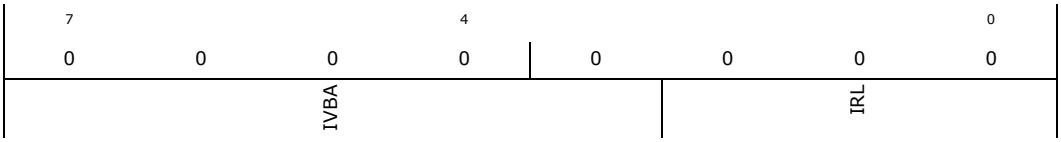
Slave ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Access Method

Type: I/O Register
(Size: 8 bits)

SICW2: A1h

Default: 00h



Bit Range	Default & Access	Description
7:3	X WO	**IVBA:** Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.
2:0	X WO	**IRL:** Interrupt Request Level: When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code: Code Master Interrupt Slave Interrupt 000 IRQ0 IRQ8 001 IRQ1 IRQ9 010 IRQ2 IRQ10 011 IRQ3 IRQ11 100 IRQ4 IRQ12 101 IRQ5 IRQ13 110 IRQ6 IRQ14 111 IRQ7 IRQ15

32.3.10 SOCW2—Offset A4h

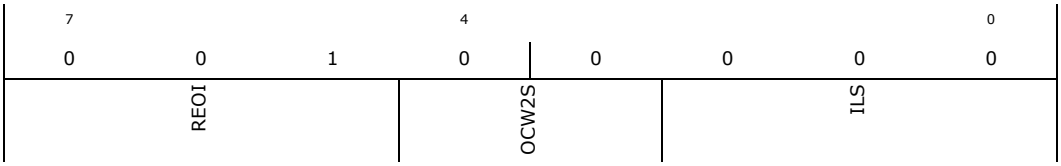
Slave Operational Control Word 2 (Interrupt Mask).Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Access Method

Type: I/O Register
(Size: 8 bits)

SOCW2: A4h

Default: 20h



Bit Range	Default & Access	Description
7:5	001b WO	**REOI:** Rotate and EOI Codes: R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition. 000 - Rotate in Auto EOI Mode (Clear) 001 - Non-specific EOI command 010 - No Operation 011 - *Specific EOI Command 100 - Rotate in Auto EOI Mode (Set) 101 - Rotate on Non-Specific EOI Command 110 - *Set Priority Command 111 - *Rotate on Specific EOI Command *L0 - L2 Are Used

Bit Range	Default & Access	Description
4:3	X WO	**OCW2S:** OCW2 Select: When selecting OCW2, bits 4:3 = 00
2:0	X WO	**ILS:** Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case. Bits Interrupt Level Bits Interrupt Level 000 IRQ0/8 100 IRQ4/12 001 IRQ1/9 101 IRQ5/13 010 IRQ2/10 110 IRQ6/14 011 IRQ3/11 111 IRQ7/15

32.3.11 SICW3—Offset A5h

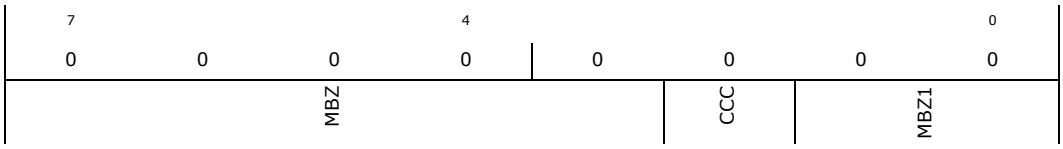
Slave Initialization Command Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

SICW3: A5h

Default: 00h



Bit Range	Default & Access	Description
7:3	X WO	**MBZ:** These bits must be programmed to zero.
2	X WO	**CCC:** Cascaded Controller Connection (CCC): This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 15 is cascaded on IRQ2.
1:0	X WO	**MBZ (MBZ1):** These bits must be programmed to zero.

32.3.12 SOCW3—Offset A8h

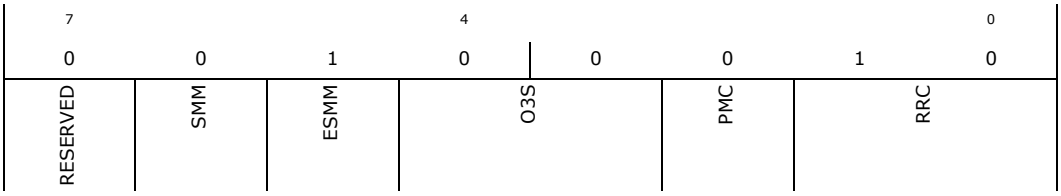
Slave Operational Control Word 3

Access Method

Type: I/O Register
(Size: 8 bits)

SOCW3: A8h

Default: 22h



Bit Range	Default & Access	Description
7	0b RO	**RESERVED:** Reserved. Must be 0.
6	0b WO	**SMM:** Special Mask Mode (SMM): If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.
5	1b WO	**ESMM:** Enable Special Mask Mode (ESMM): When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a don't care.
4:3	X WO	**O3S:** OCW3 Select (O3S): When selecting OCW3, bits 4:3 = 01
2	X WO	**PMC:** Poll Mode Command (PMC): When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	10b WO	**RRC:** Register Read Command (RRC): These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 will not affect the register read selection. Following ICW initialization, the default OCW3 port address read will be read IRR. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

32.3.13 SICW4—Offset A9h

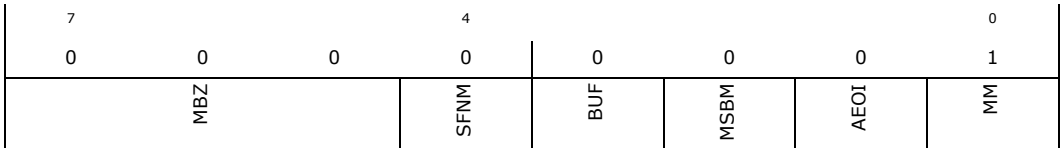
Slave Initialization Command Word 4

Access Method

Type: I/O Register
(Size: 8 bits)

SICW4: A9h

Default: 01h



Bit Range	Default & Access	Description
7:5	X WO	**MBZ:** These bits must be programmed to zero.
4	0b WO	**SFNM:** Special Fully Nested Mode (SFNM): Should normally be disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
3	0b WO	**BUF:** Buffered Mode (BUF): Must be cleared for non-buffered mode. Writing 1 will result in undefined behavior.
2	0b WO	**MSBM:** Master/Slave in Buffered Mode (MSBM): Not used. Should always be programmed to 0.
1	0b WO	**AEOI:** Automatic End of Interrupt (AEOI): This bit should normally be programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
0	1b WO	**MM:** Microprocessor Mode (MM): This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 will result in undefined behavior.

32.3.14 SOCW1—Offset ADh

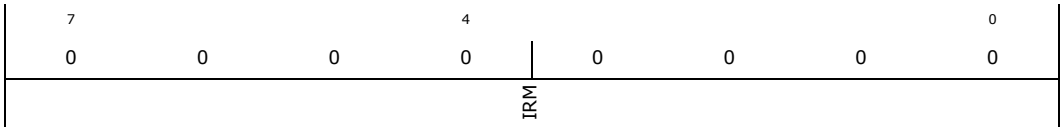
Slave Operational Control Word 1 (Interrupt Mask)

Access Method

Type: I/O Register
(Size: 8 bits)

SOCW1: ADh

Default: 00h



Bit Range	Default & Access	Description
7:0	00h RW	**IRM:** Interrupt Request Mask (IRM): When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

32.3.15 ELCR1—Offset 4D0h

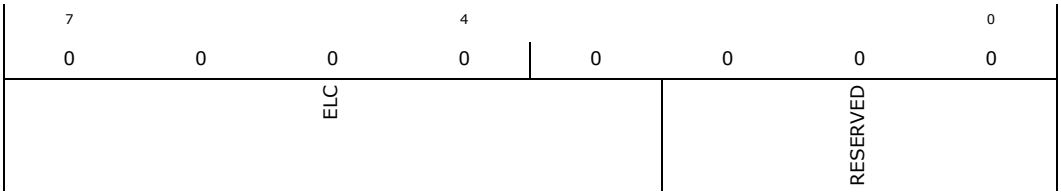
Master Edge/Level Control

Access Method

Type: I/O Register
(Size: 8 bits)

ELCR1: 4D0h

Default: 00h



Bit Range	Default & Access	Description
7:3	X RW	**ELC:** Edge Level Control (ECL[7:3]): In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level.
2:0	0b RO	**RESERVED:** Reserved.

32.3.16 ELCR2—Offset 4D1h

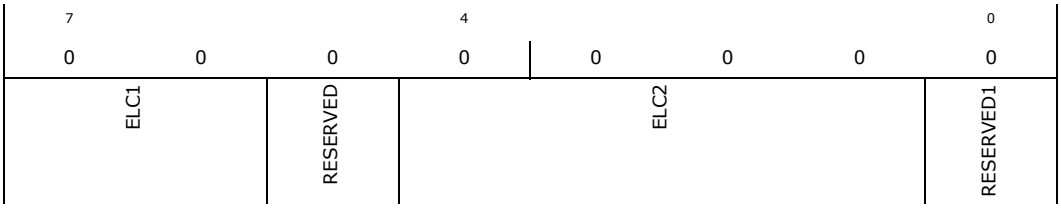
Slave Edge/Level Control

Access Method

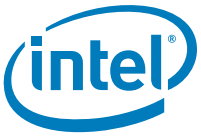
Type: I/O Register
(Size: 8 bits)

ELCR2: 4D1h

Default: 00h



Bit Range	Default & Access	Description
7:6	X RW	**ELC1:** Edge Level Control (ECL[15:14]): In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
5	0b RO	**RESERVED:** Reserved.
4:1	X RW	**ELC2:** Edge Level Control (ECL[12:9]: In edge mode, (bit cleared), the interrupt is recognized by a low to high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
0	0b RO	**RESERVED (RESERVED1):** Reserved.



X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for CPU - Central Processing Units ***category:***

Click to view products by Intel ***manufacturer:***

Other Similar products are found below :

AT80612003090AAS LBWJ B4860NSE7QUMD NPIXP2855AB-S-LA88 IVPX7225-RTM-1 96MPI5-2.9-6M10T 2SC4646D-AN SMBV1061LT1G 2SC4646E-AN 2SJ268-DL-E CP80617003981AHS LBTQ MATXM-CORE-411-HTSNK TEC0193BPF TND516SS-TL-E BGSF 1717MN26 E6327 D8086-2 LF80538GF0282M-S-L8VY CM8063401293902S R1A4 CM8063501521302S R1B8 CM8066201919901 SR2L0 CM8066201928505 SR2HT CPH5855-TL-E CM8063501293200S R1A0 AV8063801129600S R10F EMS36-02-2H-MDT EMM04-MDT NG80386DX33 NHIXP432AC NK80530MZ866256S-L7XH P1021NXE2HFB R0K5ML001SS00BR LC87F2608A LC87FBK08A PRIXP425BC PRIXP423BB CM8066201921712S R2LF CM8064601467102S R152 CM8063501375800S R1AX CM8063501293506S R1A2 CM8063401293802S R1A3 CM8062107185405S R0KM LC87F0G08A CM8067702867061S R374 PB-8SMB COMX-300-HSP RTM-ATCA-7360 96MPI7-3.4-8M11T CM8066002023801S R2J1 96MPP-2.3-3M10T 96MPI7-3.4-8M11T1 96MPXE-2.0-15M20T