Integrated Device Technology, Inc.

CMOS ASYNCHRONOUS FIFO 2048 x 9, 4096 x 9, 8192 x 9 and 16384 x 9

IDT7203
IDT7204
IDT7205
IDT7206

FEATURES:

- First-In/First-Out Dual-Port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- 8192 x 9 organization (IDT7205)
- 16384 x 9 organization (IDT7206)
- High-speed: 12ns access time
- Low power consumption
  - — Active: 770mW (max.)
  - — Power-down: 44mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable in both word depth and width
- Pin and functionally compatible with IDT720X family
- Status Flags: Empty, Half-Full, Full
- Retransmit capability
- High-performance CMOS technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing for #5962-88669 (IDT7203), 5962-89567 (IDT7203), and 5962-89568 (IDT7204) are listed on this function.

DESCRIPTION:

The IDT7203/7204/7205/7206 are dual-port memory buffers with internal pointers that load and empty data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

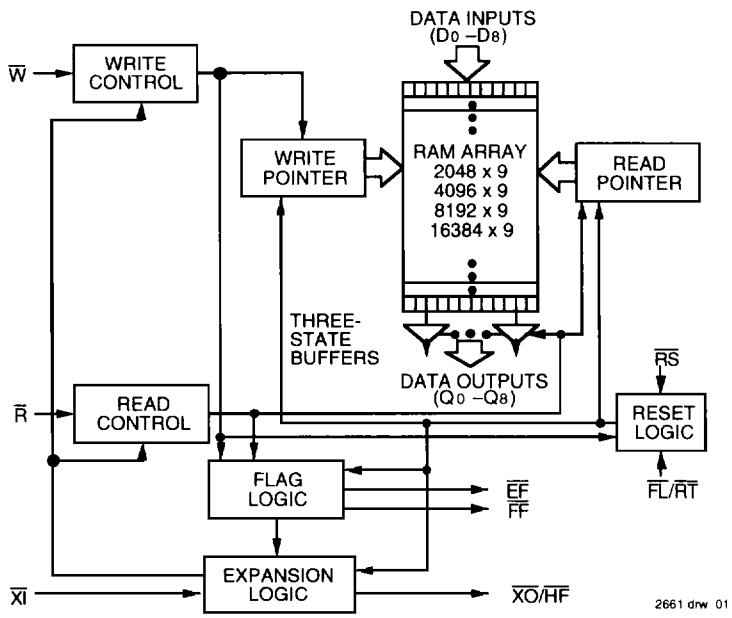
Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins.

The devices 9-bit width provides a bit for a control or parity at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows the read pointer to be reset to its initial position when $\overline{RT}$ is pulsed LOW. A Half-Full Flag is available in the single device and width expansion modes.

The IDT7203/7204/7205/7206 are fabricated using IDT's high-speed CMOS technology. They are designed for applications requiring asynchronous and simultaneous read/writes in multiprocessing, rate buffering, and other applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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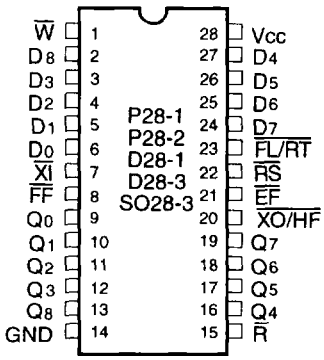
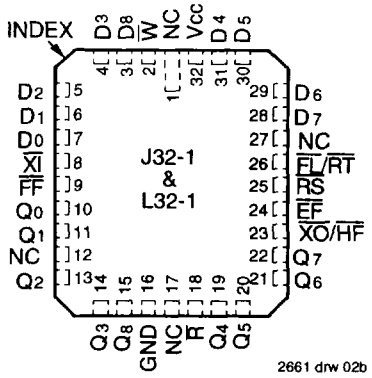
PIN CONFIGURATIONS



2661 drw 02a

DIP
TOP VIEW



2661 drw 02b

PLCC/LCC
TOP VIEW

NOTES:
1. The THINDIPs P28-2 and D28-3 are only available for the 7203/7204/7205.
2. The small outline package SO28-3 is only available for the 7204.
3. Consult factory for CERPACK pinout.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to + 7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	° C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	° C
TSTG	Storage Temperature	–55 to + 125	–65 to +155	° C
IOUT	DC Output Current	50	50	mA

NOTE: 2661 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2661 tbl 02

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS FOR THE 7203 AND 7204

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

		IDT7203/7204 Commercial t_A = 12, 15, 20, 25, 35, 50 ns			IDT7203/7204 Military[1] t_A = 20, 30, 40, 50, 65, 80, 120 ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LI}[2]	Input Leakage Current (Any Input)	−1	—	1	−1	—	1	µA
I_{LO}[3]	Output Leakage Current	−10	—	10	−10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = −2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}[4]	Active Power Supply Current	—	—	120[5]	—	—	150[5]	mA
I_{CC2}[4]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	—	12	—	—	25	mA
$I_{CC3(L)}$[4]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	2	—	—	4	mA
$I_{CC3(S)}$[4]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	8	—	—	12	mA

NOTES: 2661 tbl 03

1. Speed grades 65, 80, and 120ns are only available in the ceramic DIP.
2. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
3. R ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
4. I_{CC} measurements are made with outputs open (only capacitive loading).
5. Tested at f = 20MHz.

DC ELECTRICAL CHARACTERISTICS FOR THE 7205 AND 7206

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

		IDT7205/7206 Commercial t_A = 15, 20, 25, 35, 50 ns			IDT7205/7206 Military t_A = 20, 30, 50 ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LI}[1]	Input Leakage Current (Any Input)	−1	—	1	−1	—	1	µA
I_{LO}[2]	Output Leakage Current	−10	—	10	−10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = −2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Active Power Supply Current	—	—	120[4]	—	—	150[4]	mA
I_{CC2}[3]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	—	12	—	—	25	mA
$I_{CC3(L)}$[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	8	—	—	12	mA

NOTES: 2661 tbl 04

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. R ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commercial				Com'l & Mil.		Com'l		Military		Com'l		
		7203S/L12 7204S/L12		7203S/L15 7204S/L15 7205L15 7206L15		7203S/L20 7204S/L20 7205L20 7206L20		7203S/L25 7204S/L25 7205L25 7206L25		7203S/L30 7204S/L30 7205L30 7206L30		7203S/L35 7204S/L35 7205L35 7206L35		
Symbol	**Parameters**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
f_S	Shift Frequency	—	50	—	40	—	33.3	—	28.5	—	25	—	22.2	MHz
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RLZ}	Read LOW to Data Bus LOW[3]	3	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write HIGH to Data Bus Low-Z[3, 4]	3	—	5	—	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read HIGH to Data Bus High-Z[3]	—	12	—	15	—	15	—	18	—	20	—	20	ns
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{WPW}	Write Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	9	—	11	—	12	—	15	—	18	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{RS}	Reset Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RSS}	Reset Set-up Time[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RTR}	Reset Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{RT}	Retransmit Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RTS}	Retransmit Set-up Time[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RSR}	Retransmit Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to $\overline{EF}$ LOW	—	12	—	25	—	30	—	35	—	40	—	45	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	17	—	25	—	30	—	35	—	40	—	45	ns
t_{RTF}	Retransmit LOW to Flags Valid	—	20	—	25	—	30	—	35	—	40	—	45	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW	—	12	—	15	—	20	—	25	—	30	—	30	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH	—	14	—	15	—	20	—	25	—	30	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ HIGH	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH	—	12	—	15	—	20	—	25	—	30	—	30	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW	—	14	—	15	—	20	—	25	—	30	—	30	ns
t_{WHF}	Write LOW to $\overline{HF}$ Flag LOW	—	17	—	25	—	30	—	35	—	40	—	45	ns
t_{RHF}	Read HIGH to $\overline{HF}$ Flag HIGH	—	17	—	25	—	30	—	35	—	40	—	45	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ HIGH	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{XOL}	Read/Write LOW to $\overline{XO}$ LOW	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{XOH}	Read/Write HIGH to $\overline{XO}$ HIGH	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	8	—	10	—	10	—	10	—	10	—	15	—	ns

2661 tbl 05

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS[1] (Continued)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

		Military		Com'l & Mil.		Military[2]						
		7203S/L40 7204S/L40		7203S/L50 7204S/L50 7205L50 7206L50		7203S/L65 7204S/L65		7203S/L80 7204S/L80		7203S/L120 7204S/L120		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fs	Shift Frequency	—	20	—	15	—	12.5	—	10	—	7	MHz
tRC	Read Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
tA	Access Time	—	40	—	50	—	65	—	80	—	120	ns
tRR	Read Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
tRPW	Read Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tRLZ	Read LOW to Data Bus LOW[4]	5	—	10	—	10	—	10	—	10	—	ns
tWLZ	Write HIGH to Data Bus Low-Z[4, 5]	10	—	15	—	15	—	20	—	20	—	ns
tDV	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	5	—	ns
tRHZ	Read HIGH to Data Bus High-Z[4]	—	25	—	30	—	30	—	30	—	35	ns
tWC	Write Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
tWPW	Write Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tWR	Write Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
tDS	Data Set-up Time	20	—	30	—	30	—	40	—	40	—	ns
tDH	Data Hold Time	0	—	5	—	10	—	10	—	10	—	ns
tRSC	Reset Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
tRS	Reset Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tRSS	Reset Set-up Time[4]	40	—	50	—	65	—	80	—	120	—	ns
tRSR	Reset Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
tRTC	Retransmit Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
tRT	Retransmit Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tRTS	Retransmit Set-up Time[4]	40	—	50	—	65	—	80	—	120	—	ns
tRSR	Retransmit Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
tEFL	Reset to $\overline{EF}$ LOW	—	50	—	65	—	80	—	100	—	140	ns
tHFH, tFFH	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	50	—	65	—	80	—	100	—	140	ns
tRTF	Retransmit LOW to Flags Valid	—	50	—	65	—	80	—	100	—	140	ns
tREF	Read LOW to $\overline{EF}$ Flag LOW	—	35	—	45	—	60	—	60	—	60	ns
tRFF	Read HIGH to $\overline{FF}$ HIGH	—	35	—	45	—	60	—	60	—	60	ns
tRPE	Read Pulse Width after $\overline{EF}$ HIGH	40	—	50	—	65	—	80	—	120	—	ns
tWEF	Write HIGH to $\overline{EF}$ HIGH	—	35	—	45	—	60	—	60	—	60	ns
tWFF	Write LOW to $\overline{FF}$ LOW	—	35	—	45	—	60	—	60	—	60	ns
tWHF	Write LOW to $\overline{HF}$ LOW	—	50	—	65	—	80	—	100	—	140	ns
tRHF	Read HIGH to $\overline{HF}$ HIGH	—	50	—	65	—	80	—	100	—	140	ns
tWPF	Write Pulse Width after $\overline{FF}$ HIGH	40	—	50	—	65	—	80	—	120	—	ns
tXOL	Read/Write LOW to $\overline{XO}$ LOW	—	40	—	50	—	65	—	80	—	120	ns
tXOH	Read/Write HIGH to $\overline{XO}$ HIGH	—	40	—	50	—	65	—	80	—	120	ns
tXI	$\overline{XI}$ Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
tXIS	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	15	—	15	—	ns

NOTES:

2861 tbl 06

1. Timings referenced as in AC Test Conditions.
2. Speed grades 65, 80, and 120ns are only available in the ceramic DIP.
3. Pulse widths less than minimum are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

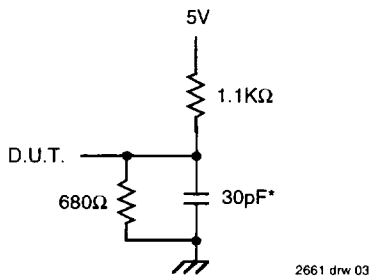
2661 tbl 07

CAPACITANCE[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:
1. This parameter is sampled and not 100% tested.
2. With output deselected.

2661 tbl 08



OR EQUIVALENT CIRCUIT

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

Inputs:

DATA IN (D_0–D_8) — Data inputs for 9-bit wide data.

Controls:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$.**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered-to, with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW, and will remain set until the difference between the write pointer and read pointer is less-than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW on the falling edge of the last write signal, which inhibits further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF}, allowing a new valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$), provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (Q_0 through Q_8) will return to a high-impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high-impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204/7205/7206 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. The status of the Flags will change depending on the relative locations of the read and write pointers. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than 2048/4096/8192/16384 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION IN ($\overline{XI}$) — This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy-Chain Mode.

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Outputs:

FULL FLAG ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations, when the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 2048/4096/8192/16384 writes.

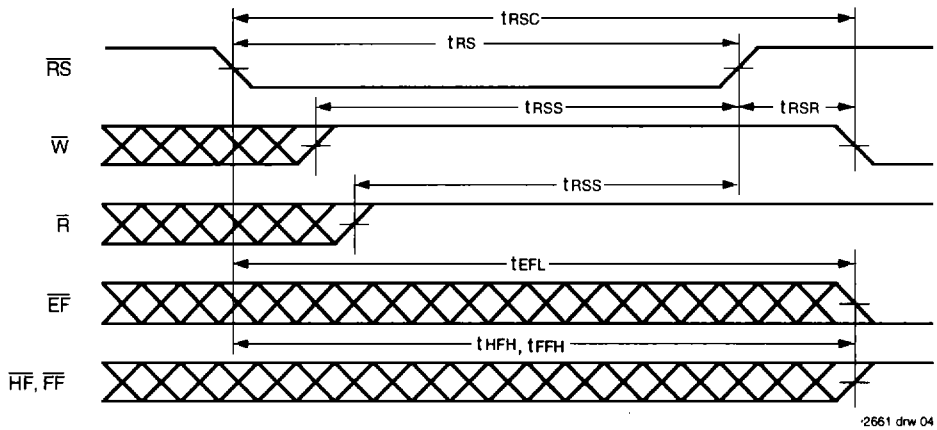
EMPTY FLAG ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$) — This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the Write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the Read pointer reaches the last location of memory.

DATA OUTPUTS (Q0-Q8) — Q0-Q8 are data outputs for 9-bit wide data. These outputs are in a high-impedance condition whenever Read ($\overline{R}$) is in a HIGH state.



NOTE:
1. $\overline{W}$ and $\overline{R}$ = VIH around the rising edge of $\overline{RS}$.

Figure 2. Reset

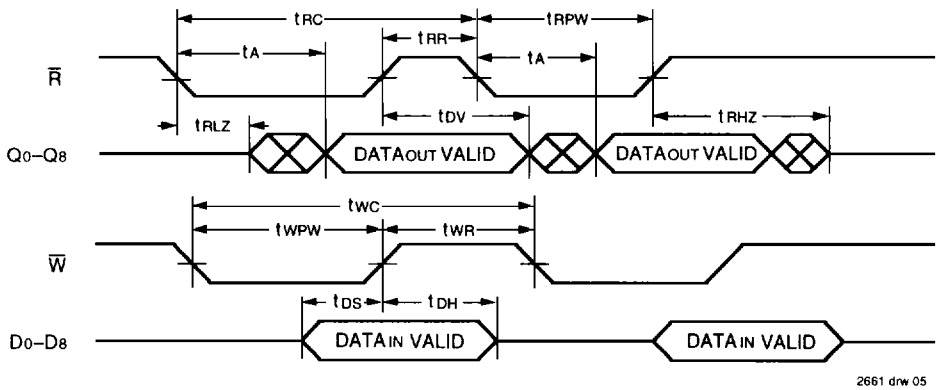


Figure 3. Asynchronous Write and Read Operation

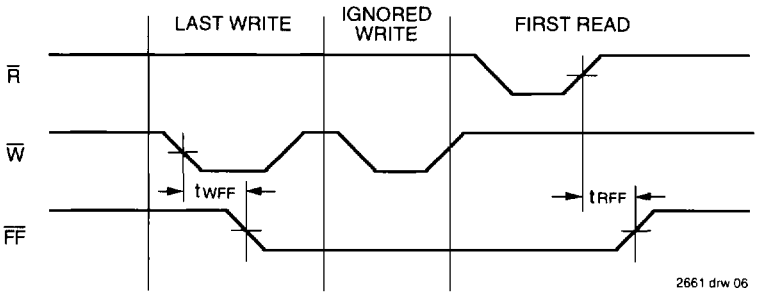


Figure 4. Full FlagTiming From Last Write to First Read

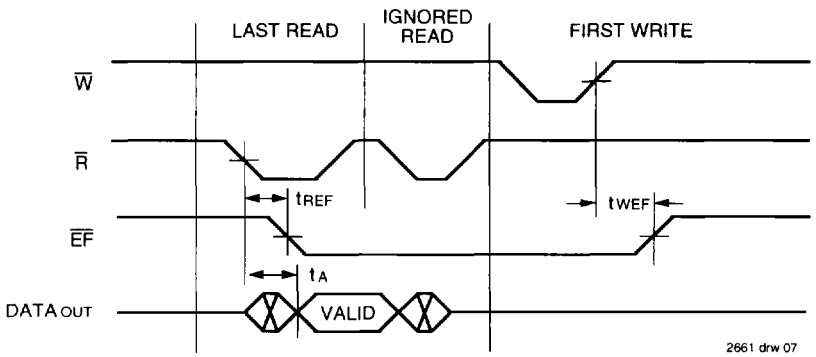
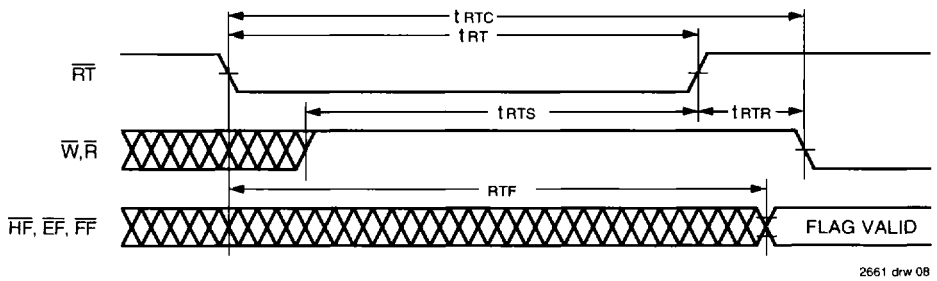


Figure 5. Empty Flag Timing From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at tRTC.

Figure 6. Retransmit

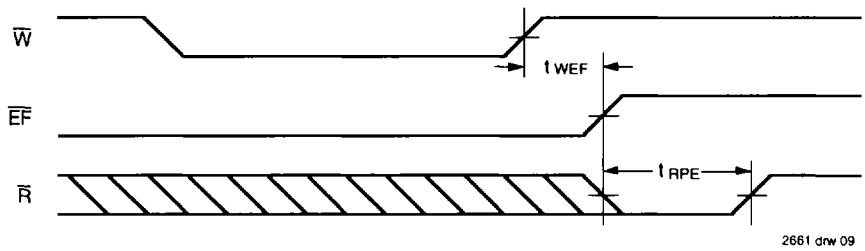


Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse.

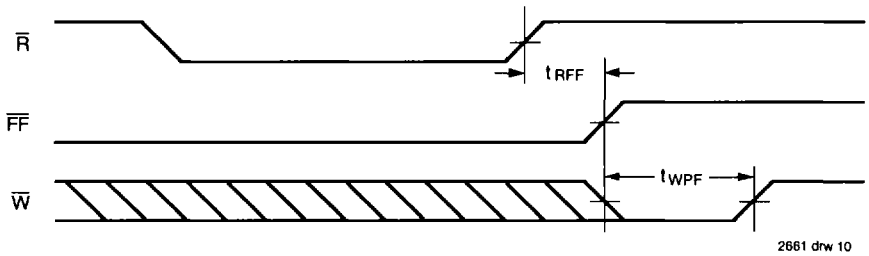


Figure 8. Minimum Timing for an Full Flag Coincident Write Pulse.

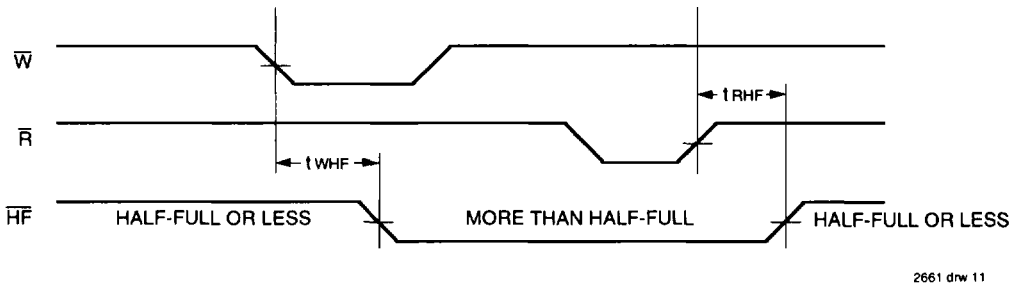


Figure 9. Half-Full Flag Timing

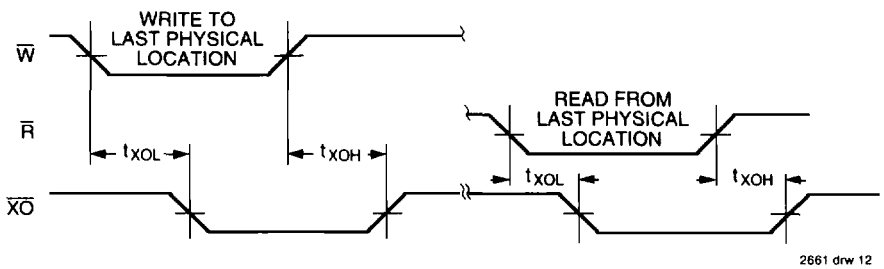


Figure 10. Expansion Out

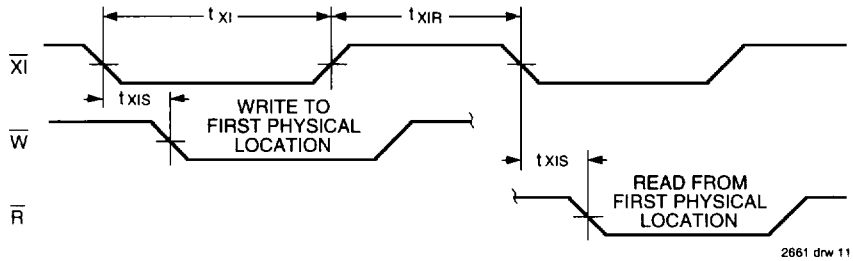


Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Single Device Mode

A single IDT7203/7204/7205/7206 may be used when the application requirements are for 2048/4096/8192/16384 words or less. The IDT7203/7204/7205/7206 is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

The IDT7203/7204/7205/7206 can easily be adapted to applications when the requirements are for greater than 2048/4096/8192/16384 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204/7205/7206s. Any depth can be attained by adding additional IDT7203/7204/7205/7206s. The IDT7203/7204/7205/7206 operates in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204/7205/7206s. Any word width can be attained by adding additional IDT7203/7204/7205/7206s (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204/7205/7206s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

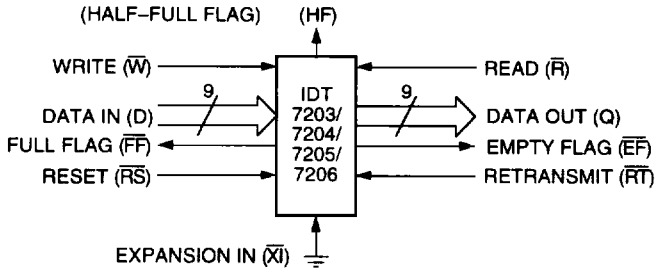
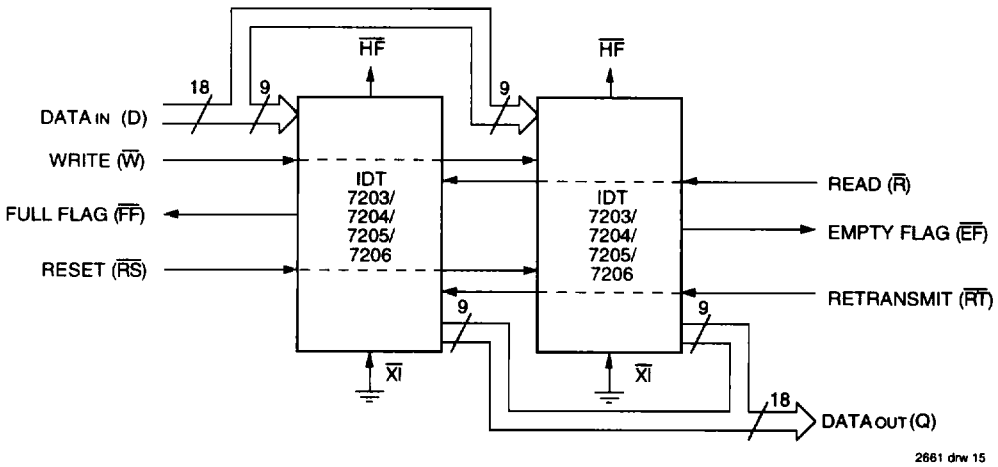


Figure 12. Block Diagram of 2048 x 9/4096 x 9/8192 x 9/16384 x 9 FIFO Used in Single Device Mode



NOTE:
1. Flag detection is accomplished by monitoring the FF, EF and HF signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

Figure 13. Block Diagram of 2048 x 18/4096 x 18/8192 x 18/16384 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will Increment if flag is HIGH.

2661 tbl 09

TABLE II – RESET AND FIRST LOAD

DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
2. $\overline{RS}$ = Reset Input, $\overline{FL/RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

2661 tbl 10

5

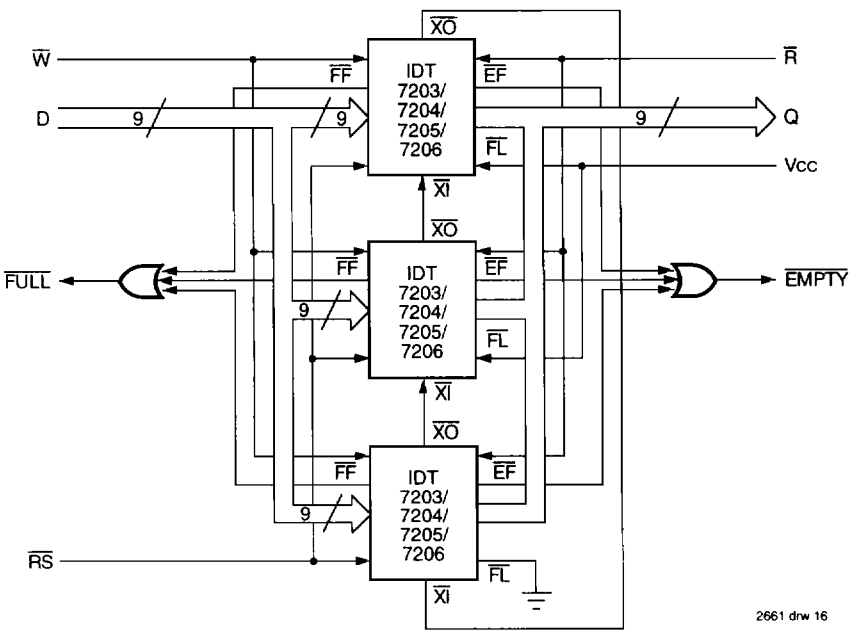
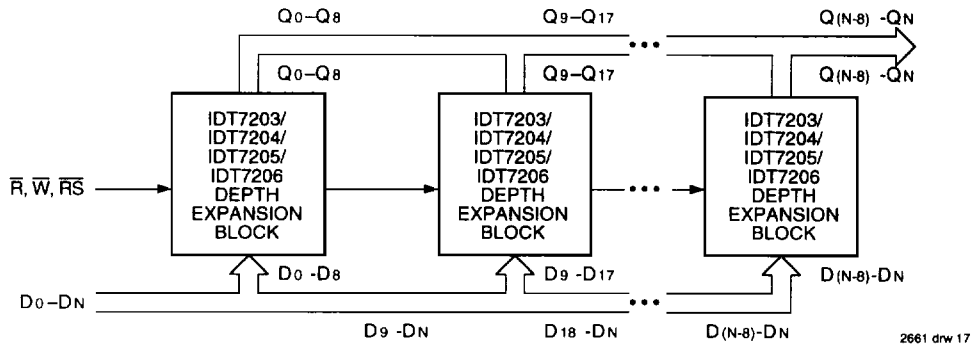


Figure 14. Block Diagram of 6149 x 9/12298 x 9/24596 x 9/49152 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

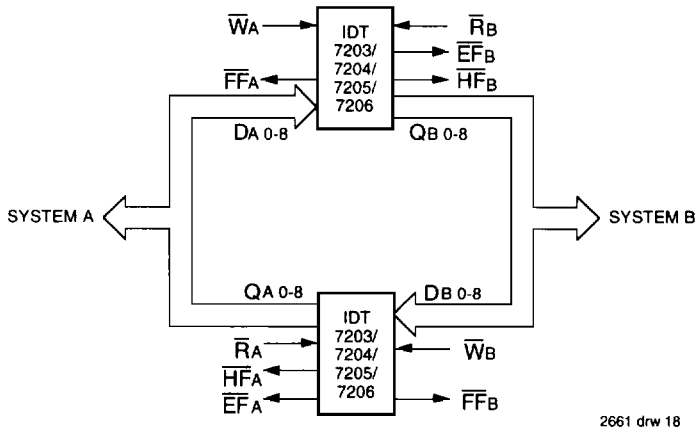


Figure 16. Bidirectional FIFO Operation

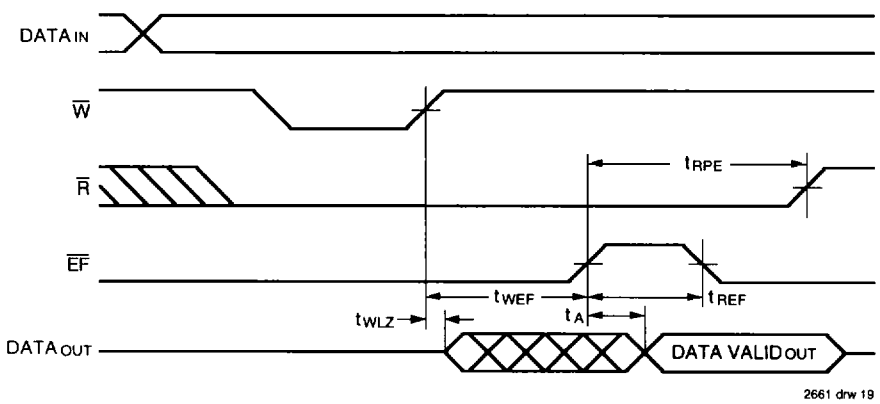


Figure 17. Read Data Flow-Through Mode

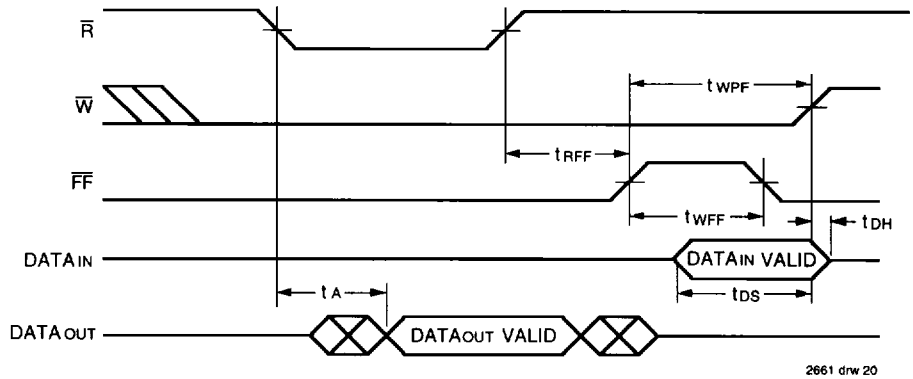
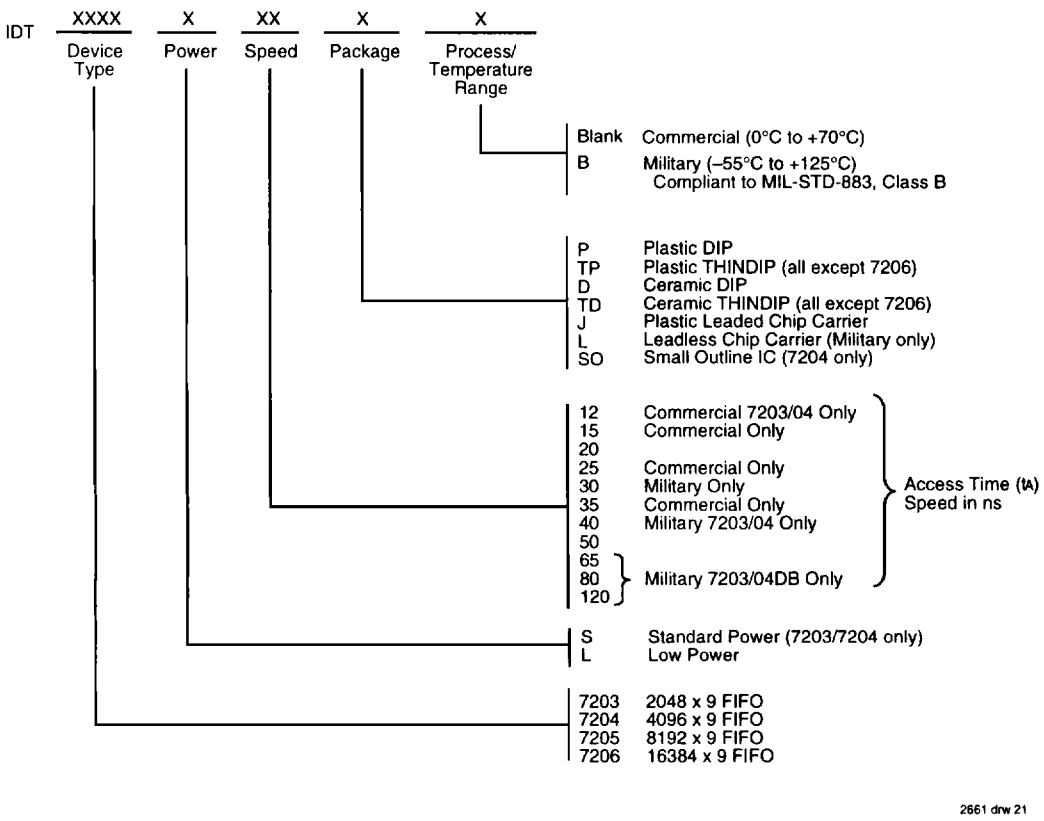


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



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