



## 8-bit Serial-In/Parallel-Out Constant Current Driver

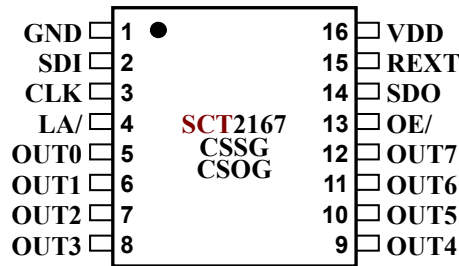
### Product Description

The SCT2167 serial-interfaced LED driver sinks 8 LED clusters with constant current to keep the uniform intensity of LED displays. In applications, an external resistor is used to set the full-scale constant output current from 5mA up to 45mA. The SCT2167 guarantees each output can endure maximum 17V DC voltage stress. The built-in shift registers and data latches making the SCT2167 effective solution in driving LED display. The output enable function gates all 8 outputs on and off, and is fast enough to be used as PWM input for LED intensity control. Since the serial data input rate can be reached up to 25MHz, the SCT2167 will satisfy system which needs high volume data transmission to control the LED

### Features

- ◆ 8 constant current sinkers with output voltage sustainable to 17V
- ◆ Constant output current : 5 – 30/45mA@3.3/5V
- ◆ Excellent regulation to load, supply voltage and temperature
  - Temperature regulation:  $\pm 0.005\%/^{\circ}\text{C}$
  - load regulation:  $\pm 0.1\%/V$
  - line regulation:  $\pm 0.5\%/V$
- ◆ High current matching accuracy:  $\pm 1\%$  between outputs,  $\pm 2\%$  between ICs
- ◆ Fine grayscale response with 180ns PWM pulse width
- ◆ Dropout voltage 0.5V@20mA,  $V_{DD}=5V$
- ◆ CMOS Schmitt trigger inputs with clock rate up to 25MHz @ cascade connection
- ◆ The constant current value of 8 outputs is set by a single external resistor
- ◆ Interlaced 30ns delay of output, preventing instant current surge and output bouncing overstress
- ◆ Built-in power on reset(POR) circuit forces all the outputs off while power on
- ◆ Package: SSOP16 and SOP16
- ◆ Applications: LED Displays, Variable Message Signs, Illumination, LED Traffic Signs

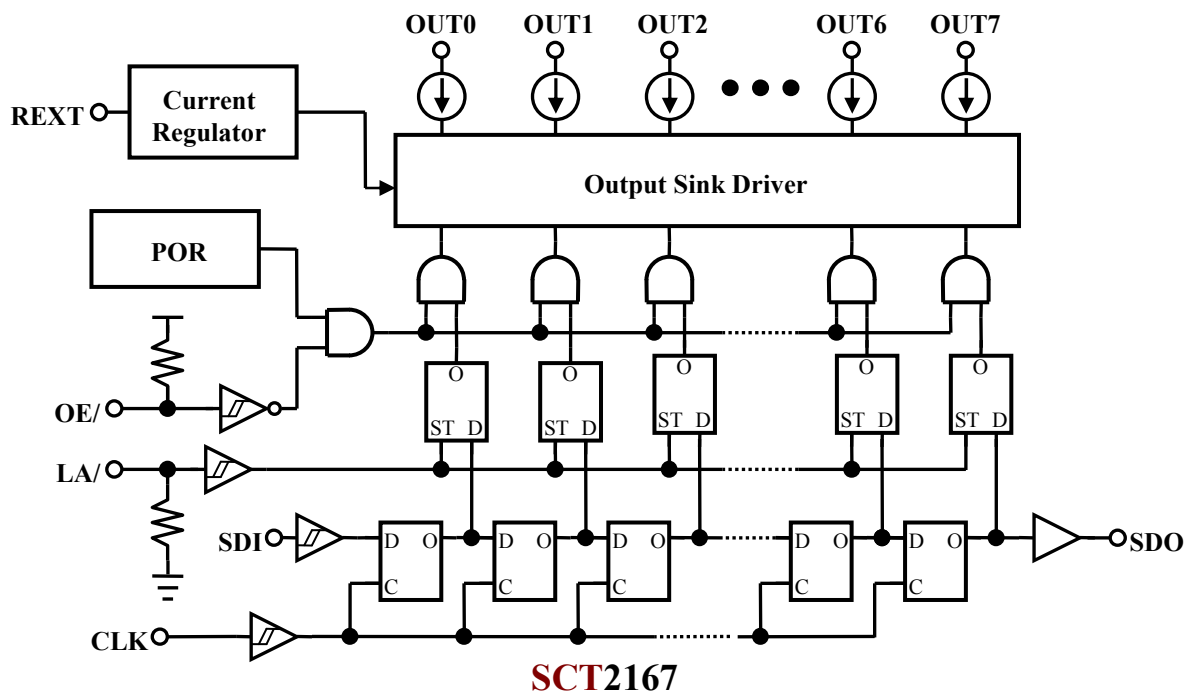
**Pin Configurations**



**Terminal Description**

Pin Name	Pin No.	I/O	Function
GND	1	-	Ground terminal
SDI	2	I	Serial input terminal of data shift register
CLK	3	I	Clock input terminal of shift register, data is sampled at the rising edge of CLK.
LA/	4	I	Data is latched when LA/ is low. Data on shift register goes through when LA/ is high.
OUT[0:7]	5-12	O	Open-drain, constant-current outputs.
OE/	13	I	Input terminal of output enable signal. Output is enabled when OE/ is low.
SDO	14	O	Output terminal of serial-data output to the SDI of next SCT2167.
REXT	15	I/O	Synchronous signal, daisy chain output terminal.
VDD	16	-	Supply voltage terminal

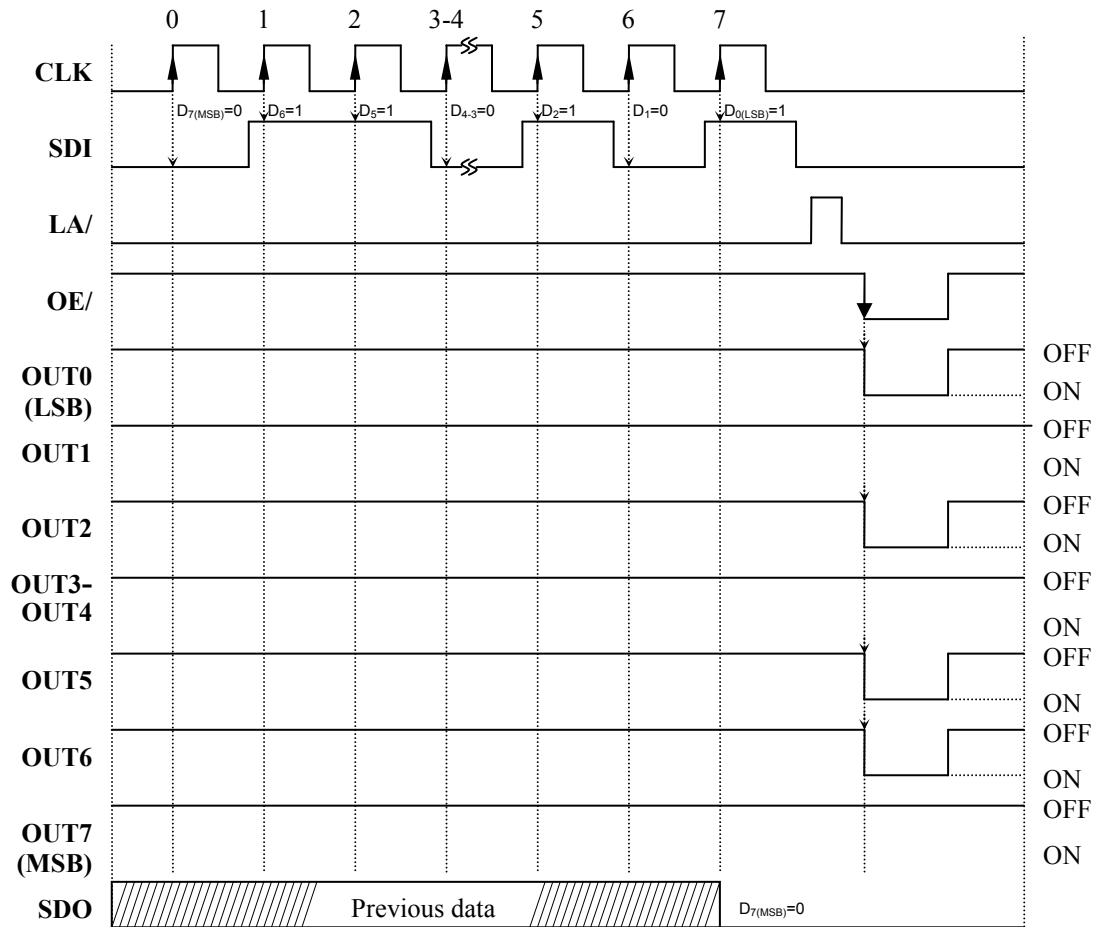
**Block Diagram**

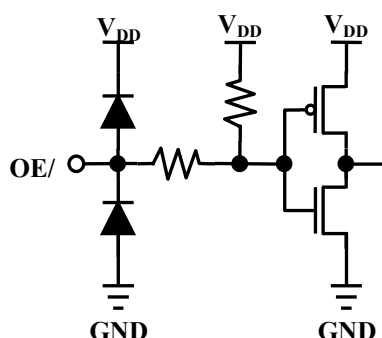
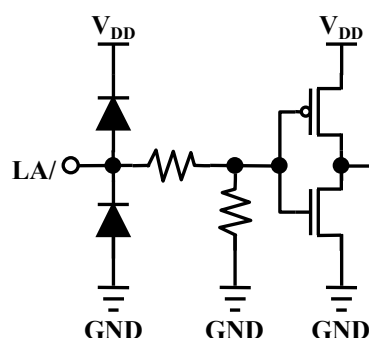
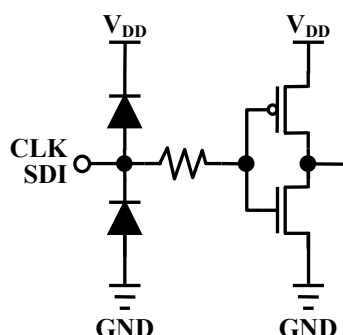
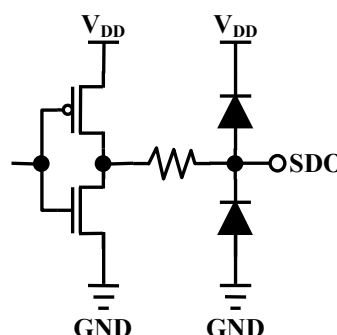


**Truth Table**

CLK	LA/	OE/	SDI	OUT0 ~ OUT7	SDO
	H	L	$D_n$	$D_n$ $D_{n-1}$ ---- $D_{n-6}$ $D_{n-7}$	$D_{n-7}$
	L	L	$D_{n+1}$	No change	$D_{n-6}$
	H	L	$D_{n+2}$	$D_{n+2}$ $D_{n+1}$ ---- $D_{n-4}$ $D_{n-5}$	$D_{n-5}$
	X	L	$D_{n+3}$	$D_{n+2}$ $D_{n+1}$ ---- $D_{n-4}$ $D_{n-5}$	$D_{n-5}$
	X	H	$D_{n+3}$	Off	$D_{n-5}$

**Timing Diagram**



**Equivalent Circuits of Inputs (1)****Equivalent Circuits of Input (2)****Equivalent Circuits of Inputs (3)****Equivalent Circuits of Output****Selector Guide**

Part	Number of Outputs	Max Output Current (mA)	Min PWM Pulse Width (ns)	Supply Voltage (V)	Error Detection
SCT2110	8	180	100	5	NA
SCT2168	8	120	120	3.3/5	NA
SCT2169	8	120	120	3.3/5	Yes
SCT2167	8	60	180	3.3/5	NA
SCT2210	16	120	50	5	NA
SCT2026	16	90	120	3.3/5	NA
SCT2027	16	90	120	3.3/5	Yes
SCT2024	16	60	180	3.3/5	NA

**Ordering Information**

Part	Marking	Package	Unit per reel(pcs)
SCT2167CSSG	SCT2167CSSG	Green SSOP16	2500
SCT2167CSOG	SCT2167CSOG	Green SOP16	2500

**StarChips Technology, Inc.**

4F, No.5, Technology Rd., Science-Based Industrial Park, Hsin-Chu, Taiwan, R.O.C.

Tel : +886-3-577-5767 Ext.555,

Fax: +886-3-577-6575,

E-mail: service@starchips.com.tw

**Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	Rating	Unit
Supply voltage	$V_{DD}$	7.0	V
Input voltage	$V_{IN}$	$-0.2 \sim V_{DD}+0.2$	V
Output current	$I_{OUT}$	60	mA/Channel
Output voltage	Outputs	$-0.2 \sim V_{DD}+0.2$	V
	OUT0~OUT7	$-0.2 \sim 17$	V
Total GND terminals current	$I_{GND}$	480	mA
Power dissipation	SSOP16	1.07	W
	SOP16	1.47	
Thermal resistance	SSOP16	117	$^\circ\text{C/W}$
	SOP16	85	
Operating junction temperature	$T_{J(max)}$	150	$^\circ\text{C}$
Operating temperature	$T_{OPR}$	$-40 \sim +85$	$^\circ\text{C}$
Storage temperature	$T_{STG}$	$-55 \sim +150$	$^\circ\text{C}$

The absolute maximum ratings are a set of ratings not to be exceeded. Stresses beyond those listed under "Maximum Ratings" may cause the device breakdown, deterioration even permanent damage. Exposure to the maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions** ( $T_A = -40$  to  $85^\circ\text{C}$  unless otherwise noted)

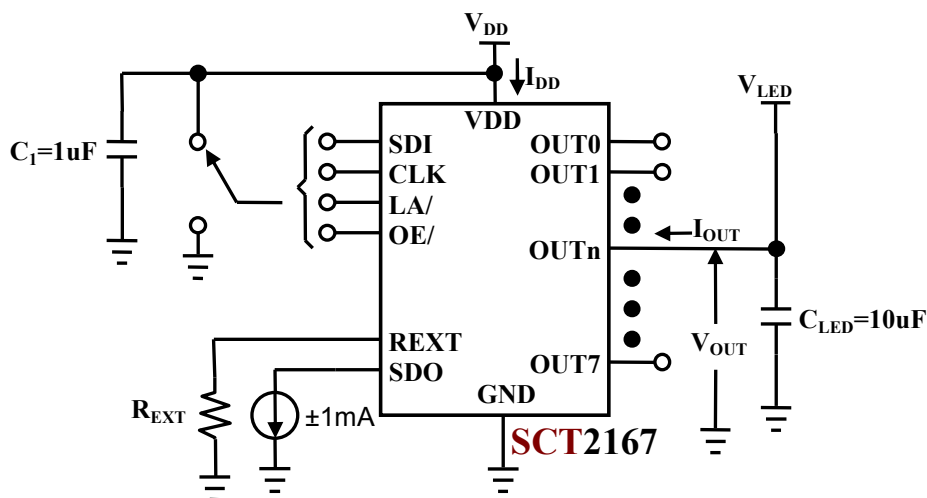
Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	$V_{DD}$	-	3	-	5.5	V
Output voltage	$V_{OUT}$	Output OFF	-	-	17	V
		Output ON	-	1 <sup>1</sup>	4 <sup>2</sup>	V
Output current	$I_{OUT}$	$V_{DD}=3.3/5\text{V}$ , $V_{OUT}=1\text{V}$	5	-	30/45	mA
Input voltage	$V_{IH}$	input signals	$0.7V_{DD}$	-	$V_{DD}$	V
	$V_{IL}$		0	-	$0.3V_{DD}$	V
OE/ pulse width	$t_{W(OE)}$	$V_{DD}=3.3\text{V}/5\text{V}$	180	-	-	ns

- The output current keep constant in range of 5-45mA if  $V_{OUT}=1\text{V}$ .  
However, user can minimize  $V_{OUT}$  to reduce power dissipation according to used current, e.g., set  $V_{OUT}$  to 0.6V if  $I_{OUT}=20\text{mA}$ .
- The maximum  $V_{out}$  is package thermal limited, user should keep  $V_{out}$  under maximum power dissipation.

**Electrical Characteristics** ( $V_{DD}=3.3/5V$ ,  $T_A=25^\circ C$  unless otherwise noted)

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Digital inputs voltage	$V_{IH}$	-	$0.7V_{DD}$	-	$V_{DD}$	V	
	$V_{IL}$	-	0	-	$0.3V_{DD}$	V	
SDO output voltage	$V_{OH}$	$V_{DD}=3.3/5V$ , $I_{OH}=-1mA$	$V_{DD}-0.4$	-	-	V	
	$V_{OL}$	$V_{DD}=3.3/5V$ , $I_{OL}=+1mA$	-	-	0.4	V	
Output leakage current	$I_{OL}$	$V_{OUT}=17V$	-	-	0.5	$\mu A$	
Output current	$I_{OUT}$	$V_{OUT}=1V$ , $R_{EXT}=900\Omega$	-	21	-	mA	
Current bit skew <sup>1</sup>	$dl_{OUT1}$	$V_{OUT}=1V$ , $R_{EXT}=900\Omega$	-	$\pm 1$	$\pm 2$	%	
Chip skew <sup>2</sup>	$dl_{OUT2}$	$V_{OUT}=1V$ , $R_{EXT}=900\Omega$	-	$\pm 2$	$\pm 5$	%	
Line regulation <sup>3</sup> $I_{OUT}$ vs. $V_{DD}$	$\%/dV_{DD}$	$3V < V_{DD} < 5.5V$ , $V_{OUT} > 1V$ , $R_{EXT}=900\Omega$	-	$\pm 0.5$	$\pm 1$	%/V	
Load regulation <sup>4</sup> $I_{OUT}$ vs. $V_{OUT}$	$\%/dV_{OUT}$	$1V < V_{OUT} < 4V$ , $I_{OUT}=42mA$ , $R_{EXT}=900\Omega$	-	$\pm 0.1$	$\pm 0.5$	%/V	
Temp. regulation <sup>5</sup> $I_{OUT}$ vs. $T_A$	$\%/dT_A$	$-20^\circ C < T_A < 80^\circ C$ , $I_{OUT}=10mA\sim 90mA$ , $V_{DD}=5V$	-	$\pm 0.005$	-	%/°C	
Pull-up resistor	$R_{UP}$	OE/	-	420	-	K $\Omega$	
Pull-down resistor	$R_{DOWN}$	LA/	-	400	-	K $\Omega$	
Supply current	OFF	$I_{DD(OFF)1}$	$V_{DD}=3.3/5V$ , $R_{EXT}=\text{Open}$ , $OUT[0:7]=\text{OFF}$	-	2	3	mA
		$I_{DD(OFF)2}$	$V_{DD}=3.3/5V$ , $R_{EXT}=900\Omega$ , $OUT[0:7]=\text{OFF}$	-	5	7	
	ON	$I_{DD(ON)}$	$V_{DD}=3.3/5V$ , $R_{EXT}=900\Omega$ , $OUT[0:7]=\text{ON}$	-	7/8	10	

1. Bit skew= $(I_{OUT}-I_{AVG}) / I_{AVG}$ , where  $I_{AVG}=(I_{OUT(max)}+I_{OUT(min)})/2$
2. Chip skew= $(I_{AVG}-I_{CEN}) / I_{CEN} * 100(\%)$ , where  $I_{CEN}$  is the statistics distribution center of output currents.
3. Line regulation= $[I_{OUT}(V_{DD}=5.5V)-I_{OUT}(V_{DD}=3V)] / \{ [I_{OUT}(V_{DD}=5.5V)+I_{OUT}(V_{DD}=3V)]/2 \} / (5.5V-3V) * 100(\%/V)$
4. Load regulation= $[I_{OUT}(V_{OUT}=4V)-I_{OUT}(V_{OUT}=1V)] / \{ [I_{OUT}(V_{OUT}=4V)+I_{OUT}(V_{OUT}=1V)]/2 \} / (4V-1V) * 100(\%/V)$
5. Temperature regulation= $[I_{OUT}(T_A=80^\circ C)-I_{OUT}(T_A=-20^\circ C)] / \{ [I_{OUT}(T_A=80^\circ C)+I_{OUT}(T_A=-20^\circ C)]/2 \} / (80^\circ C+20^\circ C) * 100(\%/^\circ C)$

**Test Circuit for Electrical Characteristics**

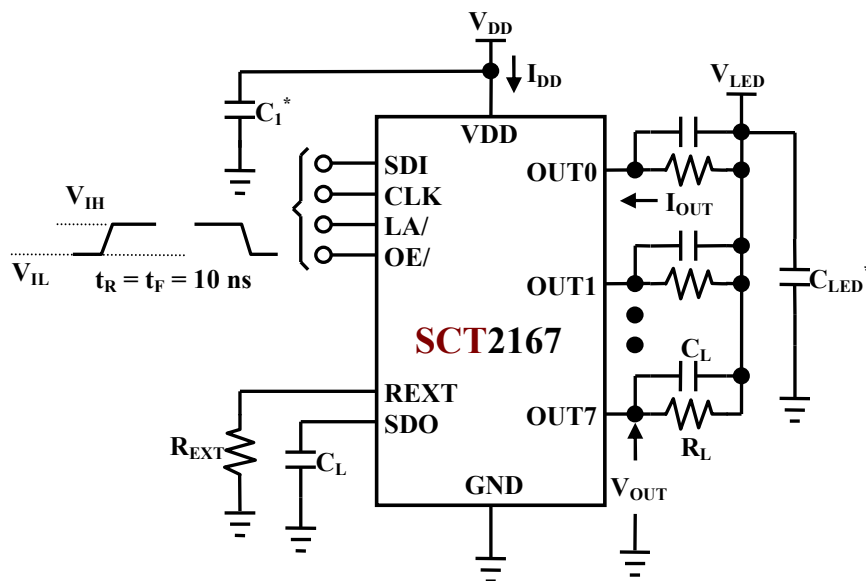
\*Place  $C_1/C_{LED}$  as close to IC VDD/OUT pin(not supply source) as possible.

**Switching Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time ("L" to "H")	CLK - OUTn	$t_{PLH1}$	$V_{DD} = 3.3/5\text{V}$ $V_{LED} = 5\text{V}$ $V_{IH} = V_{DD}$ $V_{IL} = \text{GND}$ $R_{EXT} = 900\Omega$ $R_L = 180\Omega$ $C_L = 10\text{pF}$ $C_1 = 1\mu\text{F}$ $C_{LED} = 10\mu\text{F}$	-	80	100	ns
	LA/ - OUTn	$t_{PLH2}$		-	80	100	ns
	OE/ - OUT0	$t_{PLH3}$		-	80	100	ns
	CLK - SDO	$t_{PLH}$		-	20	40	ns
Propagation delay time ("H" to "L")	CLK - OUTn	$t_{PHL1}$		-	80	100	ns
	LA/ - OUTn	$t_{PHL2}$		-	80	100	ns
	OE/ - OUT0	$t_{PHL3}$		-	80	100	ns
	CLK - SDO	$t_{PHL}$		-	20	40	ns
Pulse width	CLK	$t_{W(\text{CLK})}$		-	20	-	ns
	LA/	$t_{W(L)}$		-	20	-	ns
	OE/	$t_{W(\text{OE})}$		-	180	-	ns
Setup time for SDI	$t_{S(D)}$	-		5	-	ns	
Hold time for SDI	$t_{HD}$	-		15	-	ns	
Setup time for LA/	$t_{S(L)}$	-		5	-	ns	
Hold time for LA/	$t_{H(L)}$	-		5	-	ns	
SDO rise time	$t_{SDOR}$	-		-	20	-	ns
SDO fall time	$t_{SDOF}$	-	-	20	-	ns	
Output rise time of $I_{OUT}$	$t_{OR}$	-	-	80	100	ns	
Output fall time of $I_{OUT}$	$t_{OF}$	-	-	80	100	ns	
Delayed output	$t_{DR}$	OUT <sub>EVEN</sub> to OUT <sub>ODD</sub>	-	30	-	ns	
	$t_{DF}$	OUT <sub>ODD</sub> to OUT <sub>EVEN</sub>	-	30	-	ns	
Slow CLK rise time <sup>1</sup>	$t_R$	Cascade	-	-	500	ns	
Slow CLK fall time	$t_F$		-	-	500	ns	

1. It may not be possible to achieve the timing required for data transfer between two cascaded drivers if  $t_R/t_F$  is large.

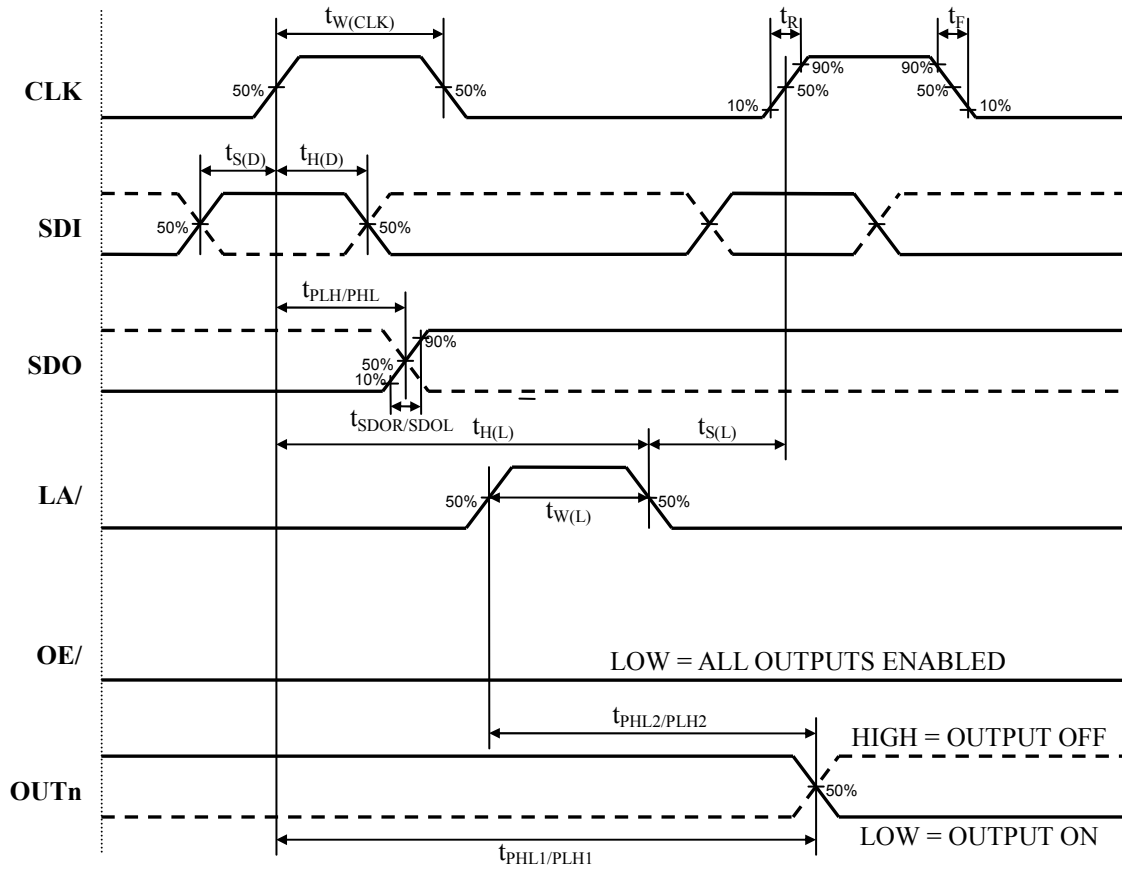
**Test Circuit for Switching Characteristics**



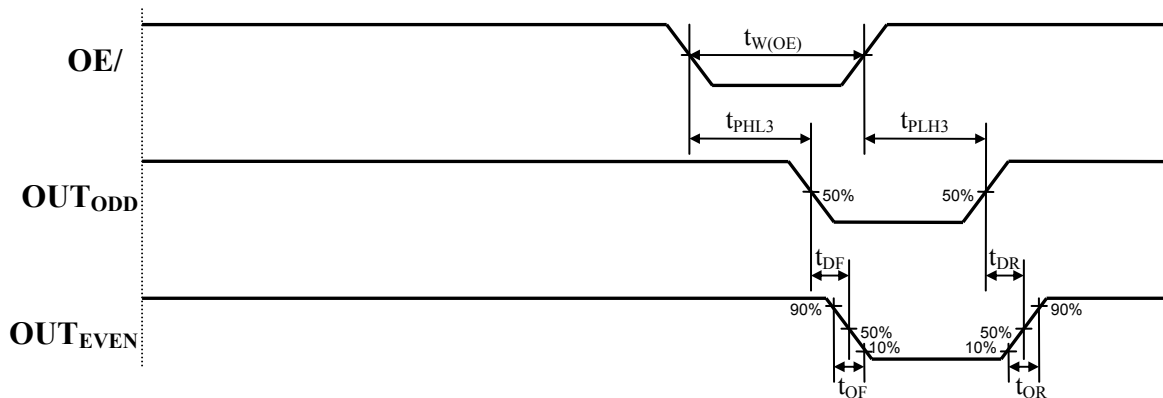
\*Place  $C_1/C_{LED}$  as close to IC VDD/OUT pin(not supply source) as possible.

### Timing Waveform

#### LA/ Control Output



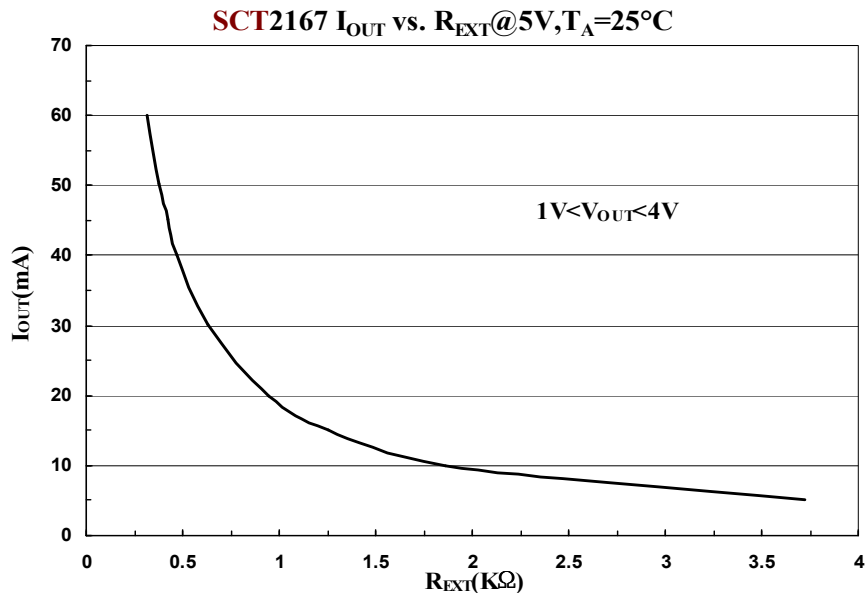
#### OE/ Control Output





## Adjusting Output Current

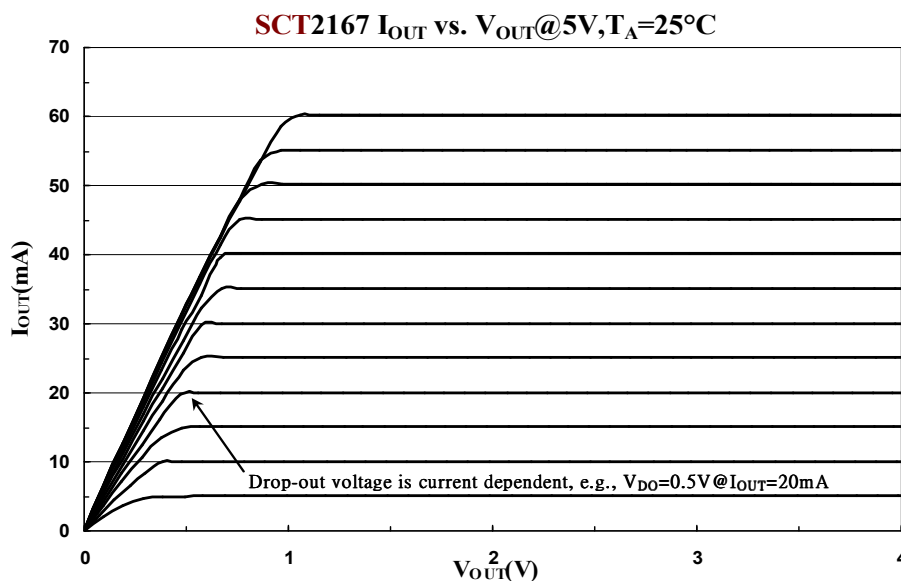
The SCT2167's output current ( $I_{OUT}$ ) are set by one external resistor at pin REXT. The output current  $I_{OUT}$  versus resistance of  $R_{EXT}$  is shown as the following figure.

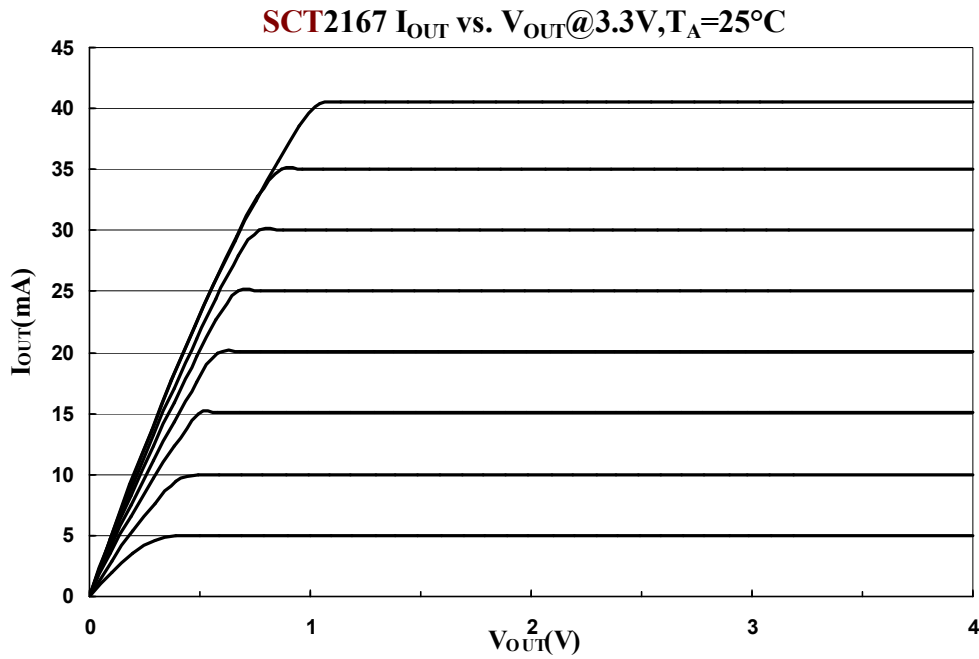


According to SCT2167' I-V curve, the output voltage should be larger than 1V to get 45 mA constant current. By applying proper output voltage, the SCT2167' output current set by an external resistor is approximate to:  $I_{OUT} = 30(630 / R_{EXT})$  (mA) (chip skew <  $\pm 5\%$ ). Thus the output current is set to be about 21mA at  $R_{EXT} = 900\Omega$ .

## Output Characteristics

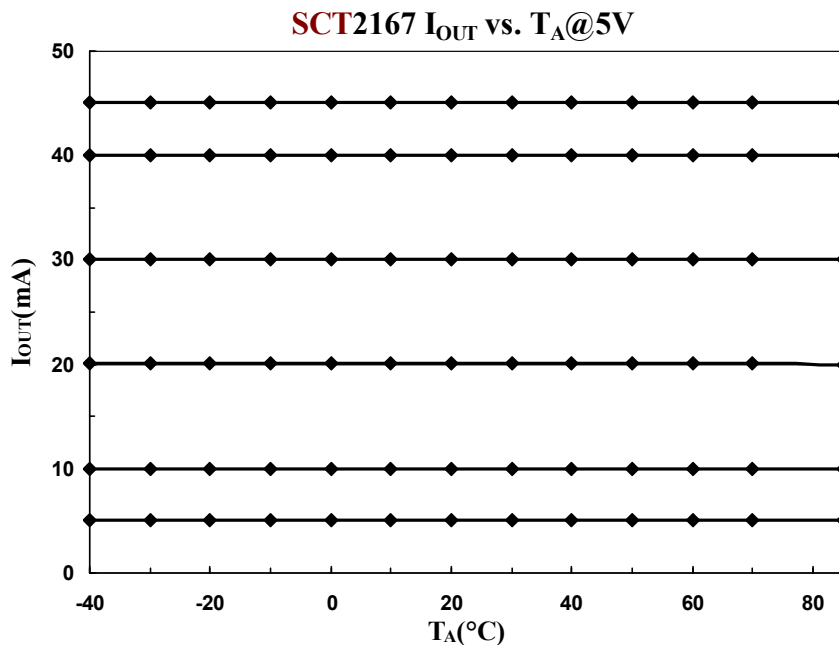
The current characteristic of output curve is flat. The output current can be kept constant regardless of the variations of LED forward voltage when  $V_{OUT} > V_{DO}$  (Drop-Out voltage). The relationship between  $I_{OUT}$  and  $V_{OUT}$  is shown below. The output voltage should be kept as low as possible to prevent the SCT2167 from being overheated.





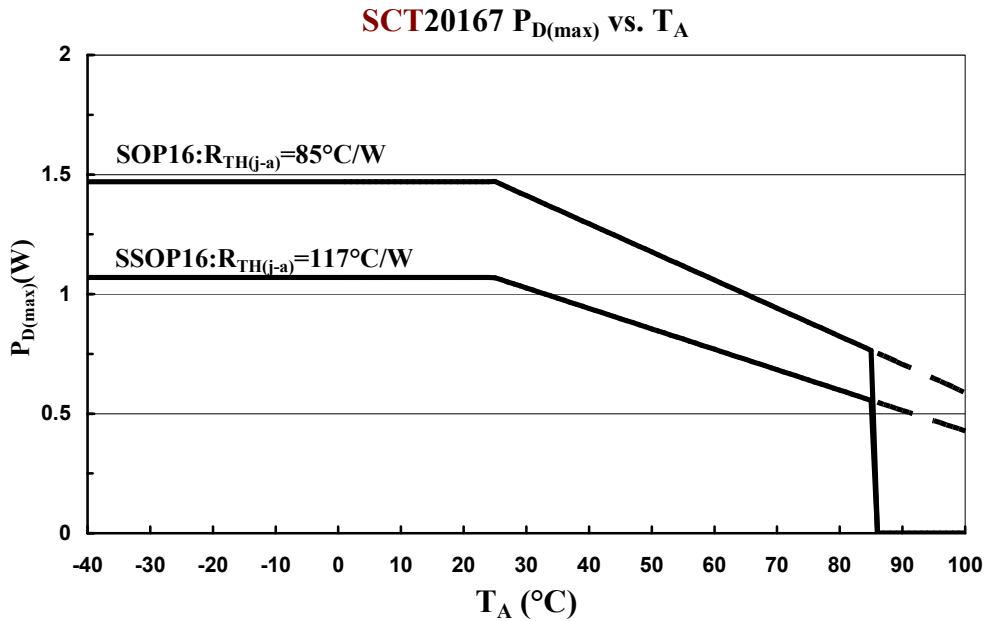
## Excellent Temperature Regulation

The constant current driver requires not only the characteristics of supply and load voltage independence, but also temperature invariance. A well thermal stable reference circuit is designed within the SCT2167. Users can get the stable output current over recommended current range  $I_{OUT}=5\text{mA}\sim 45\text{mA}$  with ambient temperature ( $T_A$ ) widely varying from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



## Power Dissipation

The maximum power dissipation ( $P_{D(max)}$ ) of a semiconductor chip varies with different packages and ambient temperature. It's determined as  $P_{D(max)} = (T_{J(max)} - T_A) / R_{TH(j-a)}$  where  $T_{J(max)}$ : maximum chip junction temperature is usually considered as 150°C,  $T_A$ : ambient temperature,  $R_{TH(j-a)}$ : thermal resistance. Since  $P=IV$ , for sinking larger  $I_{OUT}$ , users had better add proper voltage reducers on outputs to reduce the heat generated from the SCT2167.

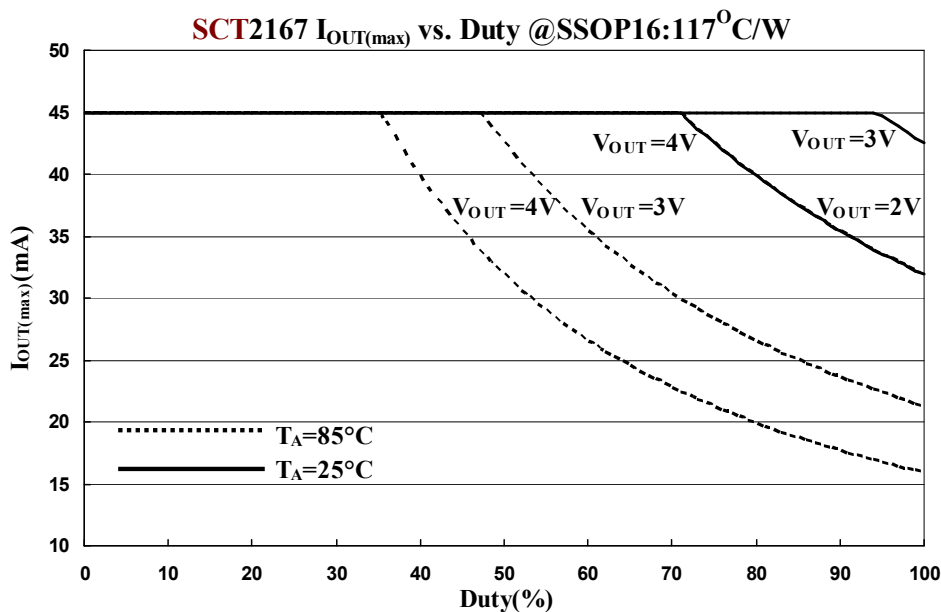


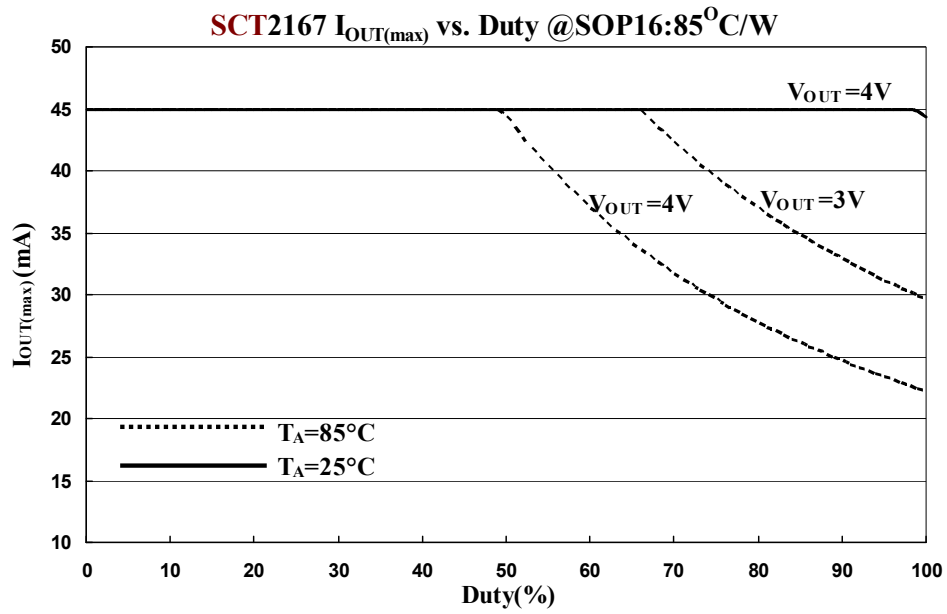
## Limitation on Maximum Output Current

The maximum output current vs. duty cycle is estimated by:

$$I_{OUT(max)} = (((T_{J(max)} - T_A) / R_{TH(j-a)}) - (V_{DD} * I_{DD})) / V_{OUT} / \text{Duty} / N$$

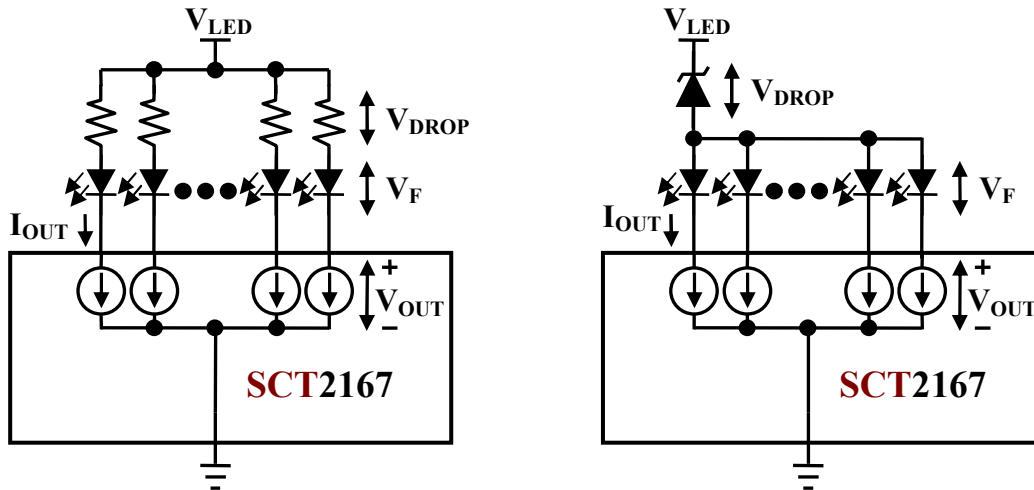
where  $T_{J(max)} = 150^\circ\text{C}$ ,  $N = 8$  (all ON)



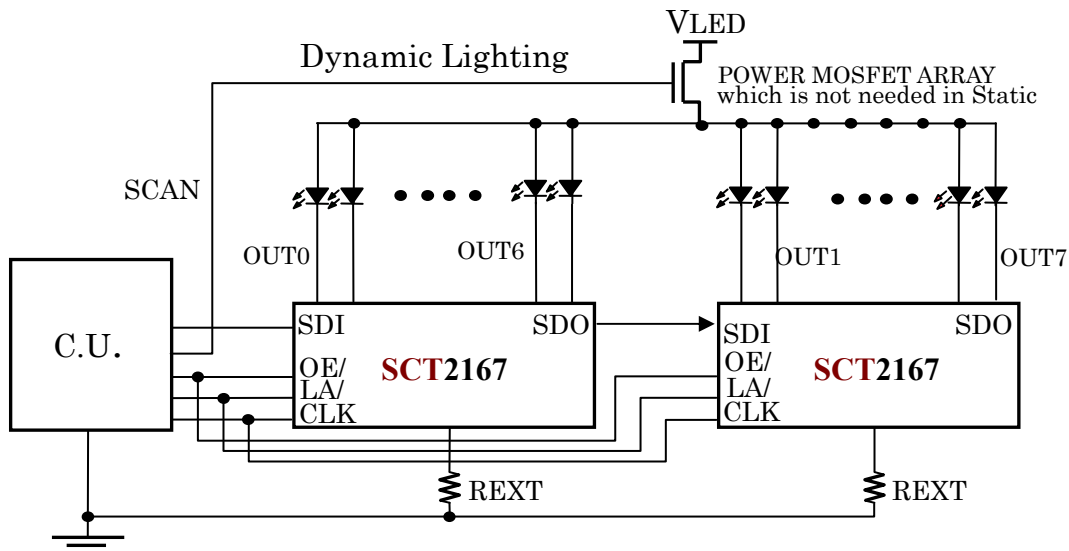


### Load Supply Voltage ( $V_{LED}$ )

The SCT2167 can be operated very well when  $V_{OUT}$  ranges from 1V to 4V. However, it is recommended to use the lowest possible supply voltage or set a voltage reducer to reduce the  $V_{OUT}$  voltage, at the same time reduce the power dissipation of the SCT2167. Suggested  $V_{OUT}$  is to be set greater than  $V_{DO}$  and less than 1V. The  $V_{DO}$  is dependent on the  $I_{OUT}$  current as indicated in section "Output Characteristics". Follow the diagram instructions shown below to lower down the output voltage. This can be done by adding additional resistor or zener diode, thus  $V_{OUT} = V_{LED} - V_{DROP} - V_F$ .



### Typical Application

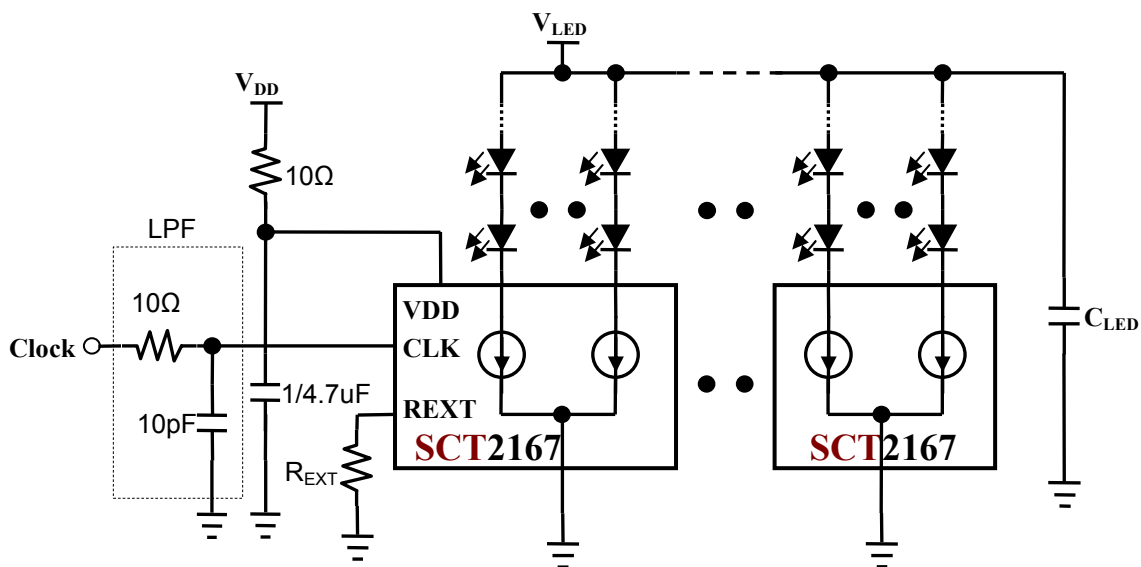


## PCB Design Considerations

Use the following general guide-line when designing printed circuit boards (PCB):

### Decoupling Capacitor

Place a decoupling capacitor e.g. 1uF between VDD and GND pins of SCT2167. Locate the capacitor as close to the SCT2167 as possible. This is normally adequate for static LED driving. For dynamic scan or PWM applications, it is suggested to add an additional capacitor of 4.7uF or more to each supply for every SCT2167. The necessary capacitance depends on the LED load current, PWM switching frequency, and serial-in data speed. Inadequate VDD decoupling can cause timing problems, and very noisy LED supplies can affect LED current regulation.



### External Resistor ( $R_{EXT}$ )

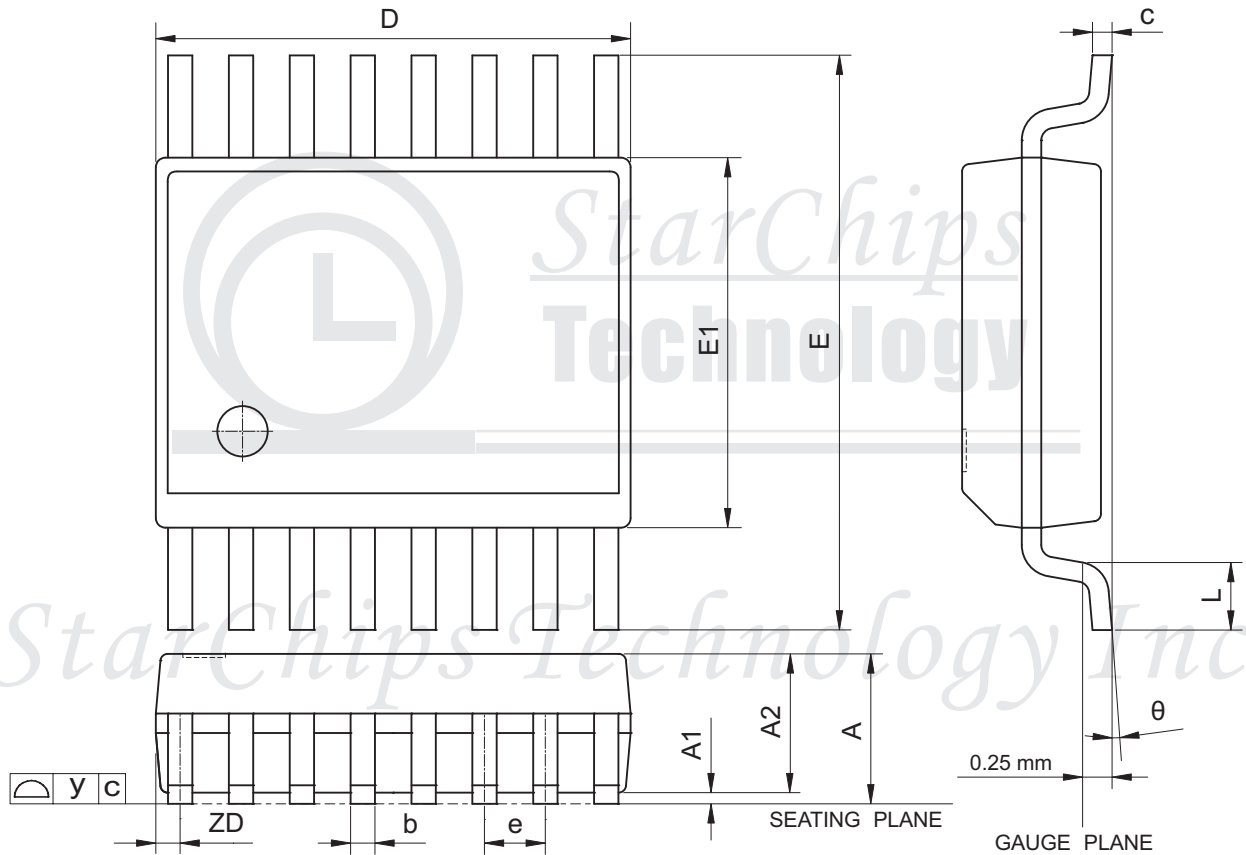
Locate the external resistor as close to the REXT pin as possible to avoid the noise influence.

### Power and Ground

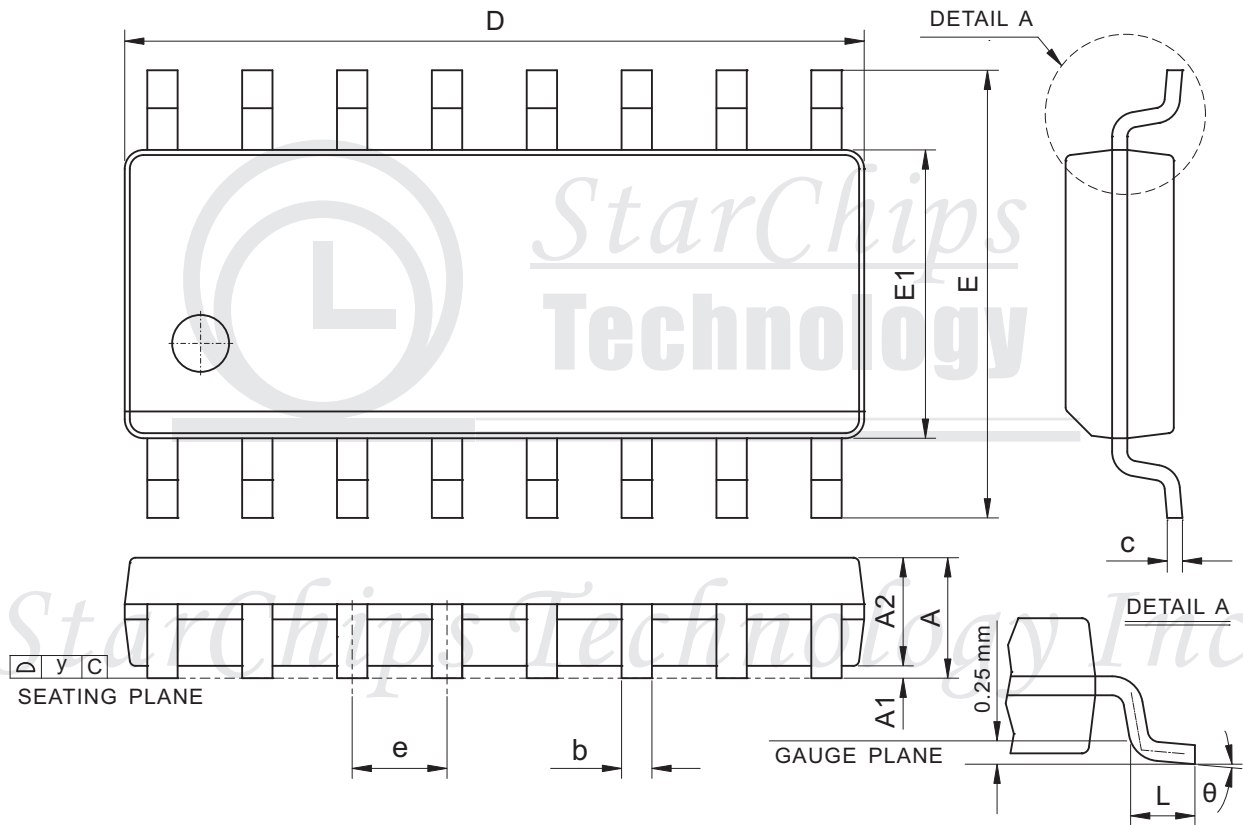
Maximizing the width and minimizing the length of VDD and GND trace improves efficiency and ground bouncing by effect of reducing both power and ground parasitic resistance and inductance. A small value of resistor, e.g., 10Ω (higher if  $I_{OUT}$  is larger) series in power input of the SCT2167 in conjunction with decoupling capacitor shunting the IC is recommended. Separating and feeding the LED power from another stable supply terminal  $V_{LED}$ , furthermore adding a capacitor  $C_{LED}$  greater than 10uF beside the LED are recommended. Please adapt  $C_{LED}$  according to total system current consumption.

### EMI Reduction

To reduce the EMI radiation from system, an economical solution of RC low pass filter (LPF) is suggested to be used to lower the transient edge of clock input signal, as shown in the figure above. Using at least four layers PCB board with two interior power and ground planes is a good scheme to decrease the signal current path which is the source of radiation emission. As a result, EMI radiation can be decreased.

**Package Dimension**SSOP16([check up-to-date version](#))

Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.35	1.63	1.75	53.1	64.2	68.9
A1	0.10	0.15	0.25	3.9	5.9	9.8
A2	-	-	1.50	-	-	59.1
b	0.20	-	0.30	7.9	-	11.8
c	0.18	-	0.25	7.1	-	9.8
D	4.80	4.90	5.00	189.0	192.9	196.9
E	5.79	5.99	6.20	228.0	235.8	244.1
E1	3.81	3.91	3.99	150.0	153.9	157.1
e	0.64 BSC			25.0 BSC		
L	0.41	0.64	1.27	16.1	25.0	50.0
y	-	-	0.10	-	-	3.9
ZD	0.23 REF			9.0 REF		
theta	0°	-	8°	0°	-	8°

SOP16([check up-to-date version](#))

Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.35	-	1.75	53.1	-	68.9
A1	0.10	-	0.25	3.9	-	9.8
A2	1.10	-	1.65	43.3	-	65.0
b	0.33	-	0.51	13.0	-	20.1
c	0.19	-	0.25	7.5	-	9.8
D	9.80	-	10.00	385.8	-	393.7
E	5.80	-	6.20	228.3	-	244.1
E1	3.80	-	4.00	149.6	-	157.5
e	1.27 BSC			50.0 BSC		
L	0.40	-	1.27	15.7	-	50.0
θ	0°	-	8°	0°	-	8°
y	-	-	0.10	-	-	3.9

Revision History([check up-to-date version](#))

Data Sheet Version	Remark
V01_02	CSWG package removed & description added

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