SP140 Development Platform Hardware

User Guide

80-Y6687-1 Rev. F

September 5, 2014

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Revision history

Revision	Date	Description
A	September 2013	Initial release
B	October 2013	Updated sections 2.4.5 and 2.4.6 to include SPI
C	January 2014	Updated for SP140-011, -012, -013. Added interface settings for SP143.
D	April 2014	Converted to regular distribution template. Updated SP140-020 board picture and components. Moved platform-specific interface routings to Installation and Configuration Guide.
E	August 2014	▪ Changed the document title from Hardware Reference Guide to Hardware User Guide. ▪ Figure 1-2, Table 1-1, Section 1.4: Updated SP140-030 board layout and components. ▪ Section 1.3.11: Added the CHIP_PWD_L/WAKE_UP_L jumper
F	September 2014	▪ Section 1.1: Fixed the styles. No content change.

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Contents

1 SP140 Development Platform

The SP140 development platform provides a fully functional interconnect between the Qualcomm® Atheros QCA4002/QCA4004 low power Wi-Fi SoC on the Wi-Fi modules and the Freescale® K22F microcontroller (MCU). The SP140 board also includes SDIO, UEXT, and Freedom/Arduino connectors to enable communication with external MCUs. See Figure 1-1 for the SP140 connection diagram.

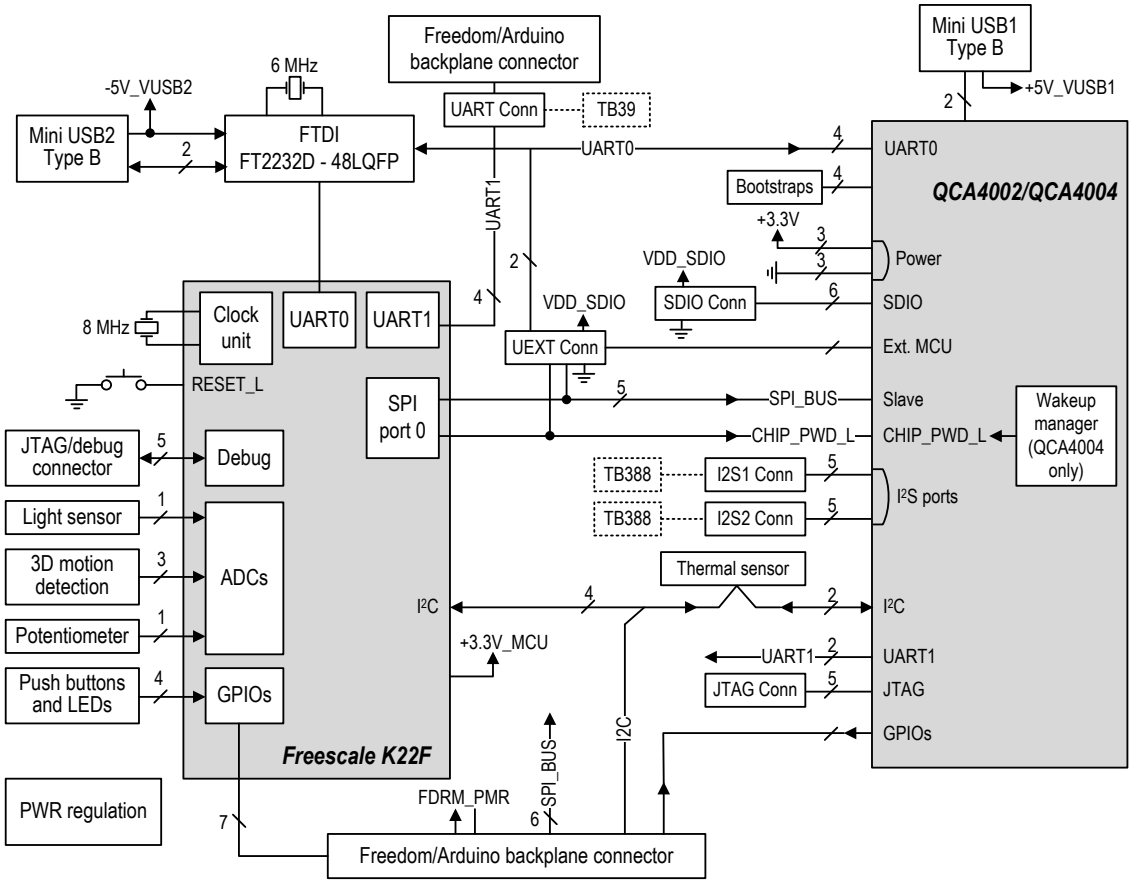


Figure 1-1 SP140 connection diagram

The SP140 board is used for software development and performance evaluation on the QCA4002/QCA4004-based Internet of Everything (IoE) systems. Qualcomm Atheros provides the Wi-Fi drivers for hostless operation as well as for hosted operation with the K22F MCU. Demo applications are supplied to facilitate the evaluation of power consumption and Wi-Fi performance of the QCA4002/QCA4004 SoC. Developers can use the drivers and the demo applications as a starting point to adapt and deploy application-specific systems.

1.1 SP140 board layout and interfaces

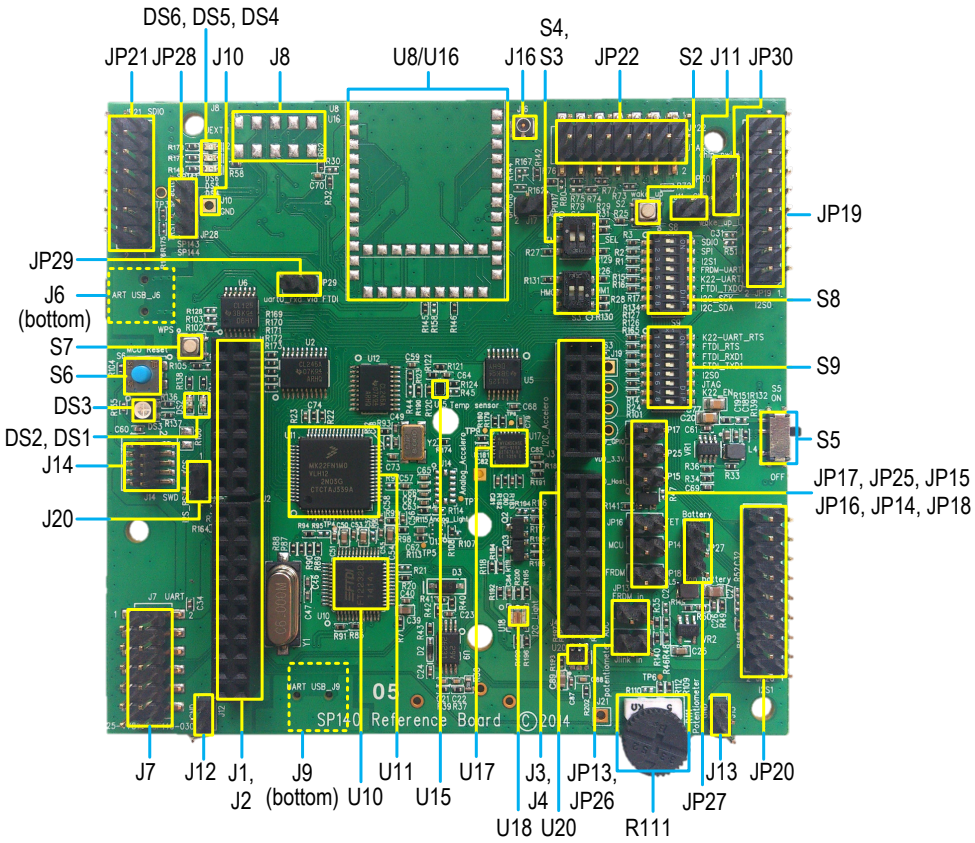


Figure 1-2 Front view of the SP140 development platform

Table 1-1 SP140 components

JP21	SDIO header	**U20**	I^2C ADC
JP28	TRST_L selector	**U18**	I^2C light sensor
J8	UEXT interface	**U17**	I^2C accelerometer
U8/U16	Footprints for Wi-Fi modules	**U15**	I^2C temperature sensor
J16	External antenna option	**U11**	Freescale K22F MCU
S3, S4	Bootstrap interface select	**U10**	Dual USB-to-UART FTDI chip
JP22	Wi-Fi module JTAG header	**J9**	FTDI mini-USB2
S2	QCA4002/QCA4004 wakeup button	**J7**	Debug UART via TB39
JP30	Reset/wakeup from K22F MCU	**J20**	SPI flash/CS signal header
JP19	I^2S0 header for TB388	**J14**	Serial Wire Debug (SWD)
S8, S9	Interface routing switches	**J10, J11, J12, J13**	Ground headers
S5	Battery ON/OFF switch	**S6**	K22F MCU reset
JP20	I^2S1 header for TB388	**S7**	WPS push button
R111	Analog potentiometer	**J6**	QCA4002/QCA4004 mini-USB1
J1, J2, J3, J4	Freedom/Arduino connectors	**JP29**	UART0_RXD signal selector
DS6, DS5, DS4, DS3, DS2, DS1			LEDs (DS3: tri-color)
JP13, JP14, JP15, JP16, JP17, JP18, JP25, JP26, JP27			Power measurement points

Table 1-2 lists the SP140 connectors and interfaces.

Table 1-2 SP140 interfaces

Interface	Description
Host UART	A host interface of QCA4002/QCA4004
Debug UART	Additional UART options for software debug
I^2S0/ I^2S1	A stereo audio CODEC interface with a daughter board (TB388)
I^2C	Access to all sensors
EJTAG	An interface for running debug firmware on the internal CPU of the QCA4002/QCA4004
USB1	An interface to the QCA4002/QCA4004. This interface is usually used during manufacturing for RF calibration, testing and firmware downloading.
USB2	Dual USB-UART interface to the QCA4002/QCA4004 and the K22F MCU
SWD	JTAG interface to the K22F MCU via J-Link TAP
UEXT	SPI and UART interfaces for accessing external MCU
SDIO	An interface to an external SDIO host via a shielded cable with minimal length
Freedom/Arduino	Connectors for plug-on daughter boards

1.2 Wi-Fi modules

The SP140 development platform supports the following Wi-Fi modules:

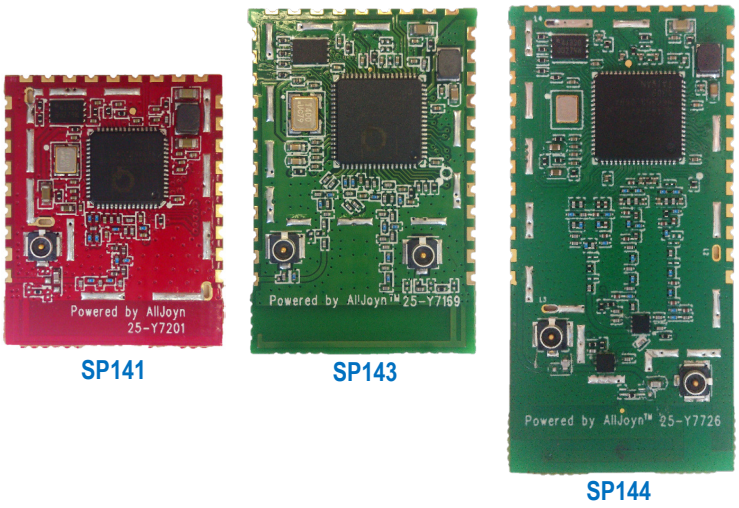


Figure 1-3 Wi-Fi modules

Table 1-3 Wi-Fi module components

Component	Description
PCB printed antenna(s)	▪ SP141, SP143: 2.4 GHz ▪ SP144: 2.4 GHz and 5 GHz
U.FL connector	Used during manufacturing test for calibration and RF testing
XTAL	40 MHz crystal
SPI flash	4-Mb SPI flash supporting quad mode

1.3 SP140 header interfaces

This section lists the headers, connectors and their pin assignments.

1.3.1 I²S0/1 headers

These headers are identical. Both headers are tested through the Qualcomm Atheros TB388 adapters. JP19 is for I²S0 and JP20 for I²S1.

Table 1-4 JP19/20, I²S header pin assignment

Pin #	Description	Pin #	Description
1	+3.3V	10	NC
2	+3.3V	11	GND
3	+5.0V	12	GND
4	+5.0V	13	I2S_SDO
5	I2S_WS	14	NC
6	I2S_RST#	15	NC
7	I2S_BCLK	16	NC
8	I2S_MCLK	17	NC
9	I2S_SDI	18	NC

1.3.2 SDIO header

Table 1-5 JP21, SDIO header pin assignment

Pin #	Description	Pin #	Description
1	SDIO_D2	8	VDD_SDIO
2	GND	9	SDIO_CLK
3	SDIO_D3	10	GND
4	GND	11	SDIO_D0
5	SDIO_CMD	12	GND
6	GND	13	SDIO_D1
7	VDD_SDIO	14	GND

1.3.3 UEXT header

Table 1-6 J8, UEXT header pin assignment

Pin #	Description	Pin #	Description
1	GND	6	CHIP_PWD#
2	+3.3V	7	SPI_MOSI
3	UART_RXD	8	SPI_MISO
4	UART_TXD	9	SPI_CS#
5	SPI_INT	10	SPI_CLK

1.3.4 Freedom/Arduino backplane header

The four headers (J1, J2, J3, J4) are sized to fit either Freedom or Arduino boards. The reference designator (RefDes) matches the Freedom RefDes.

1.3.5 K22F MCU JTAG/SWD header

Table 1-7 J14, K22F MCU JTAG header pin assignment

Pin #	Description	Pin #	Description
1	+3.3V	6	NC
2	SWD_DIO	7	+5V_SGR (Optional)
3	GND	8	NC
4	SDW_CLK	9	NC
5	GND	10	RESET

1.3.6 QCA4002/QCA4004 JTAG header

Table 1-8 JP22, QCA4002/QCA4004 JTAG header pin assignment

Pin #	Description	Pin #	Description
1	TDI	8	GND
2	GND	9	TRST
3	TDO	10	TMS
4	GND	11	Pullup
5	TCK	12	NC
6	GND	13	NC
7	NC	14	Pullup

1.3.7 Debug UART header

This header is connected through the Qualcomm Atheros TB39 adapter to the RS232 serial port on a PC.

Table 1-9 J7, Debug-UART header pin assignment

Pin #	Description	Pin #	Description
1	+3.3V	7	TB39_UART_RTS
2	+3.3V	8	NC
3	TB39_UART_RXD	9	TB39_UART_TXD
4	NC	10	NC
5	TB39_UART_CTS	11	GND
6	NC	12	GND

1.3.8 Power headers

The SP140 board includes 3.3 V on-board switch regulators to support power supply from various sources:

- Battery pack
- 5 V from USB ports (J6 or J9)
- 5 V from add-on board
- 5 V from J-Link tap

The SP140 board also provides the ability to measure power consumption on most power rails as described in Table 1-10.

Table 1-10 J14, power jumper options

RefDes	Power Rail	Supported circuit	Switch operation	Battery operation	Notes
JP13	FRDM_USB	Power source	OFF	OFF	From Freedom/Arduino Board
JP14	+3.3V_MCU	MCU peripheral	ON	ON	MCU current measurement
JP15	VDD_SDIO	Wi-Fi peripheral	ON	ON	Wi-Fi current measurement
JP16	N/A	MCU/Wi-Fi	ON	ON	Suspend current measurement
JP17	VDD_GPIO	Wi-Fi peripheral	ON	ON	Wi-Fi current measurement
JP25	+3.3V_KF	Wi-Fi peripheral	ON	ON	Wi-Fi current measurement
JP26	+5V_SGR	Power source	OFF	OFF	From j-Link TAP
JP27	N/A	All	POS. 2,3	POS. 2,1	Set switcher or battery

1.3.9 JTAG reset header

The TRST_L header (JP28) is used to route the JTAG reset signal for the Wi-Fi module. Use a jumper cap to connect the header pins:

- JP28.1&2: SP141
- JP28.2&3: SP143, SP144

1.3.10 UART routing header

The UART header (JP29) is present on SP140-020 board for routing the UART0 interface for hosted mode (SP141, SP144), hostless mode (SP143, SP144), JTAG debugging, and calibration mode.

- **Host mode**: remove jumper
- **Hostless mode**: add jumper
- **JTAG debug mode**: add jumper
- **USB calibration mode**: remove jumper

1.3.11 Chip power down/wakeup from MCU header

The CHIP_PWD_L/WAKE_UP_L header (JP30) provides an optional function to enable the K22F MCU to reset or wakeup the SP144 module.

- CHIP_PWD_L (JP30.2&3): Used in hosted mode only. This setting enables the K22F MCU to set the SP144 module to power down mode.
- WAKE_UP_L (JP30.1&2): Used in hostless mode only. This setting enables the K22F MCU to wake up the SP144 module from suspend mode before the suspend time expires. The S9.7 switch must be toggled on to receive the wakeup signal. Similar function can be achieved by pressing the S2 push button when the S9.7 switch is toggled off.

1.4 MCU components

Table 1-11 list the Freescale K22F MCU components and interfaces.

Table 1-11 MCU components

Component	Description
Sensors	▪ I^2C light sensor ▪ I^2C accelerometer ▪ I^2C temperature sensor ▪ Potentiometer with an external I^2C ADC ▪ Push button
Debug UART	Serial UART used to communicate using a CLI with the MCU via USB
UEXT interface	Exposes the SPI interface, CHIP_PWD, SPI_INT, limited UART, and 3.3 V to an external MCU. The local MCU must be bypassed when UEXT is used.
GPIO header	7 GPIOs of the local K22F MCU exposed to the Freedom connector
Serial Wire Debug (SWD)	A 2-pin electrical alternative JTAG interface with the same JTAG protocol on top and using the existing GND connection. SWD uses an ARM® CPU standard bi-directional wire protocol defined in the ARM Debug Interface v5, which enables the debugger to become another AMBA bus master to access system memory, peripherals, or debug registers.

1.5 Host interface select

Figure 1-4 shows the switch (S3, S4) configurations for the bootstrap that define the host interface. The white dot on the switch indicates pull-up, the opposite side is pull-down.

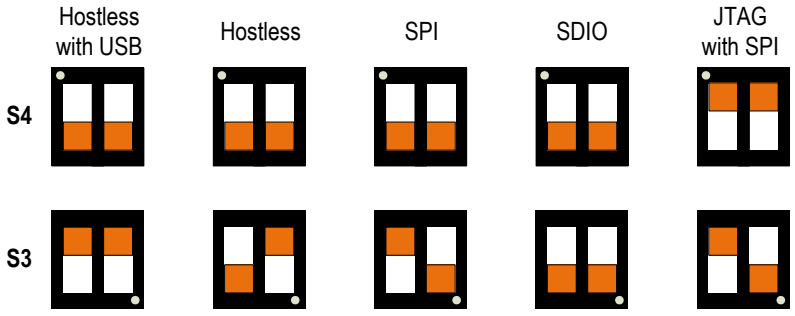


Figure 1-4 Host interface select

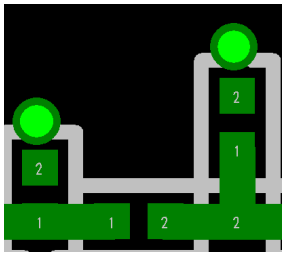
To route the host and peripheral interfaces, the S8, S9 switches must be set accordingly.

2 PCB Design Guidelines

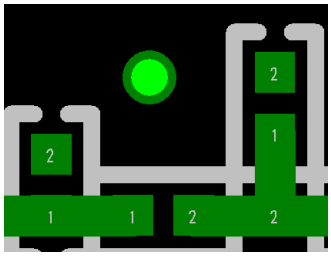
2.1 GND

2.1.1 Placement of capacitor shunted to GND

- Place bypass capacitors as close to the respective pins as possible.
- Place at least one dedicated ground via for each capacitor shunted to ground and put ground via as close to the capacitors as possible.



Good capacitor placement (2 capacitors with 2 dedicated ground vias)



Bad capacitor placement (2 capacitors sharing only 1 ground via)

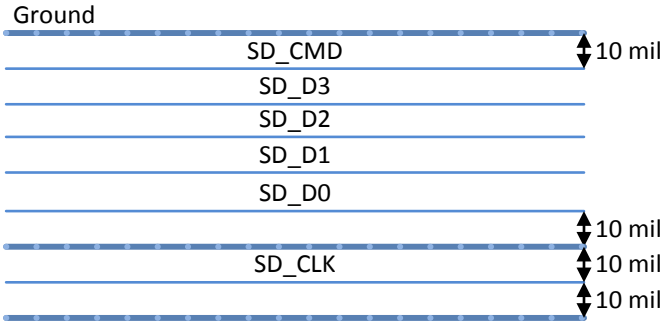
2.1.2 GND

Avoid large ground planes without ground vias. The ground plane shown in Figure 2-1 can act like an antenna radiating unwanted signals to other parts of the reference board.

Figure 2-1 Ground plane without ground vias

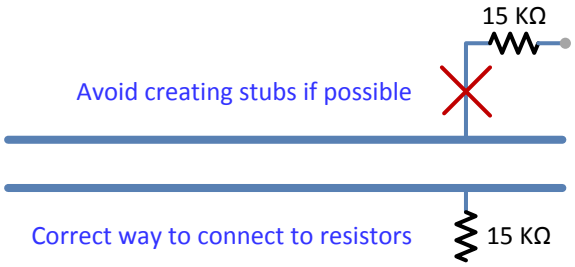
2.1.3 SDIO

- Use ground trace for SDIO routing to isolate SD_CLK.
- Avoid routing parallel to SD_CLK (above, underneath, and on both sides); SD_CLK can run up to 50 MHz and can couple to other traces.
- Keep the reference ground plane of SDIO lines as solid as possible.
- Route SDIO lines on inner layers to avoid picking up noise.



2.2 USB

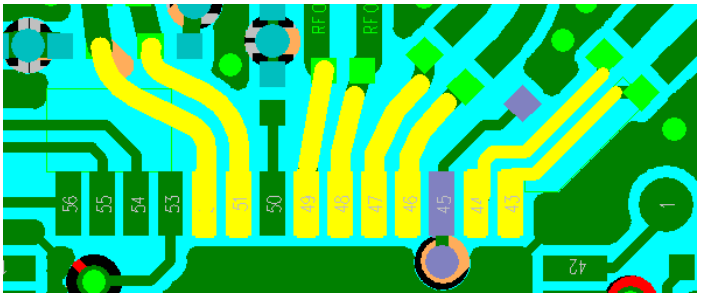
- Use 90 Ω differential lines to rout USB D+/D-.
- Avoid routing USB lines close to the edge of the board.
- Avoid routing USB lines with 90° turns. Use 45° transition.
- Avoid placing stub components on the USB data lines.



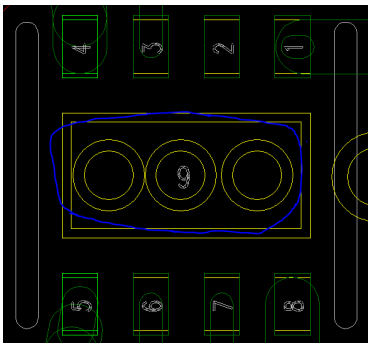
2.3 RF design for Wi-Fi modules

This section relates more to the Wi-Fi modules than the SP140 reference board.

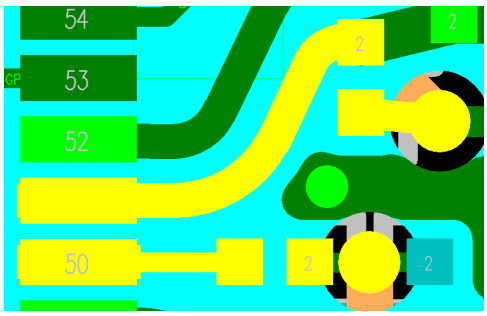
- Route all differential and single-ended traces for RF signal with an impedance of 50 Ω. Avoid right angle line routing.
- Keep the length of the RF differential output traces as short as possible.



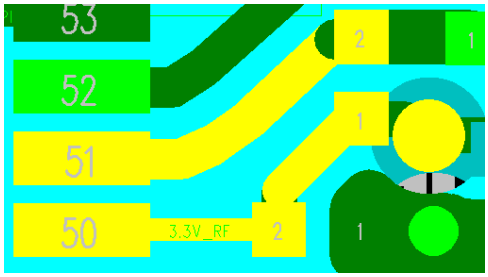
- Place three ground vias under the bottom of the RF switch.



- Use vias to tie all the power pins to the power traces or power plane. Do not make the power pins share the same VDD via.

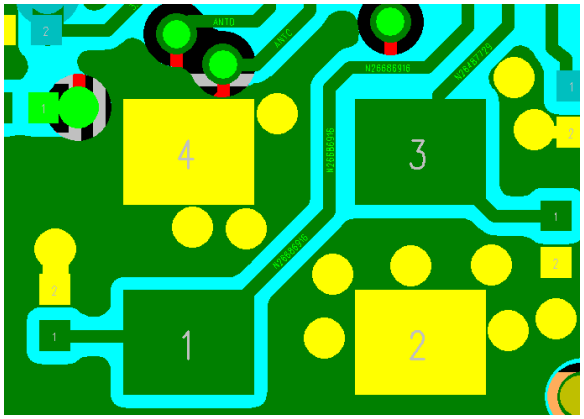


Good: Pin 50 and 51 have dedicated vias tied to 3.3 V power plane on layer 3

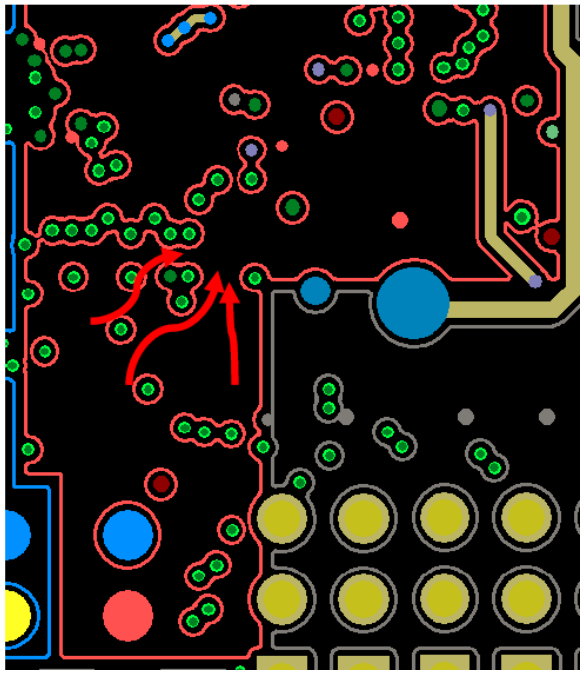


Bad: Pin 50 and 51 share one via tied to 3.3 V power plane on layer 3

- Avoid power trace routing underneath the QCA4002/QCA4004
- Enclose the crystal traces with ground plane and avoid routing power traces underneath the crystal.



- If power planes are used, avoid via holes badly breaking the integrity of the power plane. The following figure shows how via holes can block the current path on the power plane.



Example: Via holes blocking the current path on the power plane

2.4 Board stack-up

The SP140 reference design is implemented on a four-layer board:

- Layer 1 is for RF and signal traces.
- Layer 2 is the ground plane.
- Layer 3 is mostly power plane.
- Layer 4 is for signal traces.

The SP140 is comprised of the elements listed in this section, with the board stack-up as shown in Figure 2-2.

- 4-layer board
- Total stack thickness: 63 mil/1.6 mm
- Material: FR4 Tg 140
- Dielectric constant @ 5 GHz: 4.25
- Impedance @ 2.4 GHz: 50 Ω

Figure 2-2 SP140 board stack-up

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