# NCP508

# Very Low Noise, Fast Turn On, 50 mA Low Dropout Voltage Regulator

The NCP508 is a 50 mA low noise voltage regulator, designed to exhibit fast turn on time and high ripple rejection. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP508 has been designed for use with ceramic capacitors. The device is housed in SC−88A and WDFN6 1.5x1.5 packages. Standard voltage versions are 1.5, 1.8, 2.5, 2.8, 3.0, and 3.3. Other voltages are available in 100 mV steps.

### Features

- Very Low Noise at 39 μVrms without a Bypass Capacitor
- High Ripple Rejection of 70 dB at 1 kHz
- Low Dropout Voltage of 140 mV (typ) at 30 mA
- Tight Load Regulation, typically 6 mV for $\Delta I_{out}$ = 50 mA
- Fast Enable Turn−On time of 20 μsec
- Logic Level Enable
- ESR can vary from a few mΩ to 3 Ω
- These are Pb−Free Devices

### Typical Applications

- RF Subsystems in Handsets
- Noise Sensitive Circuits; VCOs, PLL

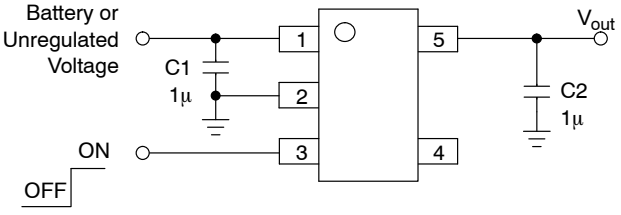
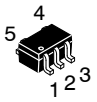



**Figure 1. Typical Application Diagram**

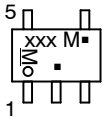
**ON Semiconductor®**

**http://onsemi.com**



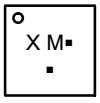
**SC70−5/SC−88A/SOT−353**
**SQ SUFFIX**
**CASE 419A**

**MARKING DIAGRAM**



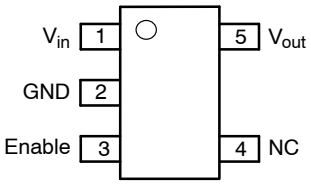

XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

**WDFN6**
**MN SUFFIX**
**CASE 511BJ**

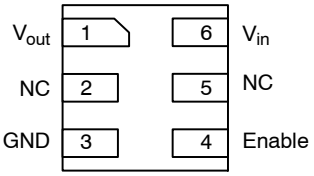



X = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

**PIN CONNECTIONS**




SC−88A
(Top View)




WDFN6
(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | $V_{in}$ | Positive power supply input voltage |
| 2 | GND | Power supply ground |
| 3 | Enable | This input is used to place the device into low−power stand by. When this input is pulled low, the device is disabled. If this function is not used, Enable should be connected to $V_{in}$. |
| 4 | N/C | Not connected pin |
| 5 | $V_{out}$ | Regulated output voltage |

## MAXIMUM RATING

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage | $V_{in(max)}$ | 13.0 | V |
| Enable Voltage | Enable | −0.3 to $V_{in(max)}$ + 0.3 | V |
| Output Voltage | $V_{out}$ | −0.3 to $V_{in(max)}$ + 0.3 | V |
| Power Dissipation and Thermal Characteristics (SC−88A)<br>Power Dissipation<br>Thermal Resistance, Junction−to−Ambient (Note 4) | <br>$P_D$<br>$R_{\theta JA}$ | <br>Internally Limited<br>200 | <br>W<br>°C/W |
| Power Dissipation and Thermal Characteristics (WDFN6)<br>Power Dissipation<br>Thermal Resistance, Junction−to−Ambient (Note 4) | <br>$P_D$<br>$R_{\theta JA}$ | <br>Internally Limited<br>313 | <br>W<br>°C/W |
| Maximum Junction Temperature | $T_J$ | +125 | °C |
| Operating Ambient Temperature | $T_A$ | −40 to +85 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +150 | °C |
| Lead Soldering Temperature @ 260°C | $T_{solder}$ | 10 | sec |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015.
   Machine Model Method 200 V
2. Latch up Capability (85°C) ± 100 mA DC with trigger voltage
3. Maximum package power dissipation limits must be observed.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

4. $R_{\theta JA}$ on a 30 x 30 mm PCB Cu thickness 1 oz; $T_A$ = 25°C.

## RECOMMENDED OPERATING CONDITIONS

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Maximum Operating Input Voltage | $V_{in}$ | 7.0 | V |

**ELECTRICAL CHARACTERISTICS** ($V_{in}$ = $V_{out(nom)}$ + 1.0 V, $V_{enable}$ = $V_{in}$, $C_{in}$ = 1.0 μF, $C_{out}$ = 1.0 μF, $T_J$ = 25°C, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage Tolerance ($T_A$ = 25°C, $I_{out}$ = 10 mA) | $V_{out}$ | −2 | – | +2 | % |
| Output Voltage Tolerance ($T_A$ = −40°C to 85°C, $I_{out}$ = 10 mA) | $V_{out}$ | −3 | – | +3 | % |
| Line Regulation ($V_{in}$ = $V_{out}$ + 1 V to 12 V, $I_{out}$ = 10 mA) (Note 5) | $Reg_{line}$ | – | 2 | 20 | mV |
| Load Regulation ($I_{out}$ = 1.0 mA to 50 mA) (Note 5) | $Reg_{load}$ | – | 6 | 40 | mV |
| Output Current ($V_{out}$ = $V_{out(nom)}$ − 0.1 V) | $I_{out(nom)}$ | 50 | – | – | mA |
| Dropout Voltage ($V_{out}$ = 3.0 V, Measured at $V_{out}$ − 100 mV)<br>$I_{out}$ = 30 mA<br>$I_{out}$ = 40 mA<br>$I_{out}$ = 50 mA | $V_{in}$–$V_{out}$ | <br>–<br>–<br>– | <br>140<br>155<br>180 | <br>250<br>300<br>– | mV |
| Quiescent Current<br>(Enable Input = 0V) | $I_Q$ | <br>– | <br>0.1 | <br>1 | μA |
| Ground Current<br>(Enable Input = $V_{in}$, $V_{in}$ = $V_{out}$ + 1 V, $I_{out}$ = 0 mA)<br>(Enable Input = $V_{in}$, $I_{out}$ = 1 mA)<br>(Enable Input = $V_{in}$, $I_{out}$ = 10 mA)<br>(Enable Input = $V_{in}$, $I_{out}$ = 50 mA) | $I_{GND}$ | <br>–<br>–<br>–<br>– | <br>145<br>160<br>300<br>1100 | <br>200<br>260<br>500<br>1900 | μA |
| Enable Input Threshold Voltage<br>(Voltage Increasing, Output Turns On, Logic High)<br>(Voltage Decreasing, Output Turns Off, Logic Low) | $V_{th(en)}$ | <br>0.9<br>– | <br>–<br>– | <br>–<br>0.15 | V |
| Enable Input Current ($V_{enable}$ = 2.4 V) | $I_{enable}$ | – | 8.0 | 15 | μA |
| Output Turn On Time (Note 6) | – | – | 20 | – | μs |
| Output Short Circuit Current Limit ($V_{out}$ = 0 V) | $I_{out(max)}$ | 100 | 250 | – | mA |
| Ripple Rejection ($V_{in}$ = $V_{out(nom)}$ + 1 Vdc + 0.5 $V_{pp}$, f = 1 kHz, Io = 10 mA) | RR | – | 70 | – | dB |
| Output Noise Voltage (f = 100 Hz to 100 kHz) ($V_{out}$ = 1.5 V) | $V_n$ | – | 39 | – | μVrms |

5. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. Turn on time is defined from Enable at 10% to $V_{out}$ at 95% nominal value. Min and max values $T_A$ = −40°C to 85°C, $T_{jmax}$ = 125°C. $V_{enable}$ = 0 V to $V_{in}$. $C_{out}$ = 1.0 μF.

## TYPICAL CHARACTERISTICS

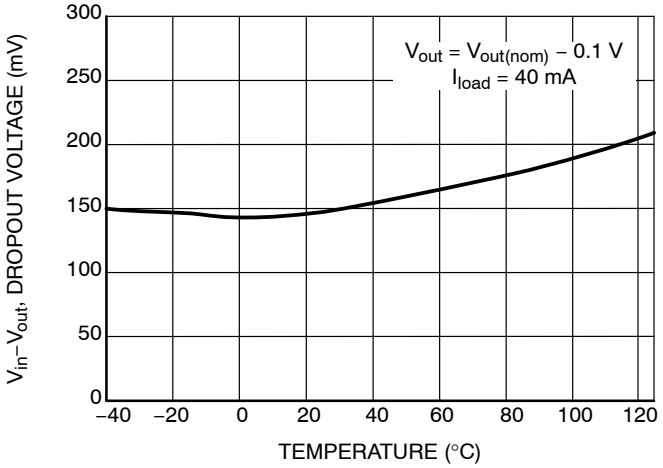



**Figure 2. Dropout Voltage vs. Temperature, 1.5 V**

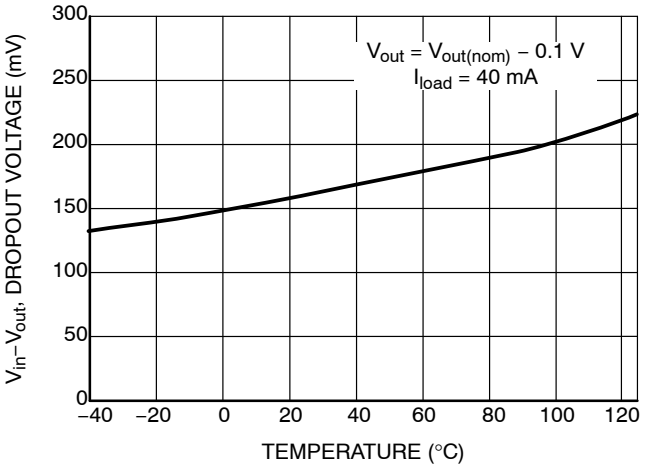



**Figure 3. Dropout Voltage vs. Temperature, 3.3 V**

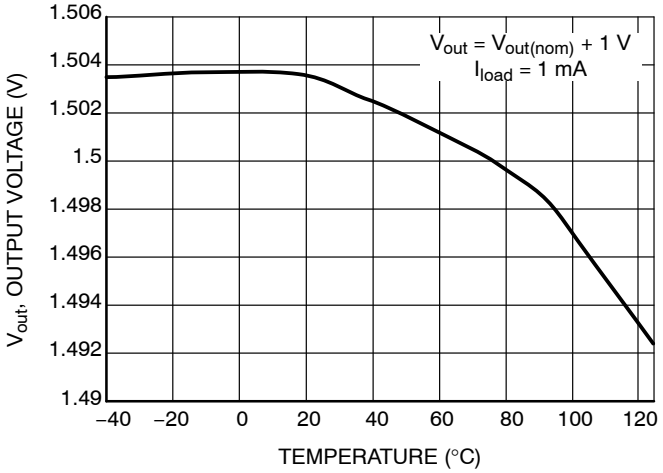



**Figure 4. Output Voltage vs. Temperature, 1.5 V**

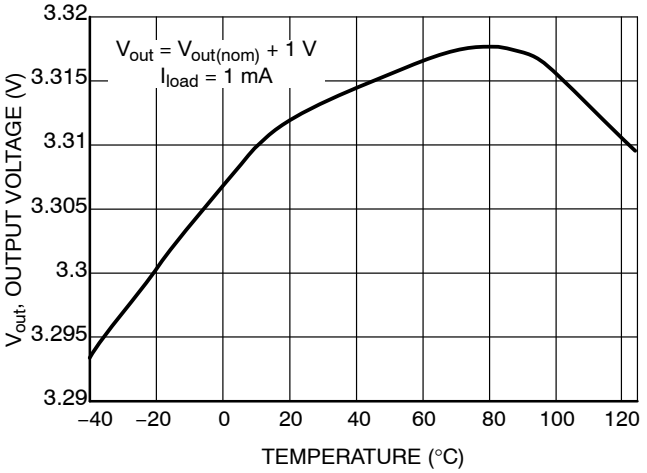



**Figure 5. Output Voltage vs. Temperature, 3.3 V**

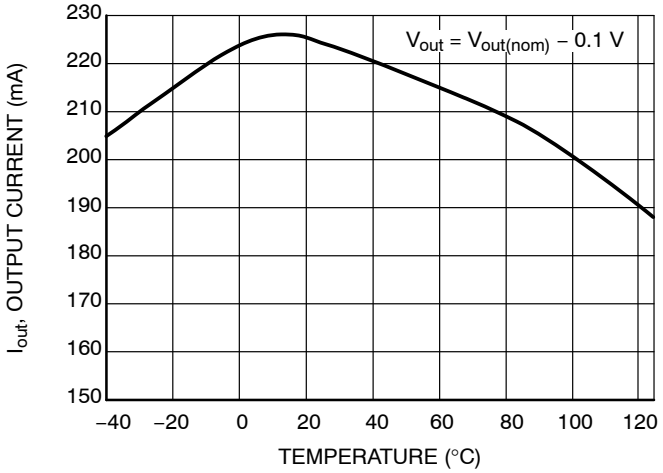



**Figure 6. Output Current Limit vs. Temperature, 1.5 V**

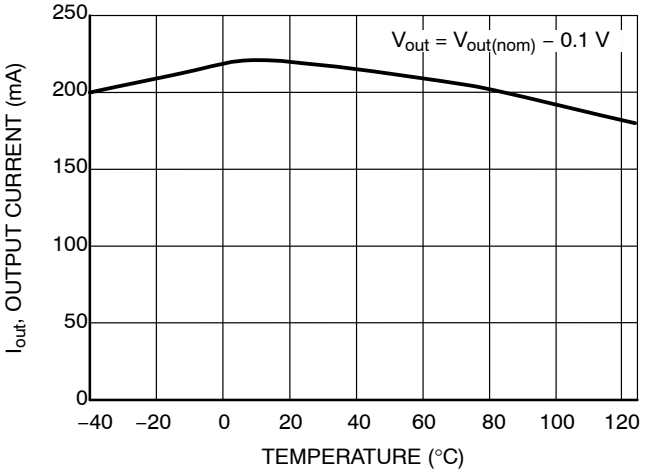



**Figure 7. Output Current Limit vs. Temperature, 3.3 V**

## TYPICAL CHARACTERISTICS

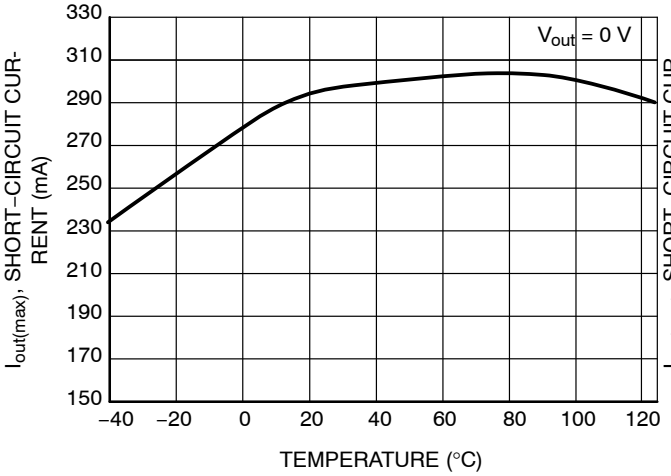



**Figure 8. Short−Circuit Current Limit vs. Temperature, 1.5 V**

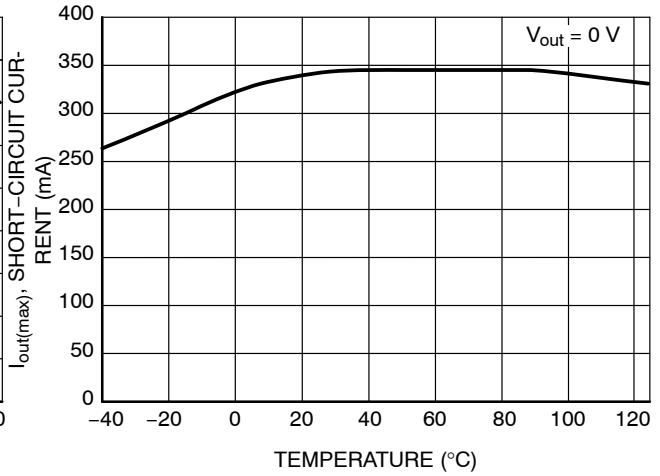



**Figure 9. Short−Circuit Current Limit vs. Temperature, 3.3 V**

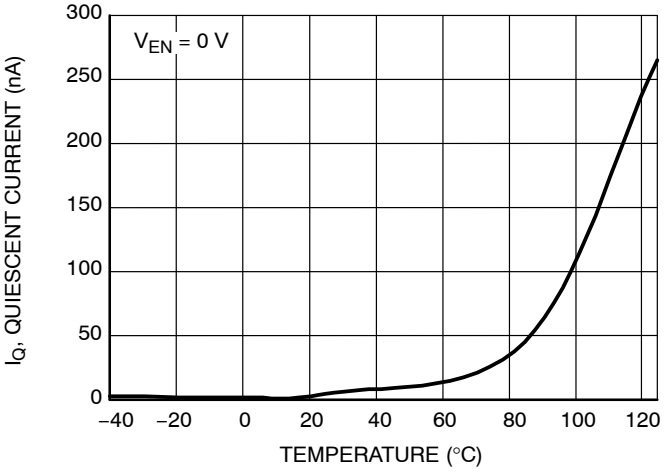



**Figure 10. Quiescent Current vs. Temperature, 1.5 V**

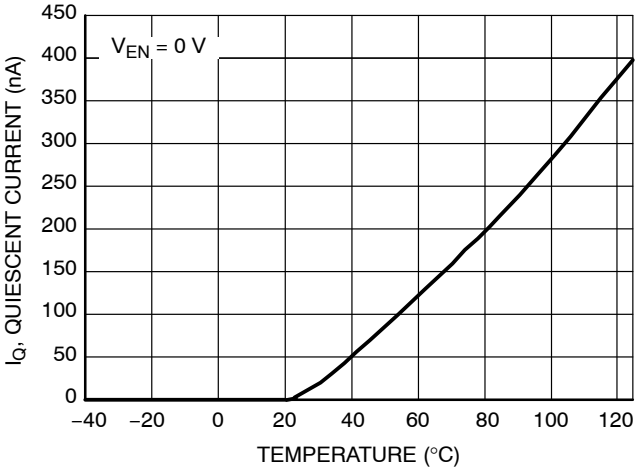



**Figure 11. Quiescent Current vs. Temperature, 3.3 V**

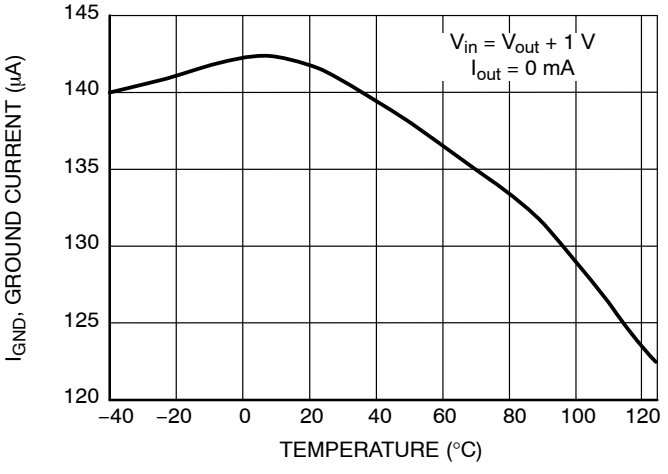



**Figure 12. Ground Current vs. Temperature, 1.5 V**

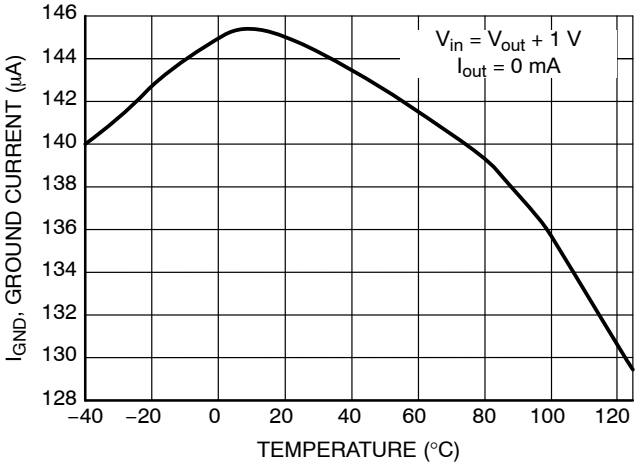



**Figure 13. Ground Current vs. Temperature, 3.3 V**

## TYPICAL CHARACTERISTICS

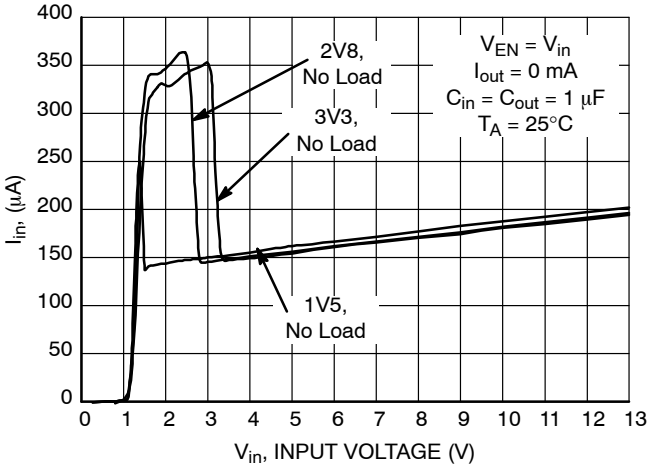



**Figure 14. Quiescent Current vs. Input Voltage**

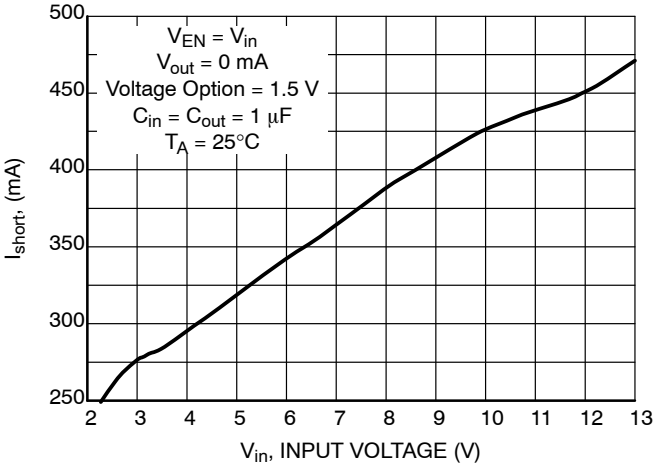



**Figure 15. Output Short−Circuit Current vs. Input Voltage**

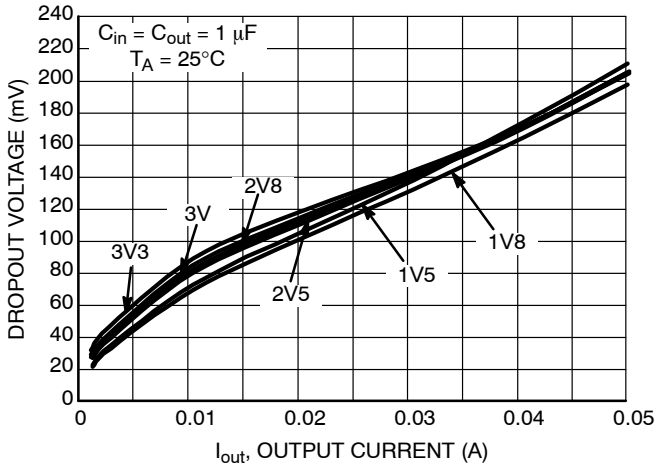



**Figure 16. Dropout Voltage vs. Output Current**

## TYPICAL CHARACTERISTICS

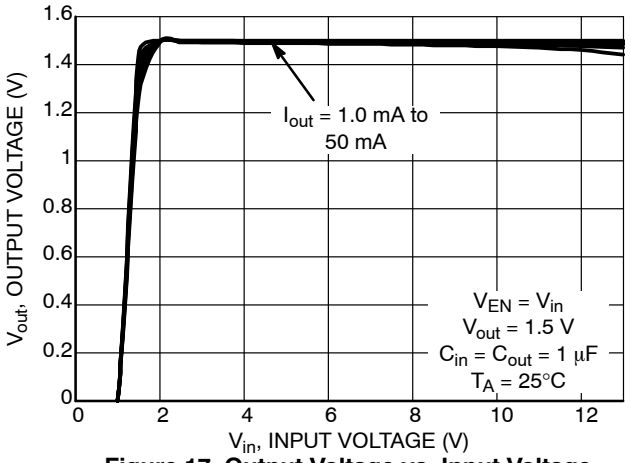



**Figure 17. Output Voltage vs. Input Voltage**

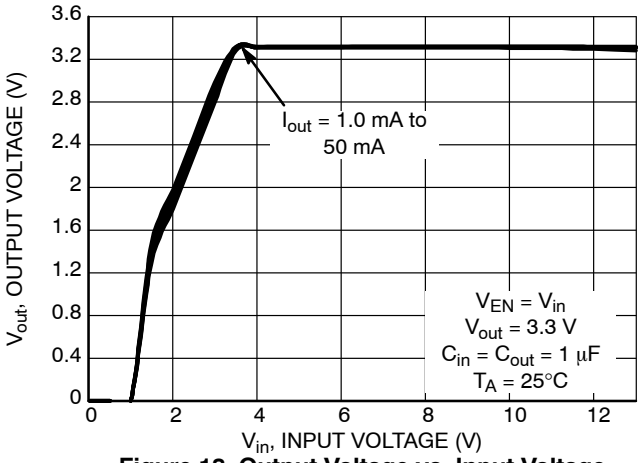



**Figure 18. Output Voltage vs. Input Voltage**

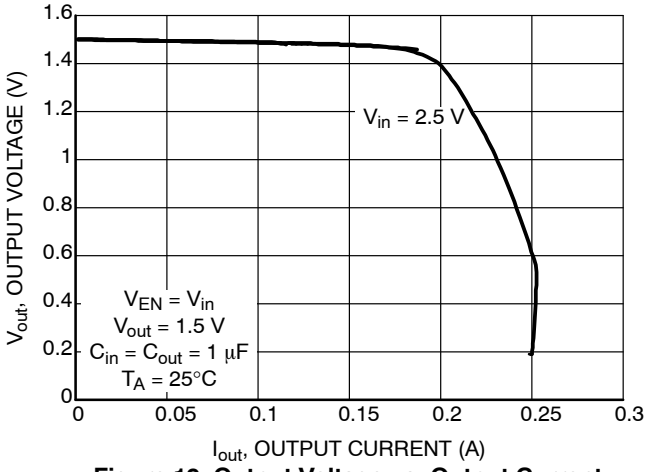



**Figure 19. Output Voltage vs. Output Current**

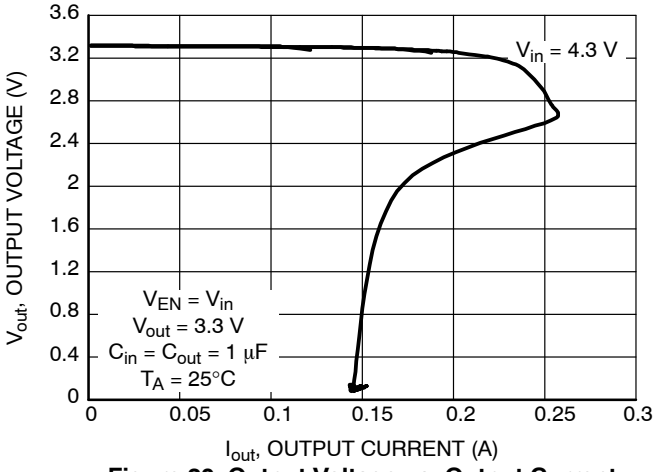



**Figure 20. Output Voltage vs. Output Current**

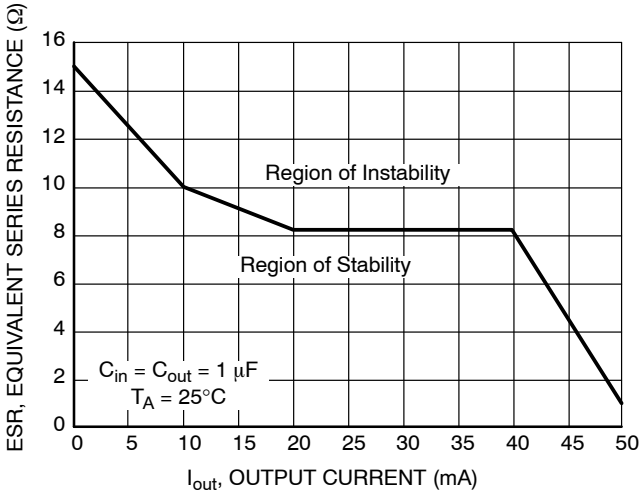



**Figure 21. Equivalent Series Resistance vs. Output Current, X7R, MLCC Capacitor**

## TYPICAL CHARACTERISTICS

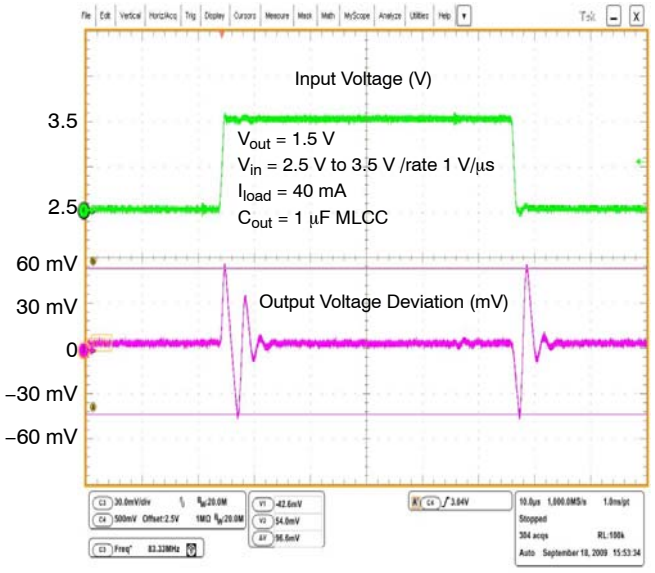



**Figure 22. Line Transient Response 1.5 V/40 mA**

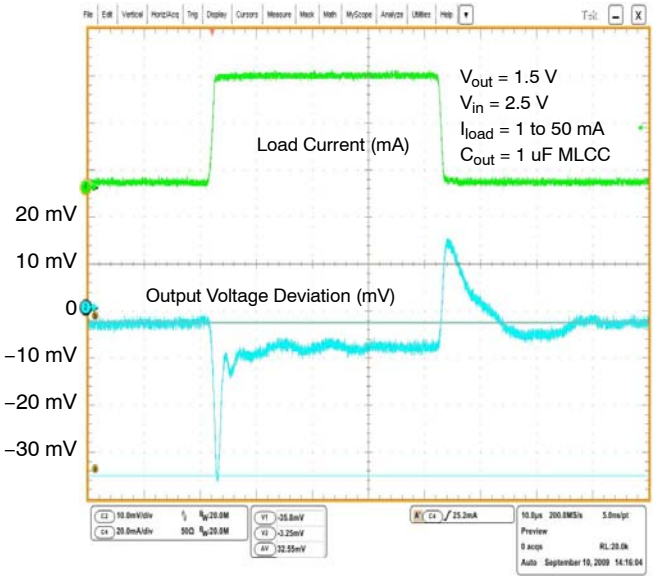



**Figure 23. Load Transient Response 1.5 V**

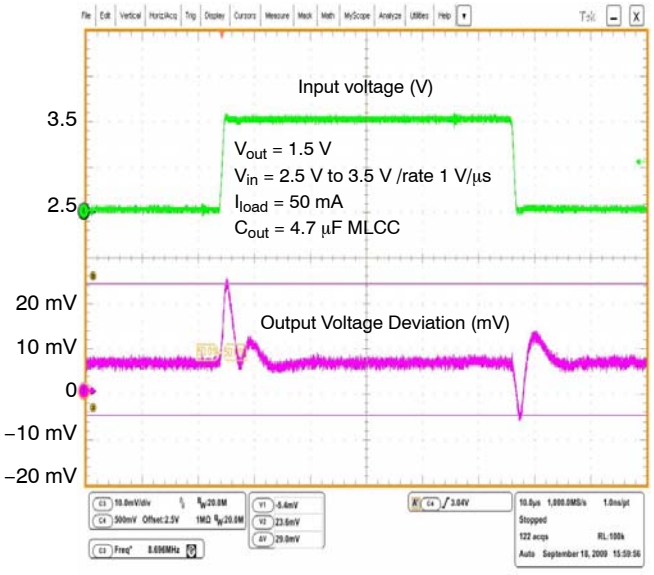



**Figure 24. Line Transient Response 1.5 V/50 mA**

## TYPICAL CHARACTERISTICS

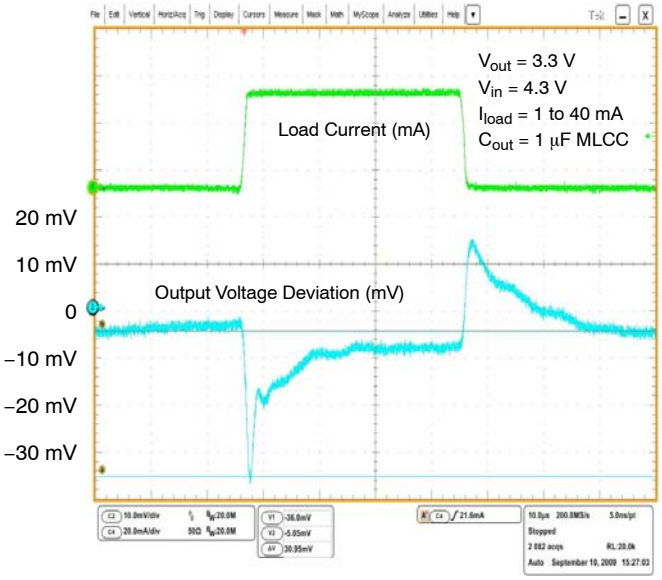



**Figure 25. Load Transient Response 3.3 V**

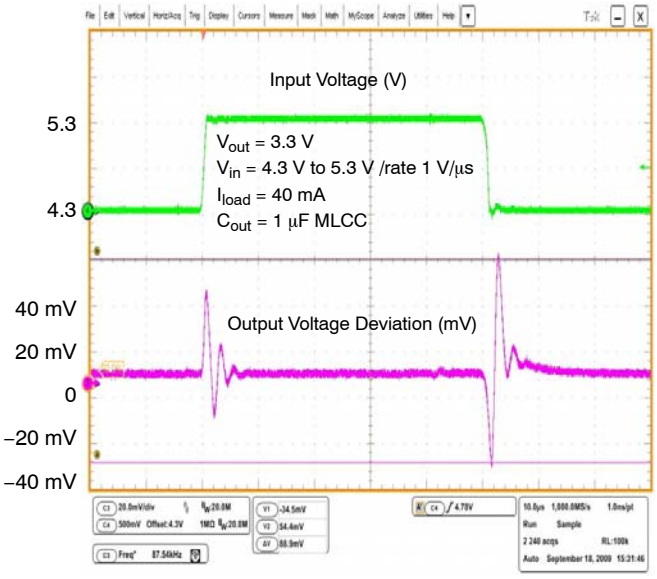



**Figure 26. Line Transient Response 3.3 V/40 mA**

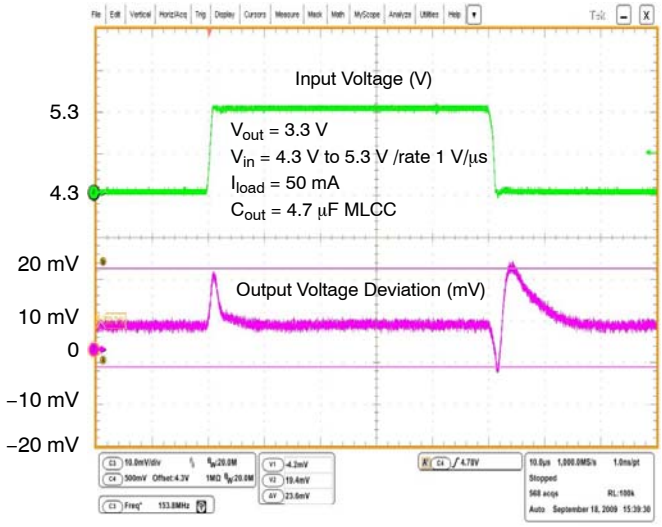



**Figure 27. Line Transient Response 3.3 V/50 mA**

## TYPICAL CHARACTERISTICS

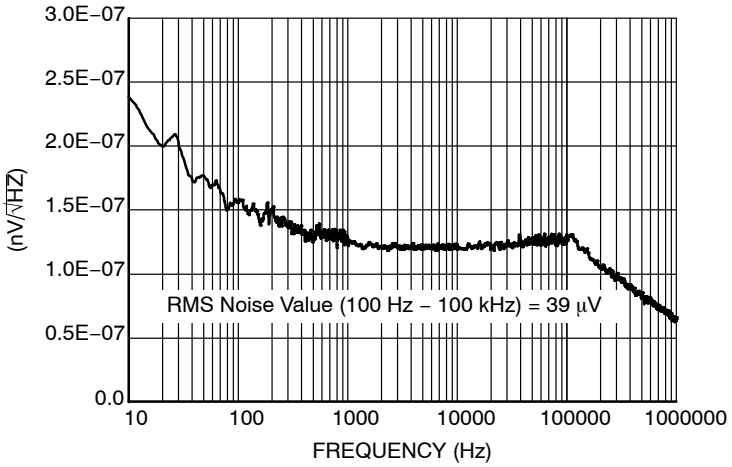



**Figure 28. Output Voltage Noise**
**$V_{out}$ = 1.5 V, $I_{out}$ = 40 mA**

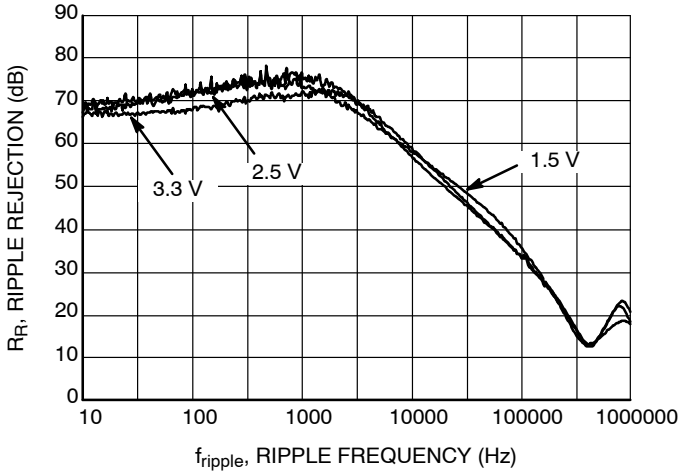



**Figure 29. Ripple Rejection vs. Frequency**
**$I_{out}$ = 40 mA, 0.5 $V_{pp}$**

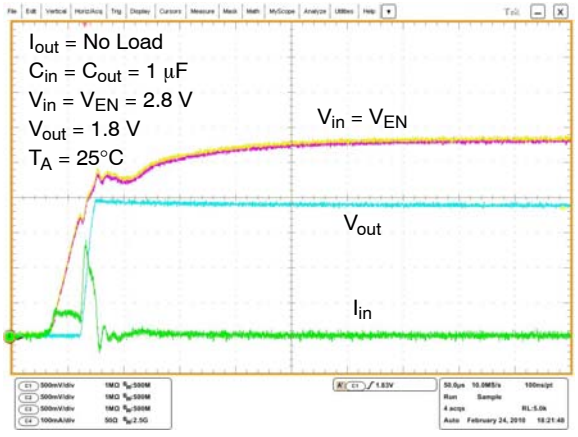



**Figure 30. Startup, No Load**

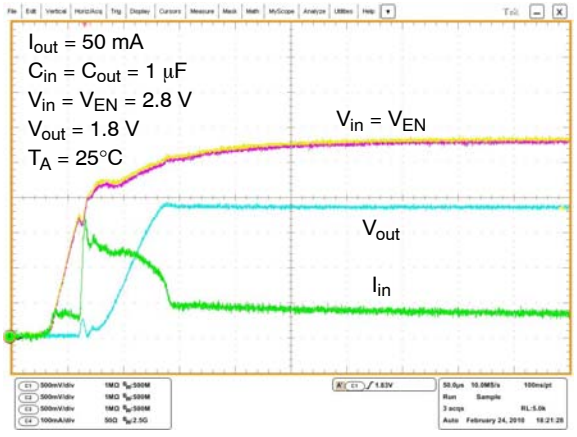



**Figure 31. Startup, $I_{out}$ = 50 mA**

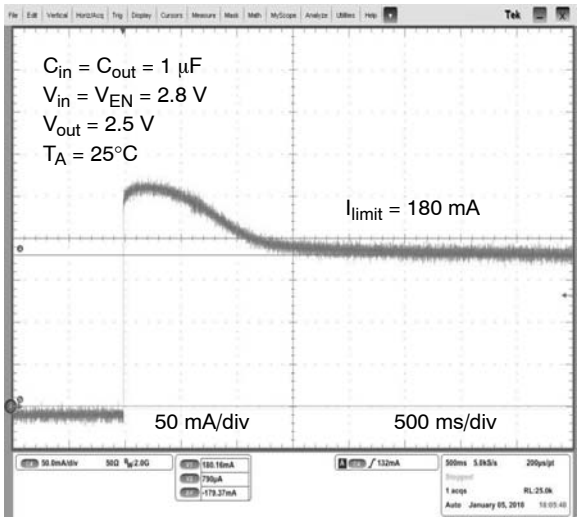



Figure 32. Hard Short−Circuit Current (by Copper Wires)

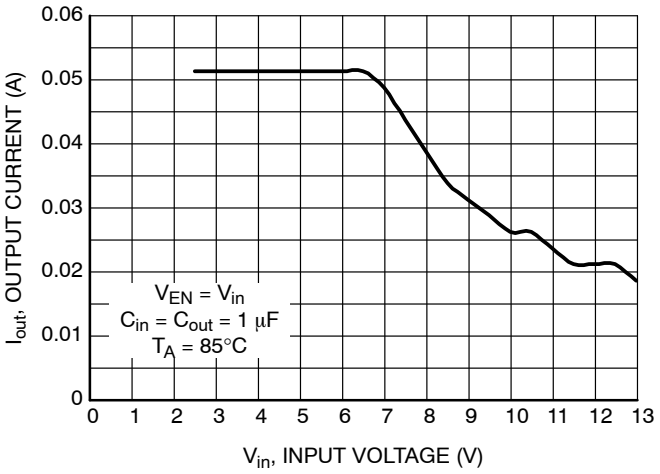



**Figure 33. Measured Power Operating Area, 1.5 V, $T_A$ = 85°C, $V_{out\_drop}$ = max 0.1 V**

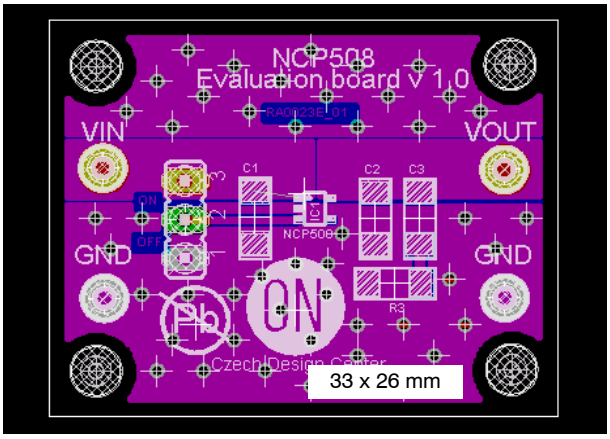



Figure 34. Evaluation Board

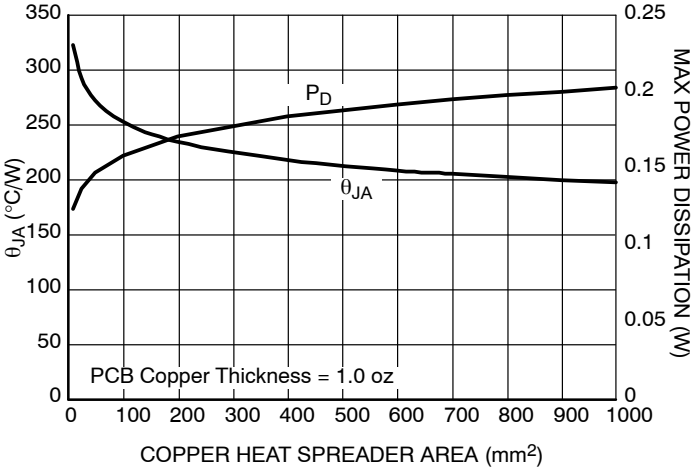



**Figure 35. SC70−5 Thermal Resistance vs. Copper Heat Spreader Area**

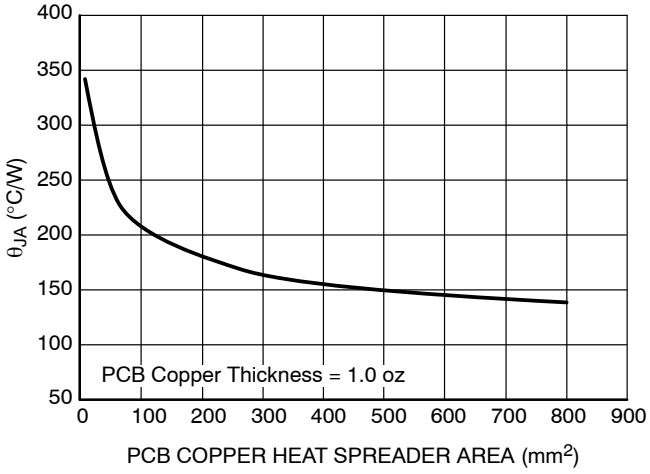



**Figure 36. WDFN6 Thermal Resistance vs. Copper Heat Spreader Area**

## DEFINITIONS

### Load Regulation

The change in output voltage for a change in output current at a constant temperature.

### Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

### Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

### Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

### Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

### Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

### Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 125°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

### Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 150°C. Depending on the ambient power dissipation and thus the maximum available output current.

## APPLICATIONS INFORMATION

Typical application circuit for the NCP508 series is shown in Figure 1.

### Input Decoupling (C1)

An input capacitor of at least 1.0 μF,(ceramic or tantalum) is recommended to improve the transient response of the regulator and/or if the regulator is located more than a few inches from the power source. It will also reduce the circuit's sensitivity to the input line impedance at high frequencies. The capacitor should be mounted with the shortest possible track length directly across the regular's input terminals. Higher values and lower ESR will improve the overall line transient response.

### Output Decoupling (C2)

The NCP508 is a stable regulator and does not require a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3 Ω can safely be used. The minimum decoupling value is 1.0 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

### Enable Operation

The enable pin will turn on or off the regulator. The limits of threshold are covered in the electrical specification section of this datasheet. If the enable is not used then the pin should be connected to $V_{in}$.

### Hints

Please be sure the $V_{in}$ and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

### Thermal Considerations

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded.

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP508 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

where:

- $T_{J\{max)}$ is the maximum allowable junction temperature of the die, which is 150°C
- $T_A$ is the ambient operating temperature
- $R_{\theta ja}$ is dependent on the surrounding PCB layout

## ORDERING INFORMATION

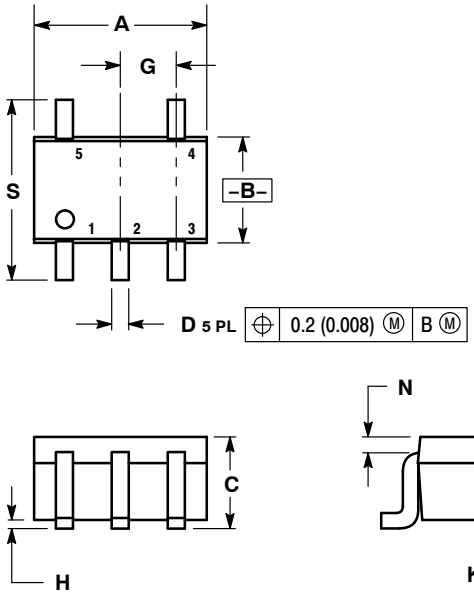
| Device | Nominal Output Voltage | Marking | Package | Shipping† |
|---|---|---|---|---|
| NCP508SQ15T1G | 1.5 | D5A | SC−88A (Pb−Free) | 3000 / Tape & Reel |
| NCP508SQ18T1G | 1.8 | D5C | SC−88A (Pb−Free) | 3000 / Tape & Reel |
| NCP508SQ25T1G | 2.5 | D5D | SC−88A (Pb−Free) | 3000 / Tape & Reel |
| NCP508SQ28T1G | 2.8 | D5E | SC−88A (Pb−Free) | 3000 / Tape & Reel |
| NCP508SQ30T1G | 3.0 | D5F | SC−88A (Pb−Free) | 3000 / Tape & Reel |
| NCP508SQ33T1G | 3.3 | D5G | SC−88A (Pb−Free) | 3000 / Tape & Reel |
| NCP508MT15TBG | 1.5 | B | WDFN6 (Pb−Free) | 3000 / Tape & Reel |
| NCP508MT18TBG | 1.8 | A | WDFN6 (Pb−Free) | 3000 / Tape & Reel |
| NCP508MT25TBG | 2.5 | C | WDFN6 (Pb−Free) | 3000 / Tape & Reel |
| NCP508MT28TBG | 2.8 | D | WDFN6 (Pb−Free) | 3000 / Tape & Reel |
| NCP508MT30TBG | 3.0 | E | WDFN6 (Pb−Free) | 3000 / Tape & Reel |
| NCP508MT33TBG | 3.3 | F | WDFN6 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

## PACKAGE DIMENSIONS

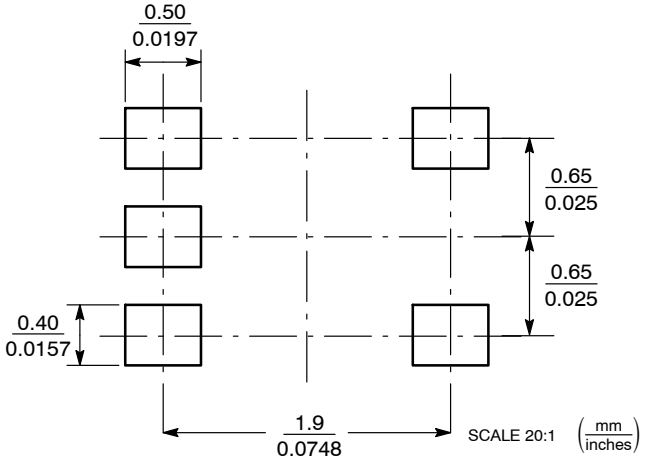
**SC70−5, SC−88A, SOT−353**
**SQ SUFFIX**
CASE 419A−02
ISSUE J




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

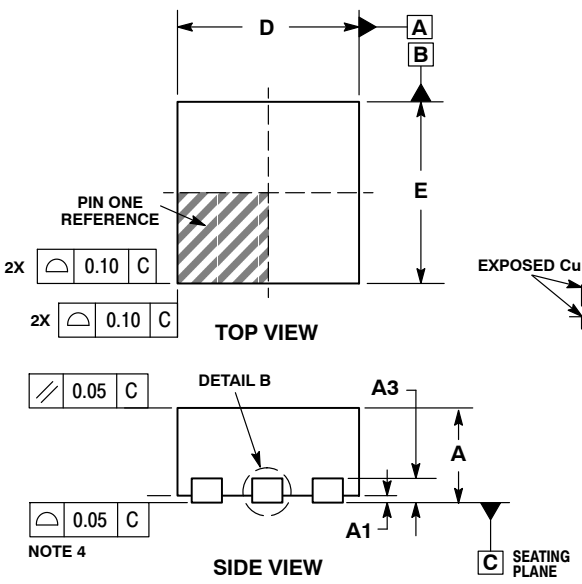
## SOLDERING FOOTPRINT*

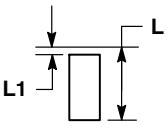



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

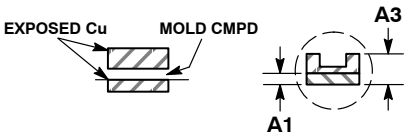
## PACKAGE DIMENSIONS

**WDFN6 1.5x1.5, 0.5P**
CASE 511BJ−01
ISSUE B



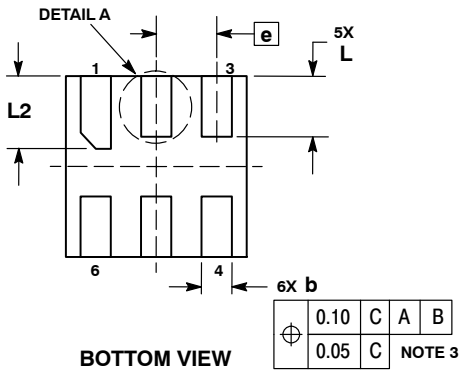

**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**




**DETAIL B**
**ALTERNATE CONSTRUCTIONS**

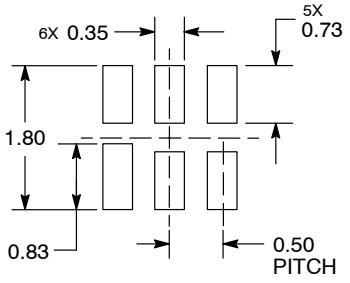
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 1.50 BSC | |
| E | 1.50 BSC | |
| e | 0.50 BSC | |
| L | 0.40 | 0.60 |
| L1 | --- | 0.15 |
| L2 | 0.50 | 0.70 |




**BOTTOM VIEW**

### RECOMMENDED MOUNTING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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