REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes IAW NOR 5962-R030-93 - wlm.	93-01-22	Monica L. Poelking
B	Changes IAW NOR 5962-R034-96 - jak.	96-02-29	Monica L. Poelking
C	Change drawing CAGE code to 67268. Update boilerplate to MIL-PRF-38535 requirements. - jak	01-11-15	Thomas M. Hess
D	Add vendor code 0C7V7 and 0DKS7. Update boilerplate to MIL-PRF-38535 requirements. -phn	08-05-27	Thomas M. Hess

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS OF SHEETS															
REV	D	D	D	D	D	D	D	D	D	D	D			
SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

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DRAWING APPROVAL DATE
86-09-04

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, HEX SCHMITT TRIGGER, MONOLITHIC SILICON

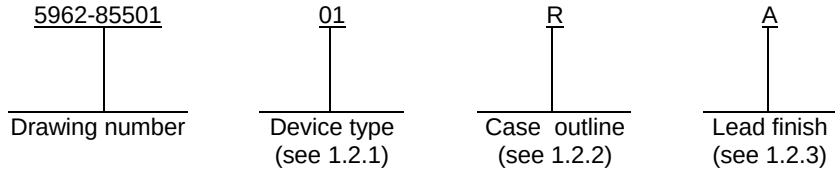
SIZE	CAGE CODE	
A	**67268**	**5962-85501**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	40106B	Hex Schmitt trigger
02	14584	Hex Schmitt trigger

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD}) ..... -0.5 V dc to +18 V dc
Input voltage range ..... -0.5 V dc to V_{DD} +0.5 V dc
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW 2/
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{DD}) ..... +3.0 V dc to +15 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C to 200 mW.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 and QML-38535 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Table I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High-level output voltage	V_{OH}	V_{IN} = 0.0 V or V_{DD} $\lvert I_O \rvert$ < 1.0 µA	V_{DD} = 5.0 V dc	All	1, 2, 3	4.95		V
			V_{DD} = 10.0 V dc			9.95		
			V_{DD} = 15.0 V dc			14.95		
Low-level output voltage	V_{OL}	V_{IN} = 0.0 V or V_{DD} $\lvert I_O \rvert$ < 1.0 µA	V_{DD} = 5.0 V dc	All			0.05	V
			V_{DD} = 10.0 V dc				0.05	
			V_{DD} = 15.0 V dc				0.05	
High-level input voltage	V_{IH}	V_{DD} = 5.0 V dc V_O = 0.5 V dc or 4.5 V dc		01	1, 2, 3	4.3		V
				02		3.5		
		V_{DD} = 10.0 V dc V_O = 1.0 V dc or 9.0 V dc		01		8.6		
				02		7.0		
		V_{DD} = 15.0 V dc V_O = 1.5 V or 13.5 V dc $\lvert I_O \rvert$ < 1.0 µA		01		12.9		
				02		11.0		
Low-level input voltage	V_{IL}	V_{DD} = 5.0 V dc V_O = 0.5 V dc or 4.5 V dc		01	1, 2, 3		0.7	V
				02			1.5	
		V_{DD} = 10.0 V dc V_O = 1.0 V dc or 9.0 V dc		01			1.4	
				02			3.0	
		V_{DD} = 15.0 V dc V_O = 1.5 V dc or 13.5 V dc $\lvert I_O \rvert$ < 1.0 µA		01			2.1	
				02			4.0	
High-level output current	I_{OH}	V_{DD} = 5.0 V dc V_O = 4.6 V dc V_{IN} = 0.0 V or V_{DD}		All	3		-0.64	mA
					1		-0.51	
					2		-0.36	
		V_{DD} = 10.0 V dc V_O = 9.5 V dc V_{IN} = 0.0 V or V_{DD}			3		-1.6	
					1		-1.3	
					2		-0.9	
		V_{DD} = 15.0 V dc V_O = 13.5 V dc V_{IN} = 0.0 V or V_{DD}			3		-4.2	
					1		-3.4	
					2		-2.4	
Low-level output current	I_{OL}	V_{DD} = 5.0 V dc V_O = 0.4 V dc V_{IN} = 0.0 V dc or V_{DD}		All	3	0.64		mA
					1	0.51		
					2	0.36		
		V_{DD} = 10.0 V dc V_O = 0.5 V dc V_{IN} = 0.0 V dc or V_{DD}			3	1.6		
					1	1.3		
					2	0.9		
		V_{DD} = 15.0 V dc V_O = 1.5 V dc V_{IN} = 0.0 V dc or V_{DD}			3	4.2		
					1	3.4		
					2	2.4		

Table I. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input current	I_{IN}	V_{IN} = 0.0 V dc or 15 V dc	All	1, 3		±0.1	µA
				2		±1.0	
Quiescent supply current	I_{DD}	V_{DD} = 5.0 V dc V_{IN} = 0.0 V dc or V_{DD}	01	1, 3		1.0	µA
				2		30.0	
			02	1, 3		0.25	
				2		7.5	
		V_{DD} = 10.0 V dc V_{IN} = 0.0 V dc or V_{DD}	01	1, 3		2.0	
				2		60.0	
			02	1, 3		0.5	
				2		15.0	
		V_{DD} = 15.0 V dc V_{IN} = 0.0 V dc or V_{DD}	01	1, 3		4.0	
				2		120.0	
			02	1, 3		1.0	
				2		30.0	
Input capacitance	C_{IN}	V_{IN} = 0.0 V dc, T_A = +25°C	All	4		7.5	pF
Functional tests		See 4.3.1d	All	7			
Positive going threshold voltage	V_{T+}	V_{DD} = 5.0 V dc	01	1, 2, 3	3.0	4.3	V
			02		1.7	3.5	
		V_{DD} = 10.0 V dc	01		6.0	8.6	
			02		3.2	7.0	
		V_{DD} = 15.0 V dc	01		9.0	12.9	
			02		5.2	10.6	
Negative going threshold voltage	V_{T-}	V_{DD} = 5.0 V dc	01	1, 2, 3	0.7	2.0	V
			02		1.5	3.3	
		V_{DD} = 10.0 V dc	01		1.4	4.0	
			02		3.0	6.7	
		V_{DD} = 15.0 V dc	01		2.1	6.0	
			02		4.5	9.9	

Table I. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Hysteresis voltage	V_H	V_{DD} = 5.0 V dc	01	1, 2, 3	1.0	3.6	V
		V_{DD} = 10.0 V dc	01	1, 2, 3	2.0	7.2	
		V_{DD} = 15.0 V dc	01	1, 2, 3	3.0	10.8	
		V_{DD} = 5.0 V dc	02	1	0.25	1.0	V
				2	0.21	1.0	
				3	0.27	1.0	
		V_{DD} = 10.0 V dc	02	1	0.30	1.2	
				2	0.25	1.2	
				3	0.36	1.3	
		V_{DD} = 15.0 V dc	02	1	0.60	1.5	
				2	0.50	1.4	
				3	0.77	1.7	
Propagation delay time, high-to-low level	t_{PHL}	V_{DD} = 5.0 V dc C_L = 50 pF R_L = 200 kΩ	01	9		300.0	ns
				10, 11		390.0	
			02	9		250.0	
				10, 11		375.0	
Propagation delay time, low-to-high level	t_{PLH}	V_{DD} = 5.0 V dc C_L = 50 pF R_L = 200 kΩ	01	9		300.0	ns
				10, 11		390.0	
			02	9		250.0	
				10, 11		375.0	
Transition time	t_{TLH}, t_{THL}	V_{DD} = 5.0 V dc C_L = 50 pF R_L = 200 kΩ	All	9		200.0	ns
				10, 11		300.0	

Case outlines	C		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	V_{SS}	14	V_{DD}

FIGURE 1. Terminal connections.

(Each Inverter)

Inputs	Outputs
mA	mY
L	H
H	L

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

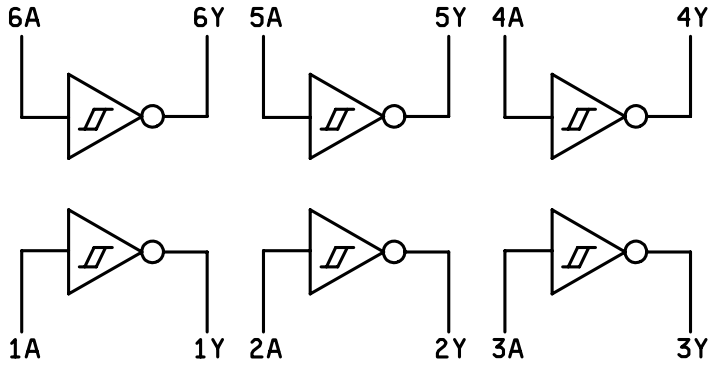
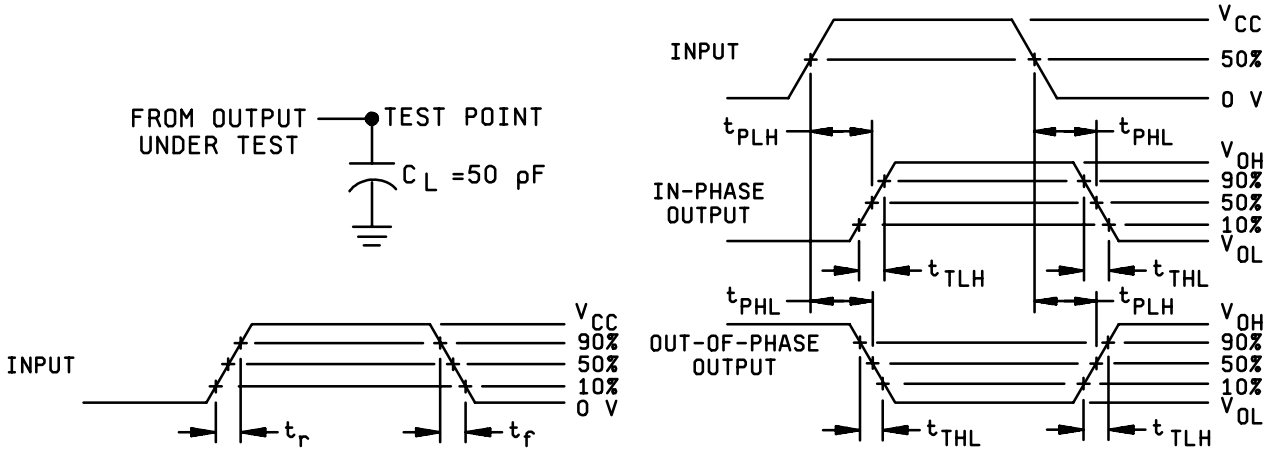


FIGURE 3. Logic diagram.



NOTES
1. C_L = 50 pF (includes probe and jig capacitance).
2. Data rise and fall time (t_r, t_f) = 20 ns.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroup 7 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, and D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1, 2, 3, 7, 9 1/
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10, 11 2/
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

1/ PDA applies to subgroup 1.
2/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 08-02-27

Approved sources of supply for SMD 5962-85501 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8550101CA	3/	MM40106J/883
5962-8550102CA	3/	14584/BCAJC
5962-8550101CA	0C7V7	CD40106BMJ/883
5962-8550102CA	0DKS7	GEM39202QCA
5962-8550102CC	0DKS7	GEM39202QCC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
0DKS7	Sarnoff Corporation 201 Washington Rd Princeton, NJ 08540-5300

X-ON Electronics

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Other Similar products are found below :

5962-8550101CA E5-652Z NL17SGU04P5T5G NL17SZ14P5T5G NLX2G04BMX1TCG 412327H 022413E NL17SG14AMUTCG NLU2G04AMUTCG NLU2GU04BMX1TCG NLV14049UBDR2G NLV14069UBDTR2G NLV17SZ14DFT2G NLVVHC1G05DFT2G 74LVC2G17FW4-7 NLU2G04CMX1TCG NLV17SZ06DFT2G NLV27WZ04DFT2G NLV74HCT14ADTR2G NLX2G14CMUTCG NLU1G04AMX1TCG SNJ54ACT14W SNJ54AC04W NCV1729SN35T1G TC74VHC04FK(EL,K) NLV74HC04ADTR2G NLV17SZ04DFT2G 74AUP2G04FW3-7 NLU1G04AMUTCG NLX2G04CMUTCG NLX2G04AMUTCG NLV74ACT00DR2G NLV74AC14DR2G NLV37WZ14USG NLV27WZ04DFT1G NLV14106BDG NLU1GU04CMUTCG NLU1GT14AMUTCG NLU1G04CMUTCG NL17SZU04P5T5G NL17SG14DFT2G 74LVC06ADTR2G 74LVC04ADR2G TC7SZ04AFS,L3J NLU1GT04AMUTCG NLV37WZ04USG NLX3G14FMUTCG NL17SZ04P5T5G NL17SG14P5T5G NLV27WZU04DFT2G