Fully Integrated GPS Modules

Including Antenna

ORG13XX Series Data Sheet

1. Introduction

ORG13XX Series GPS receiver modules with built-in antenna have been designed to address markets where stand alone operation, high level of integration, power consumption and flexibility are very important.

The ORG13XX series are OriginGPS smallest, autonomous, fully featured GPS engines, optimized for stand alone operation.

Featuring OriginGPS Microstrip Patch Antenna and OriginGPS Noise-Free Zone System™ technology the ORG13XX series offer the ultimate in high sensitivity GPS performance in small size.

The ORG13XX series modules incorporate miniature multi-channel receiver that continuously tracks all satellites in view and provides accurate positioning data in industry's standard NMEA-0183 format. Internal ARM CPU core and sophisticated firmware keep GPS payload off the host and allow integration in low resources embedded solutions.

The ORG13XX series modules are complete SiP (System-in-Package) featuring advanced miniature packaging technology and an ultra small footprint designed to commit unique integration features for high volume, low power and cost sensitive applications.

OriginGPS innovative material engineering approach resulted in Microstrip Patch Antenna with outstanding narrow band performance.
OriginGPS case study of the specifications of key components through involvement in R&D effort of major vendors derived in highest performance in industry's smallest footprint parts available. These components placement using OriginGPS NFZ™ technology created hard-to-achieve laboratory performance in heavy-duty environment.

2. Description

OriginGPS has revised and enhanced the architecture of classic GPS receivers.
In-house designed Microstrip Patch antennas with highest GPS-band performance and notch filtering for out-of band signals provides high selectivity. Furthermore, combined with internal shielding and ground plane the ORG13XX series modules reveal good noise immunity and exceptional sensitivity.
Carefully selected key components including TCXO and LNA resulted in faster TTFF and operation stability under rapid environmental changes.

2.1. Features

- Fully integrated multi channel GPS engine
- Embedded Microstrip Patch antenna
- Noise Free Zone System™ Technology
- SiRFstarIII GSC3LTf chipset
- L1 frequency, C/A code
- 20 channels searching, 12 channels parallel tracking
- Acquisition sensitivity: -157dBm
- Tracking sensitivity: -159dBm for indoor fixes
- Fast TTFF: <35s (typical) under Cold Start conditions
- Rapid TTFF by aiding information upload capability
- Multipath mitigation
- Indoor tracking
- SBAS (WAAS, MSAS, EGNOS) support
- Multi-Mode Assisted GPS (A-GPS) support[1]: Autonomous, MS Based, MS Assisted
- Extended Ephemeris for very fast TTFFs support through SiRF InstantFix[2]
- Automatic and user programmable power saving scenarios
- Low power consumption: 100mW during acquisition
- ARM7 baseband CPU
- Selectable UART or SPI hardware interface
- Programmable UART protocol and message rate
- Selectable NMEA-0183 or SiRF Binary communication standards
- Single operating voltage: 3.3V to 5.5V
- Small footprint: 17mm x 17mm
- Surface Mount Device (SMD)
- Optimized for automatic assembly and reflow equipment
- Industrial operating temperature range: -40^0 to 85^0C
- Pb-Free RoHS compliant

Notes:
1. SiRFLoc® Client (SLC) LT A-GPS Multimode Location Engine™ for GSM/3GPP or for CDMA IS-801A required
2. SiRF InstantFix service required

2.2. Architecture

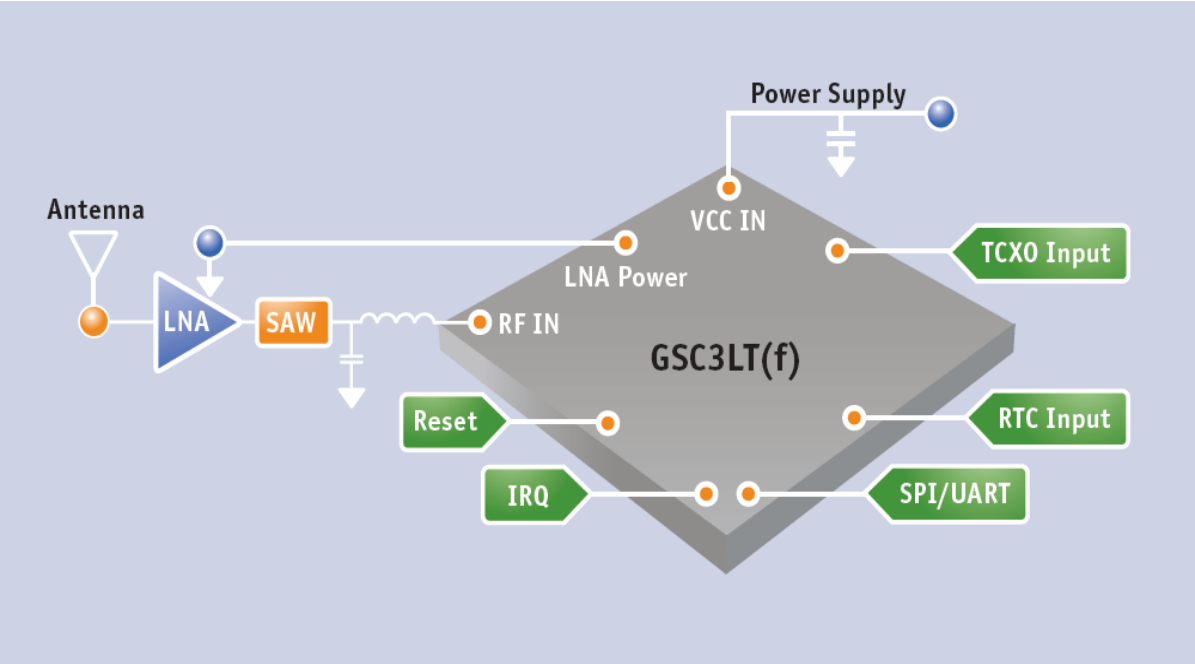


Figure 2-1: ORG13XX architecture

- **Microstrip Patch Antenna**
  OriginGPS microstrip patch antenna collects signals at 1575.42 MHz from the medium and blocks out of GPS L1 band frequencies.
- **LNA (Low Noise Amplifier)**
  The LNA amplifies the GPS signal to meet GSC3LTF RF front-end signal chain input threshold. Noise figure optimized design was implemented to provide maximum sensitivity.
- **Band-pass SAW Filter**
  Band-pass SAW filter eliminates inter-modulated out-of-band signals that may corrupt receiver performance.
- **TCXO (Temperature Compensated Crystal Oscillator)**
  This highly stable 16.369 MHz oscillator controls the down conversion process in RF block. Highest characteristics of this component are key factors in fast TTFF.
- **UART Buffers**
  UART interface is 1.8V/2.5V/3.3V compatible. Voltage level is defined externally by host.

- **GSC3LTf IC**

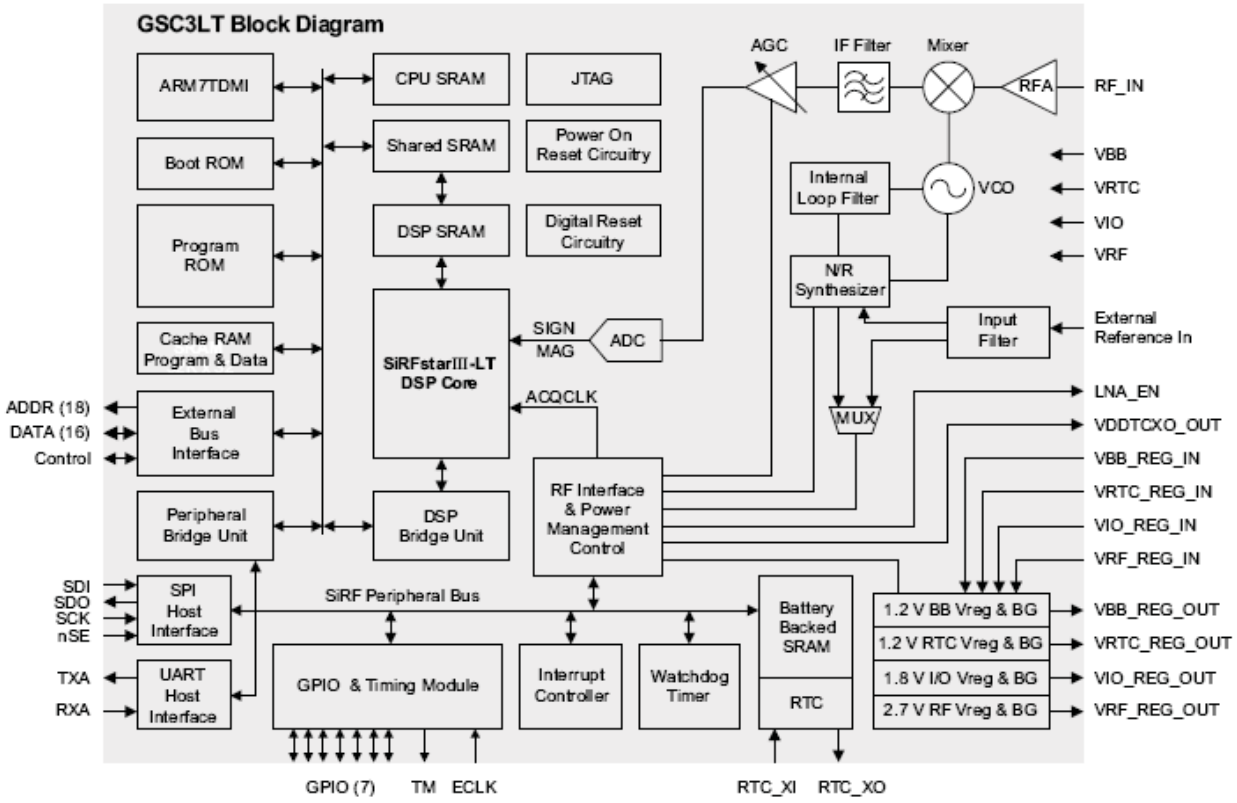


Figure 2-2: GSC3LT functional block diagram

SiRFstarIII GSC3LTf GPS Navigation Engine includes the following features:

- RF Receiver
- ARM7TDMI-S core
- 4 Mbit Program Flash memory
- SiRFstarIII-LT GPS DSP core
- ARM RAM with cache
- DSP RAM
- Interrupt Controller
- RTC Block
- Watchdog Timer
- Battery Backed RAM
- UART Block
- SPI Block
- 4 Integrated Voltage Regulators
- POR (Power-On-Reset) Circuitry

2.3. Applications

The ORG13XX series were specially designed to meet wide range of OEM configurations and applications.

ORG1300

The ORG1300 is low profile GPS Antenna Module.

The ORG1300 is ideal for portable electronics applications with height limitations:

- Handheld consumer navigation and multifunction devices
- Precise timing devices
- Micro robots and micro UAVs
- People and animal tracking systems

ORG1315

The ORG1315 is standard version of the ORG13XX series GPS antenna modules.

The ORG1315 is ideal for standard positioning and navigation applications including indoor tracking:

- People and animal tracking systems
- Sports and recreation accessories
- Vehicle tracking and fleet management systems
- Automotive navigation systems
- Rescue and emergency systems
- Marine navigation systems

ORG1318

The ORG1318 is enhanced sensitivity version of the ORG1300 GPS Antenna Module.

The ORG1318 is ideal for applications where module installation position and orientation limits satellite visibility:

- Automotive security systems
- Asset tracking SKU systems
- Telemetric systems
- Industrial navigation systems

3. Electrical Specifications

3.1. Absolute Maximum Ratings

Absolute Maximum Ratings are stress ratings only.

Stresses exceeding Absolute Maximum Ratings may damage the device.

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{CC}	0	5.5	V
UART Input Voltage	V_{RX}	-0.5	7	V
UART Output Source/Sink Current	I_{TX}	-10	+10	mA
SPI/GPIO Input Voltage	V_{IO_IN}	0	1.98	V
SPI/GPIO Output Source/Sink Current	I_{IO_OUT}	-2	+2	mA
ON_OFF Input Voltage	V_{ON_OFF}		3.78	V
RESET Input Voltage	V_{RESET}		1.26	V
1.8V Source Output Current	I_{IO_1V8}		6	mA
Storage Temperature	T_{ST}	-55	+125	^{0}C
Lead Temperature (10 sec. @ 1mm from case)	T_{LEAD}		+260	^{0}C

Table 3-1: Absolute maximum ratings

3.2. Recommended Operating Conditions

Functional operation above the Recommended Operating Conditions is not implied.

Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Parameter	Symbol	Mode / Pad	Test Conditions	Min	Typ	Max	Units
Power supply voltage	V_{CC}			3.25	3.3	5.5	V
Power Supply Current	I_{CC}	Acquisition	V_{CC} = 3.3V T_{AMB} = 25^{0}C		30	35	mA
		Tracking		9		23	mA
		Hibernate			24	25	µA
1.8 Output Voltage	V_{IO_1V8}	V_{IO-1V8}		1.62	1.8	1.98	V
Input Voltage Low State	V_{IL}	UART				0.5	V
		SPI / GPIO				0.45	V
		ON_OFF				0.6	V
Input Voltage High State	V_{IH}	UART		1.4			V
		SPI / GPIO		1.35			V
		ON_OFF		2.7			V
Output Voltage Low State	V_{OL}	UART	I_{OL} = 8mA			0.36	V
		SPI / GPIO	I_{OL} = 1mA			0.2	V
Output Voltage High State	V_{OH}	UART	I_{OH} = -50µA	V_{IO} – 0.1			V
			I_{OH} = -4mA	V_{IO} – 0.5			V
		SPI / GPIO	I_{OH} = -1mA	1.6			V
Input Capacitance	C_{IN}	UART			4	10	pF
		SPI / GPIO			1.3		pF
Operating Temperature[1]	T_{AMB}			-40	+25	+85	^{0}C
Relative Humidity	RH		Oper. Temp.	5		95	%

Table 3-2: Operating conditions

Note:
1. Operation below -20^{0}C to -40^{0}C and above +70^{0}C to +85^{0}C is accepted, but TTFF may increase

4. Performance

4.1. Acquisition times

TTFF (Time To First Fix) – is the period of time from GPS power-up till position estimation.

Hot Start

A hot start results from software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation.
In this state, all of the critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in SRAM.

Warm Start

A warm start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in memory. In this state, position and time data are present and valid, but ephemeris data validity has expired.

Cold Start

A cold start acquisition results when either position or time data is unknown.
Almanac information is used to identify previously healthy satellites.

Aided Start

Aiding is a method of effectively reducing the TTFF by making every start Hot or Warm.

	TTFF	Signal Level
Hot Start	< 1s	-130 dBm (Outdoor)
Warm Start	< 32s	-130 dBm (Outdoor)
Cold Start	< 35s	-130 dBm (Outdoor)
Signal Reacquisition	< 1s	-130 dBm (Outdoor)

Table 4-1: Acquisition times

4.2. Sensitivity

	Signal Level
Acquisition	-157 dBm (Deep Indoor)
Tracking	-159 dBm (Deep Indoor)
Cold Start	-142 dBm

Table 4-2: Sensitivity

4.3. Received Signal Strength

	ORG1300	ORG1315	ORG1318
Average C/N_0[1]	40 dB-Hz	45 dB-Hz	48 dB-Hz

Table 4-3: Received signal strength

Note:
1. Averaging of 5 SV's with highest C/N0 @ -130dBm, HDOP <1.5

4.4. Power Consumption

Operation Mode	Power
Acquisition	100mW
Tracking	30-75mW
Hibernate	80µW

Table 4-4: Power consumption

4.5. Accuracy

		Method	Accuracy	Units	Test Conditions
Position	Horizontal	CEP (50%)	< 2.5	m	-130 dBm (Outdoor), Static
			< 2	m	-130 dBm (Outdoor), SBAS, Static
		2dRMS (95%)	< 5	m	-130 dBm (Outdoor), Static
			< 4	m	-130 dBm (Outdoor), SBAS, Static
	Vertical	VEP (50%)	< 4	m	-130 dBm (Outdoor), Static
			< 3	m	-130 dBm (Outdoor), SBAS, Static
		2dRMS (95%)	<7.5	m	-130 dBm (Outdoor), Static
			< 6	m	-130 dBm (Outdoor), SBAS, Static
Velocity	Horizontal	50%	< 0.01	m/s	-130 dBm (Outdoor), 30 m/s
Heading		50%	< 0.01	0	-130 dBm (Outdoor), 30 m/s
Time		1 PPS	< 1	µs	-130 dBm (Outdoor)

Table 4-5: Accuracy

4.6. Dynamic Constrains[1]

Velocity	< 515m/s
Acceleration	< 4g
Altitude	< 18,000m

Table 4-6: Dynamic constrains

Note:
1. Standard dynamic constrains according to regulatory limitations

5. Power Management

The ORG13XX series modules have three main operating modes which are controlled by internal state-machine.
These modes provide different levels of power and performance.

5.1. Normal Mode

In Normal Mode the ORG13XX series are fully powered and will automatically acquire and track GPS satellites.

5.2. Power Saving Modes

Adaptive Trickle Power™

Adaptive Trickle Power (ATP) is best suited for applications that require navigation solutions at a fixed rate as well as low power consumption and an ability to track weak signals.
In ATP mode the ORG13XX series module is intelligently cycled between three states to optimize low power operation:

Full Power State

This is the initial state of the ORG13XX series module.
The module stays in full power until a position solution is made and estimated to be reliable.
During the acquisition mode, processing is more intense, thus consuming more power.

CPU Only State

This is the state when the RF and DSP sections are partially powered off.
The state is entered when the satellites measurements have been acquired but the navigation solution still needs to be computed.

Standby State

This is the state when the RF and DSP sections are completely powered off and baseband clock is stopped.

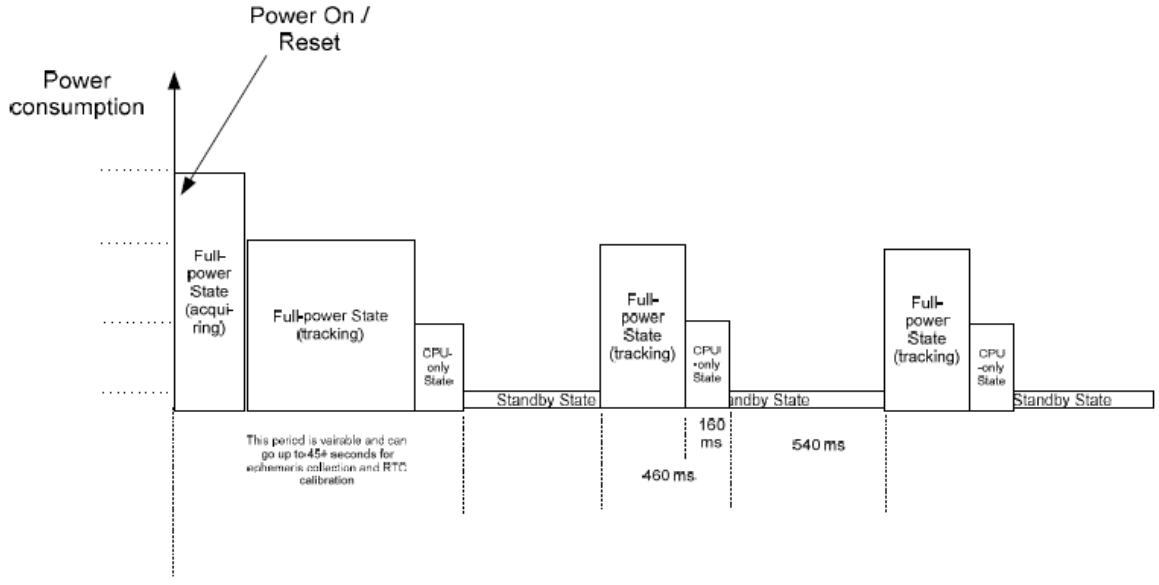


Figure 5-1: ATP timing

Push-to-Fix™

Push-to-Fix (PTF) is best suited for applications that require infrequent navigation solutions, optimizing battery life time.

In PTF mode the ORG13XX series module is mostly in Hibernate Mode, waked up for Ephemeris and Almanac refresh in fixed periods of time. The PTF period is 30 minutes by default but can be anywhere between 10 seconds and 2 hours. When the PTF mode is enabled the receiver well stay on full power until the good navigation solution is computed.

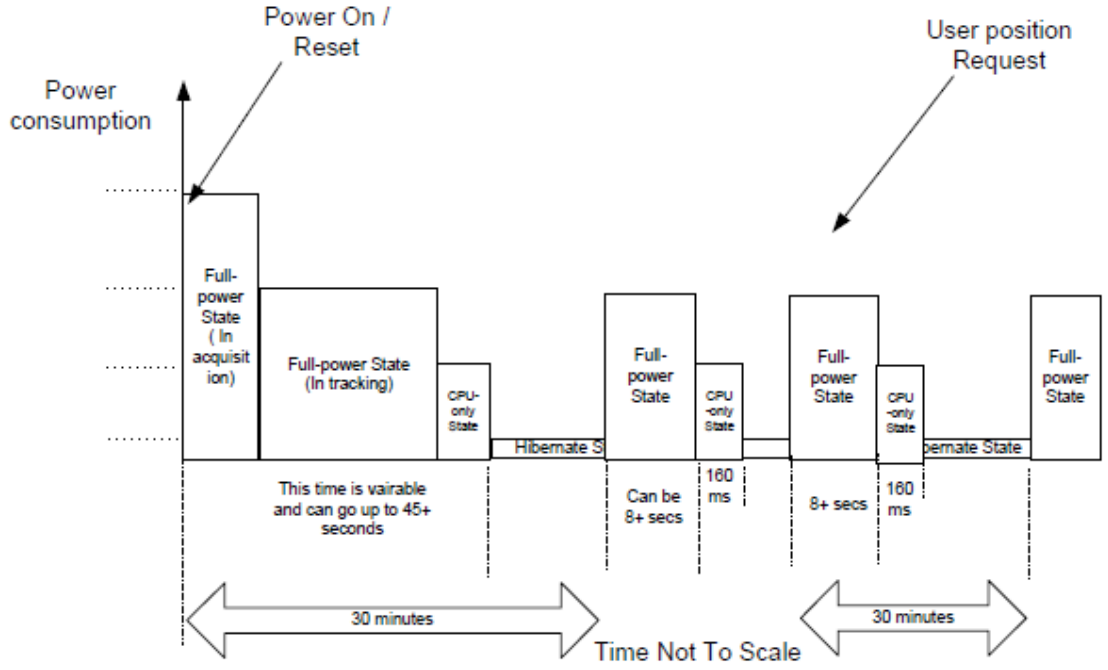


Figure 5-2: PTF timing

Hibernate State

In this state the RF, DSP and baseband sections are completely powered off leaving only the RTC and Battery-backed RAM running. When the application needs a position report it can toggle the ON_OFF pad to wake up the module. In this case, a new PTF cycle with default settings begins.

6. Interface

6.1. Pad Assignment

Pad Number	Pad Name	Pad Description	Direction	Default	Notes
1	RX	UART Receive	Input	High	1.8V/2.5V/3.3V compatible
2	TX	UART Transmit	Output	Low	1.8V/2.5V/3.3V compatible
3	V_{IO-EXT}	UART buffers power	Power		Connect to V_{CC} if powered 3.3V
4	SCK	SPI Clock	Input	Low	1.8V compatible
5	nSE	SPI Chip Select	Input	High	1.8V compatible
6	SDO	SPI Data Out	Output		1.8V compatible
7	$GPIO_{[1]}$	Valid Fix Indicator	Output	High	1.8V compatible
8	V_{CC}	System Power	Power		
9	V_{IO-1V8}	1.8V Voltage Output	Power		Connect to V_{IO-EXT} for 1.8V UART
10	GND	System Ground	Power		
11	GND	System Ground	Power		
12	GND	System Ground	Power		
13	GND	System Ground	Power		
14	GND	System Ground	Power		
15	TSYNC	Time Aiding	Input		SiRFLoc® Client (SLC) firmware required
16	nRESET	Asynchronous Reset	Input	High	
17	ON_OFF	Soft Power On/Hibernate	Input	Low	3.3V compatible
18	$GPIO_{[2]}$	Valid Fix Indicator	Output	Low	1.8V compatible
19	ECLK	External Clock Input	Input		SiRFLoc® Client (SLC) firmware required
20	COMM_SEL	UART/SPI Select	Input	High	
21	1PPS	1 Pulse Per Second	Output	Low	1.8V compatible
22	SDI	SPI Data In	Input	Low	1.8V compatible

Table 6-1: ORG13XX series pin-out

6.2. Connectivity

Power supply

The ORG13XX series module requires only one power supply V_{CC}, which can be supplied directly from a battery since the module has internal regulators.
It is recommended to keep the power supply on all the time in order to maintain the non-volatile RTC and RAM active for fastest possible TTFF. When the V_{CC} is powered off settings are reset to factory default and the receiver performs Cold Start on next power up.
Power supply current varies according to the processor load and satellite acquisition.
V_{CC} range is 3.3 to 5.5V DC.
Typical I_{CC} current is 30mA during acquisition. Peak I_{CC} current is 50 mA.
Typical I_{CC} current in Hibernate state is 25µA.
Voltage ripple below 300mV_{PP} allowed for frequency under 10KHz.
Voltage ripple below 30mV_{PP} allowed for frequency between 10KHz and 100KHz.
Voltage ripple below 10mV_{PP} allowed for frequency between 100KHz and 1MHz.
Voltage ripple below 3mV_{PP} allowed for frequency above 1MHz.
High voltage ripple may compromise the ORG13XX series module performance.
In case of powering the ORG13XX from switching mode (DC-DC) power source carefully follow manufacturer's application note and apply passive low pass filtering.

Ground

One Ground pad should be connected to the main Ground with shortest possible trace or via.

ON OFF Control Input

The ON_OFF control input can be used to switch the receiver between Normal or Hibernate modes and also to generate interrupt in Push-to-Fix operation.
The ON_OFF interrupt is generated by a low-high-low toggle, which should be longer than 62µs and less than 1s (100ms pulse length recommended).
ON_OFF interrupts with less than 1 sec intervals are not recommended. Multiple switch bounce pulses are recommended to be filtered out.
Input level is 3.3V compatible.

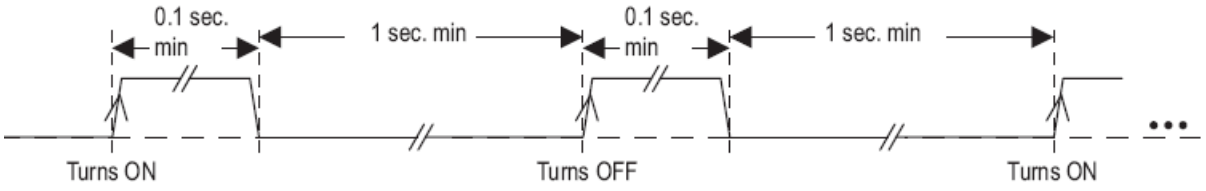


Figure 6-1: ON_OFF timing

nRESET Input

The Power-on-Reset (POR) is generated internally in the ORG13XX series module.
Additionally, manual reset option is available through nRESET pad.
Resetting the ORG13XX clears the RTC block and configuration settings become default.
nRESET pad is active low and has internal pull-up resistor.
nRESET signal should be applied for at least 1µs.

COMM_SEL

The ORG13XX is able to communicate via UART or SPI interface.
UART is default communication interface.
To select SPI communication 0Ω resistor to system Ground should be applied on this pad.
Do not connect if SPI communication is not used.

UART

The device supports full duplex 8-N-1 UART communication without flow control.
The default protocol is NMEA.
The default configuration for baud rates and respective protocols can be changed by commands via NMEA or SiRF binary protocols.
I/O levels in the serial port are LVCMOS 1.8V/2.5V/3.3V compatible.
I/O levels are defined by applying appropriate voltage to V_{IO-EXT} pad.
Do not connect if UART communication is not used.

SPI

The Host Interface SPI is a slave mode SPI that can be used as an alternative to the UART interface. The four primary pads are SDI, SDO, nSE, SCK.
I/O levels are 1.8V compatible.
Do not connect if SPI communication is not used.
SCK clock frequency must not be higher than 48fo/7 (= 7 MHz approximately).

The primary Host Interface SPI features are:

- TX and RX each have independent 1024 byte FIFO buffers.
- RX and TX have independent, software specified two byte idle patterns.
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled.
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken.
- FIFO buffers can generate an interrupt at any fill level.
- SPI detects synchronization errors and can be reset by software.

The HSPI performs bit-by-bit transmitting and receiving at the same time whenever nSE is asserted and SCK is active.
Receive operations do not require an enable.
When the system is first turned on, the master in the host system is able to send a message before software has set up the receiver's idle pattern filter. At the system level, protocols are established to specify how the host platform must verify that the GPS system and host SPI are prepared for operation.
In general, the GSC3LTF loads a ‘power on’ message to the TX_FIFO to inform the host that operations can begin. The protocol specifies the delay and repeats intervals for host query of the slave SPI for this message. This limits the receive byte volume until idle pattern filters are established.
On the receive side, the host is expected to transmit idle pattern when it is querying the transmit buffer, unless it has traffic for the GSC3LTf. In this way, the volume is discarded, bytes are kept nearly as low as in the UART application because the hardware does not place most idle pattern bytes in the RX FIFO. Most messaging can be serviced with polling.

The FIFO threshold can be placed to detect large messages requiring interrupt driven servicing. On the transmit side, the intent is to fill the FIFO only when it is disabled and empty. In this condition, the driver software loads as many queued up messages as can fit in the FIFO. Then the FIFO is enabled. The host is required to poll messages until idle pattern bytes are detected. At this point the FIFO is empty and disabled, allowing the driver to once again respond to an empty FIFO interrupt and load the FIFO with messages, if any are queued up in buffers.

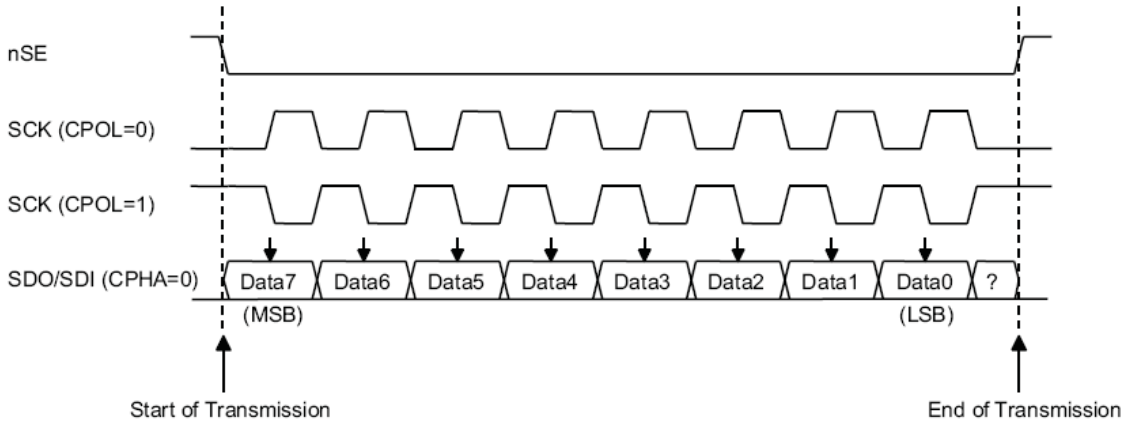


Figure 6-2: SPI timing

ECLK Input

The ECLK is available optionally for external clock input with SiRFLoc® Client (SLC) firmware used for A-GPS frequency aiding.
Input level is CMOS 1.8V compatible.
Pull low with 10kΩ when not used.
Do not connect when using standard firmware.

TSYNC Input

Optional input TSYNC input is intended for external time aiding with SiRFLoc® Client (SLC) firmware used for A-GPS.
Input level is CMOS 1.8V compatible.
Pull low with 10kΩ when not used.
Do not connect when using standard firmware.

1PPS Output

The pulse-per-second (PPS) output provides a pulse signal for timing purposes.
Pulse length (high state) is about 1µs synchronized to full UTC second.
Output level is CMOS 1.8V compatible.

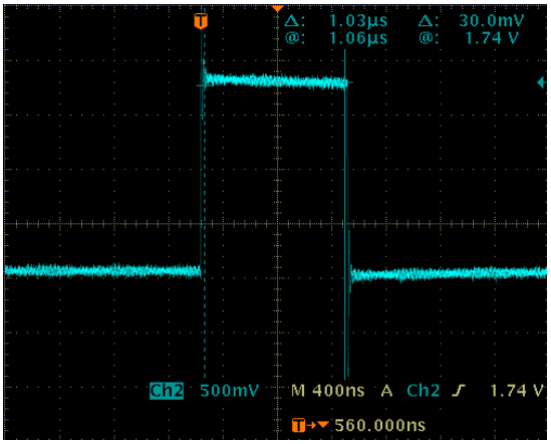


Figure 6-3: 1PPS

GPIO1 Output

GPIO1 is available as a Valid Fix indicator. Prior navigation the output stays at high state.
During valid fix the output sends 100ms high state pulses at 1Hz rate.
The output level is CMOS 1.8V compatible.

GPIO2 Output

GPIO2 is available as a Valid Fix indicator. Prior navigation the output stays at low state.
During valid fix the output sends 100ms high state pulses at 1Hz rate.
The output level is CMOS 1.8V compatible.

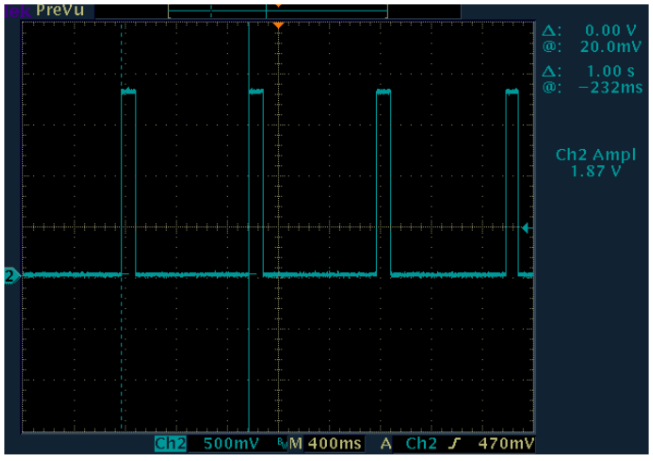


Figure 6-4: GPIO2 output period

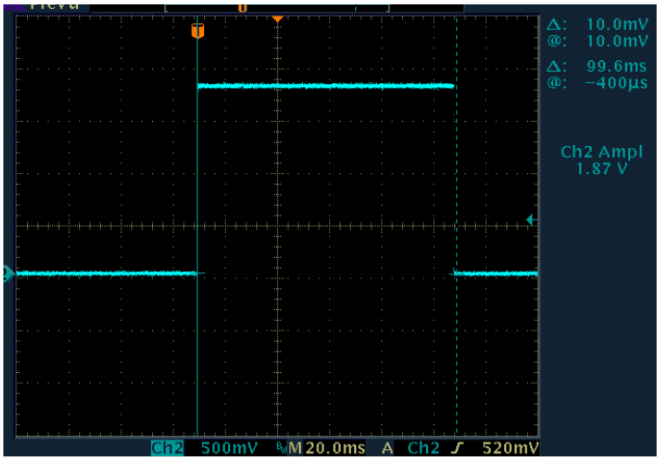


Figure 6-5: GPIO2 output

6.3. Typical Application Circuit

UART Interface

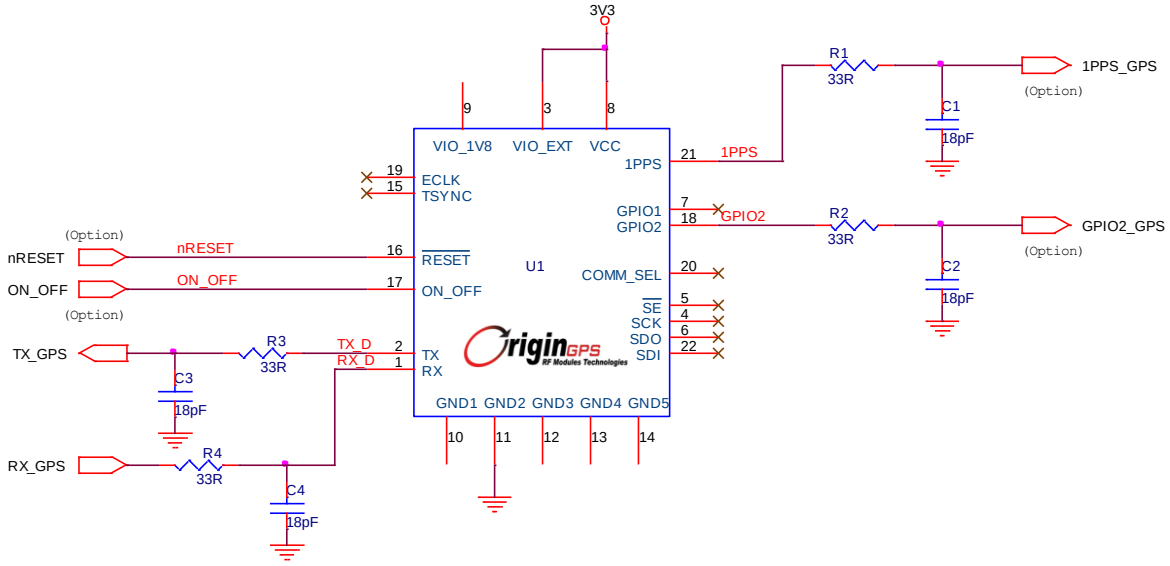


Figure 6-6: UART interface circuit

SPI Interface

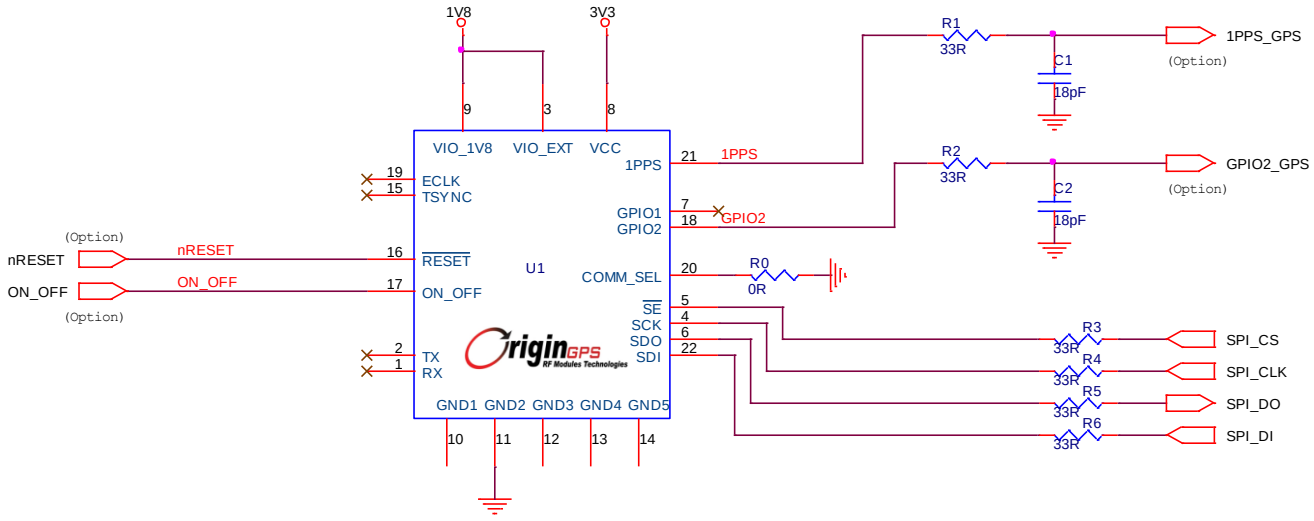


Figure 6-7: SPI interface circuit

7. PCB Layout

7.1. Footprint

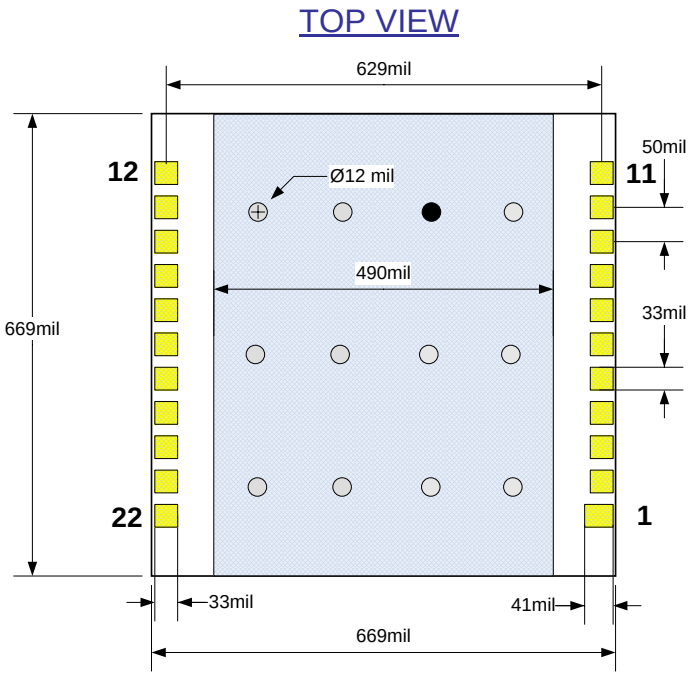


Figure 7-1: Footprint

Ground pad at the middle should be connected to main Ground plane by multiple vias.
Ground pad at the middle should be solder masked.
Silk print of module's outline is highly recommended.

7.2. Design restrictions

Avoid current loops by connecting single Ground pad to main Ground.

Route the selected Ground pad to main Ground with shortest possible trace or via.

Avoid copper pour on the module side, keeping out the module minimum 6mm from the copper planes, metals planes or enclosures, connectors or LCD screens (Fig. 7-2).

Keep out of minimum 1.6mm from the copper planes under the ORG13XX GPS module (Fig. 7-3).

Keep out of signal or switching power traces and vias under the ORG13XX GPS module.

Signal traces to/from ORG13XX GPS module should have minimum length.

In case of adjacent high speed components, like CPU or memory, high frequency components, like transmitters, clock resonators or oscillators, metal planes, like LCD or battery enclosures, please contact OriginGPS for more precise, application specific recommendations.

7.3. Placement

Special attention should be paid during GPS module placement and position on host PCB.

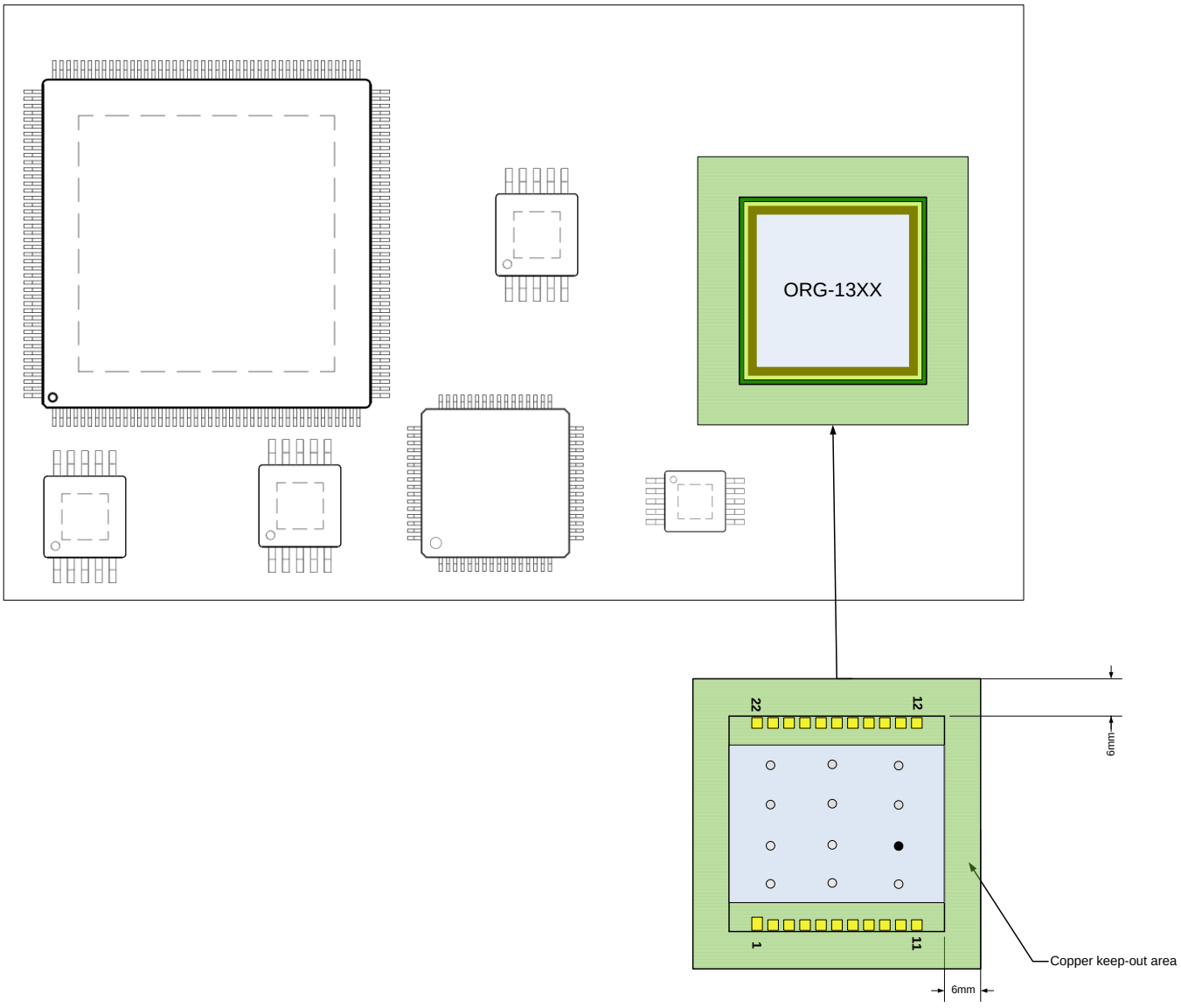


Figure 7-2: Placement

For board specific module position, follow the link: http://origingps.com/images/copper.xls
or contact OriginGPS.

7.4. PCB stack up

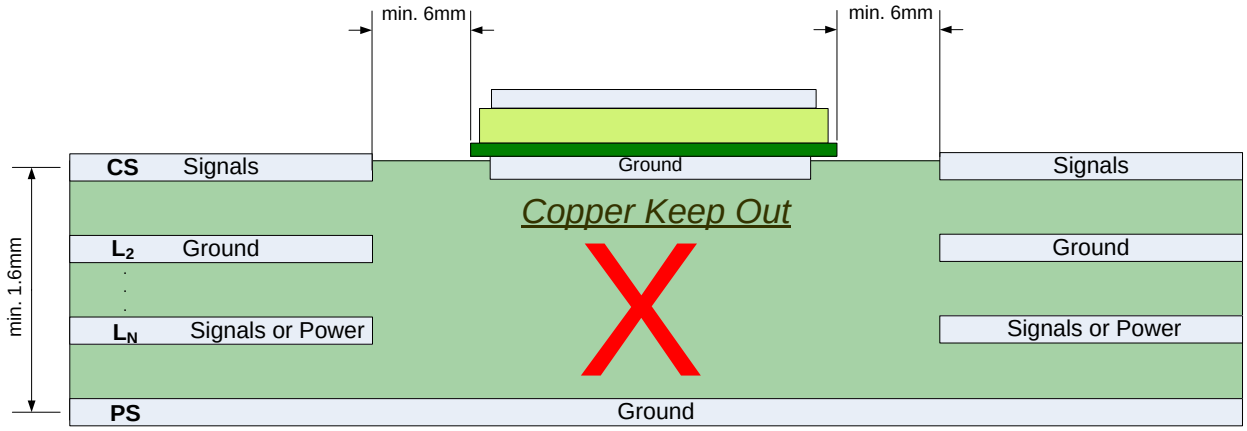


Figure 7-3: Typical PCB stack up

8. Software Functions

The ORG13XX series modules support NMEA-0183 and SiRF Binary protocols.

8.1. NMEA

NMEA Output Messages

Message	Description
GGA	Time, position and fix type data
GLL[1]	Latitude, longitude, UTC time of position fix and status
GSA	GPS receiver operating mode, satellites used in the position solution and DOP values
GSV	The number of GPS satellites in view, satellite ID, elevation, azimuth and SNR values
RMC	Time, date, position, course and speed data
VTG[1]	Course and speed information relative to the ground

Table 8-1: NMEA protocol output messages

NMEA Input Messages

Message ID	Message	Description
100	Set Serial Port	Set UART parameters and protocol
101	Navigation Initialization	Parameters required for start using X/Y/Z
103	Query/Rate Control	Query standard NMEA message and/or set output rate
104	LLA Navigation Initialization	Parameters required for start using Lat/Lon/Alt
105	Development Data On/Off	Development Data messages On/Off
106	Select Datum	Selection of an alternative map datum

Table 8-2: NMEA protocol input messages

1. Not available in standard firmware build

8.2. SiRF Binary

SiRF Binary Output Messages

HEX	Message ID	Name	Description
0 x 02	2	Measured Navigation Data	Position, velocity and time
0 x 03	3	True Tracker Data	Not implemented
0 x 04	4	Measured Tracking Data	Satellite and C/No information
0 x 06	6	SW Version	Receiver software
0 x 07	7	Clock Status	Current clock status
0 x 08	8	50 BPS Subframe Data	Standard ICD format
0 x 09	9	Throughput	Navigation complete data
0 x 0A	10	Error ID	Error coding for message failure
0 x 0B	11	Command Acknowledgement	Successful request
0 x 0C	12	Command No Acknowledgement	Unsuccessful request
0 x 0D	13	Visible List	Auto Output
0 x 0E	14	Almanac Data	Response to Poll
0 x 0F	15	Ephemeris Data	Response to Poll
0 x 10	16	Test Mode 1	For use with SiRFtest (Test Mode 1)
0 x 12	18	Ok To Send	CPU ON/OFF (Trickle Power)
0 x 13	19	Navigation Parameters	Response to Poll
0 x 14	20	Test Mode 2	Additional test data (Test Mode 2)
0 x 1C	28	Nav. Lib. Measurement Data	Measurement Data
0 x 1E	30	Nav. Lib. SV State Data	Satellite State Data
0 x 1F	31	Nav. Lib. Initialization Data	Initialization Data
0 x FF	255	Development Data	Various status messages

Table 8-3: SiRF Binary protocol output messages

SiRF Binary Input Messages

HEX	Message ID	Name	Description
0 x 55	85	Transmit Serial Message	User definable message
0 x 80	128	Initialize Data Source	Receiver initialization and associated parameters
0 x 81	129	Switch to NMEA Protocol	Enable NMEA message, output rate and baud rate
0 x 82	130	Set Almanac (upload)	Sends an existing almanac file to the receiver
0 x 84	132	Software Version (Poll)	Polls for the loaded software version
0 x 86	134	Set Main Serial Port	Baud rate, data bits, stop bits and parity
0 x 87	135	Switch Protocol	Obsolete
0 x 88	136	Mode Control	Navigation mode configuration
0 x 89	137	DOP Mask	Control DOP mask selection and parameters
0 x 8B	139	Elevation Mask	Elevation tracking and navigation masks
0 x 8C	140	Power Mask	Power tracking and navigation masks
0 x 8D	141	Editing Residual	Not implemented
0 x 8E	142	Steady-State Detection	Configuration for static operation
0 x 8F	143	Static Navigation	For use with SiRFtest (Test Mode 1)
0 x 90	144	Poll Clock Status	Polls the clock status
0 x 92	146	Poll Almanac	Polls for almanac data
0 x 93	147	Poll Ephemeris	Polls for ephemeris data
0 x 94	148	Flash Update	On the fly software update
0 x 95	149	Set Ephemeris (upload)	Sends an existing ephemeris to the receiver
0 x 96	150	Switch Operating Mode	Test mode selection, SV ID and period
0 x 97	151	Set Trickle Power Parameters	Push to fix mode, duty cycle and on time
0 x 98	152	Poll Navigation Parameters	Polls for the current navigation parameters
0 x A5	165	Set UART Configuration	Protocol selection, baud rate, data, stop and parity bits
0 x A6	166	Set Message Rate	SiRF binary message output rate
0 x A7	167	Low Power Acquisition Parameters	Low power configuration parameters

Table 8-4: SiRF Binary protocol input messages

9. Handling Information

9.1. Product Packaging and Delivery

Plastic Reel

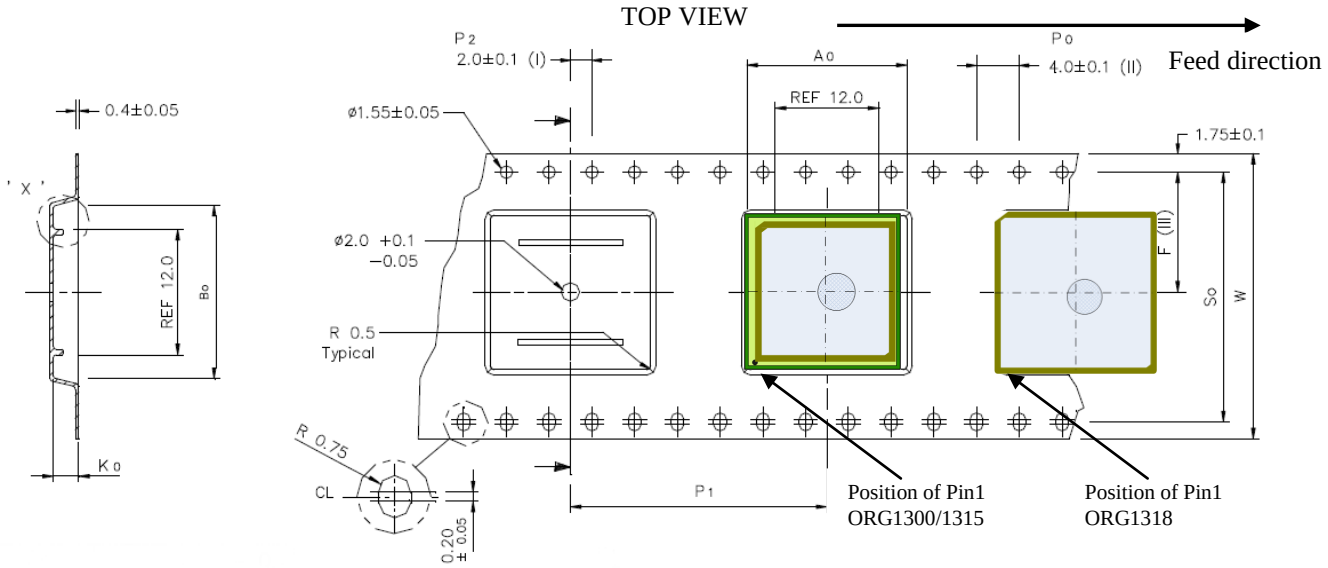


Figure 9-1: Carrier

	ORG1300/1315	ORG1318
A_0	18.00 ± 0.1	20.50 ± 0.1
B_0	18.00 ± 0.1	20.50 ± 0.1
K_0	05.70 ± 0.1	05.30 ± 0.1
F	14.20 ± 0.1	14.20 ± 0.1
P_1	24.00 ± 0.1	24.00 ± 0.1
S_0	28.40 ± 0.1	28.40 ± 0.1
W	32.00 ± 0.3	32.00 ± 0.3

Table 9-1: Carrier dimensions [mm]

Carrier material: Conductive Polystyrene

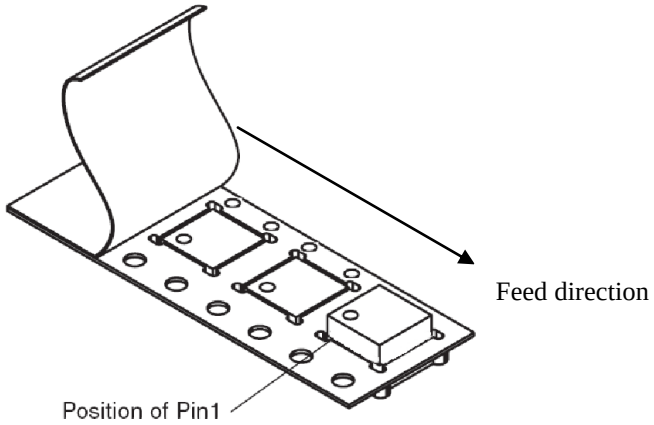


Figure 9-2: Module position

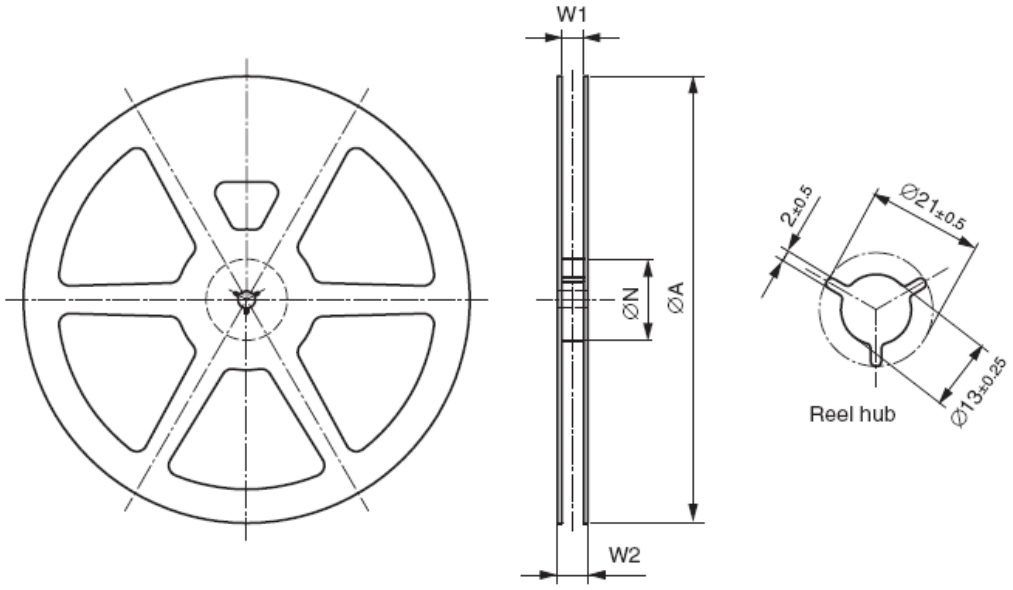


Figure 8-3: Reel

ØA	330.00 ± 0.85
ØN	60.00 ± 0.5
W_1	33.00 ± 0.5
W_2	39.00 ± 0.5

Table 9-2: Reel dimensions [mm]

Reel material: Antistatic Plastic

Each reel contains 200 or 500 modules.

Tube[1]

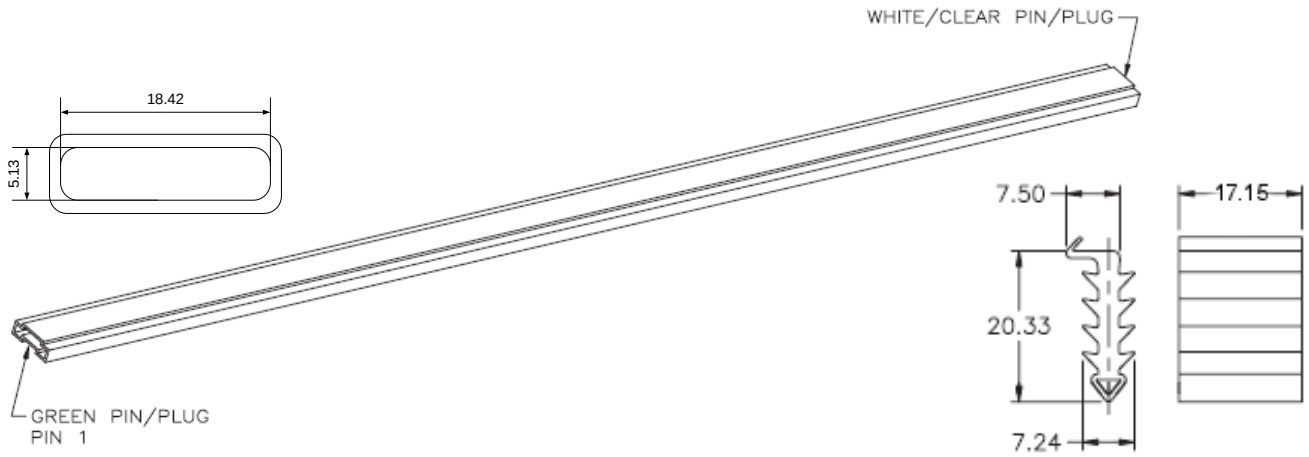


Figure 9-4: Tube

Tube length: 515mm

Tube material: Antistatic Plastic

Each tube contains up to 27 modules.

1.Not available for ORG1318

9.2. Moisture Sensitivity

The devices are moisture sensitive at MSL 3 according to standard IPC/JEDEC J-STD-033B.
The recommended drying process for samples and bulk components is to be done at 125°C for 48 hours.

9.3. Assembly

The ORG13XX series module support automatic assembly and reflow soldering processes on the component side of the motherboard PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD. Suggested solder paste stencil is 5 mil to ensure sufficient solder volume.

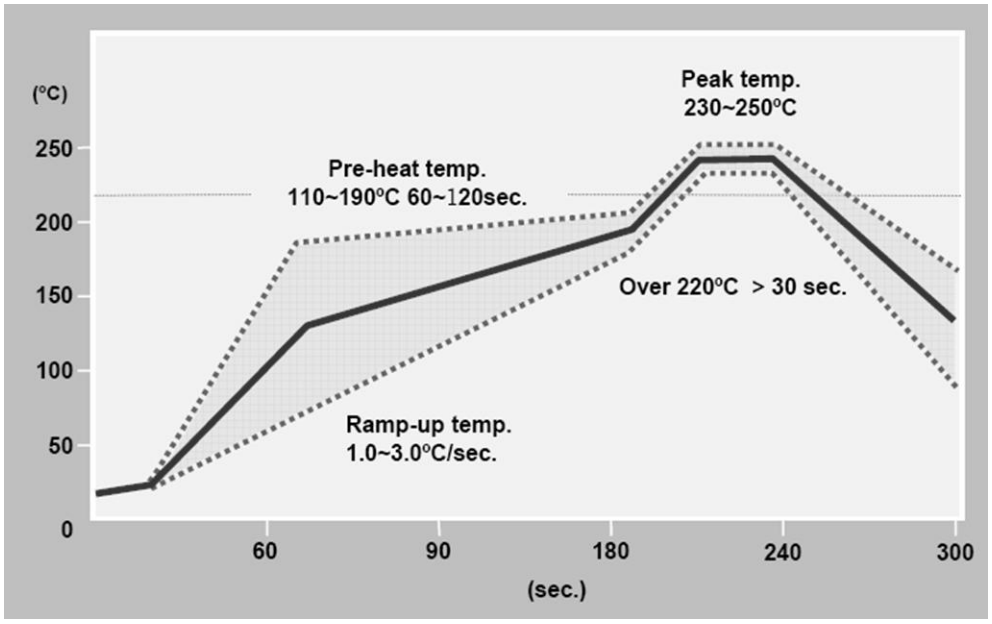


Figure 9-5: Recommended soldering profile

Suggested peak reflow temperature is 250°C for 10 sec. for Pb-Free solder paste.
Absolute Maximum reflow temperature is 260°C for 10 sec.

9.4. Rework

If localized heating is required to rework or repair the ORG13XX series module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

9.5. ESD Sensitivity

The ORG13XX series modules are ESD sensitive devices and should be handled with care.

9.6. Compliances

The ORG13XX series modules comply with the following standards:

- Pb-Free/RoHS (Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment)
- ISO 9001:2000 accredited manufacturing facility

9.7. Safety Information

Improper handling and use can cause permanent damage to the device.
There is also the possible risk of personal injury from mechanical trauma or shocking hazard.

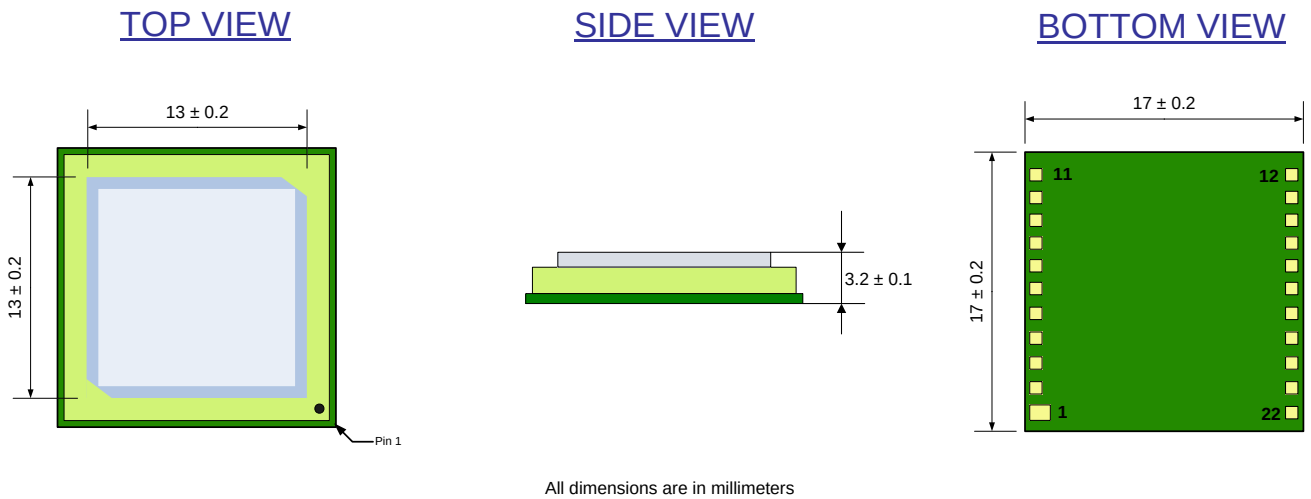
9.8. Disposal Information

The product should not be treated as household waste.
For more detailed information about recycling electronic components, please contact your local waste management authority.

10. Mechanical Specifications

- The ORG13XX series modules have advanced miniature packaging and a LGA footprint.
- The ORG13XX series modules PCB footprint size is 17mm x 17mm
- The ORG13XX series modules are surface mount devices packaged on a miniature printed circuit board with a metallic RF enclosure on one side and Microstrip Patch Antenna on top of the shield.
- There are 22 surface mount connection pads with a base metal of copper and an Electroless Nickel / Immersion Gold (ENIG) finish.
- The ORG13XX series modules have been designed for automated pick and place assembly and reflow soldering processes.

10.1. ORG1300



All dimensions are in millimeters

Figure 10-1: ORG1300 mechanical drawing

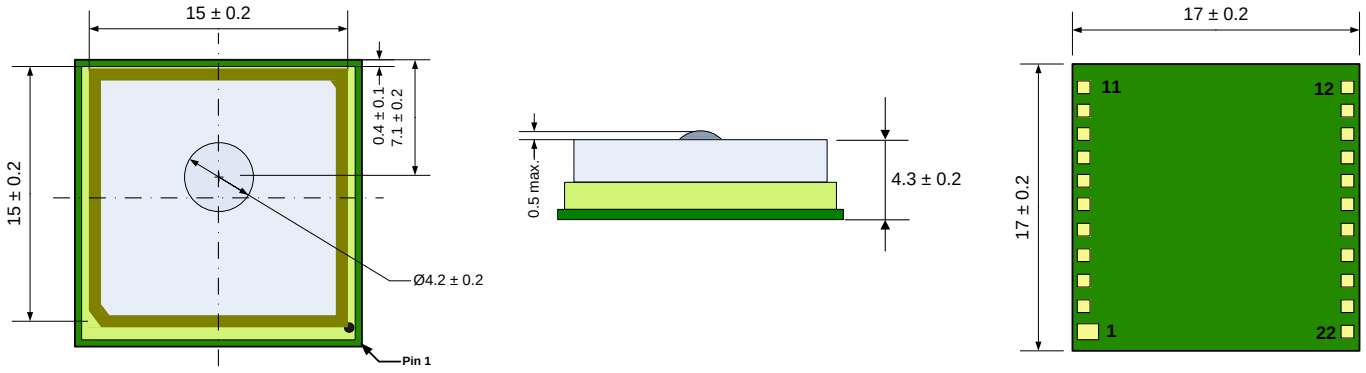
Dimensions	Length	Width	Height
mm	17 ± 0.2	17 ± 0.2	3.2 ± 0.1
inch	0.67 ± 0.008	0.67 ± 0.008	0.125 ± 0.004

Weight	
gr	2.2
oz	0.1

Table 10-1: ORG1300 mechanical information

10.2. ORG1315

TOP VIEW SIDE VIEW BOTTOM VIEW



All dimensions are in millimeters

Figure 10-2: ORG1315 mechanical drawing

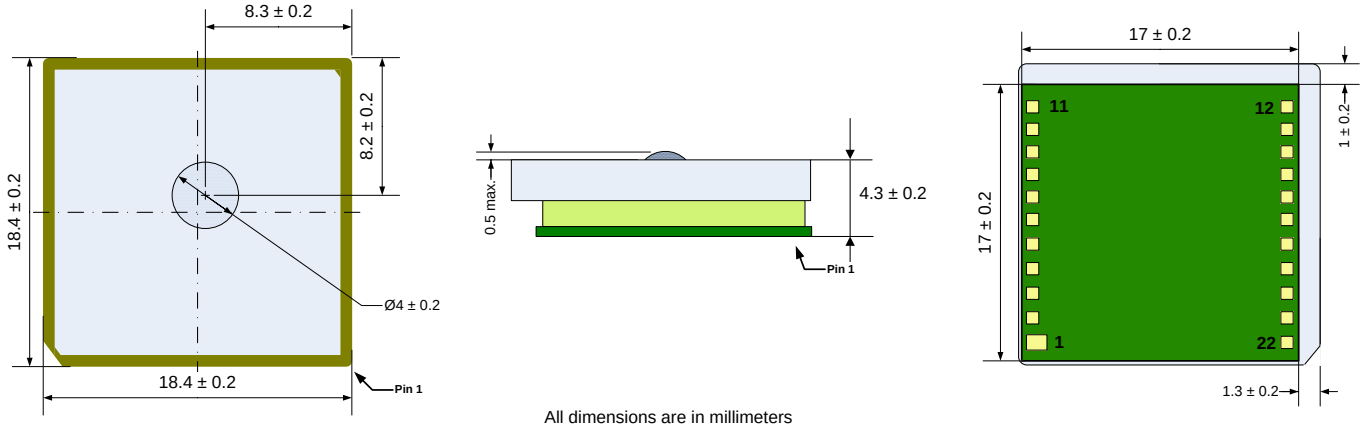
Dimensions	Length	Width	Height
mm	17 ± 0.2	17 ± 0.2	4.8 ± 0.2
inch	0.67 ± 0.008	0.67 ± 0.008	0.189 ± 0.008

Weight	
gr	3.5
oz	0.12

Table 10-2: ORG1315 mechanical information

10.3. ORG1318

TOP VIEW SIDE VIEW BOTTOM VIEW



All dimensions are in millimeters

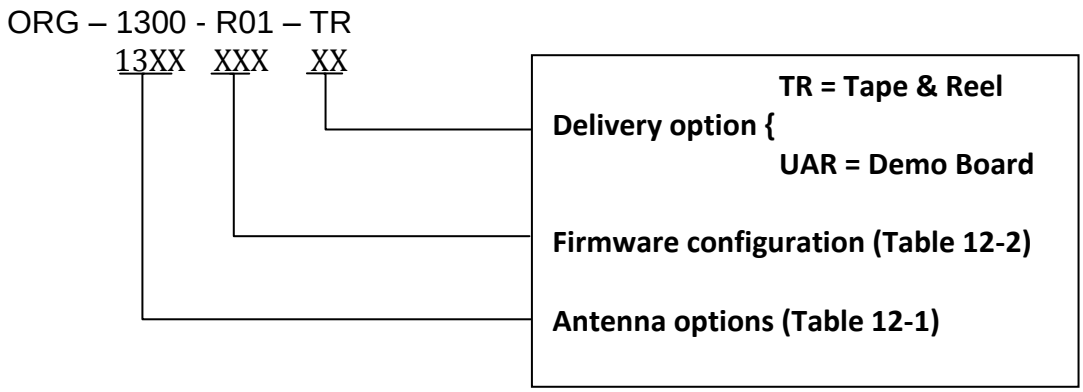
Figure 10-3: ORG1318 mechanical drawing

Dimensions	Length	Width	Height
mm	18.4 ± 0.2	18.4 ± 0.2	4.8 ± 0.2
inch	0.72 ± 0.008	0.72 ± 0.004	0.189 ± 0.008

Weight	
gr	4.75
oz	0.17

Table 10-3: ORG1318 mechanical information

11. Ordering Information



12. Design-In Checklist

Following the Design-In Checklist when developing applications with the ORG13XX series GPS antenna modules is highly recommended to reduce design risks.

12.1. Module selection

ORG13XX series modules have been intentionally designed to allow GPS functionality to be optimally tailored to application specific environment.
Changing between the different modules is easy, due to the same footprint and pin-out.

Does the application demand for ultra low profile GPS antenna module?
Is the GPS module placed in line of sight with GPS satellites?

☑ *Select ORG1300 for ultra-low profile solution.*

Does the application demand for standard positioning and navigation, including indoor tracking?

☑ *Select ORG1315 for high-sensitivity solution.*

Does the application demand for module installation position with limited GPS satellite visibility?

☑ *Select ORG1318 for ultra-sensitivity solution.*

		ORG1300	ORG1315	ORG1318
Ordering code		ORG1300-xxx	ORG1315-xxx	ORG1318-xxx
Average C/N_0[1]		40 dB-Hz	45 dB-Hz	48 dB-Hz
PCB outline[2]		17mm x 17mm	17mm x 17mm	17mm x 17mm
Dimensions (typ.)	Length	17 mm	17 mm	18.4 mm
	Width	17 mm	17 mm	18.4 mm
	Thickness	3.2 mm	4.8 mm	4.8 mm

Table 12- 1: Antenna options

2.Averaging of 5 SV's with highest C/N0 @ -130dBm, HDOP <1.5
3.Footprint and pinout are the same.

12.2. Firmware selection

ORG13XX series modules are delivered with factory loaded firmware.
Firmware selection is done according to application demands for GPS function.

Does the application demand for primary GPS function?

☑ *Select R01 option for fully operated GPS module upon power on.*
ⓘ *Note for NMEA@UART baud rate of 4,800 bps.*

Does the application demand for minimum connectivity to GPS module?

☑ *Select R01 option for data output via GPS TX (pad 2) and power via V_{CC} (pad 8) and GND (pad 11).*
ⓘ *Connect V_{IO_EXT} (pad 3) to V_{CC} (pad 8) for single supply.*
ⓘ *Note for NMEA@UART baud rate of 4,800 bps.*

Does the application demand for infrequent GPS functionality?

☑ *Select R02 option for hibernated GPS module upon power on.*
ⓘ *Connect ON_OFF (pad 17) to host output for power state control.*
ⓘ *Note for NMEA@UART baud rate of 57,600 bps.*

The table below indicates ORG13xx series modules firmware configuration options.
Configuration 1 and 2 are standard ordering options.
Configuration 3 is user defined application specific firmware version.

		Configuration 1	Configuration 2	Configuration 3
Ordering code		ORG13xx-R01	ORG13xx-R02	ORG13xx-Fxx
Power On State		Full Power	Hibernate	Full Power
UART data format		NMEA	NMEA	NMEA
UART settings		4,800 bps 8-N-1	57,600 bps 8-N-1	9,600 bps 8-N-1
SPI data format		NMEA	NMEA	N/A
I/O Functions				
ON OFF	Direction	Input	Input	N/A
	Next Toggle	Hibernate	Full Power	
1 PPS	Direction	Output	Output	Output
	No Nav	OFF	OFF	OFF
	Nav	1µs ON @ 1Hz	1µs ON @ 1Hz	1µs ON @ 1Hz
GPIO1	Direction	Output	Output	Application specific
	No Nav	ON	ON	
	Nav	100ms ON @ 1Hz	100ms ON @ 1Hz	
GPIO2	Direction	Output	Output	Application specific
	No Nav	OFF	OFF	
	Nav	100ms ON @ 1Hz	100ms ON @ 1Hz	
COMM_SEL	Direction	Input	Input	N/A
	UART	No Connect	No Connect	
	SPI	GND	GND	
Extended Features				
Navigation	SBAS	OFF	ON	Application specific
	Static Filter	OFF	ON	Application specific
	Track Smoothing	OFF	OFF	Application specific
	Internal DR	OFF	ON	Application specific

Table 12-2: Firmware configuration

12.3. Schematics verification

Check Power Supply Requirements

Is the main power supply voltage (V_{CC}) within the specified range?

- ☑ *Verify 3.3V to 5.5V. Raw battery voltage source is accepted.*
- ⓘ *The module will shut down when voltage trip below 3.25V.*
- ⓘ *nRESET pad will be internally held in low state.*

Single supply operation required?

- ☑ *Connect V_{IO_EXT} to V_{CC}.*

Is the UART buffers power supply voltage (V_{IO_EXT}) within the specified range?

- ☑ *Verify V_{IO_EXT} from 1.8V to V_{CC}.*

Is the power source ripple not exceeding maximum allowed?

- ⓘ *Voltage ripple below 300mV_{p-p} allowed for frequency under 10KHz.*
- ⓘ *Voltage ripple below 30mV_{p-p} allowed for frequency between 10KHz and 100KHz.*
- ⓘ *Voltage ripple below 10mV_{p-p} allowed for frequency between 100KHz and 1MHz.*
- ⓘ *Voltage ripple below 3mV_{p-p} allowed for frequency above 1MHz.*

Does the power source capable to handle current consumption requirements?

- ⓘ *Maximum current consumption during acquisition is 35mA.*
- ⓘ *Inrush current during module power up may exceed 120mA.*

Is only single GND pad connected to the main Ground?

Check Communication Interface

Is the UART interface used?

- ☑ *Leave COMM_SEL (pad 20) floating.*
- ☑ *Connect series ceramic resistor of 22-49Ω and shunt ceramic capacitor of 12-22pF to form low pass filter on GPS TX (pad 2) and GPS RX (pad 1) lines.*

Is the UART output high logic level voltage V_{CC} tolerant?

- ☑ *Connect V_{IO_EXT} (pad 3) to V_{CC} (pad 8).*
- ⓘ *UART voltage level is externally defined by V_{IO_EXT} pad.*

Is the SPI interface used?

- ☑ *Connect COMM_SEL (pad 20) to GND.*
- ⓘ *SPI is LVCMOS 1.8V compatible.*

Check GPIO

Is the Hot or Warm starts needed?

- ☑ *Connect host output to ON OFF input (pad 3).*
- ⓘ *Main V_{CC} is permanently applied. GPS module is hibernated by ON OFF toggle.*
- ⓘ *ON OFF input is CMOS 3.3V compatible.*

Is Valid Fix indicator required?

- ☑ *Connect GPIO1 (pad 7) or GPIO2 (pad 18) to host input.*
- ⓘ *GPIO1 and GPIO2 are 1.8V compatible.*
- ⓘ *In Normal operating mode, prior to fix, in the GPIO1 is held in high state. In Hibernate mode the GPIO1 logic level is low. GPIO1 output may be used as mode indicator for host.*

- ⃠ *Don't drive nRESET input high.*
- ⃠ *Don't connect Pull-up to ON_OFF input.*
- ⃠ *Don't Pull-up or Pull-down on any of the inputs or outputs if not in use.*
- ⃠ *1PPS, ECLK, TSYNC are LVCMOS 1.8V compatible.*

12.4. Layout verification

Is the GPS antenna module placed according to the recommendations?

☑ *Follow the link for module's pin 1 position: http://origingps.com/images/copper.xls*

Has the copper keep-out on module's layer been followed?

☑ *Keep out the module minimum 6mm from the metals planes.*
ⓘ *Reduce copper planes on module's side as much as possible.*
ⓘ *For more information refer to Fig. 7-2*

Has the copper planes keep-out under the module been followed?

☑ *Keep out of minimum 1.6mm from the copper planes under the module.*
ⓘ *For more information refer to Fig. 7-3*

Is ground paddle under the module connected to main ground plane by multiple vias?
Is ground paddle under the module solder masked?

ⓘ *Ground paddle under the module is important for EMI immunity of the GPS receiver.*
ⓘ *For more information refer to Fig. 7-1*

Does the silk print of module's footprint outline appear on host PCB?

ⓘ *Silk print of the module's footprint outline in important for automatic pick and place assembly process and inspection.*

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