



# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

RF power transistors designed for applications operating at frequencies from 900 to 1215 MHz. These devices are suitable for use in defense and commercial pulse applications, such as IFF and DME.

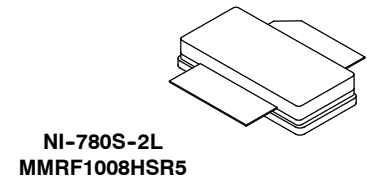
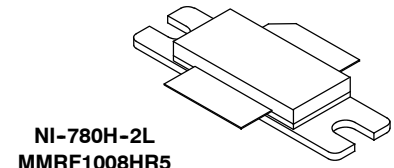
- Typical Pulse Performance:  $V_{DD} = 50$  Vdc,  $I_{DQ} = 100$  mA,  $P_{out} = 275$  W Peak (27.5 Watts Avg.),  $f = 1030$  MHz, Pulse Width = 128  $\mu$ sec, Duty Cycle = 10%  
Power Gain — 20.3 dB  
Drain Efficiency — 65.5%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 1030 MHz, 275 W Peak Power
- Typical Broadband Performance:  $V_{DD} = 50$  Vdc,  $I_{DQ} = 100$  mA,  $P_{out} = 250$  W Peak (25 Watts Avg.),  $f = 960$ -1215 MHz, Pulse Width = 128  $\mu$ sec, Duty Cycle = 10%  
Power Gain — 19.8 dB  
Drain Efficiency — 58%

### Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 50  $V_{DD}$  Operation
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- In Tape and Reel. R5 Suffix = 50 Units, 56 mm Tape Width, 13-inch Reel.

**MMRF1008HR5**  
**MMRF1008HSR5**

**960-1215 MHz, 275 W, 50 V**  
**PULSE**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +100	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	$^{\circ}$ C
Case Operating Temperature	$T_C$	150	$^{\circ}$ C
Operating Junction Temperature (1)	$T_J$	225	$^{\circ}$ C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80 $^{\circ}$ C, 275 W Peak 128 $\mu$ sec Pulse Width, 10% Duty Cycle	$Z_{\theta JC}$	0.08	$^{\circ}$ C/W

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	10	$\mu\text{A dc}$
Drain-Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 100\text{ mA}$ )	$V_{(BR)DSS}$	110	—	—	Vdc
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 50\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{A dc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 90\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	100	$\mu\text{A dc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 662\ \mu\text{A dc}$ )	$V_{GS(th)}$	0.9	1.7	2.4	Vdc
Gate Quiescent Voltage ( $V_{DD} = 50\text{ Vdc}$ , $I_D = 100\text{ mA dc}$ , Measured in Functional Test)	$V_{GS(Q)}$	1.7	2.4	3.2	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1.6\text{ A dc}$ )	$V_{DS(on)}$	—	0.25	—	Vdc

**Dynamic Characteristics** (1)

Reverse Transfer Capacitance ( $V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	0.46	—	pF
Output Capacitance ( $V_{DS} = 50\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	352	—	pF
Input Capacitance ( $V_{DS} = 50\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz)	$C_{iss}$	—	695	—	pF

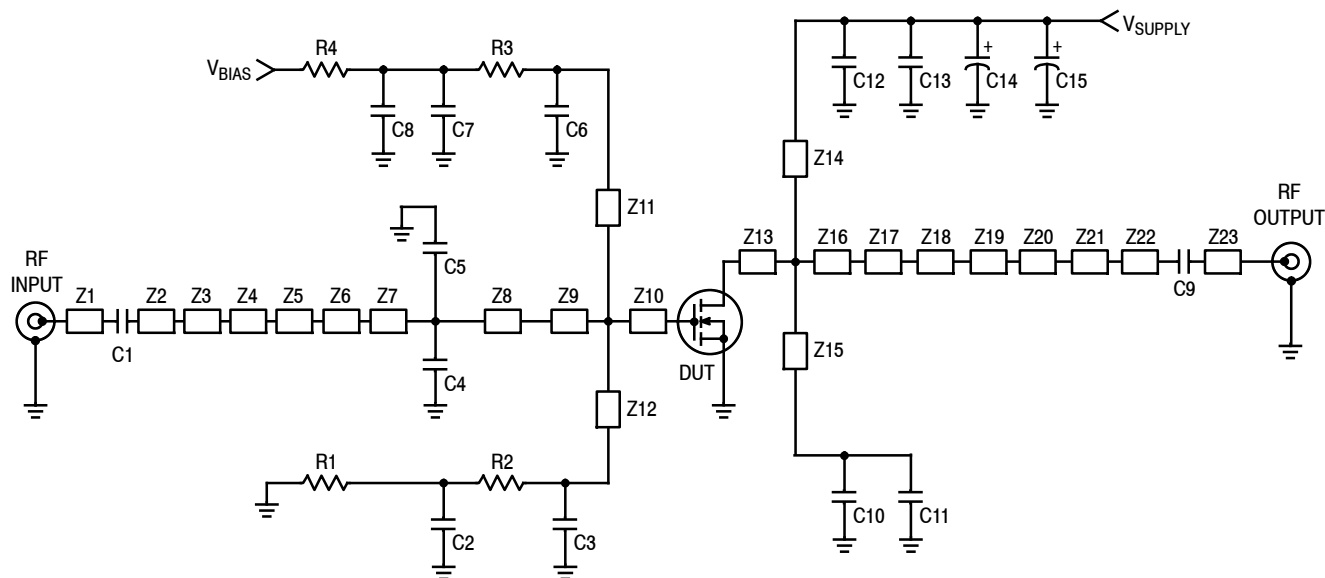
**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 50\text{ Vdc}$ ,  $I_{DQ} = 100\text{ mA}$ ,  $P_{out} = 275\text{ W Peak}$  (27.5 W Avg.),  $f = 1030\text{ MHz}$ , Pulse, 128  $\mu\text{sec}$  Pulse Width, 10% Duty Cycle

Power Gain	$G_{ps}$	19	20.3	22	dB
Drain Efficiency	$\eta_D$	63	65.5	—	%
Input Return Loss	IRL	—	-14	-9	dB

**Typical Broadband Performance — 960-1215 MHz** (In Freescale 960-1215 MHz Test Fixture, 50 ohm system)  $V_{DD} = 50\text{ Vdc}$ ,  $I_{DQ} = 100\text{ mA}$ ,  $P_{out} = 250\text{ W Peak}$  (25 W Avg.),  $f = 960\text{--}1215\text{ MHz}$ , Pulse, 128  $\mu\text{sec}$  Pulse Width, 10% Duty Cycle

Power Gain	$G_{ps}$	—	19.8	—	dB
Drain Efficiency	$\eta_D$	—	58	—	%

1. Part internally matched both on input and output.



Z1	1.055" x 0.082" Microstrip	Z13	0.190" x 1.250" Microstrip
Z2	0.100" x 0.082" Microstrip	Z14, Z15	0.517" x 0.080" Microstrip
Z3	0.084" x 0.395" Microstrip	Z16	0.225" x 1.250" Microstrip
Z4	0.419" x 0.040" Microstrip	Z17	0.860" x 0.975" Microstrip
Z5	0.498" x 0.466" Microstrip	Z18	0.140" x 0.950" Microstrip
Z6	0.110" x 1.060" Microstrip	Z19	0.028" x 0.110" Microstrip
Z7	0.050" x 1.300" Microstrip	Z20	0.397" x 0.040" Microstrip
Z8	0.092" x 1.300" Microstrip	Z21	0.264" x 0.480" Microstrip
Z9	0.219" x 1.420" Microstrip	Z22	0.100" x 0.082" Microstrip
Z10	0.087" x 1.420" Microstrip	Z23	0.521" x 0.082" Microstrip
Z11, Z12	0.187" x 0.050" Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$

**Figure 1. MMRF1008HR5(HSR5) Test Circuit Schematic**

**Table 5. MMRF1008HR5(HSR5) Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1, C4, C5	1.5 pF Chip Capacitors	ATC100B1R5BT500XT	ATC
C2, C7, C11, C13	2.2 $\mu$ F, 100 V Chip Capacitors	G2225X7R225KT3AB	ATC
C3, C6, C10, C12	33 pF Chip Capacitors	ATC100B330JT500XT	ATC
C8	22 $\mu$ F, 25 V Chip Capacitor	TPSD226M025R0200	AVX
C9	9.1 pF Chip Capacitor	ATC100B9R1CT500XT	ATC
C14, C15	470 $\mu$ F, 63 V Electrolytic Capacitors	MCGPA63V477M13X26-RH	Multicomp
R1, R2, R3, R4	0 $\Omega$ , 3.5 A Chip Resistors	CRCW12060000Z0EA	Vishay

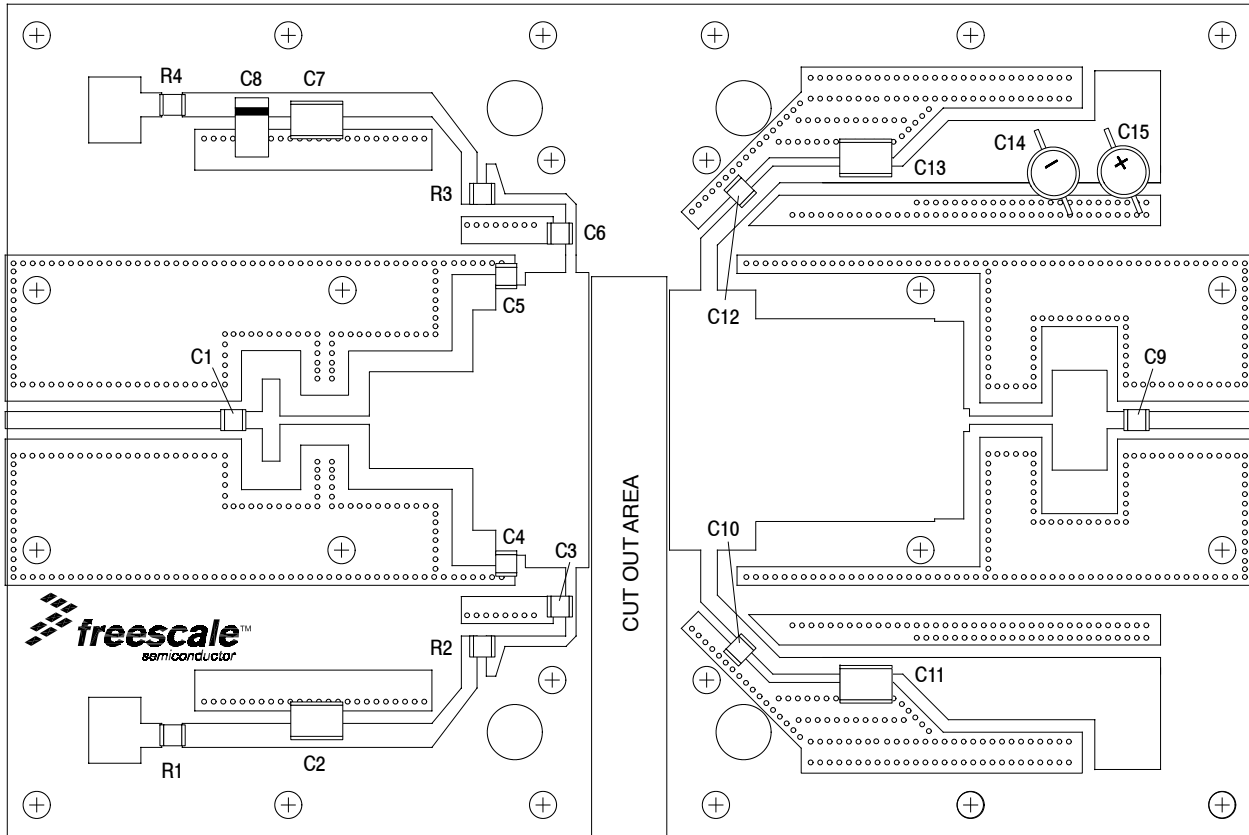
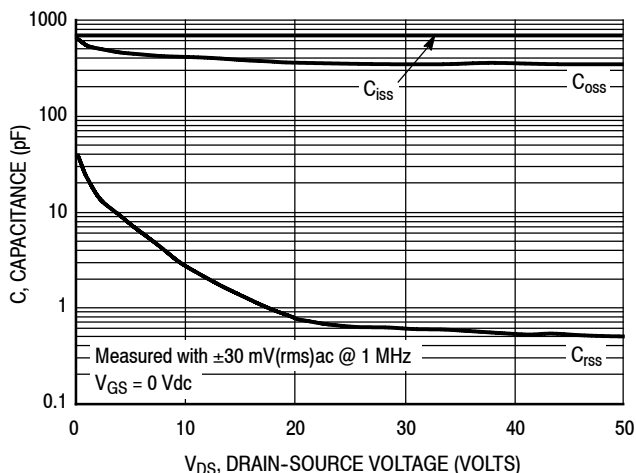
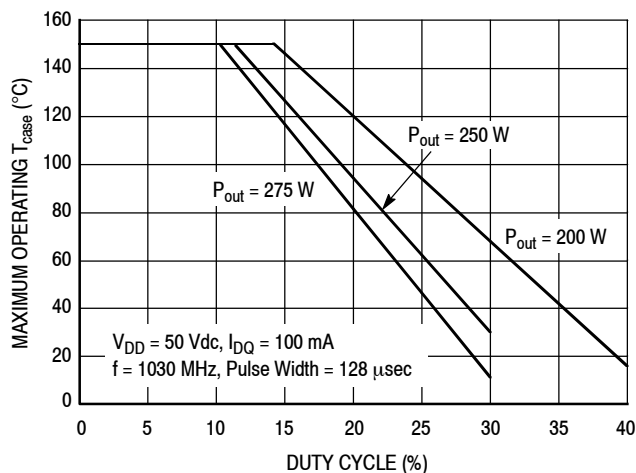


Figure 2. MMRF1008HR5(HSR5) Test Circuit Component Layout

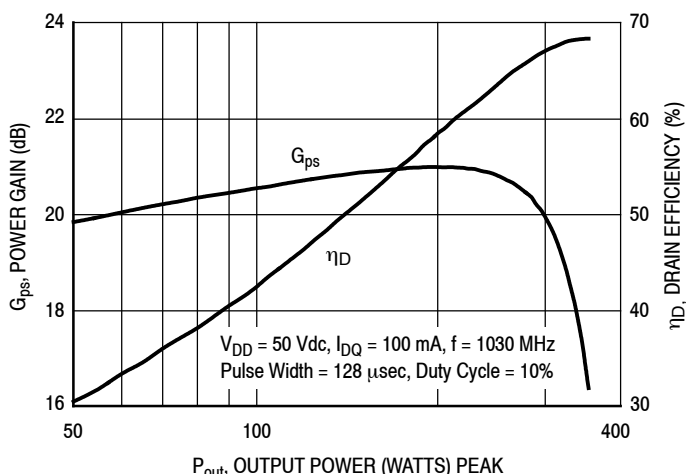
## TYPICAL CHARACTERISTICS



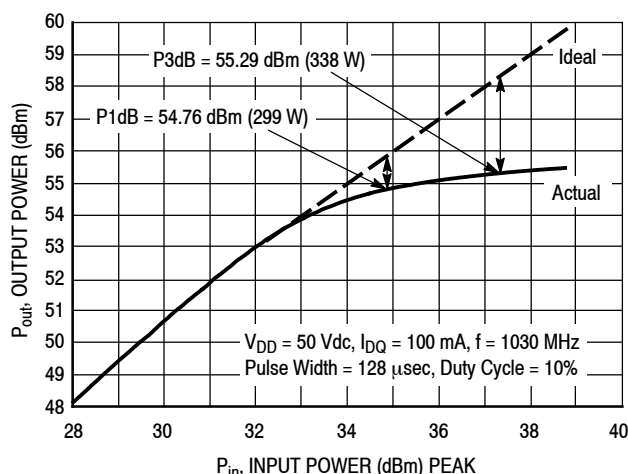
**Figure 3. Capacitance versus Drain-Source Voltage**



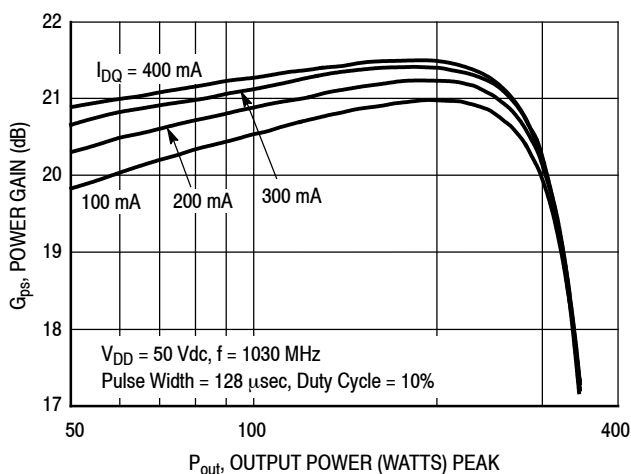
**Figure 4. Safe Operating Area**



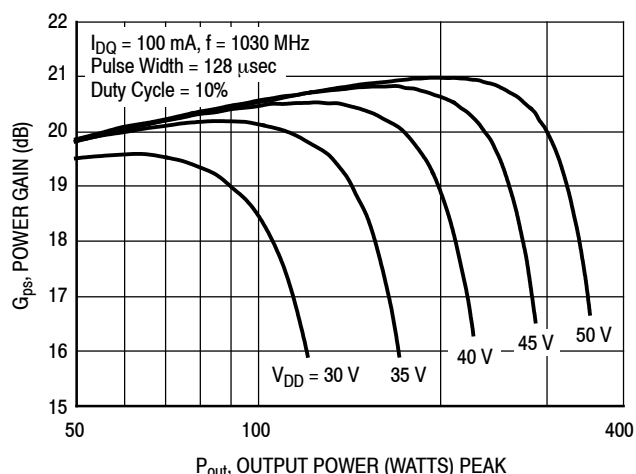
**Figure 5. Power Gain and Drain Efficiency versus Output Power**



**Figure 6. Output Power versus Input Power**

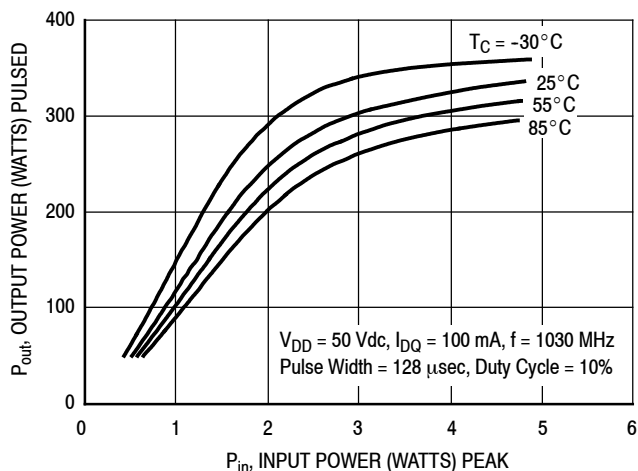


**Figure 7. Power Gain versus Output Power**

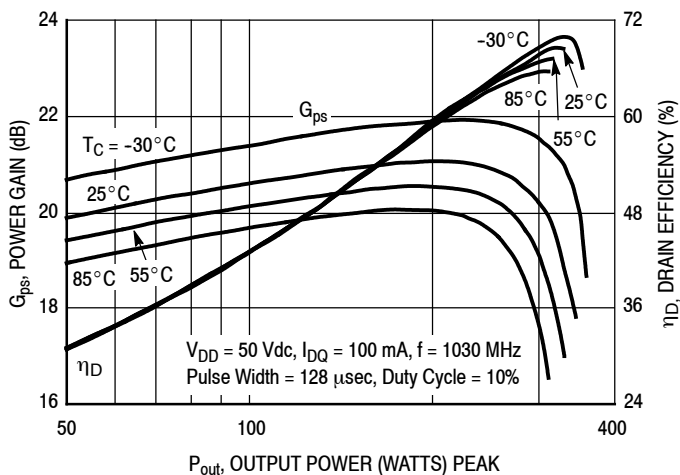


**Figure 8. Power Gain versus Output Power**

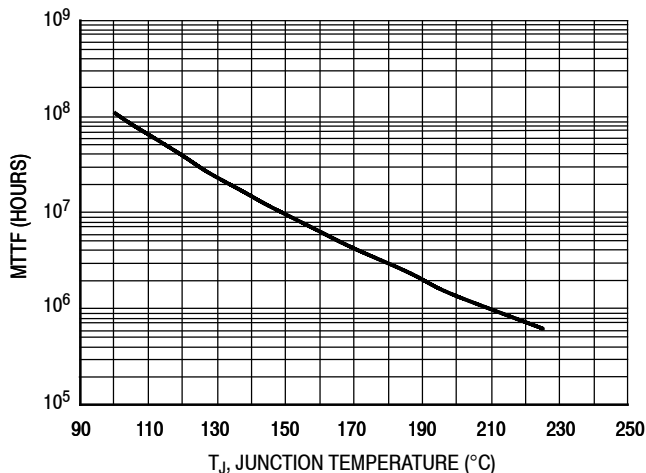
## TYPICAL CHARACTERISTICS



**Figure 9. Output Power versus Input Power**



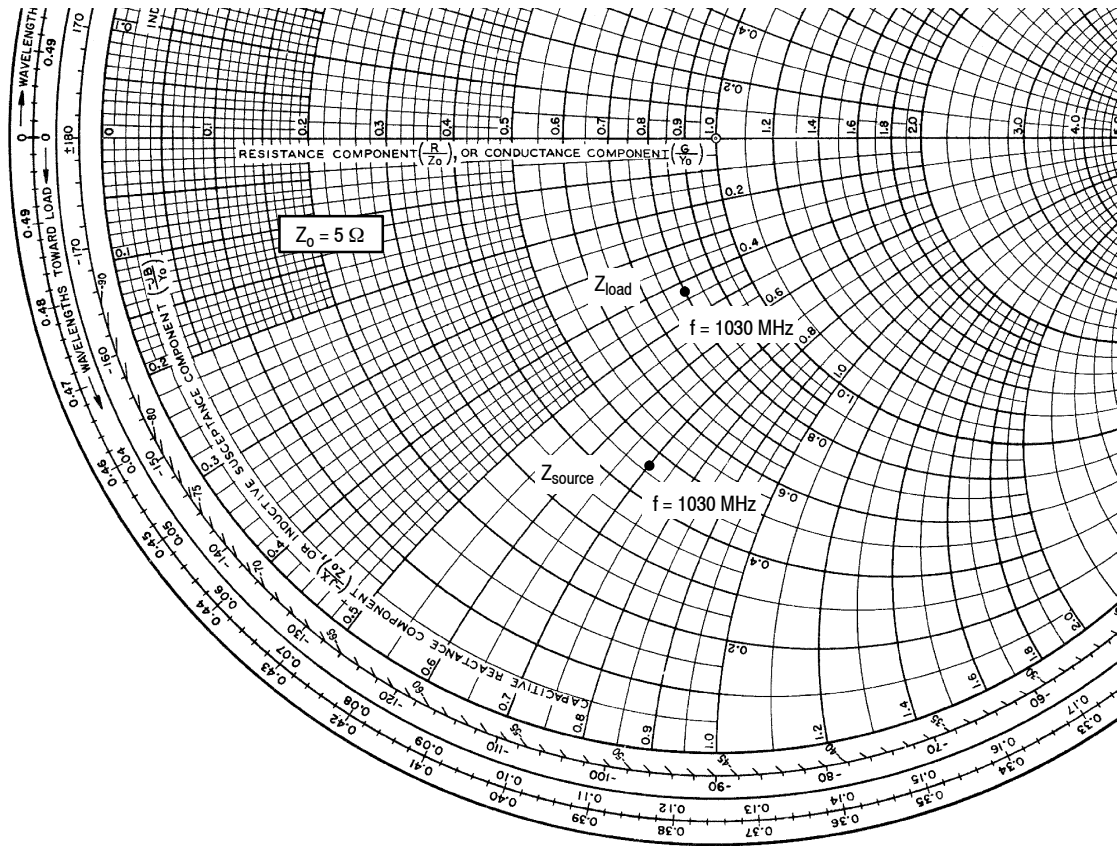
**Figure 10. Power Gain and Drain Efficiency versus Output Power**



This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 50$  Vdc,  $P_{out} = 275$  W Peak, Pulse Width = 128  $\mu$ sec, Duty Cycle = 10%, and  $\eta_D = 65.5\%$ .

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 11. MTTF versus Junction Temperature**



$V_{DD} = 50 \text{ Vdc}$ ,  $I_{DQ} = 100 \text{ mA}$ ,  $P_{out} = 275 \text{ W Peak}$

f MHz	Z <sub>source</sub> Ω	Z <sub>load</sub> Ω
1030	2.30 - j3.51	4.0 - j2.14

Z<sub>source</sub> = Test circuit impedance as measured from gate to ground.

Z<sub>load</sub> = Test circuit impedance as measured from drain to ground.

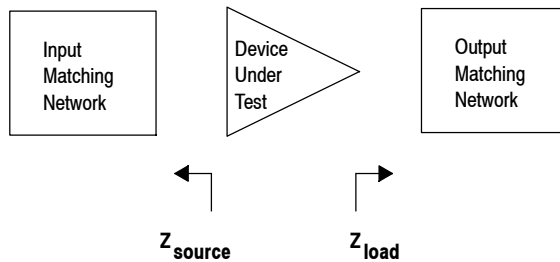


Figure 12. Series Equivalent Source and Load Impedance

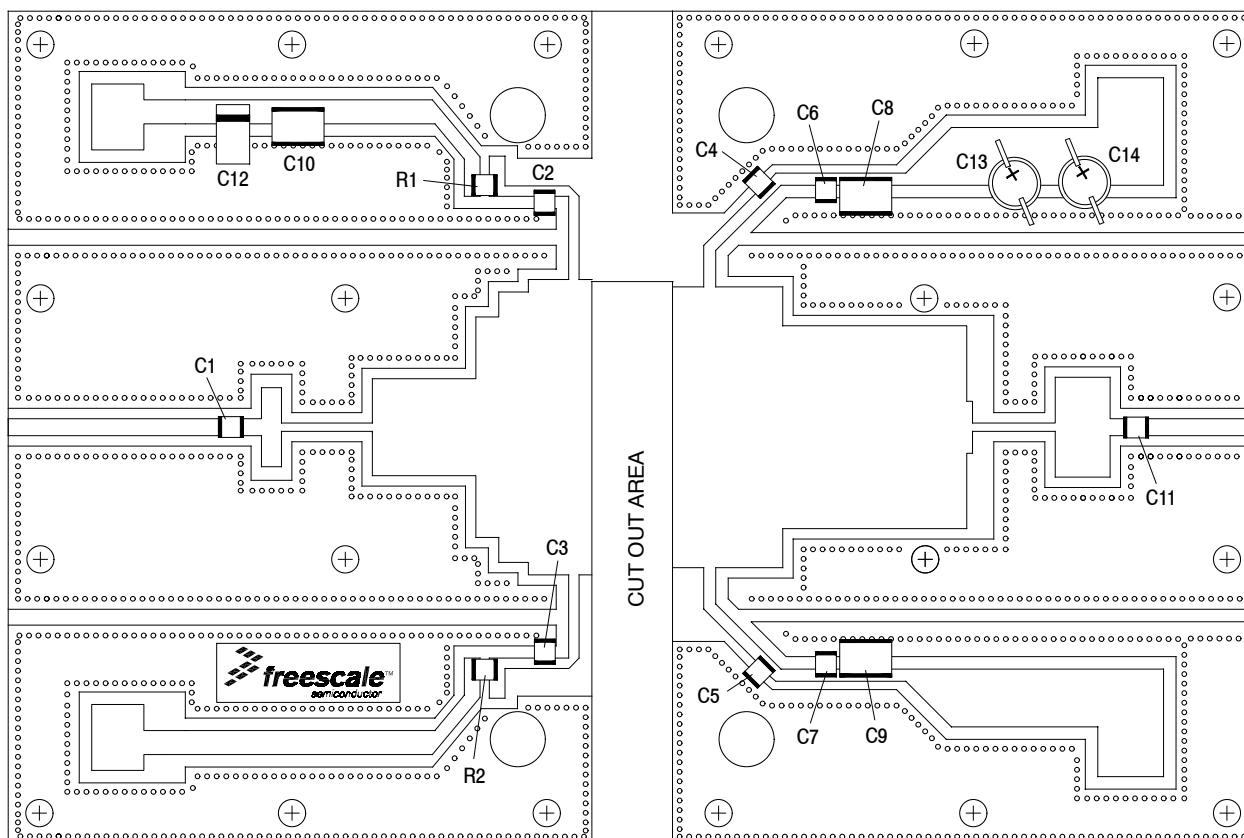


Figure 13. MMRF1008HR5(HSR5) Test Circuit Component Layout — 960-1215 MHz

Table 6. MMRF1008HR5(HSR5) Test Circuit Component Designations and Values — 960-1215 MHz

Part	Description	Part Number	Manufacturer
C1	2.7 pF Chip Capacitor	ATC100B2R7BT500XT	ATC
C2, C3, C4, C5	33 pF Chip Capacitors	ATC100B330JT500XT	ATC
C6, C7	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C8, C9, C10	2.2 $\mu$ F, 100 V Chip Capacitors	G2225X7R225KT3AB	ATC
C11	9.1 pF Chip Capacitor	ATC100B9R1CT500XT	ATC
C12	22 $\mu$ F, 25 V Tantalum Capacitor	TPSD226M025R0200	AVX
C13, C14	470 $\mu$ F, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1, R2	47 $\Omega$ , 1/4 W Chip Resistors	CRCW120647R0FKEA	Vishay
PCB	0.030", $\epsilon_r = 2.55$	AD255A	Arlon



TYPICAL CHARACTERISTICS — 960-1215 MHz

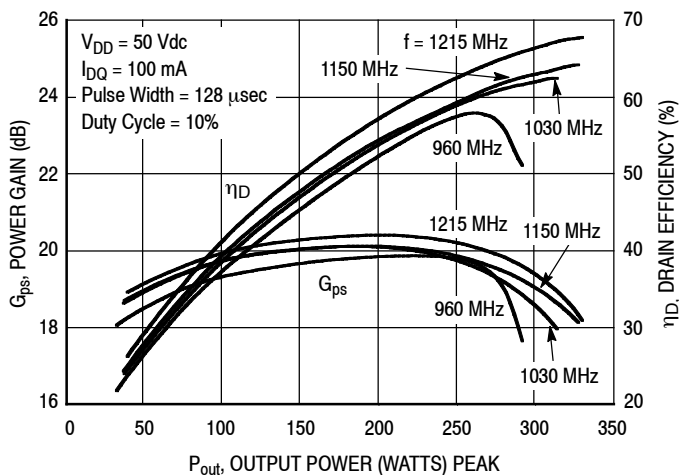


Figure 14. Power Gain and Drain Efficiency versus Output Power

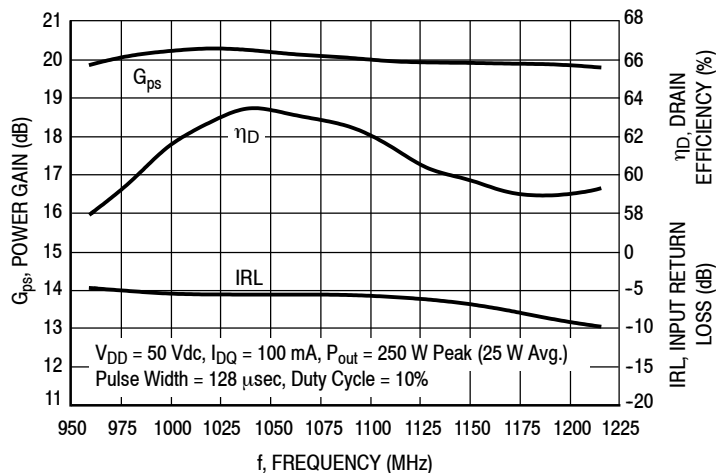
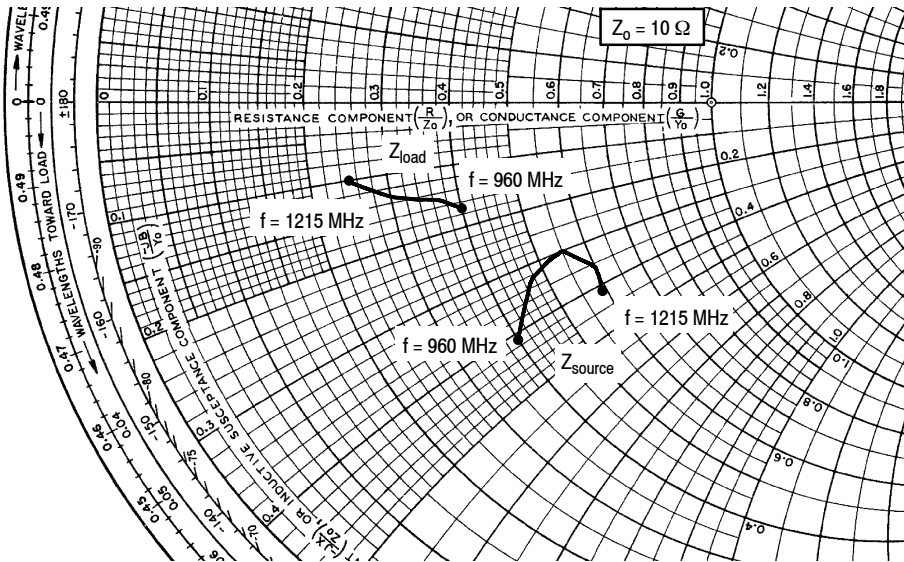


Figure 15. Broadband Performance @  $P_{out} = 250$  Watts Peak



$V_{DD} = 50 \text{ Vdc}$ ,  $I_{DQ} = 100 \text{ mA}$ ,  $P_{out} = 250 \text{ W Peak}$

f MHz	$Z_{source} \Omega$	$Z_{load} \Omega$
960	4.00 - j4.14	3.96 - j1.70
970	4.05 - j3.99	3.90 - j1.67
980	4.16 - j3.86	3.83 - j1.66
990	4.33 - j3.71	3.75 - j1.66
1000	4.49 - j3.57	3.70 - j1.65
1010	4.61 - j3.43	3.68 - j1.62
1020	4.66 - j3.33	3.69 - j1.59
1030	4.68 - j3.26	3.69 - j1.54
1040	4.72 - j3.20	3.67 - j1.52
1050	4.83 - j3.13	3.59 - j1.53
1060	5.02 - j3.06	3.48 - j1.53
1070	5.24 - j2.99	3.38 - j1.53
1080	5.42 - j2.96	3.32 - j1.51
1090	5.51 - j2.99	3.30 - j1.47

$V_{DD} = 50 \text{ Vdc}$ ,  $I_{DQ} = 100 \text{ mA}$ ,  $P_{out} = 250 \text{ W Peak}$

f MHz	$Z_{source} \Omega$	$Z_{load} \Omega$
1100	5.49 - j3.04	3.32 - j1.43
1110	5.47 - j3.07	3.31 - j1.42
1120	5.52 - j3.09	3.24 - j1.40
1130	5.68 - j3.13	3.12 - j1.39
1140	5.89 - j3.20	2.99 - j1.36
1150	6.06 - j3.32	2.88 - j1.30
1160	6.09 - j3.47	2.83 - j1.23
1170	5.98 - j3.60	2.83 - j1.19
1180	5.85 - j3.69	2.80 - j1.15
1190	5.78 - j3.76	2.75 - j1.11
1200	5.81 - j3.87	2.65 - j1.07
1210	5.89 - j4.02	2.52 - j1.01
1215	5.91 - j4.11	2.47 - j0.97

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

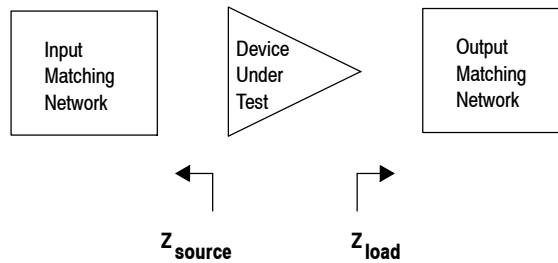
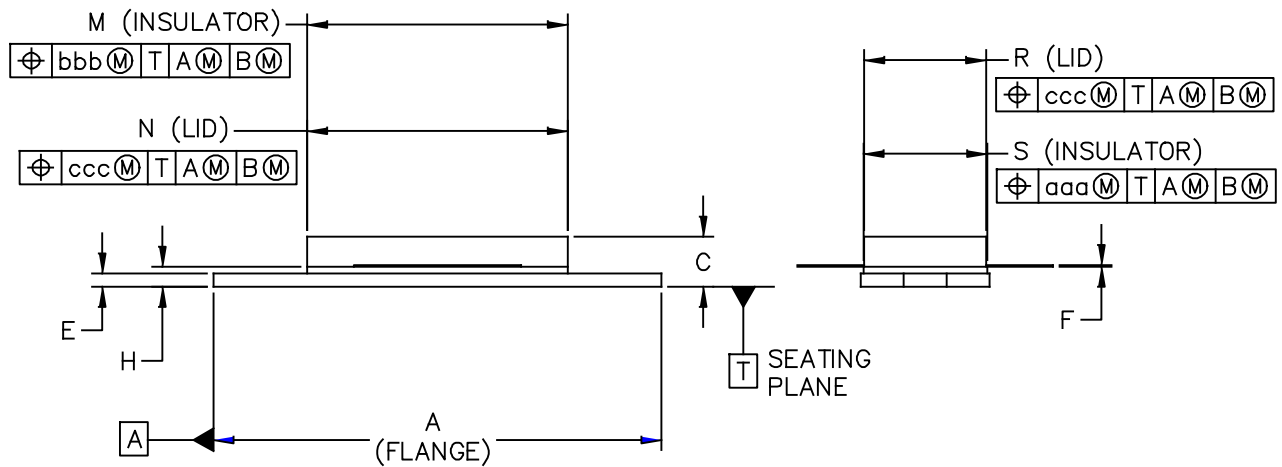
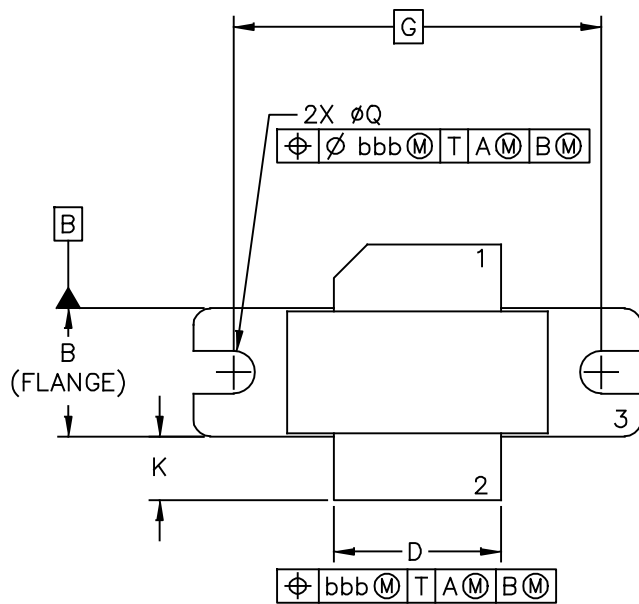


Figure 16. Series Equivalent Source and Load Impedance — 960-1215 MHz

## PACKAGE DIMENSIONS



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TITLE:  <div style="text-align: center; font-size: 1.2em;">NI-780</div>	DOCUMENT NO: 98ASB15607C CASE NUMBER: 465-06 STANDARD: NON-JEDEC	REV: G 31 MAR 2005	

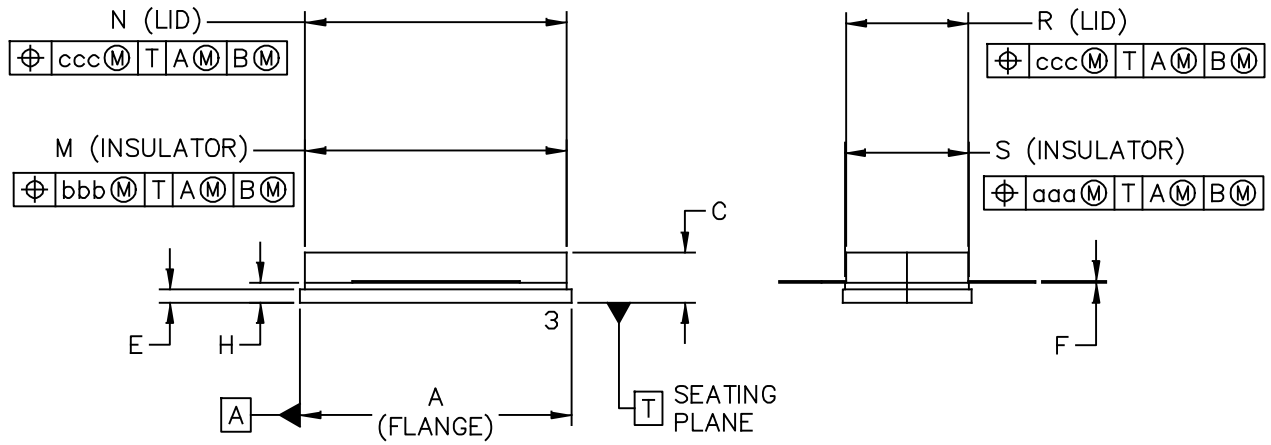
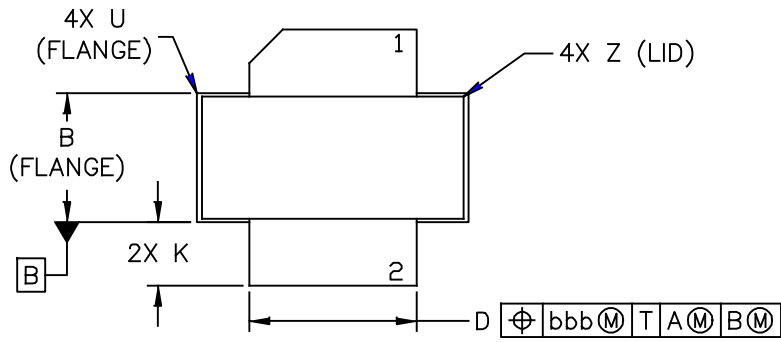
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	1.335	– 1.345	33.91	– 34.16	R	.365	– .375	9.27	– 9.53
B	.380	– .390	9.65	– 9.91	S	.365	– .375	9.27	– 9.52
C	.125	– .170	3.18	– 4.32	aaa	– .005	–	– 0.127	–
D	.495	– .505	12.57	– 12.83	bbb	– .010	–	– 0.254	–
E	.035	– .045	0.89	– 1.14	ccc	– .015	–	– 0.381	–
F	.003	– .006	0.08	– 0.15	–	–	–	–	–
G	1.100 BSC		27.94 BSC		–	–	–	–	–
H	.057	– .067	1.45	– 1.7	–	–	–	–	–
K	.170	– .210	4.32	– 5.33	–	–	–	–	–
M	.774	– .786	19.66	– 19.96	–	–	–	–	–
N	.772	– .788	19.6	– 20	–	–	–	–	–
Q	∅.118	– ∅.138	∅3	– ∅3.51	–	–	–	–	–
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TITLE:  NI-780					DOCUMENT NO: 98ASB15607C			REV: G	
					CASE NUMBER: 465-06			31 MAR 2005	
					STANDARD: NON-JEDEC				



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TITLE:  NI-780S		DOCUMENT NO: 98ASB16718C		REV: H	
		CASE NUMBER: 465A-06		31 MAR 2005	
		STANDARD: NON-JEDEC			

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	– .815	20.45	– 20.7	U	–	– .040	–	– 1.02
B	.380	– .390	9.65	– 9.91	Z	–	– .030	–	– 0.76
C	.125	– .170	3.18	– 4.32	aaa	–	.005 –	–	0.127 –
D	.495	– .505	12.57	– 12.83	bbb	–	.010 –	–	0.254 –
E	.035	– .045	0.89	– 1.14	ccc	–	.015 –	–	0.381 –
F	.003	– .006	0.08	– 0.15	–	–	– –	–	– –
H	.057	– .067	1.45	– 1.7	–	–	– –	–	– –
K	.170	– .210	4.32	– 5.33	–	–	– –	–	– –
M	.774	– .786	19.61	– 20.02	–	–	– –	–	– –
N	.772	– .788	19.61	– 20.02	–	–	– –	–	– –
R	.365	– .375	9.27	– 9.53	–	–	– –	–	– –
S	.365	– .375	9.27	– 9.52	–	–	– –	–	– –

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TITLE:  NI–780S	DOCUMENT NO: 98ASB16718C CASE NUMBER: 465A–06 STANDARD: NON–JEDEC	REV: H 31 MAR 2005

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2013	• Initial Release of Data Sheet

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