

The Right Choice for HMI Designs

RZ/A1 Embedded ARM® Microprocessors

Expanded product family – now with Linux support





RZ/A1 Embedded ARM® Microprocessors

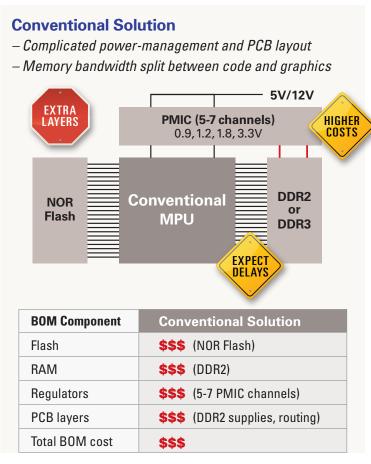
Innovative Architecture & Advanced Integration

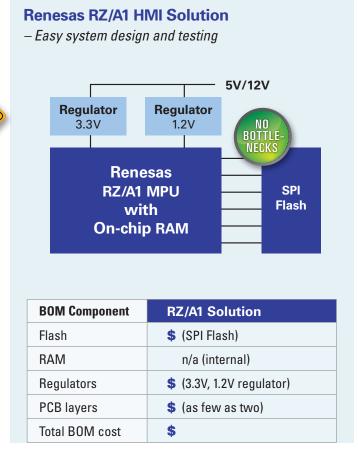
Renesas RZ/A1 series microprocessors (MPUs) offer an innovative architecture based on the ARM Cortex®-A9 processor and up to an industry-leading 10 MB of on-chip memory. RZ/A1 MPUs can execute code at 1000 DMIPS from the abundant on-chip memory or in-place from inexpensive QSPI memory, while using on-chip memory for graphics buffering up to WXGA (1280x800) resolution. The 128-bit wide internal memory bus with x4 parallel access enables higherthroughput memory access as compared to systems with external DDR memory. The RZ/A1 series offers enormous advantages in terms of BOM cost, performance, power consumption, and system design time, making it the right choice for Human Machine Interface (HMI) and other system-on-chip applications.



- ARM Cortex®-A9 processor that can execute code at 1000 DMIPS
- Remove need for external RAM with up to 10 MBs of on-chip RAM
- Execute-In-Place (XIP) from QSPI memory enabled with three layers of cache
- Up to two Camera inputs available for video and graphics blending usages
- Scalable line-up with three sizes of on-chip RAM to choose from: 3 MB (RZ/A1L or RZ/A1LU), 5 MB (RZ/A1M), and 10 MB (RZ/A1H)
- Implement up to two independent LCD displays with WXGA (1280x800) resolution for impressive graphical user interfaces

Renesas RZ/A1 solution streamlines board design and reduces BOM cost

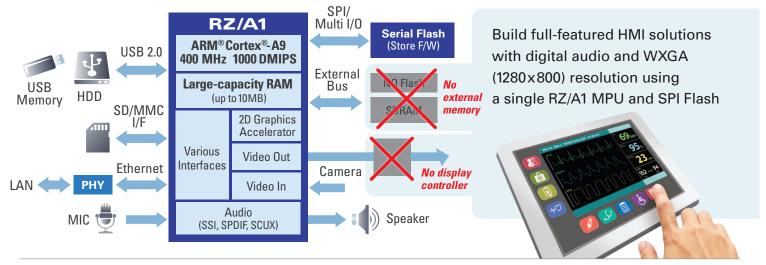




Create superior HMI designs with fewer components

On-chip functions provided by RZ/A1 MPUs reduce BOM cost, save board space and minimize integration tasks. Typical applications like the one shown below take advantage of a rich portfolio of intellectual property from Renesas and can utilize a range of built-in peripherals, including: CMOS camera interface, JPEG Codec Unit, 12-bit ADC, and OpenVG 2D graphics engine, among others.

RZ/A1 Series System Diagram



Features

Up to 10 MB on-chip RAM

■ For code execution/data buffering

128-bit memory bus

With parallel (x4) access to deliver superior memory throughput

Execute-In-Place (XIP) from inexpensive QSPI memory

With three layers of cache

LCD controller to drive up to two independent WXGA displays

For vivid displays

Graphics Capabilities

	RZ	/A1L	RZ/A1M		RZ/A1	Н		
sef 4	0.6 MB	1.0 MB	4.7 MB	5.9 MB	7.3 MB	9.4 MB		
f Images Buffer 8	0.4 MB	0.7 MB	3.5 MB	4.4 MB	5.5 MB	7.0 MB	9.0 MB	
umber of in Frame I	0.3	0.5	2.3	2.9	3.7	4.7	6.0	7.8
	MB	MB	MB	MB	MB	MB	MB	MB
Num 1	0.1	0.2	1.2	1.5	1.8	2.3	3.0	3.9
	MB	MB	MB	MB	MB	MB	MB	MB
	QVGA	WQVGA	VGA	WVGA	SVGA	WSVGA	XGA	WXGA
	320x240	480x272	640x480	800x480	800x600	1024x600	1024x768	1280x800
	16bpp	16bpp	32bpp	32bpp	32bpp	32bpp	32bpp	32bpp

Display Resolutions Supported by RZ/A1 MPUs

Benefits

Lower BOM Cost

- No external SDRAM or LCD controller
- Simpler voltage regulators
- Reduced PCB layers

Increased Performance

- 1000 DMIPS at 400 MHz
- 6x throughput of 333 MHz 16-bit DDR2

Decreased Power Consumption

- Fewer board components
- No copying of code from flash to RAM

Accelerate Time to Market

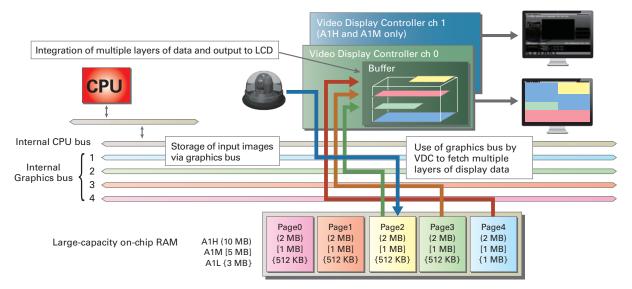
- Simpler PCB design
- Decreased EMI via reduced switching



One RZ/A1 MPU can accommodate an entire software stack (libraries, operating system and application code), plus a graphics frame buffer.

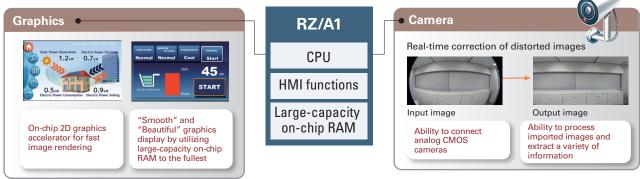
Graphics display and camera input capabilities on a single chip

RZ/A1 MPUs have a unique combination of graphics display and camera functions that, coupled with their parallel-access, 128-bit memory bus, enables systems with rich graphical and video capabilities.



The bus configuration, with independent buses for images and hardware-based superimposition processing, makes it easy to create graphical applications.





Target applications

The performance of the ARM Cortex-A9 MPU and the simplicity of a MCU-style platform design makes the RZ/A1 MPU the ideal choice for a range of applications, such as those shown below.



Renesas RZ/A1 packaging options

176-LFBGA



176-LFQFP



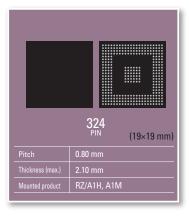
208-LFQFP



256-LFBGA



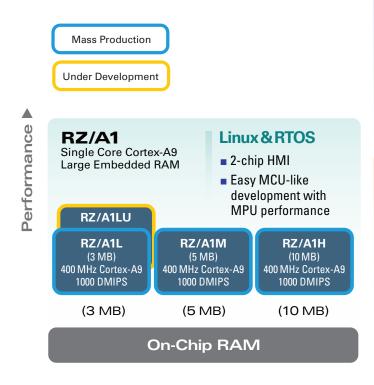
324-FBGA



256-LFQFP



RZ Family of ARM-based MPUs



Linux & Android

- High-end graphics, video and network gateways
- Easy development with Linux and Android open-source software

RZ/G1

Dual Core Cortex-A7 & Cortex-A15 options

RZ/G1E 1 GHz Dual Cortex-A7 3800 DMIPS RZ/G1M 1.5 GHz Dual Cortex-A15 10500 DMIPS

RZ/T RTOS

Industrial

Ethernet RZ/T1

(1.5 MB) 450-600 MHz Cortex-R4F & Cortex-M3 (RIN) 747-996 DMIPS

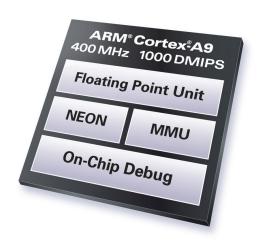
DDR3 (1 ch) DDR3 (2 ch)

External DDR

RZ/A1H and RZ/A1M MPUs

Best choices for higher-end HMI designs (up to WXGA resolution)

- Buffer up to two independent WXGA (1280x800) images with a single RZ/A1H MPU chip
- Buffer up to two WSVGA (1024x600) images or a single WXGA (1280x800) image with one RZ/A1M MPU chip
- Utilize the on-chip OpenVG graphics engine for impressive 2D graphics acceleration
- Connect to one or two independent LCD displays
- Exploit additional peripherals, including: NAND Flash interface, JPEG Codec Unit, IMR engine, sound generator, NTSC/PAL decoder for video, and PWM timer



Highly Efficient 32-bit CPU Core (ARM Cortex-A9)

- 1000 DMIPS performance at 400MHz
- ARM NEON multimedia engine
- Boots from parallel or serial flash

10 MB (RZ/A1H) and 5 MB (RZ/A1M) Internal RAM

- Use as large data buffer or to run system from internal memory
- Employs parallel bus structure dedicated to SRAM to speed processing

Execute-In-Place Operation from QSPI Flash

- Take full advantage of cost-effective external serial flash
- Simplifies program execution

Single- and Double-Precision Floating Point Unit, IEEE754 Compliant

 Accelerates trigonometric operations such as scaling and rotation

2D-Graphics Engine with OpenVG 1.1 Capability

- Fully supports the Khronos™ OpenVG 1.1 API
- Offloads CPU for rendering, animation and video acceleration operations

LCD Controller with 24-bit RGB and 16-bit LVDS Interfaces

- Handles 4-layer overlays
- Provides 2-ch video input, 2-ch display output with 1 ch of LVDS
- Implements alpha blending
- Supports chroma keying

Bus Interface Controller

 Directly connects to SRAM, SDRAM, and flash (NOR, NAND, eMMC), as well as 128 KB L2 cache

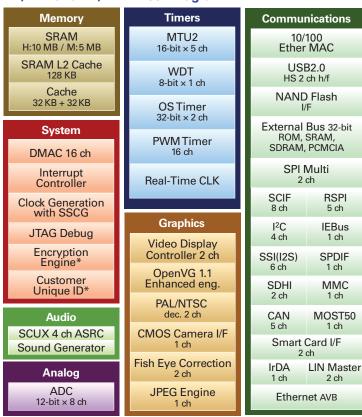
Multiple Network Connectivity Interfaces

- Integrates 10/100 EtherMAC controller (1 ch)
- Includes USB 2.0 host and function controller with integrated USB transceiver (2 ch)
- Offers up to 5 CAN channels

Three Package Options

- 324-pin BGA (0.8 mm)
- 256-pin QFP (0.4 mm)
- 256-pin BGA (0.5 mm)

RZ/A1H and RZ/A1M Block Diagram



RZ/A1L MPUs

Ideal solutions for cost-sensitive designs (up to WSVGA resolution)

- Buffer up to WSVGA (1024x600) images in internal memory
- Accelerate multimedia processing with ARM NEON™SIMD (Single Instruction, Multiple Data) engine
- Connect to single LCD display

Single- and Double-Precision Floating Point Unit, IEEE754 Compliant

 Accelerates trigonometric operations such as scaling and rotation

LCD Controller with 24-bit RGB Interface

- Handles 3-layer overlays
- Provides 1-ch video input,1-ch display output
- Implements alpha blending
- Supports chroma keying

Bus Interface Controller

 Directly connects to SRAM, SDRAM, and flash (NOR, NAND, eMMC), as well as 128 KB L2 cache

RZ/A1LU MPUs

More features to expand system capabilities

- Secure Boot and Secure Communications with optional security unit
- Simplify designs with JPEG Codec Unit
- Transport audio and video over Ethernet with Ethernet AVB support
- Use Dual-Data-Rate QSI support to get higher bandwidth access to the SPI Flash

Highly Efficient 32-bit CPU Core (ARM Cortex-A9)

- 1000 DMIPS performance at 400 MHz
- ARM NEON multimedia engine
- Boots from parallel or serial flash

3 MB Internal RAM

- Use as large data buffer or to run system from internal memory
- Employs parallel bus structure dedicated to SRAM to speed processing

Execute-In-Place Operation from QSPI Flash

- Take full advantage of cost-effective external serial flash
- Simplifies program execution

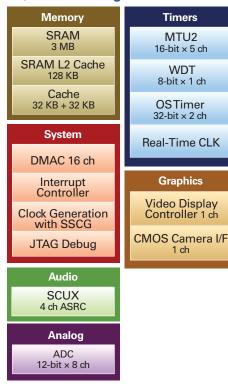
Multiple Network Connectivity Interfaces

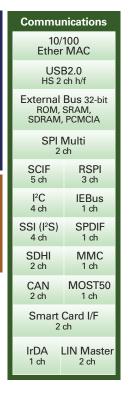
- Integrates 10/100 EtherMAC controller (1 ch)
- Includes USB 2.0 host and function controller with integrated USB transceiver (2 ch)
- Offers up to 2 CAN channels

Three Package Options

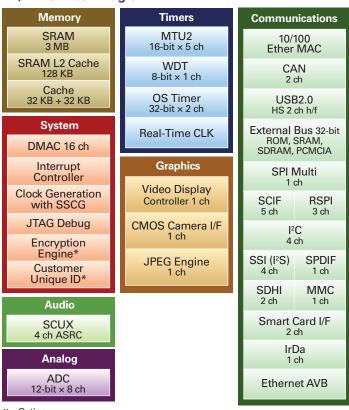
- 208-pin QFP (0.5 mm)
- 176-pin QFP (0.5 mm)
- 176-pin BGA (0.5 mm)

RZ/A1L Block Diagram





RZ/A1LU Block Diagram



Renesas RZ/A1 Device Selector

	RZ/A1H			RZ/A1M				RZ/A1L				RZ/A1LU								
Pin count	256-pin					176-pin 208-pin														
Product name	R7S7210 00VCBG	R7S7210 00VCFP	R7S7210 00VLFP	R7S7210 01VCBG	R7S7210 01VLBG	R7S7210 10VCBG	R7S7210 10VCFP	R7S7210 10VLFP	R7S7210 11VCBG	R7S7210 11VLBG	R7S7210 20VCBG	R7S7210 20VCFP	R7S7210 20VLFP	R7S7210 21VCFP	R7S7210 21VLFP	R7S7210 30VCBG	R7S7210 30VCFP	R7S7210 30VLFP	R7S7210 31VCFP	R7S7210 31VLFP
CPU core		ARM® Cortex®-A9																		
RAM	10 MB 5 MB 3 MB 3 MB																			
Cache memory		Primary cache: 64 KB (instruction 32 KB/data32 KB), TLB128 Secondary cache: 128 KB (Corelink**Level 2 Cache Controller L2C-310)																		
Max. operating frequency (MHz)		Seculturi y cache. 120 kb (curentik Level 2 cache cuntumer L20-310) 400																		
Subclock (external: 32.768kHz)	Yes																			
PLL											es									
Real-time clock											es									
Power-on reset											es									
Floating-point unit											es									
DMA External memory	Sorial flac	h (eXecute	-In-Place (YIP) suppor	-+1	Sprial flag	h la Yacuta	e-In-Place (YIP) sunnor		× 16 ch	h (a Yacuta	-In-Place ((IP) suppor	·+\	Sprial flag	ch (a Yacuta	-In-Place (YIP) suppor	rt)
interfaces External	SRAM, SI	DRAM, burs	st ROM, NA	ND flash	ч,	SRAM, SI		st ROM, NA	ND flash	ц,	Serial flash (eXecute-In-Place (XIP) support), SRAM, SDRAM, burst ROM				Serial flash (eXecute-In-Place (XI SRAM, SDRAM, burst ROM				ι,,	
interrupt pins	148			180		148			180		109			131		109			131	
I/O ports	139			171		139			171		100			122		100			122	
16-/32-bit timer (ch)										5	/2									
Watchdog timer (ch)		- 4 II D\A/A4	T: 0			1	- 4 II D\A/A	AT: 0			-					1				
Other timers		ntroll PWM	1 imer × 8			Motor Controll PWM Timer × 8 –						-								
PWM output 3-phase PWM output function	16 Yes					16														
12-bit A/D converter (channels)	8																			
CAN (channels)	5 2 2																			
Ethernet	Yes																			
Ethernet AVB	Yes Yes - Yes																			
USB host function										Υ	es									
USB peripheral function										Υ	es									
USB (channels)											2									
USB High Speed support										Υ	es									
USB endpoints		16																		
USB isochronous transfer support	Yes																			
USB additional information	Low-speed Support (host only)																			
SD host interface (channels) MMC host interface		2																		
(channels) Clock-synchronous																				
serial interface (ch) SPI (channels)	17 5					12						3								
UART (channels)	8 8							8					5							
I ² C (channels)	4																			
LIN (channels)	2 2 2 -																			
IEBus (channels)	1	1 1																		
Serial additional information	SCIF (CSI: RSPI (SPI SPDIF (CS	: 5 ch), SPI r	: 8 ch), SCI nulti (SPI: 2	SCI (CSI: 2 ch), PI: 2 ch), SSI (CSI: 6 ch), RSPI (SPI: 5 ch), SPI multi (SPI: 2 ch), SSI (CSI: 6 ch), SPDIF (CSI: 1 ch)					SCIF (CSI: 5 ch/UART: 5 ch), SCI (CSI: 2 ch), RSPI (SPI: 2 ch), SPI multi (SPI: 1 ch), SSI (CSI: 4 ch), SPDIF (CSI: 1 ch)				SCIF (CSI: 5 ch/UART: 5 ch), SCI (CSI: 2 ch), RSPI (SPI: 2 ch), SPI multi (SPI: 1 ch), SSI (CSI: 4 ch), SPDIF (CSI: 1 ch)							
Other display functions	SP DIT (CSL. 1 CIT)																			
Power supply voltage (V)		3.3V/1.18V																		
Power supplies		VCC = PLLVCC = LVDSPLLVCC = USBAVCC = USBDVCC = 1.10 to 1.26 V, PVCC = AVCC = USBAPVCC = VDAVCC = LVDSAPVCC = USBDPVCC = 3.0 to 3.6 V, VSS = AVSS = 0 V																		
Operating temp (°C)										TA = -40	to +85°C									
Package (size [mm])	256- LFBGA (11 × 11 mm)	256- LFQFP (28 × 28 m	m)	324- FBGA (19 × 19 m	m)	256- LFBGA (11 × 11 mm)	256- LFQFP (28 × 28 n	nm)	324- FBGA (19 × 19 m	m)	176- LFBGA (8×8 mm)	176- LFQFP (24×24 mr	n)	208- LFQFP (28×28 mr	m)	176- LFBGA (8×8 mm)	176- LFQFP (24×24 mr	n)	208- LFQFP (28×28 mr	m)

Renesas RZ/A1 Series Starter Kit

Shorten product development cycles with the Renesas Starter Kit (RSK). The RZ/A1 kit includes everything you need to jump-start your system development and ease the design and debug process.

The kit includes:

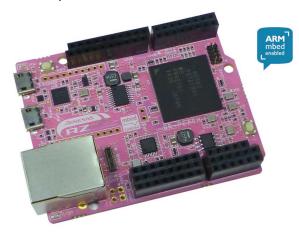
- 800 x 480 touch panel for HMI development (optional)
- Segger JTAG-lite debugger
- Embedded IDE and compiler with evaluation license
- Sample code and peripheral drivers

Part Number	TFT Display	Debugger
YR0K77210S001BE	No	Yes
YR0K77210S003BE	Yes	Yes



Renesas (GR-PEACH) ARM® mbed™ Platform

GR-PEACH from Renesas is an mbed enabled platform that combines the advantages of the mbed ecosystem and Arduino form factor. It is the first and only ARM mbed platform powered by a Cortex®-A class MPU.



Features

- 8 MB Flash
- 2xUSB Host/Device Interface, 1xEthernet
- 3xSPI, 3xI²C, 8xUART, 7x12-bits ADC, 2xCAN
- 2xCamera Input

Arduino form-factor

- Compatible with a wide range of commercially available shields
- Built-in USB 'drag & drop' Flash programmer

mbed.org Developer Website

- Online Compiler
- High-level C/C++ SDK
- Active developer community

https://developer.mbed.org/platforms/Renesas-GR-Peach/

Part Number	Description
YGRPEACHFULL	GR-PEACH
YGRPEACHAUDIOCAMERASHIELD	GR-PEACH Audio Camera Shield
YGRPEACHLCDSHIELD	GR-PEACH LCD Shield

Linux support now available on RZ/A1 MPUs

Implementation Options

- 1. XIP Linux (Execute-in-Place) with Advanced XIP File System (AXFS)
 - Run from QSPI NOR Flash or on-chip SRAM
 - Buildroot and Yocto build options available
- 2. Execute from SDRAM (up to 128 MB SDRAM)

Commercial support

Community support





GPIO

Benefits of XIP Linux on RZ/A1 MPUs

- Direct execution from low-cost Quad-SPI Flash
- Memory size expansion without changing board layout
- Dual QSPI interface provides data access up to 528 Mb/s
- No external memory required
- Kernel memory usage as low as 1.5 MB of RAM
- Advanced XIP File System (AXFS) allows for lowest possible memory usage
- Faster system boot and application startup times
- Faster zero-copy page faults
- Separate buses allow simultaneous instruction fetches, data accesses and LCD frame buffer displaying without contention

Renesas RZ/A1 XIP Linux Solution

MMC

Device drivers provided for:

- Ethernet
- USB Host/
- **USB** Gadget RTC (real-time
- clock)
- NOR Flash
- LCD Display
- Touch Panel
- Audio
- SDHC



Wi-Fi Support – SX-SDCAN for RZ/A1 XIP Linux

802.11 a/b/g/n plus Bluetooth® SDIO Radio Card

This proven connectivity solution has an SD-card form factor that implements a vendor-independent form factor





- Offers IEEE 802.11a/b/g/n conformity (2.4 & 5 GHz)
- Applies single-stream 1x1 SISO technology and 40 MHz bandwidth mode for 5 GHz connectivity
- Supports IEEE 802.11e, IEEE 802.11h and IEEE 802.11i
- Supports SDIO 2.0 as host IF of wireless LAN
- Supports Bluetooth 4.0 + LE dual mode

H.264 Solution Enabled for XIP Linux

Encoder RZ/A1H (Linux XIP) H 264 MPEG2 Network Camera Driver Ethernet Driver Encode TS Mux

Decoder





www.consilient-tech.com

Graphics Support Packages for XIP Linux

Accelerates embedded UI development



Crank Storyboard™Suite www.cranksoftware.com



www.at.io

Speed up your development with the RZ/A1 ecosystem

Integrated Software Development Environments



IAR Embedded Workbench®

- Integrated development environment and optimized compiler for RZ/A1 MPUs
- Project management tools and editor
- Configuration files for all RZ devices
- Emulator debugger support
- Run-time libraries



ARM

- The ARM DS-5™ Development Studio, Renesas RZ Edition, is a complete software development environment for systems that use RZ/A1 MPUs.
- This IDE provides the DS-5's code editor, compiler, debugger and performance analyzer. These tools seamlessly generate, debug and optimize code for the powerful ARM Cortex-A9 CPU built into RZ/A1 series chips.



Renesas e² studio

- Based on the popular Eclipse open-source environment
- Complete IDE supports IAR and free GNU compilers
- Powerful project management
- Download free at: am.renesas.com/e2studio



Green Hills Software

Green Hills Software supports Renesas RZ/A1 MPUs with its MULTI® IDE, C/C++ optimizing compilers, Probe debugger, and many other development tools. These products let system engineers generate fast, compact code, quickly find and fix bugs, and make sense of complex systems.

Real-Time Operating Systems

expresslogic

ThreadX® www.expresslogic.com

Micrium

uC/OS-III® www.micrium.com



FreeRTOS www.freertos.com



Linux BSP

oss.renesas.com



RTX www.keil.com



embOS® www.segger.com



SMX® RTOS www.smxrtos.com

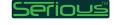


Unison RTOS www.rowebots.com

Graphics Packages

expresslogic

GUIX™ www.expresslogic.com



SHIPTide www.seriousintegrated.com



Crank Storyboard™Suite www.cranksoftware.com





MicroEJ® www.microej.com



DeepScreen® www.altia.com



www.qt.io

emWin™ www.segger.com

Linux Solution

ARM Ecosystem



www.consilient-tech.com

H.264 Solution



www.timesys.com





www.mbed.com

Wi-Fi Solutions







www.murata.com

Fast track your success with RZ Express!

Design your next embedded microprocessor system with Renesas RZ/A1 MPUs and receive Express Logic X-Ware Platform™ and IAR Embedded Workbench® for ARM® *at no cost!**

Renesas, Express Logic and IAR Systems have teamed up to bring you the RZ Express promotion! This is a chance for qualified production customers of the Renesas RZ/A1 microprocessor (MPU) to apply to receive a single-product license of Express Logic's ThreadX[®] real-time operating system (RTOS) and middleware stack, including NetX[™], GUIX[™], FileX[®] and USBX[™], which are all components of the X-Ware Platform, at no cost. Customers who are

chosen to receive this valuable single-product license free





IAR Embedded Workbench®

of charge will also enjoy free software support from Express Logic for 90 days, plus one free IAR Embedded Workbench® for ARM® IDE (Integrated Development Environment) seat. *The RZ Express promotion is available for a limited time, so apply today!*

See website for more details on this offer: renesas.com/rzexpress









RZ Express Benefits

- Pay no royalties! No licensing fees!
- Speed your time to revenue with X-Ware™ by Express Logic and the IAR Systems' Embedded Workbench® for ARM IDE
- Differentiate your product with RZ/A1 ARM® Cortex-A9 MPUs by Renesas
- Use the Express Logic RTOS and middleware, including GUIX[™], to quickly and effectively build differentiated HMI solutions on top of the Renesas RZ/A1 hardware platform



Renesas Ecosystem



*Some restrictions apply

The Alliance Partner Program allows you to connect instantly with hundreds of qualified design consulting and contracting professionals.

am.renesas.com/Alliance



 A forum and community site to share technical information, questions and opinions with others who use Renesas MCUs and MPUs.

www.RenesasRulz.com



Sain the technical knowledge you need. Evaluate, research and learn at your own pace, where you want, when you want, for free.

www.RenesasInteractive.com



> For educators and students. Teach with professional grade tools. Learn MCUs with a modern architecture.

www.RenesasUniversity.com

My Renesas

Customize your data retrieval needs on the Renesas web site. You'll receive updates on the products you're interested in.

am.renesas.com/MyRenesas

Software Library – Free SW

am.renesas.com/softwarelibrary

Free Samples

am.renesas.com/samples

Technical Support

am.renesas.com/tech_support

For additional information, please visit am.renesas.com/RZA





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