Tsi568A Serial RapidIO Switch Hardware Manual

Formal
April 2007
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Product information	www.tundra.com/Tsi568A contains the features, benefits, typical applications, and block diagram for the Tsi568A. This webpage also provides links to other product information located on the Tundra website.
Technical support resources	www.tundra.com/support contains an extensive list of technical resources to assist with your design needs. Some of the key support resources include: • Technical support FAQ • User documentation • Schematic design checklists and debug guidelines You can also opt to receive email notification when a support resource is added or changed.
Technical support request	To contact Tundra support personnel about a technical question, fill out the Technical Support Request Form in the Support section of the website.
Sales support	www.tundra.com/sales contains information that will help you locate a Tundra sales representative nearest you.
Email	docfeedback@tundra.com can be used to provide feedback on a Tsi568A customer document.
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About this Document

This section discusses the following topics:

- "Scope" on page 7
- "Document Conventions" on page 7
- "Revision History" on page 8

Scope

The *Tsi568A Serial RapidIO Switch Hardware Manual* discusses the features, capabilities, and configuration requirements for the Tsi568A. It is intended for hardware and software engineers who are designing system interconnect applications with the device.

Document Conventions

This document uses the following conventions.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase "_b". An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAME_b	NAME_b[3]
Active high	NAME	NAME[3]

Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal's active or inactive state (they are denoted by "_p" and "_n", respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] =1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

Object Size Notation

- A *byte* is an 8-bit object.
- A *word* is a 16-bit object.
- A *doubleword* (Dword) is a 32-bit object.

Numeric Notation

- Hexadecimal numbers are denoted by the prefix *0x* (for example, 0x04).
- Binary numbers are denoted by the prefix *0b* (for example, 0b010).
- Registers that have multiple iterations are denoted by {x..y} in their names; where *x* is first register and address, and *y* is the last register and address. For example, REG{0..1} indicates there are two versions of the register at different addresses: REG0 and REG1.

Symbols

This symbol indicates a basic design concept or information considered helpful.

This symbol indicates important configuration information or suggestions.

This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Document Status Information

- Advance – Contains information that is subject to change, and is available once prototypes are released to customers.
- Preliminary – Contains information about a product that is near production-ready, and is revised as required.
- Formal – Contains information about a final, customer-ready product, and is available once the product is released to production.

Revision History

80B8000_MA002_04, Formal, April 2007

This is the current release of the *Tsi568A Serial RapidIO Switch Hardware Manual*. The following information was updated:

- “Power Distribution” on page 60
- “Package Characteristics” on page 25
- “Heatsink Attachment” on page 29

80B8000_MA002_03, Final, February 2007

The following information was updated:

- “Thermal Characteristics” on page 28

80B8000_MA002_02, Formal, December 2006

The following information was added to the document:

- “Line Rate Support” on page 73
- “Power Sequencing” on page 34.
- The $T_{storage}$ minimum value was changed to -55°C (see Table 6 on page 31).
- “Heatsink Requirement and Analysis” on page 29

80B8000_MA002_01, Formal, March 2006

This was the first release of the *Tsi568A Serial RapidIO Switch Hardware Manual*.

Contents

Figures

Tables

1. Signals and Packaging

This chapter describes the packaging (mechanical) features for the Tsi568A. It includes the following information:

- "Pinlist" on page 17
- "Signals" on page 17
- "Package Characteristics" on page 25
- "Thermal Characteristics" on page 28\

1.1 Pinlist

Please refer to the *Tsi568A User Manual* and the Tundra website at www.tundra.com for information on the package pinlist and ballmap.

1.2 Signals

The following conventions are used in the pin description table:

- Signals with the suffix "_p" are the positive half of a differential pair.
- Signals with the suffix "_n" are the negative half of a differential pair.
- Signals with the suffix "_b" are active low.
- DDR signals are Double Data Rate, data is transferred on both edges of the associated clock.

Signals are classified according to the types defined in Table 1 on page 17.

Table 1: Signal Types

Pin Type	Definition
I	Input
O	Output
I/O	Input/Output
OD	Open Drain
SRIO	CML driver/receiver defined by *RapidIO Interconnect Specification (Revision 1.2)*
PU	Pulled Up internal to the Tsi568A
PD	Pulled Down internal to the Tsi568A

Table 1: Signal Types *(Continued)*

Pin Type	Definition
Hyst	Hysteresis
Core Power	Core supply
Core Ground	Ground for core logic
I/O Power	I/O supply

1.2.1 Endian Ordering

This document follows the bit-numbering convention adopted by *RapidIO Interconnect Specification (Revision 1.2)*, where [0:7] is used to represent an 8 bit bus with bit 0 as the most-significant bit.

1.2.2 Signal Groupings

Figure 1 summarizes the Tsi568A signals.

Figure 1: Tsi568A Pinout List

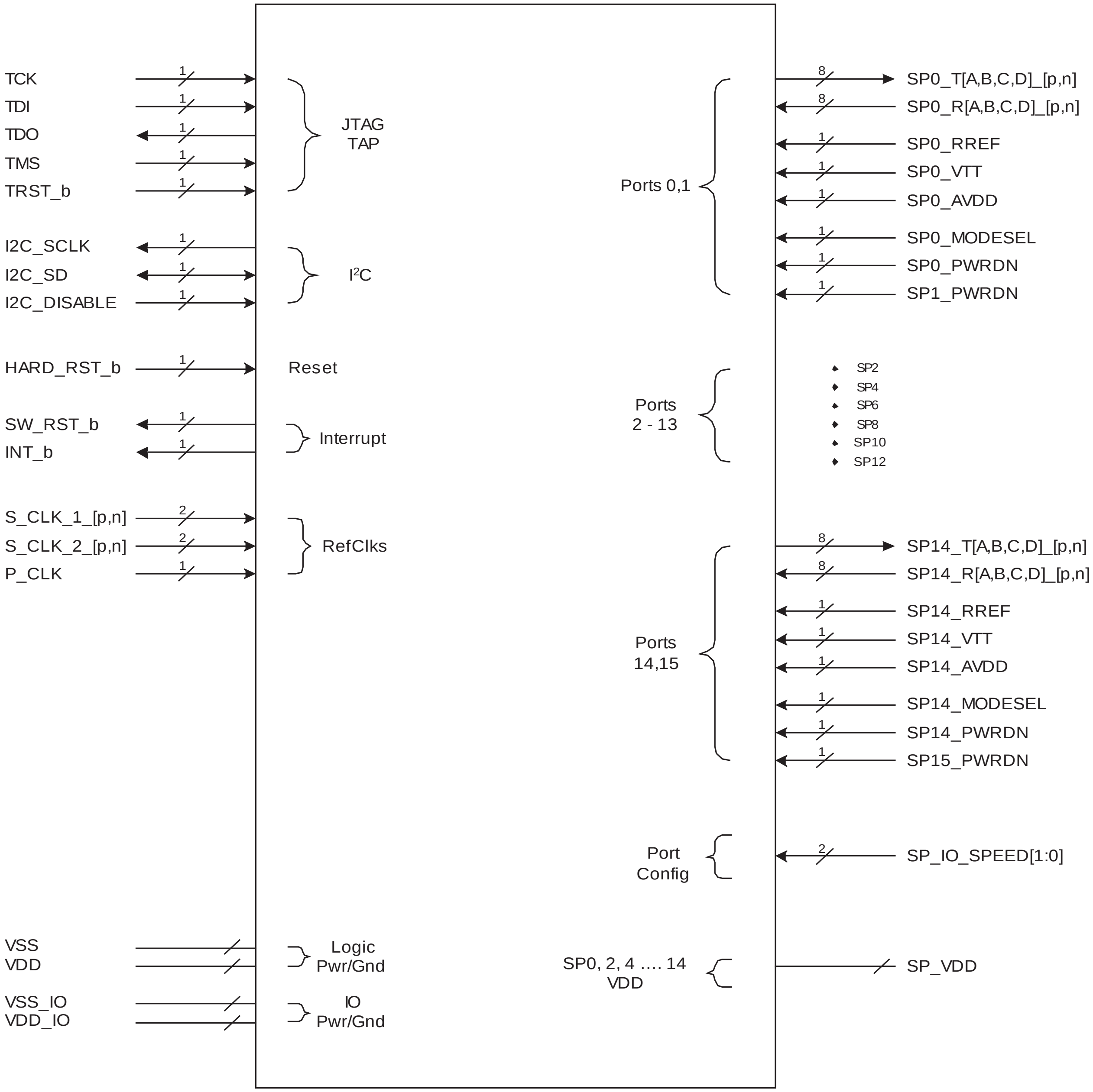


Table 2 describes the Tsi568A signals.

Table 2: Tsi568A Signal Description

Pin Name	Pin Count	Type	Description
PORT n - 1x/4x Mode Serial RapidIO PORT (n+1) - 1x Mode Serial RapidIO where n = 0, 2, 4, 6, 8, 10, 12, 14			
SERIAL PORT n/n+1 TRANSMIT where n = 0, 2, 4, 6, 8, 10, 12, 14			
SP{n}_TA_p	1	O, SRIO	Port n Lane A Differential Non-inverting Transmit Data output (4x mode) Port n Differential Non-inverting Transmit Data output (1x mode)
SP{n}_TA_n	1	O, SRIO	Port n Lane A Differential Inverting Transmit Data output (4x mode) Port n Differential Inverting Transmit Data output (1x mode)
SP{n}_TB_p	1	O, SRIO	Port n Lane B Differential Non-inverting Transmit Data output (4x mode) Port n+1 Differential Non-inverting Transmit Data output (1x mode)
SP{n}_TB_n	1	O, SRIO	Port n Lane B Differential Inverting Transmit Data output (4x mode) Port n+1 Differential Inverting Transmit Data output (1x mode)
SP{n}_TC_p	1	O, SRIO	Port n Lane C Differential Non-inverting Transmit Data output (4x mode)
SP{n}_TC_n	1	O, SRIO	Port n Lane C Differential Inverting Transmit Data output (4x mode)
SP{n}_TD_p	1	O, SRIO	Port n Lane D Differential Non-inverting Transmit Data output (4x mode)
SP{n}_TD_n	1	O, SRIO	Port n Lane D Differential Inverting Transmit Data output (4x mode)
SERIAL PORT n/n+1 RECEIVE where n = 0, 2, 4, 6, 8, 10, 12, 14			
SP{n}_RA_p	1	I, SRIO	Port n Lane A Differential Non-inverting Receive Data input (4x node) Port n Differential Non-inverting Receive Data input (1x mode)
SP{n}_RA_n	1	I, SRIO	Port n Lane A Differential Inverting Receive Data input (4x node) Port n Differential Inverting Receive Data input (1x mode)
SP{n}_RB_p	1	I, SRIO	Port n Lane B Differential Non-inverting Receive Data input (4x mode) Port n+1 Differential Non-inverting Receive Data input (1x mode)
SP{n}_RB_n	1	I, SRIO	Port n Lane B Differential Inverting Receive Data input (4x mode) Port n+1 Differential Inverting Receive Data input (1x mode)
SP{n}_RC_p	1	I, SRIO	Port n Lane C Differential Non-inverting Receive Data input (4x mode)
SP{n}_RC_n	1	I, SRIO	Port n Lane C Differential Inverting Receive Data input (4x mode)
SP{n}_RD_p	1	I, SRIO	Port n Lane D Differential Non-inverting Receive Data input (4x mode)
SP{n}_RD_n	1	I, SRIO	Port n Lane D Differential Inverting Receive Data input (4x mode)
SERIAL PORT n/n+1 CONFIGURATION where n = 0, 2, 4, 6, 8, 10, 12, 14			

Table 2: Tsi568A Signal Description *(Continued)*

Pin Name	Pin Count	Type	Description
SP{n}_RREF	1		Used to connect a 1K +/-1% resistor to SP{n}_AVDD to provide a reference current for the driver and equalization circuits.
SP{n}_MODESEL	1	I/O, CMOS PD	Selects the serial port operating mode for ports n and n+1 0 - Port n operating in 4x mode (Port n+1 not available) 1 - Ports n and n+1 operating in 1x mode Must remain stable for 10 P_CLK cycles after HW_RST_b is de-asserted in order to be sampled correctly. Ignored after reset.
SP{n}_PWRDN	1	I/O, CMOS PU	Port n Transmit and Receive Power Down control This signal controls the state of Port n *and Port n+1* The PWRDN controls the state of all four lanes (A/B/C/D) of SerDes Macro. 0 - Port n Powered Up. Port n+1 controlled by SP{n+1}_PWRDN. 1 - Port n Powered Down. Port n+1 Powered Down. Override SP{n}_PWRDN using PWDN_x1 field in SRIO MAC x Clock Selection Register Output capability of this pin is only used in test mode. Must remain stable for 10 P_CLK cycles after HW_RST_B is de-asserted in order to be sampled correctly. Ignored after reset.
SP{n+1}_PWRDN	1	I/O, CMOS PU	Port n+1 Transmit and Receive Power Down control This signal controls the state of Port n+1. Note that Port n+1 is never used when 4x mode is selected for a Serial Rapid IO MAC, and it must be powered down. 0 - Port n+1 Powered Up 1 - Port n+1 Powered Down Override SP{n+1}_PWRDN using PWDN_x4 field in SRIO MAC x Clock Selection Register. Output capability of this pin is only used in test mode. Must remain stable for 10 P_CLK cycles after HW_RST_B is de-asserted in order to be sampled correctly. Ignored after reset.
SERIAL PORT SPEED SELECT			

Table 2: Tsi568A Signal Description *(Continued)*

Pin Name	Pin Count	Type	Description
SP_IO_SPEED[1]	1	I/O, CMOS, PD	Serial Port Transmit and Receive operating frequency select, bit 1. When combined with SP_IO_SPEED[0], this pin selects the default serial port frequency for all ports. 00 - S_CLK_2 reference divided by 2 01 - S_CLK_2 reference (default) 10 - S_CLK_1 reference 11 - reserved The output data rate per lane is 10 times the selected input clock. Selects the speed at which the ports operates when reset is removed. This could be either due to HARD_RST_b being de-asserted or by the completion of a self-reset. This signal must remain stable for 10 P_CLK cycles after HW_RST_B is de-asserted in order to be sampled correctly. The signal is ignored after reset. The SP_IO_SPEED[1:0] setting is equal to the SCLK_SEL field in the SRIO MAC x Clock Selection Register Output capability of this pin is only used in test mode.
SP_IO_SPEED[0]	1	I/O, CMOS, PU	See SP_IO_SPEED[1]
CLOCK and RESET			
P_CLK	1	I CMOS	This clock is used for the register bus clock. The maximum frequency of this input clock is 100 MHz.
S_CLK_1_p	1	I CML	Differential non-inverting reference clock. The clock is used for following purposes: SerDes reference clock, serial port system clock, ISF clock (equal to half of this clock) and test clock. The clock frequency is defined in the Minimum Clock Frequency Requirements section. The maximum frequency of this input clock is 312.5 MHz. If this clock input is not used, pull this signal up.
S_CLK_1_n	1	I CML	Differential inverting reference clock. The clock is used for following purposes: SerDes reference clock, serial port system clock, ISF clock (equal to half of this clock) and test clock. The clock frequency is defined in the Minimum Clock Frequency Requirements section.The maximum frequency of this input clock is 312.5 MHz. If this clock input is not used, pull this signal down.
S_CLK_2_p	1	I CML	Differential non-inverting reference clock. The clock is used for following purposes: SerDes reference clock, serial port system clock, 125MHz clock (equal to half of this clock) and test clock. The clock frequency is defined in the Minimum Clock Frequency Requirements section. The maximum frequency of this input clock is 250 MHz. If this clock input is not used, pull this signal up.

Table 2: Tsi568A Signal Description *(Continued)*

Pin Name	Pin Count	Type	Description
S_CLK_2_n	1	I CML	Differential inverting reference clock. The clock is used for following purposes: SerDes reference clock, serial port system clock, 125MHz clock (equal to half of this clock) and test clock. The clock frequency is defined in the Minimum Clock Frequency Requirements section.The maximum frequency of this input clock is 250 MHz. If this clock input is not used, pull this signal down.
HARD_RST_b	1	I CMOS, Hyst, PU	Schmidt-triggered hard reset. Asynchronous active low reset for the entire device.
INTERRUPTS			
INT_b	1	O, OD, CMOS	Interrupt signal (open drain output)
SW_RST_b	1	O, OD, CMOS	Software reset (open drain output): This signal is asserted when a RapidIO port receives a valid reset request on a RapidIO link. If self-reset is not selected, this pin remains asserted until the reset request is cleared from the status registers. If self-reset is selected, this pin remains asserted until the self reset is complete. If the Tsi568A is reset from the HARD_RST_b pin, this pin is de-asserted and remains de-asserted after HARD_RST_b is released.
I^2C			
I2C_SCLK	1	O, OD, CMOS, PU	I^2C clock, up to 100 kHz. Although this clock is open drain, the I2C controller does not support multiple bus masters. This clock signal must be connected to the clock of the serial EEPROM on the I2C bus.
I2C_SD	1	I/O, OD, CMOS,PU	I^2C input and output data bus (bidirectional open drain)
I2C_DISABLE	-	I, CMOS, PD	Disable I^2C register loading after reset. When asserted, the Tsi568A will not attempt to load register values from I^2C. 0 - Enable I^2C register loading 1- Disable I^2C register loading
JTAG / TAP CONTROLLER			
TCK	1	I, CMOS, PD	IEEE 1149.1 Test Access Port - Clock Input
TDI	1	I, CMOS, PU	IEEE 1149.1 Test Access Port - Serial Data Input

Table 2: Tsi568A Signal Description *(Continued)*

Pin Name	Pin Count	Type	Description
TDO	1	O, CMOS	IEEE 1149.1 Test Access Port - Serial Data Output
TMS	1	I, CMOS, PU	IEEE 1149.1 Test Access Port - Test Mode Select
TRST_b	1	I, CMOS, PU	IEEE 1149.1 Test Access Port - TAP Reset Input This input should asserted during a power-up reset.
POWER SUPPLIES			
PORT n/n+1 n = 0, 2, 4, 6, 8, 10, 12, 14			
SP{n}_AVDD	1	-	Port n & n+1: 1.2V supply for bias generator circuitry. This is required to be a low-noise supply.
SP{n}_VTT	1	-	Port n & n+1: Driver termination voltage - common to all lanes
COMMON SUPPLY			
VDD_IO	15	-	Common 3.3V supply for CMOS I/O
VSS_IO	12	-	Common ground supply for I/Os
VSS	285	-	Common ground supply for digital logic
VDD	50	-	Common 1.2V supply for digital logic
SP_VDD	114	-	1.2V supply for CDR, Tx/Rx, and digital logic for all Serial RapidIO ports
Total Power and Ground	474		

1.3 Package Characteristics

Tsi568A’s package characteristics are summarized in the following table. Figure 2 and Figure 3 illustrates the Top and Side views of the Tsi568A package. Figure 4 presents the Bottom view of the device.

Table 3: Package Characteristics

Feature	Description
Package Type	Flip-Chip Ball Grid Array (FCBGA)
Package Body Size	27x27 mm
JEDEC Specification	95-1 Section 14
Pitch	1.00 mm
Ball pad size	500 um
Soldermask opening	400 um
Moisture Sensitivity Level	4

Figure 2: Package Diagram — Top view

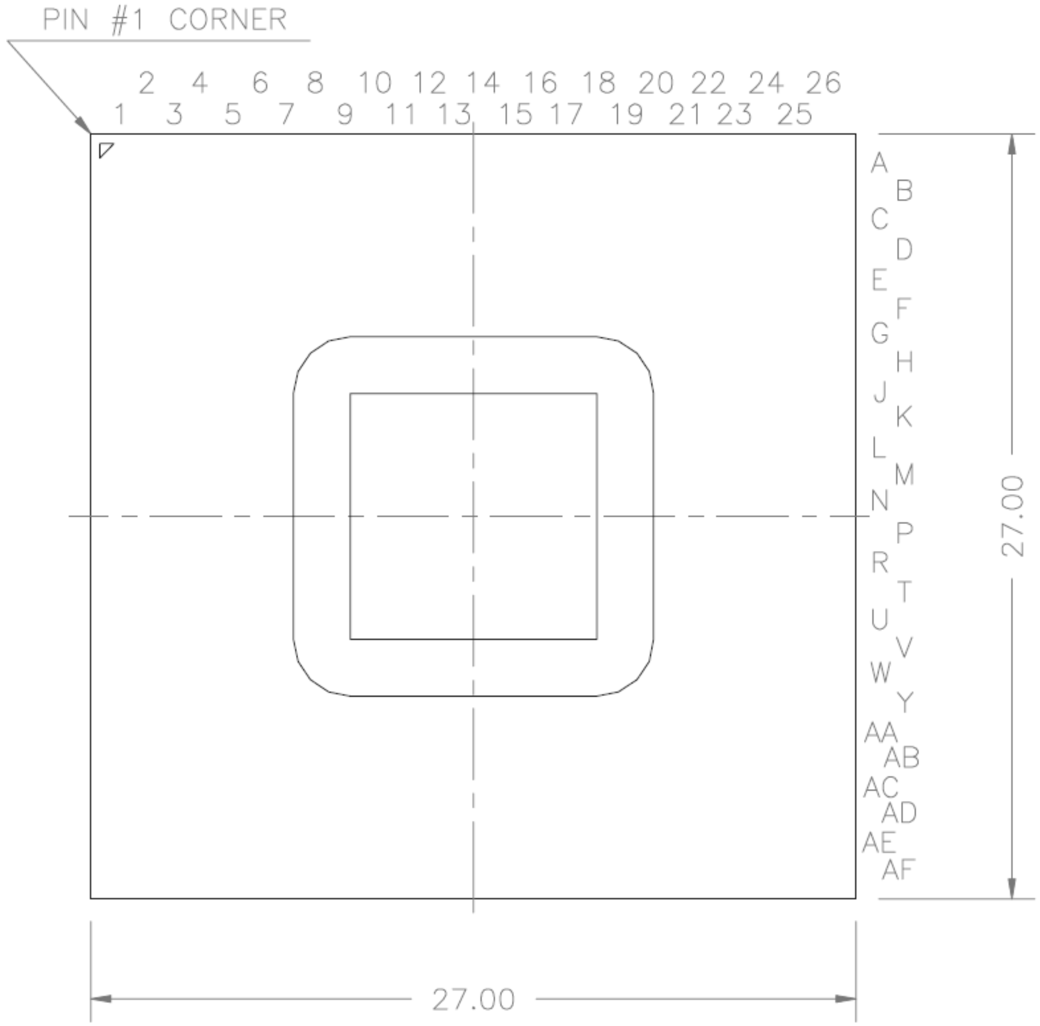


Figure 3: Package Diagram — Side View

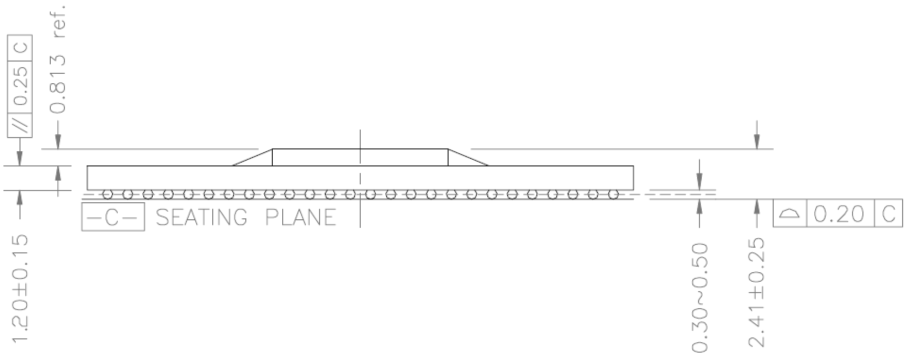
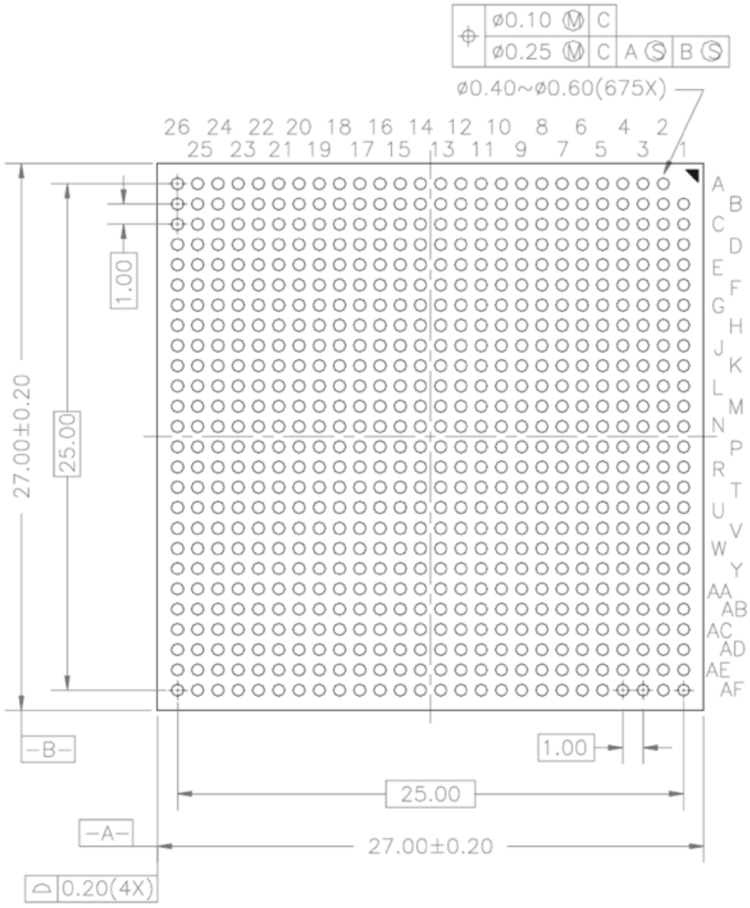


Figure 4: Package Diagram — Bottom View



1.4 Thermal Characteristics

Heat generated by the packaged IC has to be removed from the package to ensure that the IC is maintained within its functional and maximum design temperature limits. If heat buildup becomes excessive, the IC temperature may exceed the temperature limits. A consequence of this is that the IC may fail to meet the performance specifications and the reliability objectives may be affected.

Failure mechanisms and failure rate of a device have an exponential dependence of the IC operating temperatures. Thus, the control of the package temperature, and by extension the Junction Temperature, is essential to ensure product reliability. The Tsi568A is specified safe for operation when the Junction Temperature is within the recommended limits.

Table 4 shows the simulated Theta jb and Theta jc thermal characteristics of the Tsi568A FCBGA package.

Table 4: Thermal Characteristics of Tsi568A

Interface	Result
Theta jb (junction to board)	11.8 °C/watt
Theta jc (junction to case)	0.09 °C/watt

1.4.1 Junction-to-Ambient Thermal Characteristics (Theta ja)

Table 5 shows the simulated Theta ja thermal characteristic of the Tsi568A FCBGA package.The results in Table 5 are based on a JEDEC Thermal Test Board configuration (JESD51-9) and do not factor in system level characteristics. As such, these values are for reference only.

The Theta ja thermal resistance characteristics of a package depend on multiple system level variables.

Table 5: Simulated Junction to Ambient Characteristics

Package	Theta ja at specified airflow (no Heat Sink)		
	0 m/s	1 m/s	2 m/s
Tsi568A FCBGA	14.3 C/watt	13.5 °C/watt	12.8 °C/watt

1.4.1.1 System-level Characteristics

In an application, the following system-level characteristics and environmental issues must be taken into account:

- Package mounting (vertical / horizontal)
- System airflow conditions (laminar / turbulent)
- Heat sink design and thermal characteristics (see "Heatsink Requirement and Analysis" on page 29)
- Heat sink attachment method (see "Heatsink Requirement and Analysis" on page 29)
- PWB size, layer count and conductor thickness
- Influence of the heat dissipating components assembled on the PWB (neighboring effects)

Example on Thermal Data Usage

Based on the Theta$_{JA}$ data and specified conditions, the following formula can be used to derive the junction temperature (Tj) of the Tsi568A with a 0m/s airflow:

- $Tj = \theta_{JA} * P + Tamb$

  Where: Tj is Junction Temperature, P is the Power consumption, Tamb is the Ambient Temperature

Assuming a power consumption (P) of 3.5 W and an ambient temperature (Tamb) of 70°C, the resulting junction temperature (Tj) would be 121.1°C.

1.4.2 Heatsink Requirement and Analysis

The Tsi568A is packaged in a Flip-Chip Ball Grid Array (FCBGA). With this package technology, the silicon die is exposed and serves as the interface between package and heatsink. Where a heatsink is required to maintain junction temperatures at or below specified maximum values, it is important that attachment techniques and thermal requirements be critically analyzed to ensure reliability of this interface. Factors to be considered include: surface preparations, selection of thermal interface materials, curing process, shock and vibration requirements, and thermal expansion coefficients, among others. Each design should be individually analyzed to ensure that a reliable thermal solution is achieved.

1.4.2.1 Heatsink Attachment

Both mechanical and adhesive techniques are available for heatsink attachment.

> ⚠ Both mechanical and adhesive techniques are available for heatsink attachment. Tundra makes no recommendations as to the reliability or effectiveness of either approach. The designer must critically analyze heatsink requirements, selection criteria, and attachment techniques.

For heatsink attachment methods that induce a compressive load to the FCBGA package, the maximum force that can be applied to the package should be limited to 5 gm / BGA ball (provided that the board is supported to prevent any flexing or bowing). The maximum force for the Tsi568A package is 3.38 Kg.

2. Electrical Characteristics

This chapter provides the electrical characteristics for the Tsi568A. It includes the following information:

- "Absolute Maximum Ratings" on page 31
- "Electrical Characteristics and Operating Conditions" on page 32
- "AC Timing Waveforms" on page 43

2.1 Absolute Maximum Ratings

Operating the device beyond the operating conditions is not recommended. Stressing the Tsi568A beyond the Absolute Maximum Rating can cause permanent damage.

Table 6 lists the absolute maximum ratings.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$T_{storage}$	Storage Temperature	-55	125	°C
T_{case} (T_j)	Case Temperature under Bias	-40	120	°C
V_{DD_33}	3.3V DC Supply Voltage	-0.5	4.6	V
V_{DD}, SP_V_{DD}	1.2V DC Supply Voltage	-0.5	1.7	V
SP{n}_AV_{DD}	1.2V Analogue Supply voltage	-0.5	1.7	V
SP{n}_V_{TT}	Driver Termination Voltage	-0.5	2.5	V
$V_{I\_SP\{n\}-R\{A-D\}\_\{p,n\}}$	SERDES Port CML Receiver Input Voltage	-0.3	3	V
$V_{O\_SP\{n\}-T\{A-D\}\_\{p,n\}}$	SERDES Port CML Transmitter Output Voltage	-0.3	3	V
V_{I_LVTTL}	LVTTL Input Voltage	-0.5	V_{DD_33} +0.5	V
V_{O_LVTTL}	LVTTL Output or I/O Voltage	-0.5	V_{DD_33} +0.5	V

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{ESD_HBM}	Maximum ESD Voltage Discharge Tolerance for Human Body Model (HBM). [Test Conditions per JEDEC standard - JESD22-A114-B]		1000	V
V_{ESD_CDM}	Maximum ESD Voltage Discharge Tolerance for Charged Device Model (CDM). Test Conditions per JEDEC standard - JESD22-C101-A		300	V

2.2 Electrical Characteristics and Operating Conditions

Table 7 lists the recommended operating conditions and electrical characteristics for the power supply pins of the Tsi568A.

Table 7: Power Supply Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_j	Junction temperature	-40		120	°C	
V_{DD_33}	3.3V DC Supply Voltage	2.97		3.63	V	Maximum AC voltage ripple must be less than 2.5% measured at device pin
SP_VDD, VDD, SP{n}_AVDD	1.2V DC Supply Voltage	1.14		1.29	V	Maximum AC voltage ripple must be less than 2.5% measured at device pin
SP{n}_VTT	1.2V Driver Termination Voltage	1.14		1.26	V	Maximum AC voltage ripple must be less than 2.5% measured at device pin
	1.5V Driver Termination Voltage	1.42		1.58	V	Maximum AC voltage ripple must be less than 2.5% measured at device pin
	1.8V Driver Termination Voltage	1.71		1.89	V	Maximum AC voltage ripple must be less than 2.5% measured at device pin
I_{VDD}	Core Supply Current			2420	mA	I_{VDD}(in mA) = (I_VDDC1 x N1)+(I_VDDC4 x N4), where I_VDDC1 is the active x1 port current, N1 is the number of active x1 ports, I_VDDC4 is the active x4 port current, and N4 is the number of x4 ports active. I_VDDC1(in mA) = 0.0361 x F + 38.4, where F is the SERDES port frequency of operation in MHz I_VDDC4(in mA) = 0.062 x F + 72.7, where F is the SERDES port frequency of operation in MHz

Table 7: Power Supply Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{VDD_33}	3.3V IO Supply Current			10	mA	
I_{SP_VDD}	SERDES Digital Supply Current			2600	mA	I_{SP_VDD}(in mA)=0.026xCxNxF, where C is the number of active SERDES channels, N is the number of active SERDES ports, and F is the SERDES port frequency of operation in MHz
I_{SP_AVDD}	SERDES Analog Supply Current			80	mA	I_{SP_AVDD}(in mA)=10xN, where N is the number of SERDES Ports active Brent to get Cpk of 2 number
I_{SP_VTT}	SERDES Termination Supply Current			1140	mA	I_{SP_VTT}=Inom x RIdr/Inom x C x N, where Ridr/Inom is the Idr to Inom ratio, C is the number of active SERDES channels, and N is the number of SERDES Ports with termination active.
PD_Core	Core Power Dissipation			3050	mW	PD_Core(in mW)= VDD x Rvdd/vdd_max x I_VDDC, where Rvdd/vdd_max is the ratio of VDD to VDD_MAX, and I_VDDC is the core current calculated for the Core Supply Current Parameter
PD_IO	IO Power Dissipation			5570	mW	PD_IO(in mW)= (SP_VDD x Rsp_vdd/sp_vddmax x ISP_VDD) + (VDD33 x Rvdd33/vdd33_max x I_VDD33) + (SP_AVDD x Rsp_avdd/sp_avddmax x ISP_AVDD) + (SP_VTT x ISP_VTT), where Rxxxx/xxxx is the ratio of the supply voltage to the supply voltage maximum, ISP_VDD is the SERDES Digital Supply Current parameter, I_VDD33 is the 3.3V IO Supply Current parameter, ISP_AVDD is the SERDES Analog Supply Current parameter, and ISP_VTT is the SERDES Termination Supply Current parameter
PD_standby	Standby Power Dissipation			256	mW	PD_standby (in mW) = 32 x N, where N is the number of disabled ports. The standby power of each disabled port must be included in the total power dissipation calculation. The value shown here is for 8 ports in standby.
PD	Total Power Dissipation			7890	mW	This parameter is configuration dependent and can be calculated from the PD_Core, PD_IO, and PD_standby parameters for a given configuration. The number shown here is for the Maximum power configuration of 8 x4 ports operating at 3.125Gb/s

2.2.1 Power Sequencing

The recommended power sequence for the Tsi568A is in the following order:

- VDD (1.2V), SP_VDD, and SP{n}_VDDA (1.2V) power-up together
- SP{n}_VTT
- VDD_IO (3.3V)

It is recommended that there not be more than 50ms between ramping of the 1.2V and 3.3V supplies. The power supply ramp rates must be kept between 10V/sec and 1x10^6V/sec to minimize power current spikes during power up. For applications requiring Power sequencing that is different than the recommended sequence, please contact Tundra Applications Engineering.

2.2.1.1 Power-down

Power down is the reverse sequence of power up:

- VDD_IO (3.3V)
- SP{n}_VTT
- VDD (1.2V), SP_VDD, and SP{n}_AVDD (1.2V) power-down at the same time.

This section describes the DC signal characteristics for the Tsi568A.

2.2.2 LVTTL I/O and Open Drain Electrical Characteristics

Table 8 lists the Electrical characteristics for the LVTTL Interface pins on the Tsi568A

Table 8: LVTTL I/O and Open Drain Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	LVTTL Input Low Voltage			0.8	V	All inputs and I/Os of LVTTL type
V_{IH}	LVTTL Input High Voltage	2.0			V	All inputs and I/Os of LVTTL type
I_{IL}	LVTTL Input Low Current			10	uA	All non-PU inputs and I/Os of LVTTL type
I_{IH}	LVTTL Input High Current			-10	uA	All non-PD inputs and I/Os of LVTTL type
I_{OZL_PU}, I_{IL_PU}	LVTTL Input Low/ Output Tristate Current	5		100	uA	All PU inputs and I/Os of LVTTL type for voltages from 0 to V_{DD_33} on the pin.
I_{OZH_PD}, I_{IH_PD}	LVTTL Input High/ Output Tristate Current	-5		-100	uA	All PD inputs and I/Os of LVTTL type for voltages from 0 to V_{DD_33} on the pin.
V_{OL}	LVTTL Output Low Voltage			0.4	V	I_{OL}=2mA for INT_b, SW_RST_b, and TDO pins I_{OL}=8mA for I2C_CLK and I2C_SD pins

Table 8: LVTTL I/O and Open Drain Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{OH}	LVTTL Output Low Voltage	V_{DD_33} -0.5			V	I_{OH}=2mA for INT_b, SW_RST_b, and TDO pins
V_{Hyst}	LVTTL Input Hysteresis Voltage		200		mV	All Hyst inputs and I/Os of LVTTL type
C_{Pad}	LVTTL Pad Capacitance			10	pF	All pads of LVTTL type
T_{cfgpS}	Configuration Pin Setup Time	100			ns	For all Configuration pins (except SP{n}_MODESEL with respect to HARD_RST_b rising edge (See Figure 6)
T_{cfgpH}	Configuration Pin Hold Time	100			ns	For all Configuration pins (except SP{n}_MODESEL) with respect to HARD_RST_b rising edge (See Figure 6
$T_{sp\_modeselS}$	SP{n}_MODESEL Setup Time	5			ns	with respect to rising edge of P_CLK. SP{n}_MODESEL pins are sampled on every rising edge of P_CLK. (See Figure 6)
$T_{sp\_modeseH}$	SP{n}_MODESEL Hold Time	5			ns	with respect to rising edge of P_CLK. SP{n}_MODESEL pins are sampled on every rising edge of P_CLK. (See Figure 6)
T_{ISOV1}	INT_b/SW_RST_b Output Valid Delay from rising edge of P_CLK			15	ns	Measured between 50% points on both signals. Output Valid delay is guaranteed by design.(See Figure 7)
T_{ISOF1}	INT_b/SW_RST_b Output Float Delay from rising edge of P_CLK			15	ns	A float condition occurs when the output current becomes less than I_{LO}, where I_{LO} is 2 x I_{OZ}. Float delay guaranteed by design.(See Figure 7)
F_{in_PCLK}	P_CLK Input Clock Frequency Range	100 - 100 ppm		100 + 100 ppm	MHz	
$F_{in\_PCLK\_DC}$	P_CLK Input Clock Duty Cycle	40	50	60	%	See Figure 8
J_{PCLK}	P_CLK Input Jitter			300	ps	
T_{R_PCLK}, T_{F_PCLK}	P_CLK Input Rise/Fall Time			2.5	ns	
Rpu	Internal pull-up resistor	82	170	260	KOhm	at Vol=0.8 V
Rpd	Internal pull-down resistor	28	40	54	KOhm	at Vih=2.0 V

2.2.3 Serial Interface Electrical Characteristics

Table 9 lists the Electrical characteristics for the Serial Receiver Interface pins on the Tsi568A

Table 9: Serial Interface Receiver Input Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Z_{DI}	RX Differential Input impedance	80		120	Ohm	
V_{DIFFI}	RX Differential Input Voltage	170		2000	mV	
L_{CR}	RX Common Mode Return Loss			6	dB	Over a range 100MHz to 0.8* Baud Frequency
L_{DR}	RX Differential Return Loss			10	dB	Over a range 100MHz to 0.8* Baud Frequency
V_{LOS}	RX Loss of Input Differential Level	85			mV	Port Receiver Input level below which Low Signal input is detected
J_{RT1250}	RX Total Jitter Tolerance (peak-to-peak)			0.71	UIpp	For 1.25Gb/s +/- 100ppm @BER=10e-12
J_{RR1250}	RX Deterministic + Random Jitter component			0.61	UIpp	For 1.25Gb/s +/- 100ppm @BER=10e-12
J_{RD1250}	RX Deterministic Jitter component			0.45	UIpp	For 1.25Gb/s +/- 100ppm
J_{RT2500}	RX Total Jitter (peak-to-peak)			0.67	UIpp	For 2.5Gb/s +/- 100ppm @BER=10e-12
J_{RR2500}	RX Deterministic + Random Jitter component			0.57	UIpp	For 2.5Gb/s +/- 100ppm @BER=10e-12
J_{RD2500}	RX Deterministic Jitter component			0.42	UIpp	For 2.5Gb/s +/- 100ppm
J_{RT3125}	RX Total Jitter (peak-to-peak)			0.65	UIpp	For 3.125Gb/s +/- 100ppm @BER=10e-12
J_{RR3125}	RX Deterministic + Random Jitter component			0.55	UIpp	For 3.125Gb/s +/- 100ppm @BER=10e-12
J_{RD3125}	RX Deterministic Jitter component			0.41	UIpp	For 3.125Gb/s+/- 100ppm
$T_{RX\_ch\_skew}$	RX Channel to Channel Skew Tolerance			24	ns	Between channels in a given x4 port
$R_{TR,}R_{TF}$	RX Input Rise/Fall times			160	ps	between 20% and 80% levels

Table 10 lists the Electrical characteristics for the Serial Transmitter Interface pins on the Tsi568A

Table 10: Serial Interface Transmitter Output Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Z_{SEO}	TX Single-Ended Output impedance	40	50	60	Ohm	
Z_{DO}	TX Differential Output Impedance	80	100	120	Ohm	
V_{SW}	TX Output Voltage Swing (Single-ended)	350		750	mVp-p	V_{SW} (in mV) = Z_{SEO}/2 x Inom x RIdr/Inom, where Ridr/Inom is the Idr to Inom ratio.
V_{DIFFO}	TX Differential Output Voltage Amplitude	2 x VSW_min		2 x VSW_max	mVp-p	P
V_{OL}	TX Output Low-level Voltage		V_{TT} -(1.5 x Vsw)		V	
V_{OH}	TX Output High-level Voltage		V_{TT} -(0.5 x Vsw)		V	
V_{TCM}	TX common-mode Voltage		V_{TT} - Vsw		V	
L_{DR1}	TX Differential Return Loss			-10	dB	For (Baud Frequency)/10<Freq(f)<625MHz and
L_{DR2}	TX Differential Return Loss			-10 + 10log(f/625MHz)	dB	For 625MHz<=Freq(f)<= Baud Frequency
J_{TT1250}	TX Total Jitter (peak-to-peak)			0.24	UIpp	For 1.25Gb/s +/- 100ppm @BER=10e-12
J_{TD1250}	TX Deterministic Jitter component			0.1	UIpp	For 1.25Gb/s +/- 100ppm
J_{TT2500}	TX Total Jitter (peak-to-peak)			0.28	UIpp	For 2.5Gb/s +/- 100ppm @BER=10e-12
J_{TD2500}	TX Deterministic Jitter component			0.13	UIpp	For 2.5Gb/s+/- 100ppm
J_{TT3125}	TX Total Jitter (peak-to-peak)			0.35	UIpp	For 3.125Gb/s +/- 100ppm @BER=10e-12
J_{TD3125}	TX Deterministic Jitter component			0.16	UIpp	For 3.125Gb/s+/- 100ppm

Table 10: Serial Interface Transmitter Output Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
T_{TX_skew}	TX Differential signal skew			15	ps	Skew between _p and _n signals on a give Serial channel
$T_{TX\_ch\_skew}$	TX Channel to Channel Skew Tolerance			2	UI	Between channels in a given x4 port
$T_{TR,}T_{TF}$	TX Input Rise/Fall times	80		110	ps	between 20% and 80% levels

2.2.4 Serial Reference Clock Input Electrical Characteristics

Table 11 lists the Electrical characteristics for the Serial Reference clock input pins on the Tsi568A..

Table 11: Serial Reference Clock Input Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CM}	CML Input Common Mode Range	0.6	0.65	0.7	V	
Vsw	CML Input voltage swing	400		800	mV	
V_{DIFF}	CML Differential Input Voltage	800		1600	mV	
UI	Unit Interval	320		800	ps	Unit Interval = 1/F, where F is the Serial port frequency of operation in Hz
Fin_range	Input Clock Frequency Range	125		312.5	MHz	
Fin_ppm	Input Clock Frequency stability requirment			100	ppm	
Fin_DC	Input Clock Duty Cycle	40	50	60	%	
T_{skew}	Input Clock Skew			0.05	RCUI	Between _p and _n inputs. RCUI=Reference Clock Unit Interval
T_{R_SCLK}, T_{F_SCLK}	S_CLK{p,n} Input Rise/Fall Time			0.25	RCUI	RCUI=Reference Clock Unit Interval
JCLK-REF	Input jitter (peak-to-peak)			0.1	UI	UI is a bit time interval
R_{DIFF}	Internal Termination			110	ohm	Documented in Tsi568A *Device Errata and Design Notes* available at www.tundra.com.

2.2.5 Serial Interface Capability and Implementation

The configuration settings for DRV_STRENGTH and DTX give Tsi568A Serial Interface the flexibility to configure Transmitter Output Voltage Amplitudes to optimize both power and Serial link performance. It is possible to select combinations of these setting that allow the Transmitter to operate outside of the RapidIO specified limits. Care must be used to select appropriate values for both DRV_STRENGTH and DTX to match the Serial link performance requirements and meet the limits defined for the Tsi568. his is also true for the DEQ settings which are covered in the SRIO MAC x SERDES configuration registers.

The SERDES has been tested to meet the RapidIO specification, however operation beyond this range is possible.

The Serial Rapid IO specification is defined by the RapidIO Interconnect Spec, Part VI, Chapter 8, Rev 1.2. Table 12 lists the amplitudes as stated in the RapidIO specifications as a reference.

Table 12: RapidIO Specification Requirements

Ranges	TX Amplitude limits		RX Amplitude limits	
	Min mVpp	Max mVpp	Min mVpp	Max mVpp
Short Range	500	1000	200	1600
Long Range	800	1600	200	1600

The Tsi568A uses the DRV_STRENGTH and DTX bits in each port SRIO MAC x SERDES Configuration registers to control the drive current for each port. All four lanes are set to the same drive currents.

Table 13 shows the programming options for DRV_STRENGTH and drive currents outputs from the programming options.

Table 13: Drive Current Register Setting

DRV_STRENGTH	Inom mA
0 1	10
0 0	20
1 0	28
1 1	Reserved

Table 14 Shows the Idr/Inom Ratio options as a function of the DTX[3:0] selection codes. ..

Table 14: Idr/Inom Ratios vs. DTX[3:0]Swing into Termination

DTX[3:0]	Idr/Inom Ratio	DTX[3:0]	Idr/Inom Ratio
0000	1.00	1000	0.60
0001	1.05	1001	0.65
0010	1.10	1010	0.70
0011	1.15	1011	0.75
0100	1.20	1100	0.80
0101	1.25	1101	0.85
0110	1.30	1110	0.90
0111	1.35	1111	0.95

The single-ended voltage swing for the Serial Transmitter Output (V_{SW}) is determined by the following equation:

(Section 2.2.5-eq1) **V_{SW} (in mV) = $Z_{SEO}/2$ x Inom x RIdr/Inom**, where RIdr/Inom is the Idr to Inom ratio

There are possible combinations of DRV_STRENGTH and DTX that will violate allowable output swing limits. Allowable Output swing amplitudes are limited by the V_{TT} Range used in the system.

Table 15 shows the output swing limits as a function of V_{TT}.

⚠ For proper performance it is required that the Inom and RIdr/Inom parameters be selected such that VSW calculated using equation Section 2.2.5-eq1 meet the requirement specified in Table 15.

Table 15: V_{TT} to Output Swing Limits

V_{TT}	Maximum VSW
1.2	350mV
1.5	500mV
1.8	750mV

2.2.6 I^{2}C Interface AC Specifications

The DC characteristics of the I^{2}C Interface are defined in Table 8 on page 34. Table 16 lists the AC specifications for Tsi568A’s I^{2}C Interface (see notes below).

Table 16: AC Specifications for I^{2}C Interface

Symbol	Parameter	Min	Max	Units	Notes
F_{SCL}	SD_I2C_CLK/I2C_SCLK Clock Frequency	0	100	kHz	10uS
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7	-	µs	1
T_{LOW}	SD_I2C_CLK/I2C_SCLK Clock Low Time	4.7	-	µs	1
T_{HIGH}	SD_I2C_CLK/I2C_SCLK Clock High Time	4	-	µs	1
T_{HDSTA}	Hold Time (repeated) START condition	4	-	µs	1,2
T_{SUSTA}	Setup Time for a Repeated START condition	4.7	-	µs	1
T_{HDDAT}	Data Hold Time	0	3.45	µs	1
T_{SUDAT}	Data Setup Time	250	-	ns	1
T_{SR}	SD_I2C_CLK, SD_I2C_SDA, I2C_SCLK, and I2C_SDA Rise Time	-	1000	ns	1
T_{SF}	SD_I2C_CLK, SD_I2C_SDA, I2C_SCLK, and I2C_SDA Fall Time	-	300	ns	1
T^{SUSTO}	Setup Time for STOP Condition	4	-	µs	1

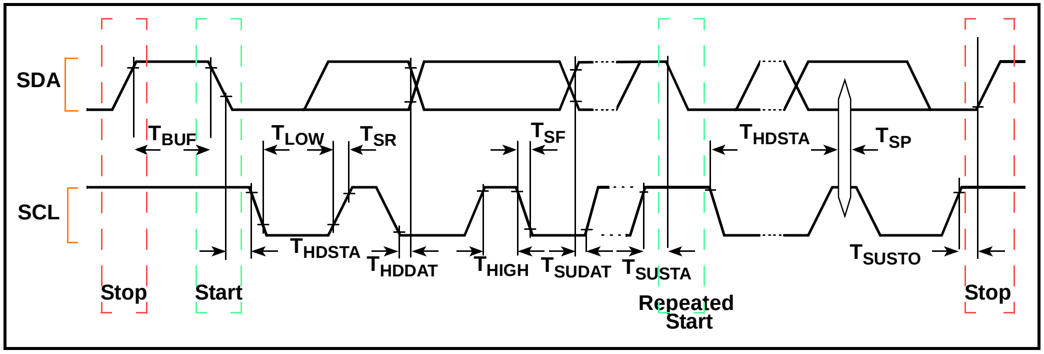
Notes:

1. See Figure 5, I^{2}C Interface Signal Timings

2. After this period, the first clock pulse is generated

Figure 5 shows I^{2}C interface signal timings

Figure 5: I^{2}C Interface Signal Timings



2.2.7 Boundary Scan Interface AC Specifications

Table 17 lists the signal timings for the Boundary Scan Interface for Tsi568A.

Table 17: Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	TCK Frequency	0	10	MHz	-
T_{BSCH}	TCK High Time	50	-	ns	Measured at 1.5V, 1
T_{BSCL}	TCK Low Time	50	-	ns	Measured at 1.5V, 1
T_{BSCR}	TCK Rise Time	-	25	ns	0.8V to 2.0V, 1
T_{BSCF}	TCK Fall Time	-	25	ns	2.0V to 0.8V, 1
T_{SIS1}	Input Setup to TCK	10	-	ns	2
T_{BSIH1}	Input Hold from TCK	10	-	ns	2
T_{BSOV1}	TDO Output Valid Delay from falling edge of TCK.	-	15	ns	1
T_{OF1}	TDO Output Float Delay from falling edge of TCK	-	15	ns	3, 4

Notes:

1. Outputs precharged to V_{DD}.

2. See Figure 7, “Output Timing Measurement Waveforms”.

3. See Figure 6, “Input Timing Measurement Waveforms”.

4. A float condition occurs when the output current becomes less than I_{LO}, where I_{LO} is 2 x I_{OZ}, the Output Tri-state DC current. Float delay guaranteed by design. See Figure 7, “Output Timing Measurement Waveforms”.

2.3 AC Timing Waveforms

This section shows the AC timing waveforms for timing specifications for the Tsi568A.

2.3.1 LVTLL I/O pins

Figure 6 shows the input timing relationships for all LVTTL input signals to the corresponding clock input. The waveform is generalized for both input and clk naming. The parameter TIS represents the setup time and the TIH parameter represents the hold time.

Figure 6: Input Timing Measurement Waveforms.

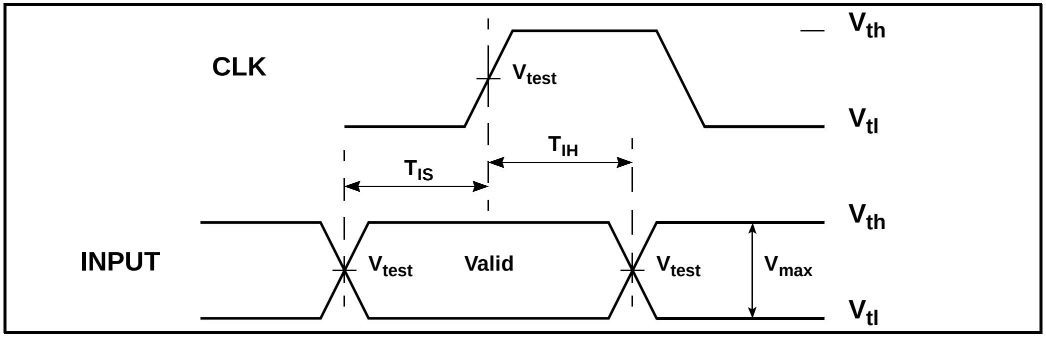


Figure 7 shows the generalized output timing relationships for all LVTTL I/O pins. The TOV parameter represents the Output Valid time or propagation delay of a given output signal with respect to the corresponding clock input.

Figure 7: Output Timing Measurement Waveforms

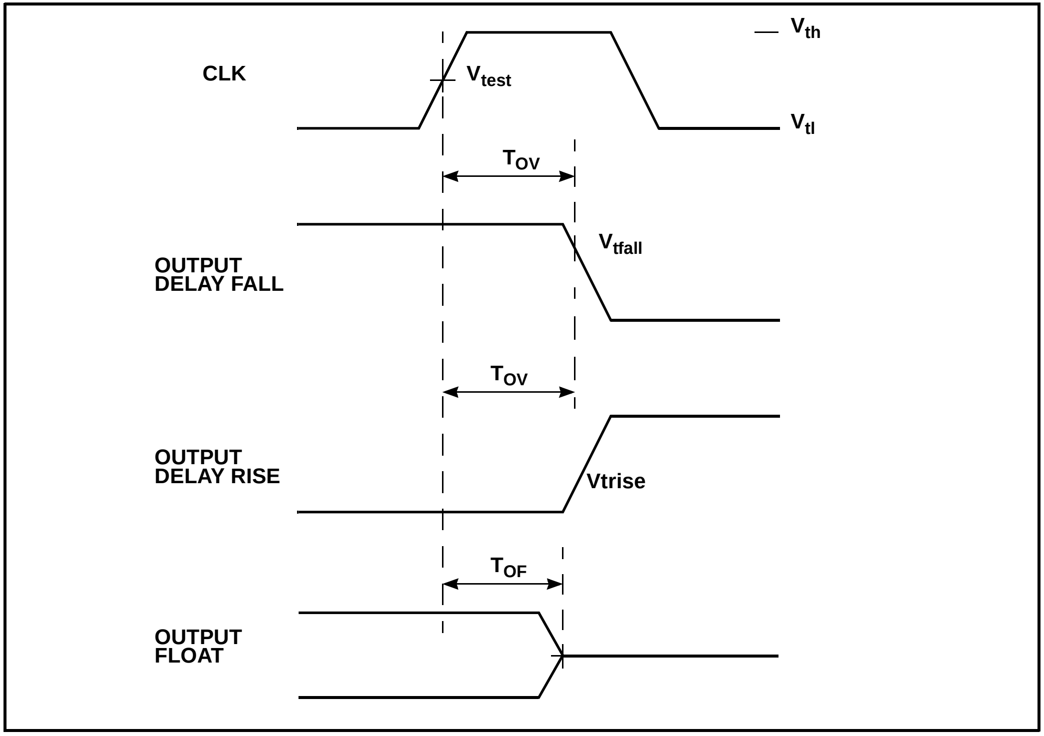
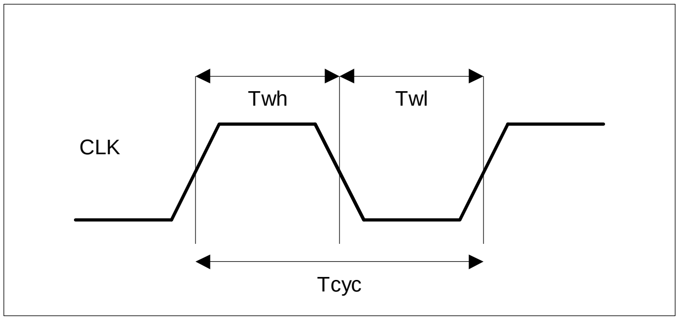


Figure 8 shows the relationship for the CLK duty cycle. The duty cycle by is defined as Twh/Tcyc and Twl/Tcyc, where Twh/Tcyc + Twl/Tcyc = 100%

Figure 8: Duty Cycle Definition Waveforms



2.3.2 Serial Interface Pins

Figure 9 shows the important voltage levels and timing relationships for the Serial Interface Transmitter and Receiver pins.

Figure 9: Serial Interface Transmitter and Receiver signal waveforms

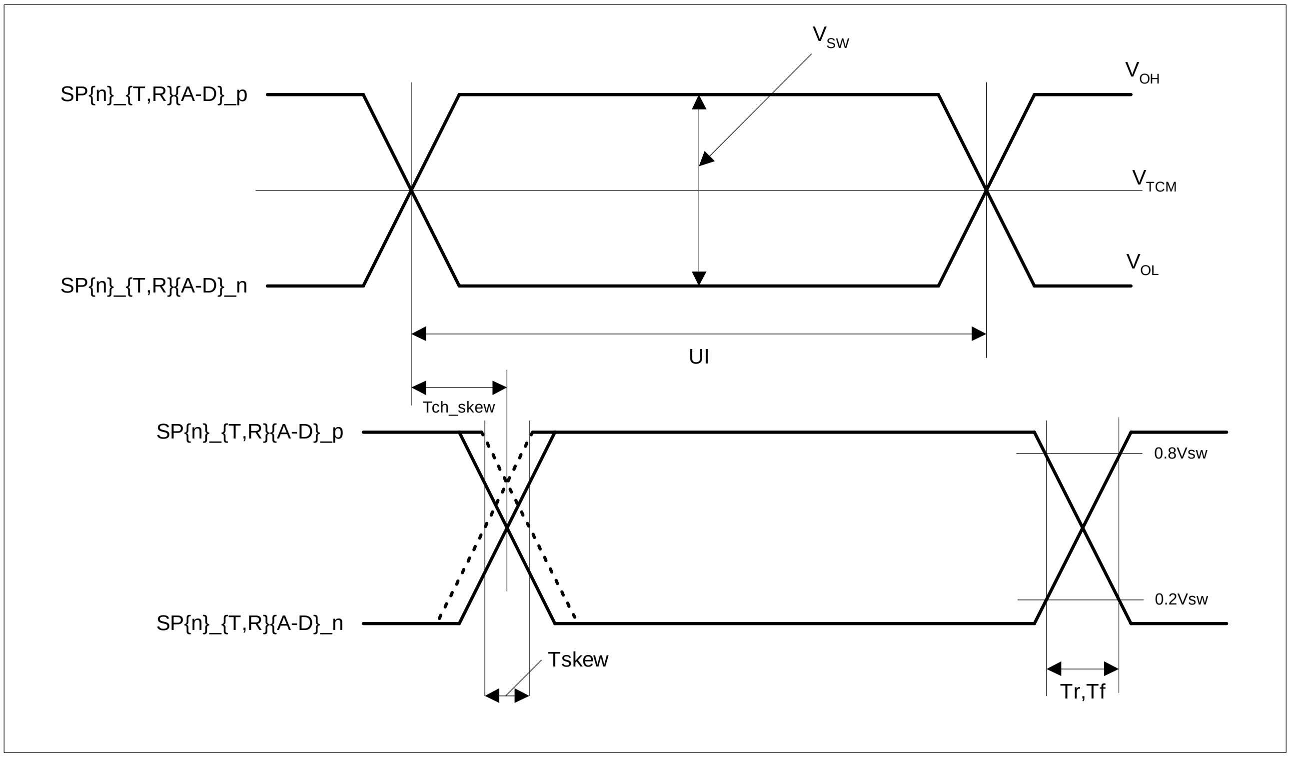
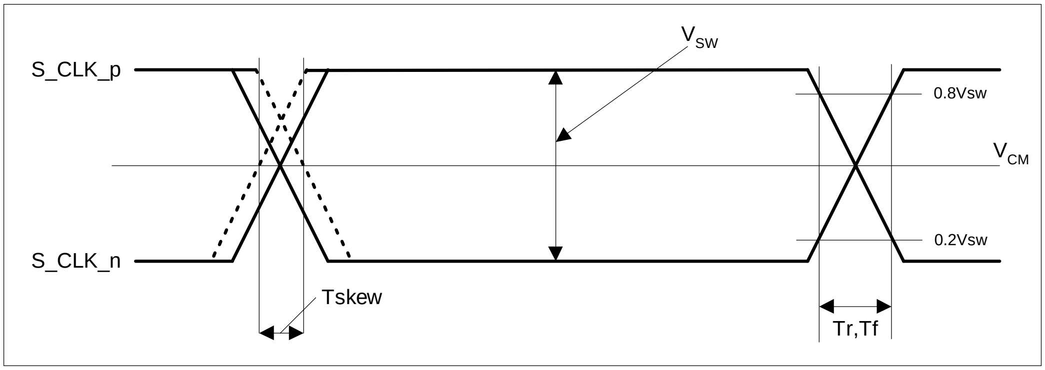


Figure 10 shows the important voltage levels and timing relationships for the Serial Reference Clock Inputs.

Figure 10: Serial Reference Clock Waveforms



3. Layout Guidelines

This chapter describes the layout guidelines for the Tsi568A. It includes the following information:

3.1 Overview

The successful implementation of a Tsi568A in a board design is dependent on properly routing the Serial RapidIO signals and maintaining good signal integrity with a resultant low bit error rate. The sections that follow contain information for the user on principals that will maximize the signal quality of the links.

Since every situation is different, Tundra urges the designer to model and simulate their board layout and verify that the layout topologies chosen will provide the performance required of the product.

3.2 Impedance Requirements

The impedance requirements of the Serial RapidIO interface are:

- 100 ohms differential
- 50 ohms single-ended

3.3 Tracking Topologies

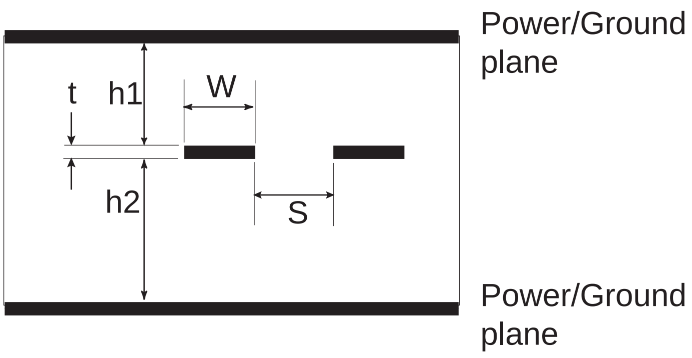
The tracking topologies required to maintain a consistent differential impedance of 100 ohms to the signal placed on the transmission line are limited to Stripline and Microstrip types. The designer must decide whether the signalling must be moved to an outer layer of the board using a Microstrip topology, or if the signalling may be placed on an inner layer as stripline where shielding by ground and power planes above and below is possible.

3.3.1 Stripline

The RapidIO buses should be routed in a symmetrical edge-coupled stripline structure in order to ensure a constant impedance environment. The symmetrical stripline construction is shown in Figure 11. This method also provides clean and equal return paths through VSS and VDD from the I/O cell of the Tsi568A to the adjacent RapidIO device. The use of broadside coupled stripline construction as shown in Figure 12 is discouraged because of its inability to maintain a constant impedance throughout the entire board signal layer.

The minimum recommended layer count of a board design consists of 12 layers. The optimum design consists of 16 layers. The designer should consider both of these designs and weigh their associated costs versus performance.

Figure 11: Recommended Edge Coupled Differential Stripline (symmetric when h1=h2)



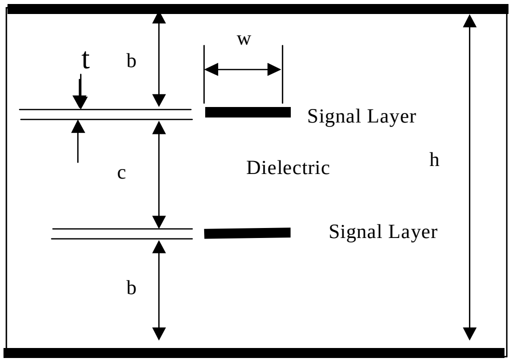
Equations for Stripline and Differential Stripline Impedance (in Ohms):

$$Zo = \frac{60}{\sqrt{\varepsilon_r}} \times \ln\left(\frac{1.9\left(2(h1 + h2) + t\right)}{0.67\,\pi\left(0.8w + t\right)}\right)$$

$$Zdiff = 2 \times Zo\left(1 - 0.374\, e^{-2.9\left[\frac{s}{h1 + h2}\right]}\right)$$

The broadside coupled stripline construction is not recommended for use with RapidIO because of the manufacturing variations in layer spacings. These variations will cause impedance mismatch artifacts in the signal waveforms and will degrade the performance of the link.

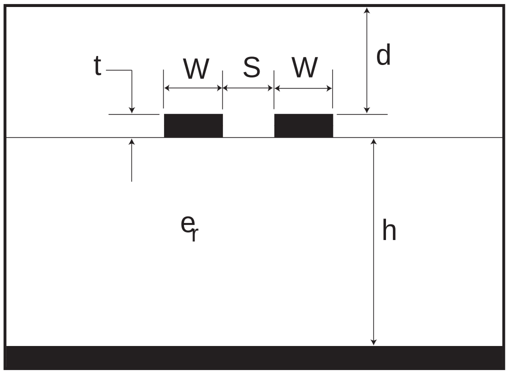
Figure 12: Not Recommended Broadside Coupled or Dual Stripline Construction



3.3.1.1 Microstrip

When it is necessary to place the differential signal pairs on the outer surfaces of the board, the differential microstrip construction is used. Figure 13 shows the construction of the microstrip topology. Below the figure are the design equations for calculating the impedance of the trace pair.

Figure 13: Differential Microstrip Construction



Equations for the Differential Microstrip construction:

$$Z_o = \frac{60}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left[\frac{4h}{0.67(0.8w+t)}\right] ohms$$

$$Z_{diff} \cong 2Z_o\left(1-0.48e^{-0.96\frac{s}{h}}\right) ohms$$

3.3.1.2 Signal Return Paths

The return path is the route that current takes to return to its source. It can take a path through ground planes, power planes, other signals, or integrated circuits. The return path is based on electro-magnetic field effects. The return path follows the path of least resistance nearest to the signal conductor. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths need to be given similar consideration. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance.

If via densities are large and most of the signals switch at the same time (as would be the case when a whole data group switches layers), the layer to layer bypass capacitors fail to provide an acceptably short signal return path to maintain timing and noise margins.

Since the signals are routed using symmetric stripline, return current is present on both the VDD and VSS planes. If a layer change must occur, then VCC and VSS vias must be placed as close to the signal via as possible in order to provide the shortest possible path for the return current.

The following return path rules apply to all designs:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Do not route impedance controlled signals over splits in the reference planes.
- Do not route signals on the reference planes in the vicinity of system bus signals.
- Do not make signal layer changes that force the return path to make a reference plane change.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not route over via anti-pads or socket anti-pads.

If reference plane changes must be made:

- Change from a VSS reference plane to another VSS reference plane and place a via connecting the two planes as close as possible to the signal via. This also applies when making a reference plane change from one VCC plane to another VCC plane.
- For symmetric stripline, provided return path vias for both VSS and VCC.
- Do not switch the reference plane from VCC to VSS or vice versa.

3.3.1.3 Guard Traces

Guard traces are used to minimize crosstalk. Guard traces are tracks that run parallel to a signal trace for the entire length and are connected to the reference plane to which the signal(s) are associated. Guard traces can lower the radiated crosstalk by as much as 20dB, but will also lower the characteristic impedance of the signal trace due to their proximity.

The use of guard tracks requires some planning and foresight. The guard tracks will consume board real estate. Simulation has shown that a 5 mil ground trace with 5 mil spaces between the aggressor and receptor traces offers as much isolation as a 20 mil space between aggressor and receptor traces. The aggressor trace is the trace with a driven waveform on it. The receptor trace is the trace onto which the crosstalk is coupled.

Guard tracks are required to be stitched or connected with vias to the reference plane associated with the aggressor signal. To ensure that there is no resonance on the guard traces the stitching vias should be spaced at intervals that equal $1/20\lambda$ of the 3rd harmonic.

Figure 14: Equation

$$\lambda = \sqrt{\varepsilon_r} \times {}^{c}\!/_{f}$$

$$ {}^{1}\!/_{20}\,\lambda_{3rd} = \frac{3 \times 10^{8}\, m/s}{20 \times f_{3rd}} \sqrt{\varepsilon_r}$$

In the case of the 3.125 Gbits/s data rate, the rise and fall times must be less than 40 pS. This relates to an upper frequency of 25Ghz and a corresponding wavelength of 25 mm based on a permittivity of 4.3. Therefore, the stitching vias must not be further apart than 8 mm.

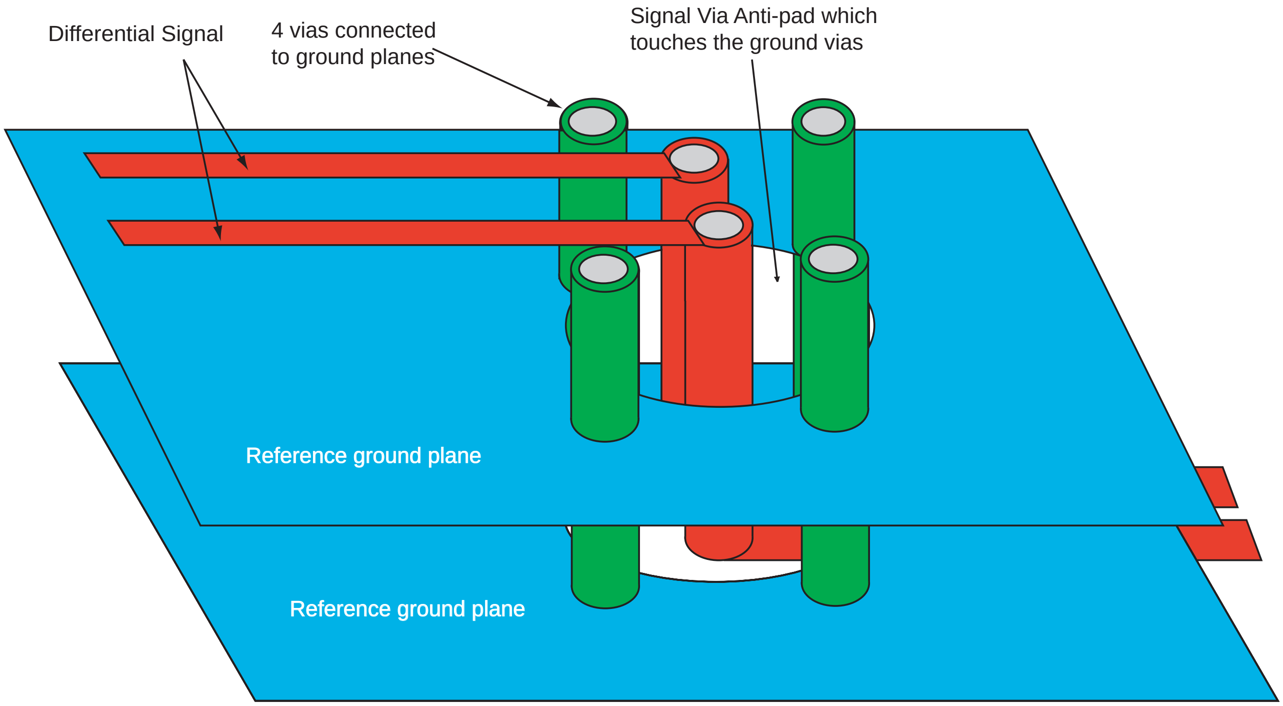
3.3.1.4 Via Construction

Due to the high frequency content of the Serial RapidIO signals, it is necessary to minimize the discontinuities imposed by crossing ground and power planes when it is necessary to transition to different signal layers. The use of a controlled impedance via is necessary. The construction of the vias is shown in Figure 15.

TIP

Detailed design information can be found in bibliography entry 15, "*Designing Controlled Impedance Vias*" by Thomas Neu, EDN Magazine October 2, 2003.

Figure 15: Differential Controlled Impedance Via



3.3.1.5 Layer Transitioning with Vias

The basic rule is to keep vias in the signal path down to a minimum. Vias represent a significant impedance discontinuity and should be minimized. When routing vias, try to ensure that signals travel through the via rather than across the via.

A via where the signal goes through the via, has a much different effect than a via where the signal travels across the via. These two cases are shown in Figure 17 and in Figure 18. The "in" and "out" nodes of the via model are shown on the their corresponding locations in the figures.

Transitioning across a via that is not blind or buried leaves a stub which appears as a capacitive impedance discontinuity. The portion of the via that conducts current appears inductive while the stub that develops only an electric field will appear capacitive.

In order to minimize the effects of a via on a signal, the following equations may be used to approximate the capacitance and inductance of the via design. It can be seen that the proximity of the pad and antipad have a direct relationship on the capacitance, and that the length of the barrel (h) has a direct effect on the inductance.

$$L = 5.08h\left[\ln\left(\frac{4h}{d}\right) + 1\right] \qquad C = \frac{1.41\varepsilon_r TD_1}{D_2 - D_1}$$

C is the capacitance in pF.
T is the thickness of the circuit board or thickness of pre-preg.
D_1 is the diameter of the via pad.
D_2 is the diameter of the antipad.
ε_r is the dielectric constant of the circuit board material.

L is the inductance in nH.
h is the overall length of the via barrel.
d is the diameter of the via barrel.

Figure 16: Via Construction

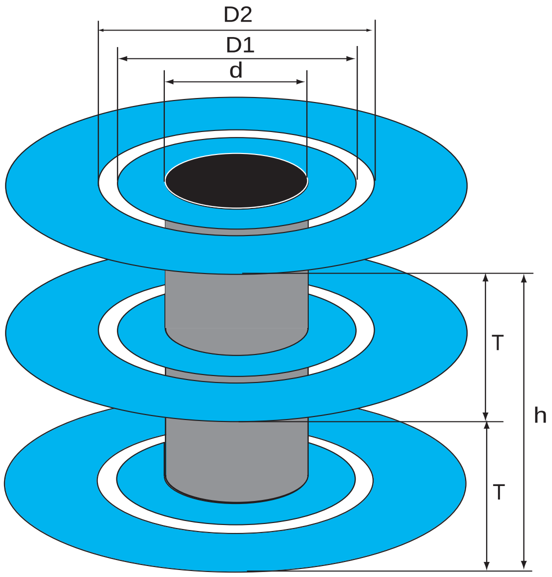


Figure 17: Signal Across a Via

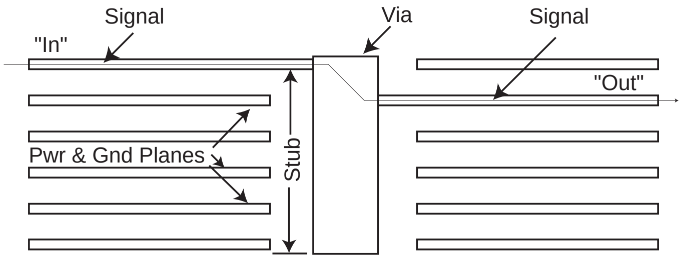
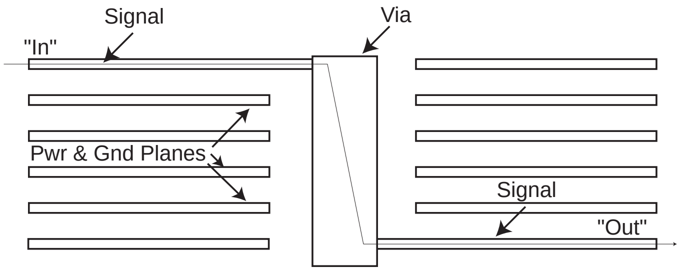


Figure 18: Signal Through a Via



Because of the high frequencies present in the RapidIO signal, vias become a significant contributor to signal degradation. Most vias are formed by a cylinder going through the PCB board. Because the via has some length, there is an inductance associated with the via. Parasitic capacitance comes from the power and ground planes through which the via passes. From this structure we model the via in RLC lumps as shown in Figure 19 and Figure 20. Cvia is the total capacitance of the via to ground or power, Rvia is the total resistance through the via, and Lvia is the total inductance of the via. These parameters may be extracted using 3D parasitic extraction tools. By distributing the R, L, and C, the model better represents the fact that the capacitance, resistance and inductance are distributed across the length of the via. For the Via model to be accurate in simulation, the propagation delay of each LC section should be less than 1/10 of the signal risetime. This is to ensure the frequency response of the via is modeled correctly up to the frequencies of interest. More information may be found in reference [16].

Figure 19: Signal Transitioning Across a Via Simulation Model

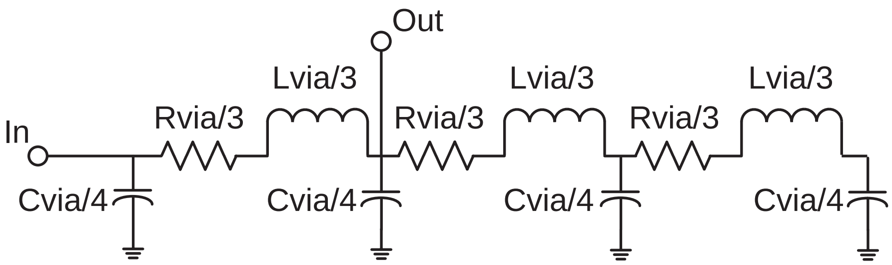
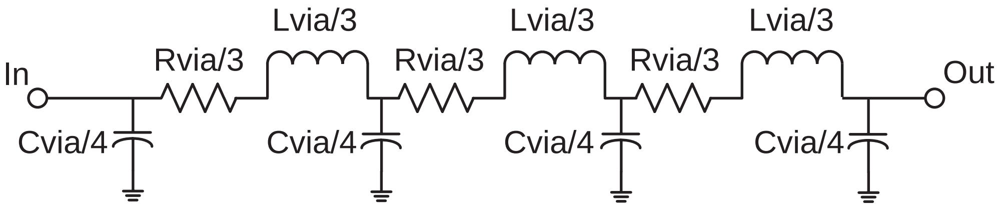


Figure 20: Signal Transitioning Through a Via Simulation Model



3.3.1.6 Buried Vs. Blind

The use of buried and blind vias is recommended because in both cases the signal travels through the via and not across it. Examples of these two types of structures are shown in Figure 21 and Figure 22.

Figure 21: Buried Via Example

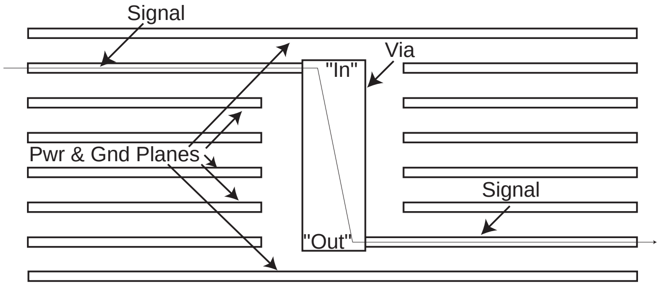
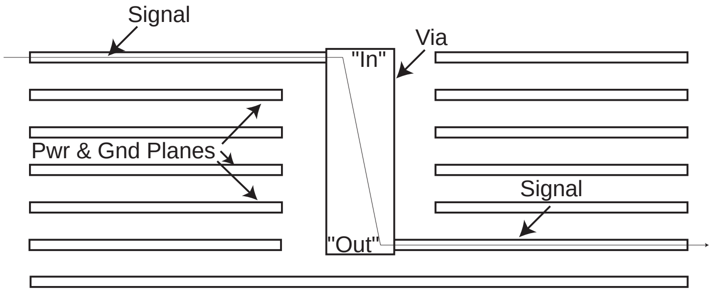


Figure 22: Blind Via Example

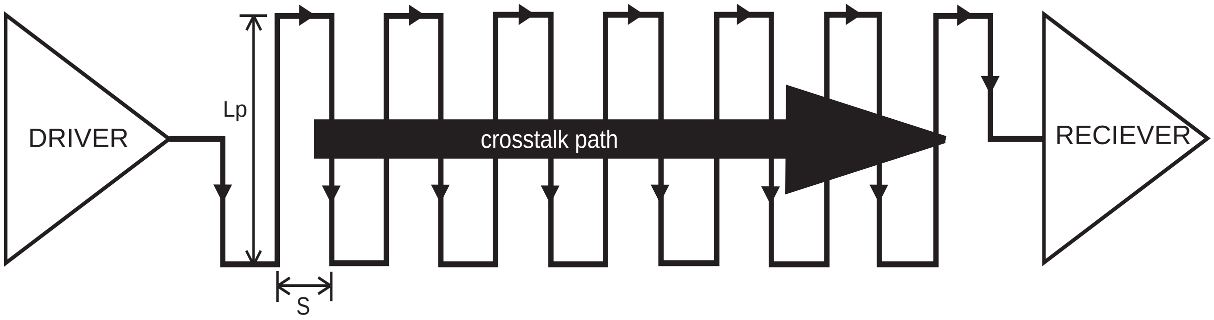


3.3.1.7 Serpentine Traces

During layout, it is necessary to adjust the lengths of tracks in order to accommodate the requirements of equal track lengths for pairs of signals. In the case of the LVDS/CML signals, this ensures that both the negative and positive halves of the signals arrive at the receiver simultaneously, thus maximizing the data sampling window in the eye diagram. Creating a serpentine track is a method of adjusting the track length.

Ensure that the wave front does not propagate along the trace and through the crosstalk path perpendicular to the parallel sections, as shown in Figure 23. The arrival of a wave front at the receiver ahead of the wave front travelling along the serpentine route is caused by the self-coupling between the parallel sections of the transmission line (Lp).

Figure 23: Serpentine Signal Routing



To maximize the signal integrity, clock lines should not be serpentine.

Figure 26 describes the guidelines for length matching a differential pair.If it is necessary to serpentine a trace, follow these guidelines:

- Make the minimum spacing between parallel sections of the serpentine trace (see “S” in Figure 23) at least 3 to 4 times the distance between the signal conductor and the reference ground plane.
- Minimize the total length (see “Lp” in Figure 23) of the serpentine section in order to minimize the amount of coupling.
- Use an embedded microstrip or stripline layout instead of a microstrip layout.

For a detailed discussion about serpentine layouts, refer to Section 12.8.5 of *“High-Speed Signal Propagation, Advanced Black Magic”* by Howard Johnson and Martin Graham.

3.3.2 Crosstalk Considerations

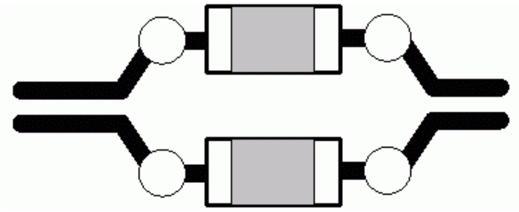
The Serial RapidIO signals easily capacitively couple to adjacent signals due to their high frequency. It is therefore recommended that adequate space be used between different differential pairs, and that channel transmit and receive be routed on different layers. Cross coupling of differential signals results in an effect called Inter-Symbol Interference (ISI). This coupling causes pattern dependent errors on the receptor, and can substantially increase the bit error rate of the channel.

3.3.3 Receiver DC Blocking Capacitors

The Serial RapidIO interface requires that the port inputs be capacitor coupled in order to isolate the receiver from any common mode offset that may be present in the transmitter outputs. DC blocking capacitors should be selected such that they have low dissipation factor and low series inductance. Figure 24 shows the recommended tracking and capacitor pad placement required. It will be necessary to model and simulate the effects of the changed track spacing on the channel quality and determine if any changes are required to the topology. An often used method of correcting the decreased impedance caused by the larger capacitor mounting pads is to create a slot in the shield plane below the capacitor bodies and soldering pads. Since the impedance change caused by the slot is dependent on the capacitor geometry, core thickness, core material characteristics and layer spacings, the size and shape of the slot will have to be determined by simulation.

Do not place the capacitors along the signal trace at a $\lambda/4$ increment from the driver in order to avoid possible standing wave effects.

Figure 24: Receiver Coupling Capacitor Positioning Recommendation



3.3.4 Escape Routing

All differential nets should maintain spacing throughout a route. Separation of differential pairs to go around objects should not be allowed. Figure 25 illustrates several options for breaking out a differential pair from the Tsi568A device. The order of preference is from A to D.

Case D below has a small serpentine section used to match the inter-pair skew of the differential pair. In this case each serpentine section should be greater than 3 x W (W=width), and the gap should not increase by more than 2x. Figure 26 illustrates these requirements.

Figure 25: Escape Routing for Differential Signal Pairs

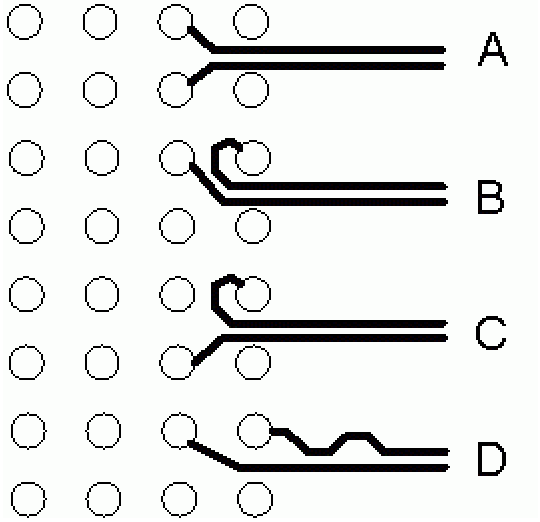
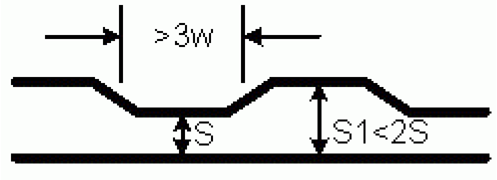


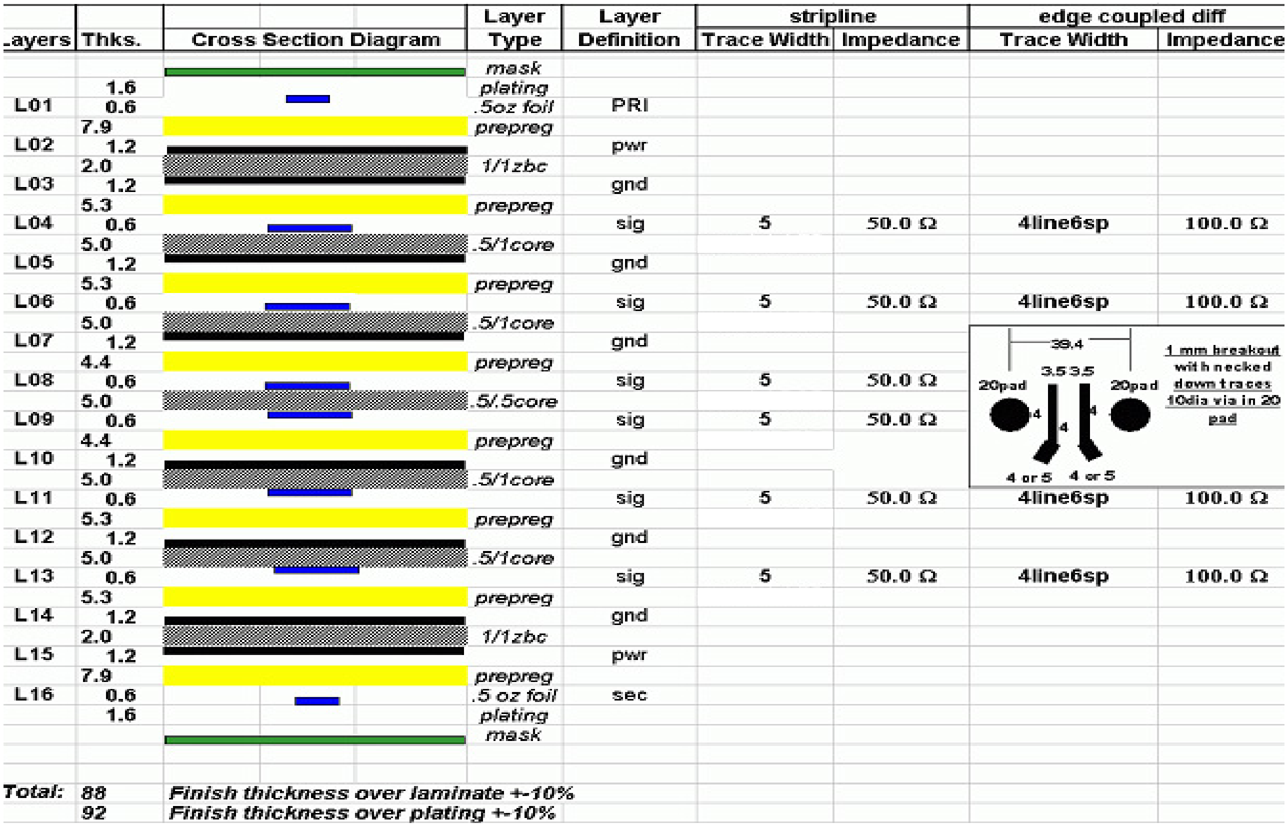
Figure 26: Differential Skew Matching Serpentine



3.3.5 Board Stackup

The recommended board stack up is shown in Figure 27. This design makes provision for four stripline layers and two outer microstrip layers. Layers eight and nine are provisioned as orthogonal low speed signal routing layers.

Figure 27: Recommended Board Stackup



			Layer	Layer	stripline		edge coupled diff	
ayers	Thks.	Cross Section Diagram	Type	Definition	Trace Width	Impedance	Trace Width	Impedance
			mask					
	1.6		*plating*					
L01	0.6		*.5oz foil*	PRI				
	7.9		*prepreg*					
L02	1.2			pwr				
	2.0		*1/1zbc*					
L03	1.2			gnd				
	5.3		*prepreg*					
L04	0.6			sig	5	50.0 Ω	4line6sp	100.0 Ω
	5.0		*.5/1core*					
L05	1.2			gnd				
	5.3		*prepreg*					
L06	0.6			sig	5	50.0 Ω	4line6sp	100.0 Ω
	5.0		*.5/1core*					
L07	1.2			gnd				
	4.4		*prepreg*					
L08	0.6			sig	5	50.0 Ω		
	5.0		*.5/.5core*					
L09	0.6			sig	5	50.0 Ω		
	4.4		*prepreg*					
L10	1.2			gnd				
	5.0		*.5/1core*					
L11	0.6			sig	5	50.0 Ω	4line6sp	100.0 Ω
	5.3		*prepreg*					
L12	1.2			gnd				
	5.0		*.5/1core*					
L13	0.6			sig	5	50.0 Ω	4line6sp	100.0 Ω
	5.3		*prepreg*					
L14	1.2			gnd				
	2.0		*1/1zbc*					
L15	1.2			pwr				
	7.9		*prepreg*					
L16	0.6		*.5 oz foil*	sec				
	1.6		*plating*					
			mask					
Total:	***88***	***Finish thickness over laminate +-10%***						
	92	***Finish thickness over plating +-10%***						

1 mm breakout with necked down traces 10dia via in 20 pad

3.4 Power Distribution

The Tsi568A is a high speed device with both digital and analogue components in its design. The core logic has a high threshold of noise sensitivity within its 1.2V operating range. However, the analogue portion of the switch is considerably more sensitive.

The correct treatment of the power rails, plane assignments and decoupling is important to maximizing the performance the Tsi568A can deliver. The largest indicator of poor performance on the Serial RapidIO interfaces is the presence of jitter. The die, I/O and package designs have all been optimized to provide jitter performance well below the limits required by the Serial RapidIO specifications. The guidelines provided below will assist the user in achieving a board layout that will provide the best performance possible. The required decoupling by each voltage rail can be found in Table 18 on page 61. The ripple specifications for each rail are maximums, and every effort should be made to target the layout to achieve lower values in the design.

A solid, low impedance plane must be provided for the VDD 1.2V core supply referenced to VSS. It is strongly recommended that the VDD and VSS planes be constructed with the intent of creating a buried capacitance. The connection to the power supply must also be low impedance in order to minimize noise conduction to the other supply planes.

A solid, low impedance plane must be provided for the SP_VDD 1.2 V SerDes supply, referenced to the VSS plane. This supply can be derived from the same power supply as VDD, as long as a Kelvin connection is used. The preference however, is to use a separate power supply.

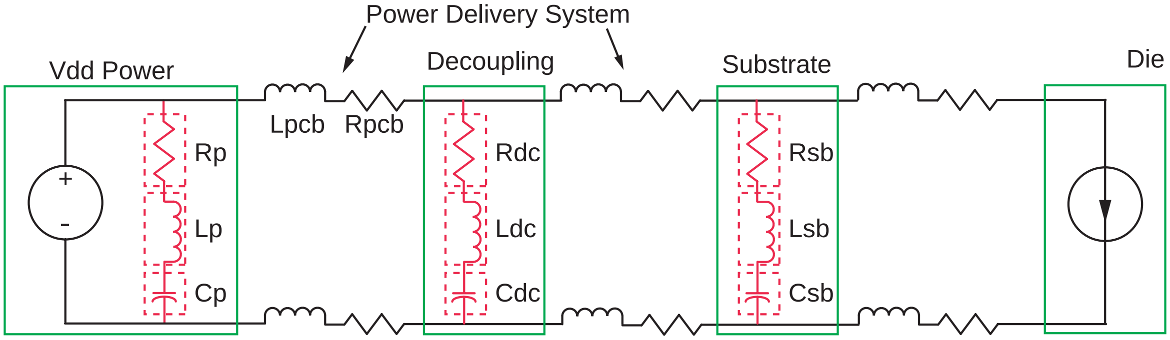
The SPn_AVDD 1.2 V SerDes analogue supply also needs to be sourced from a low impedance supply plane. This supply voltage powers the SerDes PLLs. The SP_VDD plane may also be used for the SPn_AVDD supply. Connect all of the SPn_AVDD pins to this plane through the filters shown in Figure 29 and decouple the plane directly to VSS.

The VDD_IO supply powers the 3.3V I/O cells on the switch. This supply requires no special filtering other than the decoupling to the VSS_IO plane. Connect the VSS_IO plane to the VSS plane using a Kelvin connection.

3.5 Decoupling Requirements

This section deals with the subject of decoupling capacitors required by the Tsi568A. To accomplish the goal of achieving maximum performance and reliability, the power supply distribution system needs to be broken down into its individual pieces, and each designed carefully. The standard model for representing the components of a typical system are shown in Figure 28. This figure graphically represents the parasitics present in a power distribution system.

Figure 28: System Power Supply Model



3.5.1 Component Selection

The recommended decoupling capacitor usage for the Tsi568A is shown below in Table 18 on page 61. The capacitors should be selected with the smallest surface mount body that the applied voltage permits in order to minimize the body inductance.

The components should be distributed evenly around the device in order to provide filtering and bulk energy evenly to all of the ports.

Use the Tsi568A ball map (available at www.tundra.com) to aid in the distribution of the capacitors.

The SerDes PLLs require extra care in order to minimize jitter on the transmitted signals. The circuit shown in Figure 29 is recommended. One filter is required for each RapidIO port.

Figure 29: PLL Filter

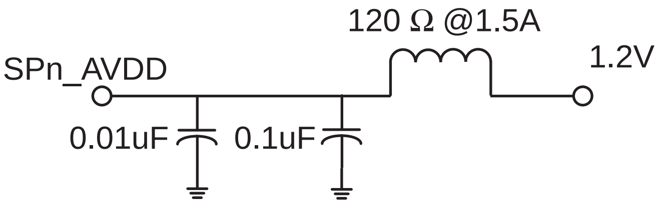


Table 18: Decoupling Capacitor Quantities and Values Recommended for the Tsi568A

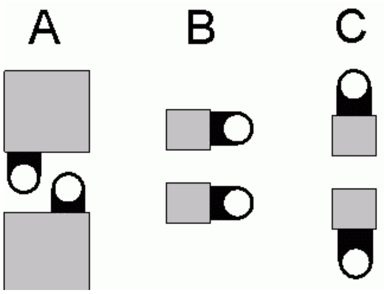
Voltage	Usage	Acronym	Component Requirements			
1.2V	Logic Core	VDD	20 x 0.1uF	20 x 0.01uF	16 x 1nF	16 x 22uF
1.2V	SerDes core, SerDes bias Serial drivers	SP_VDD	8 x 0.1uF	48 x 0.01uF	8 x 10uF	8 x 100uF
1.5V	SerDes termination supply	VTT	8 x 0.1uF	8 x 0.01uF	--	--
3.3V	Single ended I/O ports	VDD_IO	12 x 0.1uF	12 x 0.01uF	--	--
1.2V	PLL	SPn_AVDD	8 x 0.1uF	8 x 0.01uF	8 x ferrite bead 120 ohm @ 1.5Amp	

3.5.1.1 Effective Pad Design

Breakout vias for the decoupling capacitors should be kept as close together as possible. The trace connecting the pad to the via should also be kept as short as possible with a maximum length of 50mils. The width of the breakout traces should be 20mils, or the width of the pad.

Via sharing should not be used in board design with the Tsi568A.

Figure 30: Recommended Decoupling Capacitor Pad Designs

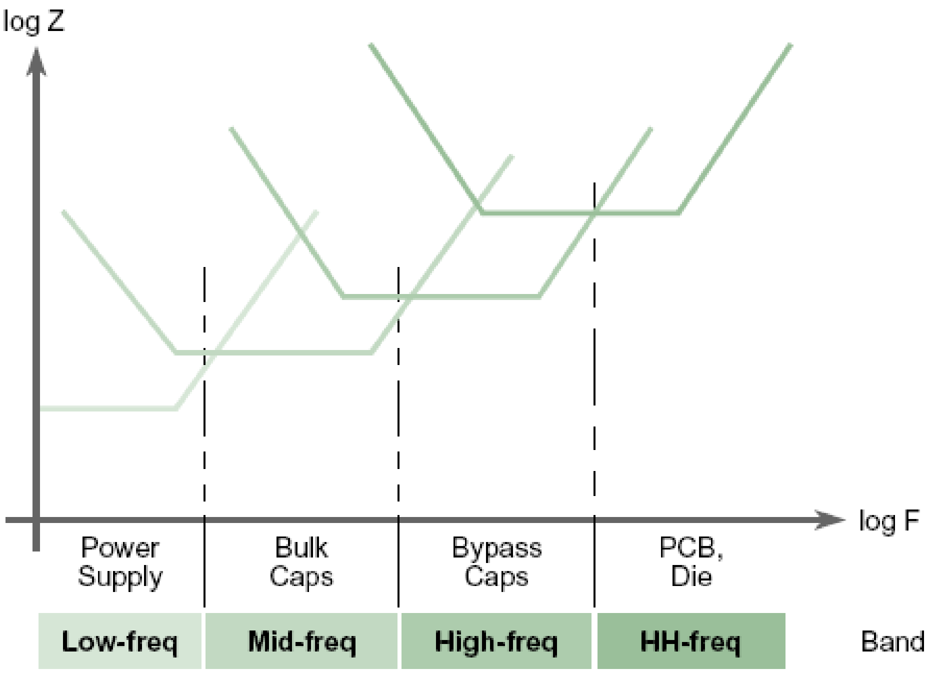


3.5.2 Power Plane Impedance and Resonance

The intent of adding decoupling to a board is to lower the impedance of the power supply to the devices on the board. It is necessary to pay attention to the resonance of the combined bulk capacitance and to stagger the values in order to spread the impedance valleys broadly across the operating frequency range. Figure 31 demonstrates the concept of staggered bands of decoupling. Calculate the impedance of each of the capacitor values at the knee frequency to determine their impact on resonance.

$$F_{knee} = \frac{0.5}{T_{rise}} \text{ where } T_{rise} = \text{time from 10\% to 90\%}$$

Figure 31: Decoupling Bypass Frequency Bands



As the frequency changes, each part of the PDS responds proportionally; the low-impedance power supply responds to slow events, bulk capacitors to mid-frequency events, and so forth.

3.6 Clocking and Reset

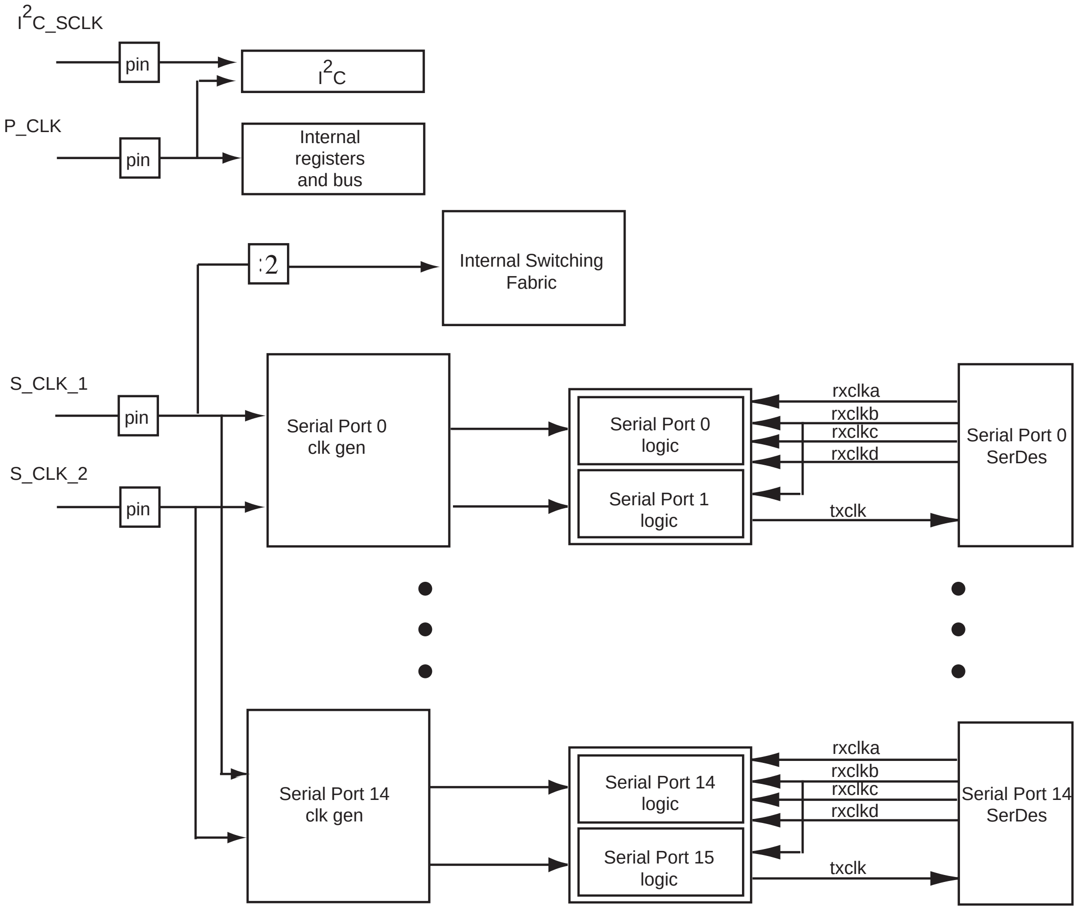
This section discusses the requirements of the clock and reset inputs.

3.6.1 Clock Overview

The Tsi568A has three input reference clocks that are used to produce the Tsi568A internal clock domains.

The following diagram illustrates the clocking architecture of the Tsi568A.

Figure 32: Tsi568A Clocking Architecture



The three reference clocks are described in Table 19. Each of the listed clock domains is described in detail in the following sub-section. For more information about special line rate support see "Line Rate Support" on page 73.

Table 19: Clock Input Sources

Clock Input Pin	Type	Maximum Frequency	Clock Domain
S_CLK_1_[P/N]	Differential	312.5 MHz	Serial Transmit Domain 2 (Nominally 312.5MHz) Internal Switching Fabric (ISF) Domain
S_CLK_2_[P/N]	Differential	250 MHz	Serial Transmit Domain 1 (Nominally 250 MHz) Serial Transmit Domain 0 (Nominally 125 MHz) Note: if the Tsi568A never uses Serial Transmit Domains 1 and 2, then this input reference clock is not required to be driven.
P_CLK	Single Ended	100 MHz	Internal Register Domain and I^2C Domain

3.6.1.1 Frequencies Required

The clock signals should be shielded from neighboring signal lines using ground traces on either side. This reduces jitter by minimizing crosstalk from the neighboring signal lines. Since P_CLK is single-ended, extra precaution should be taken so that noise does not get coupled onto it.

In order to preserve the quality of the low jitter clock, the shielding requirement of the clock lines is critical. It is possible that low-frequency noise can interfere with the operation of PLLs, which can cause the PLLs to modulate at the same frequency as the noise. The high-frequency noise is generally beyond the PLL bandwidth which is about 1/10th the RefClk frequency.

3.6.1.2 Stability, Jitter and Noise Content

The maximum input jitter on the S_CLK_1 and S_CLK_2 inputs is 7pS peak to peak from 1.8 to 32 Mhz to avoid passing through the PLL loop filter in the SerDes and afftecting the transmit data streams. The maximum input jitter allowable on the P_CLK input is 300 pSpp. Jitter on this input would be reflected outside of the chip on the I^2C bus.

Jitter Equation

The following equation can be used to convert Phase Noise in dBc to RMS jitter:

$$\text{RMSjitter pS(rms)} = [((10^{(\text{dBc}/10)})^{1/2}) * 2] / [2 * \text{pi} * (\text{frequency in hz})]$$

Using this equation, an example of 312.5 MHz and a phase noise of -63dBc, would produce 0.72pS RMS jitter.

3.6.2 Clock Domains

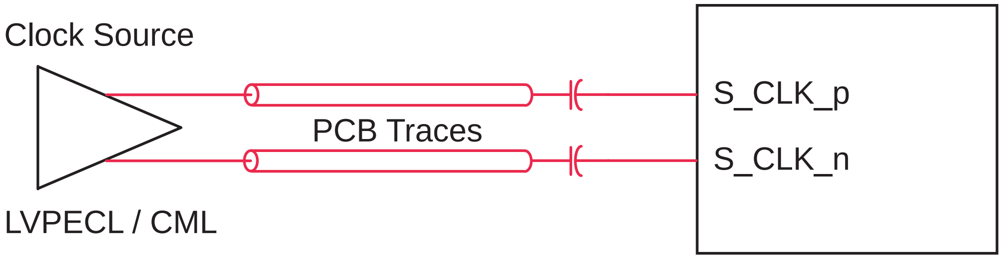
Table 20: Tsi568A Clock Domains

Clock Domain	Clock Source	Description
Internal Register Domain	P_CLK	This clock domain includes all of the internal registers and their interconnect bus. The domain uses the input P_CLK directly.
Internal Switching Fabric Domain	S_CLK_1_[p/n] divided by 2	This clock domain includes the switching matrix of the ISF and the portion of each RapidIO block that interfaces to the ISF.
I^{2}C Domain	P_CLK divided by 1000	This clock domain is responsible for driving the I2C output clock pin I2C_SCLK. This clock domain is generated by dividing the P_CLK input by 1000. The majority of the I2C logic runs in the Internal Register Domain
Serial Transmit Domain 0	S_CLK_2_[p/n] divided by 2	This clock domain is used to clock all of the Serial RapidIO transmit ports that have the SCLK_SEL field in the SMACx_CLK_SEL register set to 00. The S_CLK_2_p/n input is divided in half and used to clock the transmit logic. This clock is multiplied by 10 to produce the high-speed clock that is used to output the serial data on output pins SP{0..15}_T{A..D}_p/n. The maximum data rate available using this domain is 1.25 Gb/s per lane.
Serial Transmit Domain 1	S_CLK_2_[p/n]	This clock domain is used to clock all of the Serial RapidIO transmit ports that have the SCLK_SEL field in the SMACx_CLK_SEL register set to 01. The S_CLK_2_p/n input is used directly to clock the transmit logic. This clock is multiplied by 10 to produce the high-speed clock that is used to output the serial data on output pins SP{0..15}_T{A..D}_p/n. The maximum data rate available using this domain is 2.5 Gb/s per lane.
Serial Transmit Domain 2	S_CLK_1_[p/n]	This clock domain is used to clock all the Serial RapidIO transmit ports that have the SCLK_SEL field in the SMACx_CLK_SEL register set to 10. The S_CLK_1_p/n input is used directly to clock the transmit logic. This clock is multiplied by 10 to produce the high-speed clock that is used to output the serial data on output pins SP{0..15}_T{A..D}_p/n. The maximum data rate available using this domain is 3.125 Gb/s per lane.

3.6.2.1 Interfacing to the S_CLK_x inputs

The interface for a LVPECL or CML clock source to the converter cell is shown in Figure 33. Note that an AC-coupled interface is required so that only the AC information of the clock source is transmitted to the clock inputs of the Tsi568A.

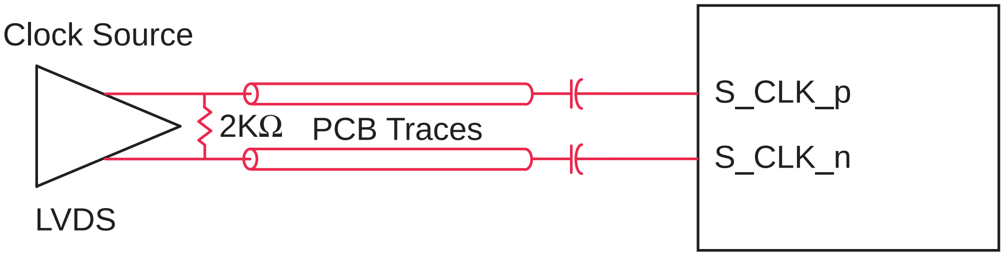
Figure 33: Tsi568A driven by LVPECL or CML clock source



The interface for an LVDS clock source to the converter cell is shown in Figure 34. Since an LVDS driver requires a DC termination path, a 2-K. resistor should be inserted before the capacitors. This resistor can be placed anywhere along the signal path between the clock source and the AC-coupling capacitors, although Tundra recommends placing it close to the clock source.

Note that the effective termination resistance seen by the clock source is about 95Ω. due to the parallel combination of this external resistor and the integrated termination resistor of the converter cell. Again, an AC-coupled interface is required so that only the AC information of the clock source is transmitted to the clock inputs of the Tsi568A.

Figure 34: Tsi568A driven by an LVDS clock source



3.6.3 Reset Requirements

The Tsi568A requires only one reset input, HARD_RST_b. The signal provided to the device must be a monotonic 3.3V swing that de-asserts a minimum of 1mS after supply rails are stable. The signal de-assertion is used to release synchronizers based on P_CLK which control the release from reset of the internal logic. P_CLK must therefore be operating and stable before the 1mS HARD_RST_b countdown begins.

TRST_b must be asserted while HARD_RST_b is asserted following a device power-up to ensure the correct setup of the tap controller. TRST_b is not required to be re-asserted for non power cycle assertions of HARD_RST_b.

TIP The most versatile solution to this requirement is to AND the HARD_RST_b and TRST_b signals together to form an output with which to drive the TRST_b pin on the switch.

Power up option pins are double sampled at the release of HARD_RST_b. As such, there is no set-up time requirement, but the signals must be stable at the release of HARD_RST_b. There is a hold time requirement of 100nS or 10 P_CLK cycles minimum.

3.7 Modeling and Simulation

The need for verifying the signal integrity of the board design is very important for designs using GHz signalling. Tundra recommends that the designer invest in a simulation tool as an aid to a successful RapidIO design. Tools are available from companies such as Mentor Graphics (HyperLynx GHZ), Ansoft (SIwave) and SiSoft (SiAuditor). This is by no means a complete list, only a sample of known suppliers.

3.7.0.1 IBIS

The use of IBIS for signal integrity checking at the high frequencies of the Serial RapidIO link have been found to be too inaccurate to be useful. Also, we have found that most tools do not yet support the *IBIS Specification (Revision 3.2)* for the support of multi-staged slew rate controlled buffers. For this reason, Tundra is not presently making available an IBIS file for the Tsi568A.

3.7.0.2 Encrypted HSPICE

Please contact the Tundra Applications Engineering through the web based form at www.tundra.com/support to request the necessary Non-disclosure Agreement form required to acquire the encrypted model.

3.8 Testing and Debugging Considerations

It is prudent to make provision for debugging and testing tools in order to speed board bring-up. This section provides information on the probing requirements for monitoring the serial RapidIO link between two devices. At GHz frequencies, standard probing techniques are intrusive and cause excessive signal degradation introducing additional errors in the link stream. The recommended solution is an ultra low capacitance probe that operates in conjunction with a logic analyzer. The addition of the appropriate disassembler software to the analyzer makes it a very powerful tool for examining the traffic on a link and aiding in software debugging. Please contact your local test equipment vendor for appropriate solutions for your requirements.

3.8.1 Logic Analyzer Connection Pads

The pinout for a recommended SRIO 8-channel probe is given in Table 21. This pin/signal assignment has been adopted by several tool vendors including Tektronix, but is not an established standard.

These notes are given here:

Footprint Channel vs. Lane/Link Designations

- Channel = either an upstream OR downstream differential pair for a given lane
- C<letter> = the designator for a channel which accepts a given differential pair of signals
- C<letter><p or n> = the two signals of the differential pair. The signals within a given pair may be assigned to either P or N regardless of polarity.

3.8.1.1 General Rules for Signal Pair Assignment of Analyzer Probe

The differential pairs that make up the SRIO links must be assigned to specific pins of the footprint. However, there is some freedom in this pair assignment in order to minimize routing constraints on the platform.

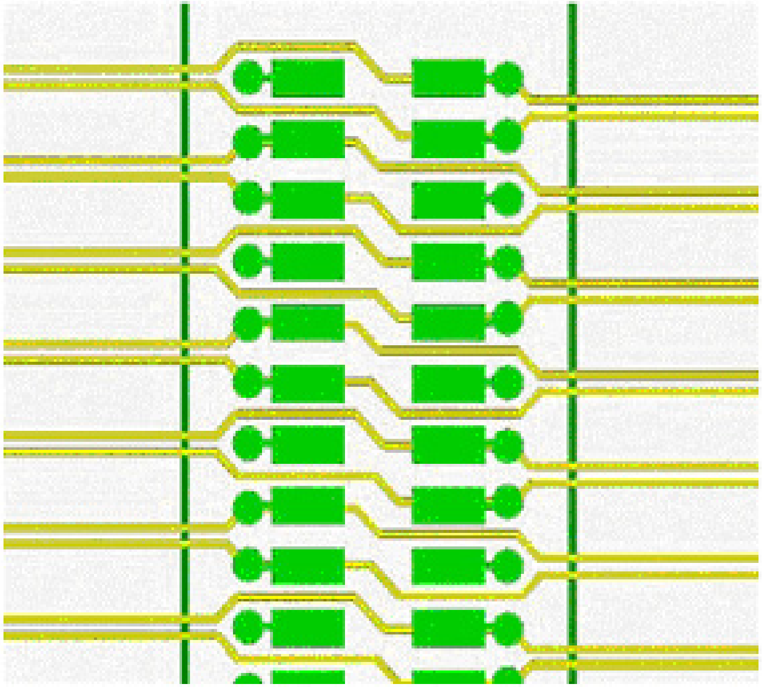
Table 21: 8-Channel Probe Pin Assignment

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	CAp/Tx0
4	CBp/Rx0	3	CAn/Tx0
6	CBn/Rx0	5	GND
8	GND	7	CCp/Tx1
10	CDp/Rx1	9	CCn/Tx1
12	CDn/Rx1	11	GND
14	GND	13	CEp/Tx2
16	CFp/Rx2	15	CEn/Tx2
18	CFn/Rx2	17	GND

Table 21: 8-Channel Probe Pin Assignment

Pin #	Signal Name	Pin #	Signal Name
20	GND	19	CGp/Tx3
22	CHp/Rx3	21	CGn/Tx3
24	CHn/rX3	23	GND

Figure 35: Analyzer Probe Pad Tracking Recommendation



3.8.2 JTAG Connectivity

The Joint Test Action Group (JTAG) created the boundary-scan testing standard (documented in the *IEEE 1149.1 Standard*) for testing printed circuit boards (PCBs).

The boundary-scan approach involves designing boundary-scan circuitry into the integrated circuit. PCBs populated with 1149.1 compliant devices can be then tested for connectivity, correct device orientation, correct device location, and device identification. All the pins on compliant devices can be controlled and observed using (typically) five pins that are routed to the board edge connector. Board designers can develop a standard test for all 1149.1 compliant devices regardless of device manufacturer, package type, technology, or device speed.

Please visit the Tundra web site to download the BSDL file for the Tsi568A.

The SerDes pins are not on the boundary scan chain.

The Tsi568A also has the capability to read and write all internal registers through the JTAG interface. Through this interface, users may load and modify configuration registers and look up tables without the use of RapidIO maintenance transactions or an I^{2}C EEPROM. Please visit the Tundra web site at www.tundra.com/support to download document number 35A8000_SW001 which is the JTAG software to use to access the internal registers.

3.9 Reflow Profile

The Tsi568A adheres to JEDEC-STD-020C for its reflow profile. For the leaded version, the peak reflow temperature is 225^{o}C (+0/-5^{o}C). For the lead-free version, the peak reflow temperature is 260^{o}C (+0/-5^{o}C).

4. Line Rate Support

The Tundra Tsi568A supports all the *RapidIO Interconnect Specification (Revision 1.2)* specified line rates (1.25, 2.50, and 3.125 Gbit/s). The device also supports line rates that are outside of the RapidIO specification. The ability to support multiple line rates gives the Tsi568A flexibility in both application support and power consumption.

Table 22 shows the supported, standard line rates for the Tsi568A.

Table 22: Tsi568A Supported Standard RapidIO Line Rates

S_CLK_1 Frequency (MHz)	S_CLK_2 Frequency (MHz)	Supported Line Rates	Lane Configuration
250	250[1]	1.25 Gbit/s 2.5 Gbit/s	1x
250	250[1]	1.25 Gbit/s 2.5 Gbit/s	4x
312.5	Not Required[2]	3.125 Gbit/s	1x
312.5	Not Required[2]	3.125 Gbit/s	4x
312.5	250[1]	3.125 Gbit/s 2.5 Gbit/s 1.25 Gbit/s	1x
312.5	250[1]	3.125 Gbit/s 2.5 Gbit/s 1.25 Gbit/s	4x

1. 1.25 Gbit/s line rates can be supported with internal divide options using a 250 MHz S_CLK_2 clock frequency
2. S_CLK_2 is only required to be present when 3.125 Gbit/s and either 1.25 Gbit/s or 2.5 Gbit/s link rates are required in the same application. If these line rates are not required, S_CLK_2 can be left unconnected.

Table 23 shows the supported, non-standard line rates for the Tsi568A.

Table 23: Tsi568A Supported Non-standard Line Rates

S_CLK_1 Frequency (MHz)	S_CLK_2 Frequency (MHz)	Supported Line Rates	Lane Configuration
245.76	245.76[1]	1.2288 Gbit/s 2.4576 Gbit/s	1x
245.76	245.76[1]	1.2288 Gbit/s 2.4576 Gbit/s	4x
307.20	Not Required[2]	3.072 Gbit/s	1x
307.20	Not Required[2]	3.072 Gbit/s	4x
307.20	245.76[1]	3.072 Gbit/s 1.2288 Gbit/s 2.4576 Gbit/s	1x
307.20	245.76[1]	3.072 Gbit/s 1.2288 Gbit/s 2.4576 Gbit/s	4x

1. 1.2288 Gbit/s SRIO link rates can be supported with internal divide options using a 245.76 MHz S_CLK_2 clock frequency
2. S_CLK_2 is only required to be present when 3.072 Gbit/s and either 1.2288 Gbit/s or 2.4576 Gbit/s link rates are required in the same application. If these line rates are not required, S_CLK_2 can be left unconnected.

All bit or register settings which apply to 1.25, 2.5, or 3.125 Gbit/s also apply to the line rates of 1.2288, 2.4576, and 3.0720 Gbit/s with the reduced S_CLK_1 and S_CLK_2 frequencies. Refer to "Clocking and Reset" on page 64 for more clocking information.

A. Ordering Information

This appendix discusses ordering information for the Tsi568A.

A.1 Ordering Information

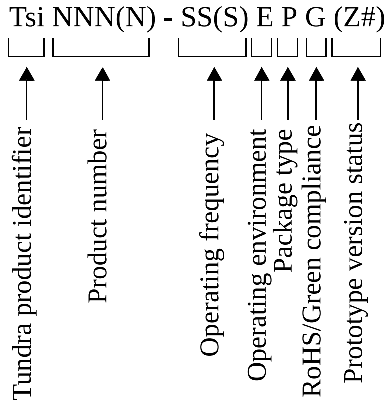
When ordering the Tsi568A, please refer to the device by its full part number as displayed in Table 24.

Table 24: Ordering Information

Part Number	Frequency	Temperature	Package	Pin Count
TSI568A-10GCL	1.25 - 3.125 Gbit/s	Commercial	FCBGA	675
TSI568A-10GCLY	1.25 - 3.125 Gbit/s	Commercial	FCBGA (RoHS)	675
TSI568A-10GIL	1.25 - 3.125 Gbit/s	Industrial	FCBGA	675
TSI568A-10GILY	1.25 - 3.125 Gbit/s	Industrial	FCBGA (RoHS)	675

A.2 Part Numbering Information

The Tundra part numbering system is explained as follows.



- ( ) – Indicates optional characters.
- Tsi – Tundra system interconnect product identifier. All Tundra semiconductor product numbers start with “Tsi.”
- NNNN – Product number (may be three or four digits)
- SS(S) – Maximum operating frequency of the fastest interface in MHz. If the speed of this interface exceeds 999 MHz then the number will be followed by a G, for GHz (for example, a 10-GHz part would be marked as 10G).
- E – Operating environment in which the product is guaranteed. This code may be one of the following characters:
    - C - Commercial temperature range (0 to +70°C)
    - I - Industrial temperature range (-40 to +85°C)
    - E - Extended temperature range (-55 to +125°C)
    - J - Junction rated temperature range (0 to 105°C)
    - K - Junction rated extended temperature range (-40 to 105°C)
- P – The Package type of the product:
    - B - Ceramic ball grid array (CBGA)
    - E - Plastic ball grid array (PBGA)
    - G - Ceramic pin grid array (CPGA)
    - J - Ultra ball grid array (EBGA), 1 mm pitch
    - K - Ultra ball grid array (EBGA), 1.27 mm pitch
    - L - Plastic ball grid array (PBGA), 1 mm pitch

  - M - Small outline integrated circuit (SOIC)
  - Q - Plastic quad flatpack

- G – Tundra products fit into three RoHS-compliance categories:
  - Y - RoHS Compliant (6of6) – These products contain none of the six restricted substances above the limits set in the EU Directive 2002/95/EC.
  - Y - RoHS Compliant (Flip Chip) – These products contain only one of the six restricted substances: Lead (Pb). These flip-chip products are RoHS compliant through the Lead exemption for Flip Chip technology, Commission Decision 2005/747/EC, which allows Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages.
  - V - RoHS Compliant/Green - These products follow the above definitions for RoHS Compliance and are denoted as Green as they contain no Halogens.
- Z# – Prototype version status (optional). If a product is released as a prototype then a “Z” is added to the end of the part number. Further revisions to the prototype prior to production release would add a sequential numeric digit. For example, the first prototype version of device would have a “Z,” a second version would have “Z1,” and so on. The prototype version code is dropped once the product reaches production status.