

REVISIONS

| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
|-----|---|-----------------|----------------|
| A | Update boilerplate to MIL-PRF-38535 requirements. Editorial changes throughout. – jak | 03-06-11 | Thomas M. Hess |
| B | Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG | 10-02-12 | Thomas M. Hess |

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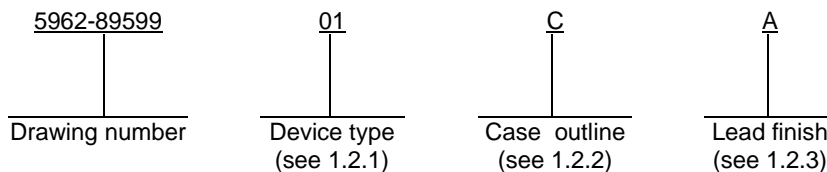
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| REV STATUS | REV | B | B | B | B | B | B | B | B | B | B | B | B | B | B | | |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | | | |

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| PMIC N/A | PREPARED BY Tim H. Noh | <p align="center">DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dsccl.dla.mil</p> | | | | | | | | | | | | | | |
| <p align="center">STANDARD MICROCIRCUIT DRAWING</p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p> | CHECKED BY Ray Monnin | | | | | | | | | | | | | | | |
| | APPROVED BY Michael A. Frye | <p align="center">MICROCIRCUIT, DIGITAL, ADVANCED CMOS, 8-INPUT MULTIPLEXER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON</p> | | | | | | | | | | | | | | |
| | DRAWING APPROVAL DATE 89-04-25 | | | | | | | | | | | | | | | |
| | REVISION LEVEL B | | <table border="1"> <tr> <td>SIZE A</td> <td>CAGE CODE 67268</td> <td>5962-89599</td> </tr> </table> | SIZE A | CAGE CODE 67268 | 5962-89599 | | | | | | | | | | |
| SIZE A | CAGE CODE 67268 | 5962-89599 | | | | | | | | | | | | | | |
| | | SHEET | 1 OF 12 | | | | | | | | | | | | | |

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

| <u>Device type</u> | <u>Generic number</u> | <u>Circuit function</u> |
|--------------------|-----------------------|--|
| 01 | 54ACT251 | 8-input multiplexer with three-state outputs, TTL compatible inputs |

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| <u>Outline letter</u> | <u>Descriptive designator</u> | <u>Terminals</u> | <u>Package style</u> |
|-----------------------|-------------------------------|------------------|-----------------------|
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line |
| F | GDFP2-F16 or CDFP3-F16 | 16 | Flat pack |
| 2 | CQCC1-N20 | 20 | Leadless-chip-carrier |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/ 2/

| | |
|--|----------------------------------|
| Supply voltage range (V_{CC}) | -0.5 V dc to +6.0 V dc |
| DC input voltage range (V_{IN}) | -0.5 V dc to $V_{CC} + 0.5$ V dc |
| DC output voltage range (V_{OUT}) | -0.5 V dc to $V_{CC} + 0.5$ V dc |
| Clamp diode current (I_{IK}, I_{OK}) | ± 20 mA |
| DC output current (per pin) (I_{OUT}) | ± 50 mA |
| DC V_{CC} or GND current | ± 100 mA |
| Storage temperature range (T_{STG}) | -65°C to +150°C |
| Maximum power dissipation (P_D) | 500 mW |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case (θ_{JC}) | See MIL-STD-1835 |
| Junction temperature (T_J) | +175°C <u>3/</u> |

1.4 Recommended operating conditions. 2/

| | |
|--|---------------------------------------|
| Supply voltage range (V_{CC}) | +4.5 V dc minimum to 5.5 V dc maximum |
| Input voltage range (V_{IN}) | 0.0 V dc to V_{CC} |
| Output voltage range (V_{OUT}) | 0.0 V dc to V_{CC} |
| Case operating temperature range (T_C) | -55°C to +125°C |
| Input rise or fall times: | |
| $V_{CC} = 4.5$ V | 0.0 to 24 ns (10-90%, 10 ns) |
| $V_{CC} = 5.5$ V | 0.0 to 20 ns (10-90%, 8 ns) |

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise specified, all voltages are referenced to ground.

3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE A | | 5962-89599 |
| | | REVISION LEVEL B | SHEET 2 |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at <http://www.jedec.org> or from Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

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| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE A | | 5962-89599 |
| | | REVISION LEVEL B | SHEET 3 |

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE A | | 5962-89599 |
| | | REVISION LEVEL B | SHEET 4 |

TABLE I. Electrical performance characteristics.

| Test and MIL-STD-883 test method <u>1/</u> | Symbol | Test conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified | | Group A subgroups | Limits <u>2/</u> | | Unit |
|--|-------------------------------|--|-------------------------|-------------------|------------------|-------|------|
| | | | | | Min | Max | |
| High-level output voltage 3006 | V _{OH} <u>3/</u> | V _{IN} = V _{IH} = 2.0 V min or V _{IL} = 0.8 V max I _{OH} = -50 μA | V _{CC} = 4.5 V | 1, 2, 3 | 4.4 | | V |
| | | | V _{CC} = 5.5 V | | 5.4 | | |
| | | V _{IN} = V _{IH} = 2.0 V min or V _{IL} = 0.8 V max I _{OH} = -24 mA | V _{CC} = 4.5 V | | 3.7 | | |
| | | | V _{CC} = 5.5 V | | 4.7 | | |
| V _{IN} = V _{IH} = 2.0 V min or V _{IL} = 0.8 V max I _{OH} = -50 mA | V _{CC} = 5.5 V | 3.85 | | | | | |
| Low-level output voltage 3007 | V _{OL} <u>3/</u> | V _{IN} = V _{IH} = 2.0 V min or V _{IL} = 0.8 V max I _{OL} = 50 μA | V _{CC} = 4.5 V | 1, 2, 3 | | 0.1 | V |
| | | | V _{CC} = 5.5 V | | | 0.1 | |
| | | V _{IN} = V _{IH} = 2.0 V min or V _{IL} = 0.8 V max I _{OL} = 24 mA | V _{CC} = 4.5 V | | | 0.5 | |
| | | | V _{CC} = 5.5 V | | | 0.5 | |
| V _{IN} = V _{IH} = 2.0 V min or V _{IL} = 0.8 V max I _{OL} = 50 mA | V _{CC} = 5.5 V | | 1.65 | | | | |
| High-level input voltage | V _{IH} | | V _{CC} = 4.5 V | 1, 2, 3 | 2.0 | | V |
| | | | V _{CC} = 5.5 V | | 2.0 | | |
| Low-level input voltage | V _{IL} | | V _{CC} = 4.5 V | 1, 2, 3 | | 0.8 | V |
| | | | V _{CC} = 5.5 V | | | 0.8 | |
| Input leakage current low 3009 | I _{IL} <u>4/</u> | V _{IN} = 0.0 V | V _{CC} = 5.5 V | 1, 2, 3 | | -1.0 | μA |
| Input leakage current high 3010 | I _{IH} <u>4/</u> | V _{IN} = 5.5 V | V _{CC} = 5.5 V | 1, 2, 3 | | 1.0 | |
| Quiescent supply current 3005 | I _{CCCH} | V _{IN} = V _{CC} or GND V _{CC} = 5.5 V | | 1, 2, 3 | | 160 | μA |
| | I _{CCCL} | | | | | 160 | |
| | I _{CCZ} | | | | | 160 | |
| Quiescent supply current delta, TTL input levels 3005 | ΔI _{CC} <u>5/</u> | V _{CC} = 5.5 V For input under test V _{IN} = V _{CC} - 2.1 V For all other inputs V _{IN} = V _{CC} or GND | | 1, 2, 3 | | 1.6 | mA |
| Three-state output leakage current high 3021 | I _{OZH} | V _{IN} = V _{CC} or GND V _{CC} = 5.5 V V _{OUT} = 5.5 V or 0.0 V | | 1, 2, 3 | | 10.0 | μA |
| Three-state output leakage current low 3020 | I _{OZL} | | | | | -10.0 | |
| Input capacitance 3012 | C _{IN} | See 4.3.1c | | 4 | | 8.0 | pF |
| Power dissipation capacitance 3012 | C _{PD} <u>6/</u> | See 4.3.1c | | 4 | | 110.0 | pF |
| Functional tests 3014 | | Tested at V _{CC} = 4.5 V and repeated at V _{CC} = 5.5 V, See 4.4.3d | | 7, 8 | L | H | |

See footnotes at end of table.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
B

5962-89599
SHEET
5

TABLE I. Electrical performance characteristics – Continued.

| Test and MIL-STD-883 test method <u>1/</u> | Symbol | Test conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified | Group A subgroups | Limits <u>2/</u> | | Unit |
|--|--------------------------------|---|-------------------|------------------|------|------|
| | | | | Min | Max | |
| Propagation delay time, In to Z 3003 | t _{PHL1} <u>7/</u> | V _{CC} = 4.5 V C _L = 50 pF R _L = 500Ω See figure 4 | 9 | 1.0 | 11.5 | ns |
| | | | 10, 11 | 1.0 | 13.5 | |
| | t _{PLH1} <u>7/</u> | | 9 | 1.0 | 11.5 | |
| | | | 10, 11 | 1.0 | 13.5 | |
| Propagation delay time, In to \bar{Z} 3003 | t _{PHL2} <u>7/</u> | | 9 | 1.0 | 12.5 | |
| | | | 10, 11 | 1.0 | 15.0 | |
| | t _{PLH2} <u>7/</u> | | 9 | 1.0 | 12.0 | |
| | | | 10, 11 | 1.0 | 14.0 | |
| Propagation delay time, S _n to Z 3003 | t _{PHL3} <u>7/</u> | 9 | 1.0 | 14.5 | | |
| | | 10, 11 | 1.0 | 18.0 | | |
| | t _{PLH3} <u>7/</u> | 9 | 1.0 | 14.5 | | |
| | | 10, 11 | 1.0 | 18.0 | | |
| Propagation delay time, S _n to \bar{Z} 3003 | t _{PHL4} <u>7/</u> | 9 | 1.0 | 15.5 | | |
| | | 10, 11 | 1.0 | 19.5 | | |
| | t _{PLH4} <u>7/</u> | 9 | 1.0 | 14.5 | | |
| | | 10, 11 | 1.0 | 18.5 | | |
| Propagation delay time, output enable, \overline{OE} to Z 3003 | t _{PZH1} <u>7/</u> | 9 | 1.0 | 8.5 | | |
| | | 10, 11 | 1.0 | 10.0 | | |
| | t _{PZL1} <u>7/</u> | 9 | 1.0 | 8.0 | | |
| | | 10, 11 | 1.0 | 9.5 | | |
| Propagation delay time, output disable, \overline{OE} to Z 3003 | t _{PHZ1} <u>7/</u> | 9 | 1.0 | 11.0 | | |
| | | 10, 11 | 1.0 | 12.5 | | |
| | t _{PLZ1} <u>7/</u> | 9 | 1.0 | 8.5 | | |
| | | 10, 11 | 1.0 | 9.5 | | |
| Propagation delay time, output enable, \overline{OE} to \bar{Z} 3003 | t _{PZH2} <u>7/</u> | 9 | 1.0 | 8.5 | | |
| | | 10, 11 | 1.0 | 10.0 | | |
| | t _{PZL2} <u>7/</u> | 9 | 1.0 | 8.5 | | |
| | | 10, 11 | 1.0 | 10.0 | | |
| Propagation delay time, output disable, \overline{OE} to \bar{Z} 3003 | t _{PHZ2} <u>7/</u> | 9 | 1.0 | 12.0 | | |
| | | 10, 11 | 1.0 | 13.5 | | |
| | t _{PLZ2} <u>7/</u> | 9 | 1.0 | 7.5 | | |
| | | 10, 11 | 1.0 | 8.5 | | |

1/ For tests not listed in the referenced MIL-STD-883 (e.g. C_{PD}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

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| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE A | | 5962-89599 |
| | | REVISION LEVEL B | SHEET 6 |

TABLE I. Electrical performance characteristics – Continued.

- 3/ V_{OH} and V_{OL} shall be tested at $V_{CC} = 4.5$ V. V_{OH} and V_{OL} are guaranteed, if not tested, for $V_{CC} = 5.5$ V. Limits shown apply to operation at $V_{CC} = 5.0$ V ± 0.5 V. Transmission driving tests are performed at $V_{CC} = 5.5$ V with a 2 ms duration maximum.
- 4/ V_{IH} and V_{IL} tests are not required, and shall be applied as forcing functions for V_{OH} and V_{OL} tests.
- 5/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limits are equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.
- 6/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$. The dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P_D and I_S , n is the number of device inputs at TTL levels, f is the frequency of the input signal, and d is the duty cycle of the input signal.
- 7/ AC limits at $V_{CC} = 5.5$ V are equal to limits at $V_{CC} = 4.5$ V and guaranteed by testing at $V_{CC} = 4.5$ V. The minimum ac limits are guaranteed for $V_{CC} = 5.5$ V by guardbanding the $V_{CC} = 4.5$ V limits to 1.5 ns, minimum.

| Device type | 01 | |
|-----------------|-----------------|-----------------|
| Case outlines | E and F | 2 |
| Terminal number | Terminal symbol | |
| 1 | I3 | NC |
| 2 | I2 | I3 |
| 3 | I1 | I2 |
| 4 | I0 | I1 |
| 5 | Z | I0 |
| 6 | \bar{Z} | NC |
| 7 | \overline{OE} | Z |
| 8 | GND | \bar{Z} |
| 9 | S2 | \overline{OE} |
| 10 | S1 | GND |
| 11 | S0 | NC |
| 12 | I7 | S2 |
| 13 | I6 | S1 |
| 14 | I5 | S0 |
| 15 | I4 | I7 |
| 16 | V_{CC} | NC |
| 17 | --- | I6 |
| 18 | --- | I5 |
| 19 | --- | I4 |
| 20 | --- | V_{CC} |

NC = No internal connection

FIGURE 1. Terminal connections.

| | | | |
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| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE A | | 5962-89599 |
| | | REVISION LEVEL B | SHEET 7 |

| Inputs | | | | Outputs | |
|-----------------|----|----|----|-----------------|----|
| \overline{OE} | S2 | S1 | S0 | \overline{Z} | Z |
| H | X | X | X | Z | Z |
| L | L | L | L | $\overline{I0}$ | I0 |
| L | L | L | H | $\overline{I1}$ | I1 |
| L | L | H | L | $\overline{I2}$ | I2 |
| L | L | H | H | $\overline{I3}$ | I3 |
| L | H | L | L | $\overline{I4}$ | I4 |
| L | H | L | H | $\overline{I5}$ | I5 |
| L | H | H | L | $\overline{I6}$ | I6 |
| L | H | H | H | $\overline{I7}$ | I7 |

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedance

FIGURE 2. Truth table.

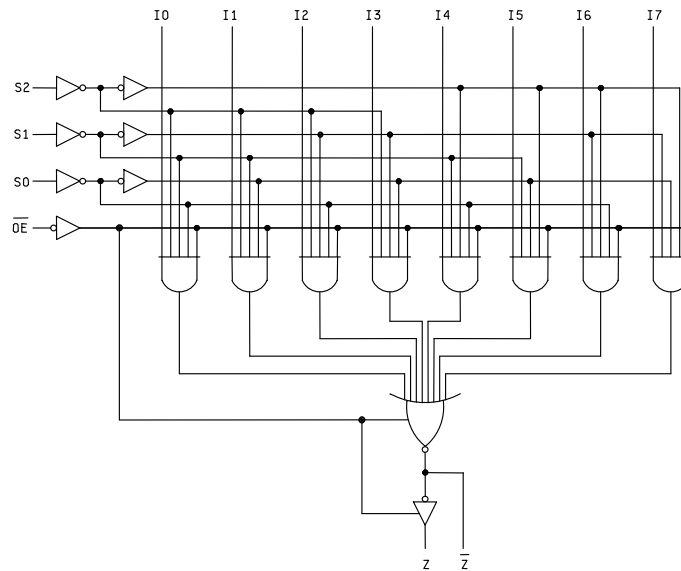


FIGURE 3. Logic diagram.

**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-89599

REVISION LEVEL
B

SHEET
8

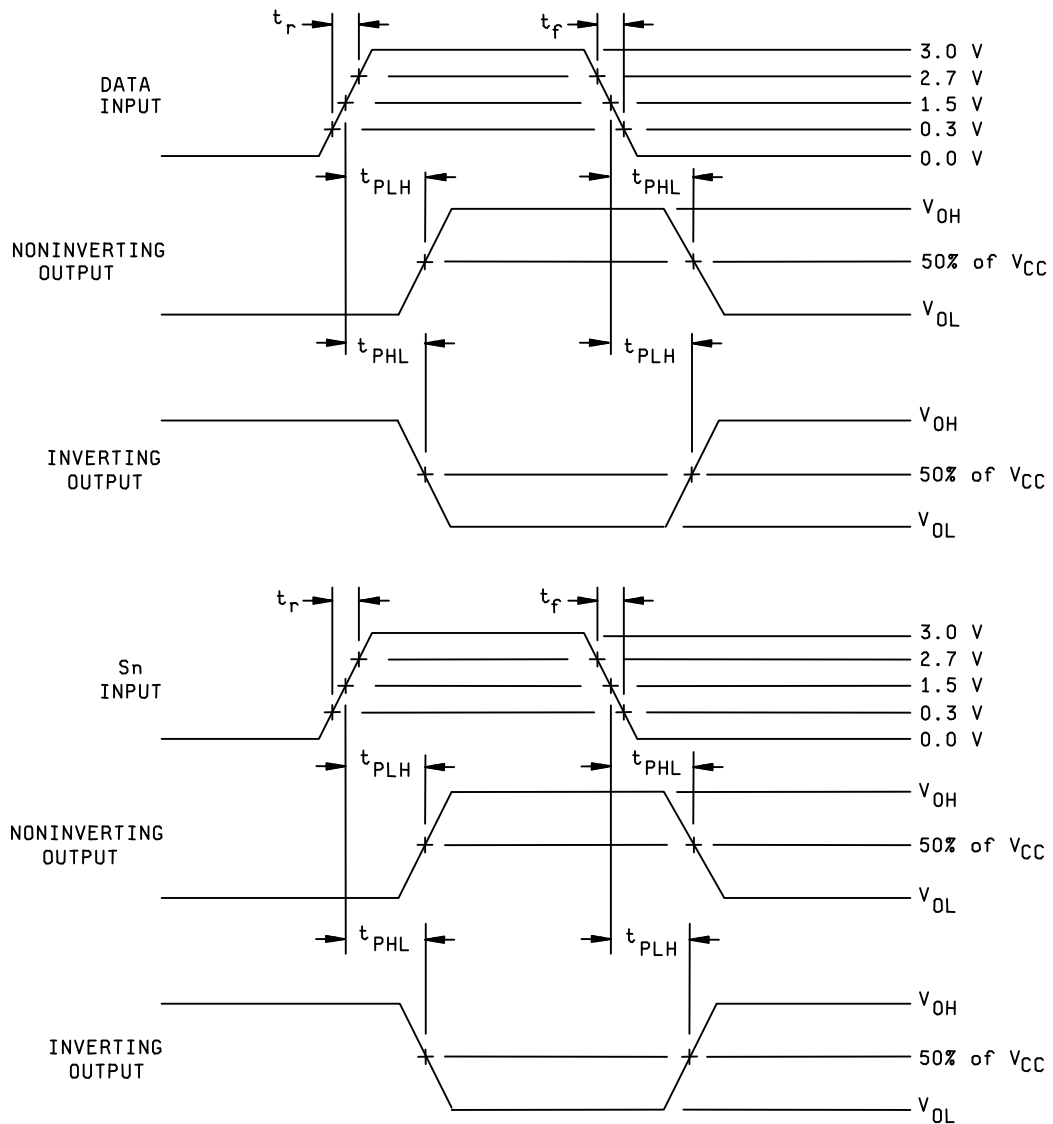


FIGURE 4. Switching waveforms and test circuit.

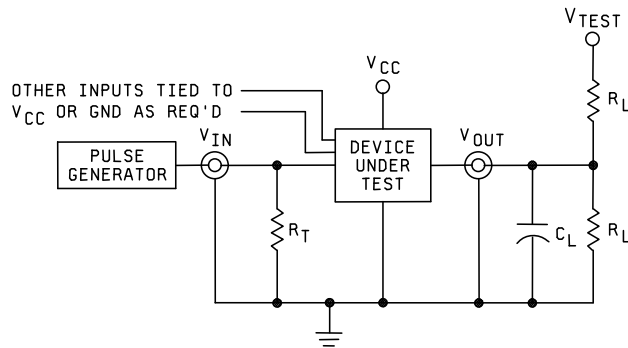
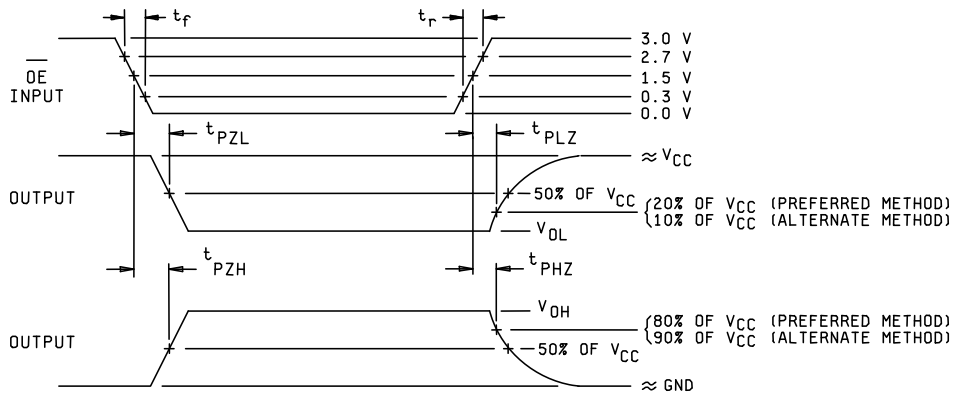
**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-89599

REVISION LEVEL
B

SHEET
9



NOTES:

1. Preferred method:
 When measuring t_{PHZ} and t_{PZH} : $V_{TEST} = GND$
 When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$
 When measuring t_{PLH} and t_{PHL} : $V_{TEST} = open$
 Alternate method:
 When measuring t_{PLZ} and t_{PZL} : $V_{TEST} = 2 \times V_{CC}$
 When measuring t_{PHZ} , t_{PZH} , t_{PLH} , and t_{PHL} : $V_{TEST} = open$
2. $C_L = 50 \text{ pF}$ minimum or equivalent (includes test jig and probe capacitance).
3. $R_T = 50\Omega$ or equivalent. $R_L = 500\Omega$ or equivalent.
4. Input signal from pulse generator: $V_{IN} = 0.0 \text{ V}$ to 3.0 V ; $PRR \leq 10 \text{ MHz}$; $t_r \leq 3 \text{ ns}$; $t_f \leq 3 \text{ ns}$; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V , respectively; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. Outputs are measured one at a time with one output per measurement.

FIGURE 4. Switching waveforms and test circuit – Continued.

| | | | |
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| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE A | | 5962-89599 |
| | | REVISION LEVEL B | SHEET 10 |

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) |
|--|---|
| Interim electrical parameters (method 5004) | ---- |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3 |

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2.

| | | | |
|---|------------------|----------------------------|--------------------|
| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE A | | 5962-89599 |
| | | REVISION LEVEL B | SHEET 11 |

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

| | | | |
|---|------------------|----------------------------|--------------------|
| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE A | | 5962-89599 |
| | | REVISION LEVEL B | SHEET 12 |

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-02-12

Approved sources of supply for SMD 5962-89599 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

| Standard microcircuit drawing PIN <u>1/</u> | Vendor CAGE number | Vendor similar PIN <u>2/</u> |
|---|--------------------|------------------------------|
| 5962-8959901EA | 0C7V7 | 54ACT251DMQB |
| 5962-8959901FA | 0C7V7 | 54ACT251FMQB |
| 5962-89599012A | 0C7V7 | 54ACT251LMQB |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

0C7V7

Vendor name and address

QP Semiconductor
2945 Oakmead Village Court
Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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