COMX-P4080 COM Express Module

Installation and Use

P/N: 6806800L20C

August 2014

ARTESYN™

EMBEDDED TECHNOLOGIES

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About this Manual

Overview of Contents

This manual is divided into the following chapters and appendices:

- *Safety Notes* summarizes the safety instructions in the manual.
- *Sicherheitshinweise* is a German translation of the Safety Notes chapter.
- *Introduction* gives an overview of the features of the product, standard compliances, mechanical data, ordering information, and board identification.
- *Hardware Preparation and Installation* outlines the installation requirements, hardware accessories, switch settings, and installation procedures.
- *Controls, LEDs, and Connectors* describes external interfaces of the board. This includes connectors and LEDs.
- *Functional Description* includes a block diagram and functional description of major components of the product.
- *Maps and Registers* provides details on the various registers and addresses used in the product.
- *Operating System and Driver Support* lists the drivers and operating systems supported by the product.
- *BSP Operations* provides information on the board support package that accomplishes most of the product's debugging operations.
- *Firmware Upgrade* lists the procedures on updating the product's firmware.
- *Related Documentation* provides a listing of related product documentation, manufacturer's documents, and industry standard specifications.

Abbreviations

This document uses the following abbreviations:

Abbreviation	Definition
A/D	Analog/Digital
ANSI	American National Standard Institute
ASIC	Application Specific Integrated Circuit
BGA	Ball Grid Array
BLT	Block Transfer
COM	Communications
COP	Common On-chip Processor
COTS	Commercial-Off-the-Shelf
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DDR	Double Data Rate
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DUART	Dual Universal Asynchronous Receiver/Transmitter
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
EPROM	Erasable Programmable Read-Only Memory
FCC	Federal Communications Commission
FEC	Fast Ethernet Controller
FIFO	First In First Out
F/W	Firmware
FPBGA	Flip Chip Plastic Ball Grid Array
GB	GigaBytes
Gbit	Gigabit

Abbreviation	Definition
Gbps	Gigabits Per Second
GMII	Gigabit Media Independent Interface
GPR	General Purpose Register
H/W	Hardware
ID	Identification
I/O	Input/Output
IEEE	Institute of Electrical and Electronics Engineers
I2C	Inter IC
JTAG	Joint Test Access Group
KB	KiloBytes
KBAUD	Kilo Baud
LBC	Local Bus Controller
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LFM	Linear Feet per Minute
LSB	Least Significant Byte
MB	MegaBytes
Mbit	Megabit
MBLT	Multiplexed Block Transfer
Mbps	Megabits Per Second
MHz	Megahertz
MII	Media Independent Interface
MSB	Most Significant Byte
Msb	Most Significant Bit
MTBF	Mean Time Between Failure
OS	Operating System
PBGA	Plastic Ball Grid Array
PCI	Peripheral Component Interconnect

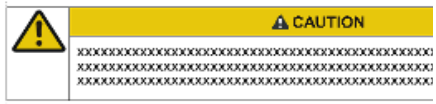
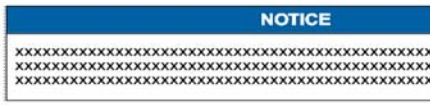
Abbreviation	Definition
PCI-X	Peripheral Component Interconnect -X
PIC	Programmable Interrupt Controller
PIM	PCI Mezzanine Card Input/Output Module
PMC	PCI Mezzanine Card (IEEE P1386.1)
PLD	Programmable Logic Device
PLL	Phase-Locked Loop
POR	Power-On Reset
PRD	Product Requirements Document
PReP	PowerPC Reference Platform
QUART	Quad Universal Asynchronous Receiver/Transmitter
RAM	Random Access Memory
Rcv	Receive
RGMII	Reduced Gigabit Media Independent Interface
ROM	Read-Only Memory
RTBI	Reduced Ten Bit Interface
RTC	Real-Time Clock
RTM	Rear Transition Module
SBC	Single Board Computer
SDRAM	Synchronous Dynamic Random Access Memory
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SMT	Surface Mount Technology
SODIMM	Small-Outline Dual In-line Memory Module
SPD	Serial Presence Detect
SRAM	Static Random Access Memory
SRIO	Serial Rapid I/O
S/W	Software

Abbreviation	Definition
USB	Universal Serial Bus
VIO	Input/Output Voltage
VPD	Vital Product Data
XAUI	10 Gigabit Attachment Unit Interface

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR

Notation	Description
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

The table below lists all the revisions implemented in this manual.

Part Number	Publication Date	Description
6806800L20C	August 2014	Re-branded to Artesyn.
6806800L20B	May 2011	• Added *COM Express Connector* on page 44. • Implemented editorial changes.
6806800L20A	January 2011	GA Version. Added Chapter 7, *BSP Operations*.

Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Artesyn Embedded Technologies intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Artesyn representative.

The product has been designed to meet the standard industrial safety requirements. It must only be used in its specific area of office telecommunication industry, industrial control, and development. It must not be used in safety critical components, life supporting devices or on aircraft.

Only personnel trained by Artesyn or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product. The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel is allowed to remove equipment covers for internal subassembly or component replacement or any internal adjustment.

This product operates with dangerous voltages that can cause injury or death. Use extreme caution when handling, testing, and adjusting this equipment and its components.

Operation

Product Damage
High humidity and condensation on surfaces cause short circuits.
Do not operate the product outside the specified environmental limits. Make sure the product is completely dry and there is no moisture on any surface before applying power.

Installation

Damage of Circuits
Electrostatic discharge and incorrect installation and removal of the product can damage circuits or shorten their life.
Before touching the product make sure that your are working in an ESD-safe environment or wear an ESD wrist strap or ESD shoes. Hold the product by its edges and do not touch any components or circuits.

Damage of the Product and Additional Devices and Modules
Incorrect installation or removal of additional devices or modules damages the product or the additional devices or modules.
Before installing or removing additional devices or modules, read the respective documentation and use appropriate tools.

Pin Damage
Forcing the module into the system may damage connector pins.
If the module stops responding during insertion, pull it out and try again.

Environment

Environmental Damage
Improper disposal of used products may harm the environment.
Always dispose of used products according to your country's legislation and manufacturer's instructions.

Sicherheitshinweise

This section provides a German translation of the Safety Notes.

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Systems innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am System zur Folge haben.

Artesyn Embedded Technologies ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem System in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem System um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Artesyn.

Das Produkt erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie, im Zusammenhang mit Industriesteuerungen und in der Entwicklung verwendet werden. Es darf nicht in sicherheitskritischen Anwendungen, lebenserhaltenden Geräten oder in Flugzeugen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Artesyn ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Systems fern. Entfernen Sie auf keinen Fall die Systemabdeckung. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf die Systemabdeckung entfernen, um Systemkomponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am System durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Artesyn. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

Artesyn und unsere Zulieferer unternehmen größte Anstrengungen um sicherzustellen, dass sich Pins und Stecker von Boards vor dem Verlassen der Produktionsstätte in einwandfreiem Zustand befinden. Verbogene Pins, verursacht durch fehlerhafte Installation oder durch Installation von Boards mit beschädigten Steckern kann die durch Artesyn gewährte Garantie für Boards und Backplanes erlöschen lassen.

Dieses Produkt wird mit gefährlichen Spannungen betrieben, die zu Verletzungen und Tod führen können. Seien Sie im Umgang mit dem Produkt und beim Testen und Anpassen des Produktes und seiner Komponenten äußerst vorsichtig.

Betrieb

Beschädigung des Systems
Hohe Luftfeuchtigkeit und Kondensat auf den Oberflächen der Produkte kann zu Kurzschlüssen führen.
Betreiben Sie die Produkte nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur und stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf den Produkten kein Kondensat befindet.

System Installation

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Produktes kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie das Produkt oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Beschädigung des Produktes und der Zusatzmodule
Fehlerhafter Ein- oder Ausbau von Zusatzmodulen führt zu Beschädigung des Produktes oder der Zusatzmodule.
Lesen Sie deshalb vor dem Ein- oder Ausbau von Zusatzmodulen die Dokumentation und benutzen Sie angemessenes Werkzeug.

Umweltschutz

Umweltverschmutzung
Falsche Entsorgung der Produkte schadet der Umwelt.
Entsorgen Sie alte Produkte gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.

1.1 Features

COMX-P4080 COM Express Module is based on the Freescale P4080 processor. COM Express is an industry-standard embedded computer module defined by PICMG.

The following table summarizes the features of COMX-P4080, including those of its variants.

Table 1-1 COMX-P4080 Features Summary

Function	Features
Form-factor	Basic (95 mm x 125 mm)
Processor	• Supports QorlQ P4080 integrated processor running at the speed of 1.5 GHz • Combines eight Power Architecture processor cores
Supported CPU	• P4080/P4040 • P5020/P5010 • P3041
Boot options	• 16-bits width NOR flash from local bus (default) • NAND flash from local bus • SPI flash • I2C EEPROM
Operating system	• Linux • VxWorks
Memory	• Dual DDR3 SDRAM slots (for P4080/P4040/P5020/P5010) • Supports up to 4 GB memory with ECC (for P4080/P4040/P5020/P5010) • For P3041: Single DDR3 slot, 2 GB memory with ECC
SERDES	• For P4080/P4040: 12 lanes of SERDES routed to the COM-E connectors, which can be configured as PCIE, XAUI, SRIO, and SGMII. • For P5020/P5010 and P3041: Two additional SATA interfaces routed through the COM-E connectors
UART	4 UART or 2 DUART
LAN	• P4080/P4040: One Gigabit ethernet port • P5020/P5010 and PP3041 Two Gigabit ethernet ports

Table 1-1 COMX-P4080 Features Summary (continued)

Function	Features
USB	• Four USB2.0 ports • P5020/P5010 and P3041: Eight USB ports
1588	1588 signals output to the COM-E connectors.
SATA	• P4080/P4040: No SATA ports • P5050/P5010 and P3041: Two SATA II ports
I2C	Total of three I2C buses
SPI	One SPI bus with four chip select signals
SDHC	Connected from the SDHC pins to the COM-E connectors
Tamper Detect	Connected from the tamper detect pins to the COM-E connectors
GPIO	Four GPIs and four GPOs routed to the COM-E connectors
RTC & WDT	On-board RTC and WDT device
Thermal sensor	Provides both remote and local thermal sensor
Debugger	• JTAG connector on module • connector on module
Power supply	• Power supplied to module from ATX-type power supply through COM-E connectors. • On-board regulators supply required voltages to devices on the module.

1.2 Standard Compliances

This product meets the following standards:

Table 1-2 Standard Compliances

Standard	Description
UL/CSA 60950-1 EN 60950-1 IEC 60950-1 CB Scheme	Legal safety requirements

Table 1-2 Standard Compliances

Standard	Description
FCC 47 CFR Part 15 Subpart B (US), Class A EN55022 Class A (EU) AS/NZS CISPR 22 Class A (Australia/New Zealand) VCCI Class A (Japan)	EMC requirements (legal) on system level (predefined Artesyn system)

Figure 1-1 Declaration of Conformity

EC Declaration of Conformity

According to EN 17050-1:2004

Manufacturer's Name:	Artesyn Embedded Technologies Embedded Computing
Manufacturer's Address:	Zhongshan General Carton Box Factory Co. Ltd. No 62, Qi Guan Road West, Shiqi District, 528400 Zhongshan City Guangdong, PRC

Declares that the following product, in accordance with the requirements of 2004/108/EC, 2006/95/EC, 2011/65/EU and their amending directives,

Product:	COMX-P4080—COM Express Form Factor Processor Pluggable Mezzanine Module
Model Name/Number:	COMX-P4080, COMX-P4080HP, COMX-P4080-HTSNK, COMX-P4080-4G-KIT

has been designed and manufactured to the following specifications:

EN55022:2006 (A1: 2007) Class A

EN55024: 1998 (A1: 2001 + A2: 2003)

IEC 60950-1: 2005 (2nd Edition) + A1: 2009

2011/65/EU RoHS Directive

As manufacturer we hereby declare that the product named above has been designed to comply with the relevant sections of the above referenced specifications. This product complies with the essential health and safety requirements of the above specified directives. We have an internal production control system that ensures compliance between the manufactured products and the technical documentation.

Tom Tuttle, Manager, Product Testing Services

07/30/2014
Date (MM/DD/YYYY)

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1.3 Mechanical Data

1.3.1 COMX-P4080 Mechanical Data

Figure 1-2 COMX-P4080 Mechanical Dimensions (Top and Side View)

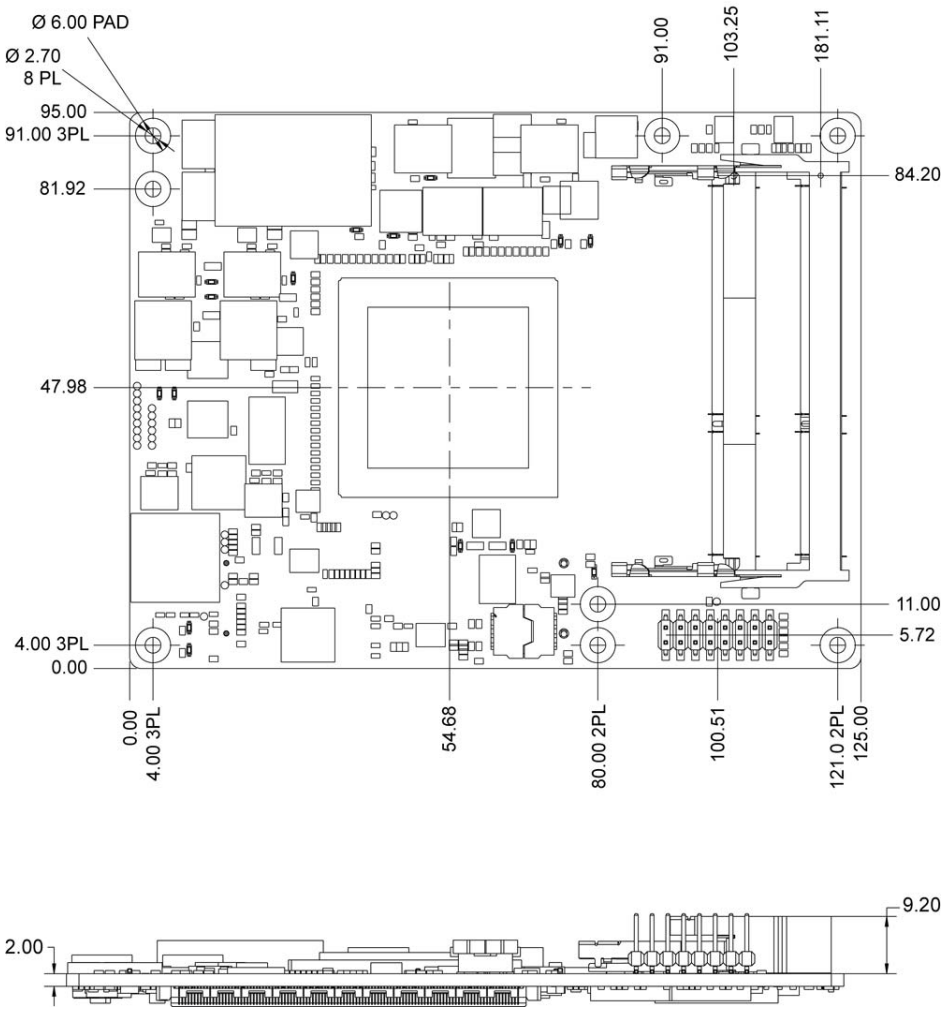


Table 1-3 Mechanical Data

Feature	Value
Dimensions	COM Express basic form factor: 95 mm x 125 mm
Weight	109.6 g

1.3.2 Heat Spreader Mechanical Data

Figure 1-3 Heat Spreader Mechanical Dimensions (Front and Side View)

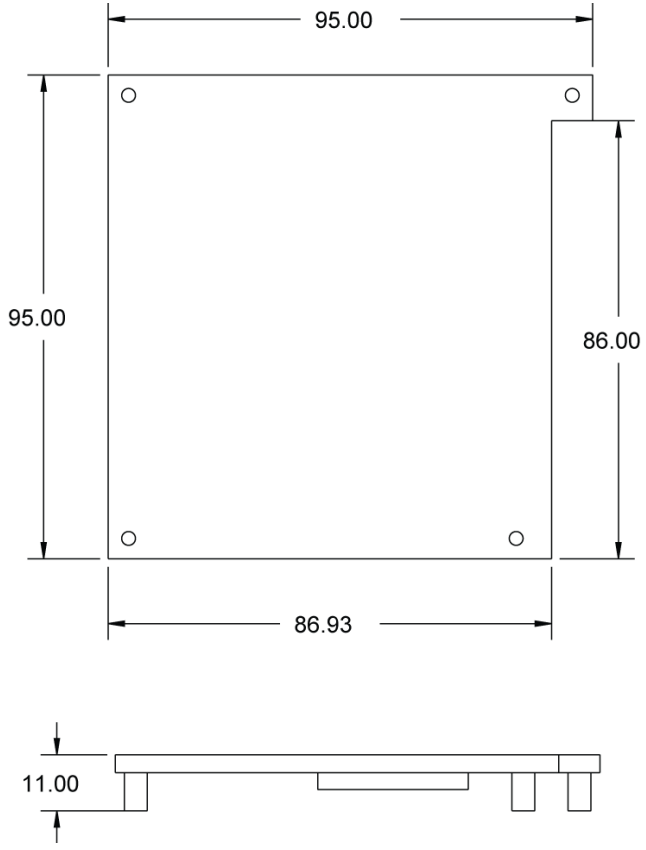
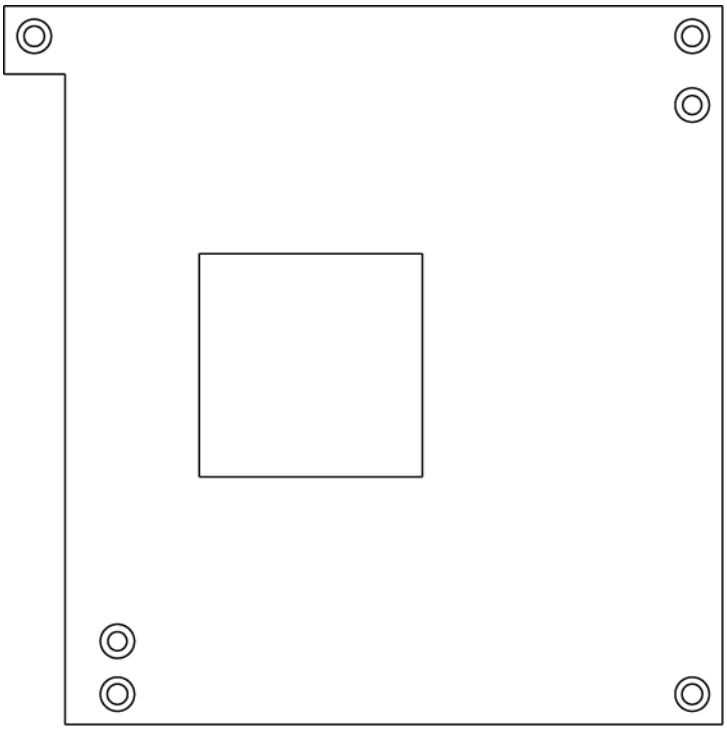


Figure 1-4 Heat Spreader Mechanical Illustration (Rear View)



1.3.3 Cooler Mechanical Data

Figure 1-5 Cooler Mechanical Dimensions (Front and Side View)

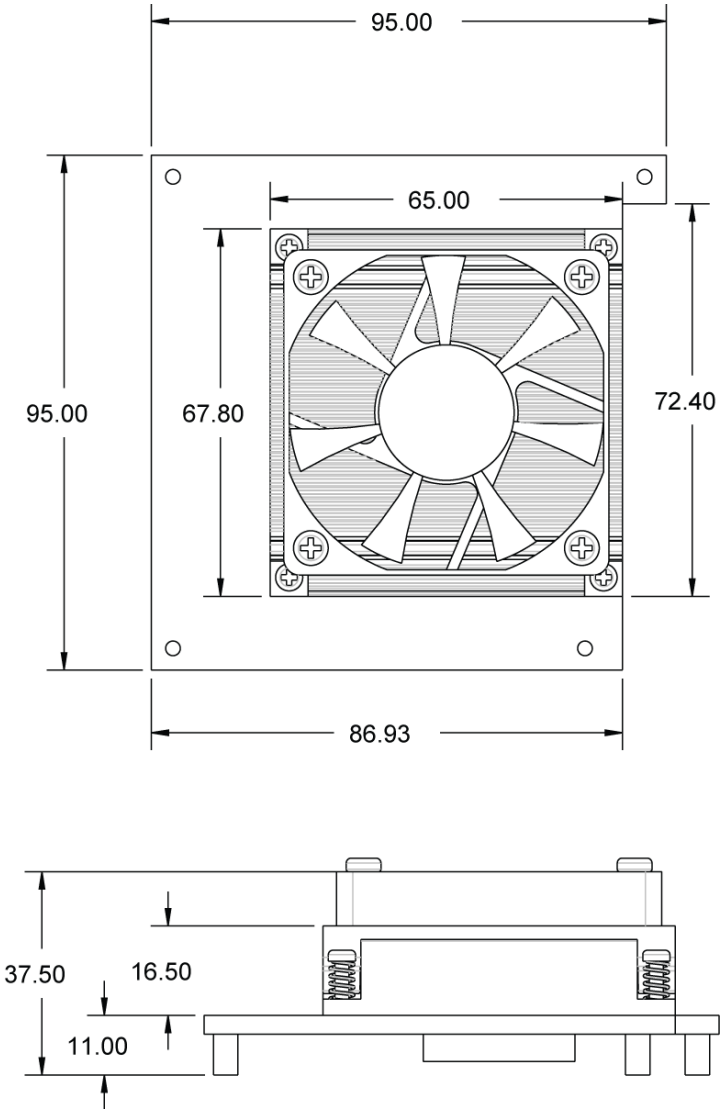
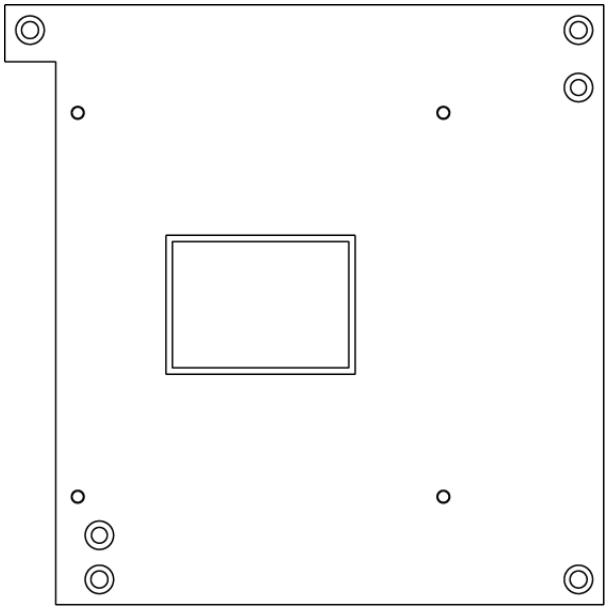


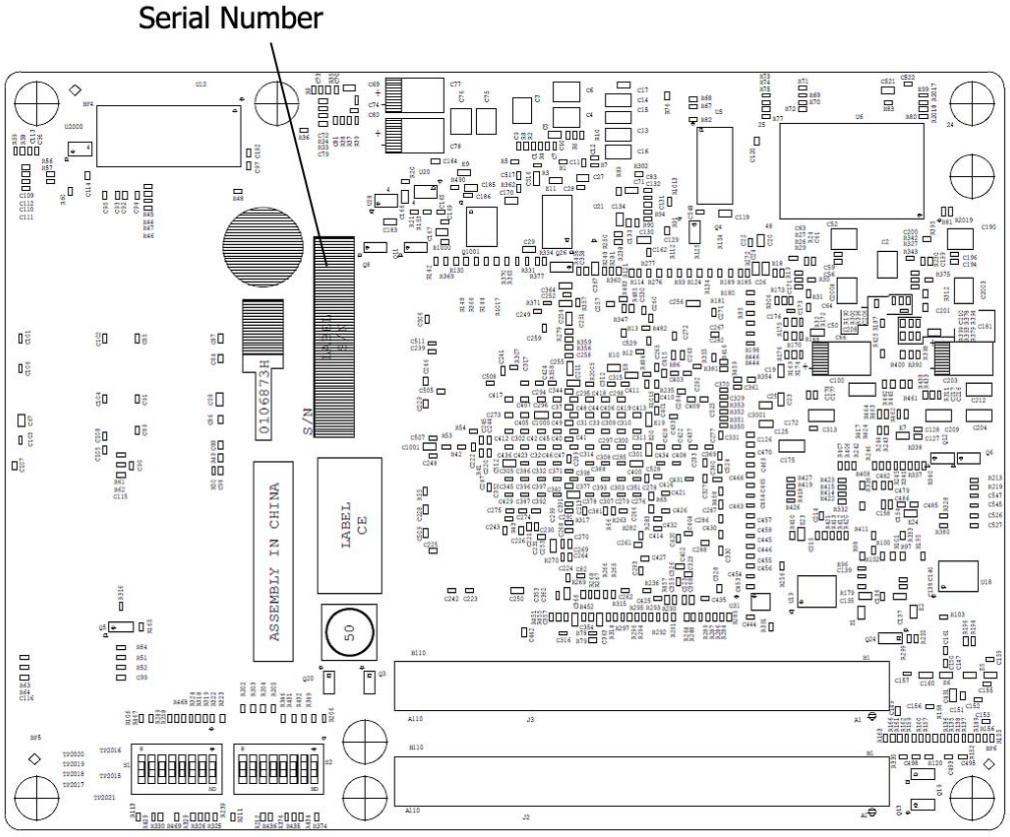
Figure 1-6 Cooler Mechanical Illustration (Rear View)



1.4 Board Identification

This section shows the serial number and its location on the board.

Figure 1-7 Serial Number Location



1.5 Ordering Information

1.5.1 Supported Board Models

The following table lists the product variants that are available upon release of this publication.

Table 1-4 Available Board Variants

Order Number	Description
COMX-P4080	COMX-P4080 COM Express module
COMX-P4080-4G-KIT	COMX-P4080 COM Express module, 4 GB memory, cooler

For availability of other variants, consult your local Artesyn sales representative.

1.5.2 Board Accessories

The following table lists the board accessories that are available upon release of this publication.

Table 1-5 Available Board Accessories

Order Number	Description
COMX-P4080-HSP	Heat spreader for COMX-P4080
COMX-P4080-HTSNK	Cooler for COMX-P4080

For availability of other board accessories, consult your local Artesyn sales representative.

2.1 Environmental and Power Requirements

2.1.1 Environmental Requirements

The following table lists the environmental requirements that the board must meet when operated in your particular system configuration.

Operating temperatures refer to the temperature of the air circulating around the board and not to the component temperature.

NOTICE

Product Damage:

- High humidity and condensation on surfaces cause short circuits.
- Do not operate the system outside the specified environmental limits. Make sure the product is completely dry and there is no moisture on any surface before applying power.

Table 2-1 Environmental Requirements

Requirement	Operating	Non-Operating
Cooling Method	Forced-air	
Temp Cycle Class	-40 to +85 °C:500cyc	
Temperature	0 to 55 °C	-40 to 85 °C
Humidity	10-90% (non-condensing)	
Vibration	0.01g^2/Hz @ 5-500 Hz	
Shock	20 g 11 ms sine or saw	
Altitude	-60 to 4000 m ASL	

2.1.2 Thermal Requirements

The following table lists the critical temperature spots for the COMX-P4080 COM Express Module.

Table 2-2 Critical Temperature Spots for COMX-P4080

Component Identifier	Heat Dissipation Power (W)	Maximum Allowable Temperature (°C)
CPU-P4080	27 W	Tjmax = 105

Contact your Artesyn sales representative for current information on the detailed thermal information including airflow and resistance of the module.

NOTICE

System Overheating

- Cooling Vents
  Improper cooling can lead to system damage and can void the manufacturer's warranty.
- To ensure proper cooling and undisturbed airflow through the system, do not obstruct the ventilation openings of the system. Make sure that the fresh air supply is not mixed with hot exhaust from other devices.

⚠ CAUTION

Personal Injury

- During operation, hot surfaces may be present on the heat sinks and the components of the product.
- To prevent injury from hot surface do not touch any of the exposed components or heatsinks on the product when handing. Use the handle and face plate, where applicable, or the board edge when removing the product from the enclosure.

2.2 Unpacking and Inspecting the Module

NOTICE

Damage of Circuits

- Electrostatic discharge and incorrect installation and removal of the product can damage circuits or shorten its life.
- Before touching the product make sure that you are working in an ESD-safe environment or wearing an ESD wrist strap or ESD shoes. Hold the product by its edges and do not touch any components or circuits.

Shipment Inspection

1. Verify that you have received all items of your shipment:
   - Printed *Quick Start Guide* and *Safety Notes*
   - COMX-P4080 COM Express Module
2. Check for damage and report any damage or differences to customer service.
3. Remove the desiccant bag shipped together with the product.

NOTICE

Environmental Damage

- Improperly disposing of used products may harm the environment.
- Always dispose of used products according to your country's legislation and manufacturer's instructions.

2.3 Preparing the Installation Environment

Before you install or replace components, pay attention to the following:

- Wear an ESD-preventive wrist strap to prevent the static electricity from damaging the device.
- Keep the area where the components reside clean and keep the components away from heat-generating devices, such as radiator.
- Ensure that your sleeves are tightened or rolled up above the elbow. For safety purposes, it is not recommended to wear jewelry, watch, glasses with metal frames, or clothes with metal buttons.
- Do not exert too much force, or insert or remove the components forcibly. Avoid damage to the components or plug-ins.
- Confirm the feasibility of the operation
  Spare parts of components are available in the equipment warehouse. If available spare parts are lacking, contact Artesyn Embedded Technologies for timely assistance. Visit http://www.artesyn.com/computing for more details.

  Make sure that the new components are in good condition and without defects such as oxidation, chemical corrosion, missing components or transportation damage. Read this document to familiarize yourself with the proper installation and replacement procedures of the component, as well as to master the skills required by the operation.
- Check the environment
  Make sure that the power supply, temperature, and humidity meet the operating requirements for the board and its components. For details, refer to the respective system documentation.
- Prepare the parts and the tools
  Prepare the components to be installed or replaced. Use the special antistatic package when holding or transporting the components. Prepare the cross screwdriver, screws, plastic supports, cooling gel, and ESD-preventive wrist strap.
- Confirm installation or changing position
  Confirm the position where COMX-P4080 COM Express Module will be installed.
- If a serious problem occurs and cannot be solved when you install or replace the component, contact Artesyn Embedded Technologies for technical support.

2.4 Installing and Removing the Memory Module

There is one 204 pin SODIMM slot on the COMX-P4080 COM Express Module.

NOTICE

Pin Damage

- Forcing the module into the system may damage connector pins.
- If the module hangs during insertion, pull it out and insert it again.

Installing a Memory Module

1. Wear the ESD-preventive wrist strap.
2. Lay the COM-E module where the SODIMM is to be installed on the antistatic desktop.
3. Check the thermal pad found in a separate package of the heat spreader/cooler pack. Tear off the pad protection paper from one side and adhere it on the center of the PCB module, between the bottom memory socket and the processor. The thermal pad for the bottom memory is necessary if they will operate with a 100% loading under 55° C ambient temperature. The thermal pad is optional otherwise.
4. Take the SODIMM out of the antistatic package, holding it by the edges.

If only one memory module is going to be installed, it is recommended to install the memory module on the lower memory slot.

5. Line up the notch located on the row of the metal pins at the bottom of the module with the key in the SODIMM slot on the COM-E module.
6. Insert the SODIMM in a slantwise position or at a 45-degree angle to slide the memory module into place.

7. Press down on the memory module against the COM-E module until you hear it snap into place. The module must be properly aligned before you press it down into its final position. You can remove the module from the socket and reinstall it if you cannot press it down into its final position.

Removing a Memory Module

1. Wear the ESD-preventive wrist strap.
2. Release the module from the slot by pushing the spring latches on either side of the module outward.
3. Lift the module from the COM-E Module.

NOTICE

Damage of the Product and Additional Devices and Modules

- Incorrect installation or removal of additional devices or modules damages the product or the additional devices or modules.
- Before installing or removing additional devices or modules, read the respective documentation and use appropriate tools.

2.5 Installing and Removing the Heat Spreader/Cooler

Installing the Heat Spreader/Cooler

1. Check the thermal interface material pads on the heat spreader/cooler. Make sure the pads are aligned to their corresponding components on the COMX-P4080 COM Express Module.
2. Align the standoffs of the heat spreader/cooler with the screw holes on the COMX-P4080 COM Express Module.

3. Hold the heat spreader/cooler and COMX-P4080 COM Express Module.
4. From the backside of the COM Express module, use two pieces of M2.5*6mm screws to fasten the module assembly to the heat spreader/cooler through the two internal mounting holes.

Removing the Heat Spreader/Cooler

1. Loosen the two pieces of screws from the backside COMX-P4080 COM Express Module.
2. While holding the edges, pull the heat spreader/cooler from the COMX-P4080 COM Express Module.

2.6 Installing and Removing the Module on the Carrier Board

The assembled COM Express module with the attached heat spreader is attached to a carrier board.

Installing the COM Express Module on the Carrier Board

1. Line up the board-to-board connector of the module assembly with the board-to-board connector of the carrier board.
2. Make sure that the interconnectors are properly aligned and that the six carrier standoffs have contact with the bottom of the module board.
3. From the topside of the module assembly, locate the screw holes on the heat spreader/cooler and module.
4. Use the M2.5*18mm screws to fasten the COMX-P4080 COM Express Module assembly to the carrier board.

Removing the COM Express Module from the Carrier Board

1. From the topside of the module assembly, locate the six screws that connect the module assembly to the carrier board.
2. Loosen and remove the screws.
3. While holding the edges, pull the COMX-P4080 COM Express Module from the carrier board.

3.1 Board Layout

Figure 3-1 COMX-P4080 COM Express Module Components

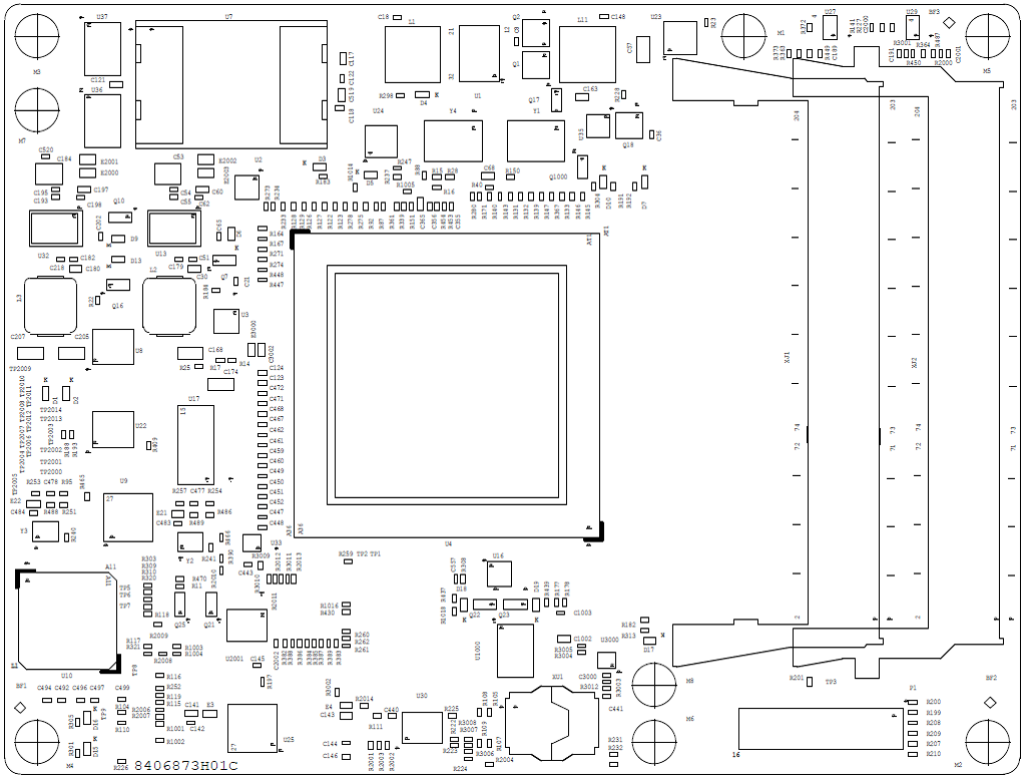
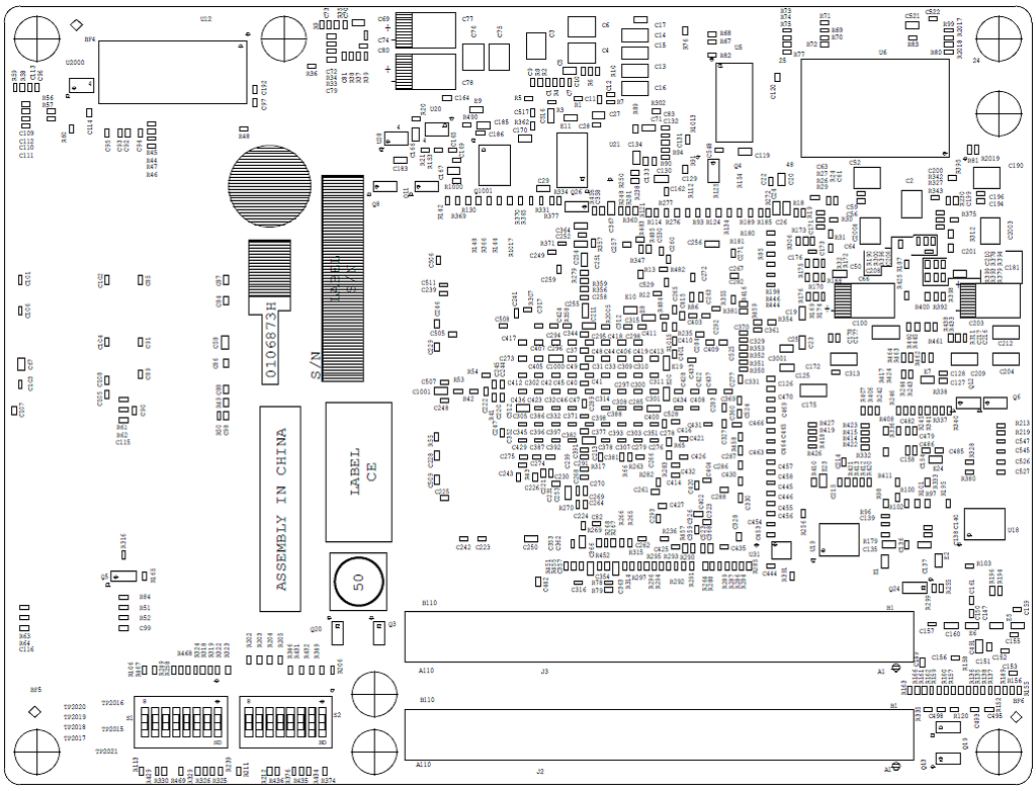


Figure 3-2 COMX-P4080 COM Express Module Components (Rear View)



3.2 Connectors and Switches

3.2.1 COM Express Connector

The following two tables provide the pin out for the Freescale type COM-E module.

The first column shows the default signal names while the succeeding columns show the differences in values.

Table 3-1 COM Express Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	GND	B1	GND	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	GBE1_ACT#	D2	GBE2_ACT#
A3	GBE0_MDI3+	B3	1588_CLK_OUT	C3	GBE1_MDI3-	D3	GBE2_MDI3-
A4	GBE0_LINK100#	B4	1588_PULSE_OUT1	C4	GBE1_MDI3+	D4	GBE2_MDI3+
A5	GBE0_LINK1000#	B5	1588_PULSE_OUT2	C5	GBE1_LINK100#	D5	GBE2_LINK100#
A6	GBE0_MDI2-	B6	1588_ALARM_OUT1	C6	GBE1_MDI2-	D6	GBE2_MDI2-
A7	GBE0_MDI2+	B7	1588_ALARM_OUT2	C7	GBE1_MDI2+	D7	GBE2_MDI2+
A8	GBE0_LINK#	B8	1588_TRIG_IN1	C8	GBE1_LINK1000#	D8	GBE2_LINK1000#
A9	GBE0_MDI1-	B9	1588_TRIG_IN2	C9	GBE1_MDI1-	D9	GBE2_MDI1-
A10	GBE0_MDI1+	B10	1588_CLK_IN	C10	GBE1_MDI1+	D10	GBE2_MDI1+
A11	GND	B11	GND	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	GBE1_MDI0-	D12	GBE2_MDI0-
A13	GBE0_MDI0+	B13	SMB_CK	C13	GBE1_MDI0+	D13	GBE2_MDI0+
A14	GBE0_CTREF	B14	SMB_DAT	C14	GBE1_LINK#	D14	GBE2_LINK#
A15	SUS_S3#	B15	SMB_ALERT#	C15	DDI1_PAIR6+/RSVD/User Display	D15	IRQ_OUT_B
A16	SATA0_TX+	B16	SATA1_TX+	C16	DDI1_PAIR6-/RSVD/User Display	D16	IRQ00
A17	SATA0_TX-	B17	SATA1_TX-	C17	CE_PB12 / LGPL0	D17	CE_PA0 / LCLK0
A18	SUS_S4#	B18	SUS_STAT#	C18	CE_PB13 / LGPL1	D18	CE_PA1 / LCLK1
A19	SATA0_RX+	B19	SATA1_RX+	C19	SERDES_RX6+	D19	SERDES_TX6+
A20	SATA0_RX-	B20	SATA1_RX-	C20	SERDES_RX6-	D20	SERDES_TX6-
A21	GND	B21	GND	C21	GND	D21	GND
A22	SATA2_TX+	B22	SATA3_TX+	C22	SERDES_RX7+	D22	SERDES_TX7+
A23	SATA2_TX-	B23	SATA3_TX-	C23	SERDES_RX7-	D23	SERDES_TX7-

Table 3-1 COM Express Connector Pinout (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A24	SUS_S5#	B24	PWR_OK	C24	DDI1_HPD/RSVD/ User Display	D24	CE_PA2 / LCS0_B
A25	SATA2_RX+	B25	SATA3_RX+	C25	DDI1_PAIR4+/RSV D/User Display	D25	CE_PA3 / LCS1_B
A26	SATA2_RX-	B26	SATA3_RX-	C26	DDI1_PAIR4- /RSVD/User Display	D26	DDI1_PAIR0+/RSV D/User Display
A27	BATLOW#	B27	WDT	C27	DDI1_AUX+/RSVD/ User Display	D27	DDI1_PAIR0- /RSVD/User Display
A28	(S)ATA_ACT#	B28	AC/HAD_SDIN2	C28	DDI1_AUX- /RSVD/User Display	D28	CE_PB18 / LAD00
A29	AC/HAD_SYNC	B29	AC/HAD_SIN1	C29	DDI1_PAIR5+/RSV D/User Display	D29	DDI1_PAIR1+/RSV D/User Display
A30	AC/HAD_RST#	B30	AC/HAD_SIN0	C30	DDI1_PAIR5- /RSVD/User Display	D30	DDI1_PAIR1- /RSVD/User Display
A31	GND	B31	GND	C31	GND	D31	GND
A32	AC/HAD_BITCLK	B32	SPKR	C32	U0_TXD	D32	DDI1_PAIR2+/RSV D/User Display
A33	AC/HAD_SDOUT	B33	I2C_CK	C33	U0_RXD	D33	DDI1_PAIR2- /RSVD/User Display
A34	BIOS_DIS0#	B34	I2C_DAT	C34	U0_CTS	D34	CE_PB19 / LAD01
A35	THERMTRIP#	B35	THRM#	C35	U0_RTS	D35	CE_PB20 / LAD02
A36	USB6-	B36	USB7-	C36	U1_TXD	D36	DDI1_PAIR3+/RSV D/User Display
A37	USB6+	B37	USB7+	C37	U1_RXD	D37	DDI1_PAIR3- /RSVD/User Display
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	U1_CTS	D38	TDM_CLK_Tx0/SSI _TCK0/User Defined

Table 3-1 COM Express Connector Pinout (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A39	USB4-	B39	USB5-	C39	U1_RTS	D39	TDM_CLK_Rx0/SSI_RCK0/User Defined
A40	USB4+	B40	USB5+	C40	MDIO1 (clause 22)	D40	TDM_TxD0/SSI_TXD0/User Defined
A41	GND	B41	GND	C41	GND	D41	GND
A42	USB2-	B42	USB3-	C42	U2_TXD/User Defined	D42	TDM_RxD0/SSI_RXD0/User Defined
A43	USB2+	B43	USB3+	C43	U2_RXD/User Defined	D43	TDM_TxFS0/SSI_TFS0/User Defined
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	U2_CTS/User Defined	D44	TDM_RxFS0/SSI_RFS0/User Defined
A45	USB0-	B45	USB1-	C45	U2_RTS/User Defined	D45	SSI_TCK1/TDM_CLK_Tx1/User Defined
A46	USB0+	B46	USB1+	C46	U3_TXD/User Defined	D46	SSI_RCK1/TDM_CLK_Rx1/User Defined
A47	VCC_RTC	B47	EXCD1_PERST#	C47	U3_RXD/User Defined	D47	SSI_TXD1/TDM_TxD1/User Defined
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	C48	U3_CTS/User Defined	D48	SSI_RXD1/TDM_RxD1/User Defined
A49	EXCD0_CPPE#	B49	SYS_RESET#	C49	U3_RTS/User Defined	D49	SSI_TFS1/TDM_TxFS1/User Defined
A50	LPC_SERIRQ	B50	CB_RESET#	C50	MDC1 (clause 22)	D50	SSI_RFS1/TDM_RxFS1/User Defined
A51	GND	B51	GND	C51	GND	D51	GND
A52	SERDES_TX5+	B52	SERDES_RX5+	C52	SERDES_RX16+	D52	SERDES_TX16+
A53	SERDES_TX5-	B53	SERDES_RX5-	C53	SERDES_RX16-	D53	SERDES_TX16-
A54	SD_DATA0	B54	SD_CMD	C54	TYPE0#	D54	TYPE3#
A55	SERDES_TX4+	B55	SERDES_RX4+	C55	SERDES_RX17+	D55	SERDES_TX17+
A56	SERDES_TX4-	B56	SERDES_RX4-	C56	SERDES_RX17-	D56	SERDES_TX17-

Table 3-1 COM Express Connector Pinout (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A57	GND	B57	SD_WP	C57	TYPE1#	D57	TYPE2#
A58	SERDES_TX3+	B58	SERDES_RX3+	C58	SERDES_RX18+	D58	SERDES_TX18+
A59	SERDES_TX3-	B59	SERDES_RX3-	C59	SERDES_RX18-	D59	SERDES_TX18-
A60	GND	B60	GND	C60	GND	D60	GND (FIXED)
A61	SERDES_TX2+	B61	SERDES_RX2+	C61	SERDES_RX19+	D61	SERDES_TX19+
A62	SERDES_TX2-	B62	SERDES_RX2-	C62	SERDES_RX19-	D62	SERDES_TX19-
A63	SD_DATA1	B63	SD_CD#	C63	MDIO2 (clause 22 or 45)	D63	MDC2 (Clause 45)
A64	SERDES_TX1+	B64	SERDES_RX1+	C64	GND	D64	LP_TAMPER_DET_ BAT
A65	SERDES_TX1-	B65	SERDES_RX1-	C65	SERDES_RX20+	D65	SERDES_TX20+
A66	GND	B66	WAKE0#	C66	SERDES_RX20-	D66	SERDES_TX20-
A67	SD_DATA2	B67	WAKE1#	C67	CE_PA12 / LAD00	D67	GND
A68	SERDES_TX0+	B68	SERDES_RX0+	C68	SERDES_RX21+	D68	SERDES_TX21+
A69	SERDES_TX0-	B69	SERDES_RX0-	C69	SERDES_RX21-	D69	SERDES_TX21-
A70	GND	B70	GND	C70	GND (FIXED)	D70	GND (FIXED)
A71	LVDS_A0+	B71	LVDS_B0+	C71	SERDES_RX22+	D71	SERDES_TX22+
A72	LVDS_A0-	B72	LVDS_B0-	C72	SERDES_RX22-	D72	SERDES_TX22-
A73	LVDS_A1+	B73	LVDS_B1+	C73	DDI1_CTRLDATA/R SVD/User Display	D73	DDI1_CTRLCLK/RS VD/User Display
A74	LVDS_A1-	B74	LVDS_B1-	C74	SERDES_RX23+	D74	SERDES_TX23+
A75	LVDS_A2+	B75	LVDS_B2+	C75	SERDES_RX23-	D75	SERDES_TX23-
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	LVDS_B3+	C77	CE_PA13 / LGPL2	D77	CE_PA14 / LWE0_B
A78	LVDS_A3+	B78	LVDS_B3-	C78	SERDES_RX24+	D78	SERDES_TX24+
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79	SERDES_RX24-	D79	SERDES_TX24-
A80	GND	B80	GND	C80	GND (FIXED)	D80	GND
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81	CE_PA15 / LGPL3	D81	CE_PA20

Table 3-1 COM Express Connector Pinout (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82	CE_PA16 / LGPL4	D82	CE_PA21
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	C83	IRQ01	D83	CE_PA18
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	SD_DATA3	B85	VCC_5V_SBY	C85	IRQ02	D85	CE_PA19
A86	KBD_RST#	B86	VCC_5V_SBY	C86	CE_PA17 / IRQ_IN3	D86	CE_PA24
A87	KBD_A20GATE	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	SERDES_CK_REF+	B88	SPI_CS1#	C88	CE_PA25 / GPI0	D88	CE_PA29 / GPO0
A89	SERDES_CK_REF-	B89	VGA_RED	C89	CE_PA26 / GPI1	D89	CE_PA30 / GPO1
A90	GND	B90	GND	C90	GND (FIXED)	D90	GND
A91	SPI_CS0#	B91	VGA_GRN	C91	CE_PA27 / GPI2	D91	CE_PA31 / GPO2
A92	SPI_MISO	B92	VGA_BLU	C92	CE_PA28 / GPI3	D92	CE_PB0
A93	SD_CLK	B93	VGA_HSYNC	C93	GND	D93	GND
A94	SPI_CLK	B94	VGA_VSYNC	C94	CE_PB1	D94	CE_PB8
A95	SPI_MOSI	B95	VGA_I2C_CK	C95	CE_PB2	D95	CE_PB9
A96	GND	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97	VCC_12V	B97	CE_PB31	C97	CE_PB3	D97	CE_PB21
A98	VCC_12V	B98	CE_PA22	C98	SP_CS2#	D98	CE_PB22
A99	VCC_12V	B99	CE_PA23	C99	SP_CS3#	D99	CE_PB23
A100	GND	B100	GND	C100	GND (FIXED)	D100	GND (FIXED)
A101	VCC_12V	B101	VCC_12V	C101	SGMII_CLK+	D101	CE_PB29
A102	VCC_12V	B102	VCC_12V	C102	SGMII_CLK-	D102	CE_PB30
A103	VCC_12V	B103	VCC_12V	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V

Table 3-1 COM Express Connector Pinout (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND	B110	GND	C110	GND	D110	GND

3.2.2 JTAG Connector Pinout

The following table details the JTAG connector pinout.

Table 3-2 JTAG Connector Pinout

Pin Number	Signal Name
1	TDO
2	NC
3	TDI
4	TRST
5	RUNSTOP
6	VDDSENSE
7	TCK
8	CKSTP INPUT
9	TMS
10	NC
11	SRST
12	NC
13	HRST
14	NC
15	CKSTP OUTPUT
16	GND

3.2.3 S1 Switch

COMX-P4080 has a bug which prevents SerDes Bank 1 and SerDes Bank 2 from using the same reference clock frequency.

For the SerDes configuration options 1, 2, 4, and 6, set sd_refclk1 as 100 MHz and sd_refclk2 as 125 MHz. For configuration options 3 and 5, set sd_refclk1 as 125 MHz and sd_refclk2 as 100 MHz.

Table 3-3 S1 Switch Settings

S1 Bit	Function	
1	Boot mode selection	ON: Secure boot mode
		OFF: Non-secure mode (Default)
2	Reference clock frequency of bank 1	ON: 125 MHz
		OFF: 100 MHz (Default)
3	Reference clock frequency of bank 2	ON: 100 MHz
		OFF: 125 MHz (Default)
4	Reference clock frequency of bank 3	ON: 100 MHz
		OFF: 125 MHz (Default)
5	RCW source selection between NOR and NAND flash	ON: NAND flash
		OFF: NOR flash (Default)
6	Not used	
7	GPI for debugging	ON: 1
		OFF: 0 (Default)
8	Local bus on carrier	ON: Enabled
		OFF: Disabled (Default)

3.2.4 S2 Switch

Table 3-4 S2 Switch Settings

S2.1~S2.5	RCW Source
OFF,ON,ON,OFF,ON	I2C1 normal addressing (supports ROMs up to 256 bytes)
OFF,ON,ON,OFF,OFF	I2C1 extended addressing
OFF,ON,OFF,OFF,ON	SPI 16-bit addressing
OFF,ON,OFF,OFF,OFF	SPI 24-bit addressing
OFF,OFF,ON,OFF,ON	eLBC FCM (NAND flash, 8-bit small page)
OFF,OFF,ON,OFF,OFF	eLBC FCM (NAND flash, 8-bit large page)
OFF,OFF,OFF,OFF,OFF	eLBC GPCM (NOR flash, 16-bit)
ON,X,X,X,X	Hard-coded RCW options
ON,ON,ON,OFF,ON	Large page NAND flash as boot location; USB2 and dual 4-pin UART enabled; Platform ratio of 8:1; Core PLL ratio of 14:1
ON,ON,ON,OFF,OFF	Large page NAND flash as boot location; RGMII FM1 MAC1 and dual 4-pin UART enabled; Platform ratio of 8:1; Core PLL ratio of 14:1
ON,ON,ON,ON,ON	16-bit NOR flash as boot location; USB2 and dual 4-pin UART enabled; Platform ratio of 8:1; Core PLL ratio of 14:1
ON,ON,ON,ON,OFF	16-bit NOR flash as boot location; RGMII FM1 MAC1 and dual 4-pin UART enabled; Platform ratio of 8:1; Core PLL ratio of 14:1
ON,ON,OFF,OFF,OFF	Three (x2, x2, x4) PCI-E @ 2.5G, 100 MHz ref clk, all agent mode; all cores in boot hold-off; dual 4-pin UART enabled
ON,ON,OFF,OFF,ON	Two (x4, x4) SRIO @ 2.5G, 100 MHz ref clk, all agent mode; all cores in boot hold-off; dual 4-pin UARTs enabled
ON,ON,OFF,ON,OFF	Large page NAND flash as boot location; USB2 and dual 4-pin UARTs enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,ON,OFF,ON,ON	Large page NAND flash as boot location; RGMII FM1 MAC1 and dual 4-pin UARTs enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,OFF,ON,OFF,OFF	16-bit NOR flash as boot location; RGMII FM1 MAC1 and dual 4-pin UARTs enabled; Platform ratio of 6:1; Core PLL ratio of 10:1

Table 3-4 S2 Switch Settings (continued)

S2.1~S2.5	RCW Source
ON,OFF,ON,OFF,ON	16-bit NOR flash as boot location; USB2 and dual 4-pin UARTs enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,OFF,ON,ON,OFF	Three (x2, x2, x4) PCIeX @ 2.5G, 100MHz ref clk, all agent mode; all cores in boot hold-off; dual 4-pin UARTs enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,OFF,ON,ON,ON	Two (x4, x4) SRIO @ 2.5G, 100MHz ref clk, all agent mode; all cores in boot hold-off; dual 4-pin UARTs enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,OFF,OFF,X,X	Reserved
S2.6	Card on the carrier
ON	SD card
OFF (Default)	Micro SD card
S2.7	SPI Flash Enable on module
ON	SPI flash disable on module
OFF	SPI flash enable on module
S2.8	
Not used	

3.3 On-board LEDs

3.3.1 System Status LEDs

Table 3-5 System Status LEDs

LED	Status
D17	Thermal issue
D18~D19	Debug LED 1~2
D3	System asleep

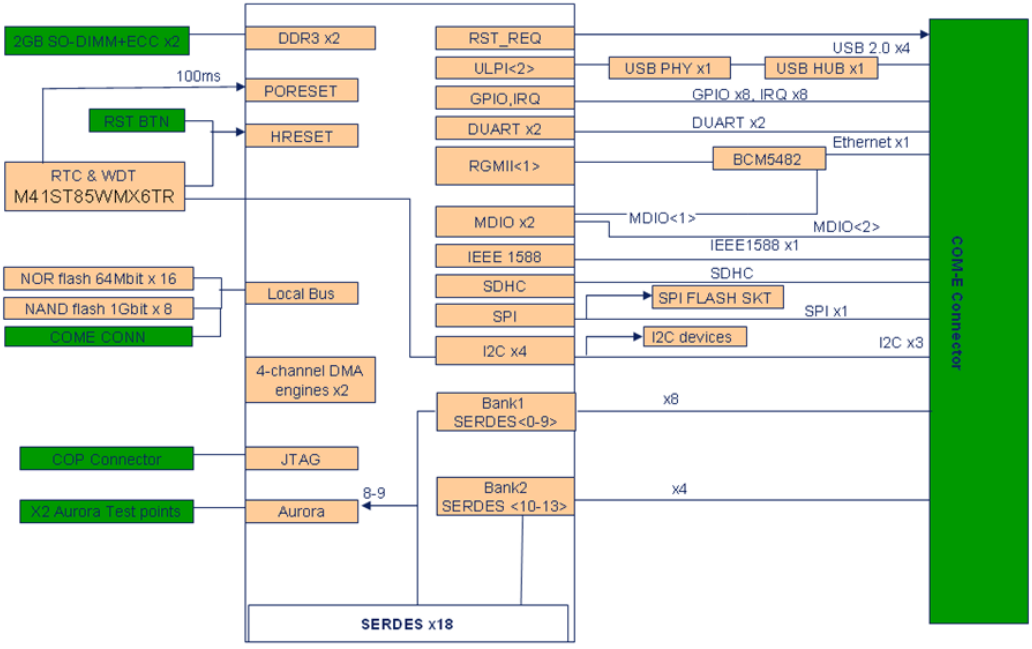
Table 3-5 System Status LEDs (continued)

LED	Status
D7	DDR3 power OK
D4	3.3 V power OK
D5	2.5 V power OK
D6	1.8 V power OK
D13	CORE power OK
D9	PLATFORM power OK
D10	1.5 V power OK
D1	USB hub 1 active
D2	USB hub 1 high speed
D15	USB hub 2 active
D16	USB hub 2 high speed

4.1 Block Diagram

The following image illustrates the block diagram of the COMX-P4080 COM Express Module.

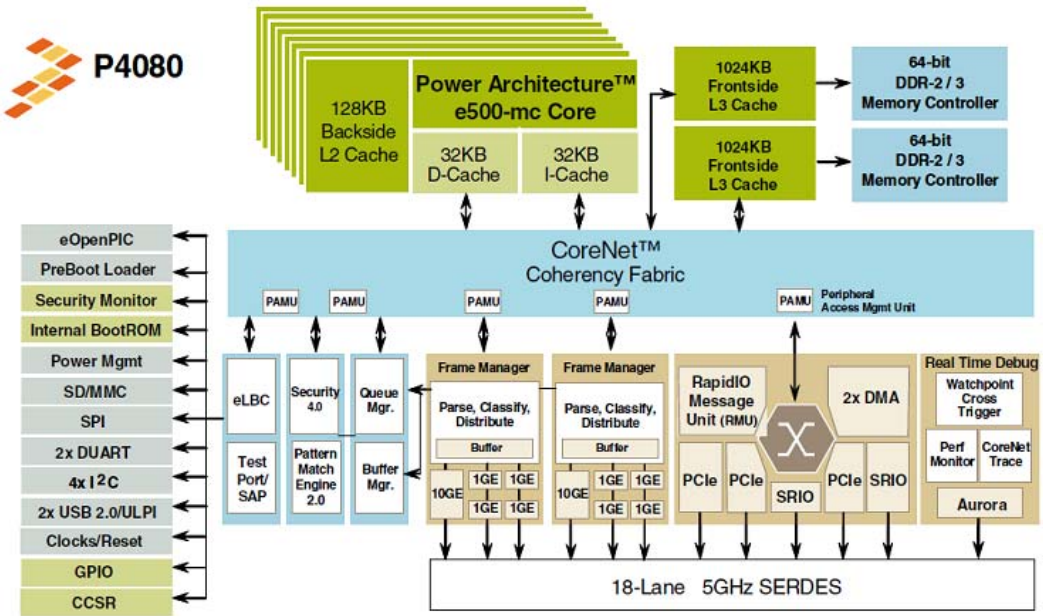
Figure 4-1 Block Diagram



4.2 Processor

The COMX-P4080 COM Express Module is based on the Freescale Power PC COMX-P4080 platform and supports the Qor1Q COMX-P4080 integrated processor. It can run at the speed of 1.5 GHz and is compatible with the P30 and P50 series. The QorIQ COMX-P4080 integrated communication processor combines eight Power Architecture ™ processor cores that allow high performance data path acceleration, logic and network, as well as peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure and military/aerospace applications.

Figure 4-2 COMX-P4080 Processor Block Diagram



4.3 Memory

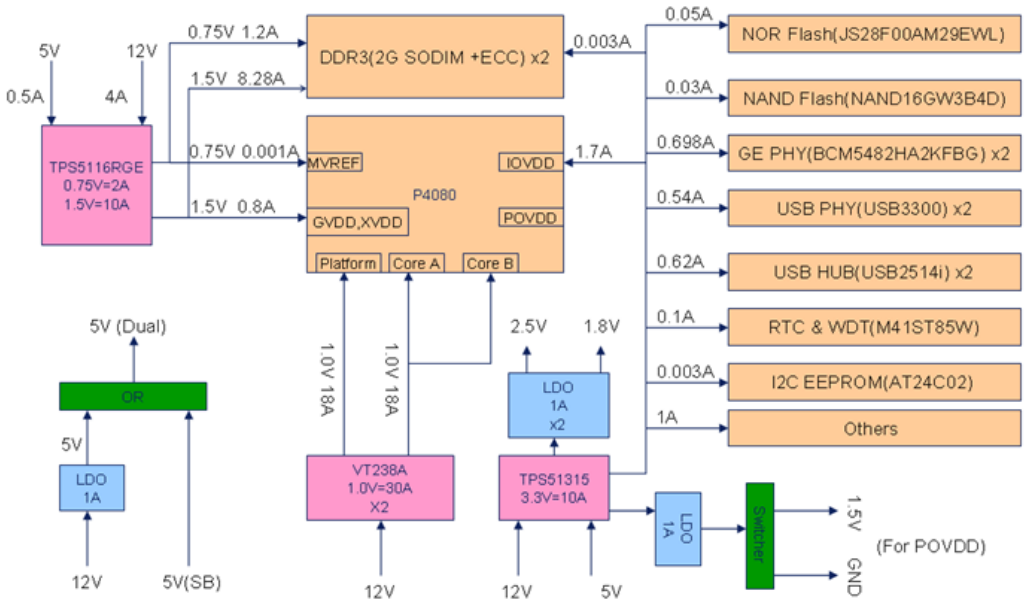
The COMX-P4080 COM Express Module supports up to 2-GB dual-rank DDR3 1066 MHz/1333 MHz ECC SO-UDIMM memory modules arranged in two ranks in one slot.

There are two 204-pin SO-UDIMM slots on the module measuring 5.2 mm high and 9.2 mm high, respectively. Both are placed on the same side of the PCB in consideration of thermal issues.

4.4 Power Supply

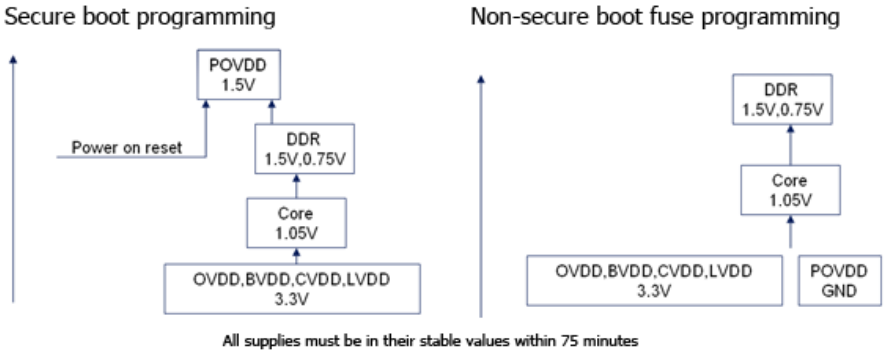
Power is supplied to the COMX-P4080 module from an ATX-type power supply through the COM-E connectors. On-board regulators supply the required voltages to devices attached to the module.

Figure 4-3 COMX-P4080 Power Tree



The power sequencing of the COMX-P4080 is different for the secure boot mode and the non-secure boot mode. For the secure boot mode, POVDD should be tied to 1.5 V DC and is powered at least 100 system clock cycles after the rising edge of power on reset signal. For non-secure boot mode, POVDD should be tied to GND. The following figure illustrates this process.

Figure 4-4 COMX-P4080 Power Sequencing



To set the boot mode, the first eight bits of the S1 switch are provided.

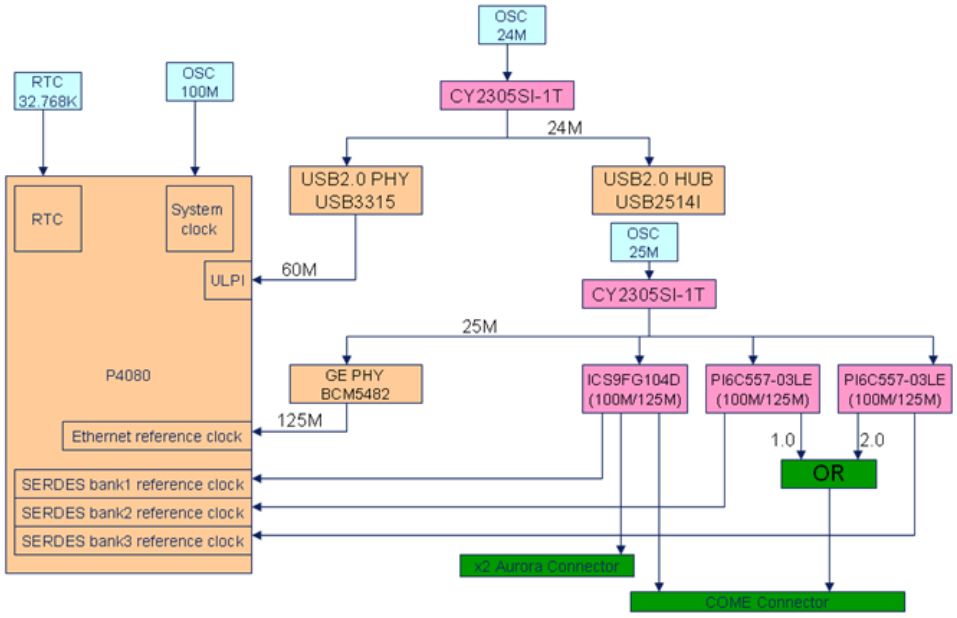
Table 4-1 COMX-P4080 Boot Mode Options

S1.1	RCW Source
ON	Secure boot mode
OFF (Default)	Non-secure boot mode

4.5 Clock Distribution

The COMX-P4080 needs several kinds of single-ended and different clocks for booting up and normal operation. The clock distribution list is illustrated below.

Figure 4-5 COMX-P4080 Clock Distribution



The frequency of the three SerDes banks' reference clocks can be set from 100 MHz to 125 MHz using the S1 switch.

Table 4-2 SerDes Clock Configuration by S1 Switch

SerDes Bank 1 Reference Clock	SerDes Bank 2 Reference Clock	SerDes Bank 3 Reference Clock
S1.2=ON, 125MHz	S1.3=ON, 100MHz	S1.4=ON, 100MHz
S1.2=OFF, 100MHz	S1.3=OFF, 125MHz	S1.4=OFF, 125MHz
Default:100MHz	Default:125MHz	Default:125MHz

It can also be set by three GPIOs.

Table 4-3 SerDes Clock Configuration by GPIO

SerDes Bank 1 Reference Clock	SerDes Bank 2 Reference Clock	SerDes Bank 3 Reference Clock
CPU_GPIO23=0, 100MHz	CPU_GPIO24=0, 100MHz	CPU_GPIO26=0, 100MHz
CPU_GPIO23=1, 125MHz	CPU_GPIO24=1, 125MHz	CPU_GPIO26=1, 125MHz
Default:100MHz	Default:125MHz	Default:125MHz

The setting of the S1 or GPIO depends on the protocols running at the SerDes lanes that belong to each bank. When the SerDes lanes are running at 3.125 Gbps, the corresponding bank reference clock should be set as 125 MHz. Any speed other than 3.125 Gbps should be set to 100 MHz. For example, if the lanes in bank 1 are configured as PCI-E, then the bank 1 reference clock should be set to 100 MHz. If it is set to XAUI, it should be at 125 MHz.

4.6 Boot Up Options

The COMX-P4080 supports several kinds of devices to load configuration information to the Reset Configuration Word (RCW) register, as well as devices in assisting the U-Boot codes to boot up the system. This includes NOR flash and NAND flash (both attached to the local bus), I2C, EEPROM, SPI flash and hardware strapping. The boot option is set by an 8-bit S2 switch. For more information, see the following table.

Table 4-4 RCW Source Location

S2.1 to S2.5	RCW Source
OFF,ON,ON,OFF,ON	I2C1 normal addressing (supports ROMs up to 256 Bytes)
OFF,ON,ON,OFF,OFF	I2C1 extended addressing
OFF,ON,OFF,OFF,ON	SPI 16-bit addressing
OFF,ON,OFF,OFF,OFF	SPI 24-bit addressing
OFF,OFF,ON,OFF,ON	eLBC FCM (NAND flash, 8-bit small page)
OFF,OFF,ON,OFF,OFF	eLBC FCM (NAND flash, 8-bit large page)
OFF,OFF,OFF,OFF,OFF (Default)	eLBC GPCM (NOR flash, 16-bit)
ON,X,X,X,X	Hard-coded RCW options

The "X" on the table indicates the "ON" or "OFF" state of the corresponding bits of the S2 switch.

Both NOR and NAND flash are attached to the local bus of the COMX-P4080. The chip select signal (CS) of the selected RCW source should be connected to the CS0 of the local bus. When set by the fifth bit of the S1 switch, neither the NOR or NAND flash can be selected as the RCW without properly setting the S1.5.

Table 4-5 Selecting RCW Sources Between NOR and NAND Flash

S1.5	RCW Source
ON	CS0 attached to NAND flash
OFF (Default)	CS0 attached to NOR flash

In cases where all the devices fail to work, hardware strapping can be picked as an option for loading the RCW. This is also useful for quick debugging purposes. The hard-code configuration details are shown the table below.

Table 4-6 RCW Hard-Coded Configuration Options

S2.1-S2.5	RCW hard-code configuration options
ON,ON,ON,OFF,ON	Large page NAND flash as boot location; USB2 and dual 4-pin UART enabled; Platform ratio of 8:1; Core PLL ratio of 14:1
ON,ON,ON,OFF,OFF	Large page NAND flash as boot location; RGMII FM1 MAC1 and dual 4-pin UART enabled; Platform ratio of 8:1; Core PLL ratio of 14:1
ON,ON,ON,ON,ON	16-bit NOR flash as boot location; USB2 and dual 4-pin UART enabled; Platform ratio of 8:1; Core PLL ratio of 14:1

Table 4-6 RCW Hard-Coded Configuration Options (continued)

S2.1-S2.5	RCW hard-code configuration options
ON,ON,ON,ON,OFF	16-bit NOR flash as boot location; RGMII FM1 MAC1 and dual 4-pin UART enabled; Platform ratio of 8:1; Core PLL ratio of 14:1
ON,ON,OFF,OFF,OFF	Three (x2, x2, x4) PCI-E @ 2.5G, 100 MHz ref clk, all agent mode; All cores in boot hold-off; Dual 4-pin UART enabled
ON,ON,OFF,OFF,ON	Two (x4, x4) SRIO @ 2.5G, 100 MHz ref clk, all agent mode; All cores in boot hold-off; Dual 4-pin UART enabled
ON,ON,OFF,ON,OFF	Large page NAND flash as boot location; USB2 and dual 4-pin UART enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,ON,OFF,ON,ON	Large page NAND flash as boot location; RGMII FM1 MAC1 and dual 4-pin UART enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,OFF,ON,OFF,OFF	16-bit NOR flash as boot location; USB2 and dual 4-pin UART enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,OFF,ON,OFF,ON	16-bit NOR flash as boot location; RGMII FM1 MAC1 and dual 4-pin UART enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,OFF,ON,ON,OFF	Three (x2, x2, x4) PCIeX @ 2.5G, 100MHz ref clk, all agent mode; All cores in boot hold-off; Dual 4-pin UART enabled; Platform ratio of 6:1 Core PLL ratio of 10:1;

Table 4-6 RCW Hard-Coded Configuration Options (continued)

S2.1-S2.5	RCW hard-code configuration options
ON,OFF,ON,ON,ON	Two (x4, x4) SRIO @ 2.5G, 100MHz ref clk, all agent mode; All cores in boot hold-off; Dual 4-pin UART enabled; Platform ratio of 6:1; Core PLL ratio of 10:1
ON,OFF,OFF,X,X	Reserved

As with Table "RCW Source Location" on page 60, the "X" on the table indicates the "ON" or "OFF" state of the corresponding bits of the S2 switch.

4.7 SerDes

The COMX-P4080 has three Serializer/Deserializer (SerDes) banks, including a total of 18 lanes. Twelve of these are routed to the COM-E connectors, defined as SERDES0 - SERDES7 (SERDES0-7 of bank 1), and SERDES16 - SERDES19 (SERDES10-13 of bank 2). SERDES8-SERDES9 of bank 1 are used for Aurora debugger . The four lanes of bank 3 are not used in COMX-P4080 and are reserved for the P30 and P50 series SATA interfaces.

The protocol running at each lanes that are routed to COM-E connectors are configured by the RCW. The following table shows the available options.

The U-Boot provides commands to change the configurations, allowing the user to select any of the twelve options available. In addition, the frequency of the reference clock for each bank should be properly configured based on the *Clock Distribution*.

The following table describes the distribution of SerDes lanes on the COMX-P4080.

Figure 4-6 SerDes Lanes Distribution

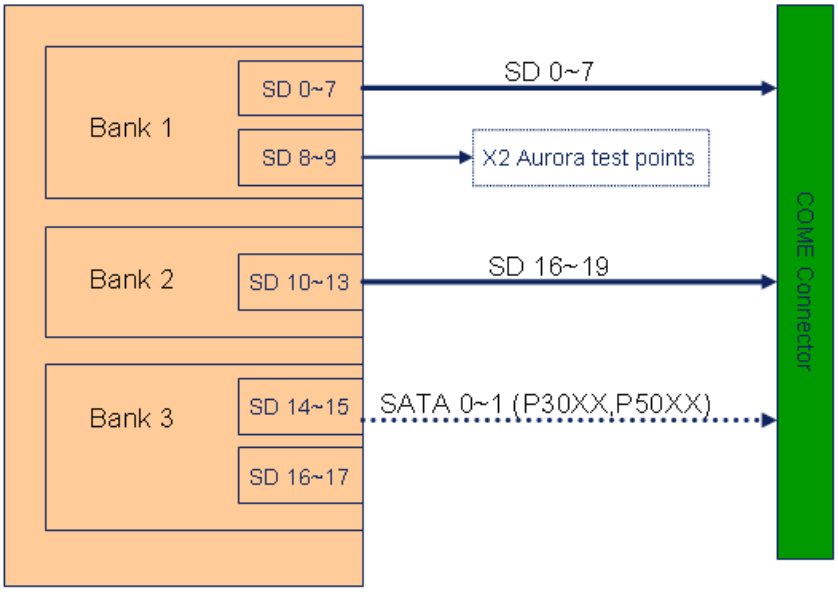


Table 4-7 SerDes Options When Routed to COM-E Connectors

Option	Bank 1 SerDes 0 ~ 3 (Slot J6)	Bank 1 SerDes 4 ~ 7 (Slot J14)	Bank 2 SerDes 10 ~ 13 (Slot J10)	S1.2 (Bank 1 RefClock)	S1.3/S1.4 (Bank 2/3 RefClock)
1	PEX1 x4 (2.5 Gbps)	PEX2 x4 (2.5 Gbps)	XAUI (3.125 Gbps)	OFF	OFF
2	PEX1 x4 (2.5 Gbps)	PEX2 x4 (5 Gbps)	XAUI (3.125 Gbps)	OFF	OFF
3	PEX1 x4 (5 Gbps)	PEX2 x4 (2.5 Gbps)	XAUI (3.125 Gbps)	OFF	OFF
4	PEX1 x4 (5 Gbps)	PEX2 x4 (5 Gbps)	XAUI (3.125 Gbps)	OFF	OFF
5	PEX1 x4 (2.5 Gbps)	SGMII x 4 (1.25 Gbps)	XAUI (3.125 Gbps)	OFF	OFF
6	PEX1 x4 (5 Gbps)	SGMII x 4 (1.25 Gbps)	XAUI (3.125 Gbps)	OFF	OFF
7	SRIO2 x4 (3.125 Gbps)	SRIO1 x4 (3.125 Gbps)	PEX3 x4 (2.5 Gbps)	ON	ON
8	SRIO2 x4 (3.125 Gbps)	SRIO1 x4 (3.125 Gbps)	PEX3 x4 (5 Gbps)	ON	ON
9	SRIO2 x4 (2.5 Gbps)	SRIO1 x4 (2.5 Gbps)	XAUI (3.125 Gbps)	OFF	OFF
10	SRIO2 x4 (3.125 Gbps)	SRIO1 x4 (3.125 Gbps)	SGMII x 4 (1.25 Gbps)	ON	ON

Table 4-7 SerDes Options When Routed to COM-E Connectors (continued) (continued)

Option	Bank 1 SerDes 0 ~ 3 (Slot J6)	Bank 1 SerDes 4 ~ 7 (Slot J14)	Bank 2 SerDes 10 ~ 13 (Slot J10)	S1.2 (Bank 1 RefClock)	S1.3/S1.4 (Bank 2/3 RefClock)
11	PEX1 x4 (2.5 Gbps)	SRIO1 x4 (2.5 Gbps)	XAUI (3.125 Gbps)	OFF	OFF
12	PEX1 x4 (5 Gbps)	SRIO1 x4 (2.5 Gbps)	XAUI (3.125 Gbps)	OFF	OFF

4.8 LAN

The COMX-P4080 has one Gigabit port with an LED that shows the controlling signals. It is routed to the COM-E connectors. The interface between MAC and PHY BCM5482 is the first group of the RGMII bus and is multiplexed with ULPI bus. The RCW should then be properly set to select the RGMII protocol.

There are two ports included in the GE PHY BCM5482, the first of which is the only one available in the COMX-P4080 platform. Both ports are available in the P30 and P50 platforms.

The COMX-P4080 has two groups of MDIO buses. The first group is called EMI1 and compiles with IEEE 802.3 Clause 22 standard. It has two pins, EMI1_MDC and EMI1_MDIO and is available externally only on dTSEC0@FMan1. This group is used for the communication between the MAC and PHY. It also manages SGMII PHY.

The second group is called EMI2 and it complies with IEEE 802.3ae Clause 45. EMI2 has two pins: EMI2_MDC and EMI2_MDIO and is available externally only on 10GEC of FMan1. EMI2 is used for the communication between 10GEC and PHY.

The ports in the BCM5482 has two LED controlling signals: LAN1_LINK_ACTIVITY_N and LAN_LINKSPEED_N. The COM-E connectors have four LED controlling signals: link, activity, link_100 and link_1000. The link and activity signals are attached to the LAN1_LINK_ACTIVITY of the BCM5482. Link_1000 is connected to LAN1_LINKSPEED_N and link_100 is left disconnected.

4.9 USB

The COMX-P4080 has four USB 2.0 ports, implemented by one USB PHY (USB3315) controller and one four-port USB hub (USB2514). Between the controller and the hub is the ULPI bus, which is the second group of multiplexing interface in the RGMII/ULPI, making the RCW properly set for using this group.

All four USB port signals are routed to the COM-E connectors.

The operating mode of the USB hub is configured by hardware strapping, and can be configured by the I2C bus by changing the state of the strapping pins. Hardware strapping is set as the default. When configured, the I2C bus address of the USB bus is 0x58.

4.10 UART

There are a total of four universal asynchronous receiver/transmitters (UART) in the COMX-P4080. Each UART has Tx and RX signals that are routed to the COM-E connectors. The UART can also be in two dual UART (DUART), with Tx, Rx, CTS, RTS signals for each DUART. Optional resistors are also available to determine whether UART or DUART are routed.

4.11 1588

The COMX-P4080 module supports signals for the IEEE 1588-v2 capable ethernet interface to the COM-E connector. These signals include Trigger, Alarm, Clock-In and Pulse-Out.

4.12 SDHC

The COMX-P4080 provides an SD/MMC interface to the COM-E. It needs to change the switch S2.6 according to the card type on the carrier.

Table 4-8 SD or Micro SD Card Type on the Carrier

S2.6	Card Type on the Carrier
ON	SD card
OFF (Default)	MicroSD card

4.13 Local Bus

There is one 128-MB NOR flash and one 1-GB NAND flash attached to the local bus. The NOR flash is used for storage of the RCW data, U-Boot and Linux kernel. By default, the NAND flash is used for storing the file system.

Four chip select signals, from CS0 to CS3, are included in the local bus. Of these, only CS0 is enabled during power-on reset. The chip select signal of the device from which the system boots should be connected to the local bus through CS0.

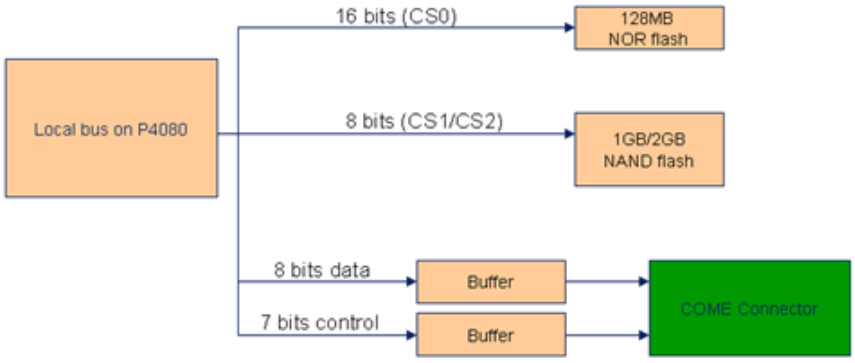
Local bus with 8 bits data bus, as well as the control signals, are routed to COM-E connectors.

Local bus signals are disabled by default, and can be enabled through the buffers using the 8th bit of S1.

Table 4-9 Local Bus on COM-E

S1.8	Local Bus on COM-E
ON	Enabled
OFF (default)	Disabled

Figure 4-7 Local Bus Distribution

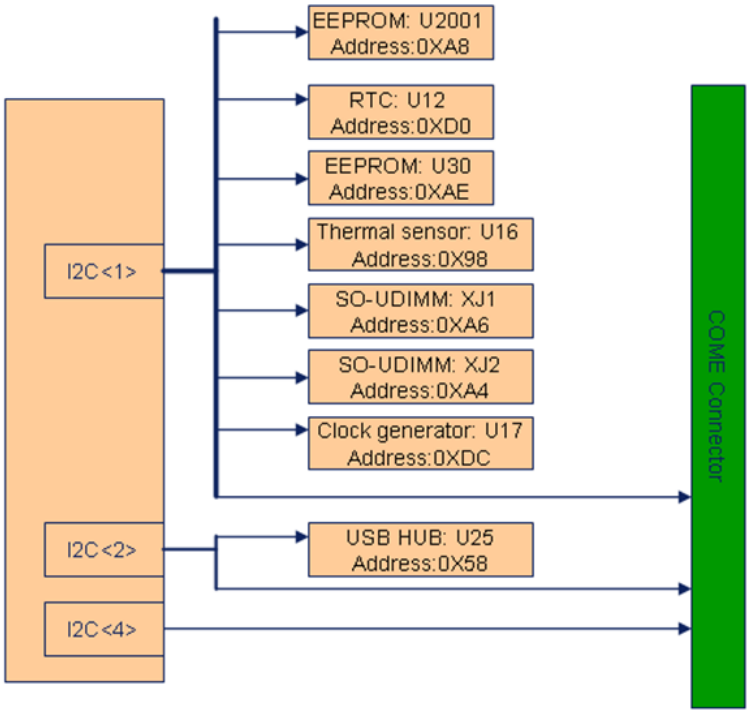


4.14 I2C

There are four physical I2C buses in the COMX-P4080. Three of these are configured as I2C buses and routed to the COM-E connectors. The fourth one is multiplexed with the SDHS bus.

The figure below illustrates the distribution of the I2C buses.

Figure 4-8 I2C Bus Distribution

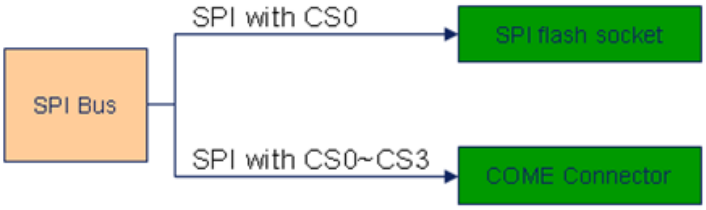


4.15 SPI

The COMX-P4080 has one SPI bus with four chip select signals. It also has an SPI flash socket attached to the SPI bus for debug purposes only. All SPI bus signals are routed to the COM-E connectors.

The figure below illustrates the distribution of the SPI bus.

Figure 4-9 SPI Bus Distribution



4.16 GPIO

The COMX-P4080 has a total of four GPI and four GPO signals that are routed to the COM-E connectors. One of the four GPI is also connected to the switch S1, while two of the four GPOs are connected to LED for debugging purposes.

The following figure and table shows the distribution of the GPIO signals.

Figure 4-10 GPIO Distribution

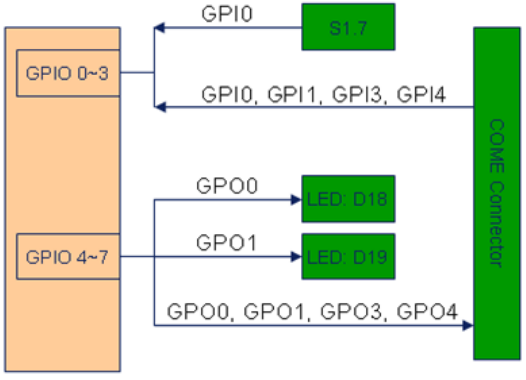


Table 4-10 GPIO Details Distribution

GPIO name	Function
GPIO 0	Connected to the GPI 0 of the COM-E carrier board
GPIO 1	Connected to the GPI 1 of the COM-E carrier board
GPIO 2	Connected to the GPI 3 of the COM-E carrier board
GPIO 3	Connected to the GPI 4 of the COM-E carrier board
GPIO 4	Connected to the GPO 0 of the COM-E carrier board
GPIO 5	Connected to the GPO 1 of the COM-E carrier board
GPIO 6	Connected to the GPO 3 of the COM-E carrier board
GPIO 7	Connected to the GPO 4 of the COM-E carrier board
GPIO 18	WDT input
GPIO 19	Clock generators enable control
GPIO 20	Carrier board reset output
GPIO 23	Clock generator of bank 1 frequency selection
GPIO 24	Clock generator of bank 2 frequency selection
GPIO 26	Clock generator of bank 3 frequency selection

4.17 RTC and Watchdog Timer

The RTC and Watchdog Timer (WDT) are integrated in the module through the IC U12, which is accessed first by the I2C bus, address 0xD0. This device also provides a reset output signal for the COMX-P4080, as well as a 32 KHz clock output for the RTC. Battery backup for the RTC is supplied by the VCC_BAT pin on the COM-E connectors.

The WDT is fed by the GPIO 18 of the COMX-P4080.

4.18 Thermal Sensor

The COMX-P4080 module supports both remote and local thermal sensors. The remote thermal sensor is available when there is a thermal diode provided in the COMX-P4080 and is accessed by the first I2C bus with the address 0x98.

The thermal sensor supplies two alarm signals for the system, defined as "ALERT" and "THRM". When the detected temperature exceeds low temperature limit, an external diode fault will cause the "ALERT" output to assert "low". This "ALERT" output is connected to the IRQ7 of the COMX-P4080.

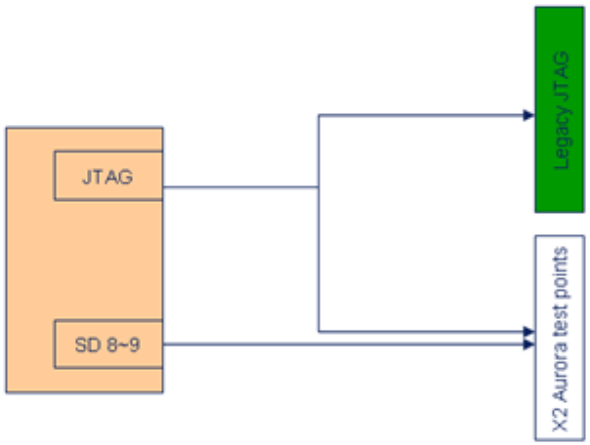
When the detected temperature exceeds the preset high temperature limit, the "THRM" output will assert "low". The "THRM" signal can be connected to the power enable signal of the core and platform power sources, and can be used to power down the COMX-P4080. This can be done by installing the resistor R178, which is not installed by default.

4.19 Debugger

The COMX-P4080 supports the JTAG debugger, which is provided by default.

Debugger selection details can be seen the following figure.

Figure 4-11 COMX-P4080 Debugger Selection Details



5.1 Maps

5.1.1 Memory Map

The following table shows COMX-P4080's memory mapping.

Table 5-1 COMX-P4080 Memory Map

Address#	Effective Address	Physical Address	Size	Description
1	0000 0000	0 0000 0000	0 8000 0000 2 GB	DDR3 Memory[1]
2	8000 0000	C 0000 0000	0 2000 0000 512 MB	PCIE1 MEM
3	A000 0000	C 2000 0000	0 2000 0000 512 MB	PCIE2 MEM [2]
4	A000 0000	C 2000 0000	0 1000 0000 256 MB	RIO1 MEM[1]
5	B000 0000	C 3000 0000	0 1000 0000 256 MB	RIO2 MEM[2]
6	C000 0000	C 4000 0000	0 2000 0000 512 MB	PCIE3 MEM
7	E800 0000	F E800 0000	0 800 0000 128 MB	LBC NOR FLASH
8	F000 0000	F 0000 0000	0 0040 0000 4 MB	DCSR
9	F400 0000	F F400 0000	0 0020 0000 2 MB	BMAN MEM
10	F420 0000	F F420 0000	0 0020 0000 2 MB	QMAN MEM
11	F800 0000	F F800 0000	0 0001 0000 64 KB	PCIE1 IO
12	F801 0000	F F801 0000	0 0001 0000 64 KB	PCIE2 IO
13	F802 0000	F F802 0000	0 0001 0000 64 KB	PCIE3 IO
14	FFA0 0000	F FFA0 0000	0 0010 0000 1MB	NAND FLASH Buffer
15	FE00 0000	F FE00 0000	0 0100 0000 16 MB	CCSR
16	FFFF F000	0 FFFF F000	0 0000 1000 4 KB	BOOT PAGE

[1]A maximum of 2 GB memory is mapped in the U-Boot. Anything more than 2 GB will leave the other memory unmapped and not used. Linux operating systems can use more than 2 GB. Up to 4 GB has been verified.

[2]Address #4 and #5 is used instead of address #3 if RIO is configured.

5.1.2 NOR Flash

The NOR flash is attached to the GPCM on local bus and works at 16-bit mode.

The NOR flash is Numonyx™ Axcell™ JS28F00AM29EWL or Spansion S29GL01GP11TFIR2. Its size is 1 Gb/128 MB. It has 1,024 uniform blocks, 128 KB or 64 kiloword each.

The physical address for NOR flash is 0xFE8000000 - 0xFEFFFFFFF.

The NOR flash should contain RCW data, U-Boot image, U-Boot environment variables, kernel image, device tree blob, RAMDISK image and FMAN ucode image. The detailed map is displayed in the following table:

Table 5-2 NOR Flash Map

Block#	Blocks	Start	End	Size	Description
0	1	0000 0000	0001 FFFF	128 KB	Active RCW Option Data
1	1	0002 0000	0003 FFFF	128 KB	RCW Option Data 1
2	1	0004 0000	0005 FFFF	128 KB	RCW Option Data 2
3	1	0006 0000	0007 FFFF	128 KB	RCW Option Data 3
4	1	0008 0000	0009 FFFF	128 KB	RCW Option Data 4
5	1	000A 0000	000B FFFF	128 KB	RCW Option Data 5
6	1	000C 0000	000D FFFF	128 KB	RCW Option Data 6
7	1	000E 0000	000F FFFF	128 KB	RCW Option Data 7
8	1	0010 0000	0011 FFFF	128 KB	RCW Option Data 8
9	1	0012 0000	0013 FFFF	128 KB	RCW Option Data 9
10	1	0014 0000	0015 FFFF	128 KB	RCW Option Data 10
11	1	0016 0000	0017 FFFF	128 KB	RCW Option Data 11
12	1	0018 0000	0019 FFFF	128 KB	RCW Option Data 12
13	3	001A 0000	0020 0000	384 KB	Not Used
16	112	0020 0000	00FF FFFF	14 MB	FMAN ucode Image
128/80	640	0100 0000	05FF FFFF	80 MB	RAMDISK Image
768/300	232	0600 0000	07CF FFFF	29 MB	Kernel Image
1000/3E8	15	07D0 0000	07ED FFFF	1.9 MB	Device Tree Blob
1015/3F7	1	07EE 0000	07EF FFFF	128 KB	U-Boot Env Variable
1016/3F8	8	07F0 0000	07FF FFFF	1024 KB	U-Boot Image

5.1.3 NAND Flash

The NAND flash is attached to the FCM on local bus and works at 8-bit mode.

The NAND flash is Numonyx NAND08GW3B2CN6E with flash size at 8 Gb or 1 GB. Each page contains 2,112 Bytes, including 2,048 Bytes of data and 64 Bytes of spare. Each block contains 64 pages including 128 KB of data and 4 KB of spare, making a total of 8,192 blocks.

The NAND flash is only used as NAND flash JFFS2 rootfs. The detailed map is displayed on the following table:

Table 5-3 NAND Flash Map

Start Address	End Address	Size	Description
0000 0000	00FF FFFF	16 MB	Not Used
0100 0000	3FFF FFFF	1 GB - 16 MB	NAND FLASH JFFS2 rootfs

5.2 Registers

5.2.1 CCSR Address Map

The full register address of any configuration, control, and status register (CCSR) is comprised of the CCSR window base address, specified in CCSRBAR (default address 0x0_FE00_0000 or 0xF_FE00_0000), plus the functional block base address, plus the specific register's offset within that block.

The table below lists the location of the functional block base address for the entire (CCSR) space.

For more details on each block, please see the COMX-P4080 Reference Manual.

Table 5-4 CCSR Block Base Address Map

Block Base Address (Hex)	Block	Comments
0x00_0000	Local access control—Local configuration control	-
	Local access control—Local access windows	-
0x00_1000–0x00_7FFF	Reserved	-

Table 5-4 CCSR Block Base Address Map (continued)

Block Base Address (Hex)	Block	Comments
0x00_8000	DDR memory controller 1	-
0x00_9000	DDR memory controller 2	-
0x00_A000–0x00_FFFF	Reserved	-
0x01_0000	CoreNet platform cache 1 (CPC1)	-
0x01_1000	CoreNet platform cache 2 (CPC2)	-
0x01_2000–0x01_7FFF	Reserved	-
0x01_8000	CoreNet coherency fabric (CCF)	-
0x01_9000–0x01_FFFF	Reserved	-
0x02_0000	PAMU partition 1	The PAMU is partitioned into 16 identical instances. Not all are necessarily backed with physical hardware. However, all of them must be programmed identically or undefined behavior may result.
0x02_1000	PAMU partition 2	
0x02_2000	PAMU partition 3	
0x02_3000	PAMU partition 4	
0x02_4000	PAMU partition 5	
0x02_5000	PAMU partition 6	
0x02_6000	PAMU partition 7	
0x02_7000	PAMU partition 8	
0x02_8000	PAMU partition 9	
0x02_9000	PAMU partition 10	
0x02_A000	PAMU partition 11	
0x02_B000	PAMU partition 12	
0x02_C000	PAMU partition 13	
0x02_D000	PAMU partition 14	
0x02_E000	PAMU partition 15	
0x02_F000	PAMU partition 16	
0x03_0000–0x03_FFFF	Reserved	-
0x04_0000	PIC—Global registers	Gbl config: 0x04_1000 Gbl timers: 0x04_1100

Table 5-4 CCSR Block Base Address Map (continued)

Block Base Address (Hex)	Block	Comments
0x05_0000	PIC—Interrupt source registers	External IRQs: 0x05_0000 Internal IRQs: 0x05_1200
0x06_0000	PIC—Processor (core) registers	-
0x07_0000–0x0B_FFFF	Reserved	-
0x0C_0000	RapidIO—Architectural registers	-
0x0D_0000	RapidIO—Implementation registers	-
0x0E_0000	Configuration/pin control	-
0x0E_1000	Clocking	-
0x0E_2000	Run control/power management (RCPM)	-
0x0E_3000–0x0E_7FFF	Reserved	-
0x0E_8000	Security fuse processor (SFP)	-
0x0E_9000–0x0E_9FFF	Reserved	-
0x0E_A000	SerDes control	-
0x0E_B000–0x0F_FFFF	Reserved	-
0x10_0000	DMA controller 1	-
0x10_1000	DMA controller 2	-
0x10_2000–0x10_FFFF	Reserved	-
0x11_0000	Enhanced serial peripheral interface (eSPI)	-
0x11_1000–0x11_3FFF	Reserved	-
0x11_4000	Enhanced secure digital high capacity (eSDHC)	-
0x11_5000–0x11_7FFF	Reserved	-
0x11_8000	Dual I2C controller 1	I2C 1: 0x11_8000 I2C 2: 0x11_8100
0x11_9000	Dual I2C controller 2	I2C 3: 0x11_9000 I2C 4: 0x11_9100
0x11_A000–0x11_BFFF	Reserved	-
0x11_C000	DUART controller 1	UART1: 0x11_C500 (DUART1) UART2: 0x11_C600 (DUART1)

Table 5-4 CCSR Block Base Address Map (continued)

Block Base Address (Hex)	Block	Comments
0x11_D000	DUART controller 2	UART3: 0x11_D500 (DUART2) UART4: 0x11_D600 (DUART2)
0x11_E000–0x12_3FFF	Reserved	-
0x12_4000	Enhanced local bus controller (eLBC)	-
0x12_5000–0x12_FFFF	Reserved	-
0x13_0000	GPIO controller	-
0x13_1000–0x13_7FFF	Reserved	-
0x13_8000	Pre-boot loader (PBL)	Software cannot write to the PBL CCSR space directly. However, special PBL commands may be leveraged during pre-boot initialization by referencing specific CCSR offsets (unique commands have unique CCSR offsets).
0x13_9000–0x1F_FFFF	Reserved	-
0x20_0000	PCI Express controller 1	-
0x20_1000	PCI Express controller 2	-
0x20_2000	PCI Express controller 3	-
0x20_2000–0x20_FFFF	Reserved	-
0x21_0000	USB 1 (host only)	-
0x21_1000	USB 2 (dual role)	-
0x21_2000–0x2F_FFFF	Reserved	-
0x30_0000	SEC 4.0	-
0x31_0000–0x31_3FFF	Reserved	-
0x31_4000	Security monitor	-
0x31_5000–0x31_5FFF	Reserved	-
0x31_6000	Pattern match engine (PME)	-
0x31_7000–0x31_7FFF	Reserved	-
0x31_8000	Queue manager (QMAN)	-

Table 5-4 CCSR Block Base Address Map (continued)

Block Base Address (Hex)	Block	Comments
0x31_9000–0x31_9FFF	Reserved	-
0x31_A000	Buffer manager (BMAN)	-
0x31_B000–0x3F_FFFF	Reserved	-
0x40_0000	Frame manager 1	-
0x50_0000	Frame manager 2	-
0x60_0000–0xFF_FFFF	Reserved	-

Operating System and Driver Support

6.1 Supported Operating Systems

This module supports the following operating systems:

- Linux (published by Artesyn)
  Includes the following:
  - U-Boot
  - Linux kernel
  - File system

6.2 Supported Drivers

The following lists the drivers supported by the COMX-P4080 COM Express Module.

Table 6-1 Driver Controller Table

	Linux (published by Artesyn)
Chipset	No (integrated in the CPU)
Graphic	No
LAN	Yes

7.1 Overview

COMX-P4080 has a board support package (BSP) that provides a shell to allow users to accomplish most of the debugging operations on most of the board's interfaces and peripheral devices. The BSP of COMX-P4080 is U-Boot, Linux, DTB and rootfs.

7.2 Setup Requirements

The following are the minimum setup requirements for the COMX-P4080:

- One serial cable to connect the COMX-P4080 to a computer
- One network cable connecting the onboard network port to the network
- A TFTP server connected to the network.
  - The IP address should 192.168.0.100
  - The TFTP root is `/tftpboot/`. You need to create a sub-directory named "comx_p4080/" in this root.
- Three copies of the BSP package comx_p4080.
- COMX_P4080_V100R00.tar.gz, which will be decompressed in the comx_p4080/ file
- NFS service is active on this TFP server and files are exported to /tftpboot/comx_p4080/rootfs_nfs

7.3 Basic Commands

The following are the commands commonly used by the U-Boot. To enter the U-Boot shell, press any key while the autoboot is counting down.

Table 7-1 Basic U-Boot Commands

Command	Description
=>	Prompt for the command line.
help [cmd] or ? [cmd]	Used to display the usage options for the command "cmd". If "cmd" is not specified, U-Boot will display the brief usage options for all of the available commands.

Table 7-1 Basic U-Boot Commands (continued)

Command	Description
printenv [vn]	Displays the value of the environment variable "vn". If "vn" is not specified, U-Boot will display the values for all of the environment variables.
setenv <vn> [vv]	Sets the value of the environment variable "vn" to "vv". If "vv" is not specified, U-Boot will not define the environment variable "vn". If "vv" includes spaces, it should be enclosed within single quote marks. For example: `setenv manufacturer 'Emerson Network Power'`
saveenv	Saves all the environment variables persistently to the U-Boot env section on NOR Flash.
run eraenv	Erases all the environment variables stored in the U-Boot env section on NOR Flash. ● Protect off EFEE0000 +00020000; erase EFEE0000 +00020000 ● Protect on EFEE0000 +00020000 A reset must be performed after "run eraenv".
tftpboot	Downloads image through network using TFTP protocol. ● tftpboot [loadAddress] [[hostIPaddr:]bootfilename] ● Exampe: tftpboot $loadaddr $ubootfile
bootm	Boots application image from memory. ● bootm [addr [arg ...]] ● Example: bootm $norbootaddr $norfsaddr $norfdtaddr ● Example: bootm $loadaddr - $fdtaddr

7.4 Basic Environment Variable Settings

7.4.1 Network Variables

Network Variables	
setenv ipaddr	192.168.0.91
setenv netmask	255.255.255.0
setenv gatewayip	192.168.0.1
setenv serverip	192.168.0.100
setenv ethaddr	MAC address stored in ID EEPROM
setenv eth1addr	00:01:af:12:23:92
setenv eth2addr	00:01:af:12:23:93
setenv eth3addr	00:01:af:12:23:94
setenv eth4addr	00:01:af:12:23:95
setenv eth5addr	00:01:af:12:23:96
setenv eth6addr	00:01:af:12:23:97
setenv eth7addr	00:01:af:12:23:98
setenv eth8addr	00:01:af:12:23:99
setenv eth9addr	00:01:af:12:23:9a

7.4.2 Filename Variables for BSP Components

Filename Variables for BSP Components
setenv rcwfile comx_p4080/COMX_P4080_V100R00/rcw.bin
setenv fmanfile comx_p4080/COMX_P4080_V100R00/fsl_fman_u-code_P4080_101_6.bin
setenv bootfile comx_p4080/COMX_P4080_V100R00/uImage
setenv norfsfile comx_p4080/COMX_P4080_V100R00/rootfs_ext2.img
setenv fdtfile comx_p4080/COMX_P4080_V100R00/comx.dtb
setenv ubootfile comx_p4080/COMX_P4080_V100R00/u-boot.bin
setenv nandfsfile comx_p4080/COMX_P4080_V100R00/rootfs_jffs2.nand
setenv rootpath /tftpboot/comx_p4080/rootfs_nfs

7.4.3 Address Variables for BSP Components on NOR Flash

Address Variables for BSP Components on NOR Flash	
norrcwaddr	Default is E8000000
norfmanaddr	Default is E8200000
norfsaddr	Default is E9000000
norbootaddr	Default is EE000000
norfdtaddr	Default is EFD00000
norubootenvaddr	Default is EFEE0000
norubootaddr	Default is EFF00000

7.4.4 Address Variables for the Boot Components in RAM

Address Variables for the Boot Components in RAM	
loadaddr	Default is 1000000
fdtaddr	Default is C0000
ramdiskaddr	Default is 2000000

7.4.5 Device Variables

Device Variables
setenv ethact FM1@DTSEC1
setenv netdev eth0
setenv uart# 0
setenv consoledev ttyS0
setenv baudrate 115200
setenv usbbdev sda2
setenv mmcbdev mmcblk0p2
setenv hdbdev sda1
setenv jffs2nand mtdblock7

7.4.6 HWCONFIG Variable

HWCONFIG Variable	
hwconfig	Default is 'fsl_ddr:ctlr_intlv=cache-line,bank_intlv=cs0_cs1;esdhc;serdes:fsl_srds_lp-d_b3=0xf;fsl_fm2_xaui_phy:xfi'.

7.4.7 Bootargs Variable

Bootargs Variable	
root	• root=/dev/ram for ramboot and norboot; • 'root=/dev/$jffs2nand rw' for nandboot; • root=/dev/nfs for nfsboot; • 'root=/dev/$usbbdev rw' for usbfatboot and usbext2boot; • oot=/dev/$mmcbdev rw' for mmcfatboot and mmcext2boot
rootfstype	'rootfstype=jffs2' is needed for nandboot
rootdelay	'rootdelay=30' is needed for usb*boot and mmc*boot
console	Default is 'console=$consoledev,$baudrate'
hwbootargs	Default is 'riohdid=0 xauiphy=1', generated by U-Boot based on hwconfig.
othbootargs	Default is 'ramdisk_size=00700000 cache-sram-size=0x10000

7.4.8 Bootup Variables

Bootup Variables	
ramboot	Default is 'setenv bootargs root=/dev/ram rw console=$consoledev,$baudrate $hwbootargs $othbootargs;tftp $ramdiskaddr $ramdiskfile;tftp $loadaddr $bootfile;tftp $fdtaddr $fdtfile;bootm $loadaddr $ramdiskaddr $fdtaddr'
norboot	Default is 'setenv bootargs root=/dev/ram rw console=$consoledev,$baudrate $hwbootargs $othbootargs;bootm $norbootaddr $norfsaddr $norfdtaddr'
nandboot	Default is 'setenv bootargs root=/dev/$jffs2nand rw console=$consoledev,$baudrate rootfstype=jffs2 $hwbootargs $othbootargs;bootm $norbootaddr - $norfdtaddr'

nfsboot	Default is 'setenv bootargs root=/dev/nfs rw nfsroot=$serverip:$rootpath ip=$ipaddr:$serverip:$gatewayip:$netmask:$hostname:$netdev:off
mmcfatboot	default is 'setenv bootargs root=/dev/$mmcbdev rw rootdelay=30 console=$consoledev,$baudrate $hwbootargs $othbootargs;mmcinfo;fatload mmc 0:1 $loadaddr /boot/$bootfile;fatload mmc 0:1 $fdtaddr /boot/$fdtfile;bootm $loadaddr - $fdtaddr'
mmcext2boot	default is 'setenv bootargs root=/dev/$mmcbdev rw rootdelay=30 console=$consoledev,$baudrate $hwbootargs $othbootargs;mmcinfo;ext2load mmc 0:2 $loadaddr /boot/$bootfile;ext2load mmc 0:2 $fdtaddr /boot/$fdtfile;bootm $loadaddr - $fdtaddr'
usbfatboot	default is 'setenv bootargs root=/dev/$usbbdev rw rootdelay=30 console=$consoledev,$baudrate $hwbootargs $othbootargs;usb start;fatload usb 0:1 $loadaddr /boot/$bootfile;fatload usb 0:1 $fdtaddr /boot/$fdtfile;bootm $loadaddr - $fdtaddr'
usbext2boot	default is 'setenv bootargs root=/dev/$usbbdev rw rootdelay=30 console=$consoledev,$baudrate $hwbootargs $othbootargs;usb start;ext2load usb 0:2 $loadaddr /boot/$bootfile;ext2load usb 0:2 $fdtaddr /boot/$fdtfile;bootm $loadaddr - $fdtaddr'

7.5 Checking the BSP Version

There are several different versions of the BSP, but no versions are availble for RCW and DTB. Below are the methods on how the versions can be checked.

1. For the FMAN uCode Version, it can be found in the U-Boot boot-up message.
   Fman: Uploading microcode version 101.6.0.

2. RAMDISK rootfs version

   - Boot up with ramboot ('run ramboot' in U-Boot) or norboot ('run norboot' in U-Boot).
     In Linux, run `'cat /etc/.version'`

```
[root@COMX-P4080 root]# cat /etc/.version
COMX-P4080 EXT2 ROOTFS ver: COMX_P4080_V100R00 build by
ec7536@cncdebaobs04.emrsn.org on Mon Nov 29 08:46:50 UTC 2010
```

3. Kernel version

   - The version can be viewed in the loading kernel message:
     ## Booting kernel from Legacy Image at XXXXXXXX ...
     Image Name: Linux-2.6.34.6
     Created: 2010-11-29 8:46:16 UTC

   - Run 'iminfo $norbootaddr' in U-Boot

```
=> iminfo $norbootaddr
## Checking Image at ee000000 ...
Legacy image found
Image Name:   Linux-2.6.34.6
Created:      2010-11-29   8:46:16 UTC
Image Type:   PowerPC Linux Kernel Image (gzip compressed)
Data Size:    3520445 Bytes = 3.4 MiB
Load Address: 00000000
Entry Point:  00000000
Verifying Checksum ... OK
```

   - In the kernel boot-up message:

```
Linux version 2.6.34.6 (ec7536@cncdebaobs04.emrsn.org) (gcc
version 4.3.2 (Sourcery G++ Lite 4.3-74) ) #1 SMP Mon Nov 29
16:46:03 CST 2010
```

4. U-Boot Version

   - Run the command "version" after the first line lf the U-Boot boot-up message

```
=> version
U-Boot 2010.06-COMX_P4080_V100R00 (Nov 29 2010 - 16:24:12)
```

5. JFFS2 rootfs version

   - In the U-Boot, boot with nanboot ('run nandboot'). In Linux, run 'cat /etc/.version'

```
[root@COMX-P4080 root]# cat /etc/.version
COMX-P4080 JFFS2 ROOTFS for nand.full FLASH ver:
COMX_P4080_V100R00 build by ec7536@cncdebaobs04.emrsn.org on
Mon Nov 29 08:47:50 UTC 2010
```

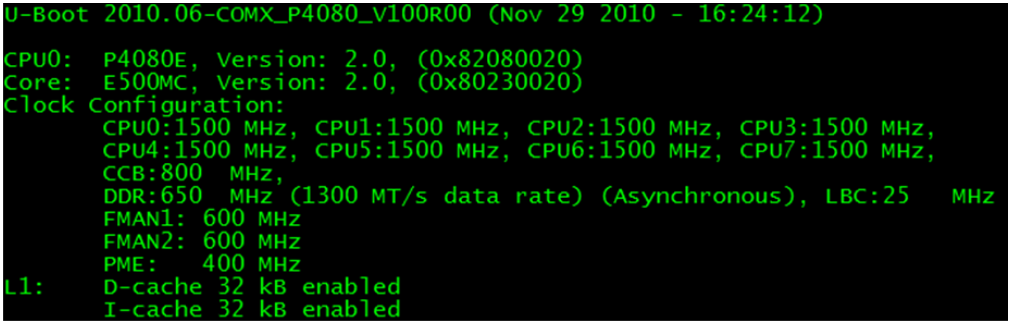
6. NFS rootfs version

   - In the U-Boot, boot with nfs ('run nfsboot'). In Linux, run 'cat/etc/.version'.
     ```
     [root@COMX-P4080 root]# cat /etc/.version
     COMX-P4080 NFS ROOTFS ver: COMX_P4080_V100R00 build by
     ec7536@cncdebaobs04.emrsn.org on Mon Nov 29 08:50:20 UTC 2010
     ```

7.6 CPU

COMX-P4080 has the Freescale QorIQ Communications Processor. The CPU information can be viewed in the terminal.

Figure 7-1 COMX-P4080 CPU Information



CPU0 is the active CPU in the U-Boot. Run the command "`reset`" to reboot the CPU/board.

7.7 Address Space

U-Boot and Linux work in 36-bit physical addressing mode. The relationship between effective address and physical address is displayed in the memory map table on Table "COMX-P4080 Address Space".

The following are mapped in to the first 4 GB address space of the 64 GB, which is the 36-bit physical address space. The 4 GB space is named as the effective address space and can be accessed by the U-Boot.

- DDR3 SDRAM
- PCIE1/2/3 MEM
- PCIE1/2/3 IO
- RIO1/2 MEM
- LBC NOR FLASH
- DCSR
- BMAN MEM
- QMAN MEM
- NAND FLASH Buffer
- CCSR
- BOOT PAGE

Table 7-2 COMX-P4080 Address Space

Address	32-bit Effective Base Address	36-bit Phyiscal Base Address	Size	Description
1	0000 0000	0 0000 0000	8000 0000 - 2 GB	DDR3 Memory
2	8000 0000	C 0000 0000	2000 0000 - 512 MB	PCIE1 MEM
3	A000 0000	C 2000 0000	2000 0000 - 512 MB	PCIE2 MEM, if #4 and #5 are unused
4	A000 0000	C 2000 0000	1000 0000 - 256 MB	RIO1 MEM, if #2 is unused
5	B000 0000	C 3000 0000	1000 0000 - 256 MB	RIO2 MEM, if #2 is unused
6	C000 0000	C 4000 0000	0800 0000 - 512 MB	PCIE3 MEM
7	E800 0000	F E800 0000	0800 0000 - 128 MB	LBC NOR Flash
8	F000 0000	F 0000 0000	0040 0000 - 4 MB	DCSR
9	F400 0000	F F400 0000	0020 0000 - 2 MB	BMAN MEM
10	F420 0000	F F420 0000	0020 0000 - 2 MB	QMAN MEM
11	F800 0000	F F800 0000	0001 0000 - 64 KB	PCIE1 IO

Table 7-2 COMX-P4080 Address Space (continued)

Address	32-bit Effective Base Address	36-bit Phyiscal Base Address	Size	Description
12	F801 0000	F F801 0000	0001 0000 - 64 KB	PCIE2 IO
13	F802 0000	F F802 0000	0001 0000 - 64 KB	PCIE3 IO
14	FFA0 0000	F FFA0 0000	0010 0000 - 1 MB	NAND Flash Buffer
15	FE00 0000	F FE00 0000	0100 0000 - 16 MB	CCSR
16	FFFF F000	0 FFFF F000	0000 1000 - 4 KB	Boot Page

U-Boot uses the following commands to display and modify the contents of the 4 GB effective address space. Note that ".b", ".w", and ".l" means the operation unit is "byte", "word", and "long" respectively.

md - Memory display
md [.b, .w, .l] address [# of objects]

mm - memory modify (auto-incrementing address)
mm [.b, .w, .l] address

nm - memory modify (constant address)
nm [.b, .w, .l] address

cp - this command copies data from one place to another
cp [.b, .w, .l] source target count

cmp - this command compares two data in different places.
cmp [.b, .w, .l] addr1 addr 2 count

7.8 DDR3 SDRAM

COMX-P4080 has two fully programmable DDR3 SDRAM controllers. A maximum of 2 GB SDRAM are mapped in U-Boot. If more than 2 GB SDRAM is fitted, the remaining sections are left unmapped. With Linux, up to 4 GB SDRAM can be verified.

Do not modify the contents of the lowest 1 MB and the top 1 MB RAM in the U-Boot. Both areas are used to store critical data by U-Boot.

When the U-Boot detects the DDR3 SDRAM during boot up, the following message appears:

```
DRAM: Initializing...
2 GB left unmapped
    DDR: 4 GB (DDR3, 64-bit, CL=9, ECC on)
    DDR Controller Interleving Mode: cache line
    DDR Chip-Select Interleaving Mode: CS0+CS1
```

7.9 GPIO

COMX-P4080 has fourteen general purpose input/output (GPIO).

Table 7-3 GPIO States

GPIO#	Input/Output	Reset State	Description
GPIO00	I	I	GPI0 of COM-E connectors
GPIO01	I	I	GPI1 of COM-E connectors
GPIO02	I	I	GPI3 of COM-E connectors
GPIO03	I	I	GPI4 of COM-E connectors
GPIO04	O	I	GPO0 of COM-E connectors and also as to control debug LED D18
GPIO05	O	I	GPO1 of COM-E connectors and also as to control debug LED D19
GPIO06	O	I	GPO3 of COM-E connectors
GPIO07	O	I	GPO4 of COM-E connectors
GPIO18	O	I	Watchdog Input
GPIO19	O	I	Clock Generator Enable
GPIO20	O	I	Carried board reset output
GPIO23	I	I	Clock generator of bank 1 frequency selection input
GPIO24	I	I	Clock generator of bank 2 frequency selection input
GPIO26	I	I	Clock generator of bank 3 frequency selection input

For more information, see Chapter 4, *GPIO*, on page 69.

The U-Boot provides several GPIO utility commands.

Table 7-4 GPIO Command Usage

Command	Description
gpio dump	Dumps the direction, od and level information for all pins
gpio get <pin>	Gets the direction, od and level information for the specified pin
gpio set dir <pin> <dir>	Sets the direction of the specified pin
gpio set dir <pin>	Sets the od of the specified pin
gpio set dir <pin> <lvl>	Sets the level of the specified pin

The parameters used in the GPIO utility commands are described below.

<pin> - 0, 1, 2, 3, 4, 5, 6, 7, 18, 19, 20, 23, 24, 26

<dir> - 0 for input
1 for output

<od> - 0 for output
1 for open drain

<lvl> - 0 for low level
1 for high level

7.10 UART

There are a total of four universal asynchronous receiver/transmitters (UART) in the COMX-P4080, each with Tx and Rx signals routed to the COM-E connectors. For more details, see *UART* on page 66.

The default active console is UART0. The working mode is 115200, 8, N, 1. Each of the four UART can become the active console by setting the environment variable "uart#".

Usage:

UART0 - setnev uart# 0; savenv; reset

UART1 - setnev uart# 1; savenv; reset

UART2 - setnev uart# 2; savenv; reset

UART3 - setnev uart# 3; savenv; reset

The UART boot up message in U-Boot is as follows:

In :	Serial
Out :	Serial
Err :	Serial
Current Console:	uart#0

7.11 NOR Flash

The NOR Flash is Numonyx™ Axcell™ JS28F00AM29EWL or Spansion S29GL01GP11TFIR2 and is attached to the GPCM on local bus and works with 16-bit data width. It is either 1 GB or 128 MB and has 1024 uniform blocks of 128 K (or 64 K words each). The 36-bit physical address of NOR Flash is 0xFE8000000 - 0xFEFFFFFFF. Boot up message in U-Boot is "FLASH: 128 MiB".

For more information on the NOR Flash memory maps, see Table "NOR Flash Map" on page 74

NOR Flash supports the following commands: md, cp, cmp, protect and erase.

Table 7-5 NOR Flash Command Usage

Command	Description
protect on start end	Protects flash from address "start" to address "end"

Table 7-5 NOR Flash Command Usage (continued)

Command	Description
protect on start +len	Protects flash from address "start" to end of section with address "start"+"len"-1
protect on all	Protects all flash banks
protect off start end	Makes flash from address "start" to address "end" writable
protect off start +len	Makes flash from address "start" to end of section with address "start"+"len"-1 writable
protect off all	Makes all flash banks writable
erase start end	Erases flash from address 'start' to address 'end'
erase start +len	Erases flash from address 'start' to the end of section with address 'start'+len-1
erase all	Erases all flash banks

The following is a NOR Flash operation example that upgrades the U-Boot.

```
tftpboot $loadaddr $ubootfile; protect off 0xeff00000 +$filesize;
erase 0xeff00000 +$filesize; cp.b $loadaddr 0xeff00000 $filesize;
protect on 0xeff00000 +$filesize;
```

7.12 NAND Flash

The NAND Flash is Numonyx NAND08GW3B2CN6E which is 1 GB in size. It is attached to the FCM on the local bus and works at 8-bit mode. Boot up message will appear as "NAND: 1024 MiB".

Each page contains 2,112 bytes, including 2048 bytes of data with 64 bytes spare. Each block contains 64 pages, including 128 KB of data with 4 KB spare, making a total of 8192 blocks.

For more information on the NAND Flash and its memory map, see Table "NAND Flash Map" on page 75.

NAND Flash supports the following commands:

Table 7-6 NAND Flash Command Usage

Command	Description
nand info	Shows available NAND devices
nand device [dev]	Shows or sets current device
nand read	Addr off | partition size
nand write	Addr off | partition size Read/write 'size' bytes starting at offset 'off' to/from memory address 'addr', skipping bad blocks.
nand erase [clean] [off size]	Erase 'size' bytes from offset 'off' (will erase on the entire device if it is not specified)
nand bad	Shows bad blocks
nand dump[.oob] off	Dumps page
nand scrub	Cleans NAND by erasing bad blocks. Considered unsafe.
nand markbad off [...]	Marks bad block or blocks at offset. Considered unsafe.
nand biterr off	Makes a bit error at offset. Considered unsafe.

7.13 I2C

There are a total of four I2C buses in the COMX-P4080, labeled as I2C<1/2/3/4>. For more information, see *I2C on page 68*.

U-Boot provides the following utilities for I2C bus and devices.

Table 7-7 U-Boot I2C Utilities

Utility	Description
i2c crc32 chip address[.0, .1, .2] count	Compute CRC32 checksum
i2c dev [dev]	Shows or sets current I2C bus
i2c loop chip address[.0, .1, .2] [# of objects] [# of delay(us)]	Loops reading of device
i2c md chip address[.0, .1, .2] [# of objects]	Reads from I2C device

Table 7-7 U-Boot I2C Utilities

Utility	Description
i2c mm chip address[.0, .1, .2]	Writes to I2C device (auto-incrementing)
i2c mw chip address[.0, .1, .2] value [count]	Writes to I2C device (fill)
i2c nm chip address[.0, .1, .2]	Writes to I2C device (constant address)
i2c probe	Shows devices on the I2C bus
i2c read chip address[.0, .1, .2] length memaddress	Reads to memory
i2c reset	Re-inititializes the I2C Controller
i2c speed [speed]	Shows or set I2C bus speed

I2C buses in the U-Boot have been re-assigned as follows:

'i2c dev 0' selects I2C<1>

'i2c dev 1' selects I2C<2>

'i2c dev 2' selects I2C<4>

7.13.1 ID EEPROM

i2C EEPROM AT24C02 (U30) is used as ID EEPROM, located on I2C<1>. COMX-P4080 uses ID EEPROM to store the board's serial number, number of network ports, MAC addresses, errata level, manufacturing date and other information. Boot up message in the U-Boot will be: "EEPROM: NXID v0".

U-Boot provides several "mac" utilities to display and program the data in ID EEPROM.

```
mac [read|save|id|num|errata|date|ports|0|1|2|3|4|5|6|7]
```

mac read	Shows content of EEPROM
mac save	Saves to the EEPROM
mac id	Programs system id
mac num	Programs system serial number

mac errata	Programs errata data
mac date	Programs date
mac ports	Programs the number of ports
mac X	Programs the MAC address for port X [X=0...7]

The following are usage examples:

- mac id
- mac num E017D99
- mac errata 0
- mac date 101021120000
- mac ports 1
- mac 0 00:80:42:05:49:d4
- mac save

7.13.2 Board EEPROM

I2C EEPROM (U2001) AT24C02) is used as BOARD EEPROM, located on I2C<1>. The COMX-P4080 uses BOARD EEPROM to store information about the board's processor family, module family and configuration, among others. Boot up message in U-Boot will appear as "EEPROM: COMX".

The U-Boot provides "brd" utilities to display and program the data in BOARD EEPROM.

```
brd [read|save|id|pf|pv|pe|mf|mv|me|ms|md|ma]
```

read	Shows content of EEPROM
brdsave	Saves to the EEPROM
brd id	Programs board id
brd pf	Programs processor family
brd pv	Programs processor version
brd pe	Programs processor errata

brd mf	Programs module family
brd mv	Programs module version
brd me	Programs module errata
brd md	Programs module description string
brd ms	Programs memory size
brd ma	Programs manufacturer string

The following are usage examples of "brd" on the COMX-P4080.

- brd id
- brd pf P4080
- brd pv B
- brd pe 00
- brd mf COME1
- brd mv GA
- brd me 00
- brd ms 4096
- brd md 'ComExpress module on P4080(1.5GHz)'
- brd ma 'Emerson Network Power'
- brd save

7.13.3 Real Time Clock (RTC) and Watchdog Timer (WDT)

COMX-P4080 uses RTC and Watchdog features on M41ST85W. The I2C RTC/WDT M41ST85W (U12) is adopted on the COMX-P4080 and located on I2C<1>.

Boot up message in the U-Boot will be as follows: "RCT: M41ST85W@68" and "WDT: M41ST85W@68(disabled)".

U-Boot provides "date" commands to operate the RTC features. These include get/set/reset date and time.

```
date [MMDDhhmm[[CC]YY][.ss]]
```

date reset

without arguments:	Prints date and time
with numeric argument:	Sets the system date and time
with 'reset' argument:	Resets the RTC

The following are usage samples for "date" on the COMX-P4080.

- date
  Date: 2010-12-01 (Wednesday) Time: 17:57:37
- date reset
  Reset RTC
  Date: 2010-18-01 (Sunday) Time: 0:00:00
- date 120117592010.00
  Date: 2010-12-01 (Wednesday) Time: 17:59:00

U-Boot provides "wdt" commands to operate on the WDT features.

wdt reset	-	Resets WDT
wdt status	-	Checks the current status of WDT
wdt disable	-	Disables WDT
wdt enable <timeout#>	-	Enables WDT with timeout <timeout#> seconds. <timeout#> range [1...124]

The following are usage examples of "wdt" for the COMX-P4080.

- wdt status
  WDT: disabled.
- wdt enable 5
  WDT: enabled with timeout 5 seconds.

- wdt reset
  System reset.

7.13.4 DTT

I2C thermal sensor ADT7461 (U16) is adopted and is located on I2C<1>. The ADT7461 is used to monitor the CPU temperature. Boot up message in the U-Boot will read as "DTT: ADT7461@4C".

U-Boot provides "dtt" to display the CPU temperature. Here is an example of dtt usage:

- dtt
  DTT1: CPU Temperature: 48 C

7.14 SPI

The COMX-P4080 has one eSPI bus with four chip select signals. One SPI flash socket is also attached to the eSPI bus for debug purposes only. All the eSPI signals are routed to the COM-E connectors.

For more information on the distribution of the SPI bus, see *SPI* on page 68.

It is advised that the Expansion S25FL032P0XMFI011 (SO-8 package) is used in the socket. The flash size is 4 MB and it has 64 uniform blocks, with 64 KB per block.

Table 7-8 SPI Flash Memory Map

Start Address	End Address	Size	Description
0000 0000	003F FFFF	4 MB	Not used

U-Boot provides "sf" utilities to operate SPI Flash.

sf probe [bus:]cs [hz] [mode]	-	Initializes flash device on given SPI bus and chip select.
sf read addr offset len	-	Reads 'len' bytes starting at 'offset' to memory at 'addr'
sf write addr offset len	-	Writes 'len' bytes from memory at 'addr' to flash at 'offset'
sf erase offset len	-	Erases 'len' bytes from 'offset'

Below are usage samples for "sf".

- sf probe 0
  4096 KiB S25FL032A(P) at 0:0 is now current device
- sf erase 0 80000
- sf read 1000000 0 10000
- sf write 1000000 0 10000

7.15 MMC/SDHC

COMX-P4080 provides a MMC/SDHC interface to the COM-E connector. There is also a connector for this provided on the carrier. By default, the MMC/SDHC 4-bit mode is selected.

U-Boot provides "mmcinfo" and "mmc" utilities to operate the MMC/SDHC card. "mmcinfo" must be excuted before other "mmc" commands can be run.

mmcinfo		
mmcread <device num> addr blk# cnt		
mmc write <device num> addr blk# cnt		
mmc rescan <device num>		
mmc list	-	Lists available devices

7.16 USB

COMX-P4080 uses the USB2 as the USB host interface. USB1 is disabled. USB PHY (USB3315) is connected to USB2 host interface through ULPI interface. The COMX-P4080 also has one four port USB hub (USB2514) connected to the USB PHY, making it a total of four provided ports.

U-Boot provides "usb" utililties to operate the USB sticks:

Utility	Function
usb reset	Resets or rescans USB controller
usb stop [f]	Stops USB [f]=force stop
usb tree	Shows USB device tree
usb info [dev]	Shows available USB devices
usb storage	Shows details of USB storage devices
usb dev [dev]	Shows or set current USB storage device
usb part [dev]	Prints partition table of one or all USB storage devices
usb read addr blk# cnt	Reads `cnt' blocks starting at block `blk#' to memory address `addr‘
usb write addr blk# cnt	Writes `cnt' blocks starting at block `blk#' from memory address `addr'

Note that "usb start/reset" must be executed before the other commands can be run. Below are usage samples of "usb start.

```
=> usb start
(Re)start USB...
USB: Register 10011 NbrPorts 1
USB EHCI 1.00
scanning bus for devices... 3 USB Device(s) found
scanning bus for storage devices... 1 Storage Device(s) found
```

7.17 SerDes

The COMX-P4080 has three Serializer/Deserializer (SerDes) banks, including a total of 18 lanes. Twelve of these are routed to the COM-E connectors, defined as SERDES0 - SERDES7 (SERDES0-7 of bank 1), and SERDES16 - SERDES19 (SERDES10-13 of bank 2). SERDES8-SERDES9 of bank 1 are used for Aurora debugger . The four lanes of bank 3 are not used in COMX-P4080 and are reserved for the P30 and P50 series SATA interfaces.

For more information on the SerDes, see *SerDes* on page 63. This includes the SerDes lane distribution and options when it is routed to the COM-E connectors.

U-Boot provides "rcw" utilities to switch SerDes lanes among the twelve SerDes/RCW options. A checking feature is also supported. Below is a usage sample of the utilities.

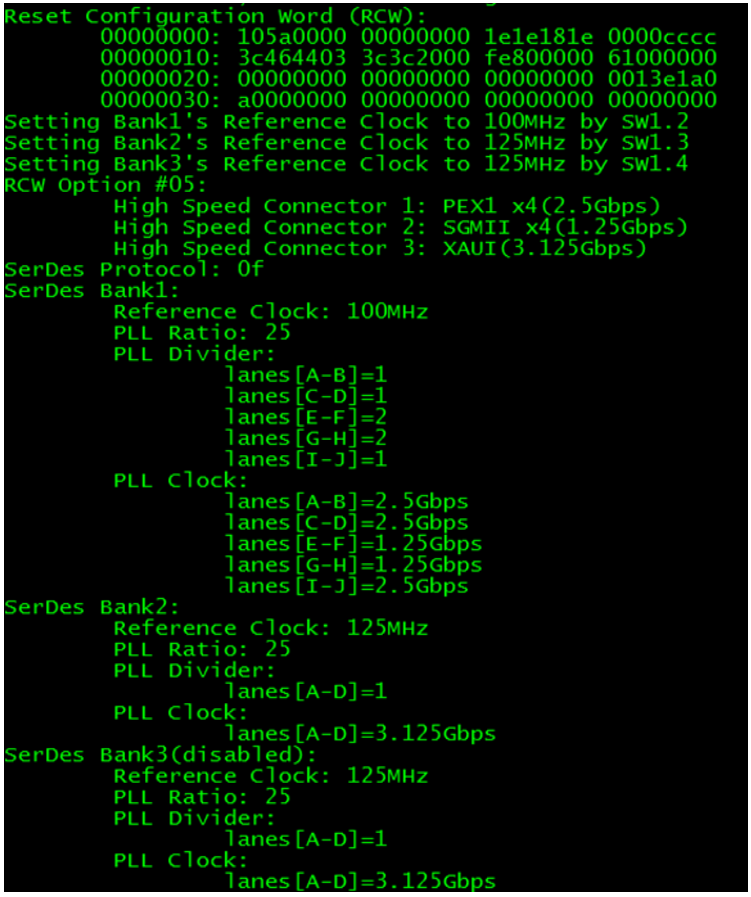
rcw list	-	Lists the status of RCW sections
rcw active <option#>	-	active <option#> RCW. <option#> range [1..12]
rcw check current	-	Checks the current RCW with which system boots up
rcw check active	-	Checks the status of the active RCW section
rcw check backup [option#]	-	Checks the status of all or # backup RCW section(s). <option#> range [1..12]

The steps below are used to activate specific SerDes/RCW options.

- Run "rcw active <option#>" to activate the SerDes/RCW option#.
- Power off the board.
- Set switch S1.2, S1.3 and S1.4 to "ON" or "OFF" (refer to Table "SerDes Options When Routed to COM-E Connectors" on page 64) in order to correctly set up reference clocks for SerDes banks.
- Power up the board.

Using option #5 from Table "SerDes Options When Routed to COM-E Connectors" on page 64 as an example, the boot up message will appear as below.

Figure 7-2 Example of Boot Up Message in U-Boot



7.18 Network

COMX-P4080 has two frame managers. Each one supports five native network interfaces broken down into four 1 GB Ethernet interfaces (DTSEC) and one 10 GB Ethernet interface (TGEC). Due to a bug in the frame manager, only 12 Gbps is supported. This does not allow the DTSEC and one XAUI to work the line speed at the same time at they total 14 Gbps.

To allow the board to function through those limitations, the COMX-P4080 powers down two SGMII ports when the XAUI is enabled through the SerDes/RCW options.

COMX-P4080 has the following combinations of network ports in the frame managers:

- 1 RGMII (FM1) + 2 SGMII (FM2) + XAUI (FM2)
- 1 RGMII (FM1) + 4 SGMII (FM2)

PCIE-based network ports like the Intel PRO/1000 are not limited by the abovementioned rules because their packets are handled not by the the frame managers but by the CPU. COMX-P4080 powers down the Bank 3 SerDes (FM1 lanes).

EC1 of pin multiplexing configuration in the RCW routes the RGMII port (FM1@DTSEC1) to the EC1 parallel mode pins. The RGMII port is always present in all of the twelve SerDes/RCW options.

Table 7-9 Network Ports Naming Rules in U-Boot

FM1 Network Ports	
	Port 0 (the RGMII port) is named as FM1@DTSEC1
FM2 Network Ports	
	Port 0 is named as FM2@DTSEC1
	Port 1 is named as FM2@DTSEC2
	Port 2 is named as FM2@DTSEC3
	Port 3 is named as FM2@DTSEC4
	Port 4 (XAUI) is named as FM2@TGEC1

With 1 SGMII-Riser (Freescale), 1 XAUI-Rise (Freescale), 2 PRO/1000 Server Adapter (Intel), the valid combinations of network ports among the twelve SerDes/RCW options are listed in Table "Valid Network Ports Combination of SerDes/RCW" on page 109.

Refer to Table "SerDes Options When Routed to COM-E Connectors" on page 64 for the corresponding information on SerDes 0-3, SerDes 4-7 and SerDes 10-13 for each option.

Table 7-10 Valid Network Ports Combination of SerDes/RCW

Option	Onboard RGMII	SGMII-Riser	XAUI-Riser	PRO/1000 (dual-port) #1	PRO/1000 (dual-port) #2
1	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	SLOT J14 e1000#2 e1000#3
2	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	SLOT J14 e1000#2 e1000#3
3	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	SLOT J14 e1000#2 e1000#3
4	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	SLOT J14 e1000#2 e1000#3
5	FM1@DTSEC1	SLOT J14 FM2@DTSEC1 FM2@DTSEC2	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	X
6	FM1@DTSEC1	SLOT J14 FM2@DTSEC1 FM2@DTSEC2	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	X
7	FM1@DTSEC1	X	X	SLOT J6 e1000#0 e1000#1	X
8	FM1@DTSEC1	X	X	SLOT J6 e1000#0 e1000#1	X
9	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	X	X

Table 7-10 Valid Network Ports Combination of SerDes/RCW (continued)

Option	Onboard RGMII	SGMII-Riser	XAUI-Riser	PRO/1000 (dual-port) #1	PRO/1000 (dual-port) #2
10	FM1@DTSEC1	SLOT J10 FM2@DTSEC1 FM2@DTSEC2 FM2@DTSEC3 FM2@DTSEC4	X	X	X
11	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	X
12	FM1@DTSEC1	X	SLOT J10 FM2@DTGEC1	SLOT J6 e1000#0 e1000#1	X

During Linux boot up, every network port is named "ethX" by default. UDEV rules allow it to be changed by the user.

The "x" in the name is important for the nfsboot. For more information, see Chapter 7, *Boot*, on page 112. To locate the X "x" in the "ethX", refer to the list below.

0 - FM2@DTSEC1
1 - FM2@DTSEC1
2 - FM2@DTSEC2
3 - FM2@DTSEC3
4 - FM2@DTSEC4
5 - FM2@TGEC1
6 - e1000#0
7 - e1000#1
8 - e1000#2
9 - e1000#3

If certain frame manager network port or ports are not valid for the specified SerDes/RCW option, the “X” for the lower valid network port should subtract the numbers of the above invalid network ports.

Here is an example of the "ethX" naming based on the option #5. Install Intel PRO/1000 server adapter in SLOT J6. For the Freescale SGMII-Riser install it in SLOT J14 and for Freescale XAUI-Riser, install it in SLOT J10. The U-Boot boot up message will list the valid ports list: FM1@DTSEC1,FM2@DTSEC1,FM2@DTSEC2,FM2@TGEC1, e1000#0, e1000#1. The "ethX" list would then be as follows:

0	-	FM1@DTSEC1
1	-	FM2@DTSEC1
2	-	FM2@DTSEC2
*	-	FM2@DTSEC3
*	-	FM2@DTSEC4
3 (5-2)	-	FM2@TGEC1
4 (6-2)	-	e1000#0
5 (7-2)	-	e1000#1
*	-	e1000#2
*	-	e1000#3

UDEV rules rename the default name "ethX" for network ports of frame manager for convenience and identification.

Table 7-11 UDEV Rules for Network Ports in Linux

FM1 Network Ports
Port 0 (FM1@DTSEC1) is named as fm1-gb1
FM2 Network Ports
Port 0 (FM2@DTSEC1) is named as fm2-gb1
Port 1 (FM2@DTSEC2) is named as fm2-gb2
Port 2 (FM2@DTSEC3) is named as fm2-gb3
Port 3 (FM2@DTSEC4) is named as fm2-gb4

Table 7-11 UDEV Rules for Network Ports in Linux (continued)

FM1 Network Ports
Port 4 (FM2@TGEC1) (XAUI) is named as fm2-10g

An exception for frame manager network ports is when the nfsboot, which is the network port for mounting NFS, remains "ethX" and will not be renamed to "fmY-gbZ" in Linux because the udev cannot rename the device that is currently busy.

For network ports of PRO/1000, the port name is always "ethX".

In order to use SGMII/XAUI network ports of the frame managers, ten U-Boot network environment variables for MAC addresses must be set.

```
=> setnev ethaddr
=> setenv eth1addr 00:01:af:12:23:92
=> setenv eth2addr 00:01:af:12:23:93
=> setenv eth3addr 00:01:af:12:23:94
=> setenv eth4addr 00:01:af:12:23:95
=> setenv eth5addr 00:01:af:12:23:96
=> setenv eth6addr 00:01:af:12:23:97
=> setenv eth7addr 00:01:af:12:23:98
=> setenv eth8addr 00:01:af:12:23:99
=> setenv eth9addr 00:01:af:12:23:9a
=>saveenv
```

7.19 Boot

COMX-P4080 provides the following boot methods:

- *RAMboot*
- *NORboot*
- *NANDboot*

- *NFSboot*
- *USBFATboot and USBEXT2boot*
- *MMCFATboot and MMCEXT2boot*

Common device environment variables in U-Boot include the following:

- uart# and consoledev

  0 - ttyS0

  1 - ttyS1

  2 - ttyS2

  3 - ttyS3

- ethact and netdev

7.19.1 RAMboot

COMX-P4080 has a U-Boot variable called "ramboot".

```
setenv bootargs root=/dev/ram rw console=$consoledev,$baudrate
$hwbootargs $othbootargs;tftp $ramdiskaddr $ramdiskfile;tftp
$loadaddr $bootfile;tftp $fdtaddr $fdtfile;bootm $loadaddr
$ramdiskaddr $fdtaddr
```

"ramboot" will first load RAMDISK, Linux kernel and DTB into RAM through network by TFTP then boot.

The following are the critical environment variables for "ramboot":

ethact	-	Active ethernet port
ramdiskfile	-	RAMDISK file name on TFTP server
bootfile	-	Linux kernel file name on TFTP server
fdtfile	-	DTB file name on TFTP server

The following are examples of critical environment variables.

```
=> setenv ethact FM1@DTSEC1
=> setenv ramdiskfile comx_p4080/COMX_P4080_V100R00/rootfs_ext2.img
=> setenv bootfile comx_p4080/COMX_P4080_V100R00/uImage
=> setenv fdtfile comx_p4080/COMX_P4080_V100R00/comx.dtb
```

7.19.2 NORboot

COMX-P4080 has a U-Boot variable called "norboot"

```
setenv bootargs root=/dev/ram rw console=$consoledev,$baudrate
$hwbootargs $othbootargs;bootm $norbootaddr $norfsaddr $norfdtaddr
```

"norboot" will load RAMDISK, Linux kernel and DTB from NOR Flash into RAM then boot.

The following are the critical environment variables for "norboot".

norfsaddr	-	RAMDISK address on NOR FLASH
norbootaddr	-	Linux kernel address on NOR FLASH
norfdtaddr	-	DTB address on NOR FLASH

The following are examples of critical environment variables.

=> setenv norfsaddr E9000000

=> setenv norbootaddr EE000000

=> setenv norfdtaddr EFD00000

7.19.3 NANDboot

COMX-P4080 has a U-Boot variable called "nandboot".

```
nandboot=setenv bootargs root=/dev/$jffs2nand rw
console=$consoledev,$baudrate rootfstype=jffs2 $hwbootargs
$othbootargs;bootm $norbootaddr - $norfdtaddr
```

The "nandboot" will load Linux kernel and DTB from NOR flash into RAM and then boot. JFFS2 will then mount on the file system on NAND flash as rootfs.

The following are the critical environment variables for "nandboot".

jffs2nand	-	MTD device for JFFS2 rootfs on NAND FLASH
norbootaddr	-	Linux kernel address on NOR FLASH
norfdtaddr	-	DTB address on NOR FLASH

Below are examples of critical environment variables:

=> setenv jffs2nand mtdblock7

=> setenv norbootaddr EE000000

=> setenv norfdtaddr EFD00000

7.19.4 NFSboot

COMX-P4080 has a U-Boot variable called "nfsboot".

```
setenv bootargs root=/dev/nfs rw nfsroot=$serverip:$rootpath
ip=$ipaddr:$serverip:$gatewayip:$netmask:$hostname:$netdev:off
console=$consoledev,$baudrate $hwbootargs $othbootargs;tftp
$loadaddr $bootfile;tftp $fdtaddr $fdtfile;bootm $loadaddr -
$fdtaddr
```

The "nfsboot" will load Linux kernel and DTB into RAM via network by TFTP and then boot. NFS will then mount on the remote server as rootfs.

The following are the critical environment variables for "nfsboot".

ethact	-	Active ethernet port
netdev	-	The NFS mounting network port
bootfile	-	Linux kernel file name on TFTP server
fdtfile		DTB file name on TFTP server
rootpath		The NFS path the remote server exports

Below are examples of critical environment variables.

=> setenv ethact FM1@DTSEC1

=> setenv netdev eth0

=> setenv bootfile comx_p4080/COMX_P4080_V100R00/uImage

=> setenv fdtfile comx_p4080/COMX_P4080_V100R00/comx.dtb

=> setenv rootpath /tftpboot/comx_p4080/rootfs_nfs

7.19.5 USBFATboot and USBEXT2boot

COMX-P4080 has a U-Boot variable called "usbfatboot".

```
setenv bootargs root=/dev/$usbbdev rw rootdelay=30
console=$consoledev,$baudrate $hwbootargs $othbootargs;usb
start;fatload usb 0:1 $loadaddr /boot/$bootfile;fatload usb 0:1
$fdtaddr  /boot/$fdtfile;bootm $loadaddr - $fdtaddr
```

COMX-P4080 has a U-Boot variable called "usbext2boot".

```
setenv bootargs root=/dev/$usbbdev rw rootdelay=30
console=$consoledev,$baudrate $hwbootargs $othbootargs;usb
start;ext2load usb 0:2 $loadaddr /boot/$bootfile;ext2load usb 0:2
$fdtaddr  /boot/$fdtfile;bootm $loadaddr - $fdtaddr
```

The "usbfatboot" will load Linux kernel and DTB from the FAT partition (1st partition) on USB stick into RAM and then boot. EXT2 partition (2nd partition) will be mounted on the USB stick as rootfs.

The "usbext2boot" will load Linux kernel and DTB from the EXT2 partition (2nd partition) on USB stick into RAM and then boot. Mounting it on the same partition on this USB stick will boot as rootfs

The following are the critical environment variables for "usbfatboot" and "usbext2bot".

bootfile	-	Linux kernel file name
fdtfile	-	DTB file name

Below are examples of critical environment variables.

=> setenv bootfile COMX_P4080_V100R00/uImage

=> setenv fdtfile COMX_P4080_V100R00/comx.dtb

Users need to create two partitions on the USB stick. FAT32 is the first partition and the EXT2 is the second partition. Both partitiions contain a directory /boot/ and the directory has kernel DTB files. EXT2 partition contains the rootfs which can be from rootfs_nfs.tar.gz

7.19.6 MMCFATboot and MMCEXT2boot

COMX-P4080 has a U-Boot variable called "mmcfatboot".

```
setenv bootargs root=/dev/$mmcbdev rw rootdelay=30
console=$consoledev,$baudrate $hwbootargs
$othbootargs;mmcinfo;fatload mmc 0:1 $loadaddr
/boot/$bootfile;fatload mmc 0:1 $fdtaddr  /boot/$fdtfile;bootm
$loadaddr - $fdtaddr
```

COMX-P4080 also has a U-Boot variable called "mmcext2boot".

```
setenv bootargs root=/dev/$mmcbdev rw rootdelay=30
console=$consoledev,$baudrate $hwbootargs
$othbootargs;mmcinfo;ext2load mmc 0:2 $loadaddr
/boot/$bootfile;ext2load mmc 0:2 $fdtaddr  /boot/$fdtfile;bootm
$loadaddr - $fdtaddr
```

The "mmcfatboot" will load Linux kernel and DTB from the FAT partition (1st partition) on MMC/SDHC card into RAM and then boot. EXT2 partition (2nd partition) will mount on this card as rootfs.

"mmcext2boot" will load Linux kernel and DTB from the EXT2 partition (2nd partition) on MMC/SDHC card into RAM and then boot. The same partition will mount on this card as rootfs.

The following are the critical environment variables for "mmcfatboot" and "mmcext2boot".

bootfile	-	Linux kernel file name
fdtfile	-	DTB file name

Below are examples of critical environment variables.

```
=> setenv bootfile COMX_P4080_V100R00/uImage
=> setenv fdtfile COMX_P4080_V100R00/comx.dtb
```

Similar to the USB drive, users need to create two partitions on the MMC/SDHC card. FAT32 is the first partition and the EXT2 is the second partition. Both partitiions contain a directory /boot/ and the directory has kernel DTB files. EXT2 partition contains the rootfs which can be from rootfs_nfs.tar.gz.

Firmware Upgrade

8.1 Overview

This section describes in detail the procedures on how to upgrade the COMX-P4080 COM Express Module firmware.

8.2 Upgrade Procedure

1. Go to http://www.artesyn.com/computing
2. Navigate to the Customer Resource Center. First time visitors will need to register for a CRC account.
3. Download the latest BSP package COMX_P4080_<Version_Number>.tar.gz. The version number is formatted as VxxxBxx or VxxxRxx (for example: V100B13, V100R00).
4. Attach the board to the network using a network cable to the onboard RGMII Ethernet port.
5. Set up a TFTP server in this network. Assuming that the IP address of this server is 192.168.0.100 and the root directory is `/tftpboot/`. Create a subdirectory `comx_p4080/` in `/tftpboot/`.
6. Copy the released file COMX_P4080_<Version_Number>.tar.gz into the directory `/tftpboot/comx_p4080/` on this server.
7. Change current directory to `/tftpboot/comx_p4080/`.
8. Decompress the .tar.gz file to the current directory. The following files should be present:
   - comx.dtb
   - rcw.bin
   - rootfs_ext2.img
   - rootfs_nfs.tar.gz
   - uImage
   - fsl_fman_ucode_P4080_101_6.bin
   - ReleaseNotes.txt
   - rootfs_jffs2.nand
   - u-boot.bin

9. All the commands in the following steps should be run in the U-Boot command line.
10. Set the U-Boot environment variables for the network settings.

```
=> setenv ethaddr         00:01:af:12:23:01
=> setenv ipaddr          192.168.0.99
=> setenv netmask         255.255.255.0
=> setenv gatewayip       192.168.0.1
=> setenv serverip        192.168.0.100
=> setenv ethact          FM1@DTSEC1
```

11. Set up the U-Boot environment variables for upgrade files.

```
=> setenv rcwfile comx_p4080/COMX_P4080_<Version_Number>/rcw.bin
=> setenv fmanfile
comx_p4080/COMX_P4080_<Version_Number>/fsl_fman_ucode_P4080_101_6.bi
n
=> setenv bootfile comx_p4080/COMX_P4080_<Version_Number>/uImage
=> setenv norfsfile
comx_p4080/COMX_P4080_<Version_Number>/rootfs_ext2.img
=> setenv fdtfile comx_p4080/COMX_P4080_<Version_Number>/comx.dtb
=> setenv ubootfile comx_p4080/COMX_P4080_<Version_Number>/u-boot.bin
=> setenv nandfsfile
comx_p4080/COMX_P4080_<Version_Number>/rootfs_jffs2.nand
```

12. Test that the network and filename settings can download the files successfully using the following commands.

```
=> tftpboot $loadaddr $rcwfile
=> tftpboot $loadaddr $fmanfile
=> tftpboot $loadaddr $bootfile
```

```
=> tftpboot $loadaddr $norfsfile
=> tftpboot $loadaddr $fdtfile
=> tftpboot $loadaddr $ubootfile
=> tftpboot $loadaddr $nandfsfile
```

13. Individually upgrade RCW, FMAN uCode, kernel, RAMDISK image, U-Boot and device tree blob on NOR flash using this command:
    ```
    => run updrcw; run updfman; run updkernel; run updnorfs; run updfdt; run updubootl
    ```
14. Upgrade NAND flash image. It may take several minutes.
    ```
    => run updnandfs
    ```
15. Erase previous u-boot environment settings.
    ```
    => run eraenv
    ```
16. Reset the board.
    ```
    => reset
    ```
17. The board will boot up with the new BSP.

- All U-Boot environment willbe set to factory default during the upgrade procedure. If there have been changes made before the upgrade, make note to them so it can be re-applied afterwards.

Related Documentation

A.1 Artesyn Embedded Technologies - Embedded Computing Documentation

The publications listed below are referenced in this manual. You can obtain electronic copies of Artesyn Embedded Technologies - Embedded Computing publications by contacting your local Artesyn sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Go to www.artesyn.com/computing.
2. Under SUPPORT, click TECHNICAL DOCUMENTATION.
3. Under FILTER OPTIONS, click the Document types drop-down list box to select the type of document you are looking for.
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Table A-1 Artesyn Embedded Technologies - Embedded Computing Publications

Document Title	Publication Number
COMX-P4080 COM Express Module Safety Notes Summary	6806800L76A
COMX-P4080 Quick Start Guide	6806800L26A

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