Ordering number : EN6193B

# LB1945H

ON Semiconductor®

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**Monolithic Digital IC**

## PWM Current Control Type
## Stepping Motor Driver

### Overview

The LB1945H is a PWM current control type stepping motor driver.

### Feature

- PWM current control (external excitation)
- Load current digital selection (1-2, W1-2, and 2 phase excitation drives possible)
- Built-in upper/lower diode
- Simultaneous ON prevention function (feed-through current prevention)
- Built-in thermal shutdown circuit
- Built-in noise canceler

### Specifications

**Absolute Maximum Ratings** at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum motor supply voltage | $V_{BB}$ max | | 30 | V |
| Output peak current | $I_O$ peak | $t_W \leq 20\mu s$ | 1.0 | A |
| Output continuous current | $I_O$ max | | 0.8 | A |
| Logic supply voltage | $V_{CC}$ max | | 6.0 | V |
| Logic input voltage range | $V_{IN}$ max | | -0.3 to $V_{CC}$ | V |
| Emitter output voltage | $V_E$ max | | 1.0 | V |
| Allowable power dissipation | Pd max | Mounted on a specified board * | 1.9 | W |
| Operating temperature | Topr | | -20 to +90 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

* Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## Allowable Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Motor supply voltage | $V_{BB}$ | | 10 to 28 | V |
| Logic supply voltage | $V_{CC}$ | | 4.75 to 5.25 | V |
| Reference voltage | $V_{REF}$ | | 1.5 to 5.0 | V |

## Electrical Characteristics at Ta = 25°C, $V_{BB}$ = 24V, $V_{CC}$ = 5V, $V_{REF}$ = 5.0V

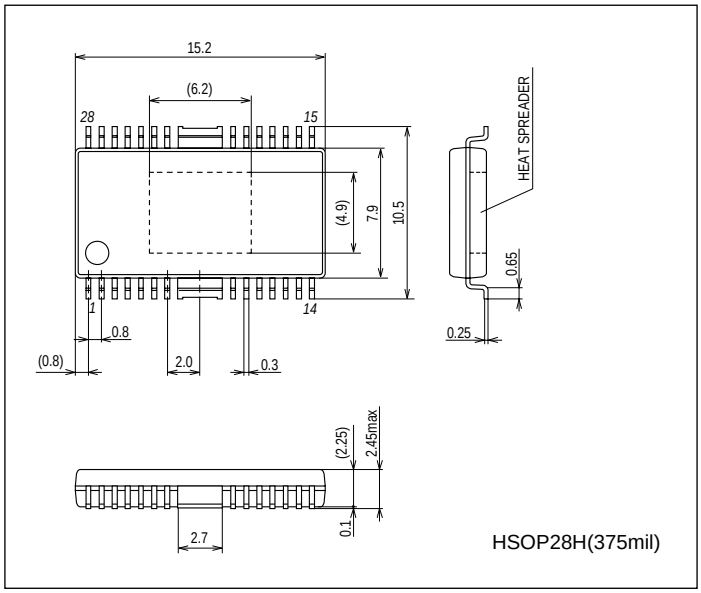
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| **Output Block** | | | | | | |
| Output stage supply current | $I_{BB}$ ON | $I_1$ = 0.8V, $I_2$ = 0.8V, ENABLE = 0.8V | 0.5 | 1.0 | 2.0 | mA |
| | $I_{BB}$ OFF | ENABLE = 3.2V | | | 0.2 | mA |
| Output saturation voltage | $V_O$sat1 | $I_O$ = +0.5A, sink | | 0.3 | 0.5 | V |
| | $V_O$sat2 | $I_O$ = +0.8A, sink | | 0.5 | 0.7 | V |
| | $V_O$sat3 | $I_O$ = -0.5A, source | | 1.6 | 1.8 | V |
| | $V_O$sat4 | $I_O$ = -0.8A, source | | 1.8 | 2.0 | V |
| Output leakage current | $I_O$1(leak) | $V_O$ = $V_{BB}$, sink | | | 50 | µA |
| | $I_O$2(leak) | $V_O$ = 0V, source | -50 | | | µA |
| Output sustain voltage | $V_{SUS}$ | L = 3.9mH, $I_O$ = 1.0A, Design guarantee value * | 30 | | | V |
| **Logic Block** | | | | | | |
| Logic supply current | $I_{CC}$ ON | $I_1$ = 0.8V, $I_2$ = 0.8V, ENABLE = 0.8V | 50 | 70 | 92 | mA |
| | $I_{CC}$ OFF | ENABLE = 3.2V | 7 | 10 | 13 | mA |
| Input voltage | $V_{IH}$ | | 3.2 | | | V |
| | $V_{IL}$ | | | | 0.8 | V |
| Input current | $I_{IH}$ | $V_{IH}$ = 3.2V | 35 | 50 | 65 | µA |
| | $I_{IL}$ | $V_{IL}$ = 0.8V | 7 | 10 | 13 | µA |
| Set current control threshold value | Vref/Vsen | $I_1$ = 0.8V, $I_2$ = 0.8V | 9.5 | 10 | 10.5 | |
| | | $I_1$ = 3.2V, $I_2$ = 0.8V | 13.5 | 15 | 16.5 | |
| | | $I_1$ = 0.8V, $I_2$ = 3.2V | 25.5 | 30 | 34.5 | |
| Reference current | Iref | Vref = 5.0V, $I_1$ = 0.8V, $I_2$ = 0.8V | 17.5 | 25 | 32.5 | µA |
| CR pin current | $I_{CR}$ | CR = 1.0V | -1.0 | | | mA |
| Thermal shutdown temperature | T-TSD | Design guarantee value * | | 170 | | °C |
| Temperature hysteresis width | Ts hys | | | 40 | | °C |

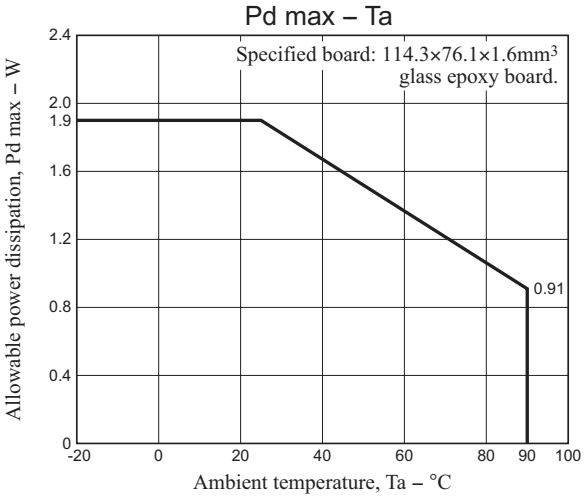
* Design guarantee value, Do not measurement.

## Package Dimensions

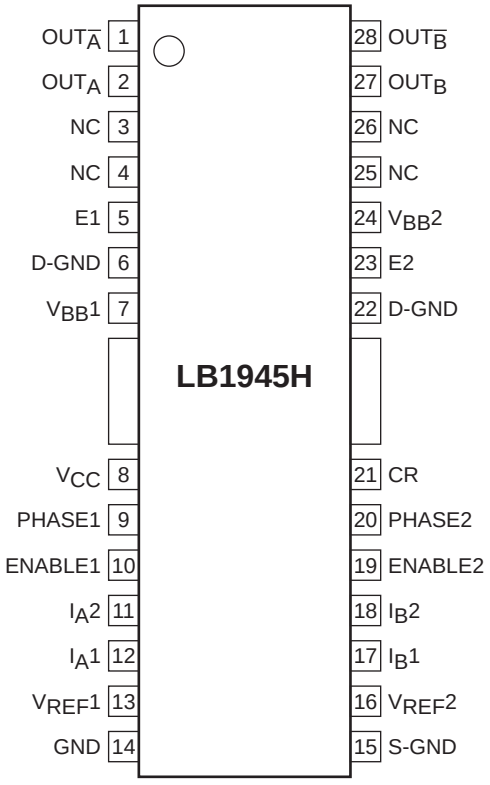
unit : mm (typ)

3233B

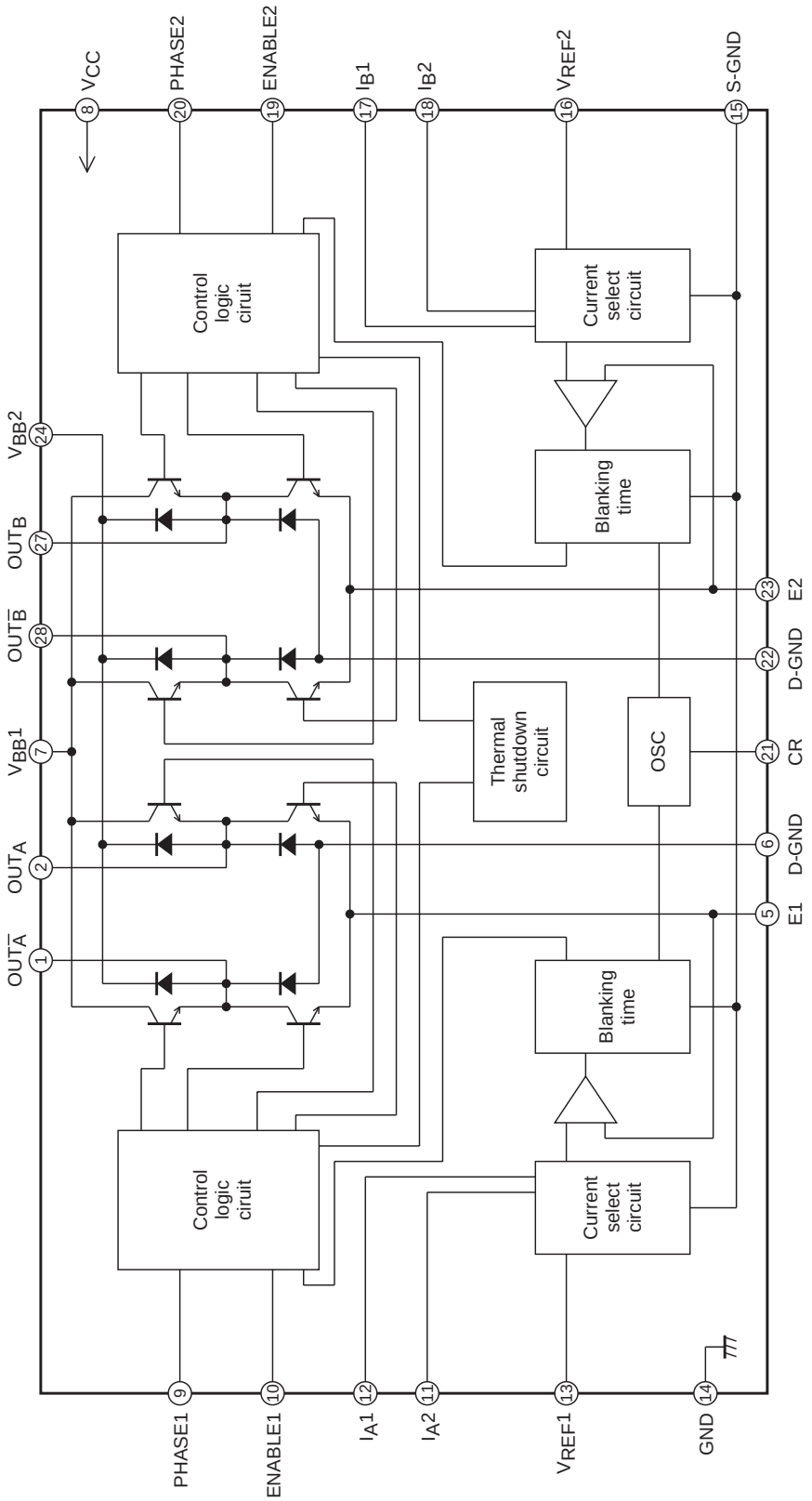



## Pin Assignment



## Block Diagram



## Truth Table

| ENABLE | PHASE | $OUT_A$ | $OUT_{\overline{A}}$ |
|---|---|---|---|
| L | H | H | L |
| L | L | L | H |
| H | – | OFF | OFF |

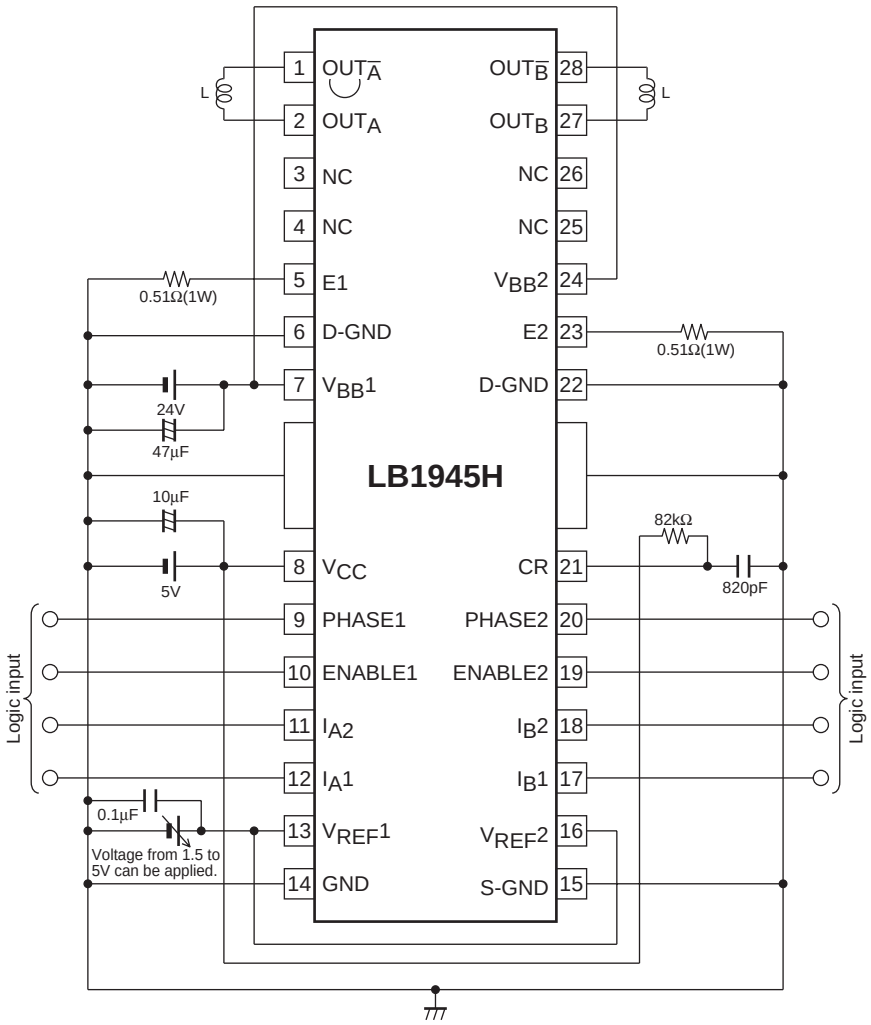
| $I_1$ | $I_2$ | Output current |
|---|---|---|
| L | L | Vref / (10 × RE) = $I_{OUT}$ |
| H | L | Vref / (15 × RE) = $I_{OUT}$ × 2/3 |
| L | H | Vref / (30 × RE) = $I_{OUT}$ × 1/3 |
| H | H | 0 |

Note: Output is OFF when ENABLE = H or when $I_1$ = $I_2$ = H.

## Pin Function

| Pin No. | Pin name | Function |
|---|---|---|
| 7 | $V_{BB}1$ | Output stage power supply voltage pin. |
| 24 | $V_{BB}2$ | Cathode pin for the upper-side diodes. |
| 5<br>23 | E1<br>E2 | Insert resistor RE between these pins and ground to control set current. |
| 2<br>1<br>27<br>28 | $OUT_A$<br>$OUT_{\overline{A}}$<br>$OUT_B$<br>$OUT_{\overline{B}}$ | Output pins. |
| 14 | GND | Ground pin. |
| 15 | S-GND | Sense ground pin. |
| 6<br>22 | D-GND<br>D-GND | Lower-side internal diode ground (anode). |
| 21 | CR | Triangular wave chopping with CR constant setting.<br>Triangular wave OFF time is noise cancel time. |
| 13<br>16 | $V_{REF}1$<br>$V_{REF}2$ | Output current setting pins.<br>(Output current is set by inputting a 1.5V to 7.5V voltage.) |
| 9<br>20 | PHASE1<br>PHASE2 | Output phase select input pin.<br>High input: $OUT_A$ = H, $OUT_{\overline{A}}$ = L<br>Low input: $OUT_A$ = L, $OUT_{\overline{A}}$ = H |
| 10<br>19 | ENABLE1<br>ENABLE2 | Output ON/OFF setting input pins.<br>High input: output OFF<br>Low input: output ON |
| 12,11<br>17,18 | $I_A1$,$I_A2$<br>$I_B1$,$I_B2$ | Output current setting digital input pins.<br>Current is set to 1/3, 2/3, 1 by High and Low combinations. |
| 8 | $V_{CC}$ | Logic block power supply voltage pin. |

## Application Circuit Example




The fin on the bottom of HSOP-28H package and the fins between pins 7 and 8 and 21 and 22 should be grounded.

## Usage Notes

1. VREF pin
   Because the VREF pin is used as reference voltage input pin for the current setting, care must be taken to prevent noise from affecting the input.

2. GND pin
   Because this IC switches large currents, the ground pattern must be designed with care. The fin on the bottom of the package and the fins between pins 7 and 8 and 21 and 22 should be grounded. Low-impedance patterns should be used in blocks where large currents flow, and these blocks should be separated from low-level signal blocks. In particular, the ground of the sense resistor RE at pin E should be located close to the IC ground. Pattern layout should be designed so that the capacitors between $V_{CC}$ and ground and $V_{BB}$ and ground are close to $V_{CC}$ and $V_{BB}$.

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