

# 3 A, 1.2 MHz/600 kHz, High Efficiency, Synchronous, Step-Down DC-to-DC Regulator

**Data Sheet** 

# **ADP2118**

### **FEATURES**

**3 A continuous output current** 75 m $\Omega$  and 40 m $\Omega$  integrated FET ±1.5% output accuracy Input voltage range from 2.3 V to 5.5 V Output voltage from 0.6 V to V<sub>IN</sub> 600 kHz or 1.2 MHz fixed switching frequency Synchronizable between 600 kHz and 1.4 MHz Selectable synchronize phase shift: 0° or 180° Selectable PWM or PFM mode operation **Current mode architecture Precision enable input** Power good output Voltage tracking input Integrated soft start Internal compensation Starts up into a precharged output UVLO, OVP, OCP, and thermal shutdown Available in 16-lead, 4 mm × 4 mm LFCSP package Supported by ADIsimPower design tool

#### **APPLICATIONS**

Point of load conversion **Communications and networking equipments** Industrial and instrumentation **Consumer electronics** Medical appliances

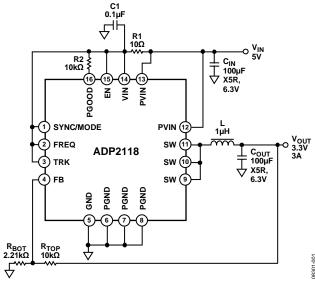


Figure 1. Typical Applications Circuit

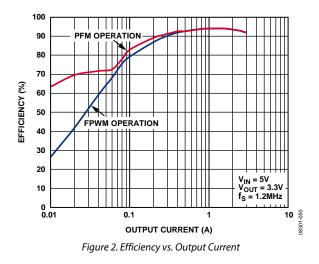
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#### **GENERAL DESCRIPTION**

The ADP2118 is a low quiescent current, synchronous, step-down dc-to-dc regulator in a compact 4mm × 4mm LFCSP package. It uses a current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient response. Under light loads, the ADP2118 can be configured to operate in pulse frequency modulation (PFM) mode that reduces switching frequency to save power.

The ADP2118 runs from input voltages of 2.3 V to 5.5 V. The output voltage of the ADP2118ACPZ-R7 is adjustable from 0.6 V to input voltage (V<sub>IN</sub>), and the ADP2118ACPZ-x.x-R7 are available in preset output voltage options of 1.2 V and 3.3 V. The ADP2118 requires minimal external parts and provides a high efficiency solution with its integrated power switch, synchronous rectifier, and internal compensation. The IC draws less than 3  $\mu$ A from the input source when it is disabled. Other key features include undervoltage lockout (UVLO), integrated soft start to limit inrush current at startup, overvoltage protection (OVP), overcurrent protection (OCP), and thermal shutdown (TSD).



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## **REVISION HISTORY**

## 7/2018—Rev. D to Rev. E

Changes to General Description Section	1
Updated Outline Dimensions	21
Changes to Ordering Guide	21

#### 6/2017-Rev. C to Rev. D

Changed LFCSP_WQ to LFCSP	Throughout
Updated Outline Dimensions	
Changes to Ordering Guide	

#### 11/2012—Rev. B to Rev. C

Changed Ordering Guide
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Tracking1
Oscillator and Synchronization 1
Current Limit and Short-Circuit Protection
Overvoltage Protection (OVP)1
Undervoltage Lockout (UVLO) 1
Thermal Shutdown1
Power Good1
Applications Information1
ADIsimPower Design Tool 1
Output Voltage Selection1
Inductor Selection 1
Output Capacitor Selection1
Input Capacitor Selection1
Voltage Tracking1
Typical Application Circuits 1
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Ordering Guide 2

7/2012—Rev. A to Rev. B	
Changes to Features Section	1
Added ADIsimPower Design Tool Section	
10/2009—Rev. 0 to Rev. A	

Changed Converter to Regulator (Throughout)1
Changes to Applications Section1

7/2009—Revision 0: Initial Version

## **SPECIFICATIONS**

 $VIN = PVIN = 3.3 V, EN = VIN, SYNC/MODE = high @ T_J = -40^{\circ}C to + 125^{\circ}C, unless otherwise noted. Typical values are at T_J = 25^{\circ}C.$ 

ParameterSymbolTest Conditions/CommentsMinTypMaxUnitVIN AND PVIN2.35.5VVIN Voltage RangeVINNo switching, SYNC/MODE = GND2.35.5VQuiescent CurrentIvinNo switching, SYNC/MODE = high60900µAVIN Undervoltage Lockout ThresholdUVLNo switching, SYNC/MODE = high0.33µAVIN Undervoltage Lockout ThresholdUVLVIN rising2.22.1VOUTPUT CHARACTERISTICSI.= 1.5 A0.05%A%ALine Regulation'I.= 1.5 A0.05%A%AFB Regulation VoltageVmVIN = 2.3 V to 5.5 V0.5910.60.609VFB Regulation VoltageVmVIN = 2.3 V to 5.5 V0.5110.60.609VFB Regulation VoltageVmVIN = PVIN = 3.3 V, kw = 500 mA75110mQSW Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, kw = 500 mA75100%ASW Maximum Duty CycleVIN = PVIN = 3.3 V, kw = 500 mA75100%ASW Maximum Duty CycleVIN = PVIN = 5.5 V, full frequency100mQSW Maximum Duty CycleVIN = PVIN = 5.5 V, full frequency100mASW Maximum Duty CycleVIN = PVIN = 5.5 V, full frequency100mASW Maximum Duty CycleVIN = PVIN = 5.5 V, full frequency100mASW Maximum Duty CycleVIN = PVIN = 5.5 V, full frequency100mASW Maximum Duty CycleVIN	Table 1.						
VIN Voltage Range PVINVIN PVIN2.35.5VQuiescent Current IVIN PVIN PVIN PS.SV, CMODE = GND Switching, no laad, SVNC/MODE = high VIN = SV, EN = GND100150µANo switching, no laad, SVNC/MODE = high VIN = SV, EN = GND0.33µAVIN Undervoltage Lockout ThresholdUVIVIN = SV, EN = GND2.22.3VOUTPUT CHARACTERISTICS Load Regulation'L-0 A to 3 A0.05%/V%/VFBFB Regulation VoltageVinVIN = 2.3 V to 5.5 V0.5910.60.609VFBFB Regulation VoltageVinVIN = 2.3 V to 5.5 V0.5910.60.609VFBFB Regulation VoltageVinVIN = PVIN = 3.3 V, Isw = 500 mA4.06.0mO1SWFBVIN = PVIN = 3.3 V, Isw = 500 mA4.06.0mO1mO1SW Maximum Duty CycleVIN = PVIN = 5.5 V, Iuli frequency100rsrsTRKTRK to FB Offset VoltageTRK = 0 mV to 500 mV-10-10nATRK to FB Offset VoltageFREQ = GND1.01.01.21.4SYNC/MODEFREQ = GND1.01.4MHzSYNC/MODESYNC Injing threshold1.01.2-VVSYNC Injing threshold1.2-VV-V1.01.4TRK to FB Offset VoltageFREQ = GND1.01.2-VVSYNC Injing threshold1.01.2-VVSYNC Injing threshold <t< th=""><th>Parameter</th><th>Symbol</th><th>Test Conditions/Comments</th><th>Min</th><th>Тур</th><th>Max</th><th>Unit</th></t<>	Parameter	Symbol	Test Conditions/Comments	Min	Тур	Max	Unit
PVIN Vortage Range Quiescent Current     PVIN Ivw     No switching, SYNC/MODE = GND Switching, no load, SYNC/MODE = high Switching, no load, SYNC/MODE = high Switching, no load, SYNC/MODE = high VIN Undervoltage Lockout Threshold     100     150     µA       Shutdown Current VIN Undervoltage Lockout Threshold     UVI     PVIN VIN S5.V, EN = GND     22     2.1     V       OUTPUT CHARACTERISTICS Load Regulation <sup>1</sup> L, = 0 A to 3 A     0.05     %(A       Line Regulation Voltage     V:n     VIN = 2.3 V to 5.5 V     0.01     0.1     µA       FB     Fa     -     0.05     %(A     -     %(A       High-Side On Resistance <sup>2</sup> V:n     VIN = PVIN = 3.3 V, low = 500 mA     -     0.01     0.1     µA       SW Maximum Duty Cycle     VIN = PVIN = 3.3 V, low = 500 mA     40     60     mΩ       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     ns     ns       TRK to FB Offset Voltage     TRK = 0 mV to 500 mV     -     -     +00     mV       SW Minimum On Time <sup>1</sup> TRK = 0 mV to 500 mV     -     1.0     1.2     .4     V       SPREA Current Imit	VIN AND PVIN						
Quiescent Current     Ivm     No switching, SVNC/MODE = ADD     100     150     μA       Shutdown Current     Isnon     VIN = PVIN = 5.5 V, EN = GND     0.3     3     μA       VIN Undervoltage Lockout Threshold     UVLD     VIN rising     2.2     2.3     V       OUTPUT CHARACTERISTICS     I.a = 0 A to 3 A     0.08     %/A     %/A       Line Regulation'     I.a = 0 A to 3 A     0.05     %/A       FB     FB     Vin     VIN = 2.3 V to 5.5 V     0.51     0.6     0.609     V       FB     FB     Vin     VIN = 2.3 V to 5.5 V     0.51     0.6     0.609     V       FB     Vin     Vin     PVIN = 3.3 V, Isw = 500 mA     40     60     mQ       SW     VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mQ     %/A       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     ns     mV       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     n     n       FREQ Input Low Voltage Range     TRK to FB Offset Voltage <t< td=""><td>VIN Voltage Range</td><td>VIN</td><td></td><td>2.3</td><td></td><td>5.5</td><td>V</td></t<>	VIN Voltage Range	VIN		2.3		5.5	V
Shutdown Current     Switching, no load, SYNC/MODE = high NN PerVIN = 5.5 V, En = GND     680     900     µA       Shutdown Current     VIN Undervoltage Lockout Threshold     VIN Falling     2     2.1     V       OUTPUT CHARACTERISTICS     La = 0 A to 3 A     0.08     %/A       Load Regulation <sup>1</sup> La = 0 A to 3 A     0.05     %/A       FB     Fggulation Voltage     V:n     VIN = 2.3 V to 5.5 V     0.51     0.6     0.609     V       FB     Fggulation Voltage     V:n     VIN = PVIN = 3.3 V, bar = 500 mA     4     5.2     6.4     A       SW     High-Side On Resistance <sup>3</sup> VIN = PVIN = 3.3 V, bar = 500 mA     4     5.2     6.4     A       SW Adaximum Dutty Cycle     VIN = PVIN = 5.5 V, full frequency     100     m0     m0       SW Maximum Dutty Cycle     VIN = PVIN = 5.5 V, full frequency     100     n     n       SW Minimum On Time <sup>3</sup> TRK = 0 mV to 500 mV     -10     +10     mV     mV       FREQ Input Voltage Range     FREQ = VIN     1.0     1.2     1.4     MHz       Synchronization	PVIN Voltage Range	PVIN		2.3		5.5	V
Shutown Current VIN Undervoltage Lockout Threshold     VIN = PVIN = 5.5 V, EN = GND     0.3     3     μA       VIN Undervoltage Lockout Threshold     VIN = Start     2.2     2.3     V       OUTPUT CHARACTERISTICS Load Regulation <sup>1</sup> I.= 0 A to 3 A     0.08     V     9%/A       Line Regulation <sup>1</sup> I.= 1.5 A     0.05     %/A     9%/A       FB     FB regulation Voltage     Vis     VIN = 2.3 V to 5.5 V     0.591     0.66     0.609     V       FB     FB accurrent     Ina     VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       SW     High-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     4     5.2     6.4     A       SW Maximum Duity Cycle     VIN = PVIN = 5.5 V, full frequency     100     mΩ     mV     mQ     mQ     mV     mQ     100     mQ     mV     mQ     mQ     mQ     mQ     100     mA     100     nA     100     nA     mQ     100     mQ     100     nA     100     nA     100     100     mQ     100	Quiescent Current	Ivin	No switching, SYNC/MODE = GND		100	150	μA
VIN Undervoltage Lockout Threshold     UVLO     VIN rising VIN falling     2.2     2.3     V       OUTPUT CHARACTERISTICS Load Regulation <sup>1</sup> I <sub>e</sub> = 0 A to 3 A     0.08     96/A       Line Regulation <sup>1</sup> I <sub>e</sub> = 0 A to 3 A     0.08     96/A       Line Regulation <sup>1</sup> I <sub>e</sub> = 1.5 A     0.05     96/V       FB     FB     1.6     0.09     V       FB Regulation Voltage     V:#     VIN = 2.3 V to 5.5 V     0.591     0.6     0.600     V       SW     FB     VIN = PVIN = 3.3 V, Isy = 500 mA     75     110     mΩ       Low-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isy = 500 mA     40     60     mΩ       SW Pask Current Limit     High-side switch, VIN = PVIN = 3.3 V     4     4     5.2     6.4     A       SW Maximum Dut Cycle     VIN = PVIN = 5.5 V, full frequency     100     mΩ     96/A       SW Maximum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     nA     4     5.2     6.4     A       SW Maximum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     nA     <			Switching, no load, SYNC/MODE = high		680	900	μA
VIN falling     2     2.1     V       OUTPUT CHARACTERISTICS Lad Regulation <sup>1</sup> I, = 0 A to 3 A I, = 1.5 A     0.08     %/A       FB     Egulation Voltage     V:=     VIN = 2.3 V to 5.5 V     0.591     0.6     0.609     V       FB     Fgulation Voltage     V:=     VIN = 2.3 V to 5.5 V     0.591     0.6     0.609     V       FB Bis Current     Ins     VIN = PVIN = 3.3 V, Isw = 500 mA     75     110     mΩ       SW     VIN = PVIN = 3.3 V, Isw = 500 mA     75     110     mΩ       SW Askinum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %       SW Maximum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     ns       TRK Input Voltage Range     TRK = 0 mV to 500 mV     -10     nV     mV       TRK Input Voltage Range     TRK = 0 mV to 500 mV     -10     nV     mV       TRK Input Bias Current     FREQ = MV     1.0     1.2     1.4     MHz       Socilator Frequency     FREQ = GND     500     600     rNO     rK       Synchronization Range <td>Shutdown Current</td> <td>ISHDN</td> <td>VIN = PVIN = 5.5 V, EN = GND</td> <td></td> <td>0.3</td> <td>3</td> <td>μA</td>	Shutdown Current	ISHDN	VIN = PVIN = 5.5 V, EN = GND		0.3	3	μA
OUTPUT CHARACTERISTICS Load Regulation'     I₀ = 0 Å to 3 Å     0.08     %/A       Line Regulation'     I₀ = 0 Å to 3 Å     0.05     %/V       FB     FB Regulation Voltage     V:#     VIN = 2.3 V to 5.5 V     0.51     0.6     0.609     V       FB Bias Current     Ina     VIN = 2.3 V to 5.5 V     0.51     0.6     0.609     V       SW     High-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mÅ     75     110     mΩ       SW Peak Current Limit     VIN = PVIN = 3.3 V, Isw = 500 mÅ     4     5.2     6.4     A       SW Maximum Dut Cycle     VIN = PVIN = 5.5 V, full frequency     100     ns     ns       SW Minimum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     ns     ns       TRK to FB Offset Voltage     TRK to FB Offset Voltage     nV     nHigh-side switch, VIN = PVIN = 5.5 V, full frequency     100     nA       FREQ Input High Voltage Range     TRK to FB Offset Voltage     N     N     nV     nHiz       FREQ Input High Voltage     FREQ = VIN     1.0     1.2     1.4     MHz       Synt	VIN Undervoltage Lockout Threshold	UVLO	VIN rising		2.2	2.3	V
Load Regulation <sup>1</sup> Is = 0 A to 3 A     0.08     %/A       Line Regulation <sup>1</sup> Is = 1.5 A     0.05     %/A       FB     FB Regulation Voltage     Vm     VIN = 2.3 V to 5.5 V     0.591     0.6     0.609     V       FB Regulation Voltage     Vm     VIN = 2.3 V to 5.5 V     0.591     0.6     0.609     V       SW     Im     VIN = PVIN = 3.3 V, Isw = 500 mA     75     110     mQ       SW Peak Current Limit     VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mQ       SW Maimum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %     ms       SW Minimum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     ms     ms       TRK     FREQUENCY     100     FREQUENCY     100     mV     mV       Gallator Frequency     FREQ = VIN     1.0     1.2     1.4     MHz       FREQ Input High Voltage     FREQ = GND     500     600     700     H412       SYNC/MODE     Synchronization Range     1.4     MHz     ms     ms			VIN falling	2	2.1		V
Line Regulation¹     Is = 1.5 A     0.05     %/V       FB     FB Regulation Voltage     Vis     VIN = 2.3 V to 5.5 V     0.591     0.6     0.609     V       FB Bias Current     Is     VIN = 2.3 V to 5.5 V     0.591     0.6     0.00     0.1     µA       SW     High-Side On Resistance²     VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       SW Maximum Dut Cycle     VIN = PVIN = 5.5 V, full frequency     100     mO     %       SW Minimum On Time³     VIN = PVIN = 5.5 V, full frequency     100     %     mV       TRK to FB Offset Voltage Range     TRK to FB Offset Voltage     6.600     mV     mV       TRK to FB Offset Voltage     TRK = 0 mV to 500 mV     -10     100     mA       Securent     FREQ = VIN     1.0     1.2     1.4     MHz       FREQ liput High Voltage     FREQ = GND     500     6.00     mV       SVNC/MOUE     Synchronization Range     Synchronization Range     0.6     1.4     MHz       SYNC Kinput High Voltage     FREQ = GND     100     .50	OUTPUT CHARACTERISTICS						
FB     Vra     VIn = 2.3 V to 5.5 V     0.591     0.6     0.609     V       FB Bias Current     Ira     VIN = PVIN = 3.3 V, Isw = 500 mA     0.01     0.1     µA       SW     High-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       SW Peak Current Limit     SW Ack Current Limit     High-side switch, VIN = PVIN = 3.3 V     4     5.2     6.4     A       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %     %       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %     %       TRK     Input Voltage Range     TRK     TRK to F8 Offset Voltage     mV     mV     mV       TRK Input Bias Current     TRK     0     600     mV     mV     mV       FREQ Liput Low Voltage     FREQ = VIN     1.0     1.2     1.4     MHz       SYNC/MODE     Synchronization Range     0.6     1.4     MHz     ns       SYNC Liput Low Voltage     1.2     V     V     SVNC Input Low Voltage     0.4     V	Load Regulation <sup>1</sup>		$I_o = 0 A \text{ to } 3 A$		0.08		%/A
FB Regulation Voltage FB Bias Current     Vin     2.3 V to 5.5 V     0.5 91     0.6 0.609     V       SW     High-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     75     110     mΩ       Low-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     mV       TRK     FB Offset Voltage     n     100     n       TRK to B Offset Voltage     TRK = 0 mV to 500 mV     100     nA       TREQ = VIN     FREQ = VIN     1.0     1.2     1.4     MHz       Socillator Frequency     FREQ = GND     100     nA     N     N       SynC/mODE     SynChronization Range     1.4     MHz     ns     ns       SynCK Input High Voltage     N     1.2     V     V     V       SynCK Input High Voltage     N     1.2     V <td>Line Regulation<sup>1</sup></td> <td></td> <td>I<sub>o</sub> = 1.5 A</td> <td></td> <td>0.05</td> <td></td> <td>%/V</td>	Line Regulation <sup>1</sup>		I <sub>o</sub> = 1.5 A		0.05		%/V
FB BlaS Current     Init     0.01     0.1     μA       SW     High-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       Low-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       SW Peak Current Limit     High-side switch, VIN = PVIN = 3.3 V     4     5.2     6.4     A       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %     %       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %     %       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %     %       TRK Input Voltage Range     TRK = 0 mV to 500 mV     -10     -10     mV     mV       TRK to FB Offset Voltage     TRK = 0 mV to 500 mV     -10     -10     mV     mV       Gocillator Frequency     FREQ = VIN     1.0     1.2     1.4     MHz       FREQ Input High Voltage     FREQ = GND     0.6     1.4     MHz       Sync Minimum Pulse Width     100     ns     ns     s     y <td< td=""><td>FB</td><td></td><td></td><td></td><td></td><td></td><td></td></td<>	FB						
FB Bias Current     Ima     0.01     0.1     μA       SW     Migh-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     75     110     mΩ       SW Maximum Duty Cycle     VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %       SW Minimum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     %       TRK     Ins     600     mV     ns       TRK Input Voltage Range     TRK = 0 mV to 500 mV     100     nA     41     100     nA       TREQUENCY     Oscillator Frequency     FREQ = VIN     1.0     1.2     1.4     MHz       SYNC/MODE     FREQ Input High Voltage     FREQ = GND     0.6     1.4     MHz       SYNC Kinimum OftTime     Synchronization Range     0.6     1.4     V     SYNC Kinimum OftTime       SYNC Kinimum OftTime     All switching frequency     0.4     V     V       SYNC Kinimum OftTime     All switching frequency     0.4     V       SYNC Kinimum OftTime	FB Regulation Voltage	V <sub>FB</sub>	VIN = 2.3 V to 5.5 V	0.591	0.6	0.609	V
High-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     75     110     mΩ       Low-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       SW Peak Current Limit     High-side switch, VIN = PVIN = 3.3 V, Isw = 500 mA     4     5.2     6.4     A       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     mV       TRK     FB Offset Voltage     ns     mV     mV       TRK to B Offset Voltage     TRK = 0 mV to 500 mV     10     -1     mV       TRK to PS Offset Voltage     FREQ = VIN     1.0     1.2     1.4     MHz       FREQ Input High Voltage     FREQ = GND     500     600     700     kHz       SYNC/MODE     Synchronization Range     0.6     1.4     MHz       SYNC Minimum Of Time     0     0.6     1.4     MHz       SYNC Minimum Of Time     0.6     1.4     MHz       SYNC Input High Voltage     1.2     V     V       SYNC		I <sub>FB</sub>			0.01	0.1	μA
Low-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       SW Peak Current Limit     High-side switch, VIN = PVIN = 3.3 V     4     5.2     6.4     A       SW Minimum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     %       SW Minimum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     %       TRK     TRK Input Voltage Range     600     mV     ns       TRK     TRK to FB Offset Voltage     TRK = 0 mV to 500 mV     -10     +10     mV       TRK to FB Offset Voltage     TRK = 0 mV to 500 mV     1.00     nA     High-side switch, VIN = 5.5 V, full frequency     mV       Oscillator Frequency     FREQ = VIN     1.0     1.2     1.4     MHz       FREQ Input High Voltage     FREQ = GND     1.0     1.2     V     V       Synchronization Range     Synchronization Range     0.6     1.4     MHz       SYNC Minimum Pulse Width     100     ns     ns     ss       SYNC Input High Voltage     1.2     V     V       SYNC Input High Voltage     1.2	SW						
Low-Side On Resistance <sup>2</sup> VIN = PVIN = 3.3 V, Isw = 500 mA     40     60     mΩ       SW Peak Current Limit     High-side switch, VIN = PVIN = 3.3 V     4     5.2     6.4     A       SW Minimum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     %       SW Minimum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     %       TRK     TRK Input Voltage Range     600     mV     ns       TRK     TRK to FB Offset Voltage     TRK = 0 mV to 500 mV     -10     +10     mV       TRK to FB Offset Voltage     TRK = 0 mV to 500 mV     1.00     nA     High-side switch, VIN = 5.5 V, full frequency     mV       Oscillator Frequency     FREQ = VIN     1.0     1.2     1.4     MHz       FREQ Input High Voltage     FREQ = GND     1.0     1.2     V     V       Synchronization Range     Synchronization Range     0.6     1.4     MHz       SYNC Minimum Pulse Width     100     ns     ns     ss       SYNC Input High Voltage     1.2     V     V       SYNC Input High Voltage     1.2	High-Side On Resistance <sup>2</sup>		$VIN = PVIN = 3.3 V$ , $I_{sw} = 500 mA$		75	110	mΩ
SW Peak Current Limit     High-side switch, VIN = PVIN = 3.3 V     4     5.2     6.4     A       SW Maximum Duty Cycle     VIN = PVIN = 5.5 V, full frequency     100     %       SW Minimum On Time <sup>3</sup> VIN = PVIN = 5.5 V, full frequency     100     %       TRK     TRK     0     600     mV       TRK Input Voltage Range     TRK = 0 mV to 500 mV     -10     +10     mV       TRK Input Bias Current     TRK = 0 mV to 500 mV     -10     1.0     n.2     1.4     MHz       FREQUENCY     FREQ = VIN     1.0     1.2     1.4     MHz       SWCMODE     FREQ = GND     500     600     700     kHz       SYNC/MODE     Synchronization Range     0.6     1.4     MHz       SYNC Minimum Pulse Width     100     ns     ns     ns       SYNC Input Ligh Voltage     1.2     V     V     V       SYNC Input Ligh Voltage     0.6     1.4     MHz       SYNC Kinimum Pulse Width     100     ns     ns       SYNC Input High Voltage     0.6 <td< td=""><td>Low-Side On Resistance<sup>2</sup></td><td></td><td></td><td></td><td>40</td><td>60</td><td>mΩ</td></td<>	Low-Side On Resistance <sup>2</sup>				40	60	mΩ
SW Maximum Duty Cycle SW Minimum On Time3VIN = PVIN = 5.5 V, full frequency100100nsTRK TRK to FB Offset Voltage TRK to FB Offset Voltage FREQUENCY Oscillator Frequency7RE 0 mV to 500 mV0600mVFREQUENCY Oscillator FrequencyFREQ = VIN FREQ = GND1.01.21.4MHzFREQ Input High Voltage FREQ Input Low VoltageFREQ = GND500600700kHzSynchronization Range SYNC Minimum Pulse Width SYNC Input Low Voltage0.61.4MHznsSYNC Input High Voltage FREQ To Dut High Voltage FREQ Input Low Voltage0.61.4MHznsSYNC/MODE Synchronization Range SYNC Input Low Voltage0.61.4MHznsSYNC Input Low Voltage0.61.2VVINTEGRATED SOFT START Soft Start TimeAll switching frequency2048Clock cyclesPower Good RangeFB rising threshold FB falling thysteresis FB falling hysteresis FB falling hysteresis2.5%Power Good Deglitch Time PGOODFrom FB to PGOOD0.11µA	SW Peak Current Limit			4	5.2	6.4	А
SW Minimum On Time3VIN = PVIN = 5.5 V, full frequency $100$ nsTRKTRK Input Voltage Range TRK to FB Offset Voltage $0$ $600$ mVTRK Input Bias CurrentTRK = 0 mV to 500 mV $-10$ $+10$ mVFREQUENCY Oscillator FrequencyFREQ = VIN $1.0$ $1.2$ $1.4$ MHzFREQ Input High Voltage FREQ Input Low VoltageFREQ = GND $500$ $600$ $700$ KHzSYNC/MODE SYNC/MODE SYNC Input Ligh Voltage $0.6$ $1.4$ MHz $100$ $1.4$ MHzSYNC/MODE SYNC Input Ligh Voltage $1.2$ $V$ $v$ $v$ $v$ $v$ SYNC Input Ligh Voltage $1.2$ $v$ $v$ $v$ $v$ $v$ SYNC Input Ligh Voltage $1.2$ $v$ $v$ $v$ $v$ $v$ SYNC Input Ligh Voltage $100$ $v$ $v$ $v$ $v$ $v$ SYNC Input Low Voltage $100$ $v$ $v$ $v$ $v$ $v$ Soft Start TimeAll switching frequency $2048$ $C$ $Clock cycles$ PGOODFB rising threshold $105$ $110$ $115$ $\%$ Power Good Deglitch TimeFB rising hysteresis $2.5$ $\%$ $\%$ PGOOD Leakage Current $v_{reccop} = 5V$ $0.1$ $1$ $\mu$	SW Maximum Duty Cycle		5			100	%
TRK     0     600     mV       TRK Input Voltage Range     TRK = 0 mV to 500 mV     -10     +10     mV       TRK Input Bias Current     100     nA     response					100		ns
TRK to FB Offset Voltage TRK Input Bias CurrentTRK = 0 mV to 500 mV $-10$ $+10$ mVTRK Input Bias Current100nAFREQUENCY Oscillator FrequencyFREQ = VIN1.01.21.4MHzFREQ Input High Voltage FREQ Input Low VoltageFREQ = GND500600700kHzSync/ronization Range SYNC Minimum Pulse Width SYNC Input Low Voltage0.61.4MHzSYNC Nonimum Off Time SYNC Input Low Voltage0.61.4MHzSYNC Input High Voltage1.2NSYNC Input Low Voltage1.2NSYNC Input High Voltage1.2NSYNC Input Low Voltage1.2NSYNC Input Low Voltage1.2NSYNC Input Low Voltage1.2NSYNC Input Low Voltage1.2NSoft Start TimeAll switching frequency2048VPGOODFB rising threshold105110115Power Good RangeFB falling hysteresis2.5%Power Good Deglitch Time PGOOD Leakage CurrentFrom FB to PGOOD1.11PGOOD Leakage CurrentVrecoon = 5 V0.111PGOCAVrecoon = 5 V0.111MA	TRK						
TRK to FB Offset Voltage TRK Input Bias CurrentTRK = 0 mV to 500 mV $-10$ $+10$ mVTRK Input Bias Current100nAFREQUENCY Oscillator FrequencyFREQ = VIN1.01.21.4MHzFREQ Input High Voltage FREQ Input Low VoltageFREQ = GND500600700kHzSync/ronization Range SYNC Minimum Pulse Width SYNC Input Low Voltage0.61.4MHzSYNC Nonimum Off Time SYNC Input Low Voltage0.61.4MHzSYNC Input High Voltage1.2NSYNC Input Low Voltage1.2NSYNC Input High Voltage1.2NSYNC Input Low Voltage1.2NSYNC Input Low Voltage1.2NSYNC Input Low Voltage1.2NSYNC Input Low Voltage1.2NSoft Start TimeAll switching frequency2048VPGOODFB rising threshold105110115Power Good RangeFB falling hysteresis2.5%Power Good Deglitch Time PGOOD Leakage CurrentFrom FB to PGOOD1.11PGOOD Leakage CurrentVrecoon = 5 V0.111PGOCAVrecoon = 5 V0.111MA	TRK Input Voltage Range			0		600	mV
TRK Input Bias CurrentImage: Image: Imag			TRK = 0 mV to 500 mV	-10		+10	mV
FREQUENCY Oscillator FrequencyFREQ = VIN FREQ = GND1.01.21.4MHzFREQ Input High Voltage FREQ Input Low VoltageFREQ = GND500600700kHzSYNC/MODE Synchronization Range SYNC Minimum Pulse Width SYNC Minimum Off Time SYNC Input High Voltage0.61.4MHzSYNC Minimum Off Time SYNC Input Low Voltage0.61.4MHzSYNC Input High Voltage100nsSYNC Input Low Voltage0.4VINTEGRATED SOFT START Soft Start TimeAll switching frequency0.4VPGOOD Power Good RangeFB rising threshold FB rising hysteresis FB falling threshold FB falling threshold FB falling hysteresis105110115%Power Good Deglitch Time PGOOD Leakage CurrentFrom FB to PGOOD Veccop = 5 V0.11µA	-					100	nA
Oscillator FrequencyFREQ = VIN FREQ = GND1.01.21.4MHzFREQ Input High Voltage500600700kHzFREQ Input Low Voltage1.2-0.4VSYNC/MODE0.6-1.4MHzSynchronization Range0.6-1.4MHzSYNC Minimum Pulse Width100nsSYNC Minimum Off Time100nsSYNC Input Low Voltage0.4VVINTEGRATED SOFT STARTVSoft Start TimeAll switching frequency105110115%PGOODFB rising threshold105110115%Power Good RangeFB rising threshold859094%Power Good Deglitch TimeFrom FB to PGOOD-16Clock cyclesPGOOD Leakage CurrentVrgood = 5 V0.11µA							
FREQ Input High Voltage FREQ Input Low VoltageFREQ = GND500600700kHzFREQ Input Low Voltage1.20.4VSYNC/MODE Synchronization Range SYNC Minimum Pulse Width SYNC Minimum Off Time SYNC Minimum Off Time SYNC Input High Voltage0.61.4MHzSYNC Minimum Off Time SYNC Input High Voltage0.61.4MHzSYNC Input High Voltage SYNC Input High Voltage100NNTEGRATED SOFT START Soft Start TimeAll switching frequency2048-Clock cyclesPGOOD Power Good RangeFB rising hysteresis FB falling threshold FB falling hysteresis105110115%Power Good Deglitch Time PGOOD Leakage CurrentVrgood = 5 V0.11µA			FREO = VIN	1.0	1.2	1.4	MHz
FREQ Input High Voltage1.2VFREQ Input Low Voltage0.4VSYNC/MODE0.61.4MHzSynchronization Range0.61.4MHzSYNC Minimum Pulse Width100100nsSYNC Minimum Off Time1001.2VNSSYNC Input High Voltage1.2VVSYNC Input Low Voltage1.2VVINTEGRATED SOFT STARTAll switching frequency2048Clock cyclesPGOODFB rising threshold105110115%PGood RangeFB rising threshold859094%FB falling hysteresis2.5%%FB falling hysteresis2.5%Power Good Deglitch TimeFrom FB to PGOOD16Clock cyclesClock cyclesPGOOD Leakage CurrentV <sub>PGOOD</sub> = 5 V0.11µA			FREO = GND	500	600	700	kHz
FREQ Input Low Voltage	FREQ Input High Voltage			1.2			v
SYNC/MODE   0.6   1.4   MHz     SYNC Minimum Pulse Width   100   ns     SYNC Minimum Off Time   100   ns     SYNC Input High Voltage   1.2   V     SYNC Input Low Voltage   0.4   V     INTEGRATED SOFT START   0.4   V     Soft Start Time   All switching frequency   2048   Clock cycles     PGOOD   FB rising threshold   105   110   115   %     PB Good Range   FB rising threshold   85   90   94   %     Power Good Deglitch Time   From FB to PGOOD   16   Clock cycles     Power Good Deglitch Time   Vregood = 5 V   0.1   1   µA						0.4	v
Synchronization Range SYNC Minimum Pulse Width SYNC Minimum Off Time SYNC Minimum Off Time SYNC Input Ligh Voltage0.61.4MHzSYNC Minimum Off Time SYNC Input Ligh Voltage100	·						
SYNC Minimum Pulse Width100nsSYNC Minimum Off Time100nsSYNC Input High Voltage1.2VVSYNC Input Low Voltage0.4VINTEGRATED SOFT STARTAll switching frequency2048Clock cyclesPGOODFB rising threshold105110115%Power Good RangeFB rising hysteresis2.5%%Power Good Deglitch TimeFrom FB to PGOOD16Clock cyclesPGOOD Leakage CurrentVPGOOD = 5 V0.11µA	Synchronization Range			0.6		1.4	MHz
SYNC Minimum Off Time SYNC Input High VoltageImage: second seco							
SYNC Input High Voltage1.2VSYNC Input Low Voltage0.4VINTEGRATED SOFT START Soft Start TimeAll switching frequency2048Clock cyclesPGOODFB rising threshold105110115%Power Good RangeFB rising hysteresis2.5%%FB falling threshold859094%Power Good Deglitch TimeFrom FB to PGOOD16Clock cyclesPOGOD Leakage CurrentVgGOOD = 5 V0.11µA	SYNC Minimum Off Time			100			
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INTEGRATED SOFT START   All switching frequency   2048   Clock cycles     PGOOD   Power Good Range   FB rising threshold   105   110   115   %     PGOOD   FB rising threshold   105   110   115   %     Power Good Range   FB rising hysteresis   2.5   %     Power Good Deglitch Time   From FB to PGOOD   16   Clock cycles     PGOOD Leakage Current   V <sub>PGOOD</sub> = 5 V   0.1   1   µA						0.4	
Soft Start TimeAll switching frequency $2048$ Clock cyclesPGOODFB rising threshold105110115%Power Good RangeFB rising threshold105110115%FB rising hysteresis $2.5$ %%FB falling threshold859094%Power Good Deglitch TimeFrom FB to PGOOD16Clock cyclesPGOOD Leakage CurrentVPGOOD = 5 V0.11 $\mu$ A							
PGOOD Power Good RangeFB rising threshold105110115%FB rising hysteresis2.5%FB falling threshold859094%FB falling hysteresis2.5%Power Good Deglitch TimeFrom FB to PGOOD16Clock cyclesPGOOD Leakage CurrentVPGOOD = 5 V0.11µA			All switching frequency		2048		Clock cycles
Power Good RangeFB rising threshold105110115%FB rising hysteresis2.5%FB falling threshold859094%FB falling hysteresis2.5%Power Good Deglitch TimeFrom FB to PGOOD16Clock cyclesPGOOD Leakage CurrentVPGOOD = 5 V0.11µA							-,
FB rising hysteresis $2.5$ %FB falling threshold859094%FB falling hysteresis $2.5$ %Power Good Deglitch TimeFrom FB to PGOOD $16$ Clock cyclesPGOOD Leakage Current $V_{PGOOD} = 5 V$ $0.1$ 1 $\mu A$			FB rising threshold	105	110	115	%
FB falling threshold859094%FB falling hysteresis $2.5$ %Power Good Deglitch TimeFrom FB to PGOOD $16$ Clock cyclesPGOOD Leakage Current $V_{PGOOD} = 5 V$ $0.1$ 1 $\mu A$	5-		-			-	
FB falling hysteresis     2.5     %       Power Good Deglitch Time     From FB to PGOOD     16     Clock cycles       PGOOD Leakage Current     V <sub>PGOOD</sub> = 5 V     0.1     1     μA				85		94	
Power Good Deglitch Time     From FB to PGOOD     16     Clock cycles       PGOOD Leakage Current     V <sub>PGOOD</sub> = 5 V     0.1     1     μA			-				
PGOOD Leakage Current $V_{PGOOD} = 5 V$ 0.11 $\mu A$	Power Good Deglitch Time						
						1	-
	<u> </u>						

Parameter	Symbol	Test Conditions/Comments	Min	Тур	Max	Unit
EN						
EN Input Rising Threshold		VIN = 2.3 V to 5.5 V	1.12	1.2	1.28	v
EN Input Hysteresis		VIN = 2.3 V to 5.5 V		100		mV
EN Pull-Down Resistor				1		MΩ
THERMAL						
Thermal Shutdown Threshold				140		°C
Thermal Shutdown Hysteresis				15		°C

<sup>1</sup> Specified by the circuit in Figure 45.
<sup>2</sup> Pin-to-pin measurements.
<sup>3</sup> Guaranteed by design.

## **ABSOLUTE MAXIMUM RATINGS**

#### Table 2.

1.0010 21	
Parameter	Rating
VIN, PVIN	–0.3 V to +6 V
SW	–0.3 V to +6 V
FB, SYNC/MODE, EN, TRK, FREQ, PGOOD	–0.3 V to +6 V
PGND to GND	–0.3 V to +0.3 V
Operating Junction Temperature Range	-40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

 $\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

#### Table 3. Thermal Resistance

Package Type	θја	Unit
16-Lead LFCSP	38.3	°C/W

#### **Boundary Conditions**

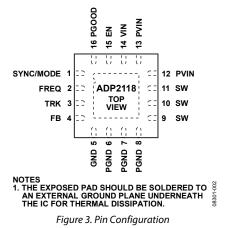
 $\theta_{JA}$  is measured using natural convection on a JEDEC 4-layer board, and the exposed pad is soldered to the printed circuit board with thermal vias.

#### **ESD CAUTION**



**ESD** (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



#### Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SYNC/MODE	Synchronization Input (SYNC). Connect this pin to an external clock between 600 kHz and 1.4 MHz to synchronize the switching frequency to the external clock (see the Oscillator and Synchronization section for details).
		CCM/PFM Selection (MODE). When this pin is connected to VIN, PFM mode is disabled and the ADP2118 only works in continuous conduction mode (CCM). When this pin is connected to ground, PFM mode is enabled and becomes active at light loads.
2	FREQ	Frequency Selection. Connect to GND to select 600 kHz and VIN for 1.2 MHz.
3	TRK	Tracking Input. To track a master voltage, drive TRK from a voltage divider from the master voltage. If the tracking function is not used, connect TRK to VIN.
4	FB	Feedback Voltage Sense Input. Connect to a resistor divider from V <sub>OUT</sub> . For the fixed output version, connect to V <sub>OUT</sub> directly.
5	GND	Analog Ground. Connect to the ground plane.
6, 7, 8	PGND	Power Ground. Connect to the ground plane and to the output return side of the output capacitor.
9, 10, 11	SW	Switch Node Output. Connect to the output inductor.
12, 13	PVIN	Power Input Pin. Connect this pin to the input power source. Connect a bypass capacitor between this pin and PGND.
14	VIN	Bias Voltage Input Pin. Connect a bypass capacitor between this pin and GND and a small (10 $\Omega$ ) resistor between this pin and PVIN.
15	EN	Precision Enable Pin. The external resistor divider can be used to set the turn-on threshold. To enable the part automatically, connect the EN pin to VIN. This pin has a 1 M $\Omega$ pull-down resistor to GND.
16	PGOOD	Power-Good Output (Open Drain). Connect to a resistor to any pull-up voltage <5.5 V.
17 (EPAD)	Exposed Pad	The exposed pad should be soldered to an external ground plane underneath the IC for thermal dissipation.

## **TYPICAL PERFORMANCE CHARACTERISTICS**

 $T_A = 25^{\circ}$ C,  $V_{IN} = 5$  V,  $V_{OUT} = 1.2$  V,  $L = 1 \mu$ H,  $C_{IN} = 100 \mu$ F,  $C_{OUT} = 100 \mu$ F, unless otherwise noted.

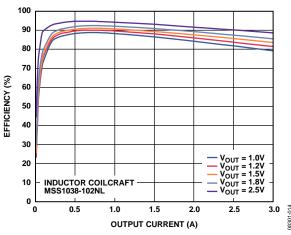


Figure 4. Efficiency (1.2 MHz, VIN = 3.3 V, FPWM) vs. Output Current

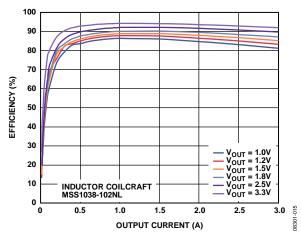


Figure 5. Efficiency (1.2 MHz, VIN = 5 V, FPWM) vs. Output Current

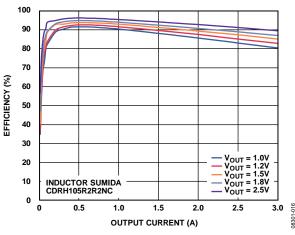


Figure 6. Efficiency (600 kHz, V<sub>IN</sub> = 3.3 V, FPWM) vs. Output Current

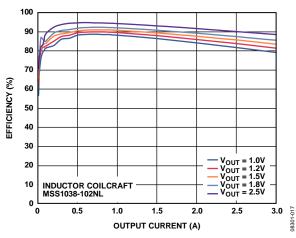


Figure 7. Efficiency (1.2 MHz, V<sub>IN</sub> = 3.3 V, PFM) vs. Output Current

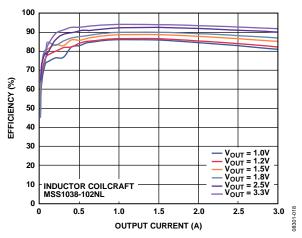


Figure 8. Efficiency (1.2 MHz, V<sub>IN</sub> = 5 V, PFM) vs. Output Current

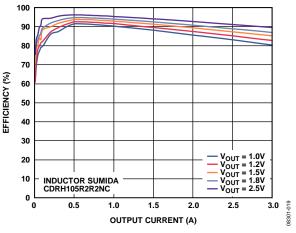


Figure 9. Efficiency (600 kHz, VIN = 3.3 V, PFM) vs. Output Current

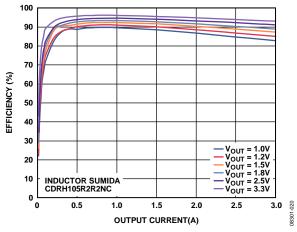


Figure 10. Efficiency (600 kHz, V<sub>IN</sub> = 5 V, FPWM) vs. Output Current

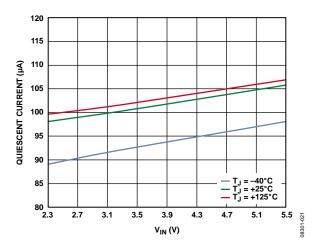


Figure 11. Quiescent Current vs. V<sub>IN</sub> (No Switching)

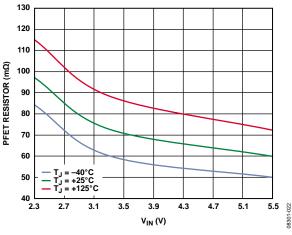


Figure 12. PFET Resistor vs. V<sub>IN</sub> (Pin-to-Pin Measurements)

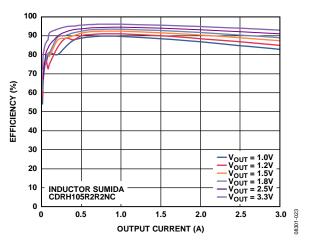


Figure 13. Efficiency (600 kHz, V<sub>IN</sub> = 5 V, PFM) vs. Output Current

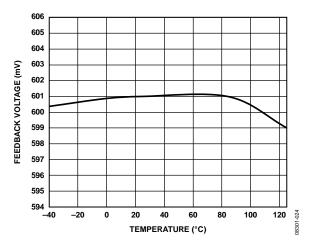


Figure 14. Feedback Voltage vs. Temperature ( $V_{IN} = 3.3 V$ )

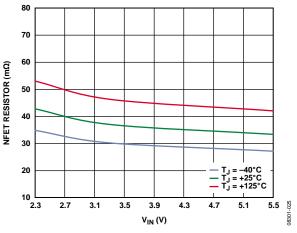
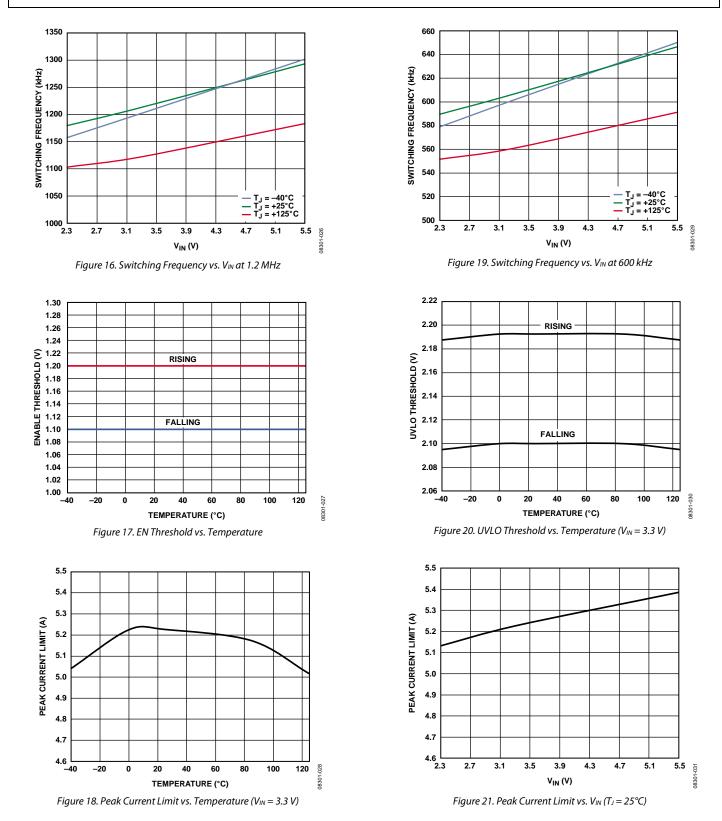


Figure 15. NFET Resistor vs. V<sub>IN</sub> (Pin-to-Pin Measurements)

## Data Sheet

ADP2118



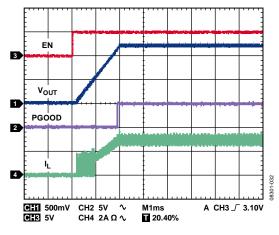


Figure 22. Soft Start with Full Load (1.2 MHz,  $V_{IN} = 5 V$ )

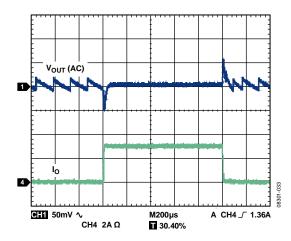


Figure 23. Load Transient (1.2 MHz, PFM,  $V_{IN} = 5 V$ )

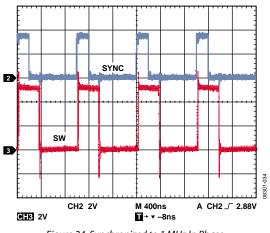


Figure 24. Synchronized to 1 MHz In Phase

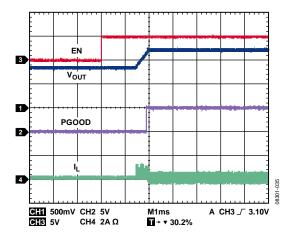
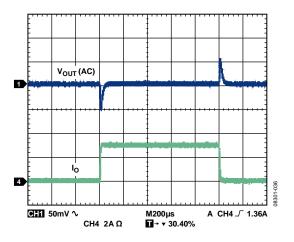
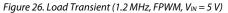


Figure 25. Soft Start with Precharge (1.2 MHz,  $V_{IN} = 5 V$ )





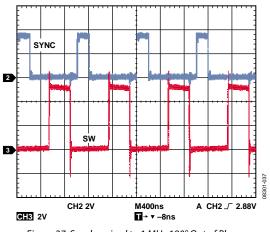


Figure 27. Synchronized to 1 MHz 180° Out of Phase

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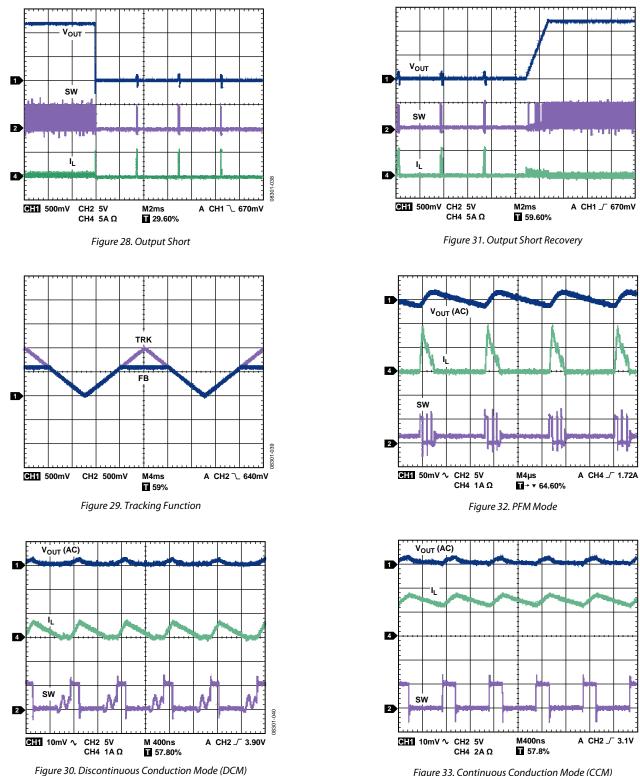
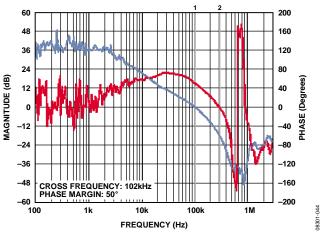
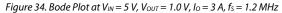
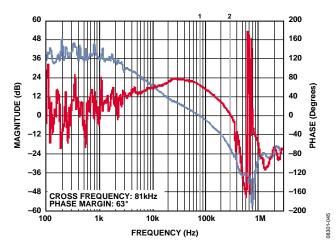
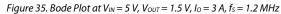


Figure 33. Continuous Conduction Mode (CCM)









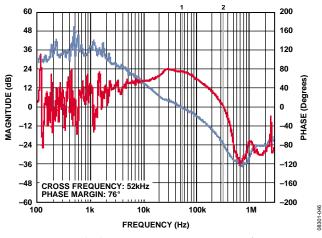
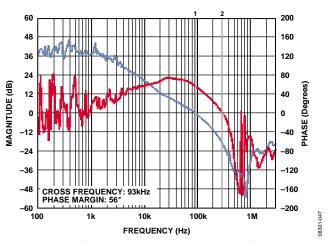
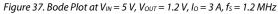
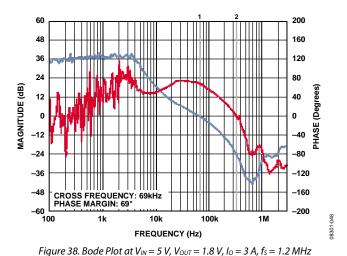
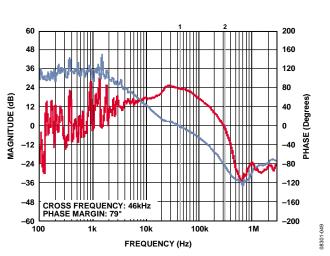


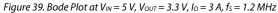
Figure 36. Bode Plot at  $V_{IN} = 5 V$ ,  $V_{OUT} = 2.5 V$ ,  $I_O = 3 A$ ,  $f_S = 1.2 MHz$ 











# FUNCTIONAL BLOCK DIAGRAM

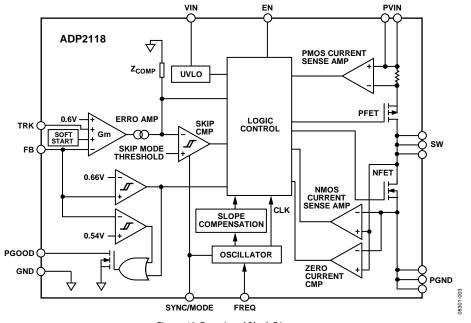


Figure 40. Functional Block Diagram

## THEORY OF OPERATION

The ADP2118 is a step-down, dc-to-dc regulator that uses fixed frequency, peak current-mode architecture with an integrated high-side switch and low-side synchronous rectifier. The high switching frequency and tiny 16-lead, 4 mm × 4 mm LFCSP package allow for a small step-down dc-to-dc regulator solution. The integrated high-side switch (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET) yield high efficiency at medium-to-full loads, and light load efficiency is improved by PFM mode.

The ADP2118 operates with an input voltage from 2.3 V to 5.5 V and regulates the output voltage down to 0.6 V. The ADP2118 is also available with preset output voltage options of 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, and 1.0 V.

## **CONTROL SCHEME**

The ADP2118 uses the fixed frequency, peak current mode PWM control architecture and operates in PWM mode for medium-to-full loads but shifts to PFM mode (if enabled) at light loads to maintain high efficiency. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted to regulate the output voltage. When operating in PFM mode at light loads, the switching frequency is adjusted to regulate the output voltage.

The ADP2118 operates in PWM mode when the load current is greater than the pulse-skipping threshold current. At load currents below this value, the regulator smoothly transitions to the PFM mode of operation.

## **PWM MODE OPERATION**

In PWM mode, the ADP2118 operates at a fixed frequency set by the FREQ pin. At the start of each oscillator cycle, the Pchannel MOSFET switch is turned on, putting a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current level, turns off the P-channel MOSFET switch, and turns on the N-channel MOSFET synchronous rectifier. This puts a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle or until the inductor current reaches zero, which causes the zerocrossing comparator to turn off the N-channel MOSFET as well.

The peak inductor current level is set by  $V_{\text{COMP}}$ . The  $V_{\text{COMP}}$  is the output of a transconductance error amplifier that compares the feedback voltage with an internal 0.6 V reference.

## **PFM MODE OPERATION**

When PFM mode is enabled, the ADP2118 smoothly transitions to the variable frequency PFM mode of operation when the load current decreases below the pulse-skipping threshold current, switching only as necessary to maintain the output voltage within regulation. When the output voltage drops below regulation, the ADP2118 enters PWM mode for a few oscillator cycles to increase the output voltage back to regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies all the load current. Because the output voltage dips and recovers occasionally, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

## **SLOPE COMPENSATION**

Slope compensation stabilizes the internal current control loop of the ADP2118 when operating close to and beyond 50% duty cycle to prevent subharmonic oscillations. It is implemented by summing an artificial voltage ramp to the current sense signal during the on-time of the P-channel MOSFET switch. This voltage ramp depends on the output voltage. When operating at high output voltages, there is more slope compensation. The slope compensation ramp value determines the minimum inductor that can be used to prevent subharmonic oscillations.

## **ENABLE/SHUTDOWN**

The EN pin is a precision analog input that enables the device when the voltage exceeds 1.2 V (typical) and has 100 mV hysteresis. When the enable voltage falls below 1.1 V (typical) the part turns off. To force the ADP2118 to automatically start when input power is applied, connect EN to VIN.

When the ADP2118 is shut down, the soft start capacitor is discharged. This causes a new soft start cycle to begin when the part is reenabled.

An internal pull-down resistor (1 M $\Omega$ ) prevents an accidental enable if EN is left floating.

## **INTEGRATED SOFT START**

The ADP2118 has integrated soft start circuitry to limit the output voltage rise time and reduce inrush current at startup. The soft start time is fixed at 2048 clock cycles.

If the output voltage is precharged prior to turn-on, the ADP2118 prevents a reverse inductor current (that would discharge the output capacity) until the soft start voltage exceeds the voltage on the FB pin.

#### TRACKING

The ADP2118 has a tracking input, TRK, that allows the output voltage to track another voltage (master voltage). It is especially useful in core and I/O voltage tracking for FPGAs, DSPs, and ASICs.

The internal error amplifier includes three positive inputs: the internal reference voltage, the soft start voltage, and the TRK voltage. The error amplifier regulates the FB voltage to the lowest of the three voltages. To track a master voltage, tie the TRK pin to a resistor divider from the master voltage.

If the TRK function is not used, connect the TRK pin to VIN.

### **OSCILLATOR AND SYNCHRONIZATION**

The internal oscillator of ADP2118 can be set to 600 kHz or 1.2 MHz. Drive the FREQ pin low for 600 kHz; drive FREQ pin high for 1.2 MHz.

To synchronize the ADP2118, drive an external clock at the SYNC/MODE pin. The frequency of the external clock can be in the range of 600 kHz to 1.4 MHz. During synchronization, the regulator operates in CCM mode only.

If the FREQ pin is low, the switching frequency is in phase with the external clock; if the FREQ pin is high, the switching frequency is 180° out of phase with the external clock.

# CURRENT LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2118 has a peak current limit protection circuit to prevent current runaway. The peak current is limited at 5.2 A. When the inductor peak current reaches the current limit value, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle while the overcurrent counter increments. If the overcurrent counter count exceeds 10, the part enters hiccup mode. The high-side FET and low-side FET are both turned off. The part remains in this mode for 4096 clock cycles and then attempts to restart from soft start. If the current limit fault has cleared, the part resumes normal operation. Otherwise, it reenters hiccup mode again after counting 10 current-limit violations.

#### **OVERVOLTAGE PROTECTION (OVP)**

The output voltage is continuously monitored by a comparator through the FB pin, which is at 0.6 V (typical) under normal operation. This comparator is set to activate when the FB voltage exceeds 0.66 V (typical), thus indicating an output overvoltage condition. If the voltage remains above this threshold for 16 clock cycles, the high-side MOSFET turns off and the low-side MOSFET turns on until the current through it reaches the limit (-0.9 A for forced continuous mode and 0 A for PFM mode).

Thereafter, both the MOSFETs are held in the off state until FB falls below 0.54 V (typical), and then the part restarts. The behavior of PGOOD under this condition is described in the Power Good section.

### **UNDERVOLTAGE LOCKOUT (UVLO)**

Undervoltage lockout circuitry is integrated on the ADP2118. If the input voltage drops below 2.1 V, the ADP2118 shuts down, and both the power switch and the synchronous rectifier turn off. When the voltage rises again above 2.2 V, the soft start period is initiated, and the part is enabled.

#### THERMAL SHUTDOWN

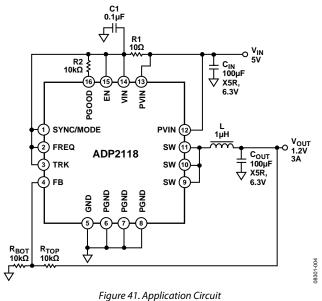
In the event that the ADP2118 junction temperature rises above 140°C, the thermal shutdown circuit turns off the regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 15°C hysteresis is included so that when thermal shutdown occurs, the ADP2118 does not return to operation until the on-chip temperature drops below 125°C. When coming out of thermal shutdown, soft start is initiated.

#### **POWER GOOD**

PGOOD is an active high, open-drain output and requires a resistor to pull it up to a voltage. A high indicates that the voltage on the FB pin (and therefore the output voltage) is within 10% of the desired value. A low on this pin indicates that the voltage on the FB pin is not within 10% of the desired value. There is a 16 cycle waiting period after FB is detected as being out of bounds. If FB returns to within the  $\pm 10\%$  range, it is ignored by PGOOD circuitry.

## **APPLICATIONS INFORMATION**

This section describes the external components selection for the ADP2118. The typical application circuit is shown in Figure 41.



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## ADISIMPOWER™ DESIGN TOOL

The ADP2118 is supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

#### **OUTPUT VOLTAGE SELECTION**

The output voltage of the adjustable version of the ADP2118 can be set by an external resistive voltage divider by using the following equation to set the voltage:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

To limit output voltage accuracy degradation due to FB bias current (0.1  $\mu$ A maximum) to less than 0.5% (maximum), ensure that R<sub>BOT</sub> is less than 30 k $\Omega$ .

#### INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and ripple current. Using a small inductor leads to larger inductor current ripple and provides fast transient response but degrades efficiency, whereas a large inductor value leads to small current ripple and good efficiency but slow transient response. As a guideline, the inductor current ripple,  $\Delta I_{L}$ , is typically set to 1/3 of the maximum load current trade-off between the transient response and efficiency. The inductor can be calculated using the following equation:

$$L = \frac{\left(V_{IN} - V_{OUT}\right) \times D}{\Delta I_L \times f_S}$$

where:

 $\label{eq:VIN} \begin{array}{l} V_{\rm IN} \mbox{ is the input voltage.} \\ V_{\rm OUT} \mbox{ is the output voltage.} \\ \Delta I_L \mbox{ is the inductor current ripple.} \\ D \mbox{ is the duty cycle.} \end{array}$ 

$$D = \frac{V_{OUT}}{V_{IN}}$$

The ADP2118 uses slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

The negative current limit (–0.9 A) also limits the minimum inductor value. The inductor current ripple ( $\Delta I_L$ ) calculated by the selected inductor should not exceed 1.8 A.

The peak inductor current should be kept below the peak current limit threshold value and can be calculated as

$$I_{PEAK} = I_O + \frac{\Delta I_L}{2}$$

Ensure that the rms current of the selected inductor is greater than the maximum load current and that its saturation current is greater than the peak current limit of the regulator.

#### **OUTPUT CAPACITOR SELECTION**

The output voltage ripple, load step transient, and loop stability determine the output capacitor selection.

The output ripple is determined by the ESR and the capacitance.

$$\Delta V_{OUT} = \Delta I_L \times \left( ESR + \frac{1}{8 \times C_{OUT} \times f_s} \right)$$

The load transient response depends on the inductor, output capacitor, and the control loop.

The ADP2118 has integrated loop compensation for simple power design. Table 5 and Table 6 show the typical recommended inductors and capacitors for the ADP2118. X5R or X7R ceramic capacitors are highly recommended.

#### Table 5. Recommended L and $C_{OUT}$ Value at $f_s = 1.2$ MHz

V <sub>IN</sub> (V)	V <sub>OUT</sub> (V)	<b>L (μH</b> )	<b>C</b> <sub>OUT</sub> (μ <b>F</b> )
3.3	1.0	1	100 + 47
3.3	1.2	1	100
3.3	1.5	1	100
3.3	1.8	1	100
3.3	2.5	1	100
5	1.0	1	100 + 47
5	1.2	1	100
5	1.5	1	100
5	1.8	1	100
5	2.5	1	100
5	3.3	1	100

#### Table 6. Recommended L and $C_{OUT}$ Value at $f_s = 600 \text{ kHz}$

$V_{IN}(V)$	Vout (V)	<b>L (μΗ</b> )	C <sub>ουτ</sub> (μF)	
3.3	1.0	1.5	100 + 47	
3.3	1.2	1.5	100	
3.3	1.5	1.5	100	
3.3	1.8	1.5	100	
3.3	2.5	1.5	100	
5	1.0	1.5	100 + 47	
5	1.2	1.5	100	
5	1.5	2.2	100	
5	1.8	2.2	100	
5	2.5	2.2	100	
5	3.3	2.2	100	

Higher or lower inductors and output capacitors can be used in the regulator, but the system stability and load transient performance need to be checked.

The minimum output capacitor can be 47  $\mu$ F. If f<sub>s</sub> = 1.2 MHz, the inductor range is 0.8  $\mu$ H to 3.3  $\mu$ H. If f<sub>s</sub> = 600 kHz, the inductor range is 1.5  $\mu$ H to 3.3  $\mu$ H.

#### Table 7. Recommended Inductors

Manufacturer	Part Number
Coilcraft	MSS1038, MSS1048, MSS1260
Sumida	CDRH103R, CDRH104R, CDRH105R

#### Table 8. Recommended Capacitors

Manufacturer	Part Number	Description	
Murata	GRM32ER60J107ME20	100 μF, 6.3 V, X5R, 1210	
Murata	GRM32ER60J476ME20	47 μF, 6.3 V, X5R, 1210	
TDK	C3225X5R0J107M	100 μF, 6.3 V, X5R, 1210	
TDK	C3225X5R0J476M	47 μF, 6.3 V, X5R, 1210	

### INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on PVIN. Place the input capacitor as close as possible to the PVIN pin. A 22  $\mu$ F or 47  $\mu$ F ceramic capacitor is recommended. The rms current rating of the input capacitor should be larger than the following equation:

$$I_{RMS} = I_O \times \sqrt{D \times (1 - D)}$$

### **VOLTAGE TRACKING**

The ADP2118 includes a tracking feature that allows the ADP2118 output (slave voltage) to be configured to track an external voltage (master voltage), as shown in Figure 42.

A common application is coincident tracking, shown in Figure 43. Coincident tracking limits the slave output voltage to be the same as the master voltage until it reaches regulation. Connect the TRK pin to a resistor divider from the master voltage. For coincident tracking, set  $R_{TRKT} = R_{TOP}$  and  $R_{TRKB} = R_{BOT}$ .

Ratiometric tracking is shown in Figure 44. The slave output is limited to a fraction of the master voltage. In this application, the slave and master voltages reach the final value at the same time. The ratio of the slave output voltage to the master voltage is a function of the two dividers.

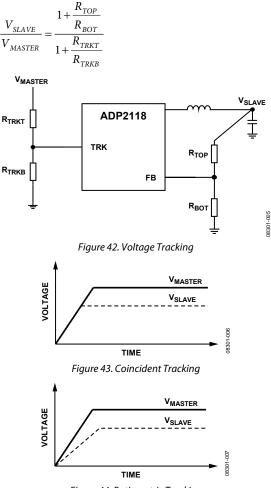
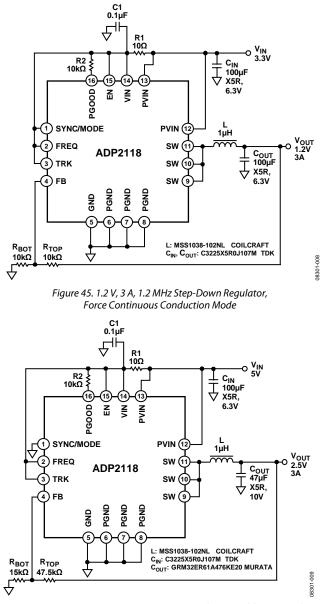
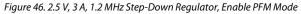
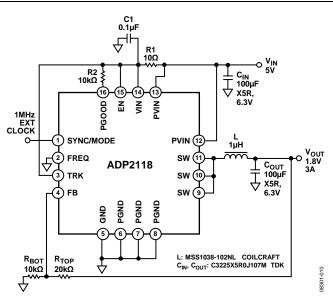


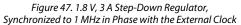
Figure 44. Ratiometric Tracking

# **TYPICAL APPLICATION CIRCUITS**









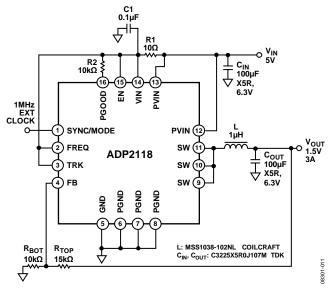


Figure 48. 1.5 V, 3 A Step-Down Regulator, Synchronized to 1 MHz, 180° Out of Phase with the External Clock

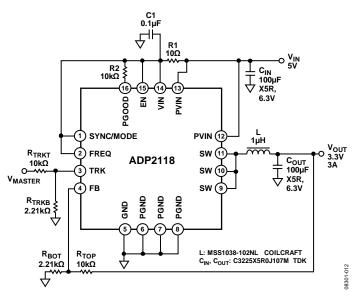


Figure 49. 3.3 V, 3 A, 1.2 MHz Step-Down Regulator, Tracking Mode

# **OUTLINE DIMENSIONS**

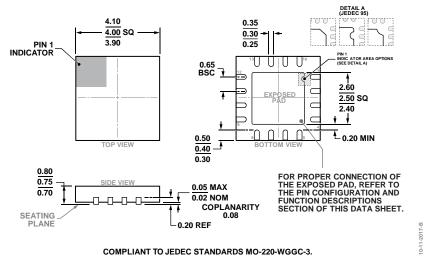


Figure 50. 16-Lead Lead Frame Chip Scale Package [LFCSP] 4 mm × 4 mm Body and 0.75 mm Package Height (CP-16-26) Dimensions shown in millimeters

#### **ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Output Voltage	Package Description	Package Option
ADP2118ACPZ-R7	-40°C to +125°C	Adjustable	16-Lead LFCSP	CP-16-26
ADP2118ACPZ-1.2-R7	-40°C to +125°C	1.2 V	16-Lead LFCSP	CP-16-26
ADP2118ACPZ-3.3-R7	-40°C to +125°C	3.3 V	16-Lead LFCSP	CP-16-26
ADP2118-EVALZ			Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

# NOTES

# NOTES

## NOTES



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