International IOR Rectifier

AUTOMOTIVE MOSFET

# IRF2204S
IRF2204L

HEXFET® Power MOSFET
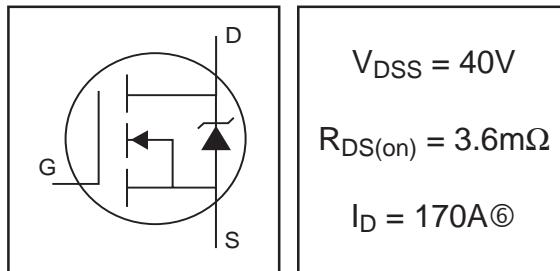
Typical Applications
- Electric Power Steering
- 14 Volts Automotive Electrical Systems

Features
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

$V_{DSS} = 40V$

$R_{DS(on)} = 3.6m\Omega$

$I_D = 170A$⑥

Description
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features to this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.


| D^2Pak | TO-262 |
| IRF2204S | IRF2204L |
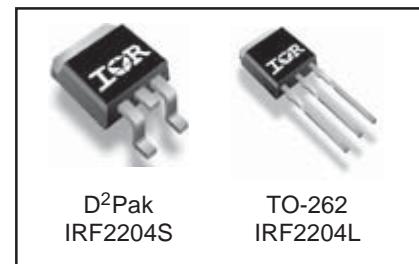
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	170⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	120⑥	
I_{DM}	Pulsed Drain Current ①	850	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	460	mJ
I_{AR}	Avalanche Current①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient	——	40	

07/01/02

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.041	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	3.0	3.6	mΩ	V_{GS} = 10V, I_D = 130A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = 10V, I_D = 250μA
g_{fs}	Forward Transconductance	120	——	——	S	V_{DS} = 10V, I_D = 130A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V
Q_g	Total Gate Charge	——	130	200		I_D = 130A
Q_{gs}	Gate-to-Source Charge	——	35	52	nC	V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	39	59		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	——	15	——		V_{DD} = 20V
t_r	Rise Time	——	140	——	ns	I_D = 130A
$t_{d(off)}$	Turn-Off Delay Time	——	62	——		R_G = 2.5Ω
t_f	Fall Time	——	110	——		V_{GS} = 10V ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	5890	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	1570	——	pF	V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	130	——		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	——	8000	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	1370	——		V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	——	2380	——		V_{GS} = 0V, V_{DS} = 0V to 32V
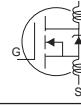
Source-Drain Ratings and Characteristics

|	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	170⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	850		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 130A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	68	100	ns	T_J = 25°C, I_F = 130A
Q_{rr}	Reverse RecoveryCharge	——	120	180	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time					Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)
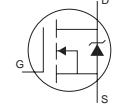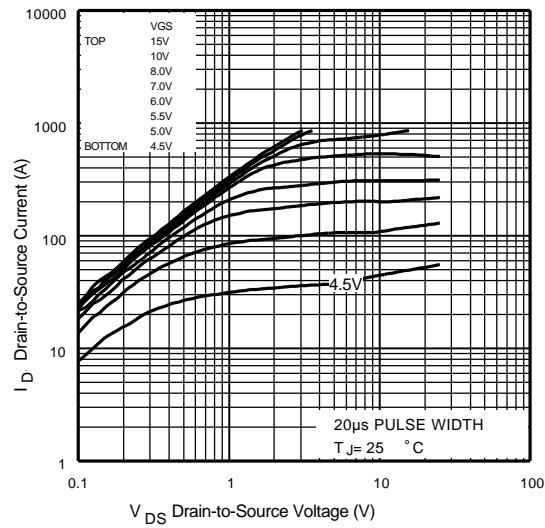
**Fig 1.** Typical Output Characteristics
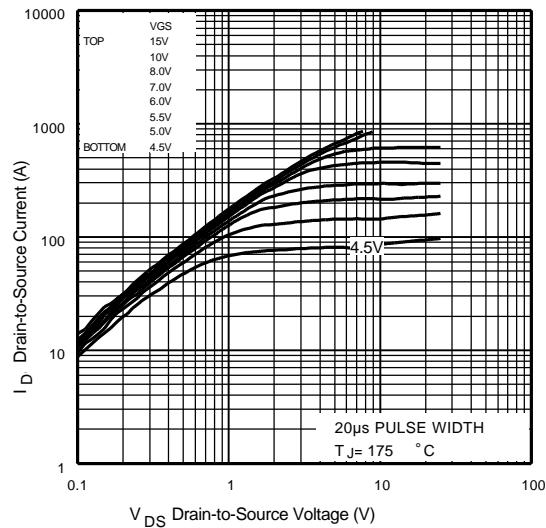
**Fig 2.** Typical Output Characteristics
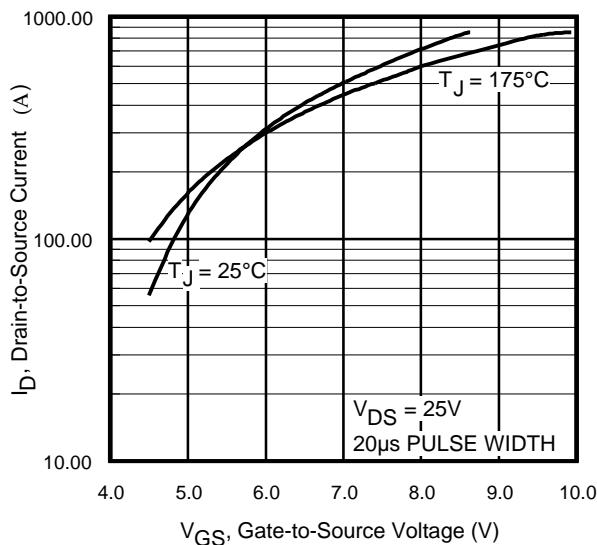
**Fig 3.** Typical Transfer Characteristics
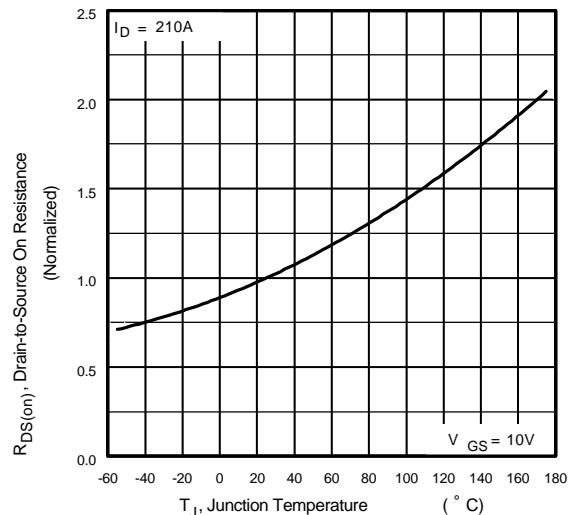
Fig 4. Normalized On-Resistance
Vs. Temperature

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Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage
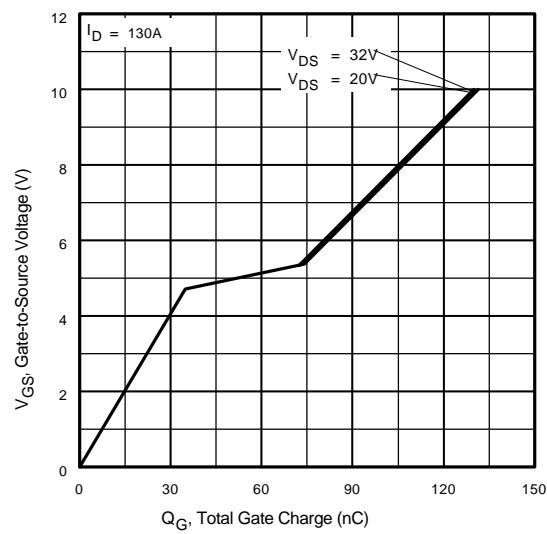

Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage
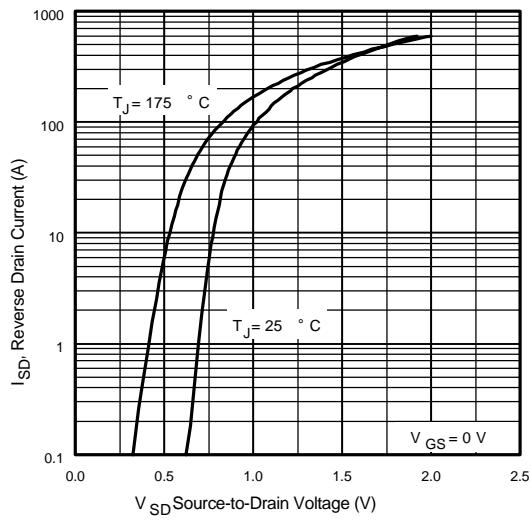

Fig 7. Typical Source-Drain Diode
Forward Voltage
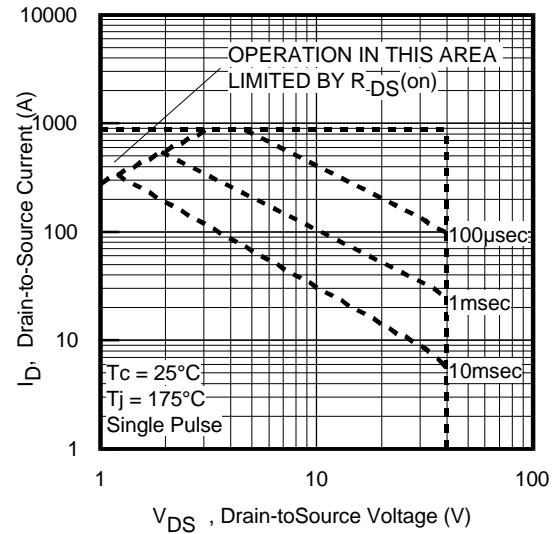
**Fig 8.** Maximum Safe Operating Area

4
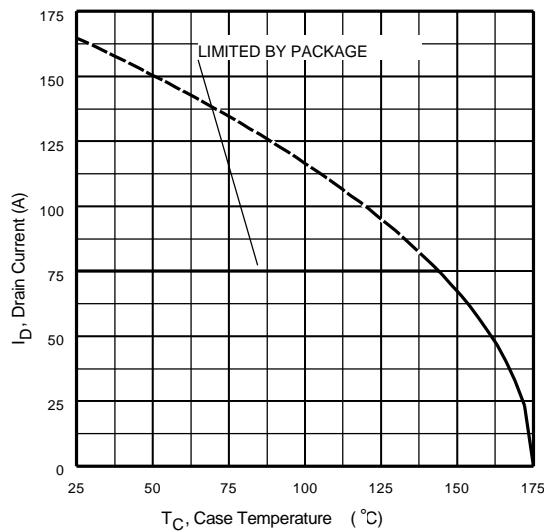
Fig 9. Maximum Drain Current Vs. Case Temperature
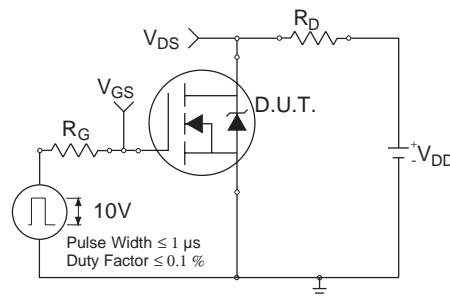

Fig 10a. Switching Time Test Circuit
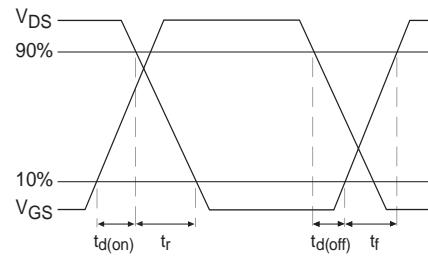
Fig 10b. Switching Time Waveforms
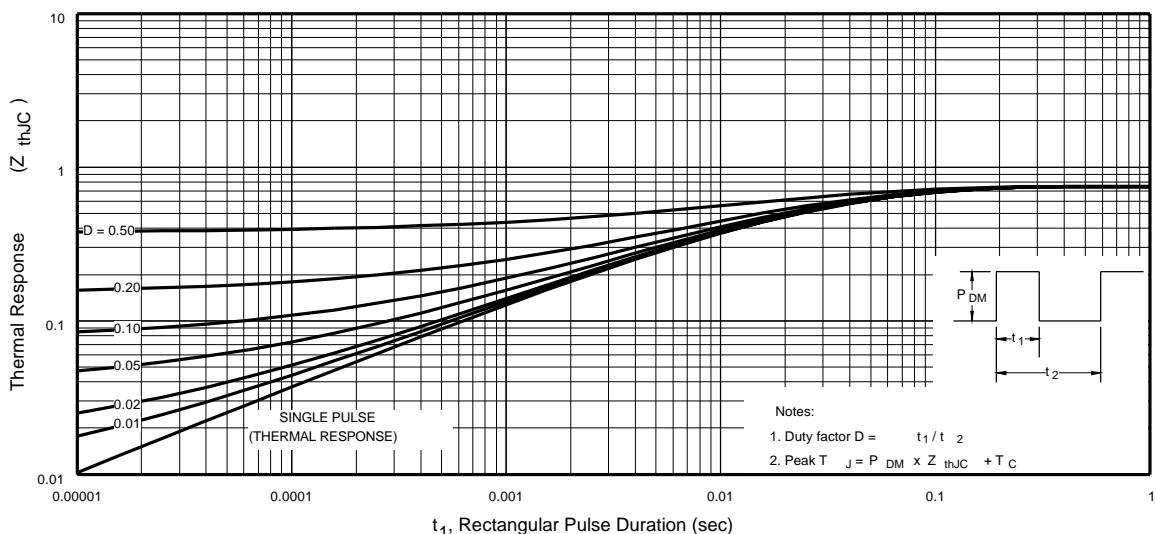
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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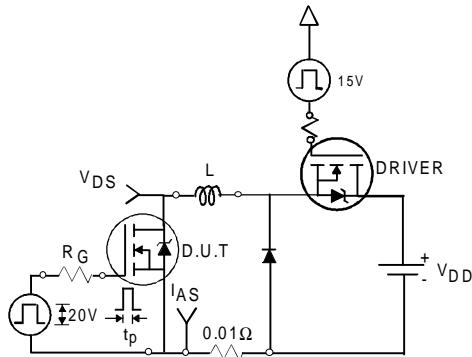
**Fig 12a.** Unclamped Inductive Test Circuit
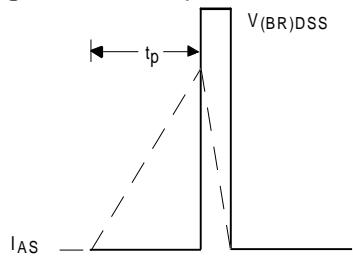
Fig 12b. Unclamped Inductive Waveforms
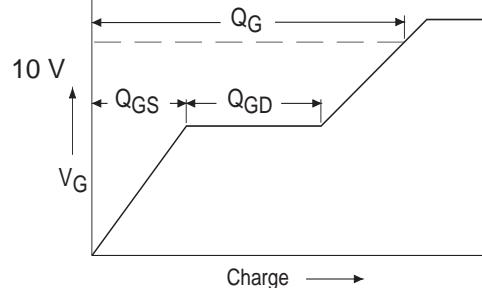

**Fig 13a.** Basic Gate Charge Waveform
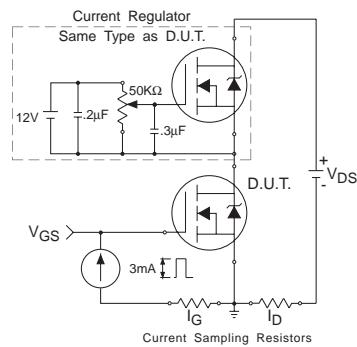
Fig 13b. Gate Charge Test Circuit

6
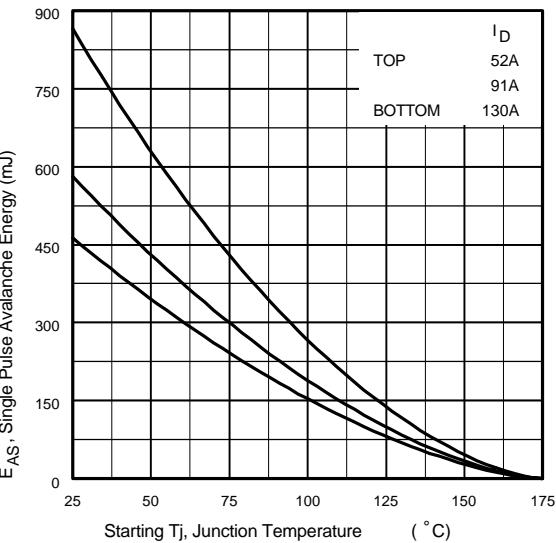
Fig 12c. Maximum Avalanche Energy
Vs. Drain Current
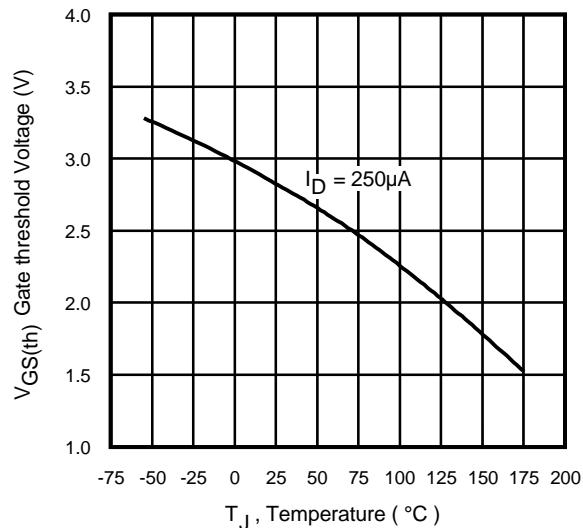
Fig 14. Threshold Voltage Vs. Temperature
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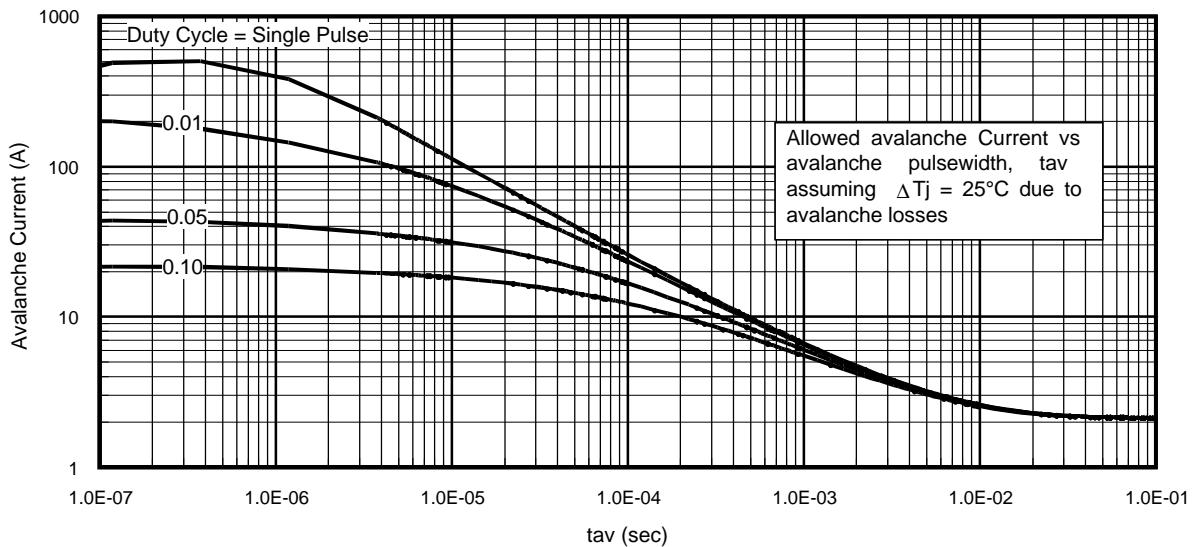
Fig 15. Typical Avalanche Current Vs.Pulsewidth
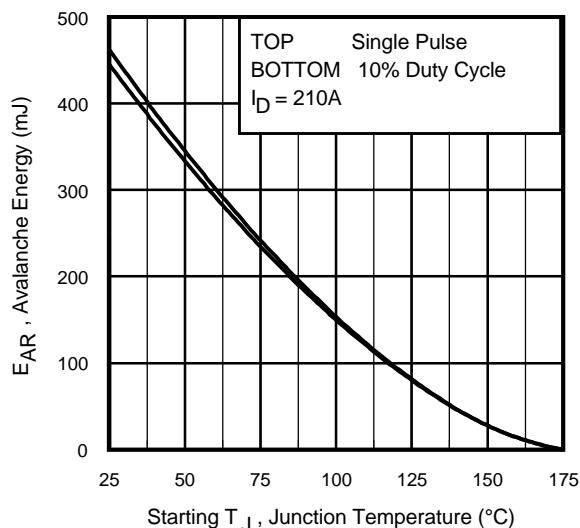
Fig 16. Maximum Avalanche Energy
Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a
   temperature far in excess of T_{jmax}. This is validated for
   every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is
   not exceeded.
3. Equation below based on circuit and waveforms shown in
   Figures 12a, 12b.
4. $P_{D (ave)}$ = Average power dissipation per single
   avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for
   voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed
   T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D (ave)} = 1/2 \ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T/ \ Z_{thJC}$$
$$I_{av} = 2\Delta T/ \ [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$

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Peak Diode Recovery dv/dt Test Circuit

D.U.T*

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

③

②

①

R_G

V_{GS}

- dv/dt controlled by R_G
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

④

V_{DD}
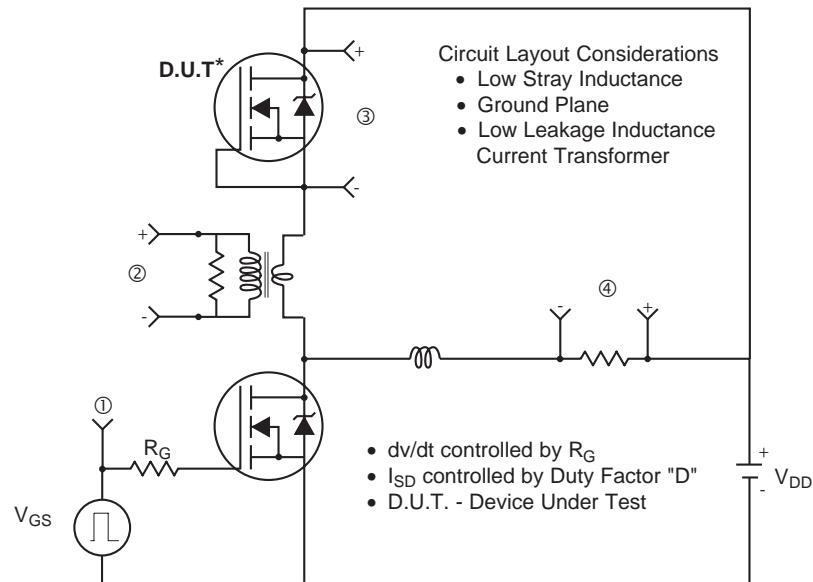
* Reverse Polarity of D.U.T for P-Channel

① Driver Gate Drive

P.W.

Period

$D = \dfrac{P.W.}{Period}$

$\left[V_{GS}=10V\right]$ ***

② D.U.T. I_{SD} Waveform

Reverse
Recovery
Current

Body Diode Forward
Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery
dv/dt

$\left[V_{DD}\right]$

Re-Applied
Voltage

Body Diode   Forward Drop

④ Inductor Curent

Ripple $\leq$ 5%

$\left[I_{SD}\right]$
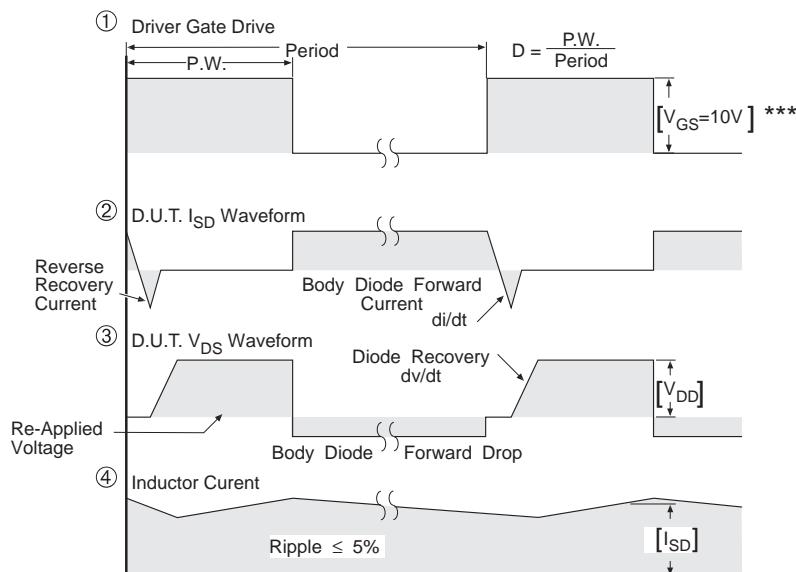
*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

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D²Pak Package Outline
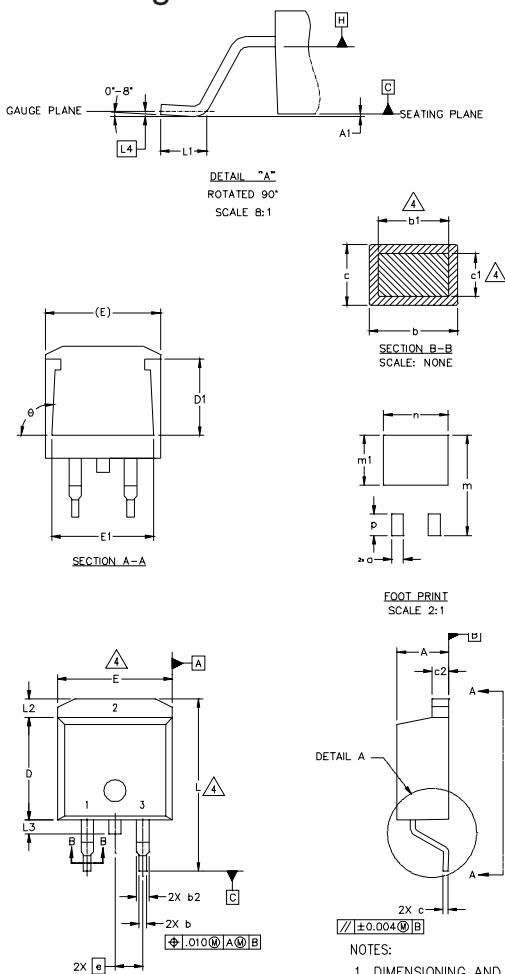
DETAIL "A"
ROTATED 90°
SCALE 8:1

SECTION B-B
SCALE: NONE

SECTION A-A

FOOT PRINT
SCALE 2:1

DETAIL A

S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.74	.015	.029	
c1	0.43	0.63	.017	.025	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.— GATE	1.— GATE	1.— ANODE *
2.— DRAIN	2.— COLLECTOR	2.— CATHODE
3.— SOURCE	3.— EMITTER	3.— ANODE

* PART DEPENDENT.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994

2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"]
   PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.

5. CONTROLLING DIMENSION: INCH.

D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

PART NUMBER

INTERNATIONAL
RECTIFIER
LOGO

F530S
I◆R 002L
80   24

ASSEMBLY
LOT CODE

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L
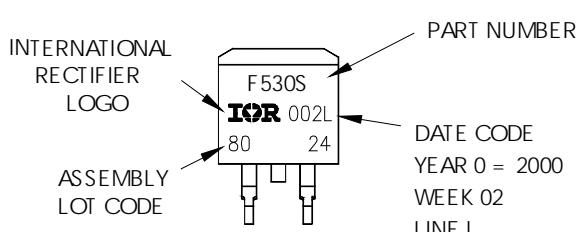
IRF2204S/IRF2204L

TO-262 Package Outline
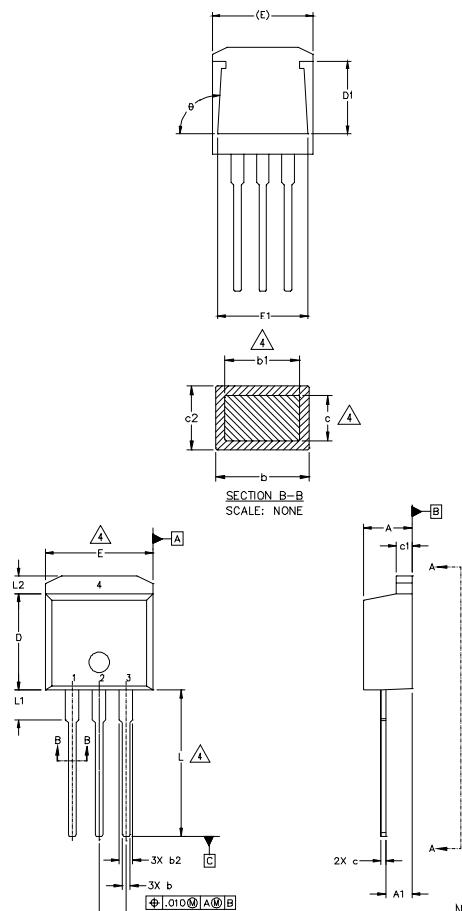
| S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.

5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

ASSEMBLY LOT CODE

IRL3103L
IΦR 719C
17   89
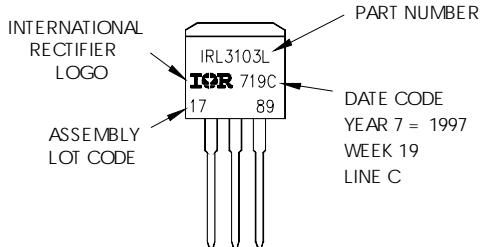
D²Pak Tape & Reel Information

TRR

FEED DIRECTION →

TRL

FEED DIRECTION →

1.60 (.063)
1.50 (.059)

4.10 (.161)
3.90 (.153)

1.85 (.073)
1.65 (.065)

Ø 1.60 (.063)
1.50 (.059)

11.60 (.457)
11.40 (.449)

Ø 1.75 (.069)
1.25 (.049)

10.90 (.429)
10.70 (.421)

16.10 (.634)
15.90 (.626)

0.368 (.0145)
0.342 (.0135)

15.42 (.609)
15.22 (.601)

24.30 (.957)
23.90 (.941)

4.72 (.136)
4.52 (.178)

13.50 (.532)
Ø 12.80 (.504)

Ø 330.00
(14.173)
MAX.

27.40 (1.079)
23.90 (.941)

④

Ø 60.00 (2.362)
MIN.

30.40 (1.197)
MAX.

26.40 (1.039)
24.40 (.961)

③

④

NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
③ DIMENSION MEASURED @ HUB.
④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Notes:

① Repetitive rating; pulse width limited by
   max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.06mH
   R_G = 25Ω, I_{AS} = 130A. (See Figure 12).

③ $I_{SD} \leq$ 130A, di/dt $\leq$ 170A/μs, $V_{DD} \leq V_{(BR)DSS}$,
   $T_J \leq$ 175°C.

④ Pulse width $\leq$ 400μs; duty cycle $\leq$ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time
   as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable
   junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive
   avalanche performance.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International **I☢R** Rectifier

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/

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