



PMZB320UPE

30 V, P-channel Trench MOSFET

24 March 2015

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Low threshold voltage
- Very fast switching
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- Ultra thin package profile of 0.37 mm

3. Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_J = 25\text{ }^\circ\text{C}$	-	-	-30	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$	[1]	-	-1	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -1\text{ A}; T_J = 25\text{ }^\circ\text{C}$	-	430	510	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².

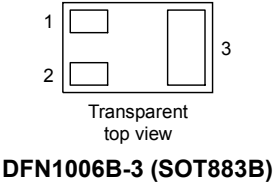
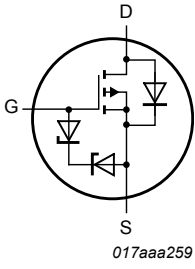


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN1006B-3 (SOT883B)</p>	 <p>017aaa259</p>
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZB320UPE	DFN1006B-3	DFN1006B-3: leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm	SOT883B

7. Marking

Table 4. Marking codes

Type number	Marking code
PMZB320UPE	0101 0010

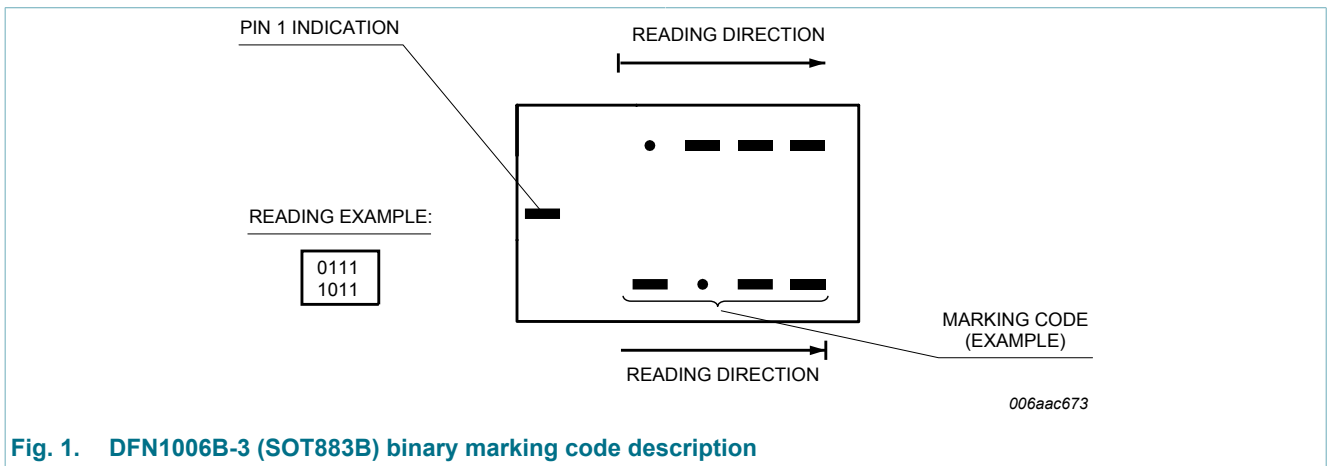


Fig. 1. DFN1006B-3 (SOT883B) binary marking code description

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-30	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-1	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-0.6	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-4	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	350	mW
			[1]	-	760	mW
		T _{sp} = 25 °C		-	6250	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-0.7	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

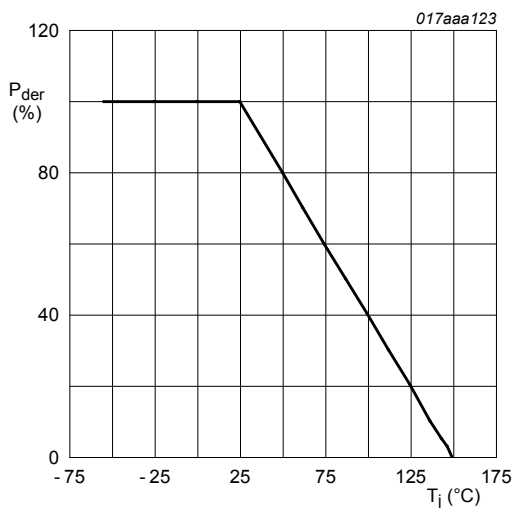


Fig. 2. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

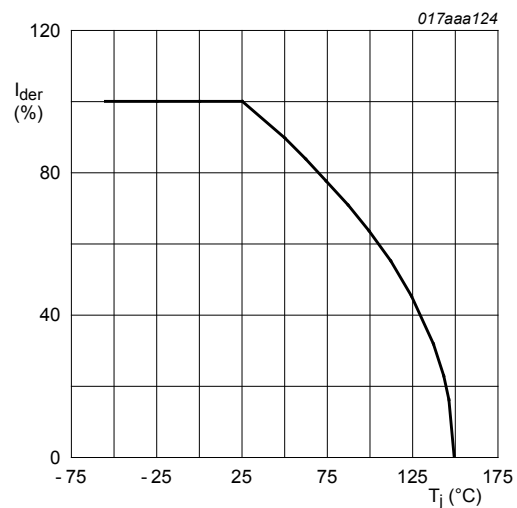
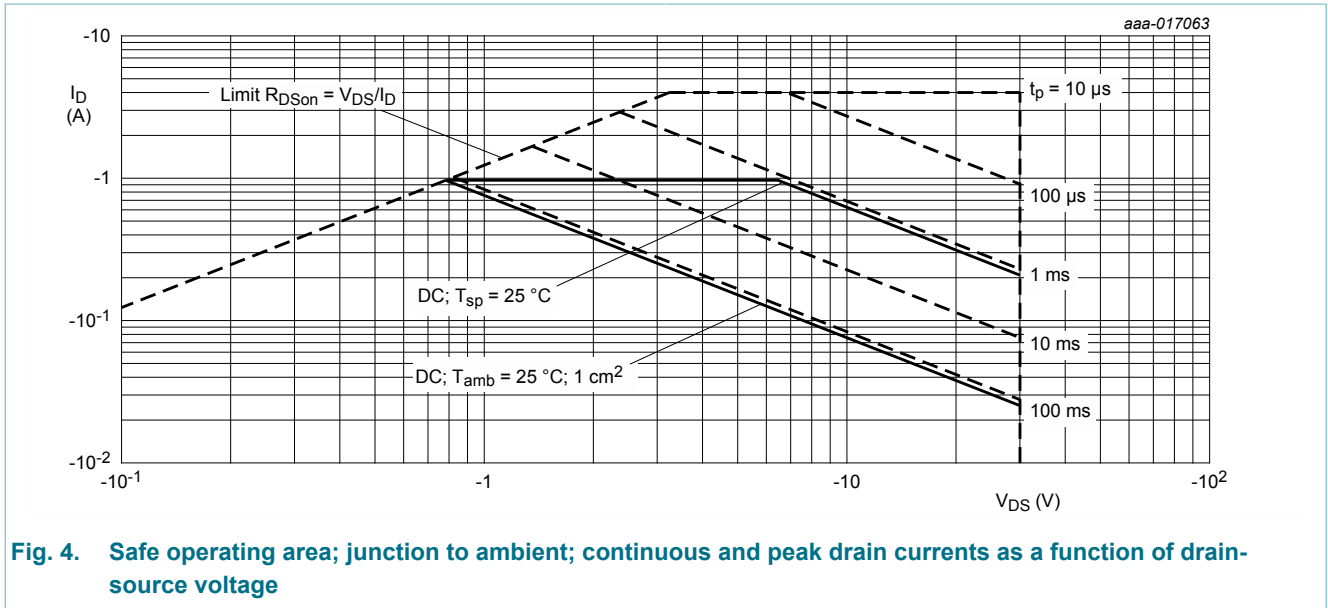


Fig. 3. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	315	360	K/W
			[2]	-	145	165	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	17	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

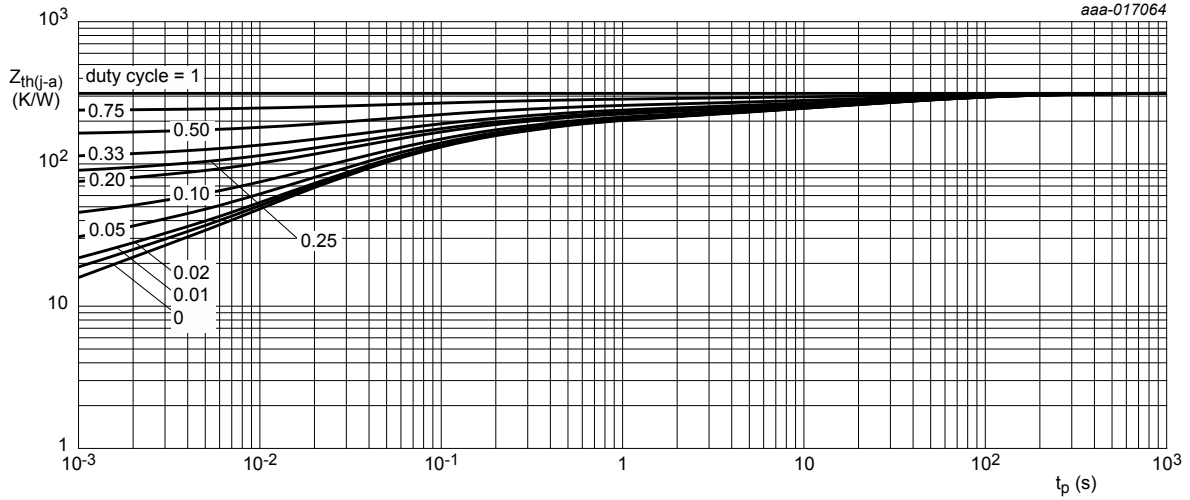


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

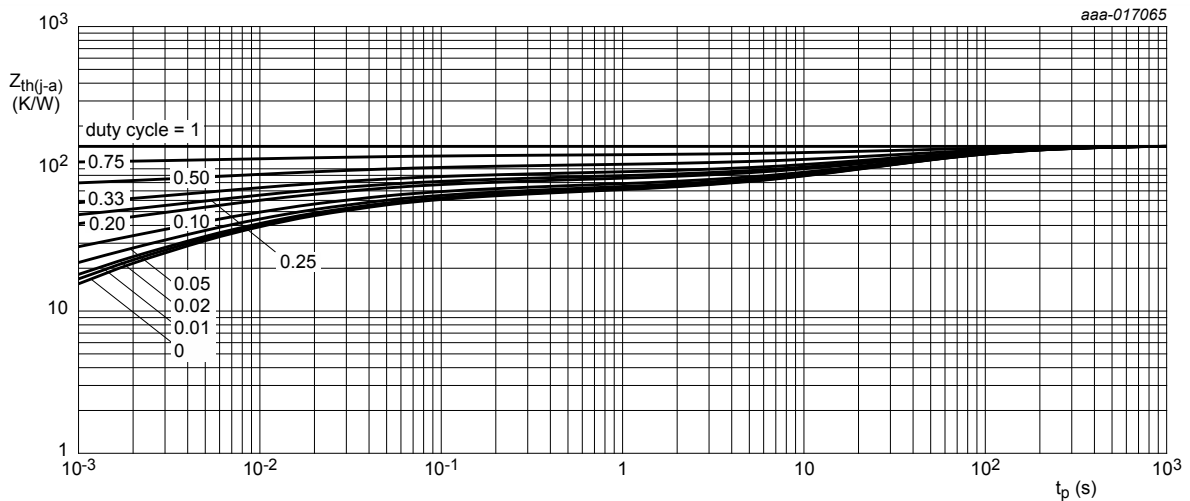


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.45	-0.7	-0.95	V
I_{DSS}	drain leakage current	$V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	5	μA
		$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-5	μA
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -1 A; T_j = 25 \text{ }^\circ C$	-	430	510	m Ω
		$V_{GS} = -4.5 V; I_D = -1 A; T_j = 150 \text{ }^\circ C$	-	680	810	m Ω
		$V_{GS} = -2.5 V; I_D = -0.8 A; T_j = 25 \text{ }^\circ C$	-	570	770	m Ω
		$V_{GS} = -1.8 V; I_D = -0.25 A; T_j = 25 \text{ }^\circ C$	-	750	1140	m Ω
		$V_{GS} = -1.5 V; I_D = -0.01 A; T_j = 25 \text{ }^\circ C$	-	950	1610	m Ω
g_{fs}	forward transconductance	$V_{DS} = -10 V; I_D = -1 A; T_j = 25 \text{ }^\circ C$	-	2.1	-	S
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -15 V; I_D = -1 A; V_{GS} = -4.5 V; T_j = 25 \text{ }^\circ C$	-	1.4	-	nC
Q_{GS}	gate-source charge		-	0.2	-	nC
Q_{GD}	gate-drain charge		-	0.3	-	nC
C_{iss}	input capacitance	$V_{DS} = -15 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	122	-	pF
C_{oss}	output capacitance		-	11	-	pF
C_{rss}	reverse transfer capacitance		-	9	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -15 V; I_D = -1 A; V_{GS} = -4.5 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	3	-	ns
t_r	rise time		-	6	-	ns
$t_{d(off)}$	turn-off delay time		-	22	-	ns
t_f	fall time		-	5	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -0.7 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-1	-1.2	V

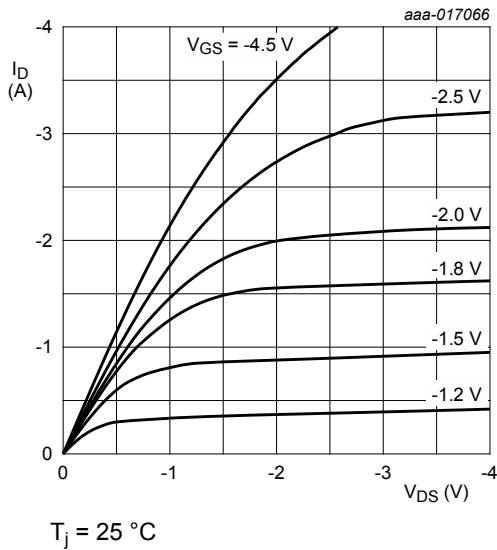


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

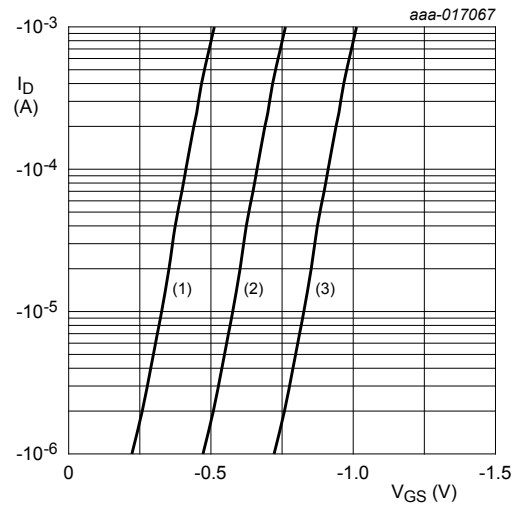


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

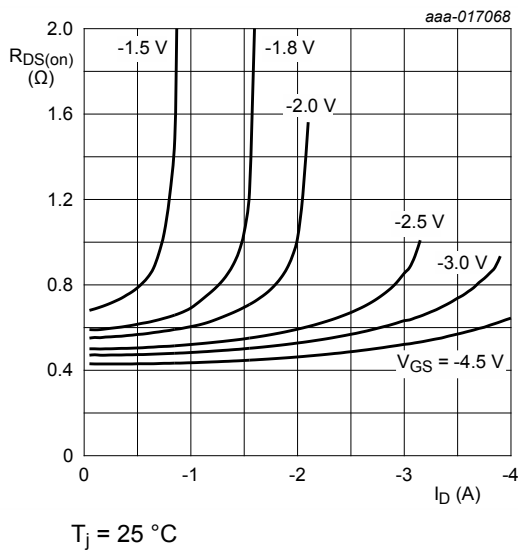


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

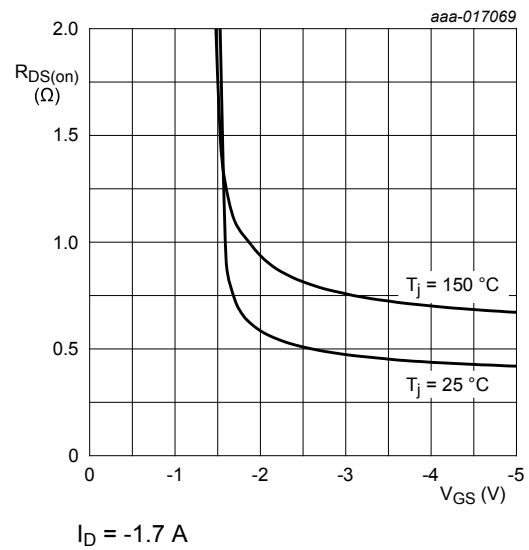
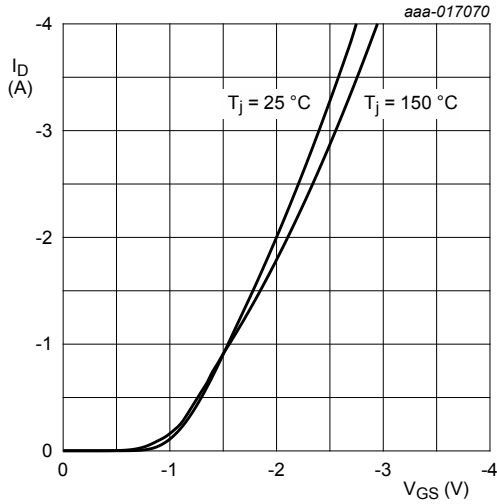


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

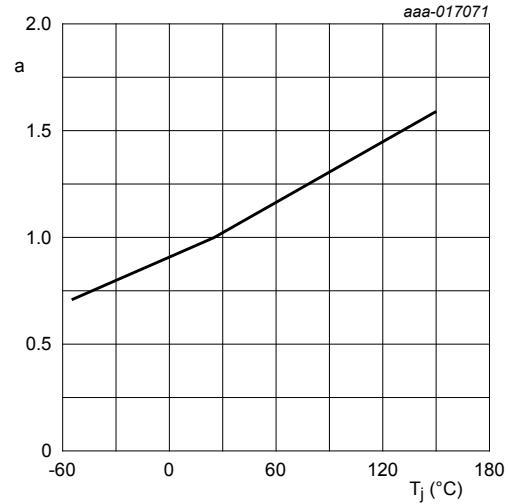
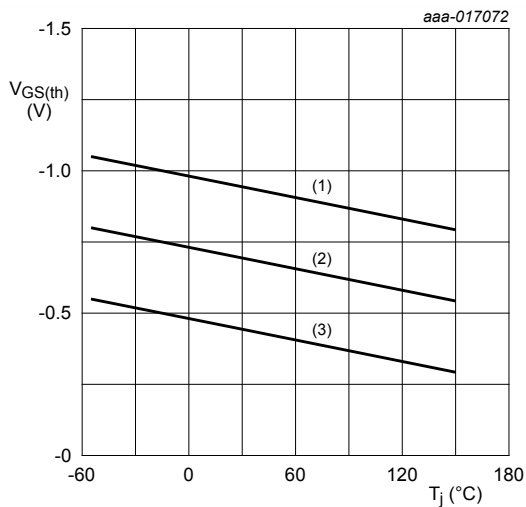


Fig. 12. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

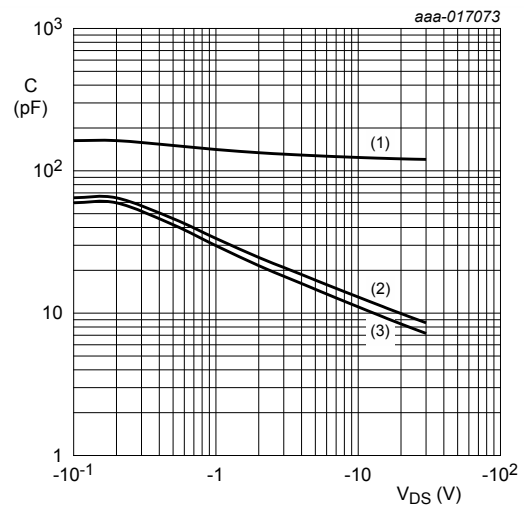
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



$I_D = -250 \mu A; V_{DS} = V_{GS}$

- (1) maximum values
- (2) typical values
- (3) maximum values

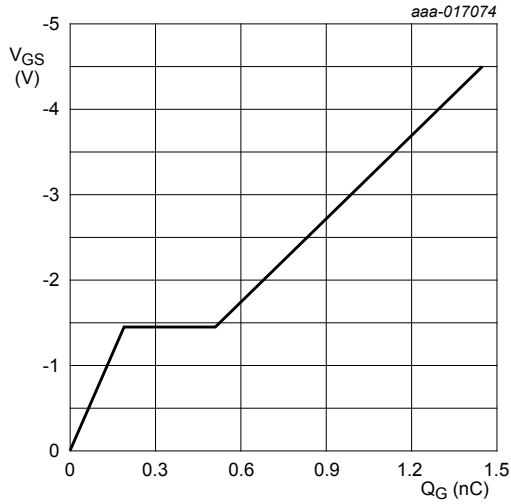
Fig. 13. Gate-source threshold voltage as a function of ambient temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

- (1) C_{iss}
- (2) C_{oss}
- (3) C_{rss}

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -15$ V; $I_D = -1$ A; $T_{amb} = 25$ °C

Fig. 15. Gate-source voltage as a function of gate charge; typical values

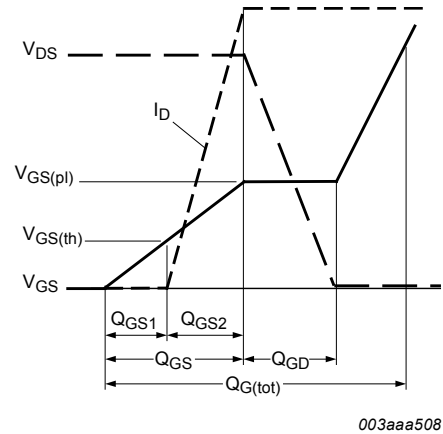
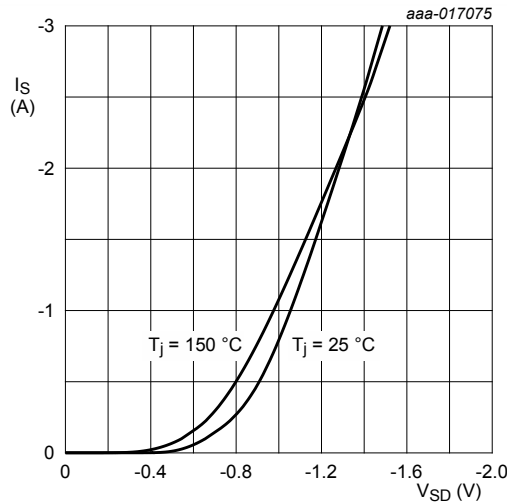


Fig. 16. Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

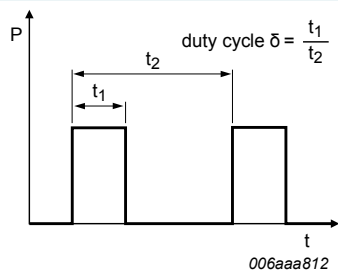


Fig. 18. Duty cycle definition

12. Package outline

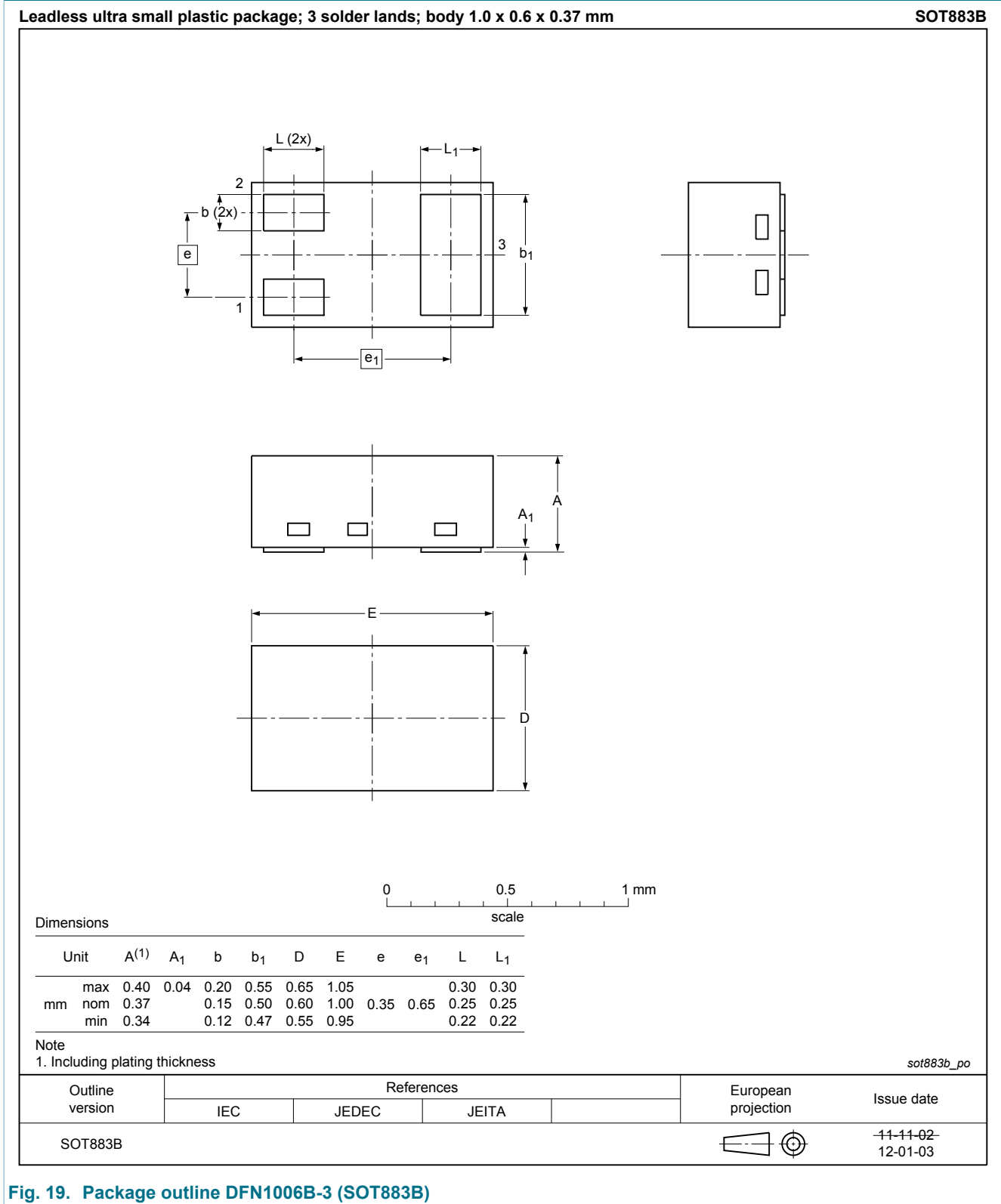


Fig. 19. Package outline DFN1006B-3 (SOT883B)

13. Soldering

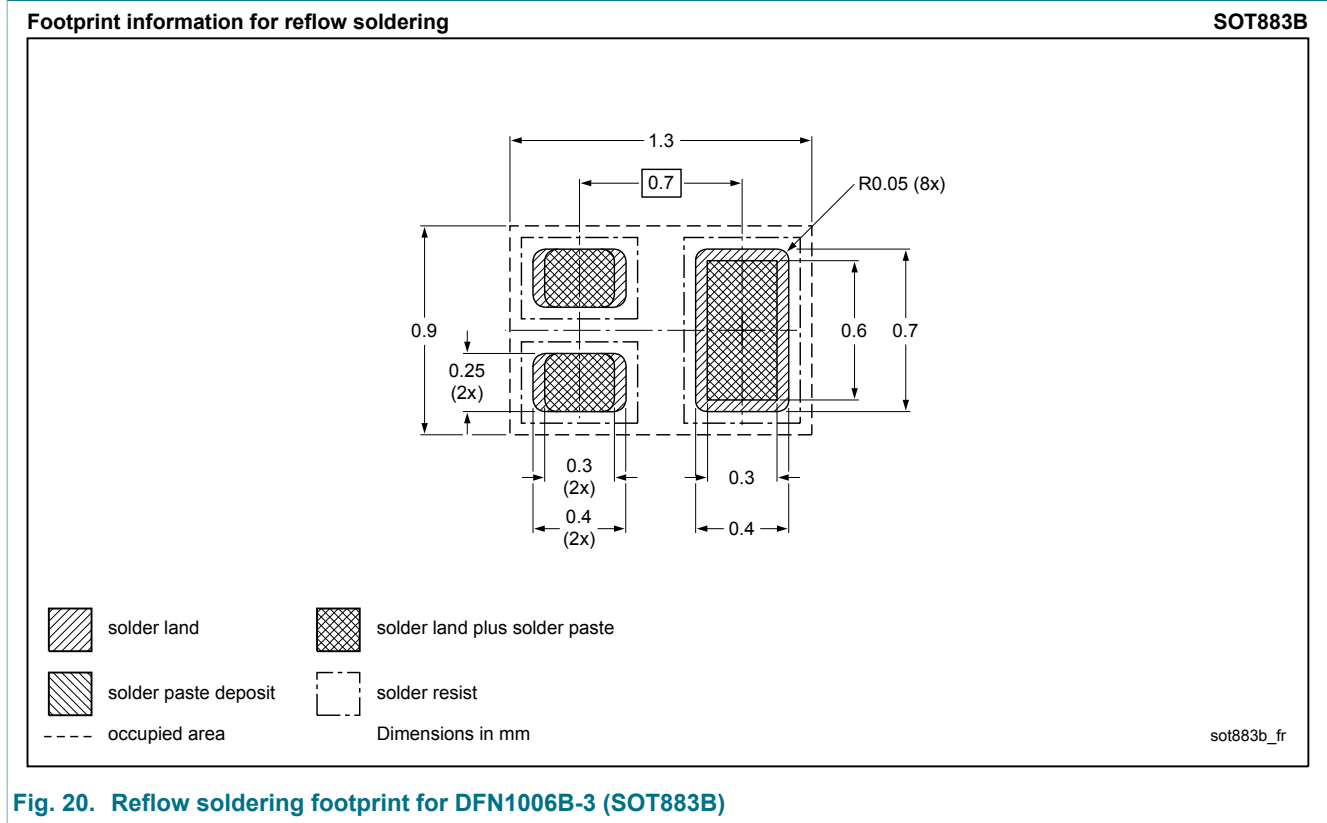


Fig. 20. Reflow soldering footprint for DFN1006B-3 (SOT883B)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMZB320UPE v.1	20150324	Product data sheet	-	-

15. Legal information

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Document status [1][2]	Product status [3]	Definition
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