Sup*IR*Buck™

USER GUIDE FOR IR3840 EVALUATION BOARD

DESCRIPTION

The IR3840 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 5mmx6mm Power QFN package.

Key features offered by the IR3840 include programmable soft-start ramp, precision 0.7V reference voltage, Power Good, thermal protection, programmable switching frequency, Sequence input, Enable input, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3840 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3840 is available in the IR3840 data sheet.

BOARD FEATURES

- V_{in} = +12V (13.2V Max)
- V_{cc}=+5V (5.5V Max)
- V_{out} = +1.8V @ 0- 12A
- F_s=600kHz
- L= 0.6uH
- C_{in}= 4x10uF (ceramic 1206) + 330uF (electrolytic)
- C_{out}= 6x22uF (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 12A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3840 has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). Separate supplies should be applied to these inputs. Vcc input should be a well regulated 4.5V-5.5V supply and it would be connected to Vcc+ and Vcc-.

If single 12V application is required connect R7 (zero Ohm resistor) which enables the on board bias regulator (see schematic). In this case there is no need of external Vcc supply.

The output can track a sequencing input at the start-up. *For sequencing application, R16 should be removed and the external sequencing source should be applied between Seq. and Agnd.* The value of R14 and R28 can be selected to provide the desired ratio between the output voltage and the tracking input. *For proper operation of IR3840, the voltage at Seq. pin should not exceed Vcc.*

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
Vcc+	Vcc input
Vcc-	Ground for Vcc input
VOUT-	Ground of V_{out}
VOUT+	V_{out} (+1.8V)
Enable	Enable
Seq.	Sequence Input
P_Good	Power Good Signal

LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. The IR3840 SupIRBuck and all of the passive components are mounted on the top side of the board.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3840. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the SupIRBuck. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

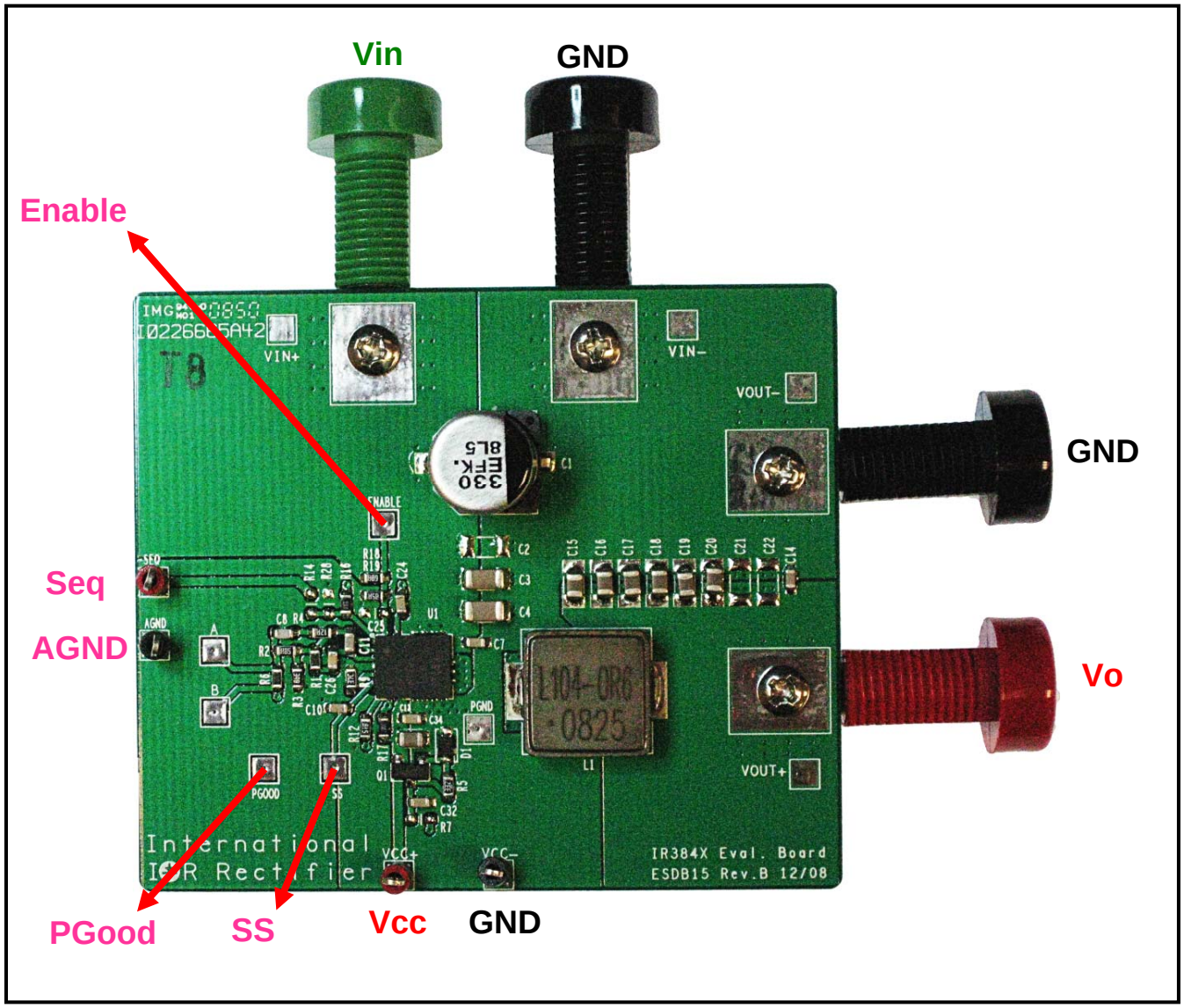


Fig. 1: Connection diagram of IR384x evaluation boards

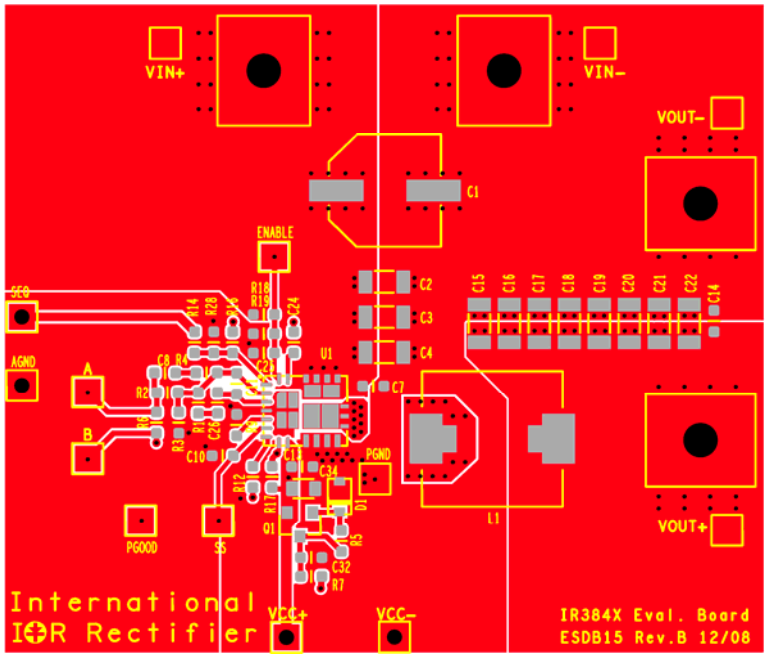


Fig. 2: Board layout, top overlay

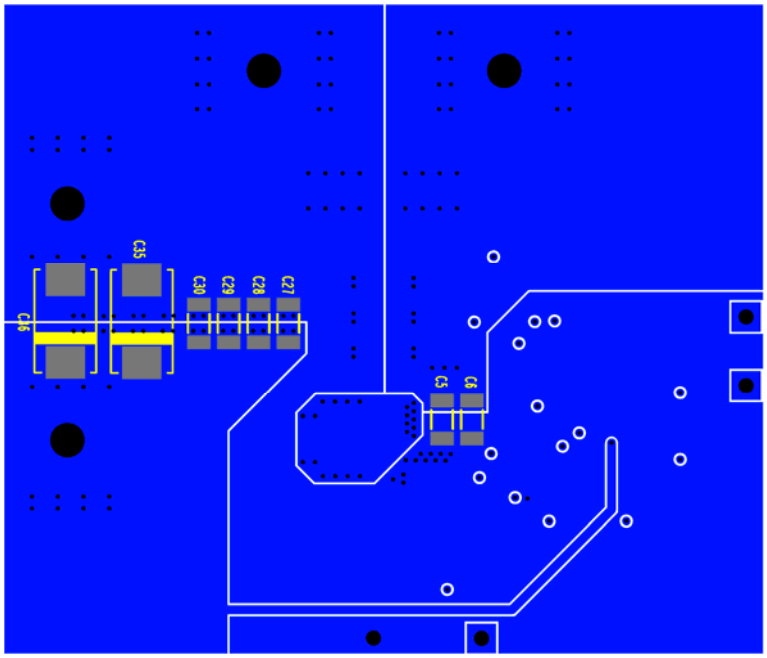


Fig. 3: Board layout, bottom overlay (rear view)

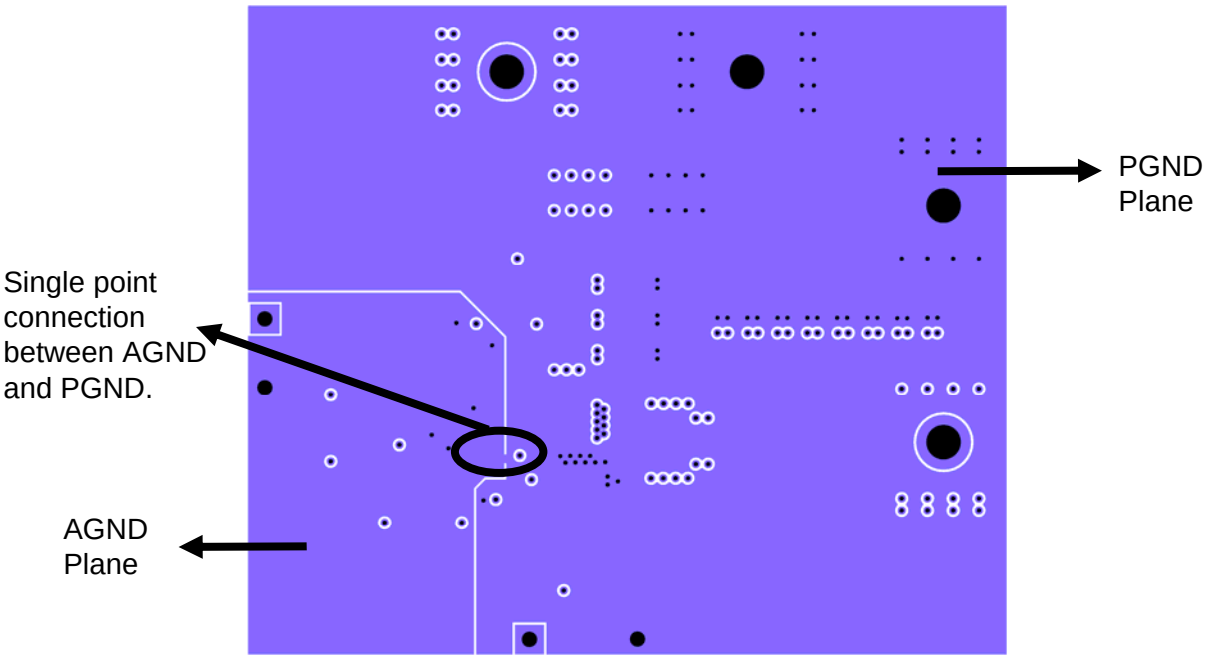


Fig. 4: Board layout, mid-layer I.

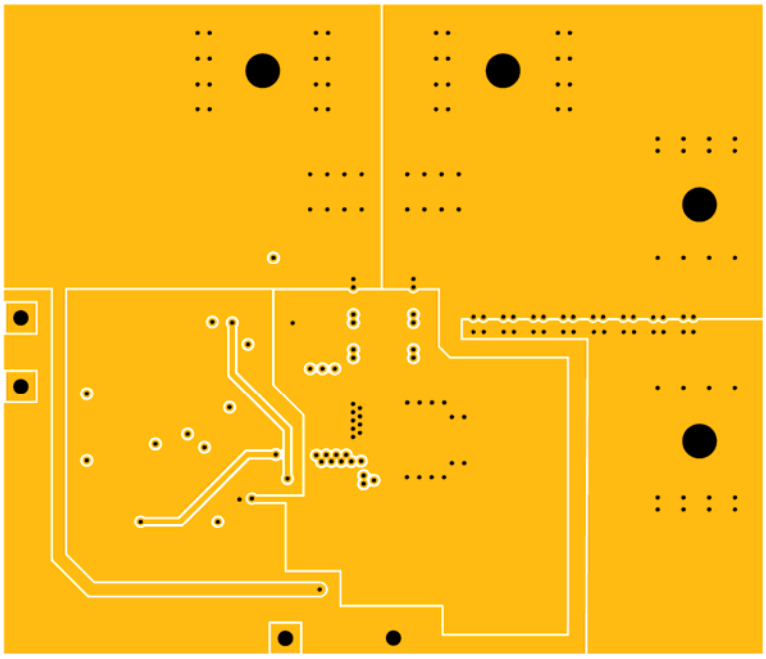
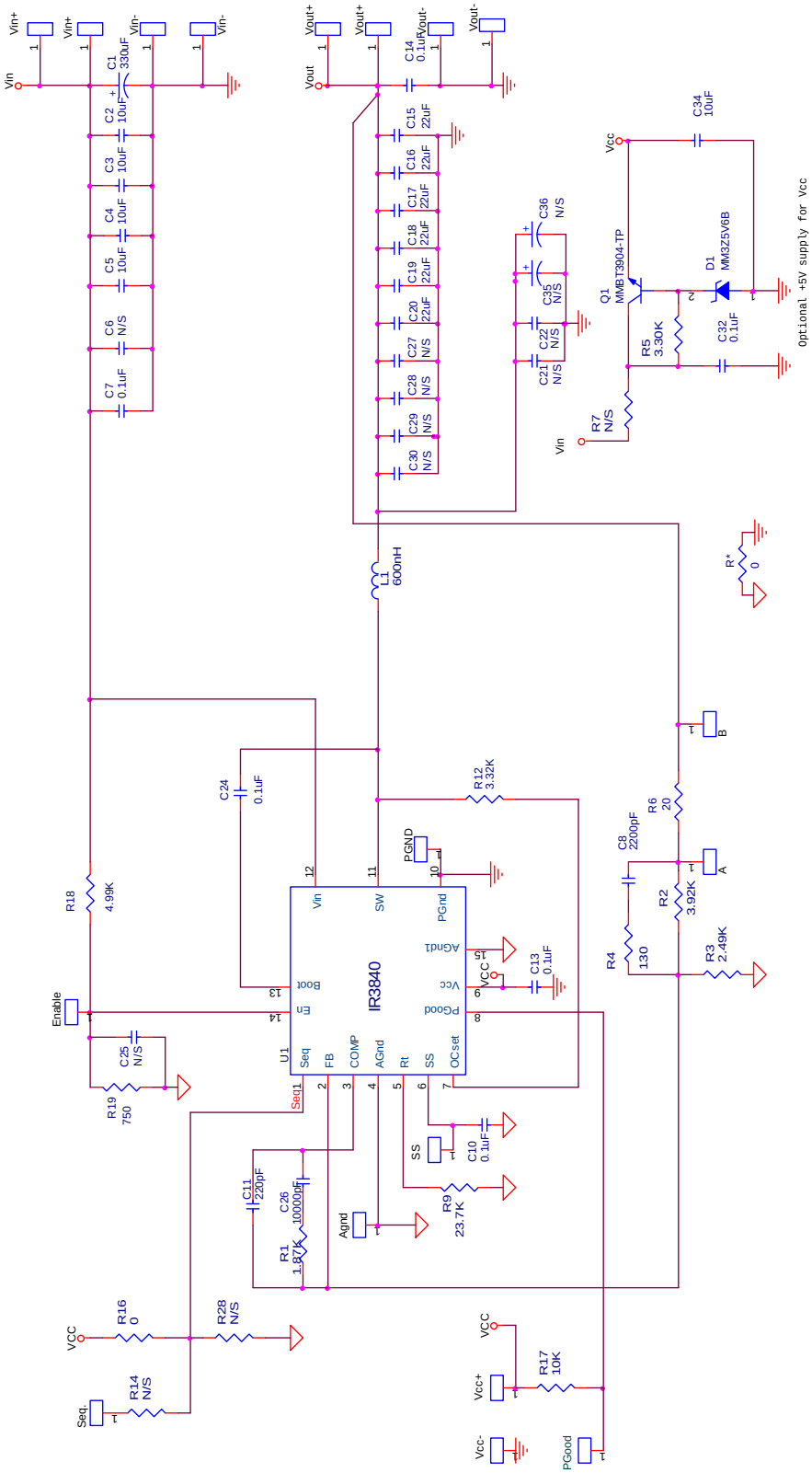


Fig. 5: Board layout, mid-layer II.



Single point of connection between Power Ground and Signal ("analog") Ground

Fig. 6: Schematic of the IR3840 evaluation board

Bill of Materials

Item	Quantity	Part Reference	Value	Description	Manufacturer	Part Number
1	1	C1	330uF	SMD Elecrolytic, Fsize, 25V, 20%	Panasonic	EEV-FK1E331P
2	1	C34	10uF	0805, 10V, X5R, 20%	Panasonic - ECG	ECJ-GVB1A106M
3	4	C3 C4 C5 C2	10uF	1206, 16V, X5R, 20%	Panasonic - ECG	ECJ-3YB1C106M
4	6	C7 C10 C13 C14 C24 C32	0.1uF	0603, 25V, X7R, 10%	Panasonic - ECG	ECJ-1VB1E104K
5	1	C8	2200pF	0603, 50V, NP0, 5%	Murata	GRM1885C1H222JA01D
6	1	C11	220pF	0603, 50V, NP0, 5%	Panasonic- ECG	ECJ-1VC1H221J
7	6	C15 C16 C17 C18 C19 C20	22uF	0805, 6.3V, X5R, 20%	Panasonic- ECG	ECJ-2FB0J226M
8	1	C26	10000pF	0603, 50V, X7R, 10%	Panasonic - ECG	ECJ-1VB1H103K
9	1	D1	MM3Z5V6B	MM3Z5V6B,Zener, 5.6V	Fairchild	MM3Z5V6B
10	1	L1	0.6uH	11.5x10x4mm, 20%, 1.7mOhm	Delta	MPL104-0R6IR
11	1	Q1	MMBT3904/SOT	NPN, 40V, 200mA, SOT-23	Fairchild	MMBT3904/SOT
12	1	R5	3.3k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX3301
13	1	R18	4.99k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX4991
14	1	R4	130	Thick Film, 0603,1/10W,1%	Panasonic - ECG	ERJ-3EKF1300V
15	1	R6	20	Thick Film, 0603,1/10 W,1%	Vishey/Dale	CRCW060320R0FKEA
16	1	R9	23.7k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2372
17	1	R16	0	Thick Film, 0603,1/10 W,5%	Vishay/Dale	CRCW06030000Z0EA
18	1	R12	3.32k	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX3321
19	1	R17	10.0k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX1002
20	1	R19	750	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX7500
21	1	R1	1.87k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX1871
22	1	R2	3.92k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX3921
23	1	R3	2.49k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2491
24	1	U1	IR3840	PQFN, 6mmx5mm, 12A SupIRBuck	International Rectifier	IR3840MPbF

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc=5V, Vo=1.8V, Io=0-12A, Room Temperature, No Air Flow

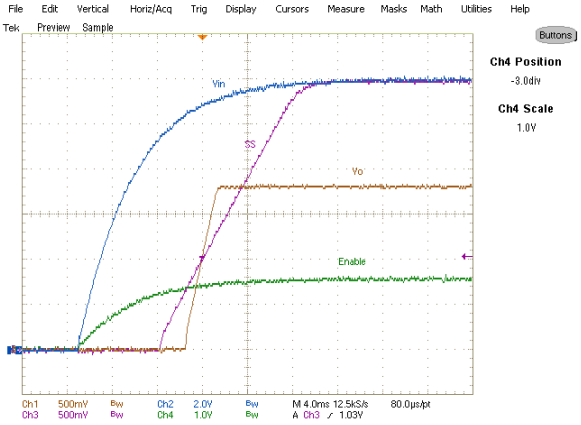


Fig. 7: Start up at 12A Load
Ch_1:V_o, Ch_2:V_{in}, Ch_3:V_{SS}, Ch_4:Enable

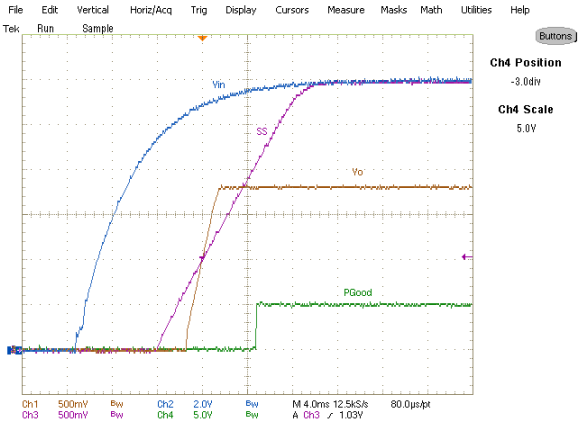


Fig. 8: Start up at 12A Load,
Ch_1:V_o, Ch_2:V_{in}, Ch_3:V_{SS}, Ch_4:V_{PGood}

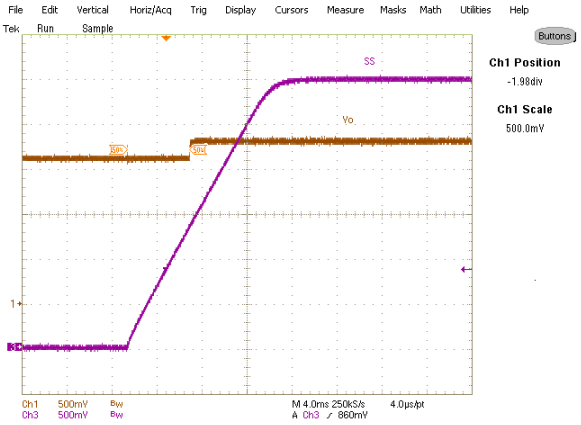


Fig. 9: Start up with 1.62V Pre Bias, 0A Load, Ch_1:V_o, Ch_3:V_{SS}

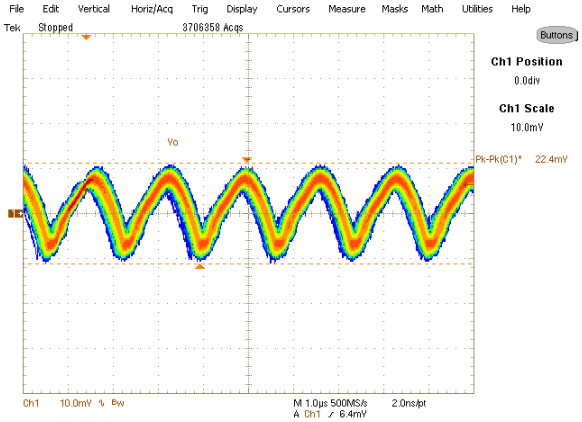


Fig. 10: Output Voltage Ripple, 12A load
Ch_1: V_{out}

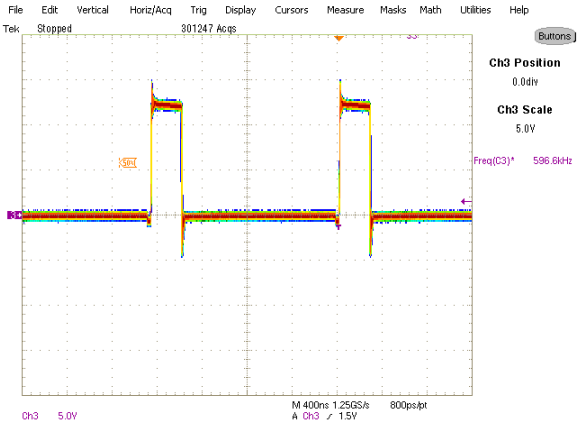


Fig. 11: Inductor node at 12A load
Ch_3:LX

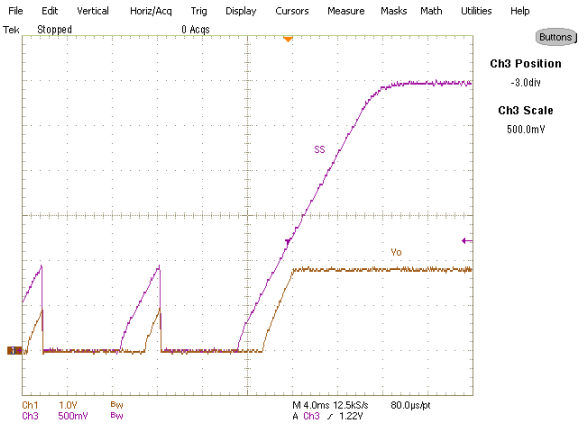


Fig. 12: Short (Hiccup) Recovery
Ch_1:V_{out} , Ch_3:V_{ss}

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=0-12A, Room Temperature, No Air Flow

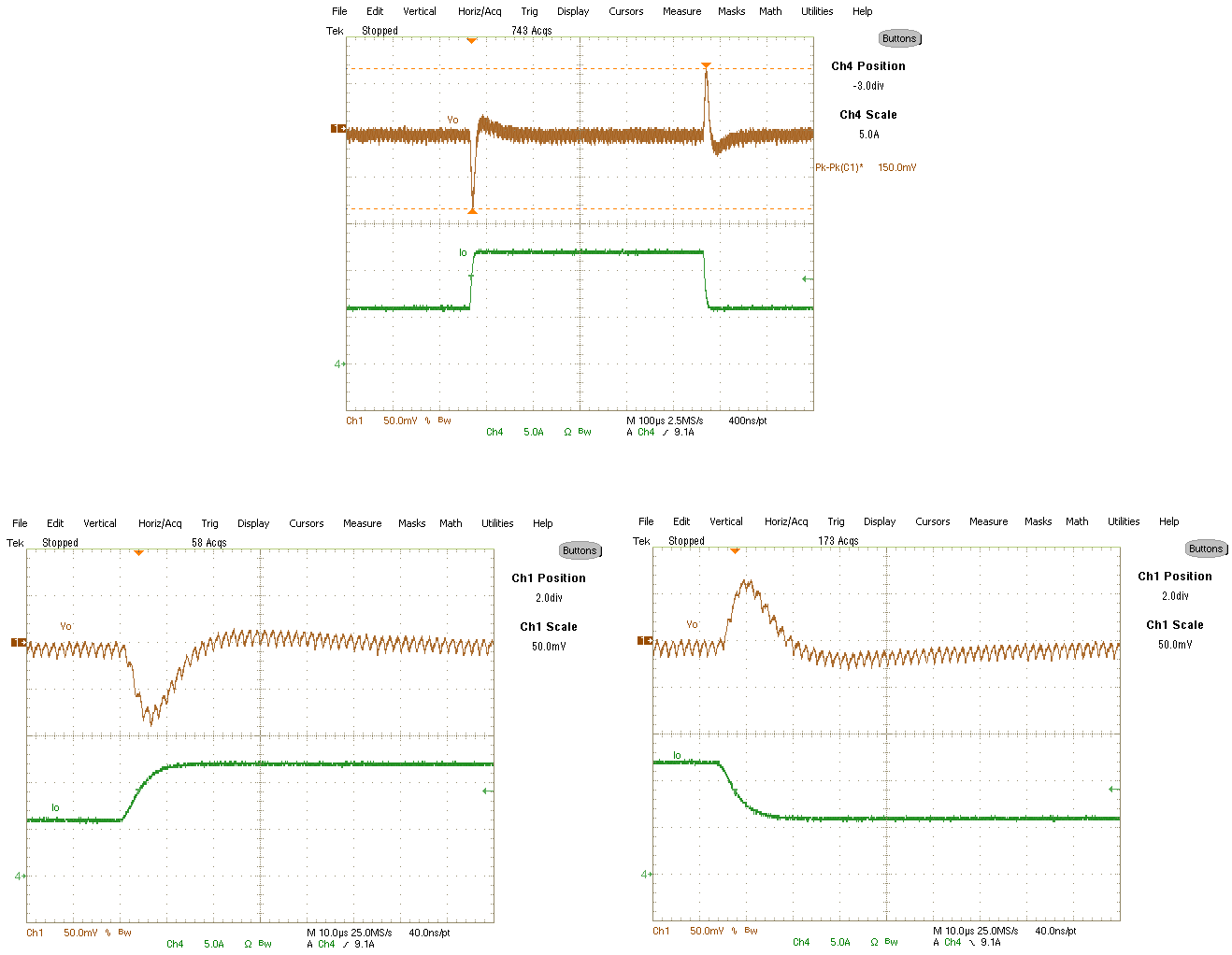


Fig. 13: Transient Response, 6A to 12A step 2.5A/µs
Ch_1:V_{out}, Ch_4:I_{out}

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=12A, Room Temperature, No Air Flow

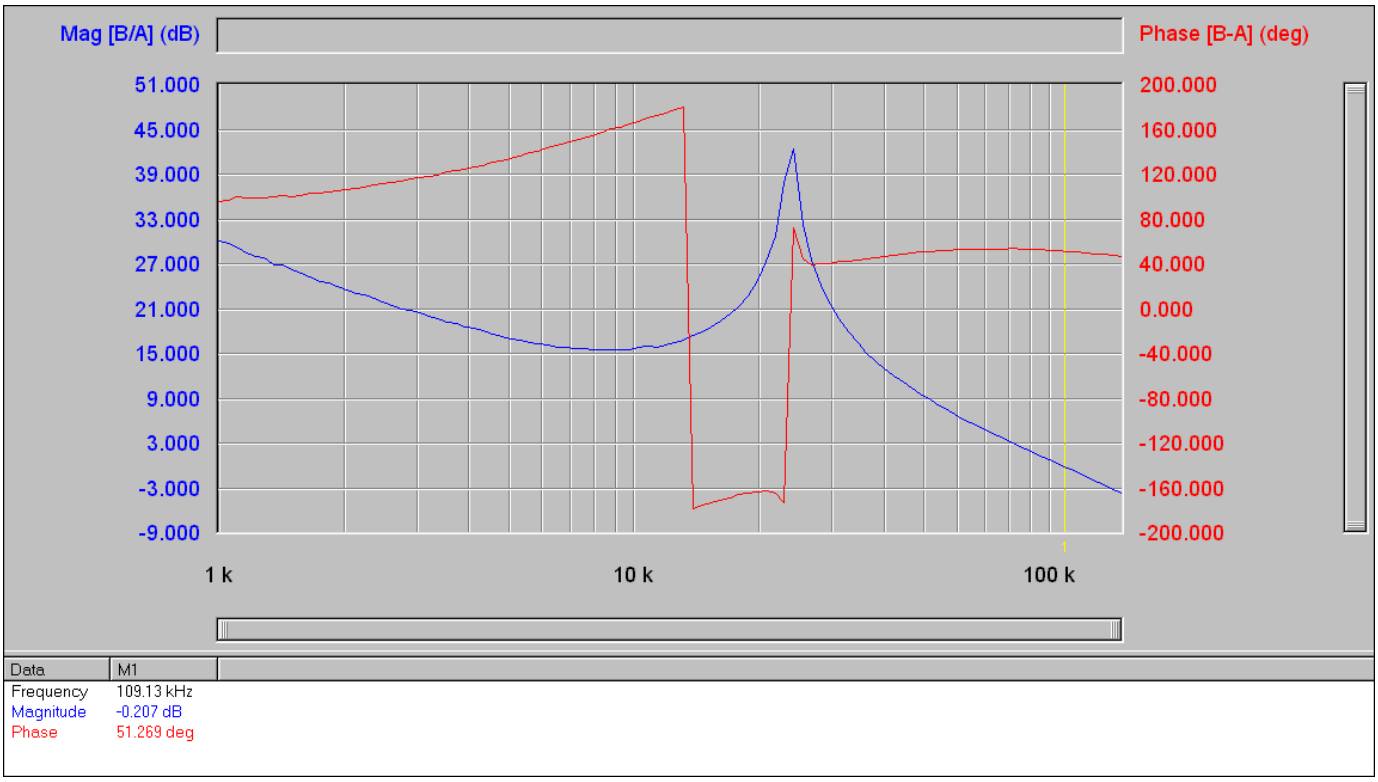


Fig. 14: Bode Plot at 12A load shows a bandwidth of 109kHz and phase margin of 51 degrees

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vo=1.8V, Io=0- 12A, Room Temperature, No Air Flow

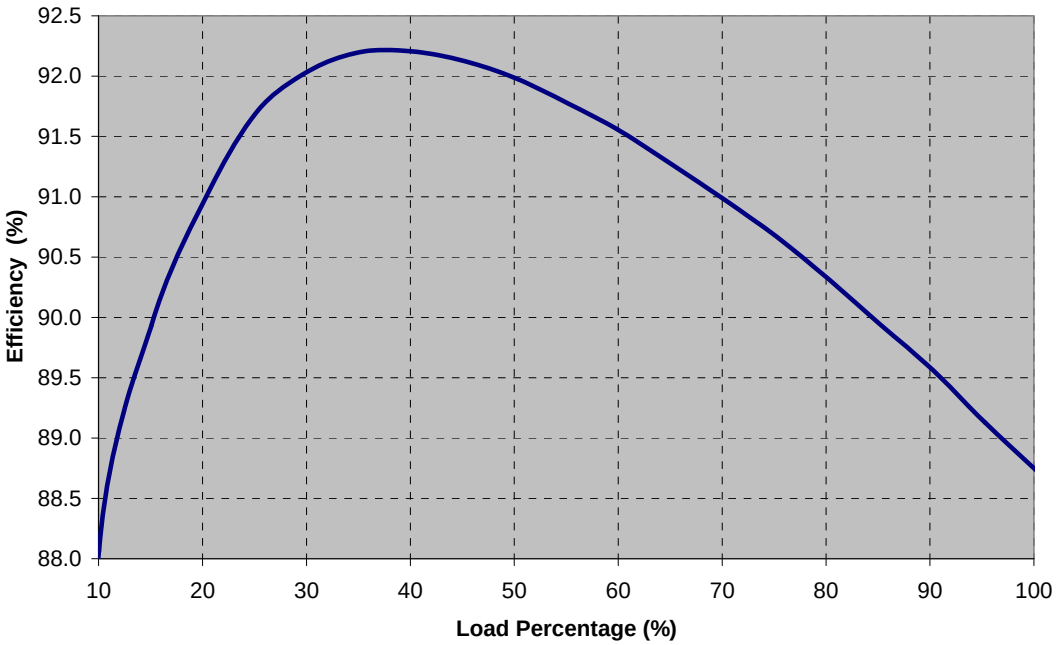


Fig.15: Efficiency versus load current

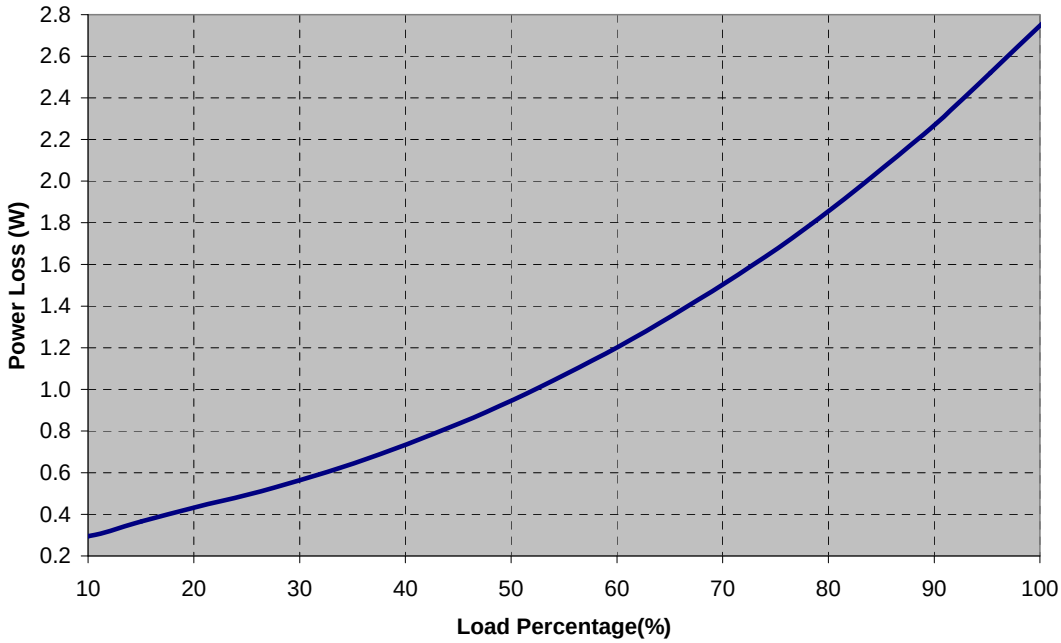


Fig.16: Power loss versus load current

THERMAL IMAGES
Vin=12V, Vo=1.8V, Io=12A, Room Temperature, No Air Flow

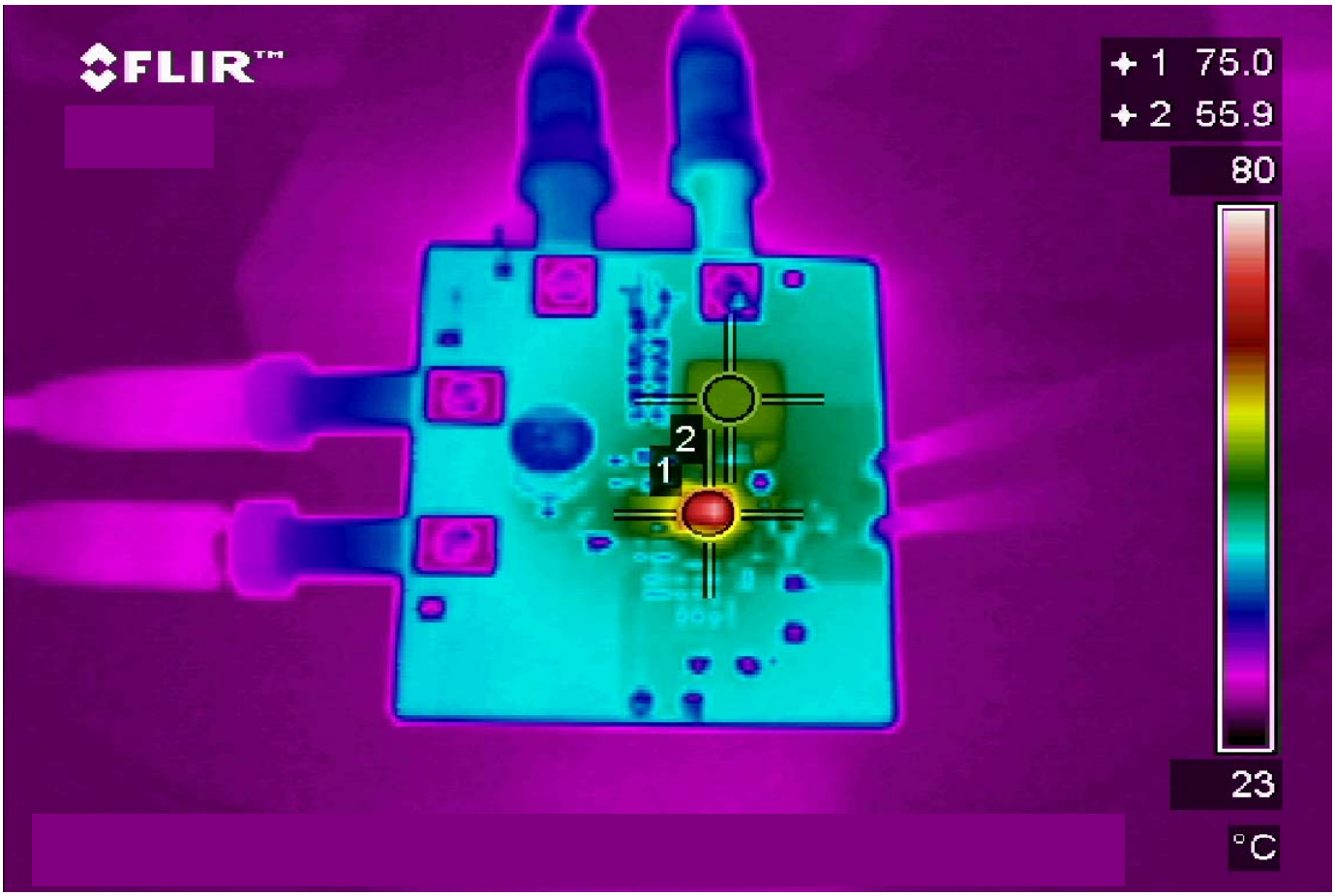


Fig. 17: Thermal Image at 12A load
Test points 1 and 2 are IR3840 and inductor, respectively.

Simultaneous Tracking at Power Up and Power Down
Vin=12V, Vo=1.8V, Io=12A, Room Temperature, No Air Flow

In order to run the IR3840 in the simultaneous tracking mode, following steps should be taken:
- Remove R16 from the board.
- Set the value of R14 and R28 as R2 (3.92K) and R3 (2.49K), respectively.
- Connect the controlling input across SEQ and AGND test points on the board. This voltage should be at least 1.15 time greater than Vo. For the following test results a 0-3.3V source is applied to SEQ pin.
- The controlling input should be applied after the SS pin is clamped to 3.0V.

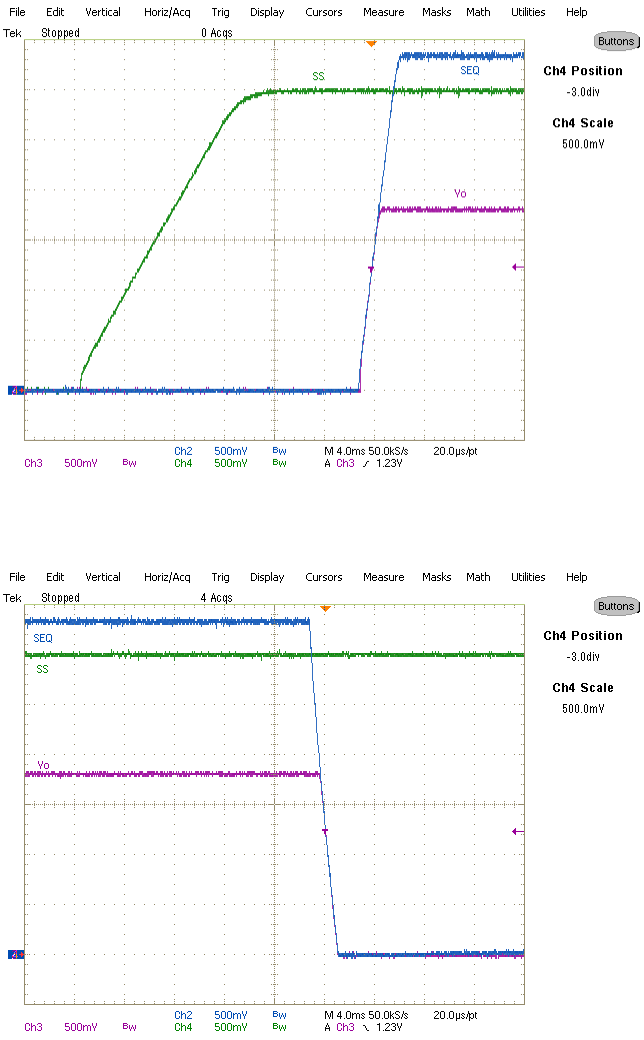


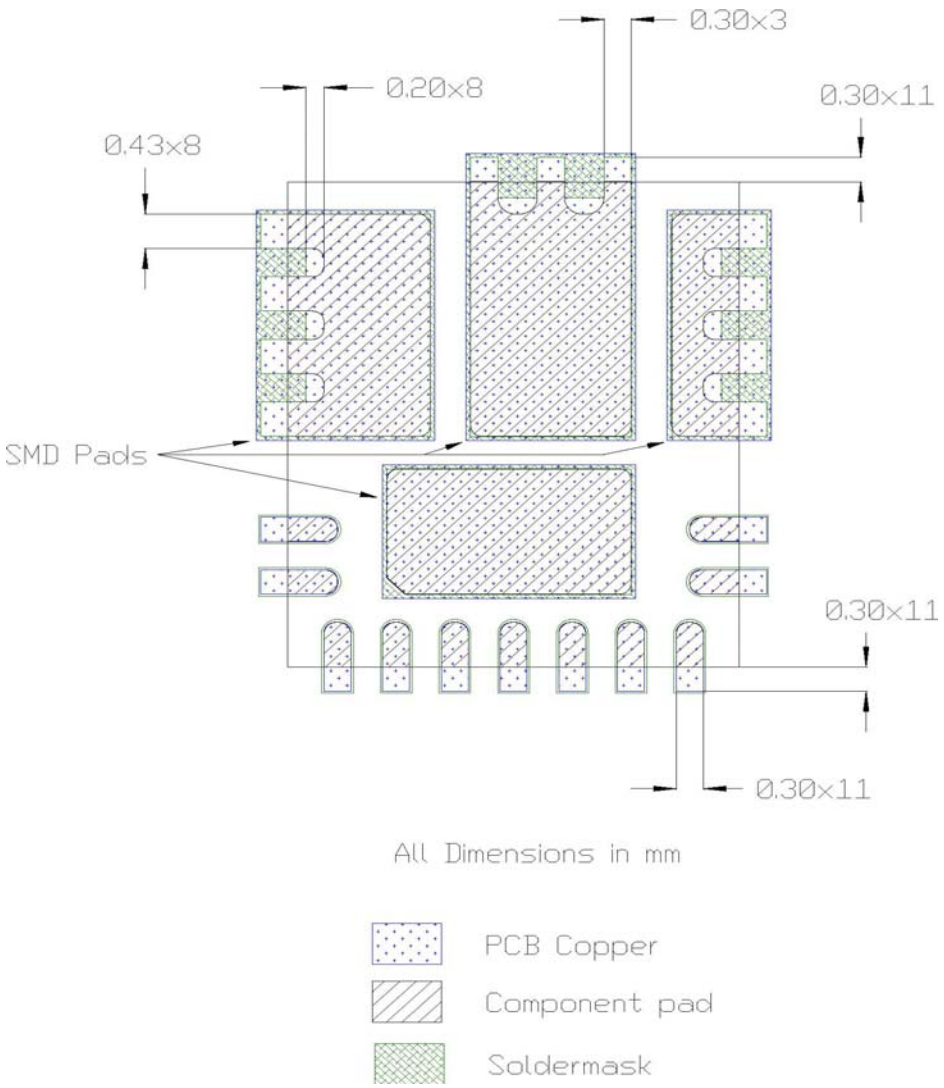
Fig. 18: Simultaneous Tracking a 3.3V input at power-up and shut-down
Ch2: SEQ Ch3:Vo Ch4: SS (1.8V)

PCB Metal and Components Placement

The lead lands (the 11 IC pins) width should be equal to the nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.

Lead land length should be equal to the maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

The pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.

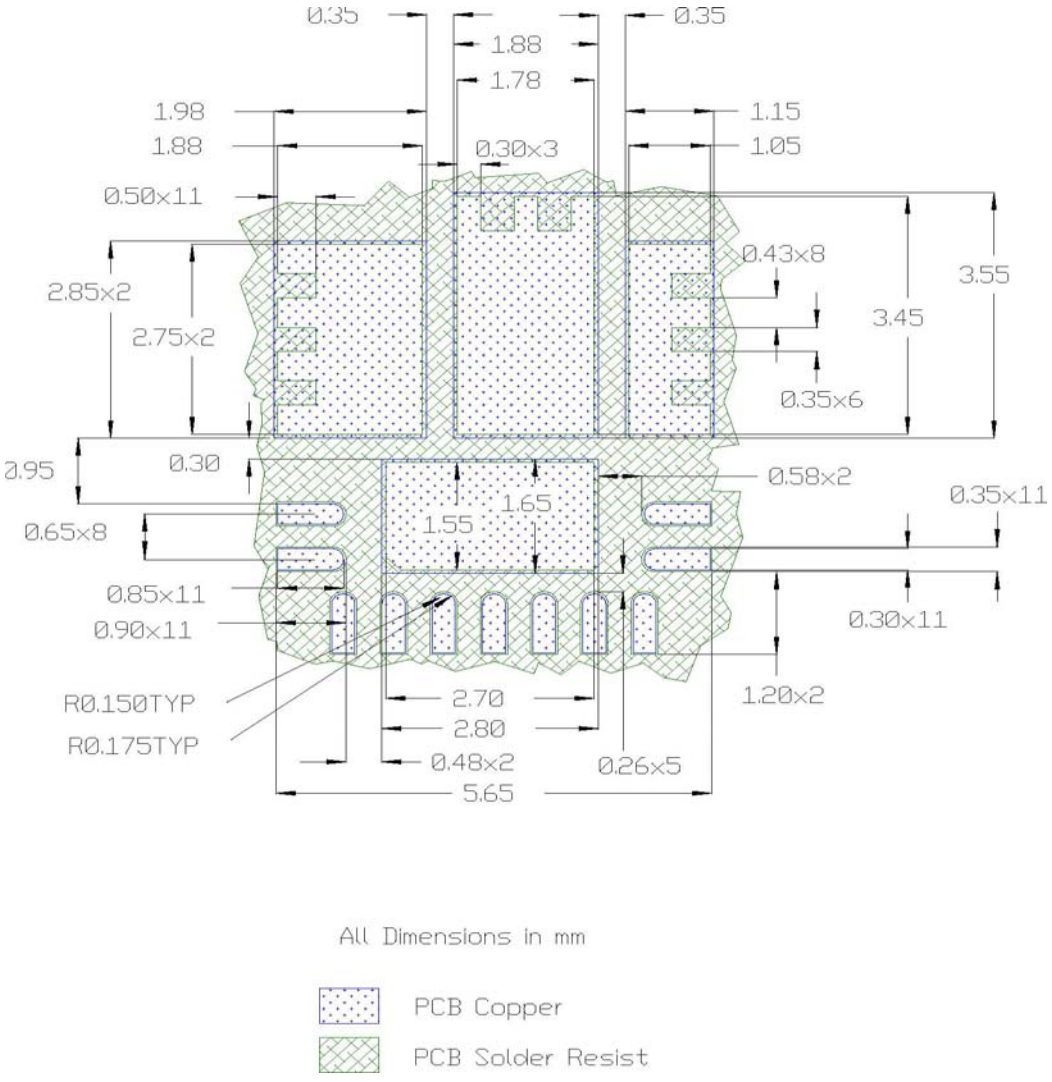


Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

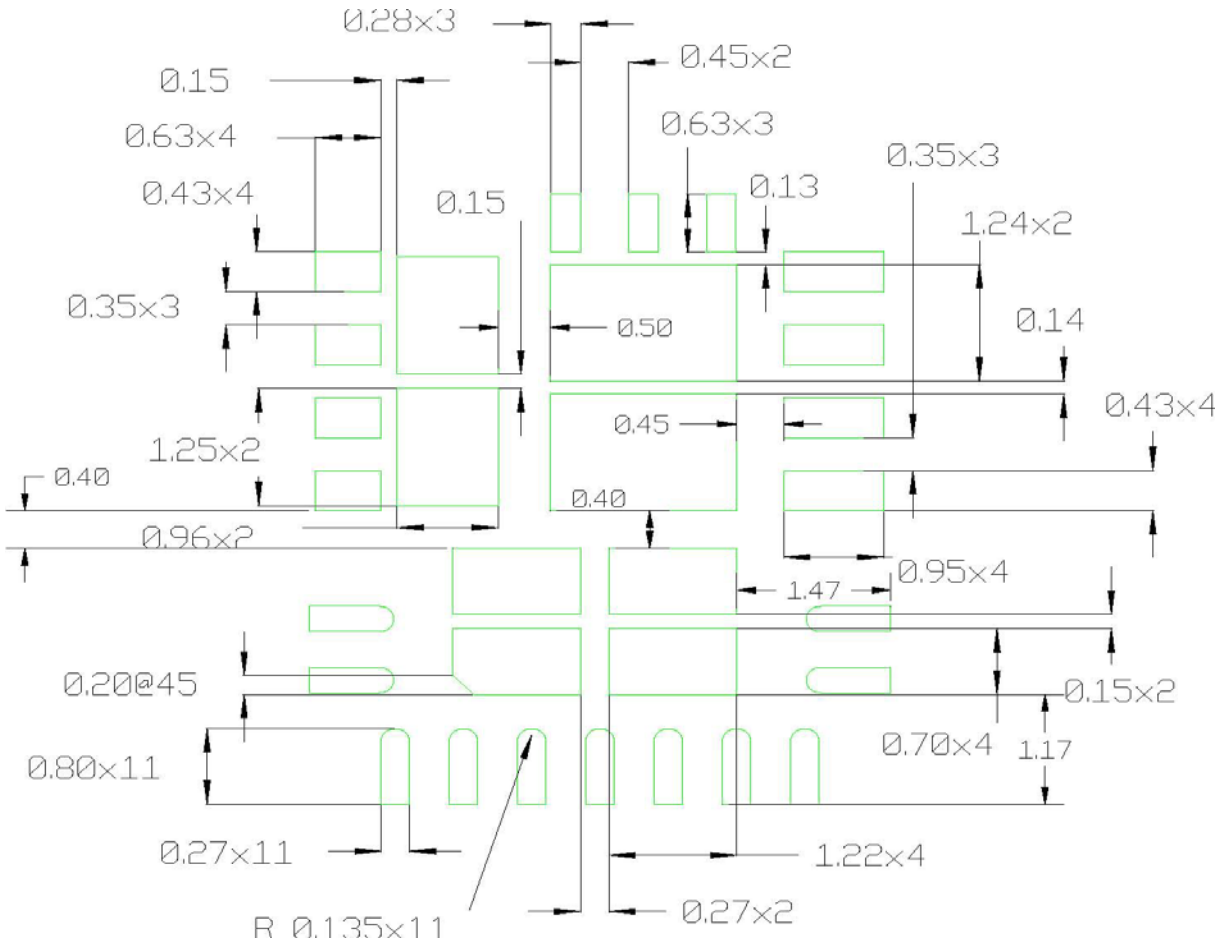
The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

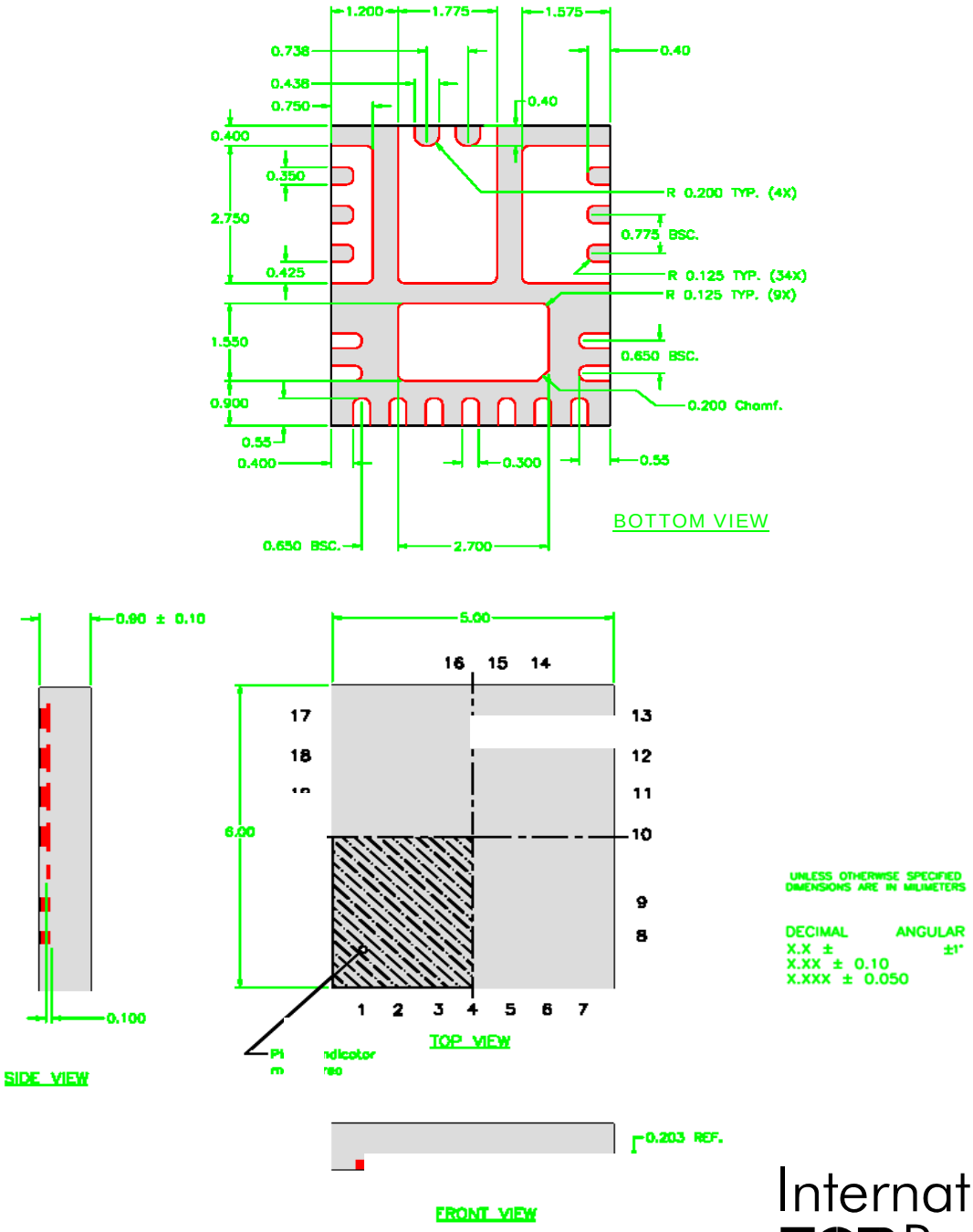


Stencil Design

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm



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