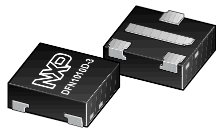


PMXB65UPE

12 V, P-channel Trench MOSFET

8 July 2014 — Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package: 1.1 × 1.0 × 0.37 mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection 1.5 kV HBM
- Drain-source on-state resistance R_{DSon} = 59 mΩ
- Very low gate-source threshold voltage for portable applications $V_{GS(th)}$ = -0.68 V

3. Applications

- High-side load switch and charging switch for portable devices
- Power management in battery driven portables
- LED driver
- DC-to-DC converter

4. Quick reference data

Table 1. Quick reference data

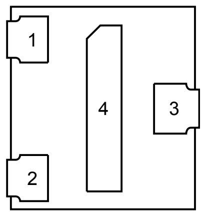
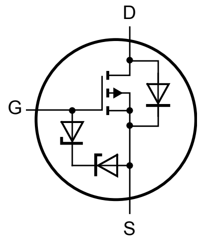
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-12	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-	-3.2	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -3.2 A; T_j = 25 °C		-	59	72	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

Scan or click this QR code to view the latest information for this product

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view **DFN1010D-3 (SOT1215)**	
2	S	source		
3	D	drain		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMXB65UPE	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB65UPE	01 10 00

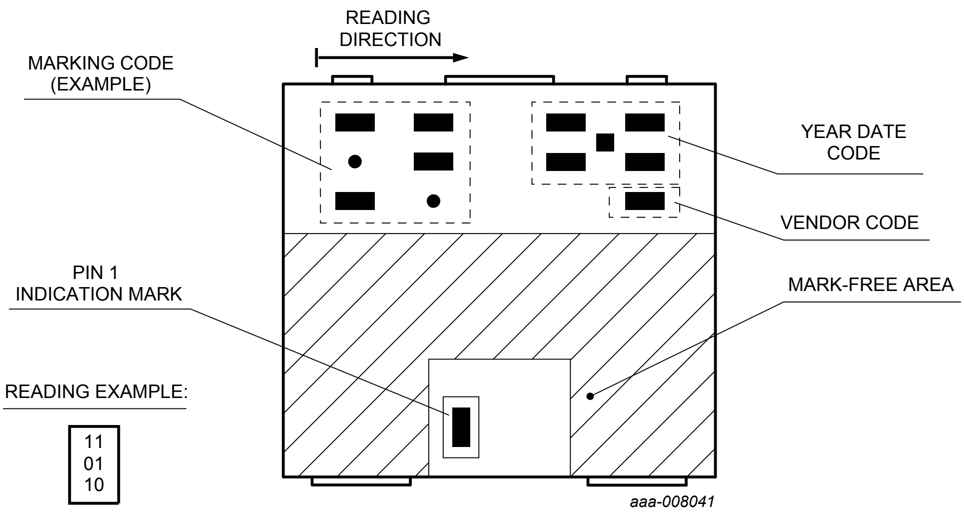


Fig. 1. DFN1010D-3 (SOT1215) binary marking code description

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-12	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-3.2	A
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-2.1	A
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	-13	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	317	mW
			[1]	-	1070	mW
		T_{sp} = 25 °C		-	8330	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-1	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

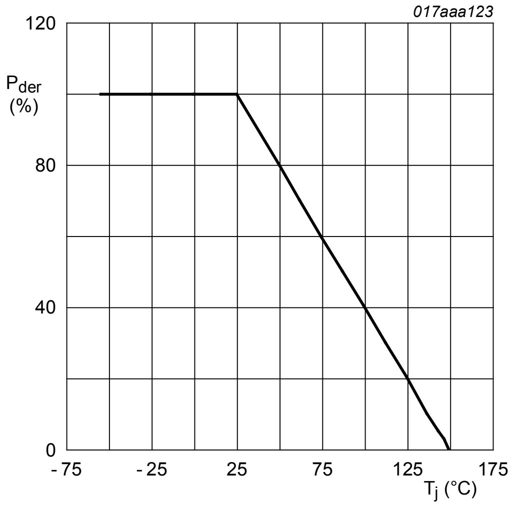


Fig. 2. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

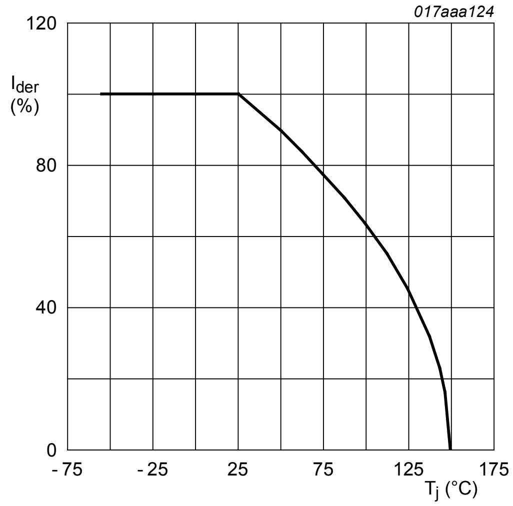
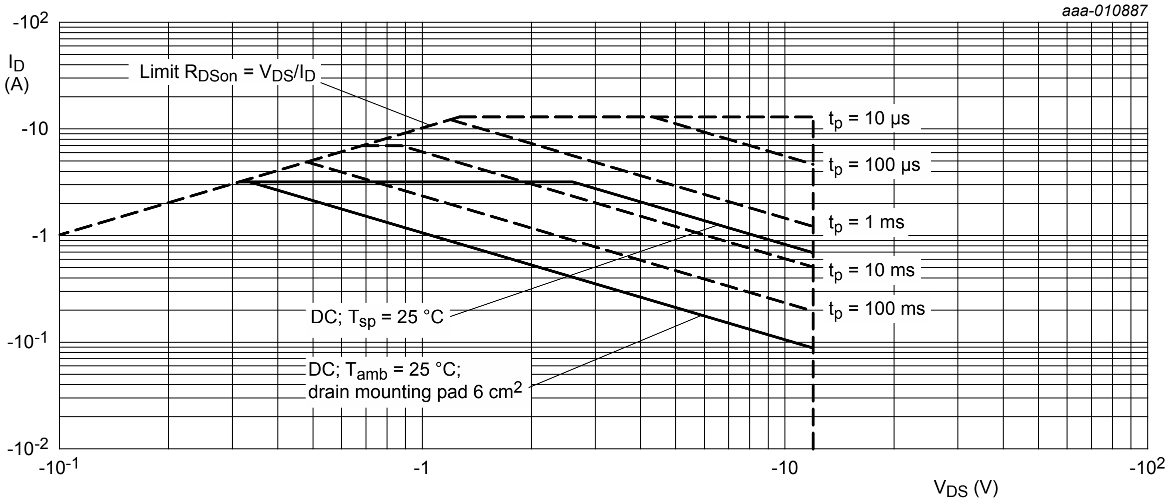


Fig. 3. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$



I_{DM} = single pulse

Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

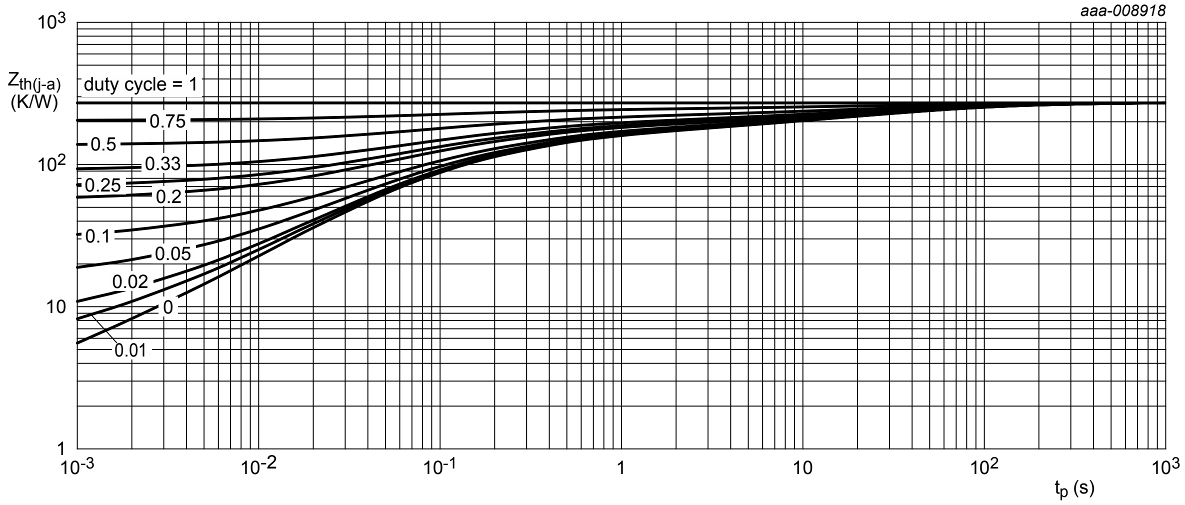
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	271	312	K/W
			[2]	-	102	117	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W

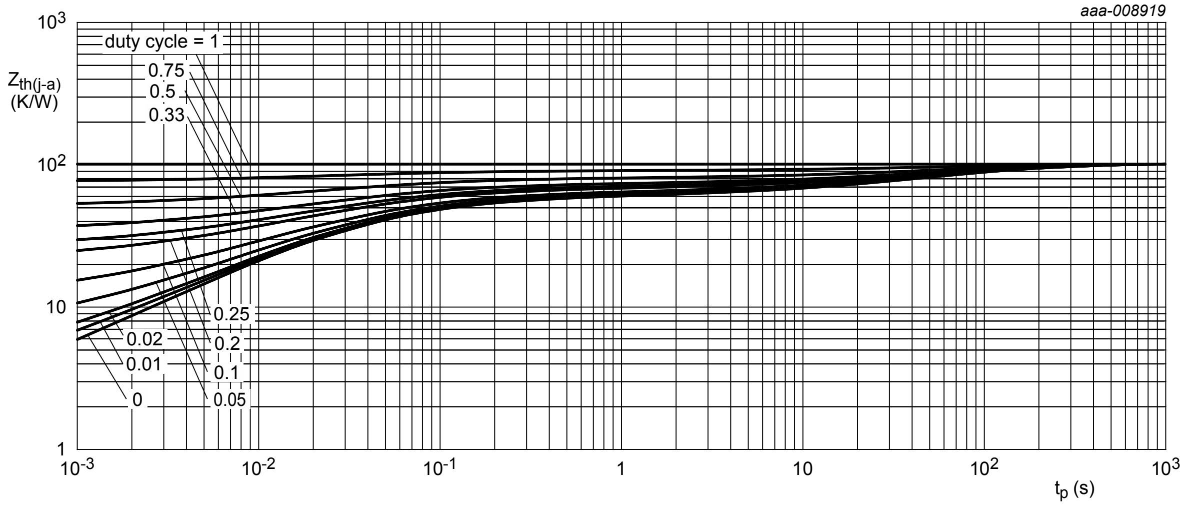
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2.



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



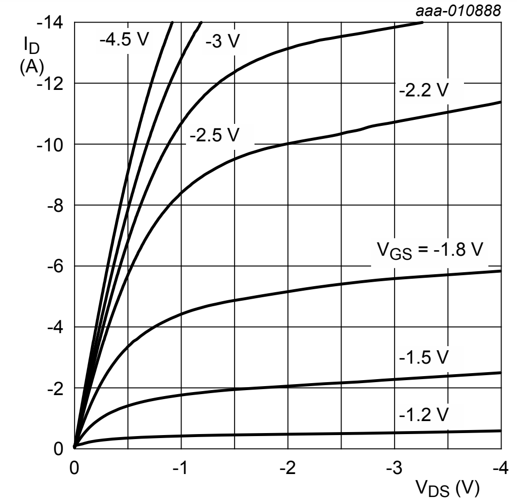
FR4 PCB, mounting pad for drain 6 cm^2

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

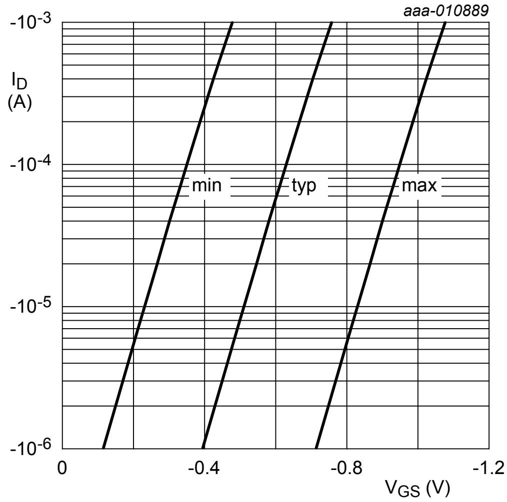
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C		-12	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS}; T_j = 25 °C		-0.4	-0.68	-1	V
I_{DSS}	drain leakage current	V_{DS} = -12 V; V_{GS} = 0 V; T_j = 25 °C		-	-	-1	µA
I_{GSS}	gate leakage current	V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-10	µA
		V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	10	µA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-1	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	1	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -3.2 A; T_j = 25 °C		-	59	72	mΩ
		V_{GS} = -4.5 V; I_D = -3.2 A; T_j = 150 °C		-	80	98	mΩ
		V_{GS} = -2.5 V; I_D = -2.7 A; T_j = 25 °C		-	78	98	mΩ
		V_{GS} = -1.8 V; I_D = -0.4 A; T_j = 25 °C		-	120	200	mΩ
		V_{GS} = -1.5 V; I_D = -50 mA; T_j = 25 °C		-	198	450	mΩ
		V_{GS} = -1.2 V; I_D = -10 mA; T_j = 25 °C		-	880	-	mΩ
g_{fs}	forward transconductance	V_{DS} = -10 V; I_D = -2 A; T_j = 25 °C		-	9.4	-	S
R_G	gate resistance	f = 1 MHz		-	8.7	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = -6 V; I_D = -3.2 A; V_{GS} = -4.5 V; T_j = 25 °C		-	6.7	12	nC
Q_{GS}	gate-source charge			-	1	-	nC
Q_{GD}	gate-drain charge			-	1.9	-	nC
C_{iss}	input capacitance	V_{DS} = -6 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	634	-	pF
C_{oss}	output capacitance			-	167	-	pF
C_{rss}	reverse transfer capacitance			-	146	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -6 V; I_D = -3.2 A; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	6.2	-	ns
t_r	rise time			-	22	-	ns
$t_{d(off)}$	turn-off delay time			-	27	-	ns
t_f	fall time			-	17	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = -1 A; V_{GS} = 0 V; T_j = 25 °C		-	-0.7	-1.2	V



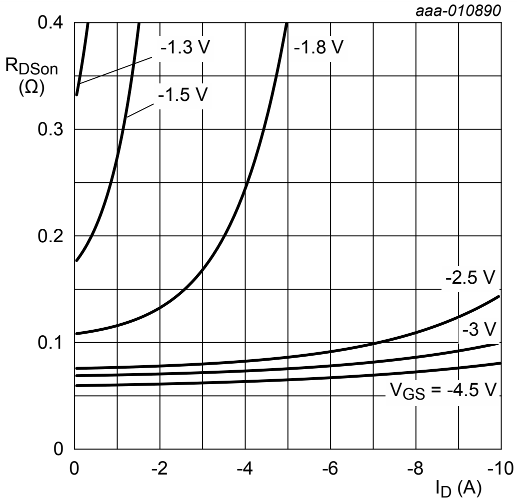
T_j = 25 °C

Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values



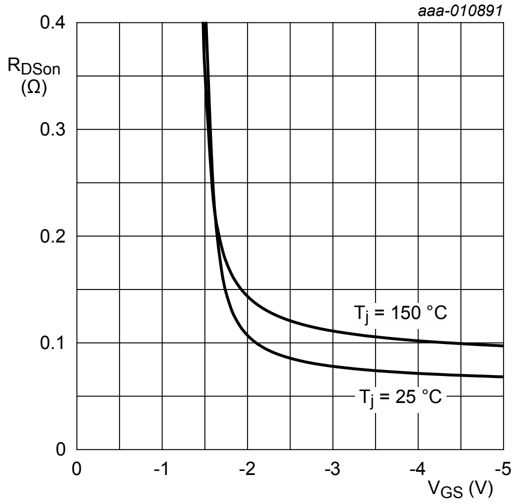
T_j = 25 °C; V_{DS} = -5 V

Fig. 8. Sub-threshold drain current as a function of gate-source voltage



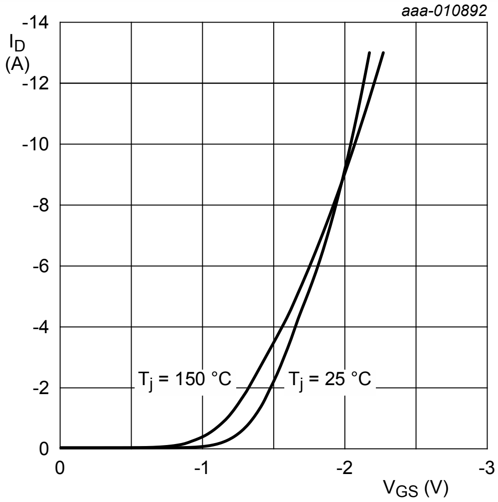
T_j = 25 °C

Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



I_D = -3.2 A

Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

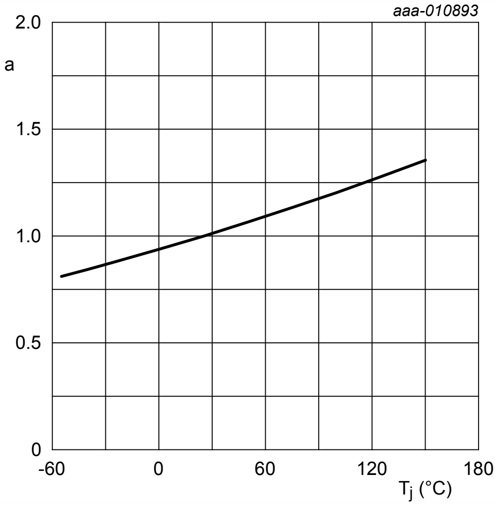
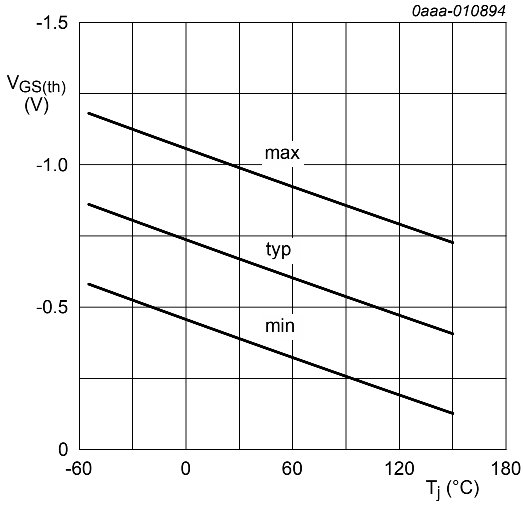


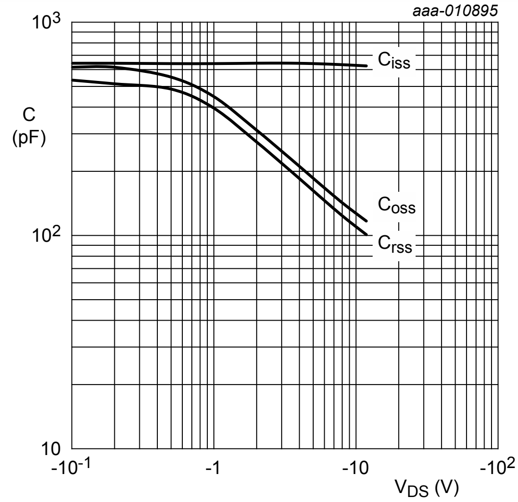
Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$



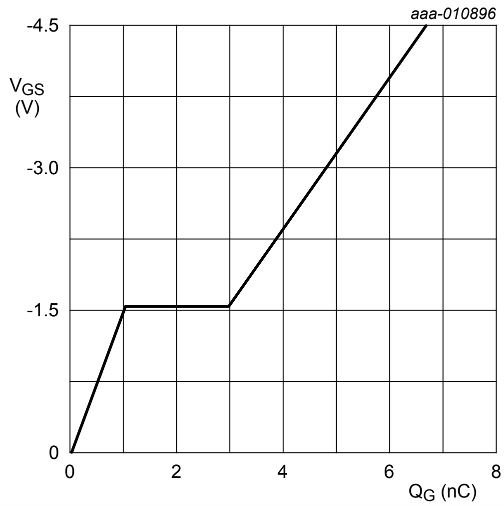
I_D = -0.25 mA; $V_{DS} = V_{GS}$

Fig. 13. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = -3.2 A; V_{DS} = -6 V; T_{amb} = 25 °C

Fig. 15. Gate-source voltage as a function of gate charge; typical values

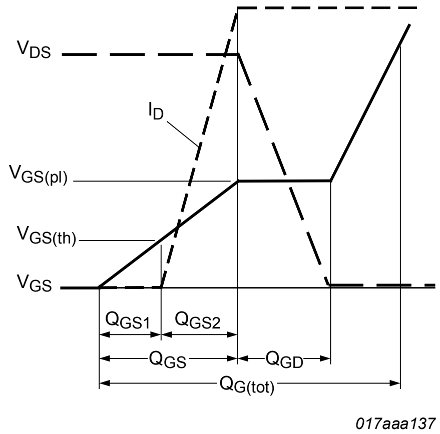
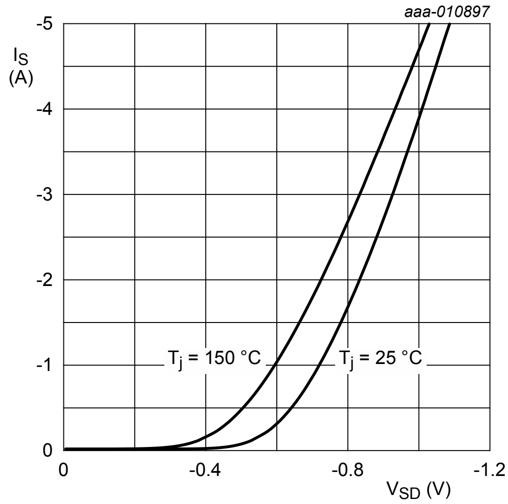


Fig. 16. MOSFET transistor: Gate charge waveform definitions



V_{GS} = 0 V

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

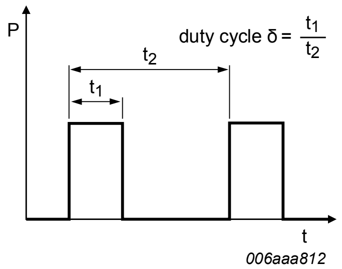
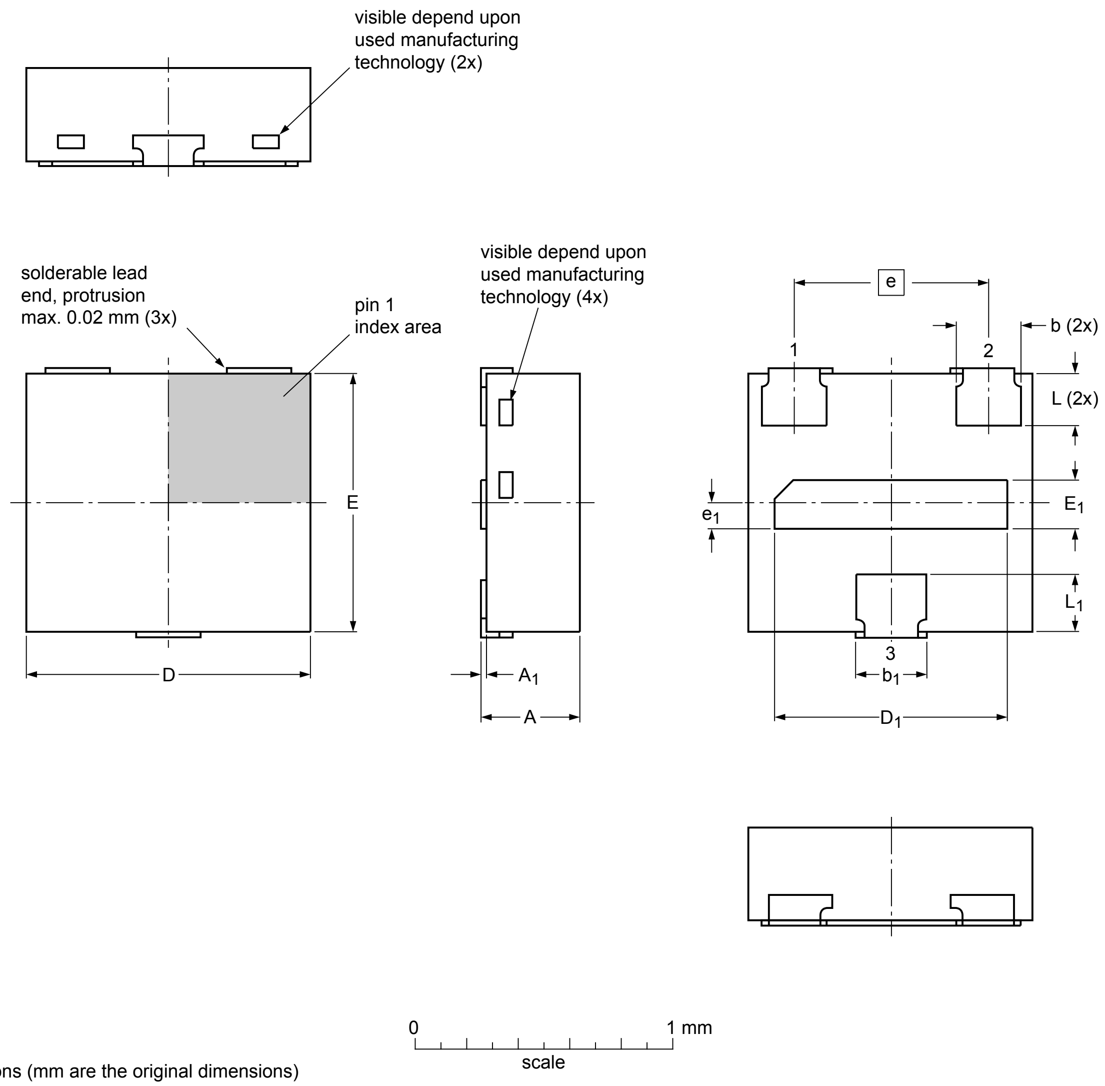


Fig. 18. Duty cycle definition

12. Package outline

DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1215



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_1	D	D_1	E	E_1	e	e_1	L	L_1
mm	min	0.34		0.22	0.245	1.05	0.87	0.95	0.16			0.17	0.195
	nom	0.37		0.25	0.275	1.10	0.90	1.00	0.19	0.75	0.1	0.20	0.225
	max	0.40	0.04	0.30	0.325	1.15	0.95	1.05	0.24			0.25	0.275

Note

1. Dimension A is including plating thickness.

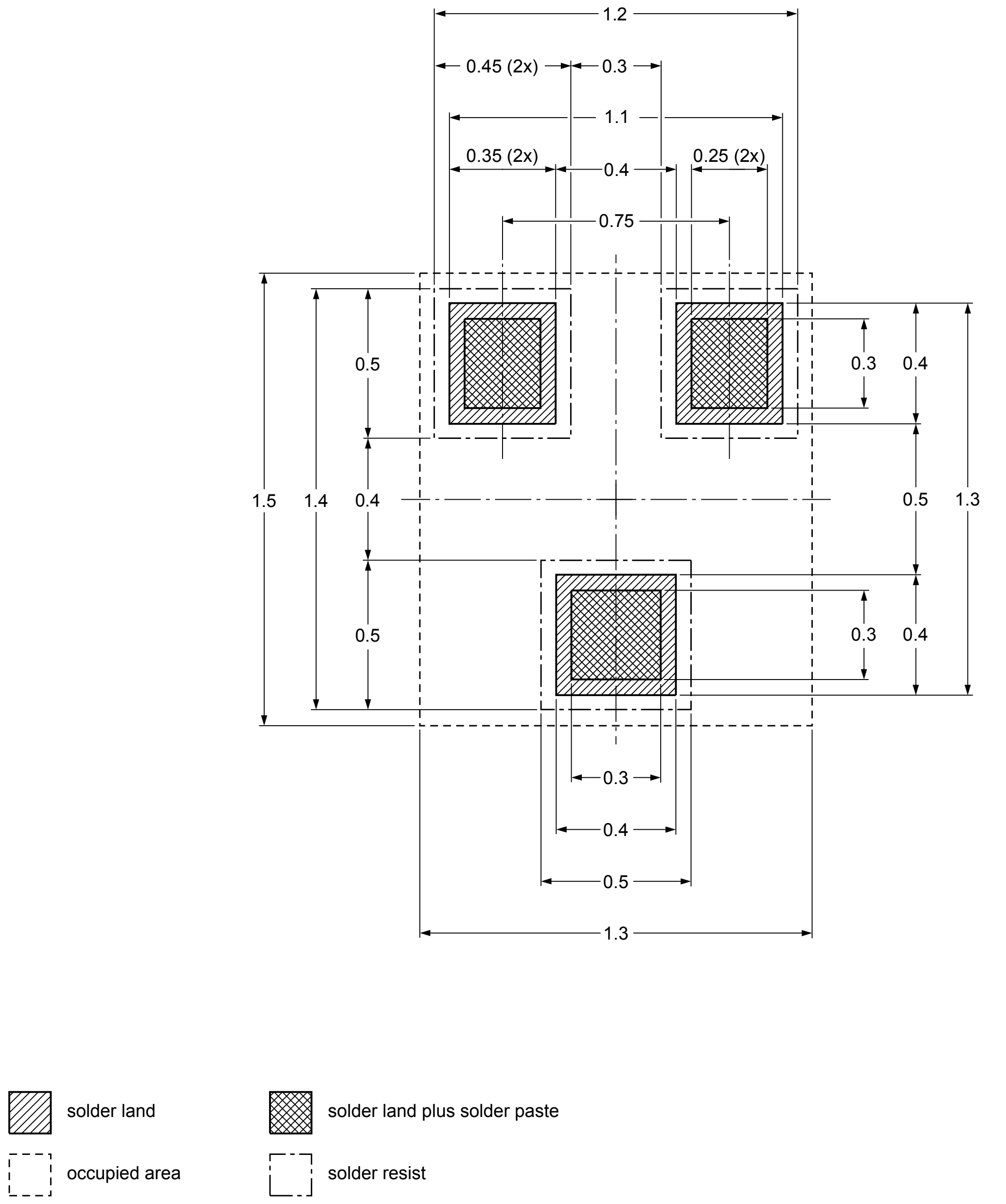
sot1215_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1215						~~13-03-05~~ 13-03-06

Fig. 19. Package outline DFN1010D-3 (SOT1215)

13. Soldering

Footprint information for reflow soldering of DFN1010D-3 package **SOT1215**



Dimensions in mm

Issue date ~~12-11-23~~ 13-03-06

sot1215_fr

Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB65UPE v.3	20140708	Product data sheet	-	PMXB65UPE v.2
Modifications:	• Product status changed			
PMXB65UPE v.2	20140218	Preliminary data sheet	-	PMXB65UPE v.1
PMXB65UPE v.1	20140204	Preliminary data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contents

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Date of release: 8 July 2014