

REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTOR

IRFE9130 JANTX2N6849U JANTXV2N6849U [REF:MIL-PRF-19500/564] 100V, P-CHANNEL

Product Summary

Part Number	BVDSS	RDS(on)	Id
IRFE9130	-100V	0.30Ω	-6.5A



The leadless chip carrier (LCC) package represents the logical next step in the continual evolution of surface mount technology. Designed to be a close replacement for the TO-39 package, the LCC will give designers the extra flexibility they need to increase circuit board density. International Rectifier has engineered the LCC package to meet the specific needs of the power market by increasing the size of the bottom source pad, thereby enhancing the thermal and electrical performance. The lid of the package is grounded to the source to reduce RF interference.

Features:

- Surface Mount
- Small Footprint
- Alternative to TO-39 Package
- Hermetically Sealed
- Dynamic dv/dt Rating
- Avalanche Energy Rating
- Simple Drive Requirements
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
Id @ VGS = -10V, TC = 25°C	Continuous Drain Current	-6.5	A
Id @ VGS = -10V, TC = 100°C	Continuous Drain Current	-4.1	
IDM	Pulsed Drain Current ①	25	
PD @ TC = 25°C	Max. Power Dissipation	25	W
	Linear Derating Factor	0.20	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	165	mJ
IAR	Avalanche Current ①	-	A
EAR	Repetitive Avalanche Energy ①	-	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-30	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Pckg. Mounting Surface Temp.	300 (for 5 S)	
	Weight	0.42(typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBVDSS/ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.10	—	V/°C	Reference to 25°C, I _D = -1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.30	Ω	V _{GS} = -10V, I _D = -4.1A④
		—	—	0.345		V _{GS} = -10V, I _D = -6.5A ④
VGS(th)	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
gfs	Forward Transconductance	1.9	—	—	S (τ)	V _{DS} > -15V, I _{DS} = -4.1A④
IDSS	Zero Gate Voltage Drain Current	—	—	-25	μA	V _{DS} = -80V, V _{GS} = 0V
		—	—	-250		V _{DS} = -80V V _{GS} = 0V, T _J = 125°C
IGSS	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
IGSS	Gate-to-Source Leakage Reverse	—	—	100	nA	V _{GS} = 20V
Qg	Total Gate Charge	—	—	35	nC	V _{GS} = -10V, I _D = -6.5A V _{DS} = -50V
Qgs	Gate-to-Source Charge	—	—	6.8		
Qgd	Gate-to-Drain ('Miller') Charge	—	—	23		
td(on)	Turn-On Delay Time	—	—	60	ns	V _{DD} = -50V, I _D = -6.5A, R _G = 7.5Ω
tr	Rise Time	—	—	140		
td(off)	Turn-Off Delay Time	—	—	140		
tf	Fall Time	—	—	140		
L _S + L _D	Total Inductance	—	—	—	nH	Measured from the center of drain pad to center of source pad
Ciss	Input Capacitance	—	790	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 1.0MHz
Coss	Output Capacitance	—	340	—		
Crss	Reverse Transfer Capacitance	—	71	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-6.5	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-25		
VSD	Diode Forward Voltage	—	—	-4.3	V	T _J = 25°C, I _S = -6.5A, V _{GS} = 0V ④
trr	Reverse Recovery Time	—	—	250	nS	T _J = 25°C, I _F = -6.5A, di/dt ≤ -100A/μs
QRR	Reverse Recovery Charge	—	—	3.0	μC	V _{DD} ≤ -50V ④
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction to Case	—	—	5.0	°C/W	Soldered to a copper clad PC board
R _{thJ-PCB}	Junction to PC Board	—	—	19		

For footnotes refer to the last page

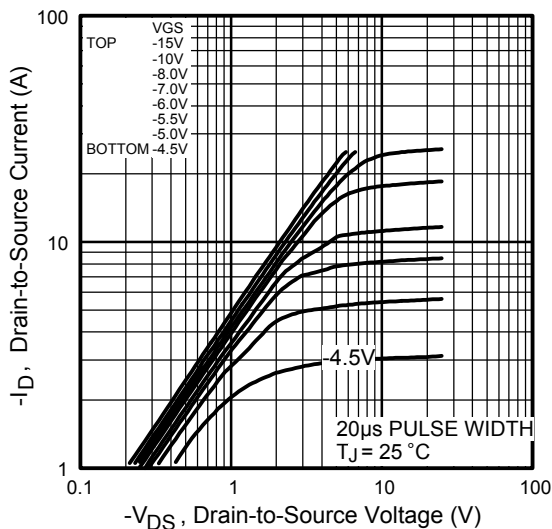


Fig 1. Typical Output Characteristics

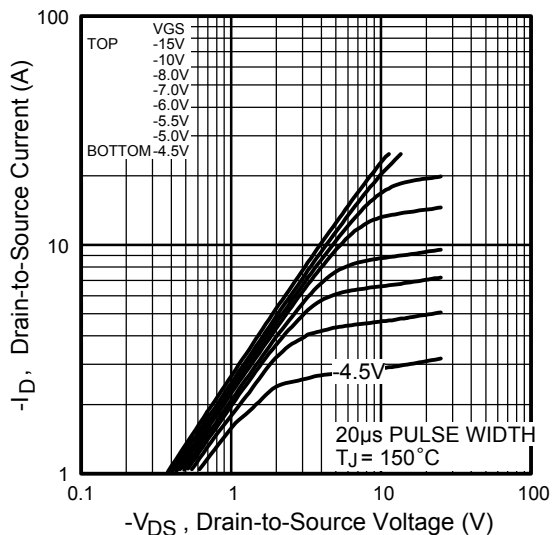


Fig 2. Typical Output Characteristics

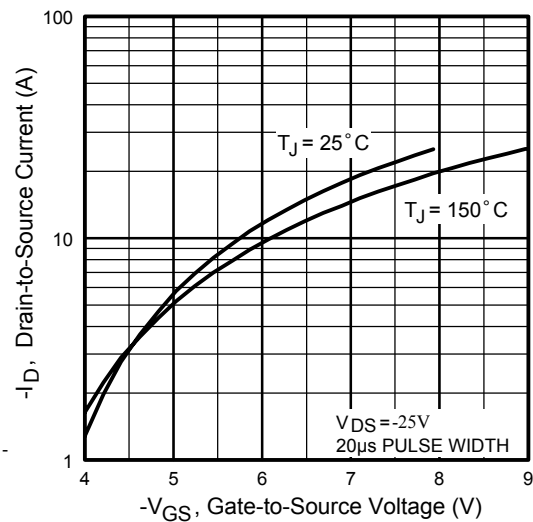


Fig 3. Typical Transfer Characteristics

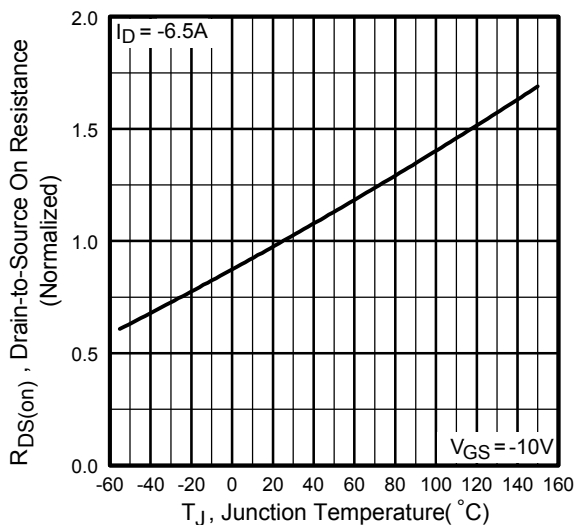


Fig 4. Normalized On-Resistance Vs. Temperature

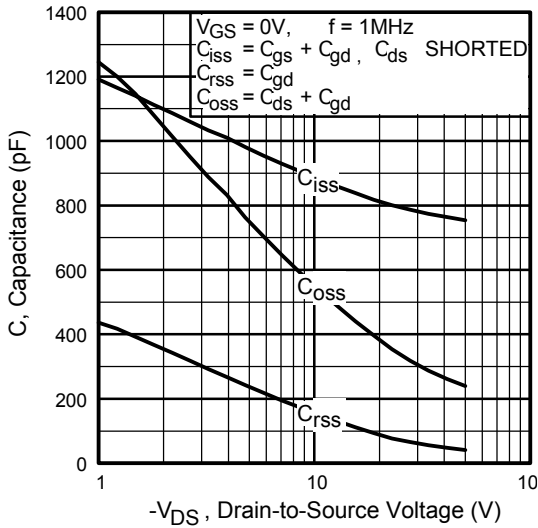


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

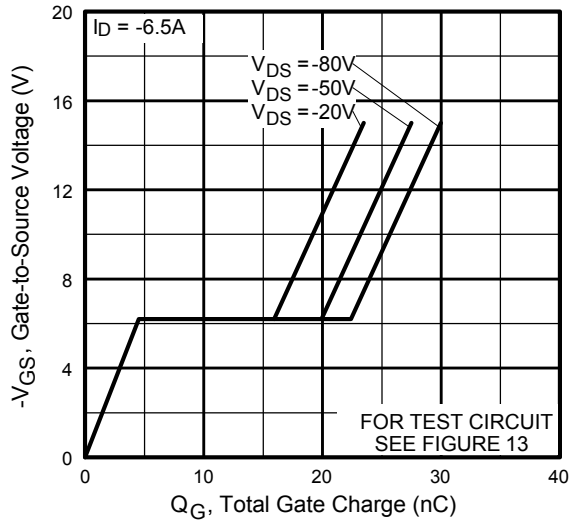


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

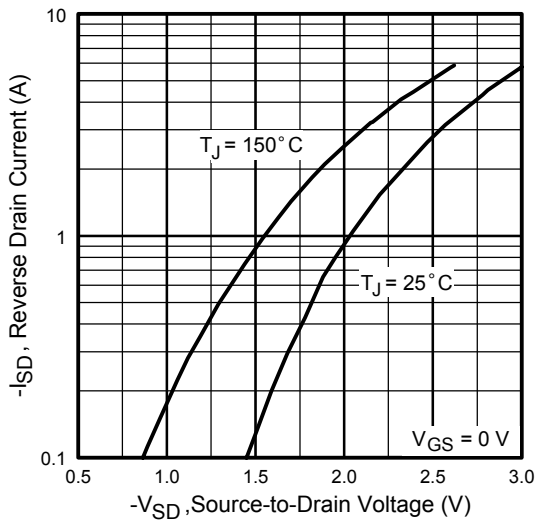


Fig 7. Typical Source-Drain Diode Forward Voltage

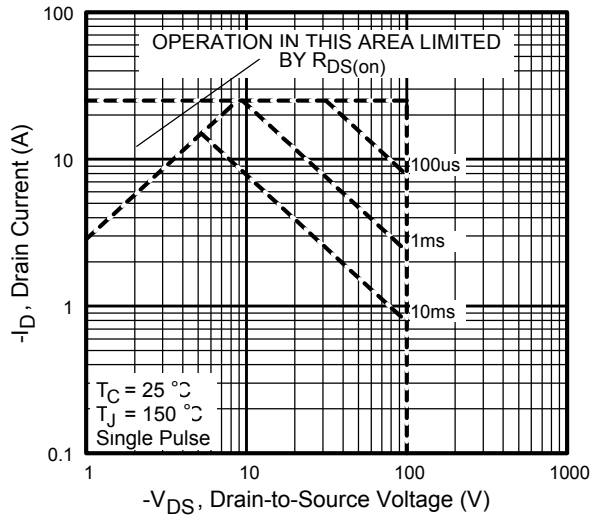


Fig 8. Maximum Safe Operating Area

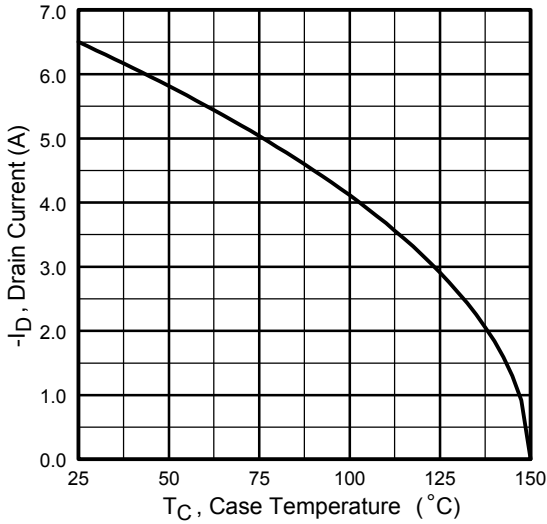


Fig 9. Maximum Drain Current Vs. Case Temperature

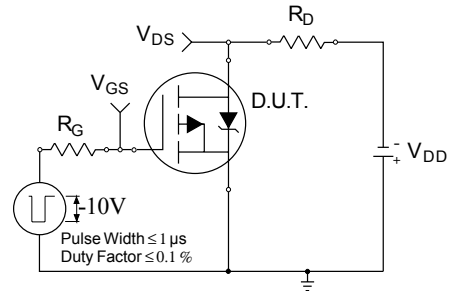


Fig 10a. Switching Time Test Circuit

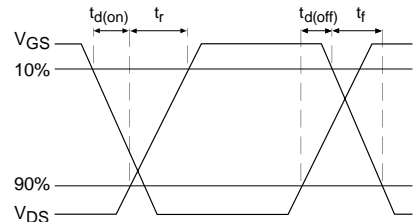


Fig 10b. Switching Time Waveforms

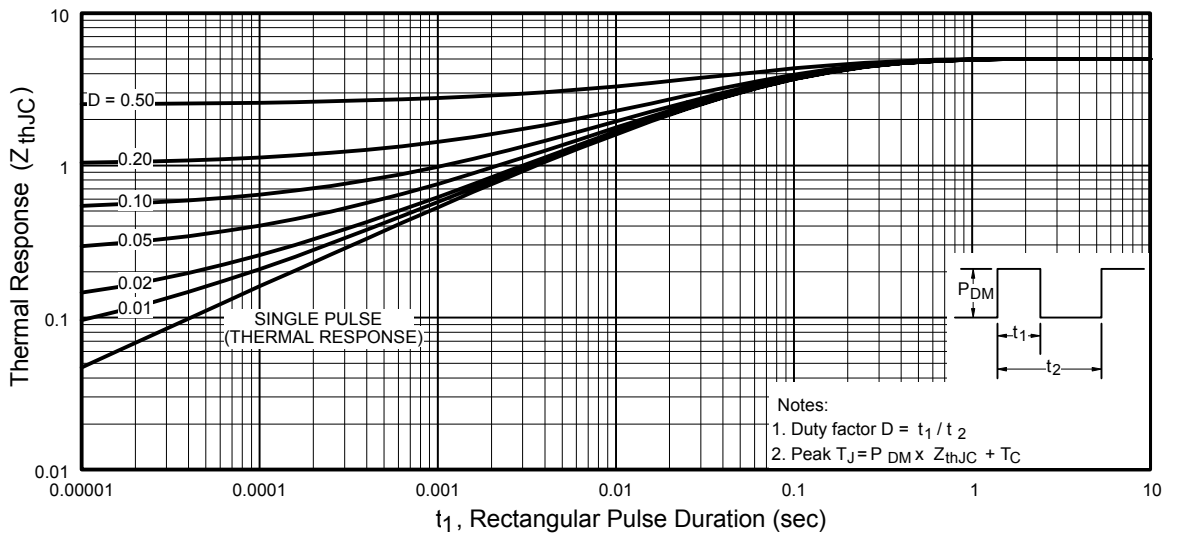


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

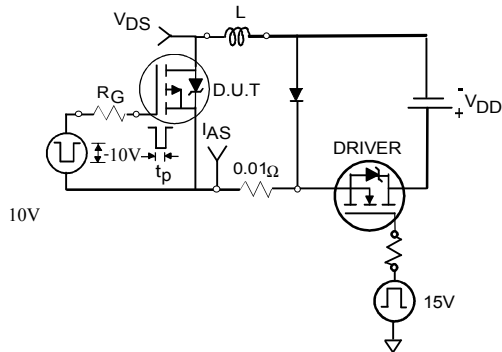


Fig 12a. Unclamped Inductive Test Circuit

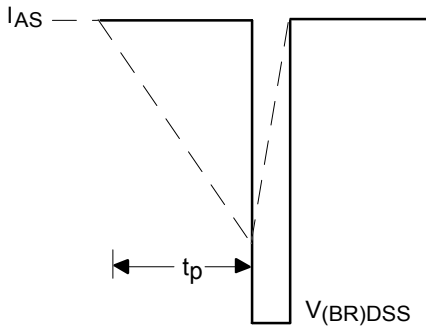


Fig 12b. Unclamped Inductive Waveforms

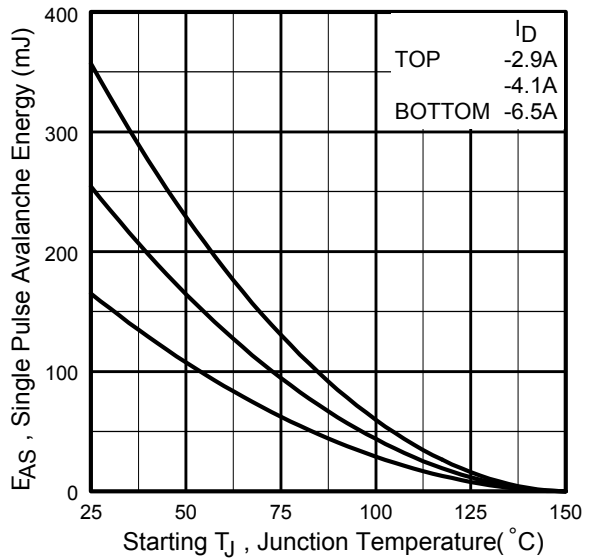


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

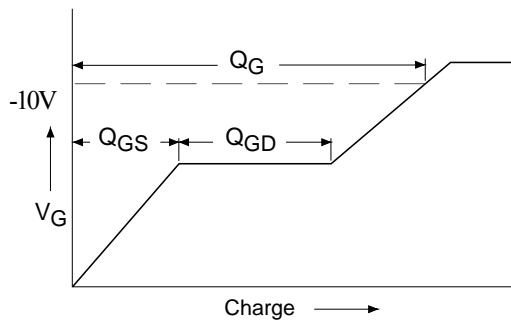


Fig 13a. Basic Gate Charge Waveform

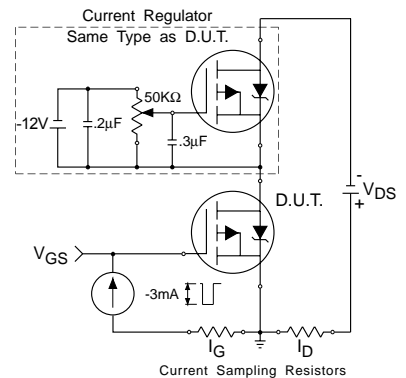
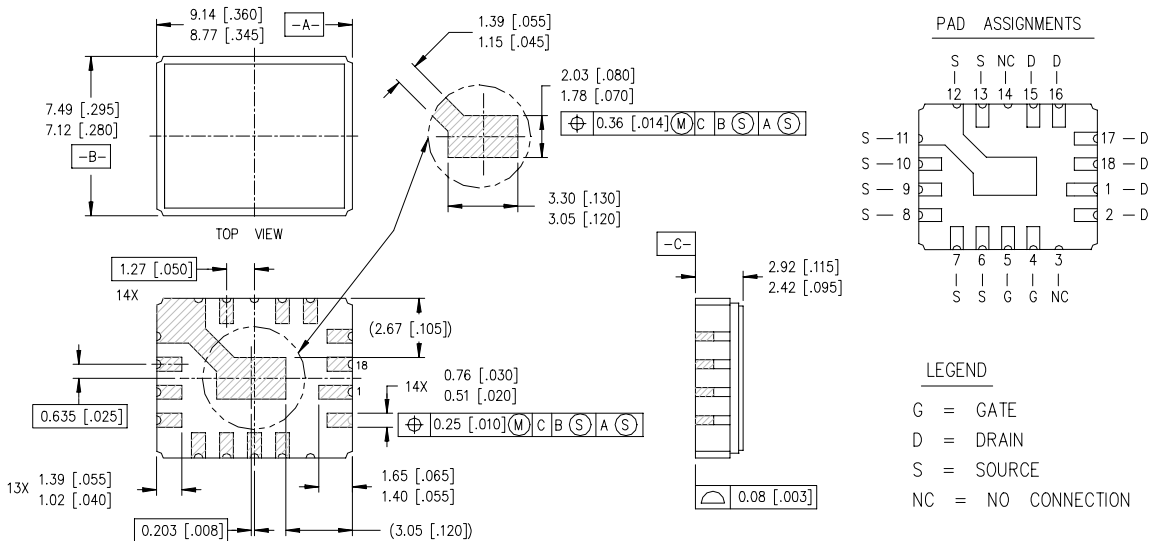


Fig 13b. Gate Charge Test Circuit

Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -25V$, starting $T_J = 25^{\circ}C$,
Peak $I_L = -6.5A$,
- ③ $I_{SD} \leq -6.5A$, $di/dt \leq -390A/\mu s$,
 $V_{DD} \leq -100V$, $T_J \leq 150^{\circ}C$
Suggested $R_G = 7.5 \Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — LCC-18



NOTES:

- 1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

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